

Natural Local Self-Boosting Effect in 3D NAND Flash Memory

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Abstract— This study examined the natural local self-boosting (NLSB) effect of an inhibited channel in three-dimensional (3D) NAND flash memory. The inhibited channel in the 3D NAND flash structure can be in the floating state easily because its channel is not connected directly to its substrate. Despite the application of the global self-boosted program-inhibit scheme, the selected WL cell is localized automatically during the program pulse application. This phenomenon is analyzed using a computer-aided design simulation, and an analytical model of boosted potential of an inhibited channel in 3D NAND flash memory is proposed.

Index Terms— 3D NAND flash memory, program inhibit string, self-boosted inhibit scheme, natural local self-booting (NLSB)

I. INTRODUCTION

THE growth of several major markets, such as mobile phones, flash memory cards, USB flash drives and solid-state drive continues to drive the explosive demand for NAND flash memory with high density and low power. Under these circumstances, 2D planar NAND flash technology should be scaled down aggressively. On the other hand, it has inherent limitations, such as cell-to-cell interference and prohibitive patterning. To overcome these limitations [1-3], 3D NAND flash technology had been introduced by stacking the memory cells vertically in a three-dimensional structure [4-8].

3D NAND flash memory has a different structure from 2D NAND flash memory, so new phenomena occur. In particular, the channel of the main cells in 3D NAND flash memory is based on the ultra-thin body (UTB) structure, which is not connected to the substrate [9]. Consequently, the channel can be in the floating state in some cases because the body bias cannot be applied to the channels of the main cells. For the first time, it was found that during program operation, the inhibited channel becomes a floating node and the natural local self-boosting (NLSB) effect occurs. The NLSB effect allows a sufficiently high boosted potential of an inhibited string to be achieved without a local self-boosted program-inhibit (SBPI) scheme, even if the number of stacks increases. This phenomenon was analyzed and a predictive modeling was

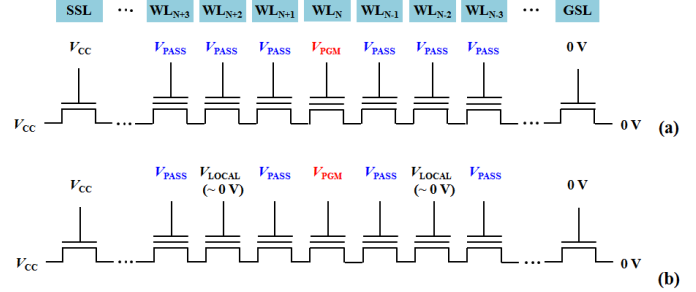


Fig. 1. Bias conditions of SBPI schemes. (a) global SBPI scheme. (b) local SBPI scheme.

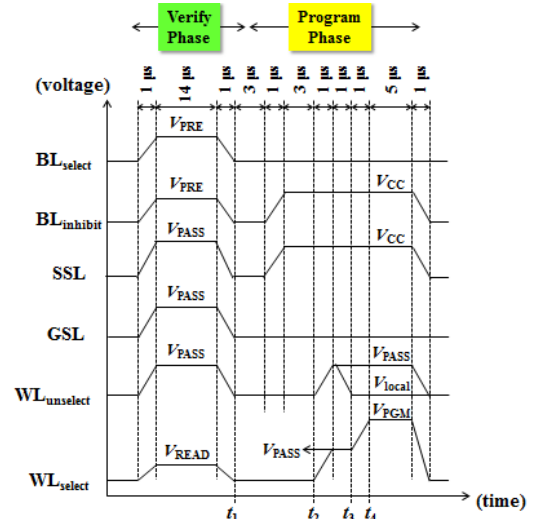


Fig. 2. Timing diagram of the self-boosted inhibit scheme. ($V_{\text{READ}} = V_{\text{PASS}} = 6 \text{ V}$, $V_{\text{PGM}} = 18 \text{ V}$)

performed using the technology computer-aided design (TCAD) simulation (ATLAS SilvacoTM).

II. NATURAL LOCAL SELF-BOOSTING EFFECT

During the program operation in NAND flash memory, the cells share the high program voltage (V_{PGM}) on the selected word line (WL_N), but the program operation should be bit selective. To achieve this selectivity, the channel potential of the unselected cells needs to be raised to reduce the voltage between the channel and the gate. For this purpose, the SBPI scheme has been used, as shown in the Fig. 1 [10]. By charging the string-select lines (SSLs) and inhibit-bit lines (BL_{inhibit}) to the voltage of the V_{CC} , the SSL transistors are turned off because the channel potential is higher than $V_{\text{CC}} - V_{\text{th,SSL}}$. (Here, $V_{\text{th,SSL}}$ is the threshold voltage of the SSL transistor.). At this point, the channel of the inhibit string becomes a floating node. By increasing the word line potential, the channel potential is boosted by the coupled capacitance networks [11]. The self-boosted program inhibit scheme can be divided in two

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TABLE I
DEVICE PARAMETERS USED IN THE SIMULATION

Quantity	Value
Gate length (main cells)	40 nm
Gate length (SSL, GSL)	150 nm
Gate spacing	30 nm
Gate dielectrics (O/N/O)	4/8/8 nm
Channel hole diameter (3D NAND)	80 nm
Poly-Si channel thickness (3D NAND)	10 nm
Selected WL (WL _{select})	WL8
Lower cells' states (WL0/WL1/.../WL7)	E/P3/P2/P1/E/P1/P2/P3/E
V _{CC}	2.4 V

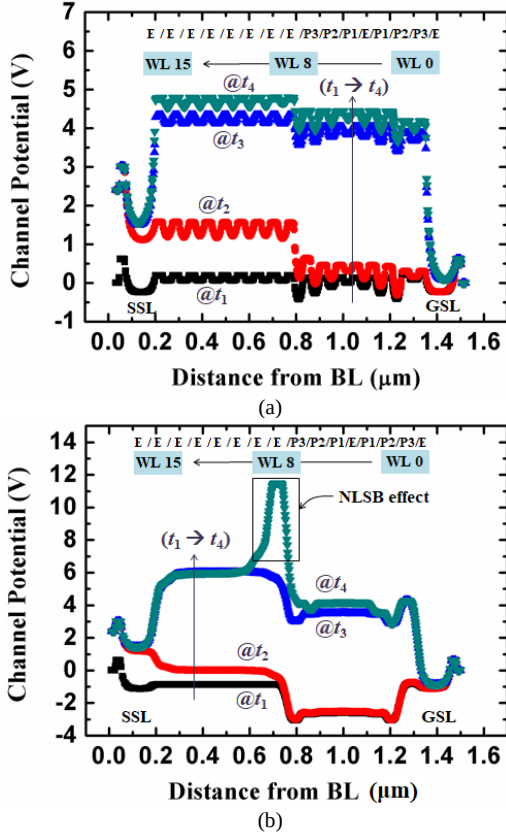


Fig. 3. Comparison of the channel potential change by the global SBPI scheme in (a) 2D NAND flash memory and (b) 3D NAND flash memory

types. The first is the global SBPI scheme, as shown in Fig. 1(a). The pass voltage (V_{PASS}) is applied to all unselect word lines.

The boosted potential of the global SBPI scheme can be modeled as follows:

$$\Delta V_{ch} = \frac{C_{WL-CH}}{N \cdot C_{total}} \cdot (N-1) \cdot V_{PASS} + \frac{C_{WL-CH}}{N \cdot C_{total}} \cdot V_{PGM} \quad (1)$$

where C_{WL-CH} is the capacitance between the channel and the gate; C_{total} is the total unit cell capacitance including other parasitic components, such as the substrate and neighboring channels; and N is the total number of WLs in a single string. The global SBPI scheme has the disadvantage that boosting the efficiency decreases with increasing the number of WLs increases. In particular, the boosting effect by V_{PGM} (the second term in Eq. (1)) is reduced significantly. As the number of WLs in a BL string has increased from 16 to 64 and now to 128 in recent nodes for higher density, the local SBPI scheme was

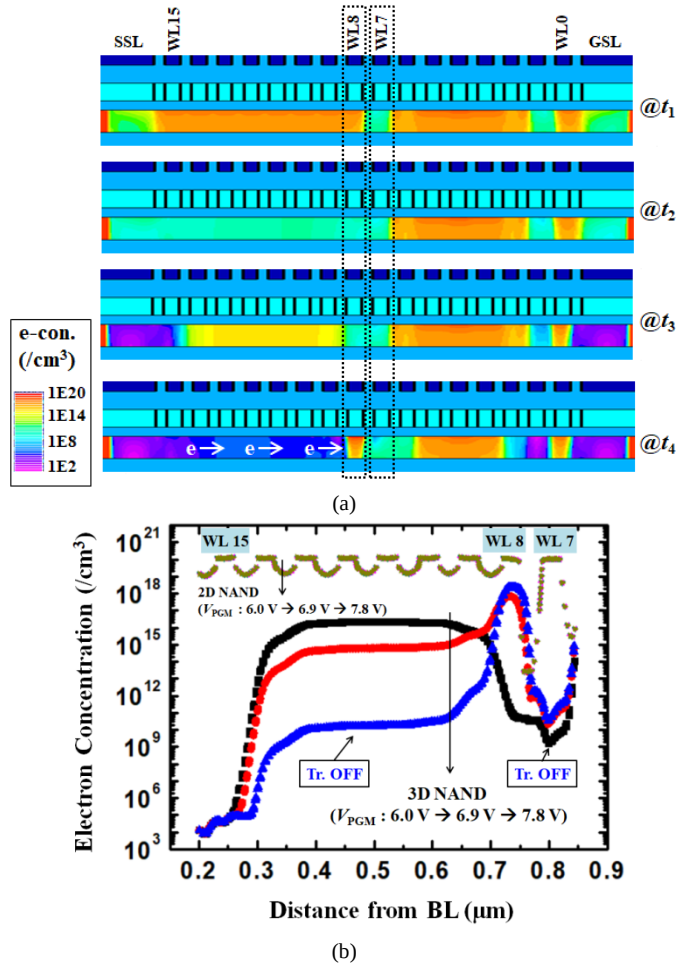


Fig. 4. (a) The change of electron distribution during the program operation in inhibited string (color online) (b) comparison of channel-electron concentration between 2D NAND and 3D NAND

introduced, as shown in Fig. 1(b) [12]. With the local SBPI scheme, the channel of the program-inhibited cell is isolated from its full string channel by lowering the voltages of the adjacent WLs from V_{PASS} to V_{local} before V_{PGM} is applied. Consequently, the boosted potential of the local SBPI scheme can be expressed as

$$\Delta V_{ch} = \frac{C_{WL-CH}}{N \cdot C_{total}} \cdot (N-1) \cdot V_{PASS} + \frac{C_{WL-CH}}{M \cdot C_{total}} \cdot V_{PGM} \quad (2)$$

where M is the number of isolated WLs by V_{local} . (In the case of Fig. 1(b), $M = 3$)

A TCAD simulation was performed to analyze the SBPI characteristics of the 2D NAND and 3D NAND flash memories. Table I lists the device parameters used in the TCAD simulation. A full NAND string with 16 WLs, a GSL (ground-select line) and a SSL was constructed. The specific structure was the same as that in previous work (Fig.1 of [9]). And, the threshold voltages of each state were as follows: $V_{th,E} = -1$ V, $V_{th,P1} = 1$ V, $V_{th,P2} = 2$ V, and $V_{th,P3} = 3$ V. The threshold voltage was obtained by adjusting the charge amount at the storage node of the corresponding cell. Fig. 2 shows the timing diagram used for the verification and program sequence simulation.

Fig. 3 presents the change in the channel potential when the global SBPI is applied. In the case of 2D NAND flash memory, the entire channel was charge-shared and boosted to approximately 4.6 V, as shown in Fig. 3(a). In the case of 3D NAND flash memory, however, the channel of the selected WL cell was boosted locally to approximately 11.7 V. Interestingly, although the global SBPI was applied, a local SBPI effect occurred, which was called the natural local self-boosting effect (NLSB effect).

As illustrated in Fig. 4(a), the mechanism of the NLSB effect was analyzed by observing the changes in channel-electron concentration during the following phases ($t_1 \rightarrow t_2 \rightarrow t_3 \rightarrow t_4$).

(t_1): After the verification, WL7 cell is turned off and its channel potential falls to -3 V due to the DCP effect [9].

(t_2): During the charging the SSL and BL, the upper WL cells with erase state (WL8 ~ WL15) are precharged. Instead, the lower cells (WL0 ~ WL7) remain unchanged because the WL7 cell isolate the upper channels.

(t_3): As the V_{PASS} is applied to all the WLs, electrons are supplied to the upper WL cells and their channel potentials are boosted by capacitive coupling. At this time, the channel potential of WL7 cell is boosted according to the V_{PASS} while maintaining the turned-off state because it is a floating channel without reference body voltage.

(t_4): When V_{PGM} was applied, the channel electrons of the neighboring cells moved to the selected WL cell by the potential difference. At this time, the upper cells were left in the off state because the 3D NAND flash structure has no N^+ region or body contact to supply electrons. Therefore, the channel of the selected WL cell was localized automatically.

Fig. 4(b) shows that after $V_{PGM} = 7.8$ V, the electron concentration of the neighboring channels becomes $10^{10}/\text{cm}^3$ (intrinsic carrier concentration level), and the selected cell becomes perfectly localized. Subsequently, the boosting by V_{PGM} rise occurs only in the channel of the selected WL cell. On the other hand, 2D NAND flash structure maintains the electron concentration constant as much as the voltage corresponding to each overdrive voltage ($V_{WL} - V_{th,cell}$) since all cells have the reference body voltage.

III. MODELING

Considering the NLSB effect in the 3D NAND flash memory, the potential boosted by the global SBPI scheme in 3D NAND flash memory can be modeled as follows:

$$\Delta V_{ch,selected\ WL} = \frac{C_{WL-CH}}{C_{total}} \cdot V_{PASS} + \frac{C_{WL-CH}}{C_{total}} \cdot (V_{PGM} - V_{PASS}) \cdot \alpha \quad (3)$$

The first term represents the amount of voltage boosted by V_{PASS} before the NLSB effect occurs. The second term refers to the amount of voltage boosted by the NLSB effect when V_{PGM} is applied. α is a correction parameter to consider the effective coupling ratio of V_{PGM} . The coupling strength by V_{PGM} is weaker than V_{PASS} because the entire channel of the upper WL cells is affected by the V_{PGM} of only one selected WL until the selected WL cell is completely isolated.

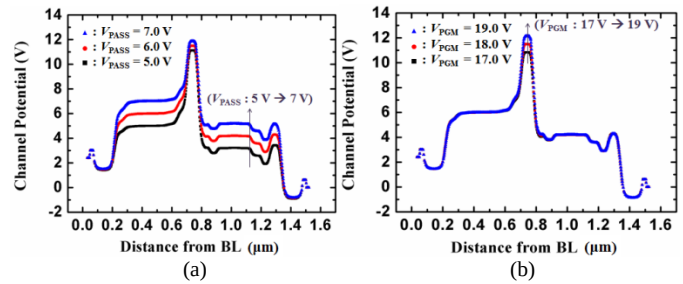


Fig. 5. Comparison of the inhibited-channel potential in 3D NAND flash memory for (a) different V_{PASS} and (b) different V_{PGM} .

On the other hand, the boosted channel potential of the unselected WLs can be expressed as

$$\Delta V_{ch,unselected\ WL} = \frac{C_{WL-CH}}{C_{total}} \cdot V_{PASS} \quad (4)$$

The channel potential of the inhibited string of the unselected WL is determined solely by V_{PASS} due to the NLSB effect. To verify this modeling, the boosted channel potentials according to V_{PGM} and V_{PASS} were simulated through a TCAD simulation. As shown in Fig. 5(a), the channel potential of the unselected WL cell is proportional to V_{PASS} . In addition, the simulation results showed that the correction parameter α is approximately 0.7. On the other hand, Fig. 5(b) shows that only the channel potential of the selected WL cell increases with V_{PGM} . These simulation results are in good agreement with the modeling data.

Through the analysis of the NLSB effect in 3D NAND flash memory, the following two points can be expected regarding the future development of 3D NAND flash memory. As the number of WL stacks increases for higher density, the program disturbance due to the degradation of boosting potential in inhibited strings will not deteriorate. Instead, 3D NAND flash memory will require new schemes to solve the problem due to the high electric field concentrated on the selected WL cell by the NLSB effect.

IV. CONCLUSION

A new phenomenon called the NLSB effect was observed in 3D NAND flash memory. Its physical mechanisms and characteristics were analyzed using a TCAD simulation. Even if the number of layers is increased in the 3D NAND flash memory, the boosted potential of the inhibit channel can be controlled by the global SBPI scheme instead of the local SBPI scheme. In addition, the obtained model can be used to optimize the operation voltages in 3D NAND flash memory.

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