

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: November 10, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00190
U.S. Patent No. 11,568,941

PATENT OWNER'S RESPONSE

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2027	Youngseok Jeong, <i>Hot Carrier Injection Phenomenon due to Excessive Natural Local Self-Boosting Effect in 3D NAND Flash Memory</i> , Extended Abstracts 2019 Int’l Conf. on Solid State Devices & Materials 685 (2019) (“Jeong”)
2028	Declaration of Dr. Sunil P. Khatri, Ph.D. in Support of Patent Owner’s Response (“Khatri2”)

I. Introduction

Petitioner fails to carry its burden to show any challenged claim of U.S. Patent No. 11,568,941 (“’941 Patent”) unpatentable. The claims require a *vertically* arranged three-dimensional memory with wordlines arranged “from bottom to top,” shown in Figure 8.

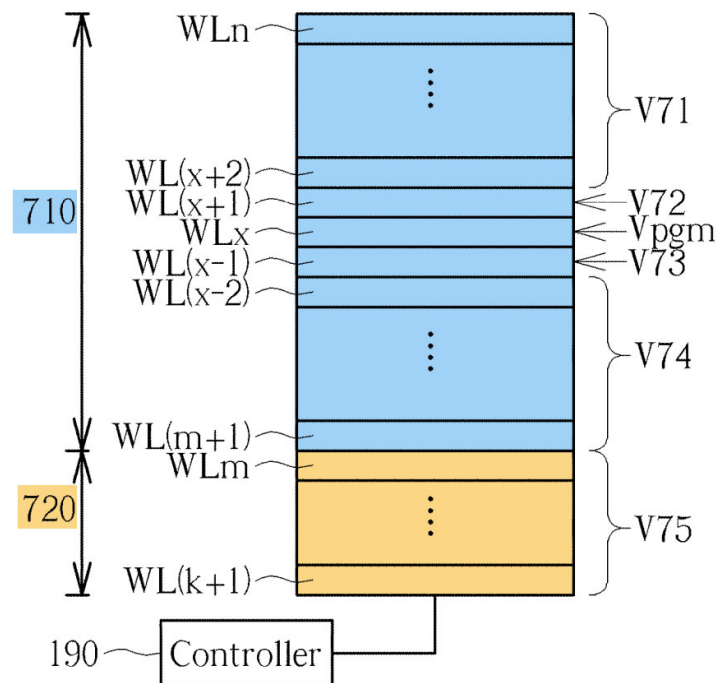
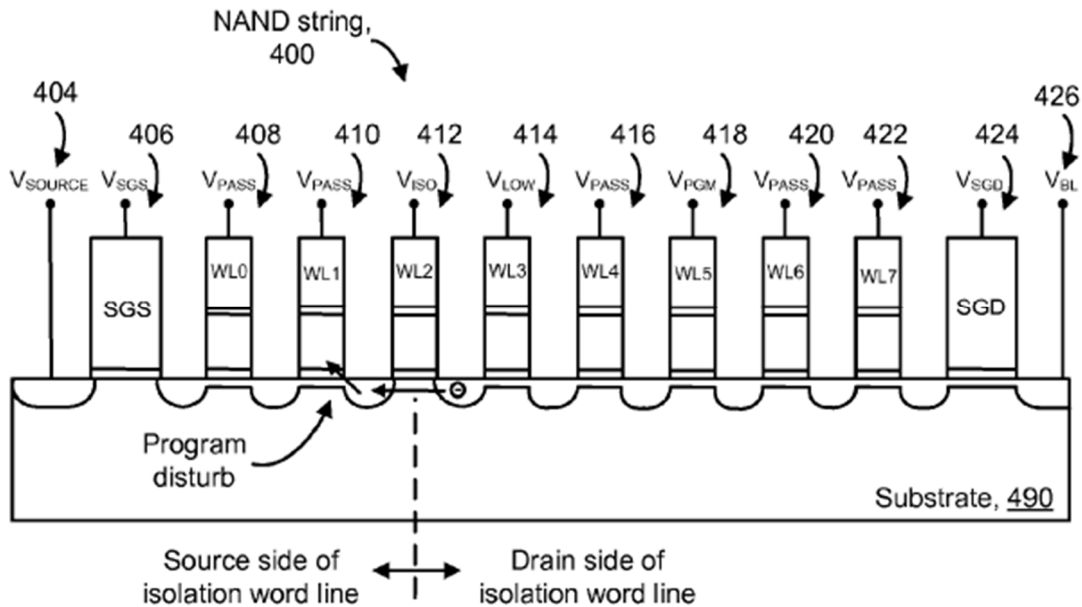


FIG. 8

Ex. 1001, Fig. 8.¹ Petitioner's four grounds hinge on Dong. But Dong discloses two-dimensional NAND with wordlines arranged horizontally as shown below in Figure 4, not vertically “from bottom to top.”

¹ Annotations are added to figures and text unless stated otherwise.



Dong, Fig. 4.

Yet Petitioner tries to map Dong's horizontal 2D scheme onto claims directed to vertically arranged 3D wordlines by (1) rewriting "from bottom to top" as from "source end" to "drain end," contrary to intrinsic evidence, (2) misreading Dong's voltage charts as depicting physical structure, and (3) invoking a passing "three dimensional" remark in Dong to apply Dong's 2D program-phase voltages in a vertical 3D NAND context. None work. And Petitioner identifies no teaching to transplant Dong's 2D voltage scheme into a vertical 3D NAND context—Ppetitioner *does not even contend* that it would have been obvious to do so. But even if Petitioner did, a POSITA would not have been motivated to make that change due to key structural and electrical differences between 2D and 3D NAND that impact program disturb mechanisms.

Petitioner's reliance on Costa (Ground 3) conflates verify/read activity with a program operation. Costa concerns a read/verify phase that checks already-programmed cells, not the program operation that actually programs those cells. Realizing this deficiency, Petitioner's expert injected during deposition a new construction for "a program operation" broad enough to include Costa's verification phase—new argument not in the Petition. Nor does the Petition contain any explanation for why the prior art would meet the claims under this new construction. It would not; this new argument fails too.

Petitioner's Shirai combination (Ground 4) applies $V_{\text{PASS-LOW}}$ to the entire lower deck, which a POSITA would not have done because of specific disturb considerations in vertical 3D NAND. Petitioner's modification is also fatally flawed for changing the values of variables (e.g., "k") it identified for independent claims.

In short, Petitioner never overcomes its core defect: Dong is horizontal; the claims are vertical. Neither Costa nor Shirai supplies the missing program-operation voltage scheme across vertically arranged wordlines as claimed. Petitioner's combinations rest on conclusory assertions, shifting reads, and claim-rewrites.

The Board should find each challenged claim patentable.

II. Background

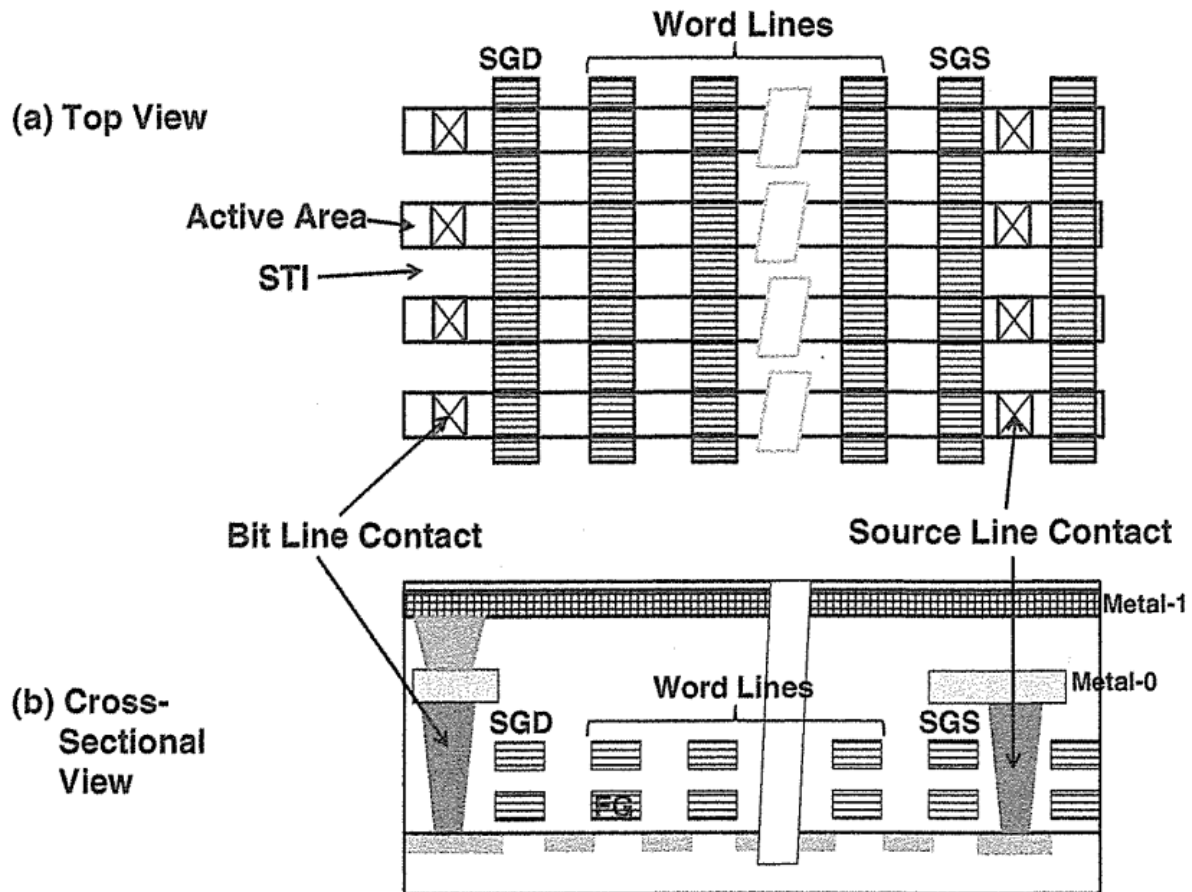
A. Technical Background

NAND arrays are controlled by wordlines; during a program operation the controller applies a program voltage (V_{PGM}) to the selected wordline and pass/isolation voltages to unselected wordline (i.e., a “**program phase**”).² Ex. 2028 (“Khatri2”), ¶¶48-64; *see, e.g.*, Ex. 1005 (“Dong”), Fig. 5a. Program disturb occurs when an unselected memory cell is unintentionally programmed during a program operation of the selected memory cell. Ex. 1009, 52 (“Program disturb is a phenomenon in which the threshold voltage (V_t) of unselected cell is increased during program operation.”); Khatri2, ¶63. By contrast, read disturb occurs during verify/read activity when a sensing/read voltage is applied to confirm the result of programming (i.e., a “**verify phase**”). *See, e.g.*, Ex. 1012 (“Costa”), Fig. 9A; Ex. 1010, 280 (“Read disturb is a phenomenon in NAND flash memory where reading data from a flash cell can cause the threshold voltages of other (unread) cells in the same block to shift to a higher value.”); Ex. 2020, 33-34; Khatri2, ¶64.

1. Two-Dimensional (2D) or Planar NAND

In 2D or Planar NAND, wordlines and select gates (source and drain) are arranged horizontally on the substrate, as seen below.

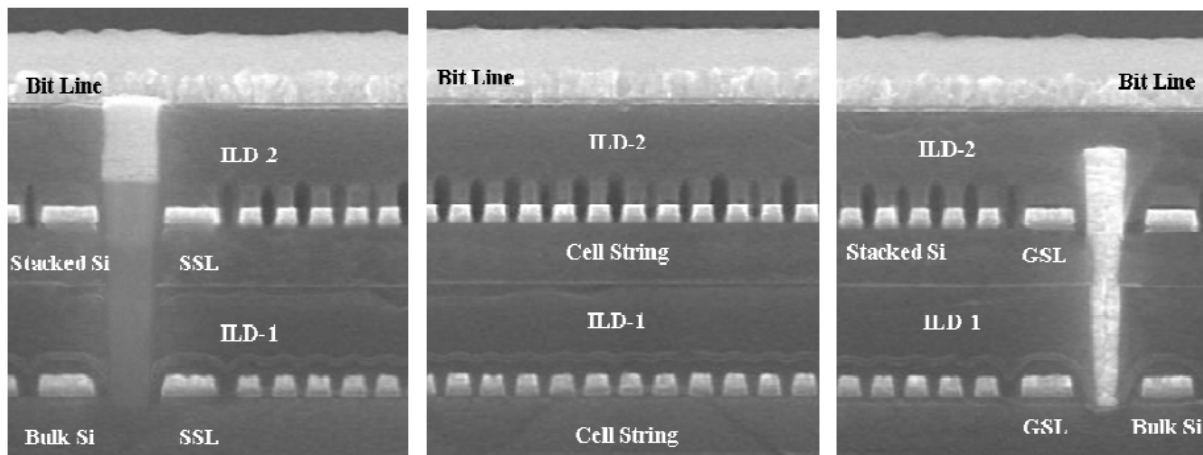
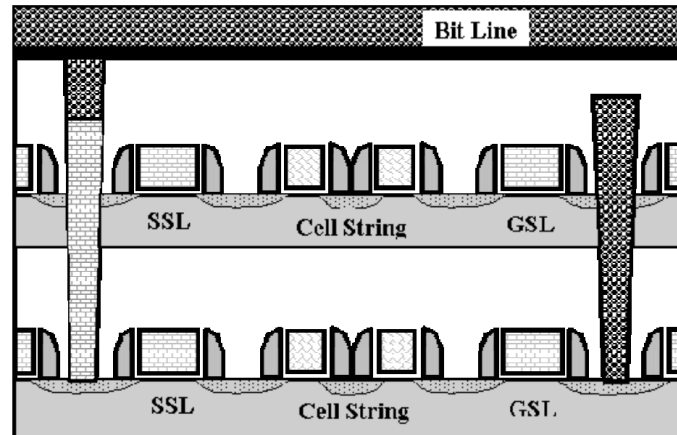
² For consistency, Patent Owner uses “wordline” instead of “word line.”



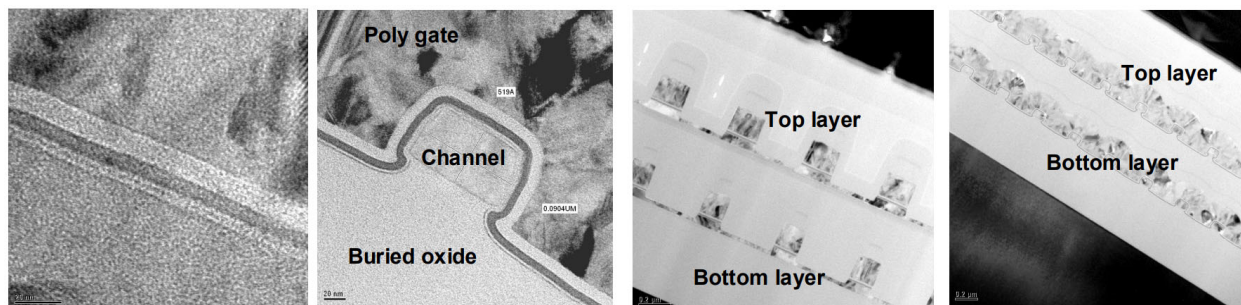
Ex. 1009, 38-40, Fig. 2.3; Khatri2, ¶¶65. However, the scaling of 2D NAND flash memory faced many limitations, including program disturb, resulting in “major scaling limitations.” Ex. 1009, 150; Khatri2, ¶¶65.

2. Three-Dimensional (3D) NAND At The Time Of Dong Included Stacked 2D NAND

To further scale NAND flash memory, some initial 3D NAND designs were available at the time of Dong. *See* Dong. Early “Stacked” and “Multi-layer Thin-Film Transistor (TFT)” approaches layered traditional 2D NAND strings; even though there are multiple layers, each layer’s wordlines are still arranged horizontally, rather than vertically. Khatri2, ¶¶66-69.



Ex. 2008, 3, Figs. 3, 4 (showing diagram and physical representations of Stacked NAND).



Ex. 2009, 4 (depicting Multi-layer TFT NAND using two two-dimensional NAND

layers (“bottom” and “top” layers) with wordlines (“channel[s]”) arranged horizontally on a substrate).

The 2D NAND-based Stacked and Multi-layer NAND designs are not the same as vertical 3D NAND as recited in the '941 Patent because the cells are not arranged vertically “from bottom to top.” Khatri2, ¶70. Moreover, “[t]he program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed.” Ex. 1009, 354; Khatri2, ¶¶70-83.

B. The '941 Patent (Ex. 1001)

The '941 Patent claims priority to February 10, 2020 and discloses and claims “a solution for reducing program disturbance and pass voltage disturbance when operating a three-dimensional memory.” Ex. 1001, 1:39-41, 1:19-22; Khatri2, ¶84. As memory cells or wordlines are in closer proximity in vertical three-dimensional NAND and “the number of layers is increased,” pass voltage occurs and program disturbance “become[s] more significant,” resulting in “a higher failure rate of programming.” Ex. 1001, 1:30-41; Khatri2, ¶84. By calibrating voltages to specific wordlines of the 3D NAND memory while programming the selected wordline, the '941 Patent reduces program disturbance and pass voltage disturbance on unselected wordlines. Ex. 1001, 6:39-41; Khatri2, ¶84.

Figure 8 illustrates a 3D memory with two vertically arranged portions: a “first portion 710” (blue) above a “second portion 720” (orange). Ex. 1001, 4:29-34; Khatri2, ¶85. Each portion includes wordlines arranged “from bottom to top.” Ex. 1001, 4:34-36; *see also id.*, 6:55-60 (cl. 1), 7:23-28 (cl. 5), 8:15-20 (cl. 11).

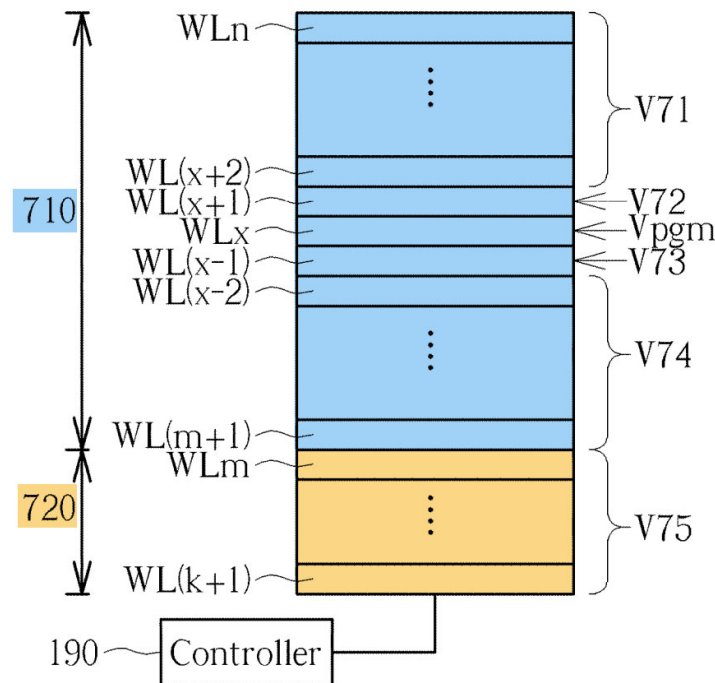


FIG. 8

Ex. 1001, Fig. 8. A POSITA would understand, in light of the intrinsic evidence, that the three-dimensional memory of the '941 Patent has a substrate located below and perpendicular to the vertical arrangement of wordlines. Khatri2, ¶85.

During programming of the xth wordline (i.e., “WL_x”), controller 190 applies V_{PGM} to WL_x and other voltages V71, V72, V73, V74, and V75 to unselected wordlines to reduce the effect of program and pass voltage disturbances. Ex. 1001, 1:30-41, 3:9-11, 4:37-61, 6:39-43, Fig. 8. The '941 Patent also discloses that the

fifth voltage V75 can be lower than the fourth voltage V74. *Id.*, 4:60-61; Khatri2, ¶86.

C. Prosecution History

The Examiner allowed the '941 Patent stating that “there is no teaching, suggestion or motivation for combination in the prior art” that discloses the recited limitations of independent claims 1, 5, and 11, and recognizing allowable subject matter in dependent claims 2-4, 6-10, and 12-14. Ex. 1002, 378-82, 379-80; Khatri2, ¶¶87-88.

D. Person of Ordinary Skill in the Art

YMTC does not dispute Petitioner's definition of a POSITA for purposes of these proceedings. Pet. 22-23; Khatri2, ¶¶42-47.

E. Challenged Claims

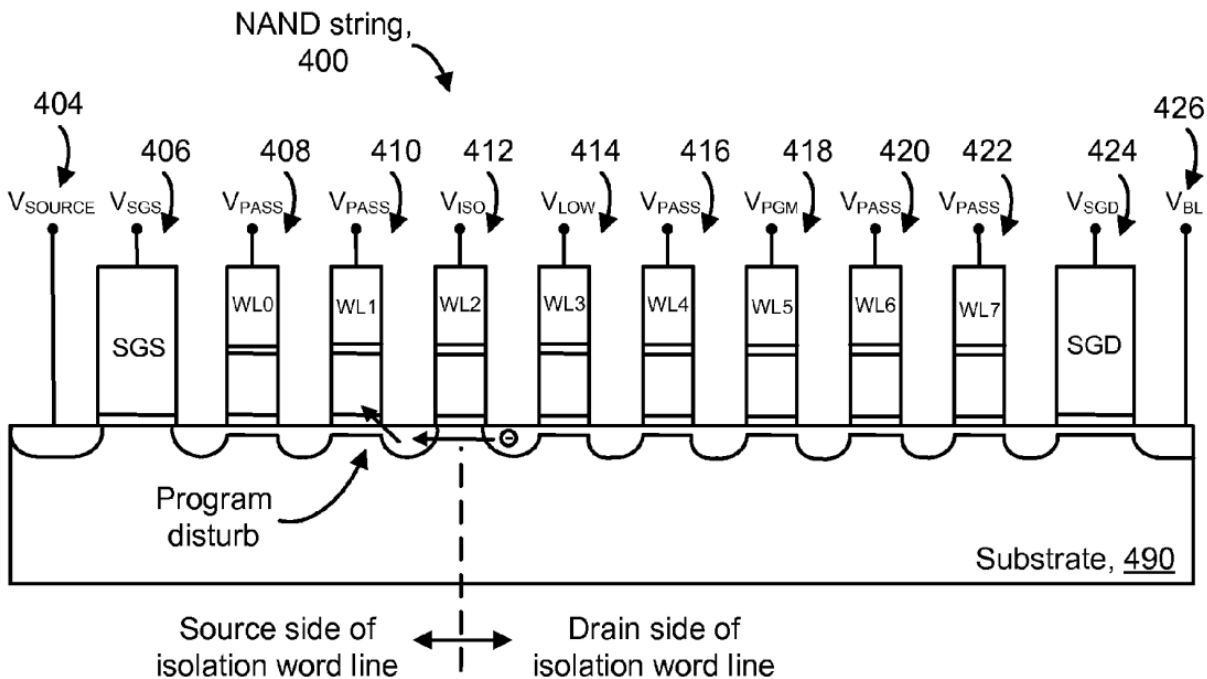
Petitioner presents four grounds, each relying on Dong:

- **Ground 1:** Dong anticipates claims 1, 3, 5-7, 11, and 13.
- **Ground 2:** Dong renders obvious claims 1, 3, 5-7, 11, and 13.
- **Ground 3:** Dong in combination with Costa renders obvious claims 8-9.
- **Ground 4:** Dong in combination with Shirai renders obvious claims 4, 10, and 14 .

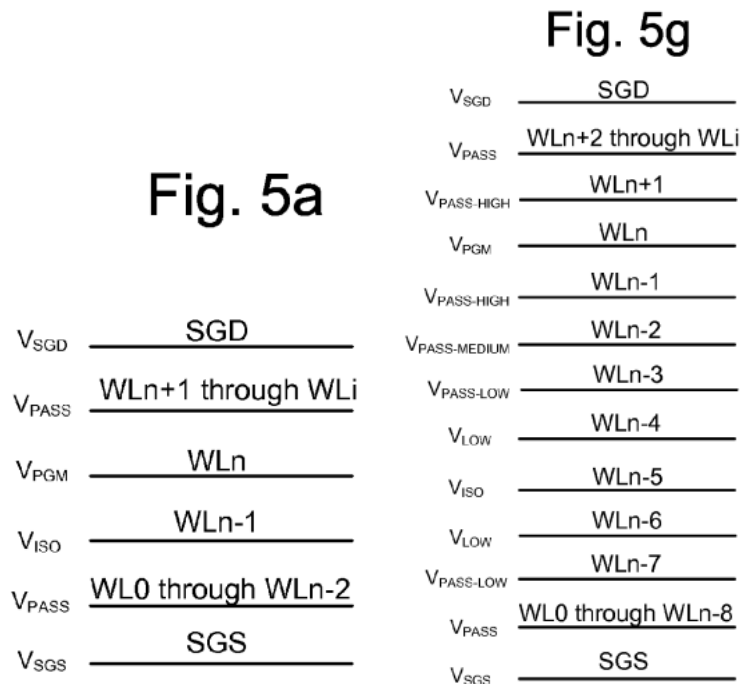
Pet. 7; Khatri2, ¶89.

F. Dong (Ex. 1005)

Dong discloses a purported solution to address program disturb in two-dimensional NAND memory strings arranged horizontally, as seen in Figure 4 below. Dong, ¶¶11, 45, Fig. 4; Khatri2, ¶90. As shown below, no wordline is at the “bottom” or “top” compared to any other wordline.

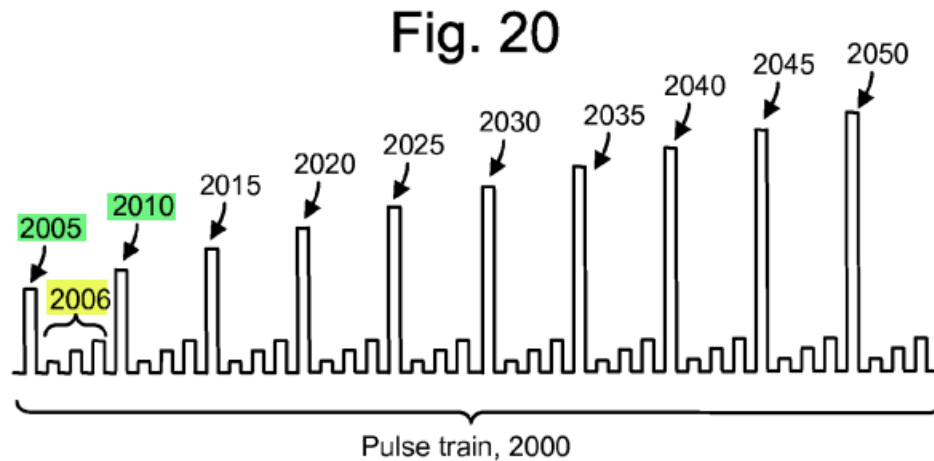


Dong, Fig. 4, ¶¶45, 48, 49; Khatri2, ¶90. Dong explains that “FIGS. 5a-h depict different examples of self-boosting modes,” showing different voltages applied to unselected wordlines. Dong, ¶20; *see also* Ex. 1009, 52-54 (describing self-boosting schemes for 2D NAND).



Dong, Figs. 5a, 5g. In these figures, which do not depict physical memory, Dong discloses local self-boosting schemes with an isolation wordline on the source side of the selected wordline WLn being programmed (i.e., program phase). Khatri2, ¶91. In Figure 5a, for example, WLn-1, located on the source side of WLn being programmed (i.e., receiving V_{PGM}), receives an isolation voltage (V_{ISO}). Dong, ¶49.

Dong also discloses a verify phase as seen in verify pulse set 2006 (yellow) between program pulses 2005 and 2010 (green).



Dong, ¶132, Fig. 20; Khatri2, ¶¶92-93.

G. Claim Construction

In Petitioner's claim construction section, Petitioner alleges "the '941 Patent's claims do not require further construction and should receive their plain and ordinary meaning." Pet. 22. However, when analyzing the claims, Petitioner rewrites the claimed phrase "from bottom to top" to "from source to drain." Pet. 34-35; Ex. 1004 ("Liu"), ¶¶112-113, 120; Khatri2, ¶¶94-100. And for the phrase "a program operation" recited in each independent claim, Petitioner fails to raise any construction in its Petition. *See* Pet. 22, 38-39, 63-64, 69. Yet during deposition, Dr. Liu revealed for the first time that he interprets "a program operation" to include **both** a program phase and a verify phase. Liu Dep. (Ex. 2021), 211:1-18 (Q: "[F]or the limitation '[w]hen an xth wordline is used to perform a program operation,' the phrase 'a program operation' is interpreted by you to include both of those phases, the program and the verifying phase?" A: "That's correct."); *see also id.*, 211:19-

212:17, 207:20-210:22; Khatri2, ¶¶101-102. Petitioner's attempts to rewrite the claims should be rejected because they conflict with plain language and the intrinsic record.

To be clear, Patent Owner does not believe these terms require construction for the Board to find all challenged claims patentable. Khatri2, ¶103. The Board need only apply the plain and ordinary meaning of these terms. If the Board were to construe “from bottom to top,” its construction would be, consistent with plain meaning, from lowest to highest—not from “source end” to “drain end” as Petitioner suggests. *Id.* Similarly, if the Board were to construe “a program operation,” its plain and ordinary meaning is an operation performed by applying a program voltage to a selected wordline to program a selected memory cell—not both a program phase and verify phase, as Petitioner suggests. *Id.*

Finally, the Board should interpret the preambles of claims 5 and 11 as limiting because they recite “essential structure” providing antecedent basis for subsequent limitations. Khatri2, ¶¶104-105.

1. “From Bottom To Top”

Petitioner states that “[t]he '941 Patent does not define the phrase *bottom to top*, but it was (and is) common in NAND flash memory devices to refer to the source end of a memory string as the ‘bottom,’ and the drain end as the ‘top.’ ... That common usage will be applied here.” Pet. 35 (emphasis original). In the

parallel district court litigation, Petitioner's expert Dr. Schubert applied the rewrite in his sworn declaration, stating, "the plain and ordinary meaning of 'from bottom to top' as understood by a POSITA would have been 'from the source to the drain side.'" Ex. 2010, 60; Khatri2, ¶¶106-109.

The Board should sustain its rejection of Petitioner's rewrite of the claim language. The plain meaning of "bottom" is not "source" and the plain meaning of "top" is not "drain." Khatri2, ¶109. The ordinary meaning of "bottom" and "top" controls—bottom means lowest point and top means highest point relative to the substrate. *See* Ex. 1001, 1:26-41, 6:39-47; Khatri2, ¶¶106-109, 124; Ex. 2013, 4-5 ("bottom": "the lowest part or place" / "top": "the highest part, point or level of something"); *see also* Ex. 2014, 3-4 ("bottom": "the deepest or lowest part" / "top": "the uppermost part, point, surface, or end"). The term "from bottom to top" has no special meaning in the semiconductor manufacturing context or in the '941 Patent. Khatri2, ¶108. Nothing in the '941 Patent or its file history provides a definition for the phrase "from bottom to top" or disclaims its ordinary meaning. *Id.*

a. The Intrinsic Evidence Shows "From Bottom To Top" Means From Lowest To Highest

The '941 Patent claims refer to wordlines in a vertical arrangement by reciting wordlines arranged "from bottom to top":

- "an (m+1)th wordline to an nth wordline *from bottom to top*" (claims 1, 7, and 11);

- “a first wordline to a kth wordline *from bottom to top*” (claims 2, 5, and 12); and
- “a (k+1)th wordline to an mth wordline *from bottom to top*” (claim 11).

Other limitations confirm this vertical arrangement, reciting portions, which consist of wordlines, formed “above” or “below” each other (claims 1-3, 5, 7, 11-13) and “dummy wordline[s]” formed “above” and “below” other portions (claims 4, 10, 14). Khatri2, ¶¶110-111. As the Board correctly recognized at institution, “[t]he independent claims state that the second memory portion is *formed* either *above* or *below* the first memory portion,” establishing “a relative top and bottom.” ID, 16-17 (emphasis original). The Board recognized that “[g]iven that the claims themselves identify relative vertical locations of the memory portions ... it follows that that claim terms referring to the top and bottom of wordlines within the memory portions also refer to relative vertical locations of the wordlines within the memory portions.” *Id.*, 17. The Board thus found that the claimed phrase “from bottom to top” means “the wordlines of the memory portions are arranged vertically from the bottom end of the memory portion toward the top of the memory portion.” *Id.*; Khatri2, ¶112.

The Board recognized this construction is confirmed by the specification, noting that the '941 Patent is directed to a three-dimensional NAND memory with wordlines arranged vertically, one on top of another. ID, 17. Like the claims, the

specification describes wordlines vertically arranged “from bottom to top”—with no reference to any source or drain. *See, e.g.*, Ex. 1001, 4:29-36; *see also id.*, Abstract; Khatri2, ¶¶113-117; ID, 17. Figure 8, for example, illustrates a three-dimensional memory with a first portion 710 (blue) and a second portion 720 (orange), each including wordlines arranged vertically from bottom to top (i.e., from lowest to highest) above the substrate (not shown).

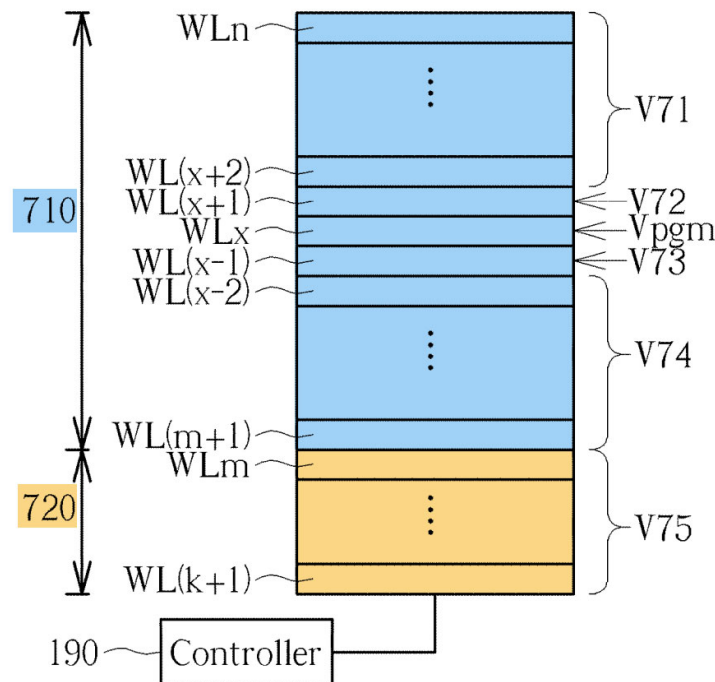


FIG. 8

Ex. 1001, Fig. 8; *see id.*, 1:26-41, 6:39-47; Khatri2, ¶113.

The first portion 710 includes “an (m+1)th wordline $WL(m+1)$ to an nth word WLn line *from bottom to top*.” Ex. 1001, 4:32-34; *see also id.*, Abstract. Consistent with the plain and ordinary meaning of the term “bottom,” the (m+1)th wordline is shown as the vertically lowest wordline in first portion 710. *Id.*, 4:29-32, Fig. 8;

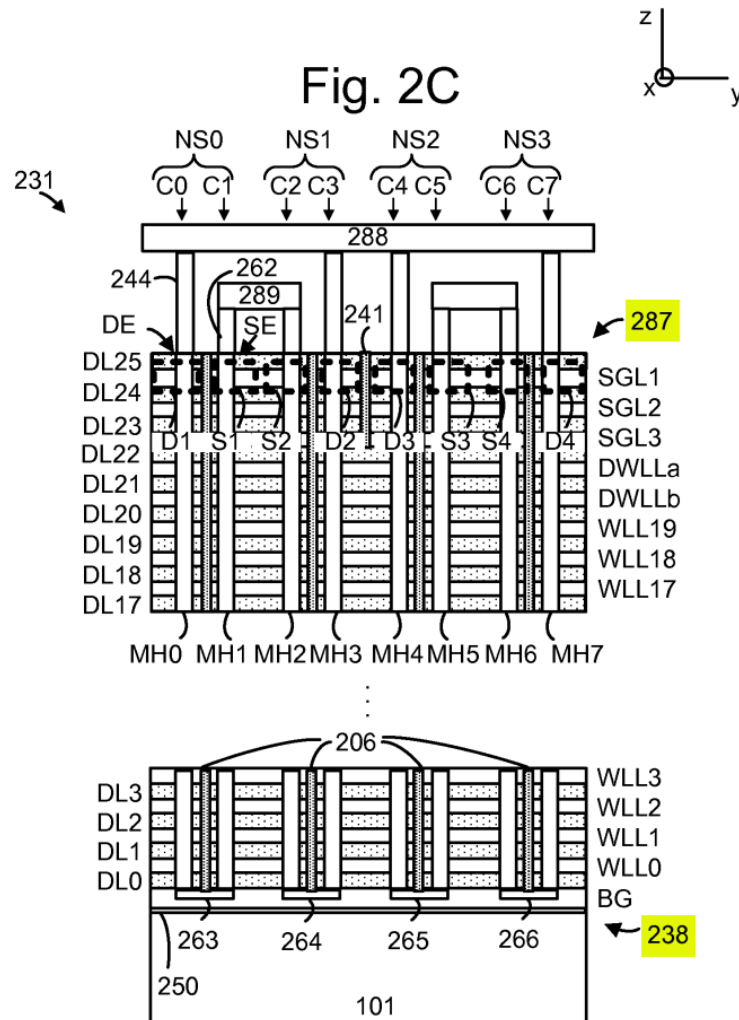
Khatri2, ¶113. Similarly, and consistent with the plain and ordinary meaning of the term “top,” the WLn wordline is shown as the vertically highest wordline in first portion 710. Ex. 1001, 4:29-32, Fig. 8; Khatri2, ¶¶113-114; *see also* Ex. 1001, 4:34-36 (same for “second portion”). The specification further describes this vertical arrangement by referring to “portions” that are “above” or “below” each other, where each “portion” consists of “wordlines.” Ex. 1001, Abstract, 2:65-3:3 (first and second portions), 4:30-36 (same), 1:46-50 (same), 1:56-60 (same), 2:4-6 (same), 2:14-18 (same); *id.* 3:46-48 (third portion), 5:7-9 (same), 5:32-34 (same); Khatri2, ¶¶114-115. At institution, the Board recognized the specification “describes embodiments with first, second, and/or third memory portions as including various wordlines ‘from bottom to top’ and that the memory portions are formed above or below each other.” ID, 17. The Board found Patent Owner’s construction correct, “not from source side to drain side” as Petitioner proposed. ID, 17-18 (collecting citations).

Notably, all other figures of the ’941 Patent illustrate wordlines arranged vertically, as in Figure 8, reinforcing that the plain and ordinary meaning of “bottom” and “top” applies. Ex. 1001, Figs. 1-7, 9-11; Khatri2, ¶116; *see Seabed Geosolutions (US) Inc. v. Magseis FF LLC*, 8 F.4th 1285, 1287-88 (Fed. Cir. 2021) (determining the plain and ordinary meaning of “fixed” is “attached or fastened” consistent with the specification); *Wis. Alumni Rsch. Found. v. Apple Inc.*, 905 F.3d 1341, 1350-52

(Fed. Cir. 2018) (interpreting a term based on consistent characterization in the specification). The Board recognized as much at institution, stating that “the ’941 patent illustrates and describes figures of memory devices having wordlines arranged vertically from bottom to top” and that “Figures 1-11 each depict ‘a memory’ having vertically arranged wordlines.” ID, 17.

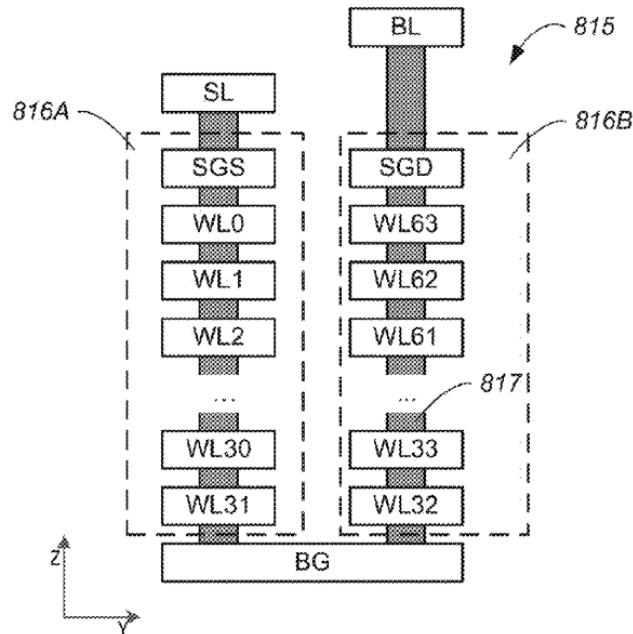
The Board also rightly recognized the specification’s description of wordlines relative to the “lowermost” or “uppermost” portion of a memory supports Patent Owner’s position. *See, e.g.*, Ex. 1001, 5:4-19, 5:38-50. This description shows “the Specification identifies the location of the wordline in relation to its vertical location, not to its location relative to the source or drain,” as the Board found. ID, 18; Khatri2, ¶117.

The references cited on the face of the ’941 Patent confirm that a POSITA would interpret wordlines arranged “from bottom to top” to mean from lowest to highest, and not from source to drain. *See Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221, 1230-31 (Fed. Cir. 2011) (“[P]rior art cited in a patent or cited in the prosecution history of the patent constitutes intrinsic evidence.”); Khatri2, ¶118. Exhibit 2011—by the same inventor as Dong—describes a 3D NAND memory stack with “a top 287 and a bottom 238,” referring to the respective highest and lowest portions of the memory stack (i.e., below bit line 288 and vias 244, 262, and above substrate 101).



Ex. 2011, ¶¶75, 77, Fig. 2C; Khatri2, ¶118.

Similarly, Exhibit 2012, also cited on the '941 Patent, discloses a NAND string in a U-shape, “with external elements (source line ‘SL’ and bit line ‘BL’) located at the top of the structure,” and “[a]t the bottom of NAND string 815 is a controllable gate (back gate ‘BG’).”

**FIG. 8**

Ex. 2012, ¶84, Fig. 8; Khatri2, ¶119. This undermines Petitioner's position that "bottom to top" means effectively "source to drain" because the word "bottom" refers to the vertically lowest element, the "back gate 'BG,'" **not** to the "source." Similarly, the word "top" refers to the two elements (source line "SL" and bit line "BL") shown vertically highest, **not** to the drain. Khatri2, ¶120.

Because the intrinsic evidence establishes that the plain and ordinary meaning of "from bottom to top" is "from vertically lowest to vertically highest," the Board need not consider extrinsic evidence. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (When "analysis of the intrinsic evidence alone will resolve any ambiguity in a disputed claim term[,] ... it is improper to rely on extrinsic evidence."); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1318, 1320-22 (Fed.

Cir. 2005) (recognizing extrinsic evidence “as less reliable than the patent and its prosecution history in determining how to read claim terms”); Khatri2, ¶121.

But to the extent extrinsic evidence is considered, however, even Petitioner's own cited references show that “from bottom to top” means from lowest to highest. Petitioner's Exhibit 1009 uses the terms “top” and “bottom” to describe the vertically highest and vertically lowest physical components of 3D NAND memory—not where the source or drain are located. *See, e.g.*, Ex. 1009, 327 (“[T]he charge trap nitride layer is physically connected from top to bottom [control gates] in 3D SONOS/TANOS NAND flash.”); Khatri2, ¶¶122-125. The Board recognized that this disclosure, along with the U-shaped example above, “belies Petitioner's contention that ‘from bottom to top’ means from source end to drain end.” ID, 19.

Given overwhelming evidence supporting Patent Owner's construction, the Board should sustain its finding at institution that “the claim language referring to first and second memory portions that comprise wordlines ‘from bottom to top’ to mean that wordlines of the memory portions are arranged vertically from bottom (lowest) to top (highest).” ID, 19; Khatri2, ¶125.

b. Petitioner's Proposed Construction Improperly Relies Solely on Extrinsic Evidence

Petitioner does not even try to argue that the intrinsic evidence supports its incorrect interpretation that “from bottom to top” means “from source to drain”—it does not. Petitioner's sole mention of the '941 Patent is to allege that it “does not

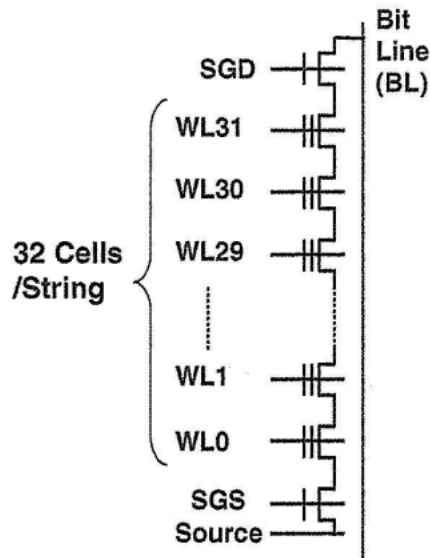
define the phrase bottom to top.” Pet. 35; Liu, ¶120. But a patent need not (and preferably does not) define plain and ordinary English words. Petitioner also ignores the '941 Patent's consistent usage of the phrase “bottom to top” to refer to the vertically lowest and highest wordlines respectively, consistent with its plain and ordinary meaning. *Supra* Section II.G.1.a; Khatri2, ¶126. As the Board recognized, “Petitioner does not point to any persuasive intrinsic evidence to support its contention that ‘from bottom to top’ means ‘from the source side to the drain side.’” ID, 18.

Indeed, nothing in the '941 Patent supports Petitioner's construction. The claims do not recite a “source” or a “drain.” *See* Ex. 1001, 6:55-8:54. The figures of the '941 Patent do not even show the source or drain. *Id.*, Figs. 1-11. And the specification never once refers to the “source” or “drain” ends of a memory string, much less uses those never-described elements to define the “bottom” and “top.” *Nystrom v. TREX Co.*, 424 F.3d 1136, 1144-46 (Fed. Cir. 2005) (construing a term at odds with the intrinsic record “violates the principles articulated in *Phillips*”). When the specification does not define a term and there is no prosecution history disclaimer (as here), the correct construction should “not depart from the natural reading of a phrase.” *Columbia Ins. Co. v. Simpson Strong-Tie Co.*, Nos. 2021-2145, 2021-2157, 2023 WL 2733427, at *7 (Fed. Cir. Mar. 31, 2023). Yet that is exactly what Petitioner proposes here, arguing that the lack of explicit definition in the patent

justifies rewriting the claim, contrary to its plain language, to have an entirely different meaning. Khatri2, ¶127.

Petitioner's construction thus *relies solely on extrinsic evidence*, which is improper. *See Seabed Geosolutions*, 8 F.4th at 1287 (rejecting construction “based entirely on extrinsic evidence”). Even if the Board were to look to on extrinsic evidence, it does not consistently teach that “bottom” means source and “top” means drain. Petitioner relies on its expert's interpretation of circuit diagrams (not physical memories) for 2D NAND flash memories, which he says show “the source end of the NAND string at the bottom, and the drain end of the NAND string at the top.” Liu, ¶113; Pet. 35; Khatri2, ¶128.

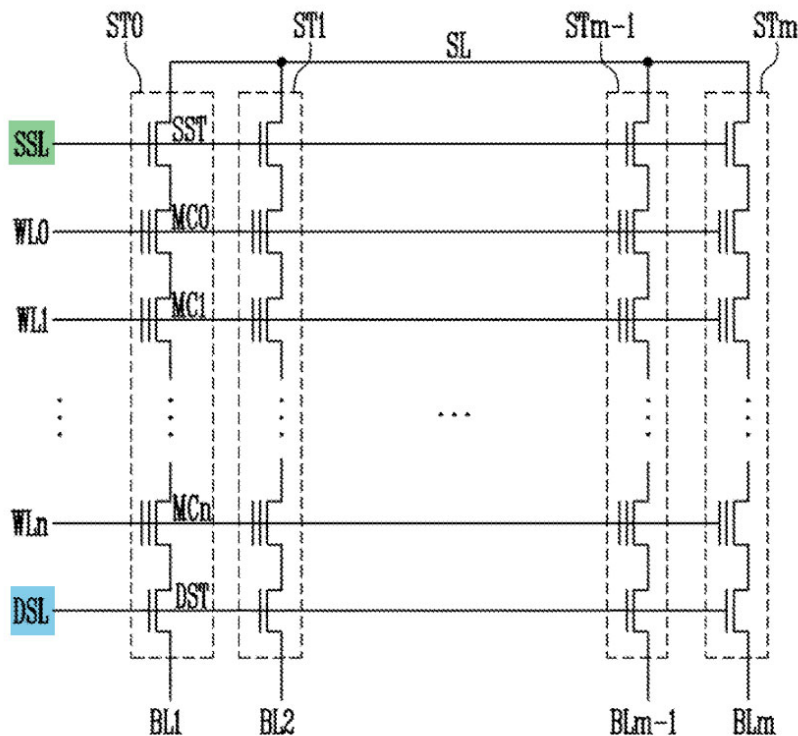
For example, Petitioner's expert refers to the following circuit diagram from Exhibit 1009, which shows a 2D NAND flash memory with several wordlines (WL0-WL31) and select transistors “SGD” and “SGS” to isolate the NAND string:



Ex. 1009, 39 (Fig. 2.2); Liu, ¶113; Khatri2, ¶¶128-129. But this diagram is not a representation of the physical layout of the memory, as a POSITA would readily understand, because it uses circuit symbols for flash and NMOS transistors. Khatri2, ¶¶129-130; *see, e.g.*, Ex. 2017, 7, Fig. 2.1 (illustrating a physical representation of a floating gate memory cell next to its circuit symbol seen in circuit diagrams); Ex. 2019, 8-9, Figs. 3-13 (physical representation of an NMOS transistor), 3-12(b) (circuit symbol for an NMOS transistor). As the Board recognized, “Petitioner fails to persuasively explain ... how figures that depict the architecture of 2D NAND strings with the source end on the bottom means that the term ‘from bottom to top’ means from source end to drain end.” ID, 18-19.

Diagrams like the above are merely symbolic depictions of a circuit and its connectivity. They do not reflect the actual, physical arrangement of wordlines. Khatri2, ¶131. Petitioner’s expert confirms that the circuit diagrams he relies on, including the one above, “are discussing two-dimensional NAND flash memories.” Liu, ¶113. While the circuit diagram shown above is oriented vertically, two-dimensional NAND flash memories have wordlines physically arranged in a horizontal plane, i.e., from left to right—not vertically, “from bottom to top.” *See, e.g.*, Ex. 1009, 38-40, Fig. 2.3; Khatri2, ¶131. Petitioner’s cited circuit diagrams do not use the word “bottom” to refer to the source, or “top” to refer to the drain. Khatri2, ¶¶128-132.

Even if Petitioner were correct that its few cited references placed the source end of a memory string at the bottom, many other references show different arrangements, disproving Petitioner's suggestion that it was common convention for "bottom to top" to mean "source to drain." *See* Pet. 35 (citing Liu, ¶¶112-113, 120); Khatri2, ¶¶132-141. For example, Exhibit 2015, cited on the '941 Patent, provides a circuit diagram of a memory string with the source ("SSL" in green) at the top and the drain ("DSL" in blue) at the bottom:



Ex. 2015, Fig. 2, ¶¶15, 44-46; Khatri2, ¶¶132-134. To the extent that Petitioner's cited diagram from Figure 2.2 of Exhibit 1009 is (incorrectly) viewed as showing the memory's physical structure, the above diagram from Exhibit 2015 shows the

opposite arrangement. Khatri2, ¶¶132-134. As another example, the Aritome reference cited by Petitioner illustrates a physical diagram of a two-dimensional NAND flash memory array with the source (near the “SGS” in green) and the drain (near the “SGD” in blue) at the same physical level as the wordlines above the substrate:

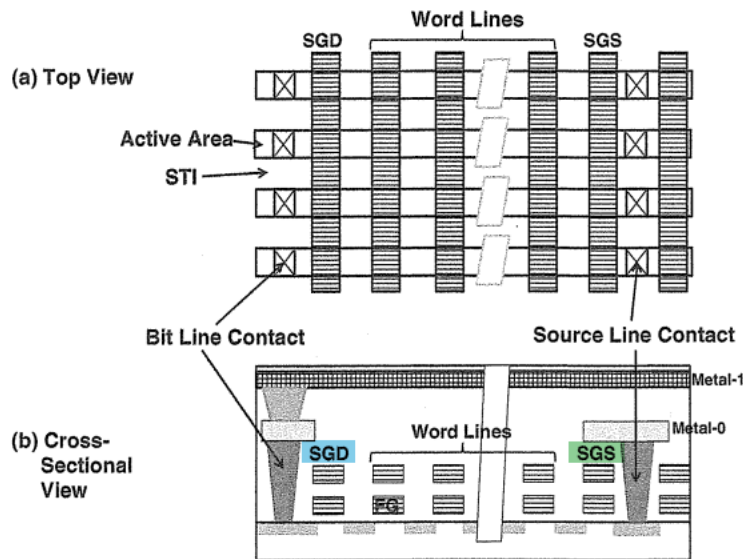


FIGURE 2.3 (a) Top schematic view and (b) cross-sectional view of NAND flash memory cells.

Ex. 1009, 39-40; Khatri2, ¶135.

If Petitioner's construction were adopted, it would lead to the absurd conclusion that, as Petitioner's expert in the district court litigation admitted, the “bottom and top are at the same physical level.” Ex. 2010, 59; Khatri2, ¶136. Indeed, Petitioner's expert admits that his interpretation makes irrelevant “whether the physical device is in a horizontal or vertical direction.” Liu, ¶113. Put simply, Petitioner's construction effectively renders both “bottom” and “top” meaningless

within the context of the challenged claims. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir. 2021) (“It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.”).

Petitioner’s rewrite makes no sense because, even in a three-dimensional NAND memory structure, the “source” is not necessarily at the “bottom” and the “drain” is not necessarily at the “top.” Khatri2, ¶137. Indeed, both the “source” and the “drain” can be at the “top.” *Id.* For example, Exhibit 2012, cited by the ’941 Patent, depicts the physical structure of a U-shaped three-dimensional NAND memory where both the source (near “SGS,” green) and the drain (near “SGD,” blue) are at the top, as shown in Figure 8 below.

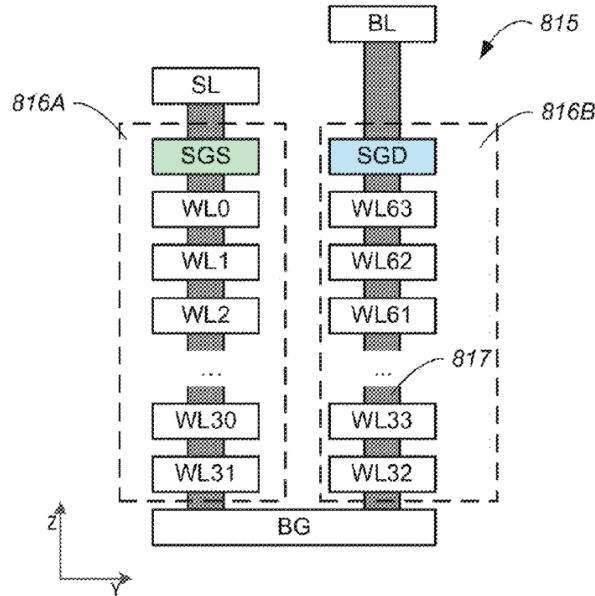
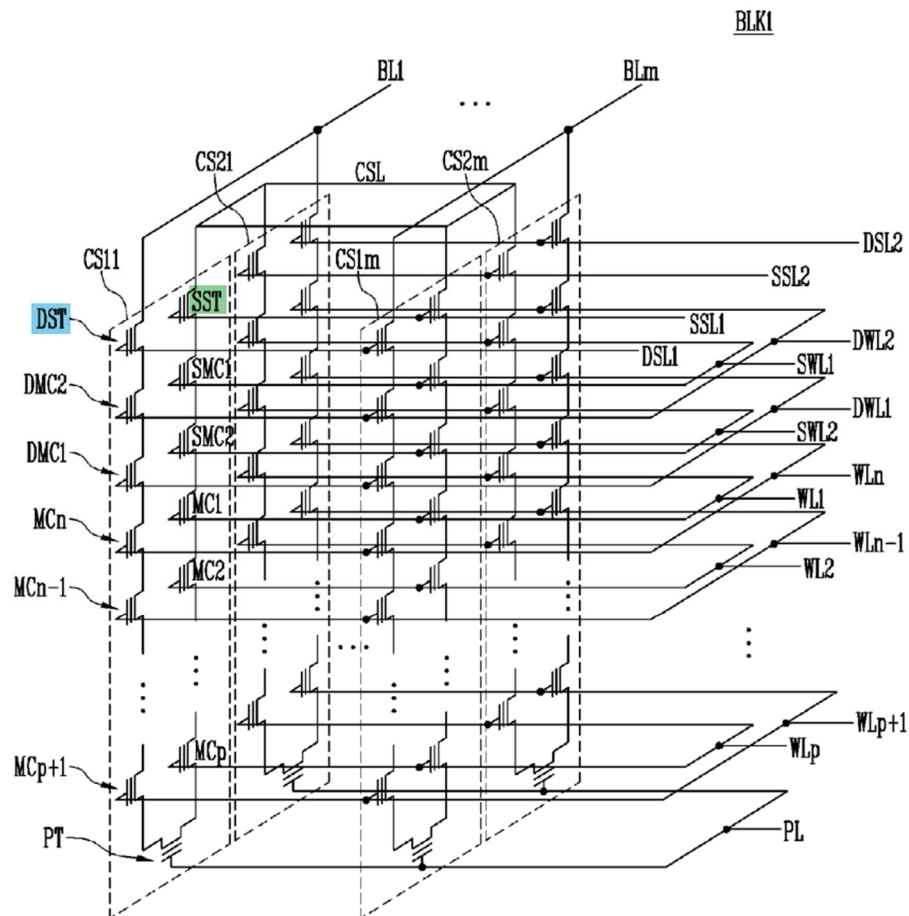


FIG. 8

Ex. 2012, Fig. 8; *see also id.* ¶¶16-17, 80, 84-87, Fig. 9; Khatri2, ¶137. If one incorrectly assumes (as Petitioner does) that circuit diagrams show physical

structure, then Exhibit 2016, also cited on the face of the '941 Patent, shows a U-shaped memory string with both the source (near the "SST" in green) and the drain (near the "DST" in blue) at the top:



Ex. 2016, Fig. 3, ¶¶50-65; Khatri2, ¶138; *see also* Ex. 1008 (cited on the face of the '941 Patent), Fig. 13, ¶¶115-129 (describing a circuit diagram of a U-shaped three-dimensional NAND memory with the source and drain select transistors (SST and DST respectively) at the top). Given these examples, Petitioner cannot reasonably argue that “it was (and is) common in NAND flash memory devices to refer to the

source end of a memory string as the ‘bottom,’ and the drain end as the ‘top.’” Pet. 35; Khatri2, ¶138.

In sum, Petitioner’s proposed construction of “from bottom to top” conflicts with the plain English meaning of the term and the intrinsic evidence and is not even supported by extrinsic evidence. Khatri2, ¶¶139-141. Petitioner’s proposed rewrite is an improper attempt to map the claimed vertical arrangement of wordlines to Dong’s horizontal arrangement of wordlines in hindsight. The Board—as it did at institution—should construe “from bottom to top” to mean “that wordlines of the memory portions are arranged vertically from bottom (lowest) to top (highest).” ID, 19.

2. “A Program Operation”

Independent claims 1, 5, and 11 each recite applying specific voltages “when an xth wordline is used to perform *a program operation*.” Ex. 1001, 6:61-67, 7:29-31, 8:21-23. The ’941 Patent claims use this phrase in its plain and ordinary sense, simply referring to “an operation performed by applying a program voltage to a selected wordline to program a selected memory cell.” Khatri2, ¶142-161.

a. Petitioner’s Construction Was Not Revealed Until Deposition of Dr. Liu

Petitioner did not disclose a construction for “a program operation” in the Petition. Dr. Liu revealed a new position during his deposition, where he stated he construes “a program operation” to include both a program phase and verify phase.

Liu Dep., 211:1-18; *see also id.* 211:19-212:17, 207:20-210:22. When asked where he disclosed this position in his declaration, he pointed only to one paragraph (¶60) in his Technology Background section—a paragraph that does not refer to the claims or even mention “a program operation,” and is referred to in the Petition only once through a mere “*see also*” cite. *Id.*, 212:22-213:12; Pet. 15; Khatri2, ¶¶144-146.

Petitioner's belated construction is improper and should be given no weight. *See, e.g.*, 37 C.F.R. § 42.104(b)(3) (a petition must identify “[h]ow the challenged claim is to be construed”); Consolidated Trial Practice Guide Nov. 2019, 44-45 (“[P]etitioner must include a statement identifying a proposed construction of the particular term and where the intrinsic and/or extrinsic evidence supports that meaning” and “cannot raise new claim construction issues that were not previously raised in its petition.”).

Regardless, as explained below, Petitioner's proposed construction is also incorrect and contravenes intrinsic evidence.

b. The Intrinsic Evidence Supports Patent Owner's Construction

The intrinsic evidence supports Patent Owner's interpretation. Khatri2, ¶¶147-154. The '941 Patent discloses a solution for reducing program disturb and pass voltage disturb on unselected wordlines when a program voltage is applied to a selected wordline—a process that occurs only during a program operation. Ex. 1001, 1:34-41, 1:19-22; *see supra* Section II.B. To implement this solution, the '941

Patent describes “[a] program operation” as “an operation for programming a memory cell.” *Id.* 3:6-8. In the next line, the ’941 Patent describes that “[w]hen an xth word line WLx is used to perform a program operation, the controller 190 may apply a program voltage Vpgm to the xth word line WLx,” as shown in all Figures. *Id.*, 3:9-11, Figs. 1-13; *see id.*, 3:53-58, 4:25-28 (describing applying voltages of Figures 1 or 2 to Figure 6), 4:37-42, 4:51-55, 5:9-12, 5:16-19, 5:29-30, 5:42-62, 6:1-3, 6:21-23. When this **program voltage** (V_{PGM}) is applied to the selected wordline WLx, voltages V1, V2, V3, and V4 are applied to unselected wordlines. *Id.*, Fig. 8, 3:9-21. The claims also specify applying voltages “when an xth wordline is used to perform a program operation.” *Id.* 6:61-67, 7:29-31, 8:21-23; *see also id.*, 6:39-41 (describing applying voltages by portion to reduce program and pass voltage disturbances). Notably, the ’941 Patent never mentions a verify operation, and the disclosed voltages only accomplish the stated aim to reduce program disturb if applied **during** a program operation. Khatri2, ¶¶147-151.

To the extent the Board considers extrinsic evidence, Petitioner’s expert Dr. Liu recognized application of a program voltage like V_{PGM} “causes electron movement into the cell and raises the cell’s threshold voltage,” i.e., programs it. Liu, ¶57; *see id.*, ¶¶58, 60, 71; Khatri2, ¶¶152-153. He also recognized a separate verification/read operation to determine the cell “has been sufficiently programmed (i.e., its threshold voltage has moved to the desired level).” Liu, ¶60. And even

Petitioner's Exhibit 1009 supports Patent Owner's interpretation, confirming that "a program operation" is "performed by applying high-voltage V_{PGM} to control gate." Ex. 1009, 44; Khatri2, ¶¶152-153. This same exhibit also confirms that "a program operation" is completed before a verify phase. Ex. 1009, 119 ("After the program operation, a verify operation is performed...."); Khatri2, ¶153. Similarly, Petitioner's Exhibit 1010 states "[a] program operation applies a high programming voltage (e.g., +15 V) to the cell to change the cell's threshold voltage to the desired range." Ex. 1010, 280; Khatri2, ¶154.

c. Petitioner's Proposed Construction Is Unsupported By Any Intrinsic Evidence

The Board should reject Petitioner's belated construction because it improperly broadens "a program operation" to sweep in a verify phase that lacks any intrinsic support. *See Genuine Enabling Tech. LLC v. Nintendo Co.*, 29 F.4th 1365, 1375 (Fed. Cir. 2022) (rejecting a construction that had "no basis anywhere in the intrinsic record"). In fact, the verify phase is not even mentioned in the '941 Patent. That is, the '941 Patent does not describe a verify phase during which a read voltage is applied to check already-programmed cells to confirm that they are at the intended threshold voltage—i.e., after the program operation during which a program voltage is applied. Khatri2, ¶155. And even if the '941 Patent disclosed a verify phase (it does not), the recited voltages only reduce program disturb as intended if applied during a program phase.

d. Dr. Liu's Proposed Construction Contradicts Prior Testimony

Dr. Liu's deposition testimony contradicts his prior testimony before the PTAB, calling into question Dr. Liu's credibility. Khatri2, ¶¶156-161.

In 2024, Dr. Liu submitted a declaration on Micron's behalf where he described a "program operation" as limited to the program phase, i.e., "a pulse that creates charge in the storage region." Ex. 2022, ¶81. Dr. Liu distinguished this "program operation" from a "verify operation," the latter of which "determines whether the pulse was sufficient to properly program the cell." *Id.*; *see id.*, ¶¶248 ("Again, the read (verify) occurs after the program operation to verify whether the program operation was successful."), 103 (same), 47 (describing a "programming operation" as limited to the step of "applying a voltage pulse to a control gate of the selected wordline"), 181 ("It goes without saying that a memory that is read was programmed."), 188, 190, 203; *see also* Ex. 2023, ¶66 ("Specifically, a verify operation is a read operation executed *after* a program operation."). Dr. Liu even testified about Costa in that prior proceeding: "the read (verify) occurs *after the program operation* to verify whether the program operation was successful." Ex. 2022, ¶248; *see id.* ("[W]hen the selected memory cell is being verified, it is programmed."); Khatri2, ¶¶157-158.

Dr. Liu takes the opposite position here, asserting that "a program operation" includes both the program and verify phase. Liu Dep., 211:1-18; *see supra* Section

II.G.2.a; Khatri2, ¶¶159-161. Dr. Liu now sees Costa as supporting that “a program operation” includes both the program and verify phases. Liu Dep., 159:17-161:18 (“[A]longside that, we have another technique which is taught by Costa, that because the program operation really involves ... two operation [or] two phases; one is injecting electron the other one verification.”), 216:15-218:16 (referencing Costa to support that a “program operation as understood by POSITA would include both injecting phase and verification phase”).

Dr. Liu's contradictory testimony is not credible and cannot justify Petitioner's new, strained construction.

3. The Preambles of Claims 5 and 11 Are Limiting

Claims 5 and 11 recite “[a] program method of a memory” wherein the “memory” includes distinct wordlines. Ex. 1001, 7:23-28, 8:15-20. As the Board found (ID, 14-15), “[b]ecause the preambles of independent claims 5 and 11 provide antecedent basis for the wordline limitations recited in the body of their respective claim,” the preambles of claims 5 and 11 are limiting. *See Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1358 (Fed. Cir. 2012) (“[A] preamble phrase that provides antecedent basis for a claim limitation generally limits the scope of the claim.”); *Bio-Rad Laboratories, Inc. v. 10X Genomics Inc.*, 967 F.3d 1353, 1371 (Fed. Cir. 2020) (claim body's reliance on preamble for antecedent basis “is a strong indication that the preamble acts ‘as a necessary component of the claimed invention’”); Khatri2,

¶¶162-167. The preamble of claim 5 recites “a first wordline to a kth wordline” and “an mth wordline” providing antecedent bases for “the first wordline” and the limitation defining x, k, and m in claim 5. Ex. 1001, cl. 5. Similarly, the preamble of claim 11 recites “an nth wordline,” “a (k+1)th wordline,” and “an mth wordline” that provide antecedent basis for wordlines recited in the body of claim 11. *Id.*, cl. 11. In addition, the preambles of claims 5 and 11 provide antecedent basis for terms in several dependent claims, including:

- “the mth wordline” (claim 6);
- “the first portion” (claims 8-10, 13, 14);
- “the second portion” (claims 7-10, 12, 14); and
- “the kth wordline” (claim 12).

See Pacing Techs., LLC v. Garmin Int'l, Inc., 778 F.3d 1021, 1024 (Fed. Cir. 2015) (holding preamble of independent claim limiting because it provided antecedent basis for dependent claims). Thus, these preambles recite “essential structure” in defining the first and second portion and their component wordlines to which recited voltages are applied. *See Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002); Khatri2, ¶¶162-167.

III. Grounds 1 and 2: Dong Does Not Disclose Wordlines Arranged “From Bottom To Top”

Under the plain and ordinary meaning of “from bottom to top”—i.e., from lowest to highest—all of Petitioner's grounds fail because they exclusively rely on

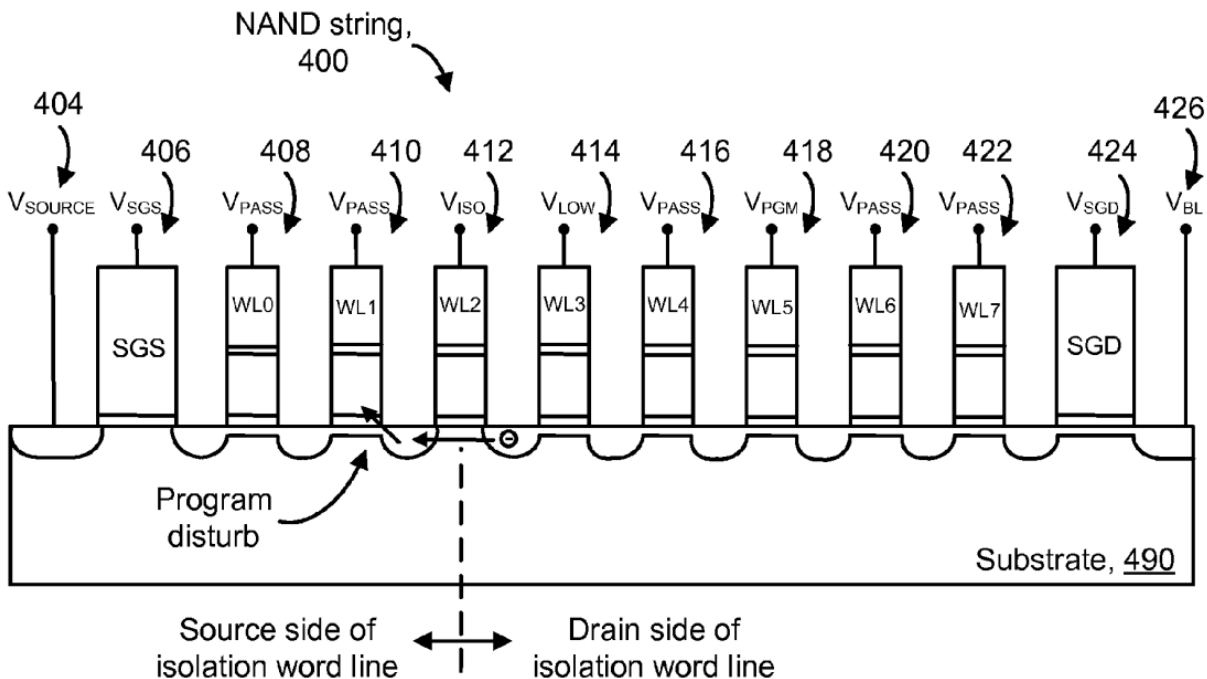
Dong. *See* Pet. 7; Khatri2, ¶¶168-169. Dong does not anticipate or render obvious the independent claims of the '941 Patent because it does not disclose or suggest wordlines vertically arranged “from bottom to top,” i.e., from lowest to highest, as claimed. Instead, Dong teaches wordlines arranged horizontally, i.e., from left to right.

Petitioner argues that “to the extent *bottom to top* is interpreted to require vertical strings in a 3D NAND memory, Dong discloses its ‘array of storage elements can be three dimensional’ and shows Figure 5a in a vertical orientation which satisfies the claim.” Pet. 35. But as explained below, these disclosures are not a teaching or suggestion to arrange wordlines vertically as claimed. Contrary to Petitioner’s allegation, Figures 5a and 5g do not represent the physical structure of the wordlines, much less depict any vertical 3D NAND memory. Khatri2, ¶¶168-169.

A. Dong’s Wordlines Are Arranged In A Horizontal Plane Above the Substrate, Not “From Bottom To Top”

Dong discloses 2D NAND with wordlines arranged horizontally—not from “bottom to top,” as claimed in the '941 Patent. Khatri2, ¶170. Petitioner points to Dong’s disclosure of a “memory die 1298” which “*includes a two-dimensional array of storage elements 1100.*” Pet. 34 (citing Dong, ¶95, Fig. 12), 51 (addressing preamble of claim 1 by citing back to claim 5), 68 (addressing preamble of claim 11 by citing back to claim 1). Figure 4 below illustrates a “cross-sectional view” of a

two-dimensional “NAND string” with storage elements, corresponding wordlines arranged horizontally from left to right, SGS, and SGD at the same physical level above a substrate. Dong, ¶¶19, 45, 48, 49; Khatri2, ¶170.



Dong, Fig. 4.

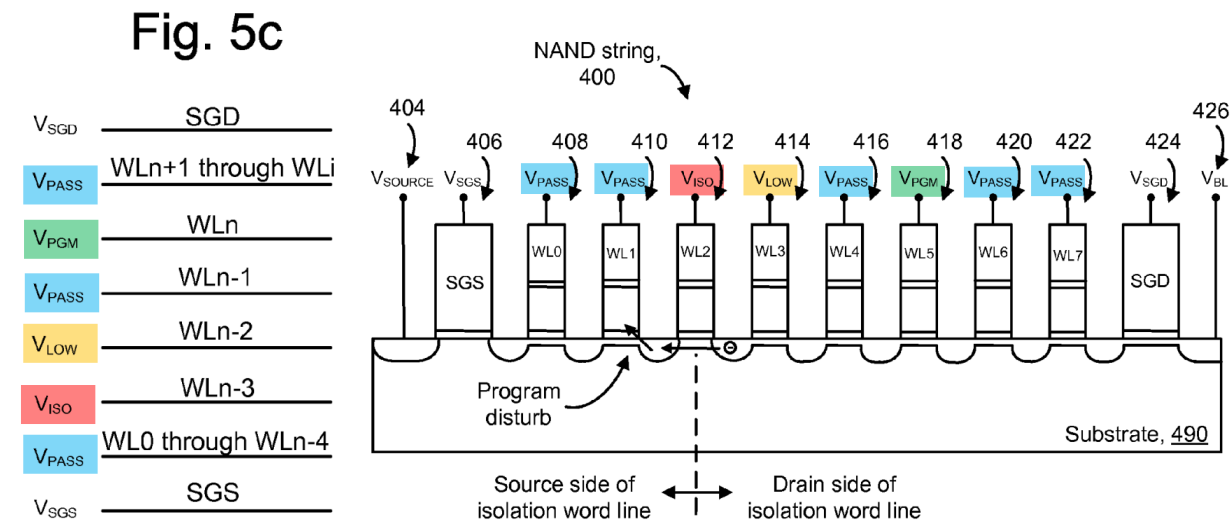
Although Figure 4 shows the memory's physical structure, Petitioner relies on Dong's voltage charts in Figures 5a and 5g, which do not “teach[] or suggest[]” (ID, 24-25) any physical arrangement of wordlines. *See* Pet. 29-38 (claim 5), 52-53 (claim 1), 68 (claim 11). As Dong explains, “FIGS. 5a-h depict different examples of self-boosting modes,” showing voltages applied differently to the wordlines. Dong, ¶20; *see* Ex. 1009, 52-54 (describing self-boosting schemes for 2D NAND). While these voltage lines are listed vertically, as most lists are, for ease of reading,

they do not represent—and cannot alter—the actual physical arrangement of the wordlines in the memory, which are horizontal as shown in Dong's Figure 4, as expected in 2D NAND memory arrays. Khatri2, ¶¶170-176; *see, e.g.*, Dong, ¶¶20, 47, 87. As the Board recognized at institution, “we do not understand Dong Figures 5a-5h to depict the physical structure of a memory cell, but rather to depict a self-boosting mode.” ID, 22 n.6.³

As shown below, the voltages applied to wordlines in the voltage chart of Figure 5c correspond to the labeled voltage inputs in the physical memory structure shown Figure 4, which shows the wordlines physically arranged in a horizontal plane:

³ Despite this finding, the Board appears to err by relying on Dong's Figures 5a and 5g arranged “in a vertical orientation” as support for the physical arrangement of the memory. *See* ID, 24-25.

Fig. 4



Dong, Figs. 4, 5c, ¶¶45-46, 54; Khatri2, ¶¶176-182.

The same is true of Dong's Figures 5a and 5g. *See* Pet. 29-44 (relying on Fig. 5a for claim 5), 50-66 (relying on Fig. 5g for claim 1), 68-70 (referring to Fig. 5g for claim 11). Dong describes Figures 5a and 5g in the context of Figure 4's two-dimensional NAND string. Dong, ¶¶47 ("FIGS. 5a-h depict different examples of self-boosting modes."), 59 ("FIG. 5g depicts another revised erased area self-boosting mode."); Khatri2, ¶94. Dong relies on elements of Figure 4, like "substrate 490" and "wordline 412," to describe the operation of the "revised erased area self-boosting mode" ("REASB") described in Figure 5g, confirming that the Figure 5 diagrams correspond to the physical arrangement of Figure 4. Dong, ¶¶49, 59, 65, 67; Khatri2, ¶¶182-184.

Thus, a POSITA would understand that the voltage charts of Figures 5a and 5g refer to the wordlines that are physically arranged in a horizontal plane above a

substrate, as shown in Figure 4. Khatri2, ¶¶182-186; *see* Ex. 1009, 52-54 (describing self-boosting schemes for 2D NAND). No other conclusion is reasonable because Figure 4's "cross-sectional view of a NAND string" is the *only* depiction in Dong of how its wordlines are physically arranged. Dong, ¶45; Khatri2, ¶185-186. Dong's voltage charts cannot meet the Petitioner's burden to demonstrate the existence of wordlines physically arranged "from bottom to top" as claimed.

The Board agreed at institution, stating that "[b]ecause we did not adopt Petitioner's proposed construction of 'from bottom to top' as meaning from source end to drain end, we disagree that Dong's method applied to a 2D memory, which has wordlines arranged horizontally from source to drain end, teaches these limitations [of claim 5]." ID, 24. That is correct.

B. Dong's Passing Reference To "Three Dimensional" Storage Does Not Disclose Or Suggest Vertically Arranged Wordlines As Recited

Petitioner points only to a single sentence in Dong referencing three-dimensional storage—"[i]n some embodiments, the array of storage elements can be three dimensional"—and assumes, without explanation, that this discloses vertically arranged wordlines as recited. Dong, ¶95; *see* Pet. 35. But this is not a reference to vertically arranged wordlines, and *Petitioner did not even argue that it would have been obvious to use vertically arranged wordlines*. Khatri2, ¶187. The cited sentence in Dong refers to those arrangement of wordlines that are 2D NAND-based,

and cannot disclose the claimed invention, which requires “[a] memory” with a “first portion” having wordlines vertically arranged “from bottom to top,” a “second portion formed below the first portion” having wordlines vertically arranged “from bottom to top,” and applying specific voltages to particular wordlines. *See, e.g.,* Ex. 1001, 6:55-7:2 (cl. 1); Khatri2, ¶187.

1. No Anticipation

Petitioner's anticipation argument (Ground 1) fails because Dong's single mention of “three dimensional” does not disclose “all elements of [the] claimed invention *arranged as in the claim.*” *Therasense, Inc. v. Becton, Dickinson & Co.*, 593 F.3d 1325, 1332 (Fed. Cir. 2010). Dong's reference to “three dimensional” storage is insufficient to disclose the specific three-dimensional memory as claimed with wordlines arranged vertically “from bottom to top,” and therefore insufficient for anticipation. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008) (recognizing a reference “cannot anticipate” unless it “discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations *arranged or combined in the same way as recited in the claim*”); Khatri2, ¶¶188-189.

Petitioner does not explain, for example, why an ambiguous reference to “three dimensional” storage would necessarily have taught arranging wordlines vertically from bottom to top, rather than horizontally. *See Wasica Fin. GmbH v.*

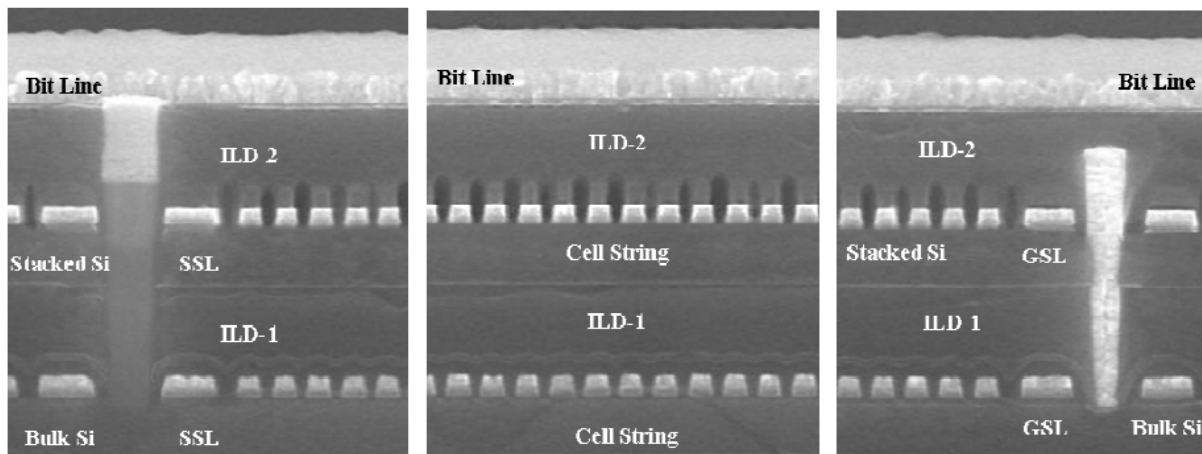
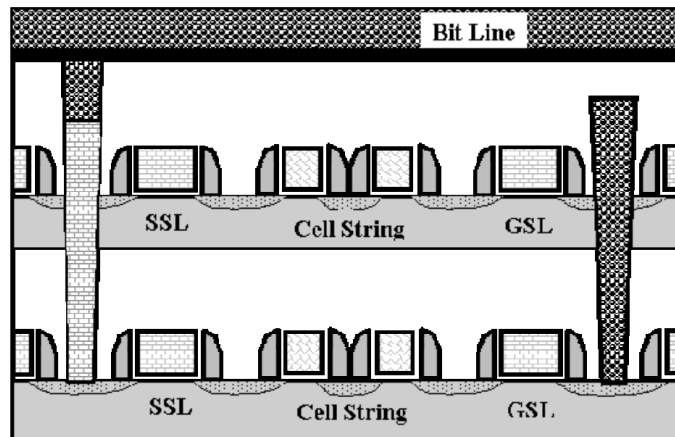
Cont'l Auto. Sys., Inc., 853 F.3d 1272, 1284 (Fed. Cir. 2017) (“Ambiguous references do not anticipate a claim.”); *Guangdong Alison Hi-Tech Co. v. Int’l Trade Comm’n*, 936 F.3d 1353, 1364 (Fed. Cir. 2019) (recognizing an element is inherently disclosed “only if it is necessarily present, not merely probably or possibly present”) (quotations omitted). That Petitioner does not try to do so is unsurprising. As explained in the following section, a reference to “three dimensional” storage would not have taught arranging wordlines vertically as recited. *Khatri2*, ¶¶188-189.

a. A POSITA Would Not Interpret Dong’s “Three Dimensional” Disclosure To Refer To Vertically Arranged 3D NAND

Petitioner improperly assumes that Dong’s single mention of “three dimensional” memory discloses the claimed vertical wordlines arranged “from bottom to top,” but that is hindsight. Petitioner provides no evidence or basis for this assumption. A POSITA would not have understood Dong’s vague mention of “three dimensional” to disclose the specific memory structure with wordlines arranged vertically “from bottom to top” as recited. *See Wasica*, 853 F.3d at 1285 (“[B]road invocation of ‘any modulation scheme’ (a genus) does not disclose with sufficient particularity the constant-frequency modulation scheme of claim 6 (a species).”); *Khatri2*, ¶¶190-195.

A POSITA would have interpreted Dong’s mention of “three dimensional” memory arrays as naturally referring to 3D memory arrays that were known as of

Dong's May 7, 2007 date, like Stacked and Multi-layer TFT 3D NAND that did not have vertically arranged wordlines as recited. Khatri2, ¶¶190-195. Those three-dimensional memory arrays had stacked layers of *horizontal* 2D NAND arrays, with wordlines arranged *horizontally* as shown below (as in Dong), not arranged vertically "from bottom to top" as recited.



Ex. 2008, 3, Figs. 3, 4; Ex. 2009, 4; Khatri2, ¶191. Moreover, Petitioner provided no evidence or support that Dong's disclosure of "three dimensional" would be interpreted by a POSITA to disclose the vertical 3D NAND implementation over the

non-vertical arrangements like Stacked and Multi-layer TFT NAND. Khatri2, ¶192. Instead, a POSITA would interpret Dong's mention of "three dimensional" as applying to 3D memory arrays to which Dong's 2D NAND voltage schemes (e.g., Figures 5a and 5g) are applicable like Stacked and Multi-layer TFT NAND, which include multiple layers of 2D NAND. Khatri2, ¶¶192-195.

Moreover, Dong's single reference to a "three dimensional" array of storage elements does not provide enough information for a POSITA to make and use a three-dimensional memory as claimed with wordlines arranged vertically "from bottom to top." *See Forest Laboratories, Inc. v. Ivax Pharms., Inc.*, 501 F.3d 1263, 1268, (Fed. Cir. 2007) ("A reference that is not enabling is not anticipating."); *Impax Laboratories, Inc. v. Aventis Pharms., Inc.*, 545 F.3d 1312, 1314 (Fed. Cir. 2008) ("In order to anticipate a claimed invention, a prior art reference must enable one of ordinary skill in the art to make the invention without undue experimentation."); Khatri2, ¶194. A POSITA would also not understand Dong's disclosure of "three dimensional" to refer to vertically arranged 3D NAND because a POSITA would not apply Dong's 2D self-boosting voltage schemes to 3D NAND. *See infra* Section III.B.2.c; Khatri2, ¶195.

2. No Obviousness

a. Petitioner Did Not Argue That A POSITA Would Apply Dong's 2D Program Disturb Method In 3D NAND

Petitioner had nothing more than obviousness handwaving if its construction was not adopted, and for good reason—the suggestion of 3D Memory in Dong was not a suggestion to use a vertical orientation, so Petitioner glossed over it.

Importantly, Petitioner *never argued in its Petition* that it would be obvious to apply Dong's voltage schemes of Figures 5a and 5g in a 3D NAND context. Despite that fact, the Board improperly raised a new position: “We understand the Petition to assert that a POSITA would have understood Dong's method could be applied to a 3D NAND memory device having vertically oriented wordlines.” ID, 25; *see In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (reversing where the Board mixed arguments raised in two different grounds of obviousness in the petition to craft its own new theory of unpatentability). Petitioner made no such argument. Khatri2, ¶¶196-200.

Petitioner also *did not argue* that it would have been obvious to modify Dong's horizontally arranged wordlines into the vertically arranged wordlines as recited. Petitioner instead chose to rely on Dong's disclosure, stating:

Regardless, to the extent bottom to top is interpreted to require vertical strings in a 3D NAND memory, Dong discloses its “array of storage elements can be three dimensional” and shows Fig. 5a in a vertical orientation which satisfies the claim. Dong, [0095]; Liu, ¶ 120.

Pet. 35. And as discussed, Dong's sole mention of "three dimensional" does not disclose vertical wordlines. Khatri2, ¶¶196-198.

Petitioner's sole obviousness modification in Ground 2 has nothing to do with the claim requirement that wordlines are arranged "from bottom to top." Pet. 30-31. Petitioner merely states that "it would have been obvious to a POSITA to utilize a 32-cell memory string," argues doing so was "well-known to POSITAs," and provides three reasons why a POSITA would "utilize a 32-cell memory string." Pet. 31; *see* Liu, ¶¶109-110. Thus, with respect to the claim limitation "from bottom to top," Petitioner's Grounds 1 and 2 are identical and fail for the same reason—there is no teaching of wordlines arranged from "bottom to top" in Dong. Khatri2, ¶¶198-199. And as explained above in Section III.B.1.a, a POSITA would not have interpreted Dong's mention of "three dimensional" as disclosing vertical 3D NAND. Khatri2, ¶199.

Petitioner cannot use the fact that it made one specific obviousness theory in the Petition as a license to raise any other type of obviousness theory simply by asserting "obviousness" in the Petition. Because Petitioner never raised an obviousness argument for the claim limitation "from bottom to top" in its Petition, no such theory is available to the Petitioner or the Board in this proceeding. *See M & K Holdings, Inc. v. Samsung Elecs. Co.*, 985 F.3d 1376, 1384-86 (Fed. Cir. 2021) (vacating and remanding because the "Board deviated impermissibly from the

invalidity theory set forth in Samsung's petition"); *Oren Techs., LLC v. Proppant Express Invs. LLC*, No. 2019-1778, 2021 WL 3120819, at *4-5 (Fed. Cir. July 23, 2021) (finding "the Board erred by repurposing the theory of a motivation to modify" not presented in the petition); Khatri2, ¶200.

b. Conclusory Expert Testimony Does Not Remedy Petitioner's Fatal Flaw

Petitioner's expert states in a bare, conclusory manner that "given the similarities between 2D and 3D NAND discussed in the Technology Background section, even a 2D memory string would at a minimum render obvious the *bottom to top* requirement, even if narrowly construed." Liu, ¶120; Khatri2, ¶¶201-206. But even if this conclusory testimony in Petitioner's expert declaration could be considered (which it cannot because this argument is not in the Petition), it does not help Petitioner. *Compare* Pet. 35, *with* Liu, ¶120. Petitioner's expert offers no explanation to support this *ipse dixit* testimony, let alone sufficient motivation to combine or reasonable expectation of success.

Neither Petitioner, nor its expert, rely on the Technology Background section to support the idea (not present in the Petition) that a POSITA would have been motivated to modify *Dong's* specific program disturb mechanism to apply to 3D NAND. *See* ID, 25. Instead, Petitioner's Background section merely describes the generic development from *2D NAND* to 3D NAND, stating "there are many similarities between 2D and 3D NAND flash memory devices." Pet. 14. Petitioner's

actual Grounds alleging unpatentability (Pet. 28-84) *never* refer to Petitioner's Technology Background section, let alone rely on these "similarities" to support an articulated rationale to apply Dong's 2D NAND program disturb schemes in a 3D NAND context. And even if they did, a mere "statement of similarity ... does not constitute an articulated reasoning with rational underpinning as to why a POSITA would combine elements of one reference with another, and why a POSITA would modify the teachings of the references to arrive at the claimed invention." *William Wesley Carnes, Sr., Inc. v. Seaboard Int'l Inc.*, No. IPR2019-00133, Paper 10 at 16-18 (PTAB May 8, 2019); *see also DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1376-77 (Fed. Cir. 2018) (holding "similarities in transmission hardware" insufficient for a motivation to combine "without additional, reasoned analysis"); Khatri2, ¶¶202-203. In fact, Petitioner's Background section describing the generic development from 2D NAND to 3D NAND is not unique to this IPR—it is mere boilerplate inserted into numerous other Micron Petitions. *Compare* Pet. 11-14, *with, e.g.*, IPR2025-00189, Paper 1 at 14-17; IPR2025-00035, Paper 1 at 13-15; IPR2025-00117, Paper 1 at 15-17; IPR2025-00228, Paper 1 at 16-17; IPR2025-00294, Paper 1 at 12-13; *and* IPR2025-00245, Paper 1 at 14-15; Khatri2, ¶204.

Petitioner cannot now advocate an obviousness argument not made in the Petition by citing its expert's declaration. *See* 37 C.F.R. § 42.6(a)(3) ("Arguments must not be incorporated by reference from one document into another document.");

3M Co. v. Evergreen Adhesives, Inc., 860 F. App'x 724, 726 (Fed. Cir. 2021) (affirming PTAB's decision that 3M failed to meet its burden because "3M's filings never sufficiently made the relevant 'contention' or argument at all, and instead supported 3M's position entirely by reference to [its expert's] declarations and testimony"); 37 C.F.R. § 42.22(a)(2); Khatri2, ¶205.

Even if Petitioner had relied on its expert's conclusory testimony (it did not), the Petition is still fatally flawed because it offers no rationale or articulation as to how or why a POSITA would have been motivated to modify Dong's voltage waveform to apply to the claimed vertically arranged 3D NAND, let alone have had a reasonable expectation of success in doing so. Khatri2, ¶¶205-206. That is, Petitioner "fails to explain why a person of ordinary skill in the art would have combined elements from specific references in the way the claimed invention does." *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012) (citing *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007)). Petitioner's expert's conclusory assertion of obviousness cannot meet Petitioner's burden as a matter of law. *KSR*, 550 U.S. at 418 (An assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."); see, e.g., *Apple Inc. v. Voip-Pal.com, Inc.*, 976 F.3d 1316, 1325 (Fed. Cir. 2020) (The Board maintained "the proper evidentiary

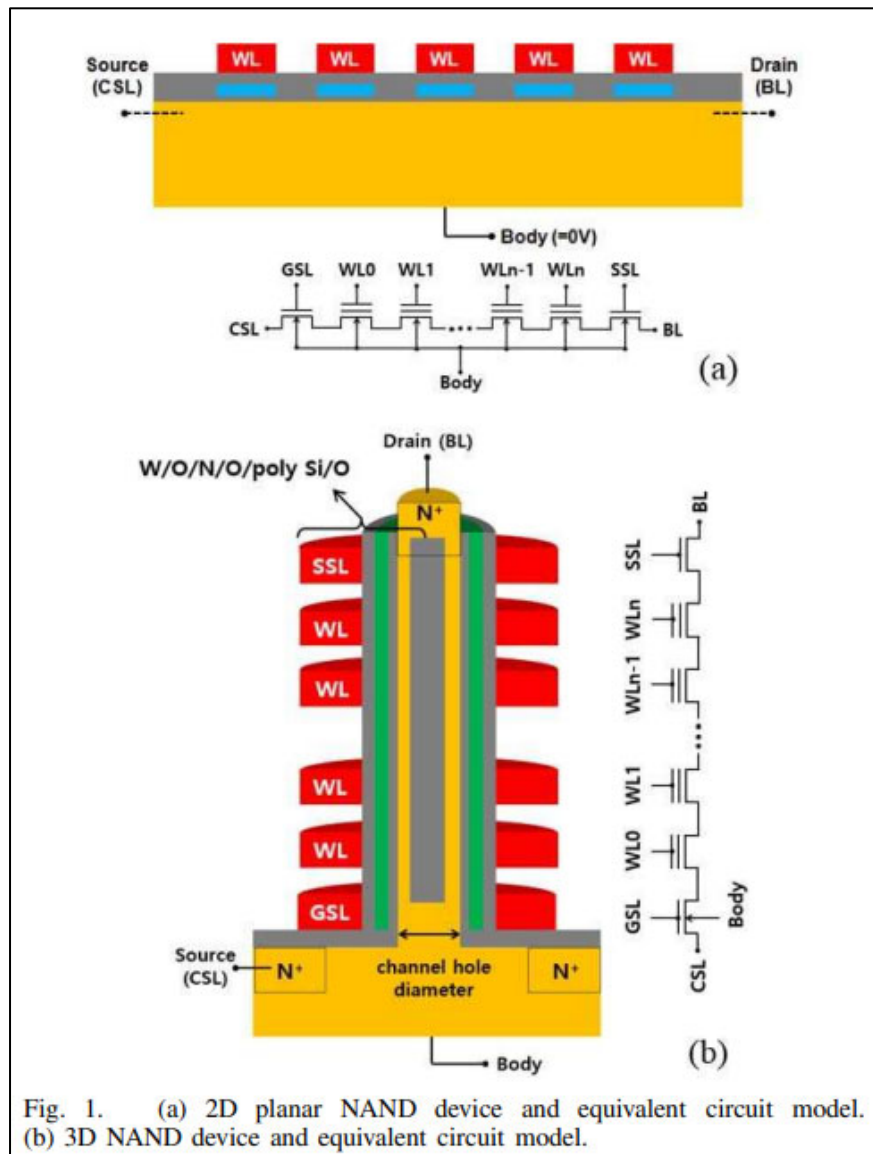
standard” by rejecting expert testimony that provided “only ‘conclusory and insufficient’ reasons.”); *Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017) (conclusory expert testimony insufficient for Petitioner to “meet its burden of presenting a sufficient rationale to support an obviousness conclusion”); *TQ Delta, LLC v. CISCO Sys., Inc.*, 942 F.3d 1352, 1358 (Fed. Cir. 2019) (“Conclusory expert testimony does not qualify as substantial evidence.”).

c. A POSITA Would Not Apply Dong’s 2D NAND Program Disturb Method In A 3D NAND Context

Dong’s 2D NAND isolation voltage scheme is a planar solution that a POSITA would not apply in vertical 3D NAND as of the priority date of the ’941 Patent. Khatri2, ¶¶48-83, 207-220. As Petitioner’s exhibit recognizes: “The program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed.” Ex. 1009, 354; *see id.*, 356 (“The program disturb conditions and characteristics of 3D cells are greatly changed from that of 2D cells.”), 362 (“Program disturb phenomena and mechanisms of a 3D NAND cell are much different from that of a 2D NAND cell.”). A POSITA would understand that “3D NAND flash memory has a different structure from 2D NAND flash memory, so new phenomena occur.” Ex. 2024, 1; Khatri2, ¶¶207-220.

Vertical 3D NAND operates on different physical principles and experiences different electrical phenomena that are not addressed by Dong’s program disturb

methods designed for 2D NAND. Khatri2, ¶¶208-211. Vertical 3D NAND strings have floating bodies, i.e., the channel is not directly connected to a substrate like a 2D NAND planar string. Khatri2, ¶212. For example, as seen in the below comparison between 2D and 3D NAND structures and circuit models, each floating gate in 2D NAND structure is connected to the body (i.e., substrate).



Ex. 2025, 1, Fig. 1; Khatri2, ¶212. The memory cells of the 3D NAND arrangement are on an ultra-thin body structure instead of a traditional substrate. Ex. 2025, 1, Fig. 1; Ex. 2026, 1. As a result, “body bias cannot be applied to the channels of main cells during read and program operations.” Ex. 2025, 1. That is, unselected channels (i.e., inhibited channels) in the 3D NAND structure “can easily be in the floating state [(i.e., it has a high impedance)], because its channel is not directly connected to its body.” *Id.*; Ex. 2027, 1; Ex. 2024, 1; Khatri2, ¶213.

“[D]uring program operation, the inhibited channel becomes a floating node and the **natural local self-boosting (NLSB)** effect occurs.” Ex. 2024, 1; Ex. 2027, 1; Ex. 2026, 1. NLSB localizes channel boosting for inhibited channels near the selected wordline rather than uniformly along the string. Ex. 2024, 1. This means that when the selected wordline is driven with V_{PGM} , the inhibited channel is locally boosted to a high voltage near the selected wordline, due to the ultra-thin body (floating) which results in a significantly reduced program disturb. Khatri2, ¶214.

This NLSB effect in 3D NAND prevents program disturb of inhibited strings without 2D NAND self-boosting techniques. In 3D NAND, boosting occurs naturally due to the vertical 3D NAND structure and the NLSB effect caused by the high-impedance ultra-thin body. In other words, “the selected WL cell is **localized automatically** during the program pulse application.” Ex. 2024, 1. A POSITA would understand that “[t]he NLSB effect does not require the local boosting scheme

used in conventional 2D NAND, because it can achieve a sufficiently high potential even if the number of stacks is increased.” Ex. 2027, 1; Khatri2, ¶215. In other words, “[t]he NLSB effect allows a sufficiently high boosted potential of an inhibited string to be achieved *without* a local self-boosted program-inhibit (SBPI) scheme” that includes an isolation wordline to isolate the selected wordline. *See* Ex. 2024, 1, Fig. 1; *id.*, 2, Fig. 3.

A POSITA would thus not have been motivated to apply Dong's local self-boosting methods shown in Figures 5a and 5g—which both include an isolation voltage applied to specific wordlines—to a vertical 3D NAND context as of the priority date of the '941 Patent. Khatri2, ¶216. Put simply, because NLSB occurs without any local-boosting tricks, a POSITA would not have been motivated to look to Dong to try to solve any problem in vertical 3D NAND. Ex. 2024, 3, Fig. 3; Khatri2, ¶216.

Moreover, implementing an isolation voltage (i.e., applying V_{ISO}) in 3D NAND (as done in Dong and in Exhibit 2024's Figure 1b) would be counterproductive during a program operation. Khatri2, ¶218. In vertical 3D NAND, in an inhibit string, V_{PASS} is driven to unselected wordlines, boosting the high-impedance channel voltage, and reducing program disturb. However, applying an isolation voltage to an unselected wordline (as suggested in Dong's Figure 5a, and also illustrated in Exhibit 2024's Figure 1b) results in a reduced voltage coupled

to the high-impedance channel, which reduces the boost voltage, and worsens program disturb. Khatri2, ¶218. Moreover, when the potential difference between the selected wordline (receiving V_{PGM}) and its neighbor (receiving V_{ISO}) increases, hot carrier injection occurs, which causes program disturb due to the significant channel electrical field that traps carriers in the floating gate that change the threshold voltage of unselected cells (i.e., program disturb). *See* Ex. 2027, 1 (“When the channel potential of the WL selected by the NLSB is increased, a large difference is generated in the channel potential of the adjacent WL, which results in a HCI phenomenon.”); Khatri2, ¶219. A POSITA would therefore avoid applying V_{ISO} to unselected wordlines in vertical 3D NAND. Ex. 2027, 1; Khatri2, ¶219.

A POSITA would further understand that the NLSB phenomenon being unique to 3D NAND explains why application of local self-boosting and erase area self-boosting schemes (i.e., those that apply little to no voltage to a wordline adjacent to the programming wordline) are cabined to 2D NAND. *See, e.g.*, Ex. 1009, 52-54; Khatri2, ¶220. To address program disturbance in 3D NAND, other methods are used, including “(1) high V_t of DSL, (2) applying negative bias to DSL, and (3) inserting dummy wordlines between DSL and edge wordline.” Ex. 1009, 363-64.

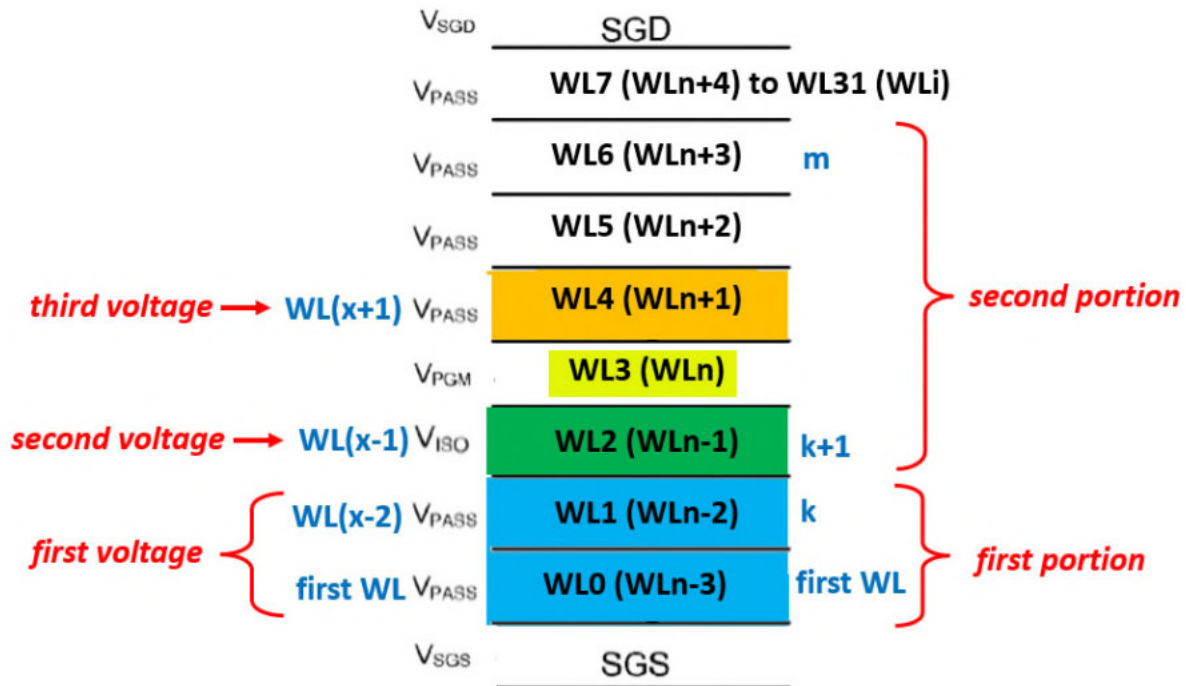
IV. Ground 3: Dong In View Of Costa Fails To Render Obvious Claims 8-9**A. Dong And Costa Fail To Render Obvious Wherein “The First Voltage Has A First Level If The Xth Wordline Is In The First Portion”**

Petitioner's application of Dong to independent claim 5 fails when carried forward to address claims 8 and 9. Khatri2, ¶¶221-227. For example, Petitioner's position for claim 5 places the xth wordline in the “second portion,” but claims 8 and 9 require the xth wordline to be in the “first portion.”

Claim 8 depends from claim 7, which depends from claim 5. Claim 9 also depends from claim 5. Claims 8 and 9 both recite wherein “the first voltage has a first level if the xth wordline is in the *first portion*.” Claim 5, from which claims 8 and 9 depend, defines “a *first portion*” as “comprising a first wordline to a kth wordline from bottom to top.” Claim 5 also requires an “xth wordline,” defining “x” as positive integer wherein “ $3 \leq x$.” Khatri2, ¶222.

For claim 5, Petitioner maps the recited “first portion” to the first two wordlines shown in Dong's Figure 5a—defining “WL0 (WL_n-3)” as the “first WL” and “WL1 (WL_n-2)” as the “kth wordline” (both in blue highlight below):

Fig. 5a



Pet. 33 (yellow highlighting added); *see also id.*, 36-37. Petitioner also argues the “claimed *x*th wordline corresponds to the selected wordline WLn in Dong Fig. 5” (Pet. 38), which is highlighted in yellow above. Pet. 33. As seen above, Petitioner depicts the *x*th wordline in the “second portion.” *Id.*; Khatri2, ¶223.

Petitioner assigns to “*x*” a value of “4,” which means the *x*th wordline is the 4th wordline from SGS (i.e., “WL3 (WLn)” in yellow highlight above), to meet the additional requirement of claim 5 that “*x*” is a positive integer wherein “ $3 \leq x$.” Pet. 33; *see also id.*, 43-44; Khatri2, ¶224.

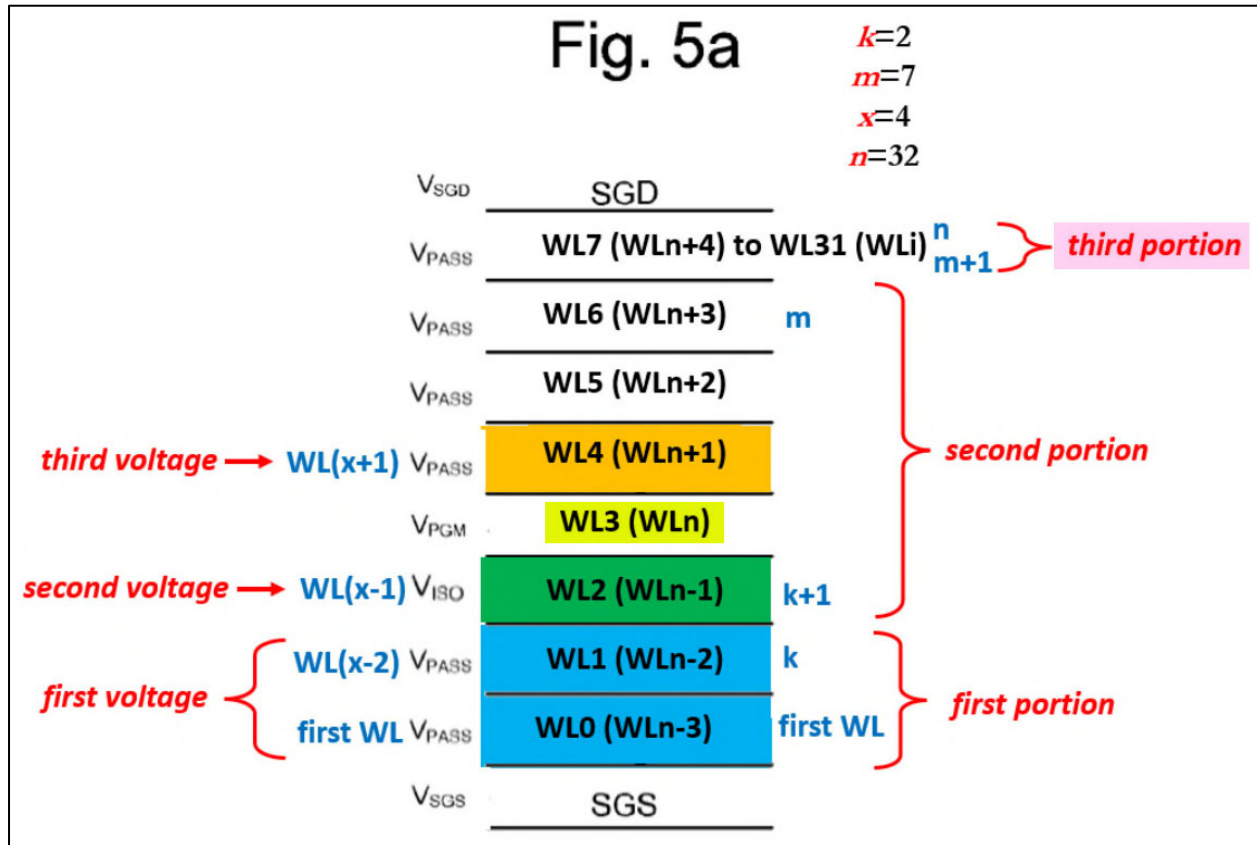
$k = 2$	$WL(m) = WL6$	$WL(x+1) = WL(n+1) = WL4$
$m = 7$	$WL(k+1) = WL2$	$WL(x) = WL(n) = WL3$
$x = 4$	$WL(k) = WL1$	$WL(x-1) = WL(n-1) = WL2$
	$first\ wordline = WL0$	$WL(x-2) = WL(n-2) = WL1$

Pet. 33; *see also id.*, 43-44. As shown above, the fourth wordline is in the “second portion.”

Petitioner's arguments fail for claims 8 and 9 because these claims require the xth wordline to be in the “*first portion*”—an impossibility given Petitioner's positions for claim 5. Khatri2, ¶225. Specifically, both claims 8 and 9 recite that “the first voltage has a first level *if the xth wordline is in the first portion.*” Petitioner's arguments for claim 5 ensure the xth wordline will *never* be in the first portion. As described above, Petitioner defined the “first portion” as the first two wordlines and defined “x” as 4. Pet. 33. To be in the “first portion” as Petitioner defines it, the xth wordline would need to be one of the first two wordlines. But the xth wordline cannot be in Petitioner's “first portion,” as required by claims 8 and 9, because “x” cannot be less than 3, as required by claim 5. Worse, Petitioner and its expert provide no basis for how the xth wordline can be in the recited “first portion.”

Petitioner similarly fails to show how Dong and Costa meet the limitation of claim 8 that requires the “xth wordline” to be “in the third portion,” which is “formed above the second portion.” Ex. 1001, cls. 7-8; Khatri2, ¶226. Petitioner defines the

“third portion” (highlighted below in pink) as extending from “an (m+1)th wordline [WL7] to an nth wordline [WL31] from bottom to top.” Pet. 47.



Pet. 46-47. Petitioner also defined “x” as 4, placing the xth wordline at WL3 (highlighted in yellow) in the “second portion.” *Id.*, 43, 49. To be in the “third portion” as Petitioner defines it, the xth wordline would need to be within the range of WL7 to WL31. Again, Petitioner and its expert fail to show or explain how the xth wordline can be in the recited “third portion”—despite recognizing claim 8 requires that “the wordline used for programming (*i.e.*, the *xth wordline*) moves up the memory string from the *first portion* to the *second portion*, to the *third portion*.” See Pet. 74; Liu, ¶214.

Costa does not resolve these deficiencies because Petitioner relies on Dong to disclose the recited positioning of the xth wordline relies, not Costa. *See* Pet. 74 (“Dong satisfies the underlying elements of claims 5 and 7.”); *id.*, 75-77; Khatri2, ¶227.

B. Dong And Costa Fail To Disclose “Applying A First Voltage” In Recited Portions During “A Program Operation”

Petitioner argues that Dong combined with Costa renders obvious claims 8-9. Pet. 70. But Petitioner admits that “Dong is silent” on these claims (Pet. 2), including “regarding how V_{PASS} (and other programming voltage values) change as the cell being programmed advances from the source end of a memory string to the drain end.” Pet. 72; *see also* Liu, ¶215. Costa does not disclose the missing limitations. But even if it did, a POSITA would not have been motivated to combine Dong with Costa as Petitioner suggests. Khatri2, ¶¶228-247.

Petitioner alleges for claims 8 and 9 that the “claimed V1 voltage (*viz.*, Dong’s V_{PASS} voltage)” is modified by Costa such that it is “applied to the previously programmed cells in a memory string” and increases “as the cell being programmed moves” upward from the first portion to the third portion. Pet. 76-77; Liu, ¶¶220-221; Khatri2, ¶229.

But during deposition, Dr. Liu changed his position. Rather than modifying “Dong’s V_{PASS} voltage” as set forth in the Petition (Pet. 76-77), Dr. Liu testified that Dong and Costa are combined as two separate processes to address claims 8 and 9:

Dong discloses applying a program voltage to transfer charge to change a cell's threshold voltage and Costa discloses a subsequent verification phase. Liu Dep., 159:17-161:18, 152:20-155:13; *see also id.*, 158:2-20. As with Dr. Liu's new claim construction position regarding "a program operation," this new position is improper. Khatri2, ¶230

For the reasons below, all of Petitioner's positions fail.

1. Dong And Costa Fail To Disclose "Applying A First Voltage" In Recited Portions During "A Program Operation" Under Patent Owner's Correct Interpretation

The claims require that "a first voltage" is applied during a program operation. Claim 5, from which claims 8 and 9 depend, requires a "program method of a memory ... comprising: *applying a first voltage* to the first wordline to an (x-2)th wordline *when an xth wordline is used to perform a program operation.*" Ex. 1001, cl. 5. Claims 8 and 9 further recite that "*the first voltage*" has a specific level depending on whether the xth wordline is in the first, second or third portion. These claims do not focus on a verify phase but instead recite "applying a first voltage" *during* a distinct program operation (i.e., an operation performed by applying a program voltage to a selected wordline to program a selected memory cell). *See* Pet. 38-39; *see supra* Section II.G.2; Khatri2, ¶231.

Costa does not disclose "applying a first voltage" during a program operation as claimed because it describes applying read voltages during a verify operation.

Khatri2, ¶¶232-235. Petitioner implies that Costa discloses “a variable pass voltage” during a program operation (Pet. 72-73, 75; Liu, ¶¶210, 212, 217). Petitioner even misrepresents Costa by stating it “specifically discloses that V_{PASS} increases (for wordlines below the cell being programmed) as programming proceeds up the memory string.” Pet. 74. But Costa discloses a read/verify waveform and adjusting read/verify pass voltage (e.g., V_{read})—*after* “a program operation.” *See e.g.*, Costa, ¶31 (“[T]he pass voltage applied *when reading* the earlier programmed memory cells is higher relative to the pass voltage applied *when reading* the later programmed memory cells.”). Put differently, Costa’s “variable pass voltage” is a variable read/verify pass voltage applied to “cells that have already been subject to programming,” not a variable program V_{PASS} . Costa, ¶¶30-33 (describing use of “*the* variable pass voltage” in reference to read voltage applied to “unselected memory cells that have already been subjected to programming”), Figs. 8-10 (applying V_{read}); *see also id.*, ¶¶96, 104, 110-111, 114-116; Liu, ¶¶90-91; Khatri2, ¶¶233-235. As Dr. Liu previously testified about this Costa reference: “Costa teaches adjusting voltages for verify operations *alone*.” Ex. 2023, ¶72; *see also* Pet. 71 (Costa “focuses on addressing program disturb impacts arising from the verification phase.”); Ex. 2022, ¶248 (“Costa discloses using its read operations to verify programming.”). In short, neither Dong nor Costa teach the limitations of these claims.

a. A POSITA Would Not Have Been Motivated To Modify Dong's Programming Waveform

As an initial matter, Petitioner provides no articulated rationale explaining how or why a POSITA would make this specific modification to Dong, inspired instead purely by hindsight. Khatri2, ¶¶236-237. When addressing claims 8 and 9, Petitioner provides no motivation to modify Dong such that Dong's V_{PASS} voltage (i.e., Petitioner's "first voltage," Pet. 41) increases as programming advances up the memory string. See Pet. 76. Instead, Petitioner states that "[t]he reasons for combining Dong and Costa are discussed in §XI.A" (i.e., Pet. 70-74). Pet. 74. But Petitioner's high-level, generic motivation in the referenced §XI.A fails to explain why a POSITA "would have combined elements from specific references in the way the claimed invention does." *ActiveVideo*, 694 F.3d at 1328; Khatri2, ¶237. Petitioner provides an *entirely different combination* of Dong and Costa in §XI.A, whereby Dong provides the program phase and Costa provides the verify phase.

Moreover, a POSITA would not have been motivated to modify Dong's program disturb schemes designed for a *program* phase when considering Costa's disclosure of a *verify* phase. Khatri2, ¶236. That is, a POSITA would not have been motivated to modify Dong's V_{PASS} voltage (Petitioner's "first voltage") as Petitioner suggests when addressing claims 8-9 (Pet. 76), because Costa's disclosure is focused on the verification/read operation of wordlines already programmed—not the program operation as recited. Khatri2, ¶¶236-238.

First, as Petitioner admits, Dong and Costa address “two different ... phenomena”—Dong addresses program disturb during programming and Costa addresses verification of cells already programmed. Pet. 71-72. Program disturb occurs during programming of cells, not during read or verification. See Pet. 1, 15, 23. A POSITA would not modify the program disturb method disclosed in Dong with the read or verification method of Costa—both describe different voltage applications for distinct purposes. Khatri2, ¶239.

Second, Petitioner alleges that a POSITA would “investigate and apply techniques (like Costa’s) to address *program disturb/errors* that occur as function of the location of a cell being programmed within a memory string” because “Dong describes a program disturb issue that occurs as programming advances along a memory string.” Pet. 73 (citing Dong, ¶11); Liu, ¶¶211-212. But this statement refers to Petitioner’s generic motivation regarding joining the “mutually compatible” program and verify phase disclosures of Dong and Costa respectively (Pet. 73), not modifying Dong’s “first voltage” as programming progresses (Pet. 76). As described above, Costa addresses a read/verification issue regarding increased channel resistance for programmed cells (i.e., “back-pattern effect”)—not program disturb. Pet. 25-26; see Liu, ¶¶82, 89, 209. Petitioner provides no rationale as to why Costa’s disclosure regarding a verify phase would apply to Dong’s program

phase, much less that there would be a reasonable expectation of success in doing so. Khatri2, ¶¶240-241.

Third, Petitioner's combination is purely derived from hindsight. Nothing in Dong or Costa teaches increasing a pass voltage for wordlines below the cell being programmed during the program phase, much less that this reduces program disturb or errors as programming advances along a memory string. *Metalcraft of Mayville, Inc. v. Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) (“[W]e cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention.”) (citation omitted); Khatri2, ¶242.

2. Dong And Costa Fail To Disclose “Applying A First Voltage” In Recited Portions During “A Program Operation” Under Petitioner’s Incorrect Interpretation

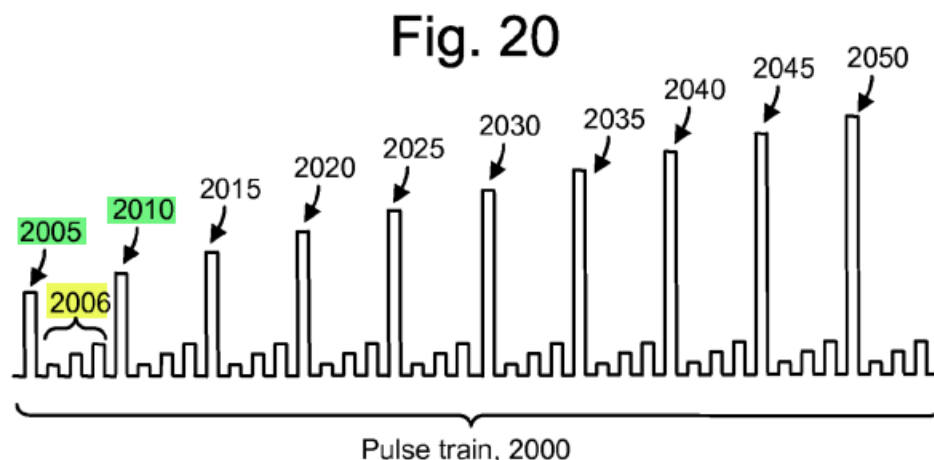
Petitioner's position also fails under Dr. Liu's new interpretation of “a program operation” (as including both a programming phase and a verify phase), which does nothing to address the fatal flaws raised in the previous section. *See supra* Section IV.B.1; Khatri2, ¶¶243-247. Under this new interpretation, Petitioner still applies Dong's V_{PASS} —used in a program phase—as the “**first voltage**.” Pet. 38-39. Even if Petitioner added Costa's verify disclosure after Dong's program disclosure to address claims 8 and 9 (Petitioner did not as seen at Pet. 76), Petitioner still fails to meet claims 8 and 9 which require “**the first voltage**” (i.e., Dong's V_{PASS}) to increase as the selected wordline moves up the memory string. Neither Costa nor

Dong disclose that limitation. And a POSITA would not modify Dong according to Costa for the reasons explained above. *Supra* Section IV.B.1.a; Khatri2, ¶¶243-247.

a. A POSITA Would Not Have Been Motivated To Supplement Dong's Programming Process With Costa's Verification Process

Petitioner's motivation to combine Dong and Costa (Pet. 70-74) focuses on supplementing Dong's programming process with Costa's verification process: "[c]ombining both teachings would address memory cell errors introduced during *both* phases of the program operation (*viz.*, the *programming* pulse and the *verification* pulse)." Pet. 73; *see id.*, 71; Liu, ¶¶211-213.

A POSITA would not have been motivated to combine Dong and Costa as Petitioner proposes because Dong already discloses a verification operation separate from its programming operation, which Petitioner did not address. Khatri2, ¶¶244-247. Dong discloses that "[i]n between the program pulses are verify pulses" as seen in verify pulse set 2006 (yellow) between program pulses 2005 and 2010 (green).



Dong, ¶132, Fig. 20. Dong discloses how boost voltages “are applied to wordlines to implement a boost mode are applied *when* programming occurs, e.g., prior to and during a program pulse,” but that “during the verify process, ... the boost voltages are not applied.” Dong, ¶133; *see also id.*, ¶¶9, 50, 71; Khatri2, ¶245.

Petitioner's expert argues that a POSITA would have been motivated by the fact that “Dong says nothing about increased channel resistance or how to address it.” Liu, ¶211. A POSITA would not have been motivated by Dong's silence on this issue, let alone be motivated to “investigate techniques that could address programming disturb or programming errors,” as Dr. Liu suggests. Khatri2, ¶246; *see* Liu, ¶211. And even if a POSITA were motivated to seek out such a solution, a POSITA would not look to Costa which does not focus on program disturb. Khatri2, ¶¶246-247. In any case, Petitioner fails to allege that this combination renders obvious claims 8 or 9. *See* Pet. 74-77.

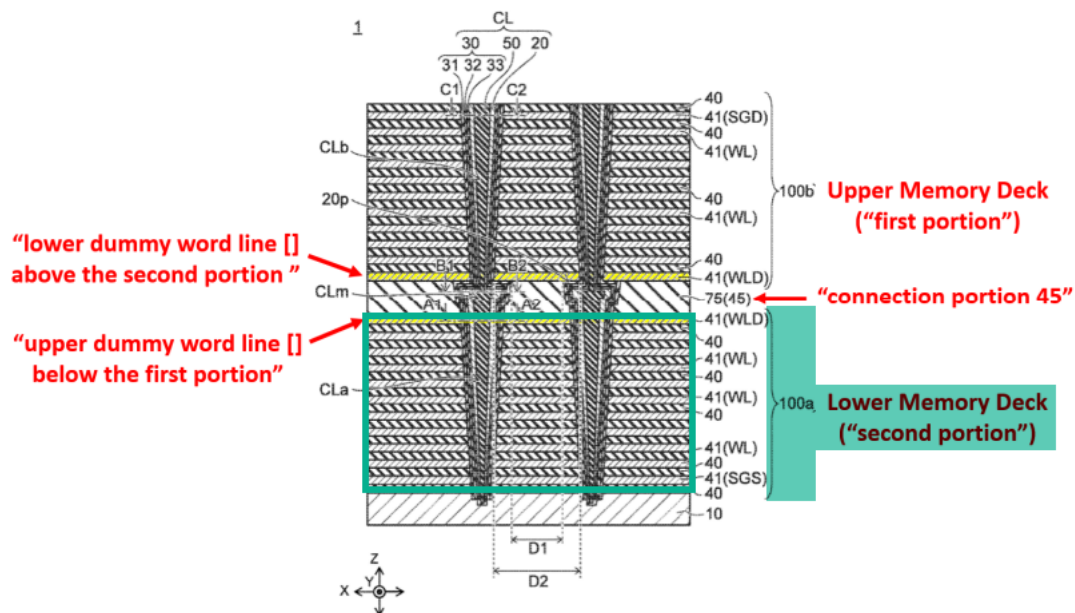
V. Ground 4: A POSITA Would Not Have Been Motivated To Modify Dong With Shirai's Disclosure

Petitioner alleges Dong and Shirai render obvious claims 4, 10, and 14, which depend from respective claims 1, 5, and 11. Pet. 77.

A. A POSITA Would Not Have Applied $V_{\text{PASS-LOW}}$ To The Entire Lower Memory Deck of Shirai

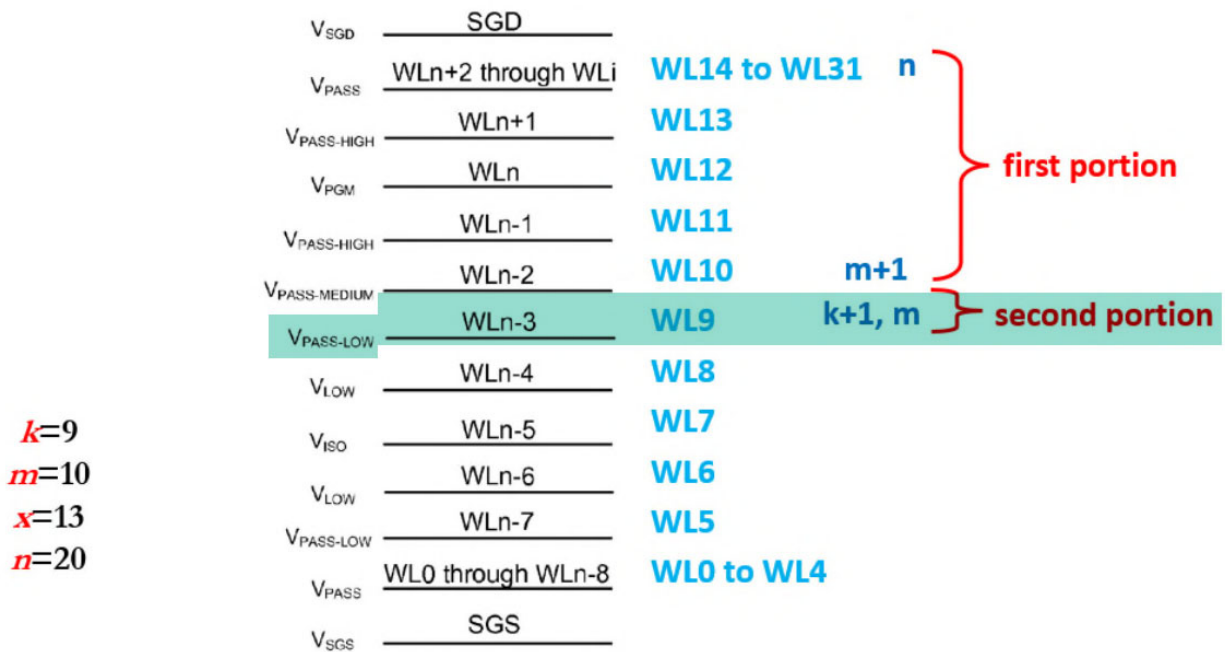
Petitioner relies on the below annotated Figure 2 of Shirai to represent its position regarding claim 4:

FIG. 2



Pet. 80-83 (annotating Shirai Fig. 2; teal annotations added by Patent Owner); Liu at 121; Liu Dep., 167:1-7. Petitioner states, “[r]ecall that in base claim 1, the second portion [is] formed below the first portion,” and admits that “Dong’s second portion corresponds to Shirai’s bottom deck 100a.” Pet. 82; Liu, ¶232; *see also* Liu Dep., 178:7-179:17. But Petitioner identifies a *single wordline* for Dong’s “second portion” of claim 1 (highlighted in teal below):

Fig. 5g



Pet. 54 (annotating Dong's Fig. 5g; teal annotation added by Patent Owner); *see also* Pet. 84. And the "second portion" of Dong relied on by Petitioner receives a voltage of $V_{PASS-LOW}$. Pet. 53-54. According to Petitioner's interpretation, the entire second portion in Shirai (see Figure 2 above) is driven with a voltage $V_{PASS-LOW}$. But Petitioner fails to explain how or why a POSITA would apply $V_{PASS-LOW}$ to Shirai's Lower Memory Deck 100a (which appears to comprise WL0 through WL8 based on the number of wordlines in Shirai's Figure 2) instead of, for example, V_{PASS} as disclosed in Petitioner's mapping of Dong (according to Petitioner, V_{PASS} is applied to WL0 through WL4). *See* Dong, Fig. 5g; Pet. 54; Khatri2, ¶¶248-251.

Moreover, a POSITA would not have been motivated to apply Dong's voltage scheme for a single wordline ($V_{PASS-LOW}$) to the entire Lower Memory Deck 100a of

Shirai, including WL0 through WLn-8. Khatri2, ¶¶251-253. Dong discloses that “V_{PASS} is applied to a first group of storage elements associated with WL0 through WLn-8, where the first group is adjacent to the source side select gate, and on a source side of the isolation wordline WLn-5.” Dong, ¶58;⁴ *see id.*, ¶51 (describing pass voltages applied to unselected wordlines near source and drain “reduce program disturb”). Dong also discloses “increasing the number of wordlines in between the selected wordline and the V_{ISO} wordline” and “*gradually* reducing the bias voltage on those wordlines” in order to reduce “the electric field in between the selected wordline and the V_{ISO} wordline,” thereby reducing program disturb (by reducing hot carrier injection (HCI) based program disturb). Dong, ¶57. But Petitioner’s combination goes against this by applying a single bias voltage (V_{PASS-LOW}) to every wordline of Shirai’s Lower Memory Deck 100a. And Dong discloses that, “[i]f V_{pass} is too low, boosting in the channel is insufficient to prevent program disturb.” Lutze, 4:19-21;⁵ Dong, ¶44 (recognizing a low V_{PASS} results in program disturb). POSITA would not be motivated to make Petitioner’s proposed combination

⁴ Petitioner admits that the description for Figure 5f “applies equally” to Figure 5g. Pet. 58 n.7.

⁵ Petitioner recognizes Dong incorporates Lutze (Ex. 1015) by reference. Pet. 30.

because it results in exactly that—applying a low V_{pass} (i.e., $V_{\text{PASS-LOW}}$) that reduces the boosting in the channel thereby increasing program disturb. Khatri2, ¶¶253-255.

Petitioner also never explains how or why a POSITA would omit V_{ISO} (or V_{LOW}) from the self-boosting mode as applied to WL7 (or WL6 and WL8) in Dong's Figure 5g when combining it with Shirai. Khatri2, ¶256. The elimination of V_{LOW} and V_{ISO} from Petitioner's combination of Dong and Shirai will result in a more abrupt change in channel voltage, and therefore an increased propensity toward program disturb due to HCI. Khatri2, ¶256-258. Moreover, Dong discloses that the isolation wordline is the mechanism that enables prevention of program disturb. Dong, Abstract; *see id.*, ¶¶67-68. That is why Dong discloses relying on an isolation wordline in every self-boosting mode to “isolate programmed and erased channel areas in the substrate.” *Id.*, ¶65; *see id.*, ¶¶66-67, Figs. 5a-5g, Title, Abstract. A POSITA would not have been motivated to omit Dong's isolation wordline (i.e., the one receiving V_{ISO}) whose sole purpose is to reduce program disturb. Khatri2, ¶¶256-259.

Petitioner's positions for claim 14 fail for the same reasons as claim 4 explained in this section. *See* Pet. 84 (“Claim 14 is identical to claim 4 and is met for the same reasons.”).

B. Petitioner Fails To Apply Prior Art To Claim 10

Petitioner fails to “show with particularity why [claim 10] is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). Instead, Petitioner provides a conclusory statement that “[c]laim 10 is substantively the same as claim 4 and is met for the same reasons.” Pet. 83. But Petitioner never explains how or why a POSITA would apply Dong’s voltage scheme of Figure 5a—which is completely different than in Dong’s Figure 5g applied to claim 4—to Shirai’s architecture. *See* Pet. 83-84; Khatri2, ¶¶260-261. Petitioner instead describes the differences between claims 4 and 10—without ever applying prior art. *Id.*

C. Petitioner Improperly Modifies The Value For The Recited “K” Limitation Used For Respective Independent Claims

Petitioner’s grounds for claims 4 and 14 are also fundamentally flawed because they each use a different interpretation for the variable “k” than independent claims 1 and 11, respectively. Khatri2, ¶¶262-267. For example, Petitioner fails to explain how or why variable k equals 9 when addressing claim 1, but the same variable k equals 0 when addressing claim 4. *Compare* Pet. 53 (“k can be taken as 9” for the recited “second portion ... comprising a (k+1)th wordline to an mth wordline from bottom to top”), *with id.*, 82-83 (depicting the recited “second portion” as the lower deck extending from the first wordline to the wordline just below the “upper dummy wordline,” resulting in k equal to 0). Petitioner never maps

claim 1 to Dong when k is 0. *See* Pet. 50-51; Liu, ¶154 (p. 79); Liu Dep., 67:2-19; Khatri2, ¶¶262-263.

Petitioner's allegations for claim 10 fail for the same reason. Khatri2, ¶264. Petitioner fails to explain how or why variable k equals 2 when addressing independent claim 5, but the same variable k equals 9 when addressing claim 10. *Compare* Pet. 43 (“k can be taken as 2” for the recited “first portion ... comprising a first wordline to a kth wordline from bottom to top”), *with id.*, 83-84 (Patent Owner assuming, without Petitioner explaining, that the “first portion” refers to Shirai's Lower Memory Deck 100a, in which case k equals 9); Shirai, Fig. 2 (showing 9 wordlines in the Lower Memory Deck 100a between “41(SGS)” to “41(WLD)”). Petitioner never provides a mapping for claim 5 assigning k a value of 9, much less explains how the variable k can be 9 and still satisfy the limitation in claim 5 that “ $k < m$ ” when Petitioner defined m as 7. *See* Pet. 34-38; Liu, ¶154 (p. 79); Liu Dep., 67:2-19; Khatri2, ¶265. Similarly, Petitioner never explains how m can equal 7 when addressing claim 5 but equal 18 for claim 10. *Compare* Pet. 38 (“m=7”), *with id.*, 83-84 (again, assuming, without Petitioner explaining, that the “second portion” refers to Shirai's Upper Memory Deck 100b, in which case m equals 18); Shirai, Fig. 2 (showing 9 wordlines in the Lower Memory Deck 100a between “41(SGS)” to “41(WLD)” and 9 wordlines in the Upper Memory Deck 100b between “41(WLD)” and “41(SGD)"); Khatri2, ¶266.

Petitioner's shifting theories of the prior art for claims 4, 10, and 14 contradict its positions for respective independent claims. *Khatri2*, ¶267. Petitioner thus fails to meet the requirement that the Petition "must specify where each element of the claim is found in the prior art patents or printed publications relied upon." 37 C.F.R. § 42.104(b)(4); *Harmonic*, 815 F.3d at 1363. Even if Petitioner were correct that "it was well-known that 3D NAND strings often exceed 100 cells by the Priority Date" (Pet. 77), it is unclear how that has anything to do with Petitioner's mappings. Petitioner fails to explain how the recited variables of the independent claims are accounted for in its allegations regarding claims 4, 10, and 14.

D. A POSITA Would Not Have Been Motivated To Combine Dong's 2D Disclosure With Shirai's 3D Disclosure

Petitioner's motivation to combine rests on the assumption that Dong's vague mention of "three dimensional" refers to vertical channel 3D NAND. Pet. 77-80. That is not the case, as explained above. *Supra* Section III.B. Petitioner's motivation to combine relies solely on etching issues unique to vertical 3D NAND as described in Shirai, but these do not apply to Dong. A POSITA would recognize that Dong does not have "challenges imposed by limitations on forming anisotropic vertical etch profiles" (Liu, ¶223) because Dong does not disclose vertical 3D NAND. *Khatri2*, ¶268.

VI. Conclusion

For the reasons set forth above, the Board should find the instituted claims patentable.

Respectfully submitted,

Dated: November 10, 2025

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(2) because the Patent Owner's Response contains a total of 13,989 words, which is the sum of 13,777 words calculated by Microsoft Word's word-count feature and 212 words hand-counted in the figures. This total excludes the cover page, signature block, and the parts of the Patent Owner's Response exempted by 37 C.F.R. § 42.24(b)(2).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 10th day of November, 2025, a true and correct copy of the foregoing **Patent Owner's Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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