

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: November 10, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00190
U.S. Patent No. 11,568,941

**DECLARATION OF DR. SUNIL P. KHATRI, PH.D
IN SUPPORT OF PATENT OWNER'S RESPONSE**

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I. Introduction

1. I have been retained on behalf of YMTC (“YMTC” or “Patent Owner”), and its counsel, Latham & Watkins, LLP, to provide expert opinions relating to U.S. Patent 11,568,941 (“’941 Patent”) in connection with Micron Technology, Inc.’s (“Petitioner”) Petition for *inter partes* review regarding the ’941 Patent and the November 26, 2024 Declaration of Dr. David Kuan-Yu Liu (Ex. 1004, “Liu”). The arguments raised in Dr. Liu’s declaration are similar to those raised in the Petition. Unless otherwise noted, my opinions with respect to the Petition also apply to the corresponding section of Dr. Liu’s declaration, and vice-versa. As explained below (discussing the Grounds raised in the Petition), the invalidity arguments raised in the Petition do not show that the prior art in view of the knowledge of a person of ordinary skill in the art (“POSITA”) renders obvious any of the Challenged Claims, and the arguments raised in Dr. Liu’s declaration are insufficient for similar reasons.

2. I have previously rendered my opinion in support of the Patent Owner’s Preliminary Response. While I believe that declaration is accurate, **this new Declaration represents my considered opinion and supersedes my previous Declaration.** Any ambiguities between the two should be resolved in favor of this declaration.

3. Where possible, I have used the exhibit numbers connected to the Petition for Inter Partes Review of the '941 Patent (IPR2025-00190).

4. I am being compensated for my time at my standard hourly rate, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with Patent Owner in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

5. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

6. This declaration, including the exhibits hereto and cited materials, identifies my opinions to date, although I may provide further testimony and opinions if asked to testify in court or at a deposition. I also reserve the right to supplement or amend my opinions, as well as the bases for those opinions, in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '941 Patent. I may rely on demonstrative exhibits, including pictures, figures, and drawings that appear in this declaration and the referenced exhibits and materials. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part.

II. Qualifications

7. My qualifications, including cases in which I was an expert, are stated more fully in my curriculum vitae which has been provided as Exhibit 2007. Here, I provide a brief summary of my qualifications.

8. I have over thirty-five years of experience with electronics, electrical engineering, and computer engineering. A copy of my latest curriculum vitae (CV) is attached hereto as Ex. 2007 and provides further details regarding my background and qualifications.

9. During my career, I have acquired extensive knowledge and experience with VLSI circuits, computer architecture, testing, computer-aided design (CAD) algorithms and algorithm acceleration, logic synthesis, semiconductor memory, redundancy, synchronous and asynchronous circuits, and related software and hardware topics. Relevant to the '941 Patent my technical expertise includes extensive work with semiconductor memory devices such as DRAM, SRAM and flash. My work with semiconductor memory devices has included work on 3D integration and novel ring-based memory architectures, power and speed tradeoffs using selective body bias, architectures and circuit approaches for processing-in-memory, radiation hardening analysis for memories, the use of flash transistors for designing logic circuits (such as ternary Content-addressable Memories (CAMs), Field Programmable Gate Arrays (FPGAs), and

traditional binary-valued as well as ternary-valued digital logic, secure logic circuits, analog circuits like Finite Impulse Response (FIR) filters, Discrete Fourier Transform (DFT) circuits, and in-memory mixed-signal computing architectures like Convolutional Neural Networks (CNNs)), large language models (LLMs) and clocking and source-synchronous design. I recently was awarded a research grant by the Air Force Research Laboratory (AFRL) in Rome, NY, to conduct research in secure digital circuits using flash-based digital design approaches.

10. Another recent research grant from the National Science Foundation (NSF) is funding research on the use of flash transistors for general purpose mixed-signal arithmetic. Additionally, I have led-authored a book chapter on the use of flash transistors in novel Very Large Scale Integrated (VLSI) design applications. My MS thesis involved designing a memory interface for a multi-threaded Reduced Instruction Set Computing (RISC) microprocessor.

11. The following describes some of my relevant experience. I earned my Bachelor of Science in Electrical Engineering in 1987 from the Indian Institute of Technology, Kanpur, India. After graduating with my B.S. degree, I was a candidate for a Master of Science degree in Electrical and Computer Engineering at the University of Texas from 1987–89. At the University of Texas, I held the Microelectronics and Computer Development (MCD) Fellowship from 1987–89.

I also conducted my M.S. research and wrote my thesis on the design of the METRIC memory interface and memory system. METRIC was one of the first super-scalar processors that was developed in the world. I earned an M.S. degree in 1989 from the University of Texas, Austin.

12. After leaving the University of Texas, I worked at Motorola Inc. from 1989–93 as a design engineer for the MC88110 reduced instruction set computing (RISC) microprocessor team. My duties included the design of digital and analog circuitry, test logic and circuits, JTAG boundary scan design, input/output driver design, and clock phase-locked loop (PLL) logic. During my time at Motorola, I was independently responsible for the design of the factory test controller of the MC88110 microprocessor. I performed all attendant tasks in a “vertical” VLSI design methodology, which included high-level modeling, circuit and layout design and verification, as well as global and detailed routing. I also helped in the design of the Translation Lookaside Buffer (TLB) unit, which included a static random-access memory (SRAM) block.

13. In 1999, I earned a Doctor of Philosophy degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley. While at Berkeley, I held the California Microelectronics (MICRO) Fellowship in 1993.

14. I joined the faculty at the University of Colorado, Boulder, in 2000 as an Assistant Professor of Electrical and Computer Engineering. At the University of Colorado my research focused on VLSI logic design automation, VLSI layout design automation, and VLSI design methodologies to address Deep Submicron (DSM) issues such as crosstalk and power.

15. I joined the faculty at Texas A&M University in 2004 as an Assistant Professor in Electrical and Computer Engineering. In 2010 I was promoted to Associate Professor in Electrical and Computer Engineering. In 2015, I was promoted to full Professor in Electrical and Computer Engineering. My research focuses on three primary areas: the first is computer systems, including computer architecture from the circuits up, and algorithm acceleration using GPUs, FPGAs and custom ICs. The second is logic and its applications, while the third area consists of interdisciplinary extensions of the first two. Some specific recent research topics include circuit design using floating gate (flash) devices, wireless power delivery and battery-less electronic systems, machine learning architectures, secure computing approached from both a hardware and software perspective, a formal framework for designing and verifying cryptographic hash functions, and extreme high-speed serial interfaces for Artificial Intelligence / Machine Learning (AI/ML) systems such as those used in Large Language Models (LLMs) like ChatGPT. One of my new focus areas is intelligent and secure computing viewed

from the hardware (circuit) as well as the software levels. I have conducted research on tamper-proof memory techniques, as well as multi-row read architectures for SRAM, DRAM and flash memory arrays.

16. At Texas A&M I teach classes that cover memories extensively, featuring thorough discussion of sense amplifiers, row and column decoders, and different types of memory circuits. For example, in Electrical and Computer Engineering (ECEN) 752 “Advances in VLSI Circuit Design,” a graduate level course, I cover all aspects of VLSI design, including memory design for various types of memories. In this course, (and also in ECEN 449/749 “Microprocessor System Design,”), I cover memories, including flash memories, the design of flash memory cells, the organization of memories into multiple banks, and the division of data across multiple banks of memory, as well as other design techniques that can be used to optimize and manage memories. The ECEN 449/749 course is attended by both undergraduate (ECEN 449) and graduate (ECEN 749) students. In ECEN 454 “Digital Circuit Design,” a senior undergraduate course, I cover circuit design techniques for memory in detail. The Ph.D. thesis dissertation topic for 3 of my current Ph.D. students covers the use of flash memory transistors for analog and digital applications. The Ph.D. thesis of one of my recent doctoral students dealt with the use of flash transistors to design logic circuits. The research of a recent M.S. student entailed a new ring-based source synchronous architecture

for 3D DRAM technologies, which has been published at a conference and in a journal and is being submitted for dissemination as a research monograph. In the past, I have conducted research into new topologies for efficient memory redundancy as part of a course project for my graduate course.

17. Since 2000, I have earned at least 24 research contracts from funders including Intel, the National Science Foundation, the National Security Agency, Altera Corporation, the National Center for Atmospheric Research, National Semiconductor Corporation, and several private sources. The total amount for these research grants is at least \$18.96 million, of which my portion is at least \$3.524 million.

18. I have a total of over 291 peer-reviewed publications. Among these papers, five received a best paper award, while seven others received best paper nominations (including one journal best paper nomination). An additional six journal papers and three conference papers are currently undergoing peer review. I have co-authored nine research monographs, one edited research monograph, and four book chapters. Additionally, I have seven awarded U.S. Patents (two of which were filed during my tenure at Texas A&M), two filed provisional U.S. Patents, and another U.S. Patent which is currently under review and was also submitted during my tenure at Texas A&M. I have co-authored one invited journal paper and 13 invited conference or workshop papers (including one from Design Automation

Conference (DAC) and one from Allerton). Moreover, I was invited to serve as a panelist at a conference eight times and have presented four conference tutorials. I received the “Outstanding Professor Award” in the ECE Department at Texas A&M University in 2007 and also in 2020. In 2009 and in 2019, I received a university-level and a college-level teaching award respectively, at Texas A&M. My H-index is 36 (per Google Scholar). In 2024, I received the “Engineering Teaching Excellence Award” from the College of Engineering, Texas A&M University.

19. Since 2003, I have published numerous research monographs, journal papers, and conference papers on flash transistors and memory systems, as detailed in my CV attached in Appendix A. A few papers on relevant subject areas authored or co-authored by me include:

- “*Flash-based Dynamic Dot Product Acceleration*”, Scott, Khatri. Proc. of the 39th International Conference on VLSI Design (VLSI-D), Pune, India, Jan 3-7, 2006.
- “*A Novel Mixed-Signal Flash-based Finite Impulse Response (FFIR)*”, Lee, Khatri, Ghrayeb. Proc. of the 30th ACM Asia and South Pacific Design Automation Conference (ASPDAC) 2025. Tokyo, Japan, January 20-23, 2025. pp 1216-1222.

- “*Flash - A "Forgotten" Technology in VLSI Design*,” Khatri, Vrudhula, Abusultan, Bharathi, Chu, Lee, Scott, Singh, Wagle. Appears "Frontiers of Quality Electronic Design (QED)". Springer publishers, Sept 2022. Pages 67-136. Ali Iranmanesh, Ed. ISBN: 978-3-031-16344-9;
- “*Flash – An Overlooked Technology in VLSI Design*,” Khatri, Vrudhula. Monday Tutorial to be presented at the ACM/CEDA Design Automation Conference (DAC), San Francisco, CA, June 2024;
- “*A Mixed-Signal Quantized Neural Network Accelerator Using Flash Transistors*,” Scott, Lee, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 71, no. 3, pp. 1025-1038, March 2024;
- “*An ASIC Accelerator for QNN With Variable Precision and Tunable Energy-Efficiency*,” Wagle, Singh, Khatri Vrudhula. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Jan 2024;
- “*A Digital Low Dropout (LDO) Voltage Regulator Using Pseudoflash Transistors*,” Lee, Khatri. IEEE Transactions on Very

Large Scale Integration (VLSI) Systems, vol. 31, no. 12, pp. 1960-1969, Dec. 2023;

- “*A Novel ASIC Design Flow using Weight-tunable Binary Neurons as Standard Cells,*” Wagle, Singh, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I (Regular Papers), 69(7): 2968-2981 (Sept 2022);
- “*CIDAN-XE: Computing in DRAM with Artificial Neurons,*” Singh, Wagle, Khatri, Vrudhula. Frontiers in Electronics, section Integrated Circuits and VLSI. vol. 3, Feb 2022;
- “*An Extremely Low-Voltage Floating Gate Artificial Neuron,*” Scott, Khatri. 2023 IEEE International Conference on Circuits and Systems (ISCAS), May 21-25, 2023. Monterey, CA;
- “*A Novel Pseudo-Flash Based Digital Low Dropout (LDO) Voltage Regulator,*” Lee, Khatri, Vrudhula. 2023 International Symposium on Quality Electronic Design (ISQED), April 5-7 2023. San Francisco, CA;
- “*A Flash-based Digital to Analog Converter for Low Power Applications,*” Scott, Khatri. IEEE 40th International Conference on Computer Design (ICCD), October 2022. Lake Tahoe, CA. pp 1-8;

- “*A Flash-based Current-mode IC to Realize Quantized Neural Networks,*” Scott, Lee, Khatri, Vrudhula. IEEE Design Automation and Test in Europe Conference, Mar 2022, Antwerp, Belgium. pp 1029-1034;
- “*CIDAN: Computing in DRAM with Artificial Neurons,*” Singh, Wagle, Vrudhula, Khatri. 39th IEEE International Conference on Computer Design (ICCD) 2021, pp 349-356, Oct 2021, virtual conference;
- “*A Statistical Methodology for Post-Fabrication Weight Tuning in a Binary Perceptron,*” Azari, Wagle, Khatri, Vrudhula. IEEE 21st International Symposium on Quality Electronic Design (ISQED) 2020. Mar 25-26, 2020, Santa Clara, CA. pp 141-148;
- “*Threshold Logic in a Flash,*” Wagle, Singh, Yang, Khatri, Vrudhula. 37th IEEE International Conference on Computer Design (ICCD), 2019. Abu Dhabi, UAE, pp 550-558. Nov 17-20, 2019;
- “*Fast, Ring-based Design of 3D Stacked DRAM,*” IEEE Transactions on Very Large Scale Integrated Circuits (TVLSI), IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Vol 27 number 8, Aug 2019. pp 1731-1741.;

- *“Fast, Ring-Based Design of 3D Stacked DRAM,”* IEEE International Conference on Computer Design 2017: pp 665-672;
- *“Selective Forward Body Bias for High Speed and Low Power SRAMs,”* Journal of Low Power Electronics, Vol. 5, No. 2, Aug. 2009, pp. 185-95;
- *“Low Power and High Performance SRAM Design using Bank-based Selective Forward Body Bias,”* IEEE/ACM Great Lakes Symposium on VLSI, May 10-12, 2009, Boston, MA, pp. 441-44;
- *“Modeling Dynamic Stability of SRAMs in the Presence of Single Event Upsets (SEUs),”* IEEE International Symposium on Circuits and Systems, May 18-21, 2008, Seattle, WA, pp. 1788-91;
- *“Design of a Flash-based Circuit for Multi-valued Logic,”* Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI) 2017, pp 41-46, May 10-12, 2017. Banff, Canada.
- *“SAT-Based Optimization for Flash-Based Digital Designs,”* IEEE/ACM Design Automation Conference (DAC), Jun 18-22, 2017, Austin, TX.
- *“A Flash-based Digital Circuit Design Flow,”* IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2016, Austin, TX, Nov 2016.

- *“Implementing low power digital circuits using flash devices,”* 2016 IEEE 34th International Conference on Computer Design (ICCD), pp 109-116, Oct 3-5, 2016, Phoenix, AZ.
- *“Exploring Flash Devices to Implement Digital Circuits,”* IEEE/ACM Design Automation Conference (DAC), June 2016, Austin, TX.
- *“FTCAM: An Area-efficient Flash-based Ternary CAM Design,”* IEEE Transactions on Computers, Vol. 65, No. 8, Aug. 2016, pp. 2652-58;
- *“An Area-efficient Ternary CAM Design Using Floating Gate Transistors,”* IEEE International Conference on Computer Design, Oct. 19-22, 2014, Seoul, S. Kor., pp. 55-60; and
- *“A Fast Ternary CAM Design for IP Networking Applications, International Conference on Computer Communications and Networks,”* October 22, 2003, Dallas, TX, pp. 434-39 (awarded best paper).

20. In addition to my work on the papers listed above, I have also served as an editor for IEEE Transactions on Computers, ACM Transactions on Design Automation of Electronic Systems, and MDPI Journal of Electronics.

21. I have served as EDA Track Co-Chair for ICECS 2014, Panel Chair for TexasWISE 2014, Track Co-Chair (VLSI Systems, Applications and Computer Aided Design track) for ICECS 2013, Poster Session Chair for TexasWISE 2013, Advisory Committee for HotPI 2013, Panel Session Chair for SLiP 2013, Track Chair (Logic track) for ICCAD 2009-10, 2015-17, Track Chair (logic track) for DAC 2016-17, General Chair for IWLS 2009, Technical Program Chair for IWLS 2008, Track Co-Chair, Computer Aided Network Design (CANDE) Track, for ISCAS 2008-10, Track Co-Chair, Test and Methodologies Track, for ICCD 2007, Panel Chair for ITSW 2009, Publicity Co-Chair for GLS-VLSI 2009, and as a member of the TPC for several conferences.

III. Understanding of Legal Standards

22. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

A. *Interpreting Claims in an Inter Partes Review Proceeding (Claim Construction)*

23. I understand that an Inter Partes Review is a proceeding before the United States Patent & Trademark Office (“USPTO”) for evaluating the validity of one or more claims of an issued patent.

24. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary.

25. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the USPTO. I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. *Invalidity*

26. I understand that a patent claim is unpatentable if it is obvious in view of the prior art. I further understand that a claim is unpatentable if it is obvious from the perspective of a person of ordinary skill in the relevant art (“POSITA”), at the time the invention was made.

27. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

28. I have been informed by Counsel that in order for a claim to be unpatentable for lack of novelty, i.e., anticipated, a single prior art reference must disclose each and every claim limitation of that patent claim. It is not considered in a vacuum, rather, one must take into account what a person having ordinary skill in the art (POSITA) would have understood from the reference. I also understand that one should consider not only what is expressly disclosed in the prior art reference, but also what would naturally, inherently have been understood by a POSITA from what is disclosed in the prior art reference. I understand that to prove inherency, the matter that is not expressly described must be necessarily present in the reference, and it would be so recognized by a POSITA.

29. I have been informed by Counsel that determining anticipation of a patent claim requires a comparison of the properly construed claim language to the prior art on an element-by-element basis. As it pertains to an IPR proceeding, a claim is “anticipated” if each and every element of the claim, as properly construed, has been disclosed in a single prior art reference, either expressly or inherently, and the claimed arrangement or combination of those elements must also be disclosed, either expressly or inherently, in that same prior art reference.

30. I also understand that to be considered prior art, a reference must be enabling, meaning it provides sufficient detail for a POSITA to make and use the invention without undue experimentation. I further understand that a reference that is not enabling is not anticipating. That is, in order to anticipate a claimed invention, a prior art reference must enable a POSITA to make the invention without undue experimentation.

31. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their

arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight-driven combination of components selectively culled from the prior art.

32. It is my understanding that a claimed invention is unpatentable as obvious if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

33. I have been informed by Counsel that a POSITA is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a POSITA at the time the invention was made, and not simply to provide his/her own personal conclusions.

34. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date). In considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution leads to improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, a conclusory assertion that a POSITA could combine the references, rather than a showing why they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

35. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been

informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

36. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a POSITA would be motivated to make a combination includes whether he/she would select particular references in order to combine their elements.

37. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a POSITA would have had a motivation to combine the potential prior art references.

38. I have also been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be

considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness.

IV. Summary Of Materials Reviewed And Considered

39. I have been asked to provide analysis and explain the subject matter of the '941 Patent, including the state of the art when the application underlying the '941 Patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '941 Patent including how that art relates to certain claims of the '941 Patent and to provide my opinions regarding whether that art invalidates those claims.

40. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor circuit design, I reviewed the Petition and all relevant exhibits attached thereto, and all exhibits cited herein.

41. My opinions are guided by my appreciation of how a person of ordinary skill in the art (defined in Section V) would have understood the claims of the '941 patent at the time of the invention, which I have been asked to assume is February 10, 2020.

V. Level of Ordinary Skill in the Art

42. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

43. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a POSITA is also a person of ordinary creativity. I have considered these factors to determine the relevant level of skill in the art.

44. Under this definition of a POSITA, the Petition does not show the challenged claims anticipated or obvious. In forming my opinion, I have drawn on my academic background and professional experiences.

45. Dr. Liu defines a POSITA as a person having “a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices (including issues relating to the operation, e.g., programming, of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Ex. 1004 ¶40. Dr. Liu further states that “this POSITA would have been aware of and generally knowledgeable about NAND flash memory’s structure and fabrication, its component parts, how it operates, and how it is controlled.” *Id.* ¶41.

46. I am informed by counsel that Patent Owner does not dispute Petitioner’s definition of a POSITA for the purposes of these proceedings.

47. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile NAND flash memory and 3D NAND—I was at least a person of the ordinary level of skill in the art as of February 10, 2020 under Dr. Liu’s interpretation of the level of a POSITA (the ’941 Patent claims priority to a Patent Cooperation Treaty (PCT) application filed on Feb. 10, 2020). In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein were formed taking into account the perspective of an ordinarily skilled artisan.

VI. Background

A. *Technical Background*

48. Volatile memory technologies, such as static random access memory (“SRAM”) and dynamic random access memory (“DRAM”), lose their contents when power is turned off. However, persistent (non-volatile) memory is needed for many applications, such as storage for photos in a digital camera, bootable code or settings in desktops, laptops or cellular phones, and a wide range of other applications. Non-volatile memories (e.g., thumb drives, hard drives, and compact discs) can store information even after the system is powered off. Traditionally, media such as hard disks, floppy disks, compact discs, or magnetic tapes was used for non-volatile storage in computing systems, but these media are large, bulky, and slow, and use a large amount of power.

49. Flash memory is a specific type of non-volatile memory, in which data is stored in transistors that have an uncontacted (floating gate), in which the presence or absence of trapped charge results in stored data. This floating gate can be a conductor (the corresponding flash transistor is called a floating gate or FG transistor), or an insulator with sites which trap charge (the corresponding flash transistor is called a charge trap transistor or CTT). Ex. 1009 at 355, 401. NAND flash memory consists of flash transistors arranged in series (in a “string”), which yields a NAND circuit. Ex. 1009, 18, Fig. 2.2.

50. Each flash transistor is a 4-terminal device, as shown in the diagram below. Ex. 2020, 81, Fig. 31. What is shown below is the symbolic representation of the flash transistor used to draw circuit schematics (on the right), and its physical structure (on the left). Although the floating gate forms a fifth terminal, it is floating (uncontacted), and therefore I do not count it as a terminal.

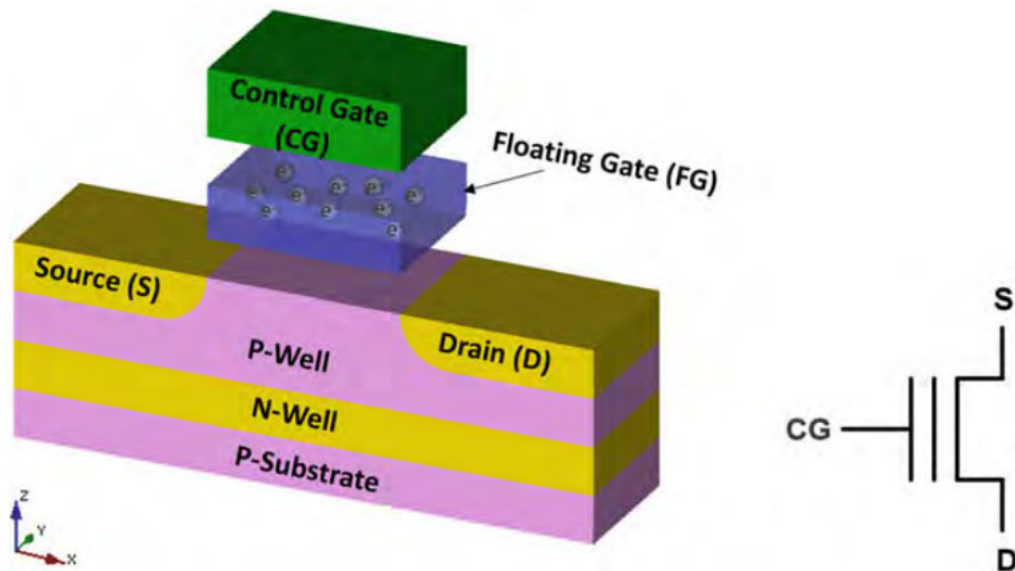


Fig. 3.1 Floating gate memory cell and its schematic symbol

Ex. 2020, 81, Fig. 31.

51. I will next describe these terminals, in no particular order. The first terminal is the control gate terminal CG. If the voltage of this gate terminal is greater than a “threshold voltage” V_T of the flash transistor, the flash transistor is conducting, otherwise the flash transistor is non-conducting.

52. Conducting means that the resistance between the source and drain (the two remaining terminals) is relatively low. Non-conducting means that the

resistance between the source and drain is relatively high. A short circuit (such as a wire, or a light bulb switch that is closed so that the light bulb is turned “on” and there is current flowing through it) is an example of a low resistance. An open circuit (such as a wire that is cut into two, or a light bulb switch that is open and the light bulb is turned off, since there is no current flowing through it) is an example of a high resistance.

53. The last terminal is the substrate (also called the body or bulk), which is shown in the image on the left. It is the layer upon which all the other features of the flash transistor are fabricated.

54. In a flash transistor, charge is stored on the floating gate, which is an isolated conductor. The floating gate cannot discharge, since it is in a high-impedance state. The charge on the floating gate controls the current flowing between the source and drain of the flash transistor, by altering the threshold voltage of the flash transistor. This current allows the user to determine the value stored in the cell. The charge stored in the floating gate is a proxy for the logical value stored in the flash memory cell that is implemented using the flash transistor.

55. I will now discuss the program and erase operations using Figure 2.10 of Aritome (Ex. 1009), excerpted below.

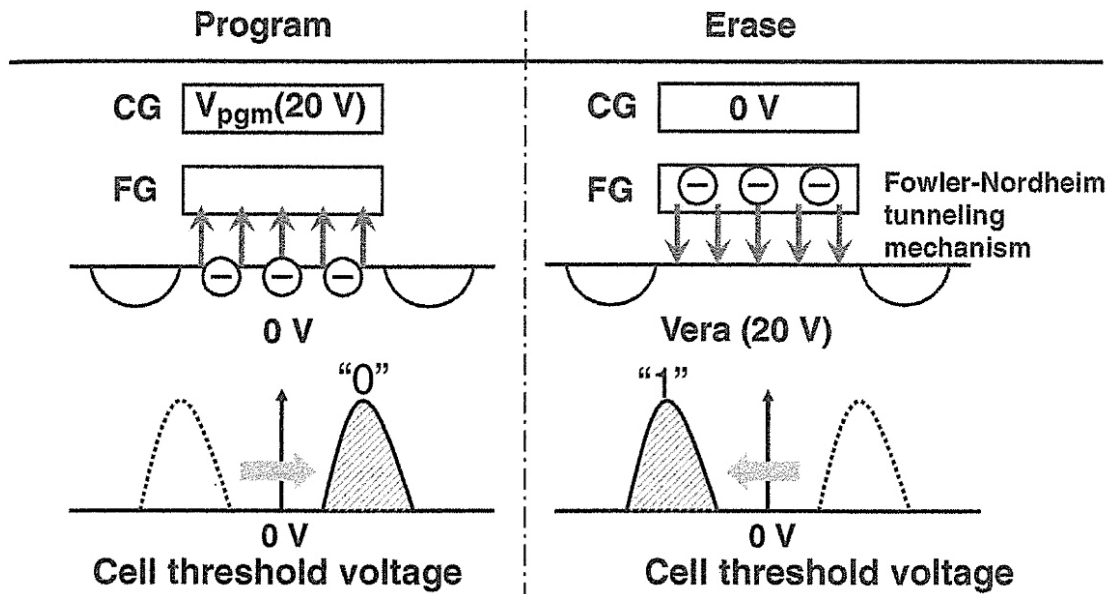


FIGURE 2.10 Principle of single-cell program and erase. Program: Injected electron to the FG through tunnel oxide. Erase: Ejected electron from the FG.

Ex. 1009, 44, Fig. 2.10.

56. To erase the cell, a large voltage is applied to the substrate while keeping the CG (control gate) to 0 V , as shown on the right side of Figure 2.10 of Aritome (Ex. 1009). This causes the trapped charge in the floating gate FG to be removed, and results in a negative threshold voltage. The charge is dissipated through a mechanism called Fowler-Nordheim tunneling (FN tunneling). Ex. 1009, 44-45.

57. To program a cell, a high voltage is applied to the CG, while keeping the substrate/source/drain to 0 V as shown in the left of Figure 2.10 above. Ex. 1009, 44. As a result, electrons are injected into the FG by FN tunneling, resulting

in an increase in the threshold voltage of the floating gate transistor. Ex. 1009, 44-45.

58. Floating gate transistors individually have limited endurance. Depending on the type of transistor and how it is configured, an individual transistor may not work reliably after it has been programmed and erased too many times. For example, the endurance for some flash transistors is on the order of up to 100,000 program-erase cycles. *See, e.g.*, Ex. 1009, 217-222.

59. In a NAND flash memory, several floating gate transistors are connected in a series configuration, as shown in the figure below (from Ex. 1009, 18). The source end of the string is depicted at one end of the figure. The drain end of the string is depicted at the other end of the figure, and is connected to a bitline BL. Two fixed-threshold transistors connect the string of floating gate transistors to the source terminal (the gate of this transistor is driven by a signal SGS) or the bitline BL (the gate of this transistor is driven by a signal SGD). The gate terminals of the floating gate transistors are driven by signals that are called word lines (WL), such as WL0, WL1, ... WL31.

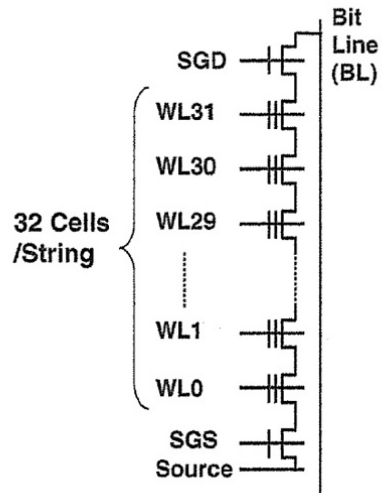


FIGURE 2.2 NAND cell string architecture. NAND cell string consists of 32 cells (for example) and two select transistors (SGD, SGS). Thirty-two cells are connected in series. SGD and SGS connect at drain and source to isolate from bit line and source line, respectively.

Ex. 1009, 18, Fig. 2.2.

60. In NAND flash memory, FN tunneling is typically used to perform both programming and erase. For programming, there is another mechanism called Hot Carrier Injection (HCI) or Channel Hot Electron (CHE) injection. In this scheme, a high voltage is applied across the source and the drain, and a positive gate voltage is applied to the control gate of the flash transistor. High-energy electrons are generated due to the strong drain-to-source electric field, and are attracted to and trapped in the floating gate, resulting in an increase in V_T (i.e. cell programming). The hot carriers are generated by a mechanism called gate-induced drain leakage (GIDL). *See* Ex. 1009 (Aritome), 42-44, 99-100.

61. Although HCI is not typically used to program floating gate transistors in NAND flash memory, it is one of the mechanisms that can cause program disturb in NAND flash memory. *See* Ex. 1009 (Aritome), 42, 99-100.

62. NAND flash arrays comprise strings of flash transistors which are controlled by wordlines, and during a program operation the controller applies a program voltage (V_{PGM}) to the selected wordline and pass/isolation voltages to unselected wordline (i.e., a “**program phase**”).¹ *See, e.g.*, Ex. 1005 (“Dong”), Fig. 5a. In the inhibit string, all transistors should not be programmed, and in the selected string, only the transistor connected to the selected wordline (the selected memory cell) should be programmed.

63. Program disturb occurs when an unselected memory cell is unintentionally programmed (i.e. its threshold voltage is increased) during a program operation of the selected memory cell. Ex. 1009, 52 (“Program disturb is a phenomenon in which the threshold voltage (V_t) of unselected cell is increased during program operation.”).

64. Read disturb, on the other hand, occurs during verify/read activity when a sensing/read voltage is applied to confirm the result of programming (i.e., a “**verify phase**”). *See, e.g.*, Ex. 1012 (“Costa”), Fig. 9A; Ex. 1010, 280 (“Read

¹ In this declaration, I use “wordline” interchangeably with “word line.”

disturb is a phenomenon in NAND flash memory where reading data from a flash cell can cause the threshold voltages of other (unread) cells in the same block to shift to a higher value.”); Ex. 2020 (Micheloni 3D Flash), 50-51 (identifying memory cells subject to read disturb when a read voltage V_{read} is applied to a selected cell).

1. *Two-Dimensional (2D) or Planar NAND*

65. A POSITA would understand that in 2D or Planar NAND, wordlines, and select gates (i.e., source and drain) are arranged horizontally on the substrate, as seen below. That is, the word lines, source terminals, and drain terminals are all physically located on the same horizontal plane above the substrate. Figure 2.3 below from Petitioner’s Exhibit 1009, for example, shows (a) a top view and (b) a cross-sectional view of an exemplary 2D NAND flash memory.

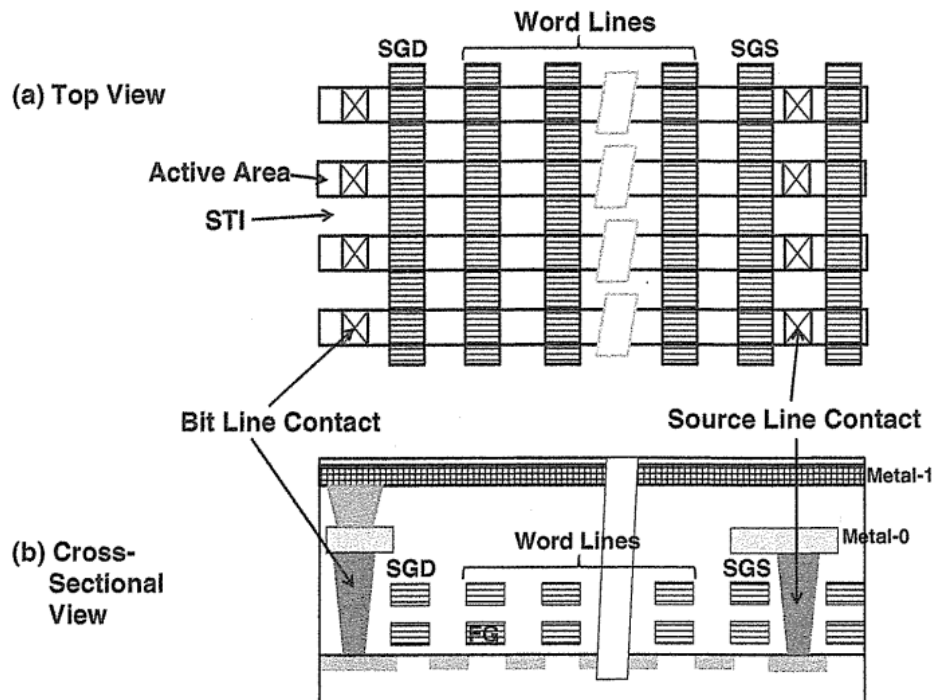


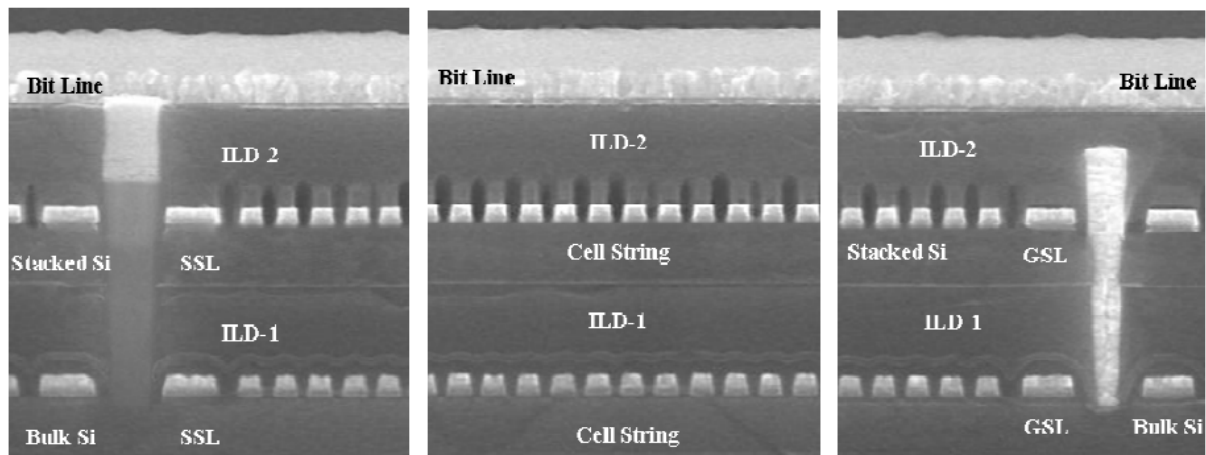
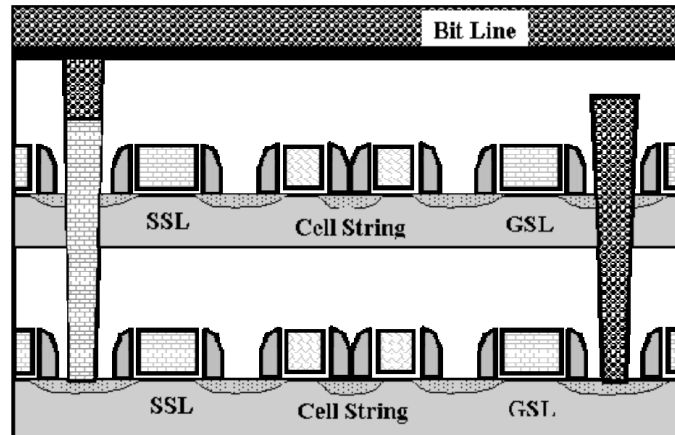
FIGURE 2.3 (a) Top schematic view and (b) cross-sectional view of NAND flash memory cells.

Ex. 1009 pt. 1 at 40. This memory array includes 32 word lines arranged between two select transistors, the source-side transistor (“SGS” or Select Gate Source) and the drain-side transistor (“SGD” or Select Gate Drain)—each arranged on the same horizontal plane above the substrate. *Id.* at 38, 40. However, the scaling of 2D NAND flash memory faced many limitations, including capacitive coupling interference, lithographic variations and patterning problems, reduced number of electrons, dopant fluctuations, and inadvertent programming of memory cells near the cell being programmed (inadvertent programming of memory cells other than the cell being programmed, i.e., “program disturb”)—thus resulting in “major scaling limitations.” *Id.* at 150.

2. *Three-Dimensional (3D) NAND At The Time Of Dong's Filing Date Included Stacked 2D NAND*

66. To further scale NAND flash memory, a POSITA would understand that some initial 3D NAND designs were available at the time of Dong's filing date, May 7, 2007. *See* Ex. 1005 at 1. For example, as I describe below, Stacked NAND and Multi-layer Thin-Film Transistor ("Multi-layer TFT") designs "stacked" horizontally arranged NAND memories on top of each other, creating a three-dimensional memory array which did not have vertically arranged word lines.

67. A POSITA would have understood that Stacked NAND, shown below, uses that same structure as the traditional 2D NAND, with the source side select transistor ("GSL" or ground select line, near the source), drain side select transistor ("SSL" or string select line, near the drain), and word lines ("Cell String") arranged horizontally. Rather than having one level, however, Stacked NAND, shown below in Figure 7.2, uses several layers of 2D horizontally arranged NAND strings stacked on top of one another, with each layer of NAND strings arranged in a 2D horizontal manner.



Ex. 2008 (Jung) at 3, Figs. 3, 4 (showing the structure of a three dimensional Stacked NAND string, along with a scanning electron microscope (SEM) photograph of the fabricated three dimensional Stacked NAND string).

68. As seen above, the word lines within each layer are still arranged on a horizontal plane above a substrate between the source and drain, not vertically. *Id.* at 3 (“In the doubly stacked NAND Flash cell strings of Fig. 3, the cell strings of the upper layers are stacked over the bottom layer ones already formed on the bulk Si Substrate.”).

69. In my opinion, a POSITA would understand that Multi-layer TFT 3D NAND is similar to the Stacked NAND design, but for the use of a special type of transistor in the NAND cells (a TFT transistor). For example, the below Multi-layer TFT 3D NAND shows two two-dimensional NAND layers (“bottom” and “top” layers) with word lines (“Poly gate[s]”) arranged horizontally on a substrate.

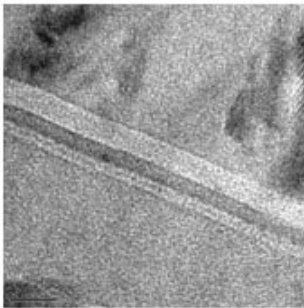


Fig. 1 TEM of the O1/N1/O2/N2/O3 structure for TFT BE-SONOS.

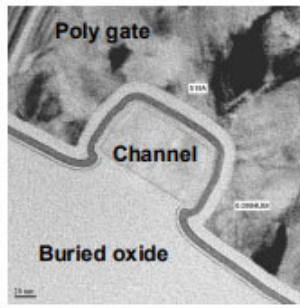


Fig. 2 Tri-gate structure of the TFT device.

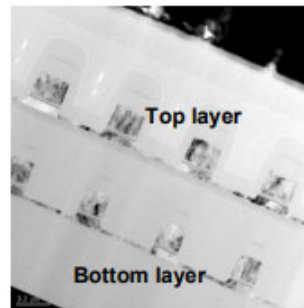


Fig. 3 Channel-length direction of double-layer TFT NAND devices.

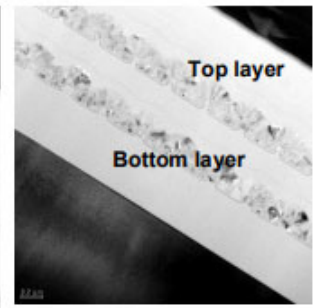


Fig. 4 Channel-width direction of double-layer TFT NAND devices.

Ex. 2009 (Lai 2006) at 4. In other words, like the Stacked NAND design, the word lines in the Multi-layer TFT design are still arranged horizontally, not vertically.

70. The 2D NAND-based Stacked and Multi-layer NAND designs are not the same as vertical 3D NAND as recited in the '941 Patent because the cells are not arranged vertically “from bottom to top.” Moreover, “[t]he program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed.” Ex. 1009, 354. In fact, as a POSITA would understand, since the Stacked NAND and the Multi-layer NAND designs above use multiple layers of 2D NAND structures, their

program disturb mechanisms would resemble the program disturb mechanism of traditional 2D NAND flash memories.

3. *Program Disturb Differences Between 2D and 3D NAND*

71. I will now discuss the differences between 2D and 3D NAND flash memories, and how they result in different program disturb mechanisms and behaviors across these two kind of flash memories.

72. The program disturb conditions and characteristics of 3D cells are greatly changed from that of 2D cells.” Ex. 1009 (Aritome), 372 (“The 3D NAND flash cell has a concern to have the larger fluctuation in cell current than the 2D NAND flash cell, because the 3D cell has a different process and structure, such as a poly-Si channel, charge trap cell (thinner tunnel oxide), and tunnel oxide by deposition process.”), 354 (“The program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed.”), 354-55 (“WL capacitance is much increased in the stacked word-line (WL) structure in the 3D NAND cell ... because a plane structure of WL has a large parasitic capacitance. However, WL resistance is decreased due to wide WL width.”), 355 (“The cell current is much decreased in the 3D NAND cell, because channel material is changed from crystal Si (substrate Si) to poly-Si.”). These electrical and manufacturing differences between 2D and 3D NAND result in vastly different program and program disturb effects.

73. The differences between 2D and 3D NAND flash program disturb arise due to differences in circuit structure and topology, and also due to electrical properties of the channel which arise from manufacturing differences. *See, e.g.*, Ex. 1009 (Aritome), 354 (“The program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed.”).

74. First, there are key differences between 2D and 3D NAND flash in terms of circuit structure. The 2D NAND flash structure is shown below, along with its disturb model. In 2D NAND flash, multiple strings are placed side by side on the chip substrate. The first kind of program disturb can occur in the flash transistors in the select string, which do not have the program voltage V_{pgm} applied on their control gate (and have V_{pass} applied on their control gates instead). Program disturb can occur in the flash transistor in the inhibit string (a string not selected for programming, such as the one on the right of the figure below) for the transistor that has the program voltage V_{pgm} applied on its control gate, as well as for transistors which do not have the program voltage V_{pgm} applied on their control gate (and have V_{pass} applied on their control gates instead). Ex. 1009 (Aritome), 53.

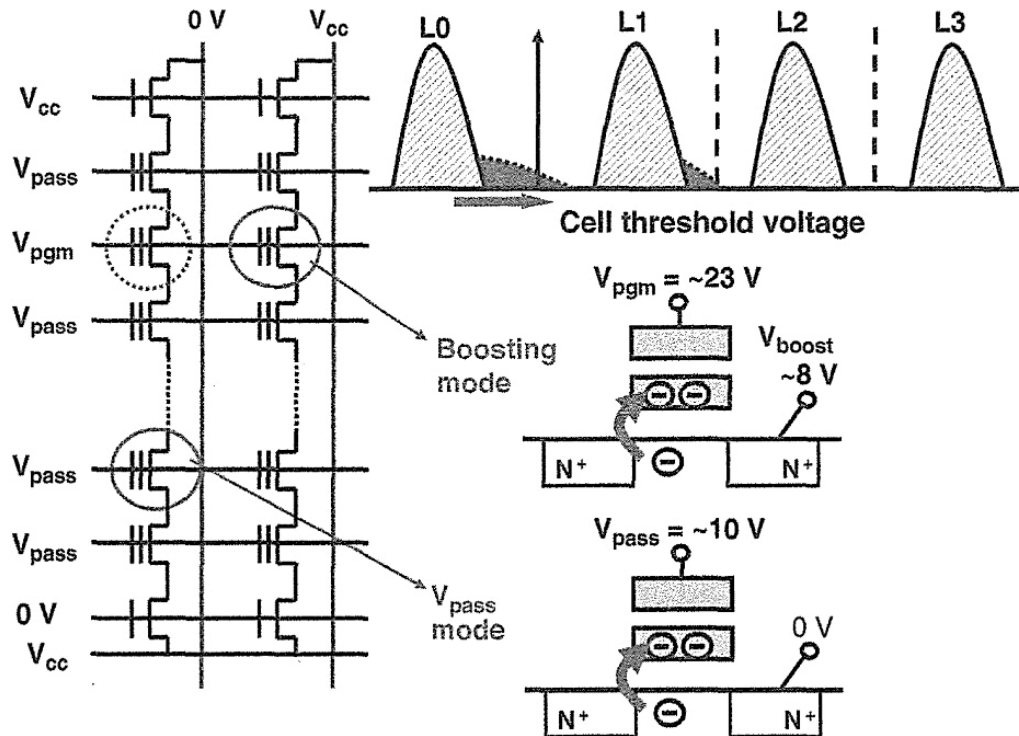


FIGURE 2.21 Program disturb of NAND flash memory cells. Weak electron injection mode is caused in an unselected cell. There are two modes of boosting mode and V_{pass} mode. The “self-boosting” scheme is used for unselected string. The channel voltage in unselected string has boosted up to $V_{boost} \sim 8 \text{ V}$.

Ex. 1009, 53, Fig. 2.21.

75. The vertical 3D structure is shown below, along with its new disturb models. See Ex. 1009 pt. 2, 363.

76. Because of this structure of vertical 3D NAND flash memory, new modes of program disturb arise. In 3D NAND, multiple planes of multiple strings are placed side by side on the chip substrate. In the figure below, some strings are arranged from left to right (in the X direction). The multiple planes of such multiple strings are arranged in a front-to-back orientation (in the Y direction). Note that the bitlines in the figure below run in the Y direction, and the bitlines connect a

single plane of multiple strings at any given time. This is achieved by driving exactly one DSL_i signal HIGH at any given time. For example, if DLS₅ was driven HIGH, then the 5th plane of strings would be connected to the bitlines for memory operations.

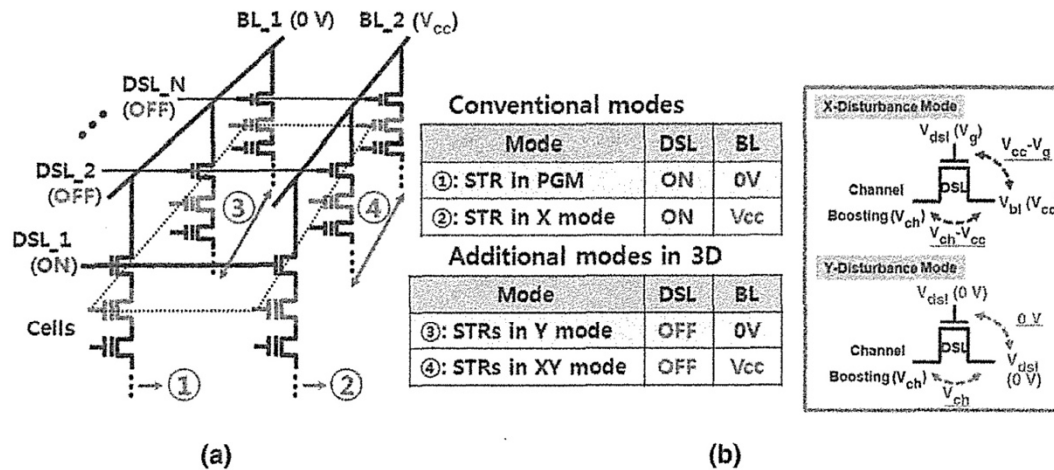


FIGURE 8.11 (a) Program disturbance modes of 3D NAND flash cell array. *N* strings are connected to the same bit line in the same block. (b) Comparison of program disturbance modes in a 3D NAND flash cell array. In a 3D NAND cell, two new modes of Y-mode and XY-mode are added.

77. I will first describe the program disturb modes that are similar to those of 2D NAND flash. The first program disturb (labeled as “STR in PGM” in the figure above) can occur in flash transistors in the selected string (a string selected for programming, such as string 1), for flash transistors that have a pass voltage V_{pass} applied on their control gates. The second program disturb (labeled as “STR in X mode” in the figure above) can occur in flash transistors in the unselected string (a string not selected for programming, such as string 2), for flash transistors

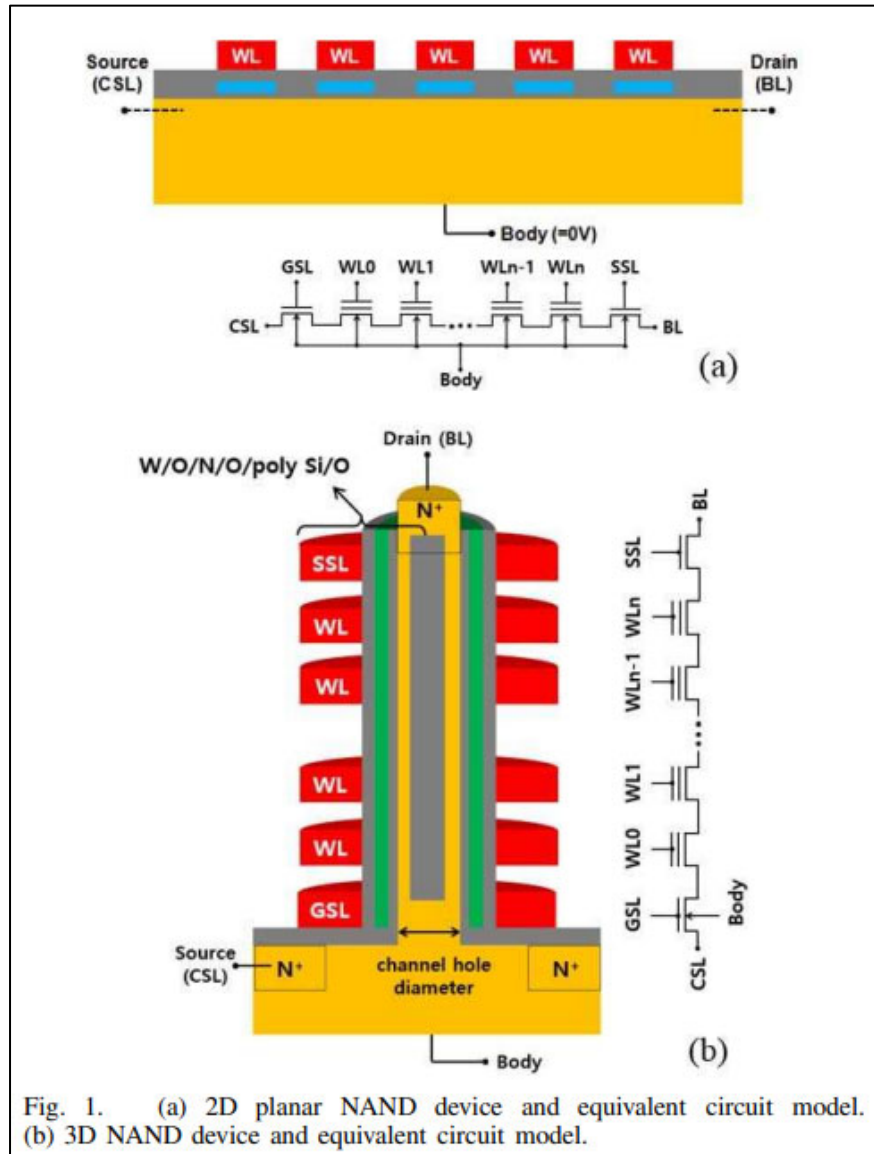
that have a pass voltage V_{pass} applied on their control gates, or also for the flash transistor that has a program voltage V_{pgm} applied to its control gate.

78. In 3D NAND flash, new program disturb modes are induced as a result of new memory architecture. A first new disturb mode (Y mode) occurs in strings which share the bitline but not the DSL line with the select string (string 3 in the figure above, labeled “STRs in Y mode”, as an example). For such strings, program disturb occurs for flash transistors that have a pass voltage V_{pass} applied on their control gates, or also for the flash transistor that has a program voltage V_{pgm} applied to its control gate. A second new disturb mode (XY mode) occurs in strings which do not share the bitline or the DSL line with the select string (string 4 in the figure above, labeled “STRs in XY mode”, as an example). For such strings, program disturb occurs for flash transistors that have a pass voltage V_{pass} applied on their control gates, or also for the flash transistor that has a program voltage V_{pgm} applied to its control gate. As a result, a POSITA would understand that the program disturb mechanisms for 2D NAND are not directly applicable to 3D NAND.

79. As illustrated in Figure 1(a) of Ex. 2025 reproduced below, the 2D NAND string has a low resistance channel below every flash transistor in the string. Ex. 2025, 1 (recognizing that for 2D NAND that “the body is connected to every cell transistor”). This is shown below, both in a cross sectional view of the

2D planar NAND string, and its equivalent circuit below the cross sectional view.

I note that the equivalent circuit figure shows the substrate (body) node of each flash transistor connected to the terminal labeled “Body.”

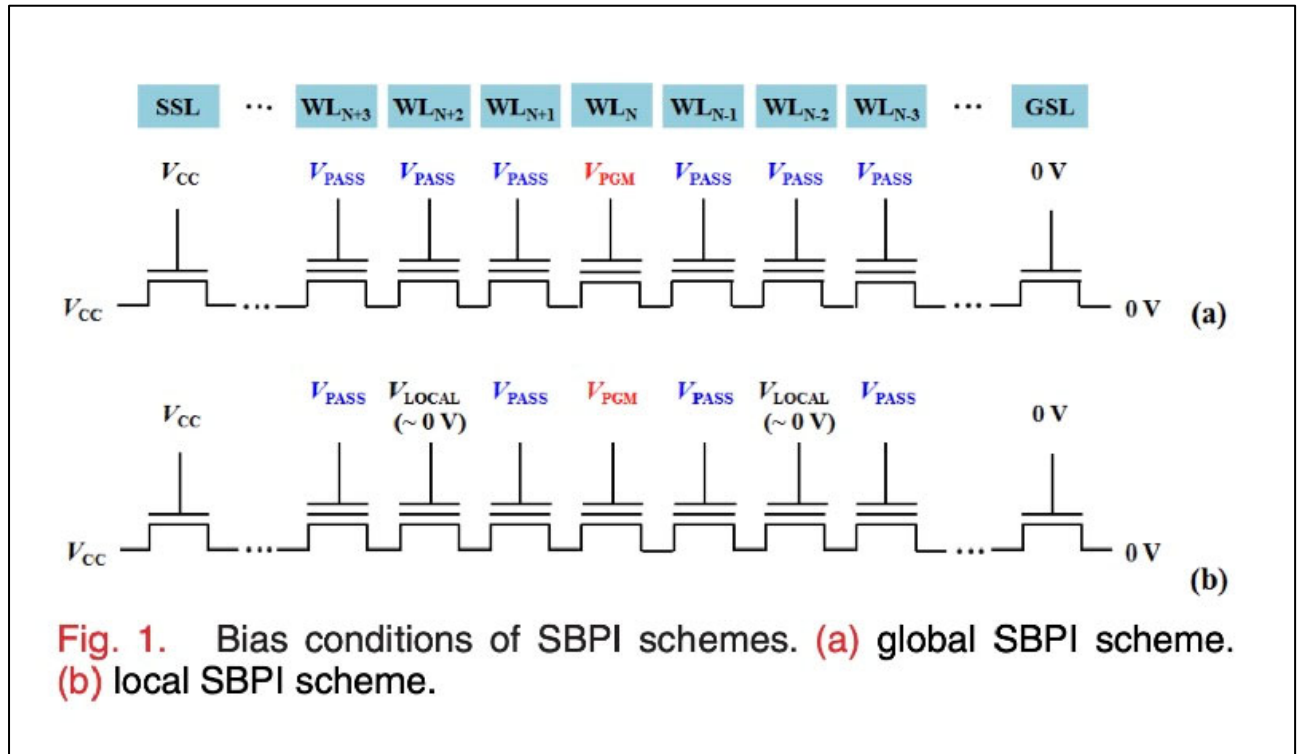


Ex. 2025, 1, Fig. 1.

80. In the 3D NAND string, shown above in Figure 1(b), the “body ... is connected only on the side with the ground select line (GSL)” and the “main cells based on the ultra-thin body (UTB) structure are not connected to the body.” Ex. 2025, 1. This is illustrated above, where the cross sectional view shows the UTB, and the equivalent circuit shows flash transistors whose body terminal is floating and not connected together (in contrast to the 2D NAND string). This results in significant electrical differences because “the channel can be in the floating state in certain circumstances.” *Id.* This floating channel is highly capacitive and resistive.

81. This electrical difference between 2D and 3D NAND results in a phenomenon called Natural Local Self-Boost (NLSB) in 3D NAND (which is not present in 2D NAND). This is described in Ex. 2024, which confirms that in 3D NAND flash memory, the “ultra-thin-body (UTB) structure ... is not connected to the substrate ... and can be in the floating state.” Ex. 2024, 1. During programming, “the inhibited channel becomes a floating node and the natural local self-boosting (NLSB) effect occurs.” *Id.* This NLSB effect allows the inhibited string to be sufficiently boosted, even with the “global self-boosted program-inhibit (SBPI) scheme” where V_{pass} is applied to unselected or inhibited wordlines (shown in the Figure 1(a) below). The simulations conducted in this reference show

that NLSB results in a boost to 11.7V (compared to the 2D NAND flash global SBPI scheme resulting in a boost of only 4.6V). Ex. 2024, 2.



Ex. 2024, 1, Fig. 1.

82. In contrast to the NLSB that occurs in 3D NAND flash, 2D NAND techniques rely on traditional boost schemes such as global self boost, local self-boost, and erase area self-boost (EASB). Ex. 1009, at 54. In EASB, the erase area is boosted, because “[b]oosting efficiency of drain side cells is higher than source-side due to lower cell V_t .” *Id.*, 53. The source side cells are already programmed, due to the “page program order” that is employed, and hence their V_t ’s are higher than the V_t ’s of the drain-side cells. *Id.*, 52-54. For example, in a local self-boosting scheme in 2D NAND, isolation voltages of little to no voltage are applied

to unselected wordlines adjacent to the selected wordline that receives V_{pgm} . *Id.*, 54, Fig. 2.23(b). In an EASB scheme applied in 2D NAND, isolation voltage of little to no voltage is applied to an unselected wordline on the source-side of the selected wordline that receives V_{pgm} . *Id.*, 54, Fig. 2.23(c).

83. It is important to understand that “[t]he NLSB effect does not require the local boosting scheme used in conventional 2D NAND, because it can achieve a sufficiently high potential even if the number of stacks is increased.” Ex. 2027, 1. As a result, the local boosting schemes used for 2D NAND flash are not applicable in 3D NAND flash.

B. *The '941 Patent (Ex. 1001)*

84. The '941 Patent was filed on Sept. 10, 2021 and I am informed that it claims priority to a Patent Cooperation Treaty (PCT) application filed on Feb. 10, 2020. The '941 Patent describes and claims “a solution for reducing program disturbance and pass voltage disturbance when operating a three-dimensional memory.” Ex. 1001 at 1:39-41, 1:19-22. Specifically, as “the number of layers is increased” for three-dimensional NAND, pass voltage disturbance occurs and program disturbance “become[s] more significant,” resulting in “a higher failure rate of programming.” *Id.* at 1:34-38. As the '941 Patent recognizes, these issues were particularly problematic in three-dimensional NAND memory with a plurality of layers wherein memory cells or word lines are in close proximity. Ex.

1001 at 1:30-41. By carefully choosing voltages to specific wordlines of the 3D NAND memory while programming the selected wordline, the '941 Patent reduces program disturbance and pass voltage disturbance on unselected memory cells. *Id.* at 6:39-43. The '941 Patent describes this solution in the specification, including with reference to the Figure 8 embodiment.

85. For example, Figure 8 illustrates a 3D memory including a “first portion 710” (blue) including word lines “WL(m+1)” to “WLn” arranged “from bottom to top.” Ex. 1001 at 4:29-34. The 3D memory also has a “second portion 720” (orange), which is “formed below the first portion 710,” and includes word lines “WL(k+1)” to “WLm” arranged “from bottom to top.” *Id.* at 4:34-36; *see also id.* at 6:55-60 (claim 1), 7:23-28 (claim 5), 8:15-20 (claim 11).

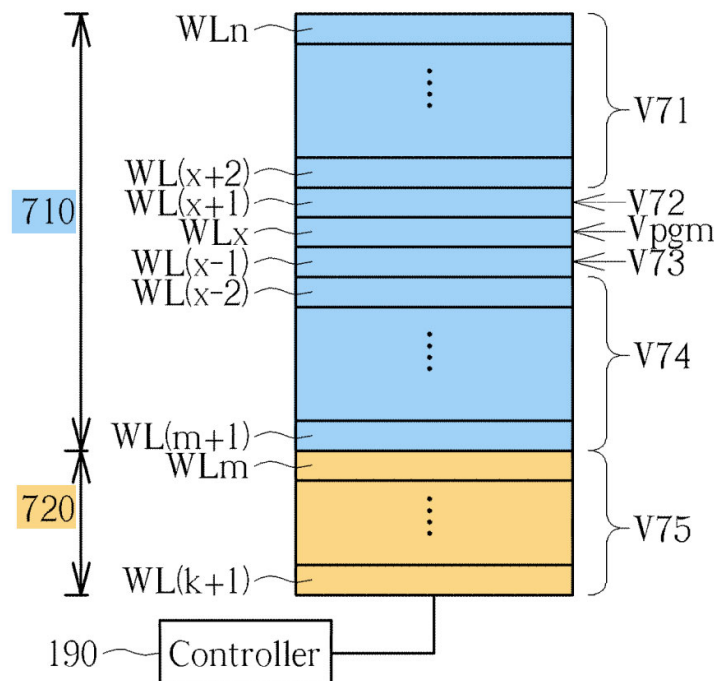


FIG. 8

Id. at Fig. 8. In my opinion, based on the intrinsic evidence, as well as my knowledge and experience, a POSITA would also understand that the three-dimensional memory of the '941 Patent has a substrate located below and perpendicular to the vertical arrangement of word lines, i.e., a “three dimensional stack NAND flash memory.” Ex. 1001 at 1:26-29, 6:39-47; Ex. 1010, 140-141 (supporting it was well known that the “Si substrate [is] under the memory array”).

86. During programming of the xth wordline (i.e., “WLx”), controller 190 applies V_{PGM} to WLx and other voltages V71, V72, V73, V74, and V75 to unselected wordlines to reduce the effect of program and pass voltage disturbances. Ex. 1001, 1:30-41, 3:9-11, 4:37-61, 6:39-43, Fig. 8. When the xth word line (i.e., “WLx”) is programmed, the controller 190 applies a program voltage “Vpm” to WLx. *Id.* at 3:9-11. At the same time, the controller 190 applies a first voltage V71 to word lines “WL(x+2)” to “WLn,” a second voltage V72 to word line “WL(x+1),” a third voltage V73 to word line “WL(x-1),” a fourth voltage V74 to word lines “WL(m+1)” to “WL(x-2),” and a fifth voltage V75 to word lines “WL(k+1)” to “WLm”). *Id.* at 4:37-42, 4:51-59. The '941 Patent also discloses that the fifth voltage V75 can be lower than the fourth voltage V74. *Id.* at 4:60-61.

C. Prosecution History

87. The '941 patent is a divisional of U.S. Pat. 11,195,590 (the “'590 patent”). Ex. 1001, Cover. I have also reviewed the file history for both the '941

and the '590 Patents, each of which had claims that received a first-action allowance (i.e., certain claims of these patent applications were approved without any rejection or office actions from the USPTO examiner). *See* Ex. 1002 ('941 Patent), 378-382; Ex. 1003 ('590 Patent), 388-389, 417, and 424-425. The Examiner allowed the '941 Patent stating that “there is no teaching, suggestion or motivation for combination in the prior art” that discloses the recited limitations of independent claims 1, 5, and 11, and recognizing allowable subject matter in dependent claims 2-4, 6-10, and 12-14. Ex. 1002, 378-82, 379-80.

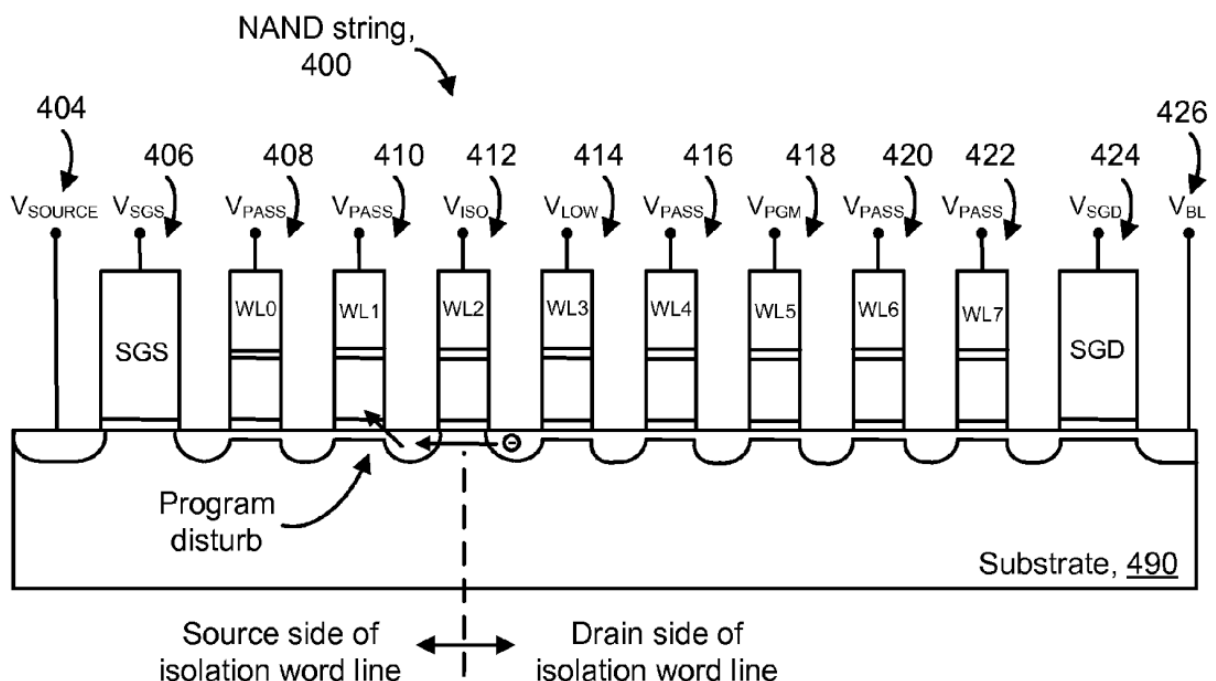
88. I did not see any prosecution history disclaimer or definitions set forth that impact any of my opinions regarding claim construction, discussed below.

D. *Challenged Claims*

89. Petitioner presents four grounds to challenge the patentability of claims 1, 3-11, and 13-14 of the '941 Patent. Pet. 7. Each ground relies on Dong (Ex. 1005) as the primary reference. *Id.* In particular, Petitioner alleges that Dong alone anticipates and renders obvious all independent claims (claims 1, 5, and 11) and several dependent claims (claims 3, 6, 7, and 13). *Id.* Petitioner also relies on Dong combined with secondary reference Costa (Ex. 1012) to allege that claims 8-9 are obvious, and on Dong combined with secondary reference Shirai (Ex. 1018) to allege that dependent claims 4, 10, and 14 are obvious. *Id.*

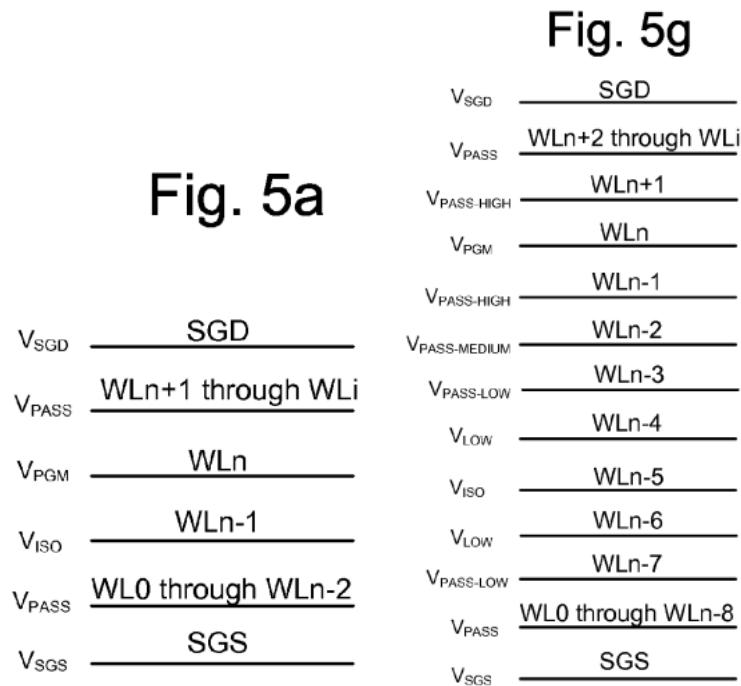
E. Dong (Ex. 1005)

90. In my opinion, Dong discloses a purported solution to address program disturb in 2D NAND memory strings. Ex. 1005 ¶¶11, 45, Fig. 4. For example, as a POSITA would understand, Figure 4 of Dong illustrates a cross-section of a two-dimensional NAND memory string 400 with storage elements (408, 410, 412, 414, 416, 418, 420, and 422), their corresponding word lines (WL0, WL1, WL2, WL3, WL4, WL5, WL6 and WL7), source-side select gate control line SGS (406), and drain-side select gate control line SGD (424) at the same physical level in a horizontal arrangement above a substrate (490). Ex. 1005 at ¶¶19, 45, 48, 49. As shown below, the wordlines (WL0 to WL7) are arranged horizontally, with no word line at the “bottom” or “top” compared to any other wordline.



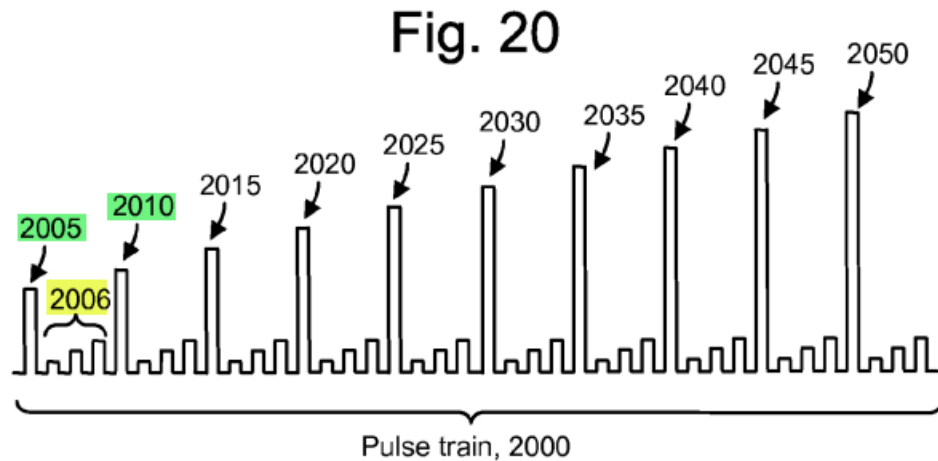
Id. at Fig. 4, ¶¶45, 48, 49. A programming voltage V_{PGM} is applied to the fifth word line (418, “WL5”) when it is selected for programming. *Id.* ¶¶45-46. As seen above, other voltages V_{PASS} , V_{ISO} , and V_{LOW} are applied to neighboring word lines of the NAND cell that are not selected for programming. *Id.* ¶46. It is important to note that even though Dong teaches applying different voltages to different word lines in a 2D (or Planar) memory, “[t]he program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed.” Ex. 1009 pt. 2 at 354.

91. Dong explains that “FIGS. 5a-h depict different examples of self-boosting modes,” showing different voltages applied to unselected wordlines. Dong, ¶20; *see also* Ex. 1009, 52-54 (describing self-boosting schemes for 2D NAND).



Dong, Figs. 5a, 5g. In these figures, which do not depict physical memory, Dong discloses local self-boosting schemes with an isolation wordline on the source side of the selected wordline being programmed (i.e., WLn). In Figure 5a, for example, WLn-1, located on the source side of WLn (which is being programmed, i.e., receiving V_{PGM}), receives an isolation voltage (V_{ISO}). *Id.*, ¶49.

92. In addition to the program operations of Figures 5a and 5g, Dong discloses a verify phase as seen in verify pulse set 2006 (yellow) between program pulses 2005 and 2010 (green).



Dong, ¶132, Fig. 20.

93. During verification, “read voltages, which are typically less than the boost voltages, are applied to the unselected wordlines.” *Id.*, ¶133; *see also id.*, ¶¶9, 50 (“verify pulses can be applied between program pulses to verify whether the selected storage elements have reached a targeted programming condition”), 71 (programming “is typically followed by a sequence of verify pulses to determine if the storage elements have reached a desired programming state”).

F. Claim Construction

94. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by Counsel of the legal standards that apply to claim construction in an inter partes review, and I have applied them in forming my opinions. I understand

that during an inter partes review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

95. I understand that claims must be construed in light of and consistent with the intrinsic evidence. In this context, intrinsic evidence includes the claims themselves, the written disclosure in the specification including all figures, and the patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office ("USPTO"), and references cited on the patent itself. I understand that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony, but that such extrinsic evidence should be given less weight than the intrinsic evidence. I also understand that extrinsic evidence can be used in claim construction when the intrinsic evidence does not clearly provide the meaning of a claim term. However, I understand that extrinsic evidence cannot contradict the intrinsic evidence.

96. I understand that claim terms are assigned their ordinary and customary meaning to a POSITA, unless the specification or prosecution history provides a special, different meaning. I further understand that a POSITA is expected to read each claim term in the context of the entire patent, including the specification, which is always highly relevant and the single best guide to the meaning of a disputed term.

97. I understand that a claim's preamble is considered to be limiting if it recites essential structure or steps or it is necessary to give life, meaning, and vitality to the claim. A preamble is also considered to be limiting if it provides antecedent basis for terms later recited in the claim or subsequent dependent claims. On the other hand, I understand that a preamble is not limiting where the body of a claim defines a structurally complete invention and the preamble only states a purpose of intended use for the invention.

98. I further understand that the relevant timeframe for assessing the '941 Patent for purposes of this declaration is around February 10, 2020, the earliest priority date. If I refer to the time of the invention in this declaration, I am referring to this timeframe.

1. *Overview of My Claim Construction Opinions*

99. Dr. Liu asserts that “the terms of the '941 patent's claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.” Ex. 1004 ¶ 79.

100. However, when analyzing the '941 Patent claims, Dr. Liu incorrectly rewrites the claimed phrase “from bottom to top” to “from source to drain.” Ex. 1004 ¶¶ 120, 112-113. Dr. Liu states that “it was (and is) common when discussing

NAND flash memory to refer to the source end of a memory string as the ‘bottom,’ and the drain end as the ‘top.’ I apply that common usage here.” Ex. 1004 ¶ 120.

101. For the phrase “a program operation” recited in each independent claim, Dr. Liu fails to raise any construction. *See* Liu, ¶¶79,128-130 (failing to provide any construction when addressing the first instance of “a program operation” when it appears for the first time for claim 5 in limitation [5.A]), 177-179 (failing to provide any construction when addressing “a program operation” when it appears for the first time for claim 1 in limitation [1.H]), 196 (failing to provide any construction when addressing “a program operation” when it appears for the first time for claim 11 in limitation [11.A]).

102. Yet during deposition, Dr. Liu revealed for the first time that he interprets “a program operation” to include **both** a program phase and a verify phase. Liu Dep. (Ex. 2021), 211:1-18 (Q: “[F]or the limitation ‘[w]hen an xth wordline is used to perform a program operation,’ the phrase ‘a program operation’ is interpreted by you to include both of those phases, the program and the verifying phase?” A: “That’s correct.”); *see also id.*, 211:19-212:17, 207:20-210:22. Dr. Liu’s attempts to rewrite the claims should be rejected because they conflict with plain language and the intrinsic record, as I explain below.

103. To be clear, I do not believe these terms require construction for the Board to find all challenged claims patentable. The Board need only apply the

plain and ordinary meaning of these terms. If the Board were to construe “from bottom to top,” its construction would be, consistent with plain meaning, from lowest to highest—not from “source end” to “drain end” as Petitioner suggests. Similarly, if the Board were to construe “a program operation,” its plain and ordinary meaning is an operation performed by applying a program voltage to a selected wordline to program a selected memory cell—not both a program phase and verify phase, as Petitioner’s expert suggests.

104. Finally, in my opinion, the Board should interpret the preambles of claims 5 and 11 as limiting because they recite “essential structure” providing antecedent basis for subsequent limitations.

105. I reserve the right to propose alternative constructions in other proceedings.

2. “From Bottom To Top” (all claims)

106. The Petition reflects Dr. Liu’s claim construction position, and adopts his erroneous interpretation of “from bottom to top.” Pet. 34-35. Petitioner states that “[t]he ’941 Patent does not define the phrase *bottom to top*, but it was (and is) common in NAND flash memory devices to refer to the source end of a memory string as the ‘bottom,’ and the drain end as the ‘top.’ ... That common usage will be applied here.” Pet. 35 (citing Ex. 1004 ¶¶112-113, 120). In the parallel district court litigation, Petitioner’s expert Dr. Schubert applied the same erroneous claim

construction in his declaration, stating, “the plain and ordinary meaning of ‘from bottom to top’ as understood by a POSITA would have been ‘from the source to the drain side.’” Ex. 2010 (Schubert Decl.) at 60 (¶157).

107. Looking at the claimed phrase “from bottom to top” as recited in the ’941 Patent claims, in my opinion, the plain meaning of “bottom” is not “source” and the plain meaning of “top” is not “drain.” In my opinion, based on the intrinsic evidence, as well as my knowledge and experience, a POSITA would understand the ordinary meaning of “bottom” and “top” controls—bottom means lowest point and top means highest point relative to the substrate. *See* Ex. 1001, 1:26-41, 6:39-47; Ex. 2013, 4-5 (“bottom”: “the lowest part or place” / “top”: “the highest part, point or level of something”); *see also* Ex. 2014, 3-4 (“bottom”: “the deepest or lowest part” / “top”: “the uppermost part, point, surface, or end”).

108. In my view, the term “from bottom to top” has no special meaning in the semiconductor manufacturing context or in the context of the ’941 Patent. The ’941 Patent and its prosecution history provides no special definition for the phrase “from bottom to top.” There is also no prosecution history disclaimer that would impact the meaning of “from bottom to top.” In my opinion, the ’941 Patent claims, which recite word lines arranged “from bottom to top,” use that phrase in its plain and ordinary sense, simply referring to word lines vertically arranged from lowest (bottom) to highest (top), as the intrinsic evidence confirms.

109. In my opinion, the terms of the '941 Patent's claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration. Accordingly, I have given the terms in the challenged claims their plain and ordinary meanings, as would have been understood by POSITA at the time of the invention, taking into consideration the language of the claims, the specification, and the prosecution history of the '941 Patent. In my declaration, I apply the plain and ordinary meaning of the recited phrase "from bottom to top" in the context of word lines, which is simply referring to word lines vertically arranged from lowest to highest, as the intrinsic evidence confirms. I have applied this understanding of the claim terms in my analysis and in forming my opinions where appropriate in this declaration.

**a. *The Intrinsic Evidence of the '941 Patent Shows
"From Bottom To Top" Means From Lowest To
Highest***

110. The '941 Patent claims refer to wordlines in a vertical arrangement by reciting wordlines arranged "from bottom to top":

- Claims 1, 7, and 11: "an (m+1)th word line to an nth word line *from bottom to top*";
- Claims 2, 5, and 12: "a first word line to a kth word line *from bottom to top*"; and

- Claim 11: “a (k+1)th word line to an mth word line *from bottom to top*.”²

111. Other limitations of the claims confirm the vertical word line arrangement, reciting portions, which consist of wordlines, formed “above” or “below” each other (claims 1-3, 5, 7, 11-13) and “dummy word line[s]” formed “above” and “below” other portions (claims 4, 10, 14).

112. As the Board correctly recognized at institution, “[t]he independent claims state that the second memory portion is *formed* either *above* or *below* the first memory portion,” establishing “a relative top and bottom.” ID, 16-17 (emphasis original). The Board also correctly recognized, in my opinion, that “[g]iven that the claims themselves identify relative vertical locations of the memory portions ... it follows that that claim terms referring to the top and bottom of wordlines within the memory portions also refer to relative vertical locations of the wordlines within the memory portions.” *Id.*, 17. The Board thus correctly found that the claimed phrase “from bottom to top” means “the wordlines of the memory portions are arranged vertically from the bottom end of the memory portion toward the top of the memory portion.” *Id.*

² Emphasis added unless stated otherwise.

113. I also agree with the Board's recognition that this construction is confirmed by the specification, noting that the '941 Patent is directed to a three-dimensional NAND memory with wordlines arranged vertically, one on top of another. ID, 17. Like the claims, a POSITA would recognize that the specification describes wordlines vertically arranged "from bottom to top"—with no reference to any source or drain. *See, e.g.,* Ex. 1001, 4:29-36; *see also id.*, Abstract; ID, 17. Figure 8, for example, illustrates a three-dimensional memory with a first portion 710 (blue) and a second portion 720 (orange), each including wordlines arranged vertically from bottom to top (i.e., from lowest to highest) above the substrate (not shown).

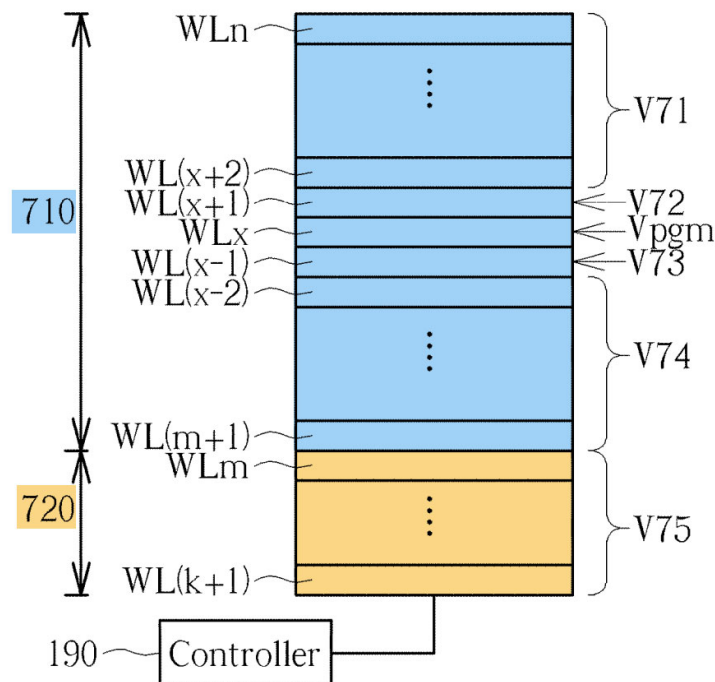


FIG. 8

Ex. 1001, Fig. 8; *see id.*, 1:26-41, 6:39-47.

114. In my opinion, the specification also clearly supports that the '941 Patent is directed to a three-dimensional NAND memory with word lines arranged vertically, one on top of another. As seen above, the first portion 710 includes “an (m+1)th wordline WL(m+1) to an nth word WLn line *from bottom to top*.” Ex. 1001, 4:32-34; *see also id.*, Abstract. Consistent with the plain and ordinary meaning of the term “bottom,” the (m+1)th wordline is shown as the vertically lowest wordline in first portion 710. *Id.*, 4:29-32, Fig. 8. Similarly, and consistent with the plain and ordinary meaning of the term “top,” the WLn wordline is shown as the vertically highest wordline in first portion 710. Ex. 1001, 4:29-32, Fig. 8; *see also* Ex. 1001, 4:34-36 (same for “second portion”). Additionally, the figure shows the “second portion 720 ... below the first portion 710” Ex. 1001, 4:34-35.

115. The specification further describes this vertical arrangement by referring to “portions” that are “above” or “below” each other, where each “portion” consists of “wordlines.” Ex. 1001, Abstract, 2:65-3:3 (first and second portions), 4:30-36 (same), 1:46-50 (same), 1:56-60 (same), 2:4-6 (same), 2:14-18 (same); *id.* 3:46-48 (third portion), 5:7-9 (same), 5:32-34 (same); *id.* 5:4-19 (describing that programming occurs in a wordline in a portion “above the lowermost portion”). At institution, the Board correctly recognized, in my opinion, that the specification “describes embodiments with first, second, and/or third memory portions as including various wordlines ‘from bottom to top’ and that the

memory portions are formed above or below each other.” ID, 17. The Board found Patent Owner’s construction correct, “not from source side to drain side” as Petitioner proposed. ID, 17-18 (citing ’941 Patent at 1:45-50, 1:55-60, 2:1-7, 2:14–18, 2:64-3:3, 3:46-48).

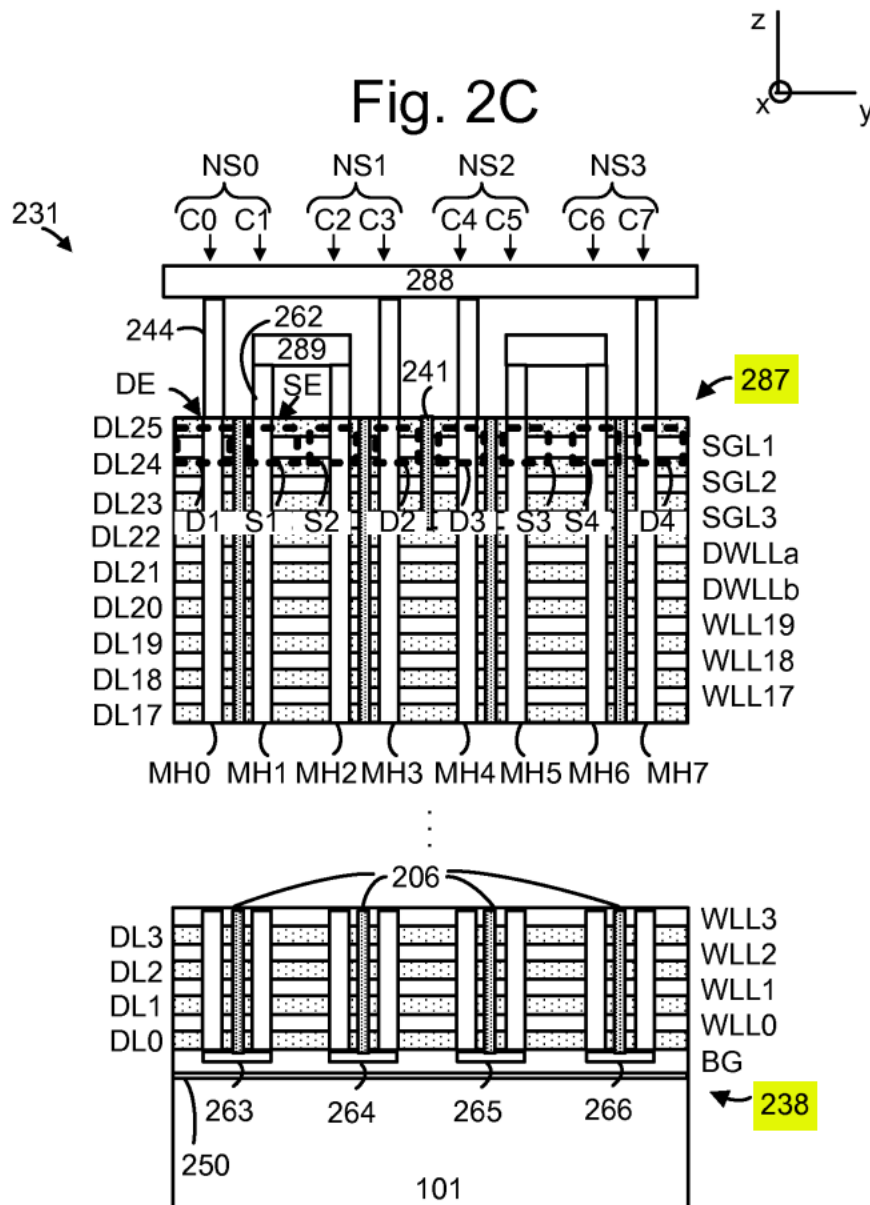
116. A POSITA would also recognize that all other figures of the ’941 Patent illustrate wordlines arranged vertically, as in Figure 8, reinforcing that the plain and ordinary meaning of “bottom” and “top” applies. Ex. 1001, Figs. 1-7, 9-11. The Board recognized as much at institution, correctly stating, in my opinion, that “the ’941 patent illustrates and describes figures of memory devices having wordlines arranged vertically from bottom to top” and that “Figures 1-11 each depict ‘a memory’ having vertically arranged wordlines.” ID, 17.

117. In my opinion, the Board also rightly recognized the specification’s description of wordlines relative to the “lowermost” or “uppermost” portion of a memory supports Patent Owner’s position. *See, e.g.*, Ex. 1001, 5:10-12, 5:15-19, 5:38-50. A POSITA would recognize that this description shows “the Specification identifies the location of the wordline in relation to its vertical location, not to its location relative to the source or drain,” as the Board found. ID, 18.

118. Other intrinsic evidence, like the references cited on the face of the ’941 Patent, reaffirm that a POSITA would interpret wordlines arranged “from

bottom to top” to mean from lowest to highest, and not from source to drain.

Exhibit 2011—by the same inventor as Dong—describes a 3D NAND memory stack with “a top 287 and a bottom 238,” referring to the respective highest and lowest portions of the memory stack (i.e., below bit line 288 and vias 244, 262, and above substrate 101).



Ex. 2011, ¶¶75, 77, Fig. 2C

119. In the same vein, Exhibit 2012, also cited on the '941 Patent, discloses a NAND string in a U-shape, “with external elements (source line ‘SL’ and bit line ‘BL’) located at the top of the structure,” and “[a]t the bottom of NAND string 815 is a controllable gate (back gate ‘BG’).”

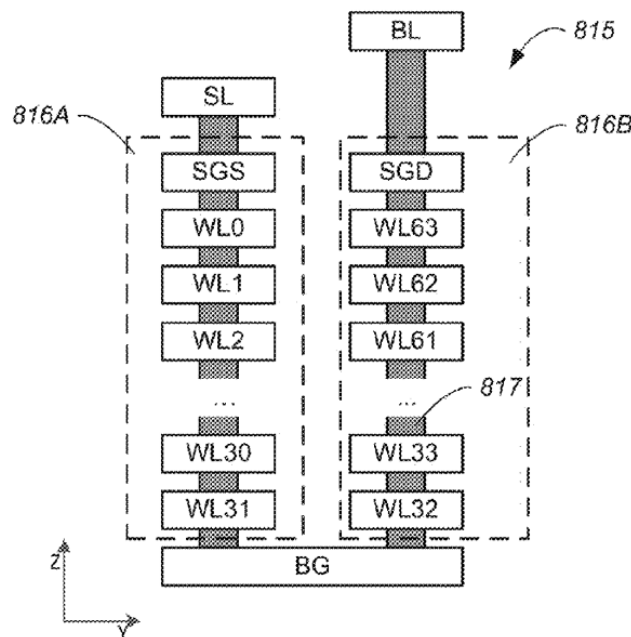


FIG. 8

Ex. 2012, ¶84, Fig. 8

120. In my opinion, this is an example that also shows Petitioner’s claim that “bottom to top” means “source to drain,” Pet. 35, is wrong because the word “bottom” refers to the vertically lowest element, the “back gate ‘BG,’” *not* to the “source.” In the same way, the word “top” refers to the two elements (source line “SL” and bit line “BL”) shown vertically highest, *not* to the drain.

121. In my opinion, because the intrinsic evidence clearly establishes to a POSITA that “from bottom to top” in the context of the '941 Patent has its plain and ordinary meaning of from vertically lowest to vertically highest, extrinsic evidence is of little use. And the extrinsic evidence provided by Petitioner and its expert is actually in stark contradiction with the intrinsic evidence.

122. However, Petitioner and its expert Dr. Liu rely on extrinsic evidence to interpret the claimed phrase “from bottom to top.” Pet. 35 (citing Ex. 1004 ¶¶112, 113, 120). But the extrinsic evidence like Exhibit 1009 cited by Petitioner and Dr. Liu support that “from bottom to top” means from lowest to highest (not from source to drain as Petitioner and Dr. Liu allege).

123. Petitioner’s Exhibit 1009 uses the terms “top” and “bottom” to describe the vertically highest and vertically lowest physical components of 3D NAND memory—not where the source or drain are located. *See, e.g.*, Ex. 1009, 327 (“[T]he charge trap nitride layer is physically connected from top to bottom [control gates] in 3D SONOS/TANOS NAND flash.”). In my opinion, the Board correctly recognized that this disclosure, along with the U-shaped example above, “belies Petitioner’s contention that ‘from bottom to top’ means from source end to drain end.” ID, 19. A POSITA would not view this use of the terms “bottom” and “top” as describing locations of the source or drain.

124. Instead, a POSITA would view this disclosure in Exhibit 1009 as aligning with the ordinary meaning in the Merriam-Webster Dictionary, which defines “bottom” as “the lowest part or place” and “top” as “the highest part, point or level of something.” Ex. 2013 at 83, 752; *see also* Ex. 2014 (2018 American Heritage Dictionary) (defining “bottom” as “the deepest or lowest part” and “top” as “the uppermost part, point, surface or end”).

125. In light of the evidence supporting Patent Owner’s construction, I agree with the Board’s correct finding at institution that “the claim language referring to first and second memory portions that comprise wordlines ‘from bottom to top’ to mean that wordlines of the memory portions are arranged vertically from bottom (lowest) to top (highest).” ID, 19.

b. *Petitioner’s Proposed Construction Relies Solely on Extrinsic Evidence*

126. Petitioner and Dr. Liu do not rely on intrinsic evidence to support their position that “from bottom to top” means “from source to drain.” Petitioner and Dr. Liu only mention the ’941 Patent once, to state that that it “does not define the phrase bottom to top.” Pet. 35; Ex. 1004 ¶120 (“The ’941 patent does not provide a definition for bottom to top.”). But a POSITA would view the intrinsic evidence (i.e., claims and specification, including figures) as instructive when interpreting the claimed phrase “from bottom to top.” Petitioner also ignores the ’941 Patent’s consistent usage of the phrase “bottom to top” to refer to the vertically lowest and

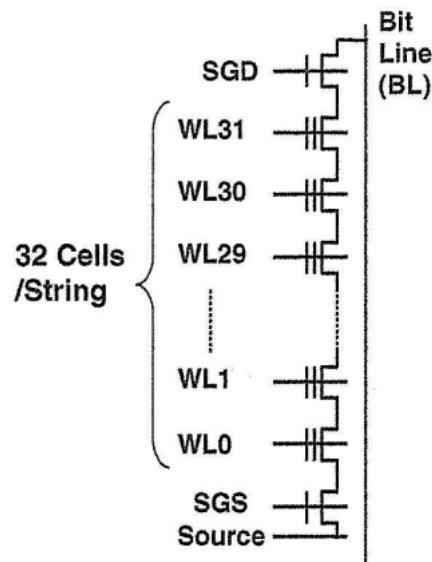
highest word lines respectively, consistent with the plain and ordinary meaning of this phrase. *See* Ex. 1001 at 1:55-60, 2:1-11, 2:12-18, 2:63-3:3, 3:46-52 4:29-36, 5:4-9, 5:24-37; *see also id.* at Abstract. I agree with the Board's recognition as institution that "Petitioner does not point to any persuasive intrinsic evidence to support its contention that 'from bottom to top' means 'from the source side to the drain side.'" ID, 18.

127. In my opinion, Petitioner's construction that "from bottom to top" means "from source to drain" is not supported by the intrinsic evidence. The figures of the '941 Patent do not show the source or drain of the inventive memory. *See* Ex. 1001 at Figs. 1-11. The claims do not recite a "source" or a "drain." *See id.* at 6:55-8:54. And the specification never refers to or depicts the "source" or "drain" ends of a memory string, much less reference "source" or "drain" to define the "bottom" and "top." In my opinion, Petitioner's construction ignores the clear intrinsic evidence and instead relies solely on extrinsic evidence which departs from the plain and ordinary meaning of "from bottom to top" to a POSITA.

128. In my opinion, the extrinsic evidence does not consistently teach that "bottom" means closest to the source and "top" means closest to the drain. Petitioner asserts that "it was (and is) common in NAND flash memory devices to refer to the source end of a memory string as the 'bottom,' and the drain end as the 'top.'" Pet. 35 (citing Ex. 1004 ¶¶112-113, 120). In support, Petitioner relies on

its expert's interpretation of circuit diagrams (not physical memories) for 2D NAND flash memories, which he says show “the source end of the NAND string at the bottom, and the drain end of the NAND string at the top.” Ex. 1004 ¶113; Pet. 35. But the examples cited by Petitioner's expert *do not actually use the word “bottom” to refer to the word line closest to the source or the word “top” to refer to the word line closest to the drain.*

129. The following circuit diagram from Exhibit 1009, relied on by Petitioner's expert, provides an example:



Ex. 1009 pt. 1 at 39 (Fig. 2.2); Ex. 1004 ¶113. This figure shows a circuit diagram for a 2D NAND flash memory consisting of several word lines (“WL0” to “WL31”) and select transistors “SGD” and “SGS” to isolate the NAND string. SGD is connected at the drain end (the bit line end) of the NAND string, while SGS is connected at the source end of the NAND string. See Ex. 1004

¶113. The description of this circuit in Ex. 1009 does not use the word “bottom” to refer to the word line closest to SGS or the word “top” to refer to the word line closest to SGD. Moreover, the diagram above is not a representation of the physical layout of the memory, as a POSITA would readily understand. On the contrary, as evidenced by its use of the circuit symbols for flash and NMOS transistors, it is a symbolic circuit diagram – a symbolic depiction of the connectivity of the circuit of the NAND string. For example, the below illustrates a physical representation of a floating gate memory cell on the left, and a circuit symbol of a floating gate memory cell on the right—the same circuit symbol that corresponds to the memory cells connected to the word lines seen in the above circuit diagram from Ex. 1009.

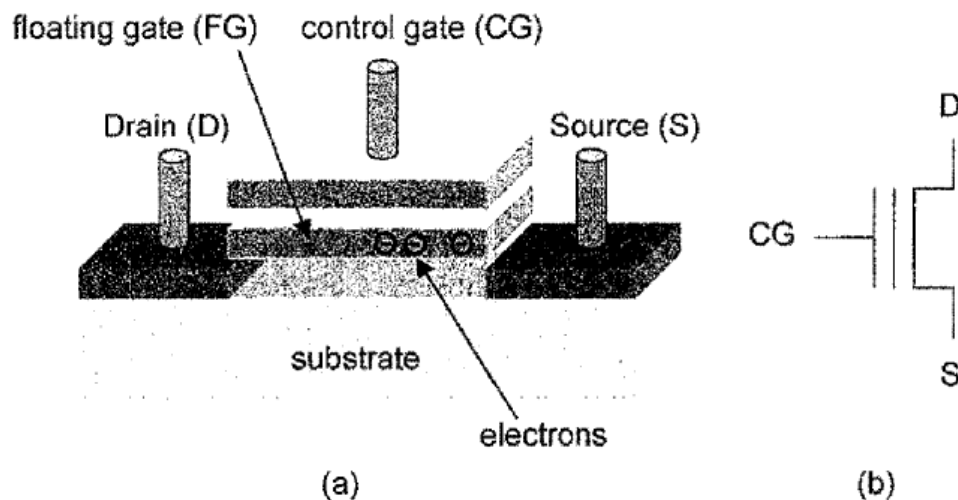
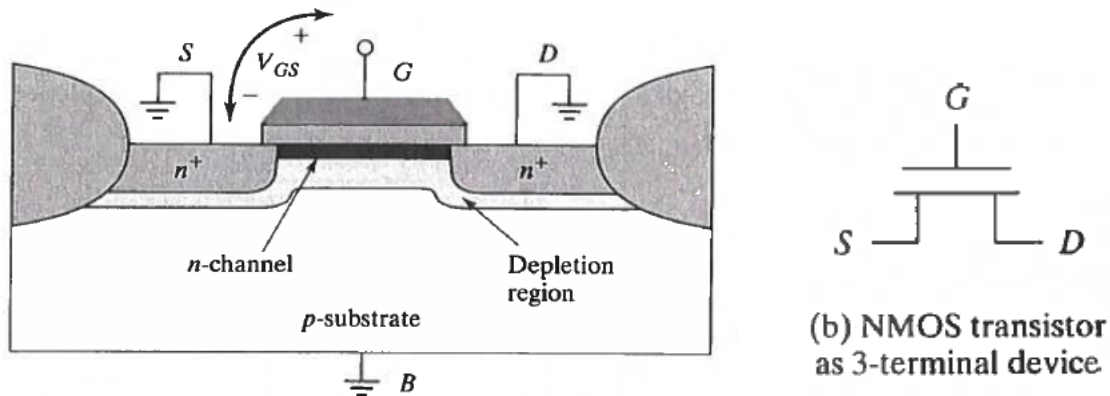


Fig. 2.1. (a) Floating gate memory cell and (b) its schematic symbol

Ex. 2017, 7, Fig. 2.1. Similarly, the below example illustrates a physical

representation of an NMOS transistor on the left, and a circuit symbol of an NMOS transistor on the right—the circuit symbol that corresponds to the select transistors seen in the above circuit diagram from Ex. 1009 (i.e., “SGS,” “SGD”).

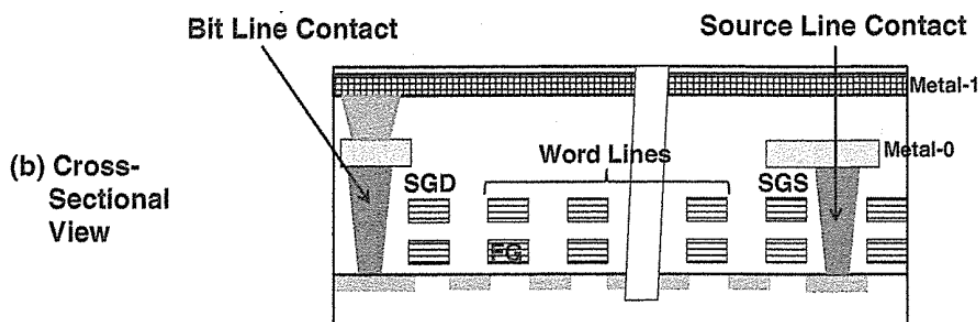


Ex. 2019, 8-9, Figs. 3-13 (physical representation of an NMOS transistor), 3-12(b) (circuit symbol for an NMOS transistor).

130. In my opinion, a POSITA would agree with the Board’s recognition at institution that “Petitioner fails to persuasively explain ... how figures that depict the architecture of 2D NAND strings with the source end on the bottom means that the term ‘from bottom to top’ means from source end to drain end.” ID, 18-19.

131. In my opinion, a POSITA would readily understand that diagrams like the above are merely symbolic depictions of the circuit and its connectivity, and do not reflect the actual, physical arrangement of word lines on the memory. Petitioner’s expert Dr. Liu confirms that the circuit diagram he relies on, including the one above from Ex. 1009, “are discussing two-dimensional NAND flash

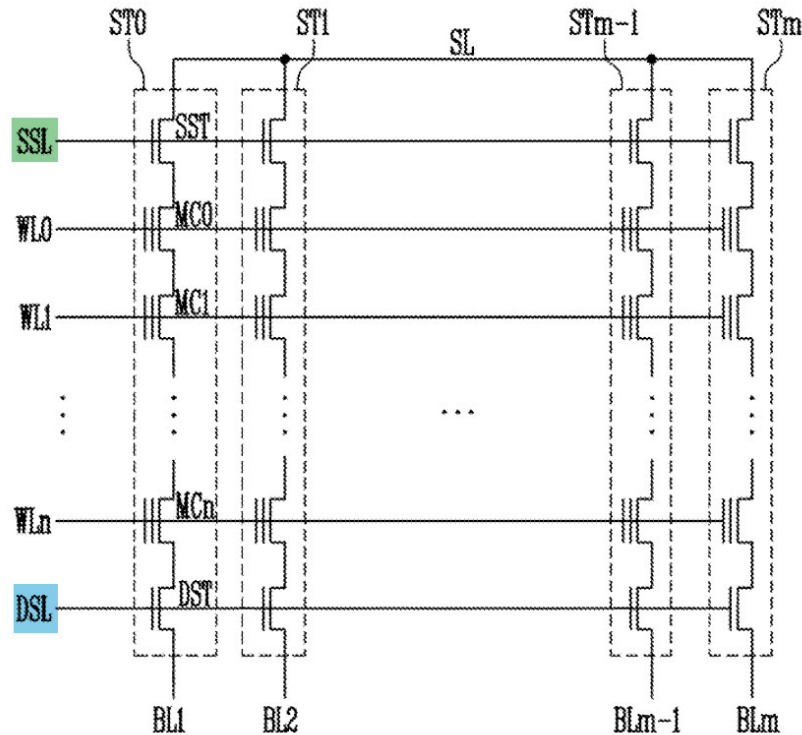
memories.” Ex. 1004 ¶113. I agree. While the symbolic circuit diagram shown above is depicted with a vertical orientation, two-dimensional NAND flash memories have word lines that are physically arranged in a horizontal plane above the substrate, i.e., from left to right, as seen in the below figure. This figure appears immediately after Figure 2.2 in Ex. 1009 (which was shown above) and is referred to as the physical “cross-sectional view” of the 2D NAND flash memory cells:



Ex. 1009 pt. 1 at 38-40, Fig. 2.3 (cropped). A POSITA would understand that in this physical planar structure, word lines are not physically arranged “from bottom to top” because they are not arranged in a vertical direction at all. Despite Petitioner’s claim that “it was (and is) common in NAND flash memory devices to refer to the source end of a memory string as the ‘bottom,’ and the drain end as the ‘top’” (Pet. 35 (relying on Ex. 1004, ¶¶112-113, 120), none of Petitioner’s expert’s support in ¶¶112-113, 120 to substantiate this faulty construction for “from bottom to top” use the word “bottom” to refer to the source, or the word “top” to refer to the drain.

132. A POSITA would not interpret “from bottom to top” to mean “from source to drain” based on a few cited references that show, but do not discuss, symbolic circuit diagrams with the source end of a memory string at the bottom of the diagram, and the drain end of a memory string at the top end of the diagram. A POSITA would know that many other references show different arrangements, disproving Petitioner’s suggestion that it was (and is) common convention for “bottom to top” to mean “source to drain.” *See* Pet. 35 (citing Ex. 1004 ¶¶112-113, 120).

133. As an example, U.S. Patent Publication No. 2016/0343414 (Ex. 2015), cited on the '941 Patent, provides a circuit diagram of a memory string with the source (“SSL” or “source select line,” in green) at the top and the drain (“DSL” or “drain select line,” in blue) at the bottom:



Ex. 2015, Fig. 2, ¶¶15, 44-46. To the extent that Petitioner's cited diagram from Figure 2.2 of Ex. 1009 is viewed as showing the memory's physical structure (which would be incorrect because it is a symbolic circuit diagram, with symbols for the circuit elements such as flash and NMOS transistors), the above diagram from Ex. 2015 shows the opposite arrangement with the source at the top and the drain at the bottom. *See, e.g.,* Ex. 2017 at 7, Fig. 2.1 (illustrating a physical representation of a floating gate memory cell next to its circuit symbol seen in circuit diagrams) Ex. 2019 at 8-9, Figs. 3-13 (physical representation of an NMOS transistor), 3-12(b) (circuit symbol for an NMOS transistor).

134. Furthermore, a POSITA would understand that in two-dimensional memory arrays (such as those discussed above) the word lines are physically arranged horizontally from left to right; and therefore neither the source nor the drain is at the “bottom” or “top” because they are at the same physical height above the substrate.

135. For example, the Aritome reference (Ex. 1009) cited by Petitioner illustrates physical diagrams (both a top view and a cross-sectional view) of a two-dimensional NAND flash memory array with the source (near the “SGS” or the Select Gate Source, in green) and the drain (near the “SGD” or Select Gate Drain, in blue) at the same physical level as the word lines above the substrate:

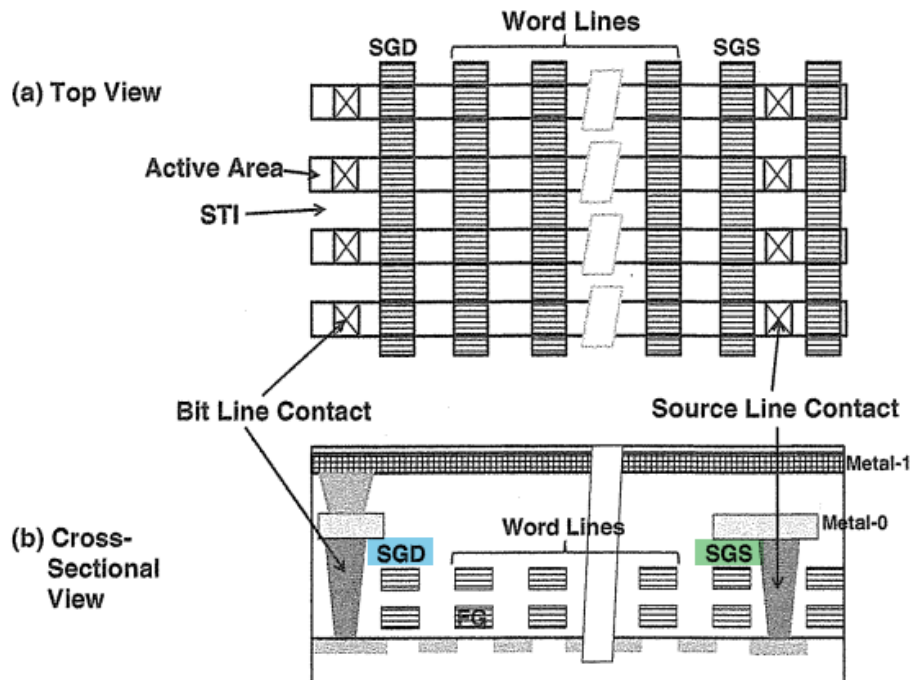


FIGURE 2.3 (a) Top schematic view and (b) cross-sectional view of NAND flash memory cells.

Ex. 1009 at 39-40.

136. In my opinion, if Petitioner's construction were adopted, it would lead to the incorrect conclusion that, as Petitioner's expert in the district court litigation admitted, the "bottom and top are at the same physical level." Ex. 2010 (Schubert Decl.) at 59. In other words, Petitioner's construction would effectively rewrite "from bottom to top" in the claims to "from source to drain," rendering both "bottom" and "top" meaningless, especially in the physical two-dimensional NAND flash memory array (like the one depicted above in Figure 2.3 of Ex. 1009) where the source and the drain are at the same physical level as the word lines above the substrate. In other words, Petitioner's construction interprets the claimed phrase "bottom to top" in a way that effectively removes its significance from the claim, by giving no meaning to "bottom" or "top," and instead allowing, for example, "from bottom to top" to effectively mean "from right to left" in the two-dimensional memory array from Ex. 1009 above.

137. Petitioner's construction also makes no sense because, even in a three-dimensional NAND memory structure, the "source" is not necessarily at the "bottom" and the "drain" is not necessarily at the "top." A POSITA would understand that both the "source" and the "drain" can be at the "top." For example, U.S. Patent Publication No. 2019/0006021 ("Ghai"), cited by the '941 Patent, depicts the physical structure of a U-shaped three-dimensional NAND memory

where both the source (near the source select line “SGS,” green) and the drain (near the drain select line “SGD,” blue) are at the top, as shown in Figure 8 below.

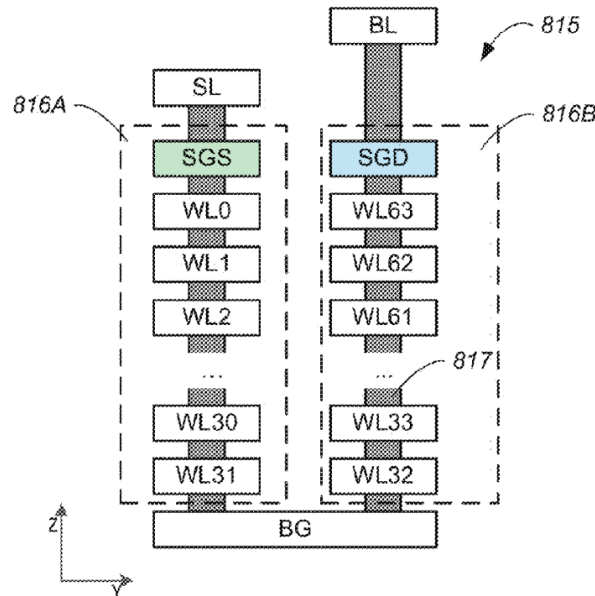
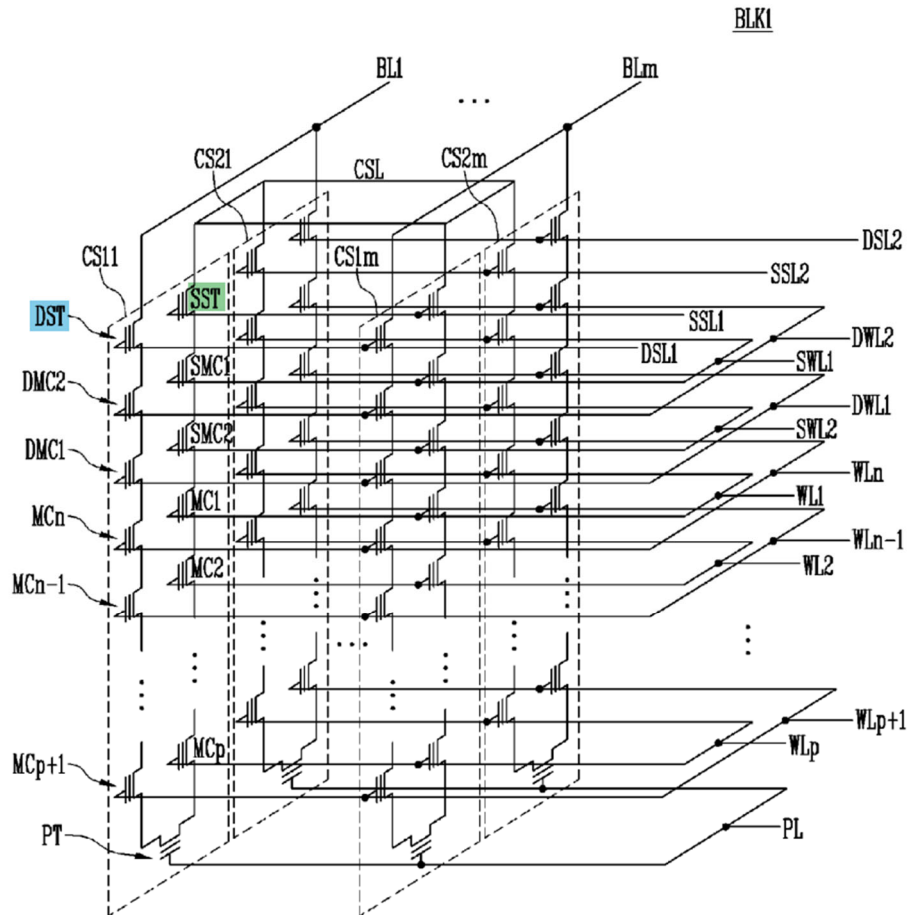


FIG. 8

Ex. 2012 (Ghai), Fig. 8 (“SGS” stands for “source select line”; “SGD” stands for “drain select line”); *see also id.* ¶¶87, 16-17, 80, 84-86, Fig. 9.

138. If one assumes that symbolic circuit diagrams show physical structure (which is incorrect, but this is what Petitioner does), then U.S. Patent Publication No. 2016/0099060 (“Yoo”), also intrinsic evidence because it is cited on the face of the ’941 Patent, shows a U-shaped memory string with both the source (near the “SST” or “source select transistor,” in green) and the drain (near the “DST” or “drain select transistor,” in blue) at the top:



Ex. 2016 (Yoo), Fig. 3, ¶¶50-65; *see also* Ex. 1008 (cited on the face of the '941 Patent) at Fig. 13, ¶¶115-129 (describing a circuit diagram of a U-shaped three-dimensional NAND memory with both the source and drain select transistors (SST and DST respectively) at the top). In light of the above examples, a POSITA would not agree with Petitioner that “it was (and is) common in NAND flash memory devices to refer to the source end of a memory string as the ‘bottom,’ and the drain end as the ‘top.’” *See* Pet. 35.

139. Petitioner’s expert Dr. Liu states that “it was well-known to POSITA’s [sic] that programming typically proceeded one cell at a time, either

from source to drain or from drain to source depending on the architecture of the system.” Ex. 1004 ¶112. In my opinion, a POSITA would not find this relevant to the meaning of “from bottom to top” as recited in the ’941 Patent.

140. In my opinion, a POSITA would view Petitioner’s proposed construction of “from bottom to top” as departing from the plain English meaning of the phrase and the intrinsic evidence. In my opinion, Petitioner’s interpretation that “from bottom to top” means “from source to drain” is not even supported by extrinsic evidence. Petitioner’s expert Dr. Liu admits that his interpretation makes it irrelevant “whether the physical device is in a horizontal or vertical direction.” Ex. 1004 ¶113.

141. I agree with the Board’s decision at institution to construe “from bottom to top” to mean “that wordlines of the memory portions are arranged vertically from bottom (lowest) to top (highest).” ID, 19.

3. “*A Program Operation*”

142. Independent claims 1, 5, and 11 each recite applying specific voltages “when an xth wordline is used to perform *a program operation*.” Ex. 1001, 6:61-67, 7:29-31, 8:21-23.

143. Looking at the claimed phrase “a program operation” as recited in the ’941 Patent claims, in my opinion, based on the intrinsic evidence, as well as my knowledge and experience, a POSITA would understand the ’941 Patent claims

use this phrase in its plain and ordinary sense, simply referring to “an operation performed by applying a program voltage to a selected wordline to program a selected memory cell.”

a. *Petitioner’s Construction Was Not Revealed Until Deposition of Dr. Liu*

144. Petitioner did not disclose a construction for “a program operation” in the Petition. Similarly, Dr. Liu did not disclose a construction for this term in his declaration.

145. Dr. Liu revealed a new position during his deposition, where he stated he construes “a program operation” to include both a program phase and verify phase. Liu Dep., 211:1-18; *see also id.* 211:19-212:17, 207:20-210:22. When asked where he disclosed this position in his declaration, he pointed only to one paragraph (¶60) in his Technology Background section. But this paragraph, in my opinion, provides no construction for the term “a program operation” because this paragraph does not refer to the claims or even mention “a program operation.” In addition, Dr. Liu’s Paragraph 60 is referred to in the Petition only once by reference through a “*see also*” cite. *Id.*, 212:22-213:12; Pet. 15.

146. In my opinion, this new construction presented for the first time during Dr. Liu’s deposition is incorrect and contravenes intrinsic evidence, as I explain further below.

b. *The Intrinsic Evidence Supports Patent Owner's Construction*

147. In my opinion, a POSITA would view the intrinsic evidence as supporting Patent Owner's interpretation.

148. As I discussed above in Section VI.B, the '941 Patent discloses a solution for reducing program disturb and pass voltage disturb on unselected wordlines when a program voltage is applied to a selected wordline. Ex. 1001, 1:34-41, 1:19-22. A POSITA would understand that these disturbances only occur when applying voltages to intentionally program a cell (to intentionally change its threshold voltage). To implement this solution, the '941 Patent describes “[a] program operation” as “an operation for programming a memory cell.” *Id.* 3:6-8.

149. The '941 Patent also describes that “[w]hen an xth word line WLx is used to perform a program operation, the controller 190 may apply a program voltage V_{pgm} to the xth word line WLx,” as shown in all Figures. *Id.*, 3:9-11, Figs. 1-13; *see id.*, 3:53-58, 4:25-28 (describing applying voltages of Figures 1 or 2 to Figure 6), 4:37-42, 4:51-55, 5:9-12, 5:16-19, 5:29-30, 5:42-62, 6:1-3, 6:21-23. When this ***program voltage*** (V_{PGM}) is applied to the selected wordline WLx, voltages (such as V1, V2, V3, and V4, or V71, V72, V73, V74 and V75) are applied to unselected wordlines. *Id.*, Fig. 8, 3:9-21, 4:29-61.

150. A POSITA would also recognize that the claims specify applying voltages “when an xth wordline is used to perform a program operation.” *Id.* 6:55-

7:2, 7:23-34, 8:15-31; *see also id.*, 6:39-43 (describing applying voltages by portion to reduce program and pass voltage disturbances).

151. It is also notable that the '941 Patent never mentions a verify phase or operation, and the disclosed voltages only accomplish the stated aim to reduce program disturb if applied **during** a program operation (i.e., an operation performed by applying a program voltage to a selected wordline to program a selected memory cell).

152. Petitioner's expert Dr. Liu's declaration supports that the program phase described in the '941 Patent is distinct from the verify phase. Petitioner's expert Dr. Liu recognized application of a program voltage like V_{PGM} "causes electron movement into the cell and raises the cell's threshold voltage," i.e., programs it. Liu, ¶57; *see id.*, ¶¶58, 60, 71. He also recognized a separate verification/read operation to determine the cell "has been sufficiently programmed (*i.e.*, its threshold voltage has moved to the desired level)." Liu, ¶60.

153. A POSITA would further recognize, in my opinion, that Petitioner's Exhibit 1009 supports Patent Owner's interpretation, confirming that "**a program operation**" is "performed by applying high-voltage V_{PGM} to control gate." Ex. 1009, 44. In my opinion, a POSITA would understand that use of a "control gate" in this context means the gate of the cell that is selected for programming (driven by the wordline WLx in the '941 Patent). This same exhibit also confirms that "a

program operation” is completed before a verify phase. Ex. 1009, 119 (“***After the program operation***, a verify operation is performed....”).

154. Similarly, Petitioner’s Exhibit 1010 states “[a] ***program operation*** applies a high programming voltage (e.g., +15 V) to the cell to change the cell’s threshold voltage to the desired range.” Ex. 1010, 280.

c. *Petitioner’s Proposed Construction Is Unsupported By Any Intrinsic Evidence*

155. In my opinion, Petitioner’s proposed construction improperly broadens “a program operation” to include a verify phase that lacks any intrinsic support. A POSITA would recognize that the ’941 Patent does not even mention a verify phase. In other words, the ’941 Patent does not describe a verify phase during which a read voltage is applied to check already-programmed cells to confirm that they are at the intended threshold voltage—i.e., after the program operation during which a program voltage is applied. Moreover, in my opinion, even if the ’941 Patent disclosed a verify phase (it does not), the recited voltages only reduce program disturb as intended if applied during a program phase.

d. *Dr. Liu’s Proposed Construction Contradicts Prior Testimony*

156. In my opinion, Dr. Liu’s deposition testimony contradicts his prior testimony before the PTAB.

157. In 2024, Dr. Liu submitted a declaration on Micron's behalf where he described a "program operation" as limited to the program phase, i.e., "a pulse that creates charge in the storage region." Ex. 2022, ¶81 ("The program operation is a pulse that creates charge in the storage region and the verify operation determines whether the pulse was sufficient to properly program the cell."). Dr. Liu distinguished this "program operation" from a "verify operation," the latter of which "determines whether the pulse was sufficient to properly program the cell." *Id.*; *see id.*, ¶¶248 ("Again, the read (verify) occurs after the program operation to verify whether the program operation was successful."), 103 (same), 47 (describing a "programming operation" as limited to the step of "applying a voltage pulse to a control gate of the selected wordline"), 181 ("It goes without saying that a memory that is read was programmed."), 188 ("This refers to the basic programming process of a programming pulse and then the read (verification) to determine whether the programming pulse was sufficient for the memory cell to reach the correct data state."), 190 ("These concerns are no less important when verifying a program operation, because the read operation to verify programming can cause the exact same problems."), 203 (describing "a program loop comprising a program operation *followed by* a verify operation"); *see also* Ex. 2023, ¶66 ("Specifically, a verify operation is a read operation executed *after* a program operation.").

158. Dr. Liu even testified about Costa (Ex. 2012 in this proceeding) in that prior proceeding: “the read (verify) occurs *after the program operation* to verify whether the program operation was successful.” Ex. 2022, ¶248; *see id.* (“[W]hen the selected memory cell is being verified, it is programmed.”).

159. Yet, in my opinion after reviewing Dr. Liu’s prior testimony and his declaration and testimony in the present proceeding, Dr. Liu takes the opposite position here, asserting that “a program operation” includes *both* the program and verify phase. Liu Dep., 211:1-18; *see supra* Section VI.F.3.a.

160. Dr. Liu now sees Costa (Ex. 2012) as *supporting* that “a program operation” includes *both* the program and verify phases. Liu Dep., 159:17-161:18 (“[A]longside that, we have another technique which is taught by Costa, that because the program operation really involves ... two operation [or] two phases; one is injecting electron the other one verification.”), 216:15-218:16 (referencing Costa to support that a “the program operation as one would be understand [sic] by a POSITA, and in the convention, would include both the injecting phase and the verification phase.”).

161. In my opinion, Dr. Liu’s contradictory testimony undermines Petitioner’s new construction.

4. *The Preambles of Claims 5 and 11 Are Limiting*

162. Claims 5 and 11 recite “[a] program method of a memory” wherein the “memory” includes distinct wordlines. Ex. 1001, 7:23-28, 8:15-20.

163. I agree with the Board’s finding at institution (ID, 14-15) that “[b]ecause the preambles of independent claims 5 and 11 provide antecedent basis for the wordline limitations recited in the body of their respective claim,” the preambles of claims 5 and 11 are limiting.

164. In the preamble of claim 5, this includes “a first wordline to a kth wordline” and “an mth wordline” providing antecedent bases for “the first wordline” and the limitation defining x, k, and m in claim 5. Ex. 1001, cl. 5.

165. Similarly, the preamble of claim 11 recites “an nth wordline,” “a (k+1)th wordline,” and “an mth wordline” that provide antecedent basis for wordlines recited in the body of claim 11. *Id.*, cl. 11.

166. In addition, the preambles of claims 5 and 11 provide antecedent basis for terms in several dependent claims, including:

- “the mth wordline” (claim 6);
- “the first portion” (claims 8-10, 13, 14);
- “the second portion” (claims 7-10, 12, 14); and
- “the kth wordline” (claim 12).

167. In my opinion, a POSITA would understand these preambles recite essential structure in defining the first and second portion and their component wordlines to which recited voltages are applied.

VII. Grounds 1 and 2: Dong Does Not Disclose Wordlines Arranged “From Bottom To Top”

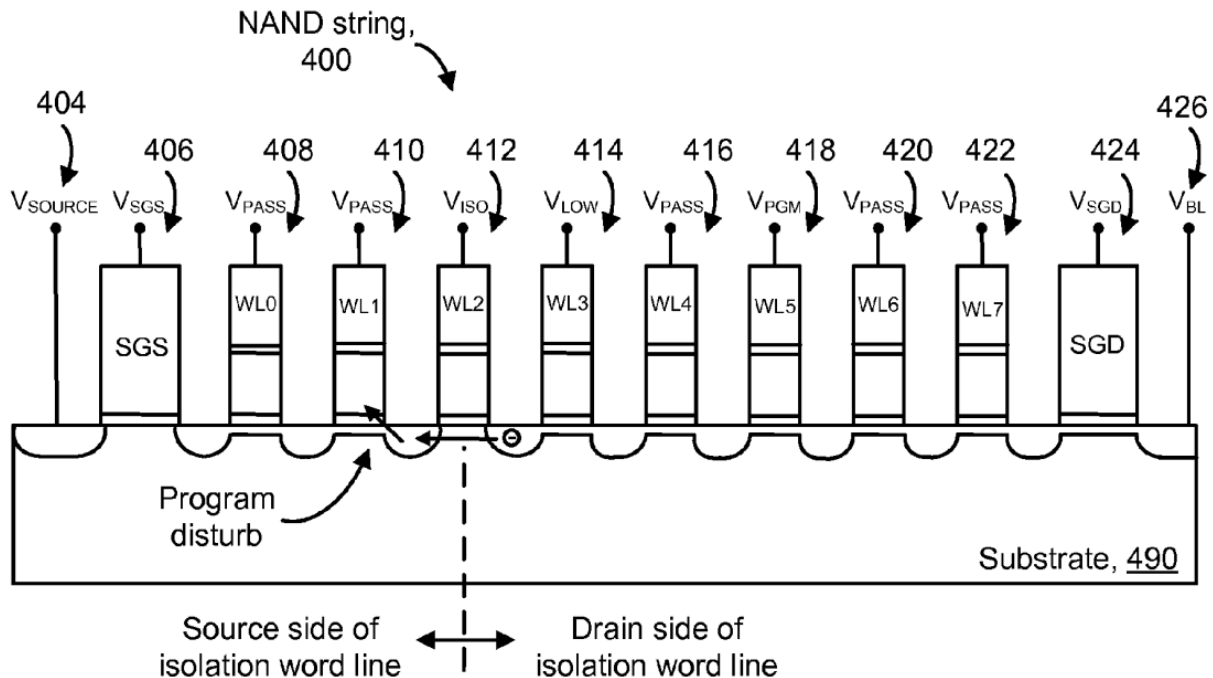
168. In my opinion, under the plain and ordinary meaning of “from bottom to top” as understood by a POSITA—i.e., from lowest to highest—all Petitioner’s grounds fail because they exclusively rely on Dong for the elements of the challenged independent claims. *See* Pet. 7. In my opinion, Dong does not anticipate or render obvious the independent claims of the ’941 Patent because it does not disclose or suggest the claimed word lines vertically arranged “from bottom to top,” i.e., from lowest to highest. Instead, Dong teaches word lines arranged horizontally, i.e., from left to right (or right to left), above the substrate.

169. Petitioner argues that “to the extent *bottom to top* is interpreted to require vertical strings in a 3D NAND memory, Dong discloses its ‘array of storage elements can be three dimensional’ and shows Fig. 5a in a vertical orientation which satisfies the claim.” Pet. 35. But as I explain below, a POSITA would have understood that a mention that an “array of storage elements can be three dimensional” is not a teaching or suggestion to have word lines arranged vertically, and Figures 5a and 5g do not represent the physical structure of the word lines.

Moreover, a POSITA would understand that these figures do not depict any vertical 3D NAND memory.

A. *Dong's Word Lines Are Arranged In A Horizontal Plane Above the Substrate, Not "From Bottom To Top"*

170. A POSITA would understand that Dong discloses its memory is 2D or Planar NAND, with word lines arranged horizontally—not from “bottom to top,” as claimed in the '941 Patent. Petitioner points to Dong's disclosure of a “memory die 1298” which “*includes a two-dimensional array of storage elements 1100.*” Pet. 34 (citing Ex. 1005 ¶¶95, Fig. 12), 51 (addressing preamble of claim 1 by citing back to claim 5), 68 (addressing preamble of claim 11 by citing back to claim 1). Dong's Figure 4 (copied below) illustrates a “cross-sectional view” of a 2D “NAND string” with storage elements (408, 410, 412, 414, 416, 418, 420, and 422), their corresponding word lines (WL0, WL1, WL2, WL3, WL4, WL5, WL6 and WL7), source-side select gate control line SGS (406), and drain-side select gate control line SGD (424) at the same physical level above a substrate (490). Ex. 1005 at ¶¶19, 45, 48, 49.



Id. at Fig. 4. As shown in Figure 4 above, a POSITA would understand that the word lines (WL0 to WL7) are arranged horizontally, from left to right. *Id.*; see also *id.* at ¶¶19, 45, 48, 49.

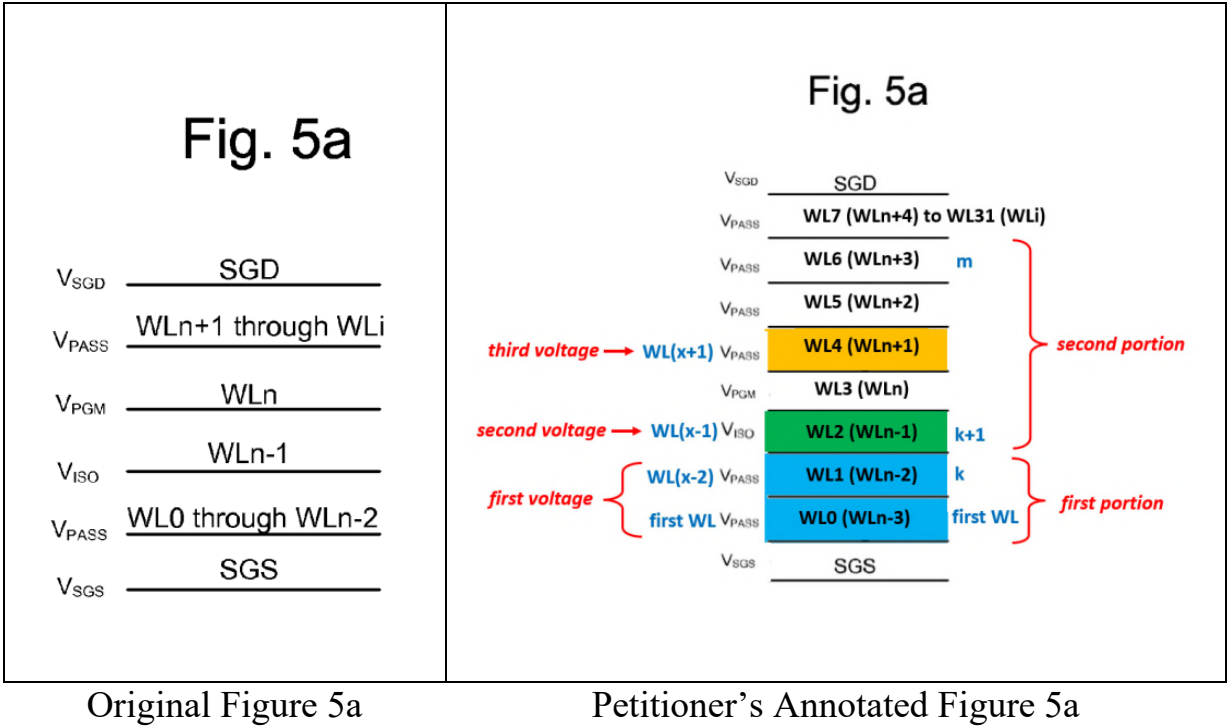
171. While Figure 4 shows the memory's physical structure, Petitioner relies on Dong's voltage charts in Figures 5a and 5g, which do not show physical structure, for the "bottom to top" claim limitations. See Pet. 29-38 (claim 5), 52-53 (claim 1), 68 (claim 11). But as mentioned, a POSITA would have understood that Dong's Figures 5a and 5g do not "teach[] or suggest[]" (ID, 24-25) any physical arrangement of wordlines. A POSITA would have understood that these voltage charts simply represent which voltages are applied to which word lines. As Dong explains, "FIGS. 5a-h depict different examples of self-boosting modes,"

showing voltages applied differently to the word lines. Dong, ¶¶20; *see* Ex. 1009, 52-54 (describing self-boosting schemes for 2D NAND).

172. A POSITA would understand that Figs. 5a-h are illustrated vertically, but they do not represent—and cannot alter—the actual physical arrangement of the word lines in the memory, which is horizontal as shown in Dong's Figure 4, as would be expected in two-dimensional NAND memory arrays. *See, e.g.,* Dong, ¶¶20, 45, 47, 87. A POSITA would also understand that Figures 5a-h simply to show the voltages applied to different word lines in different “self-boosting modes,” and they are not intended to depict the physical orientation of these word lines. *Id.*

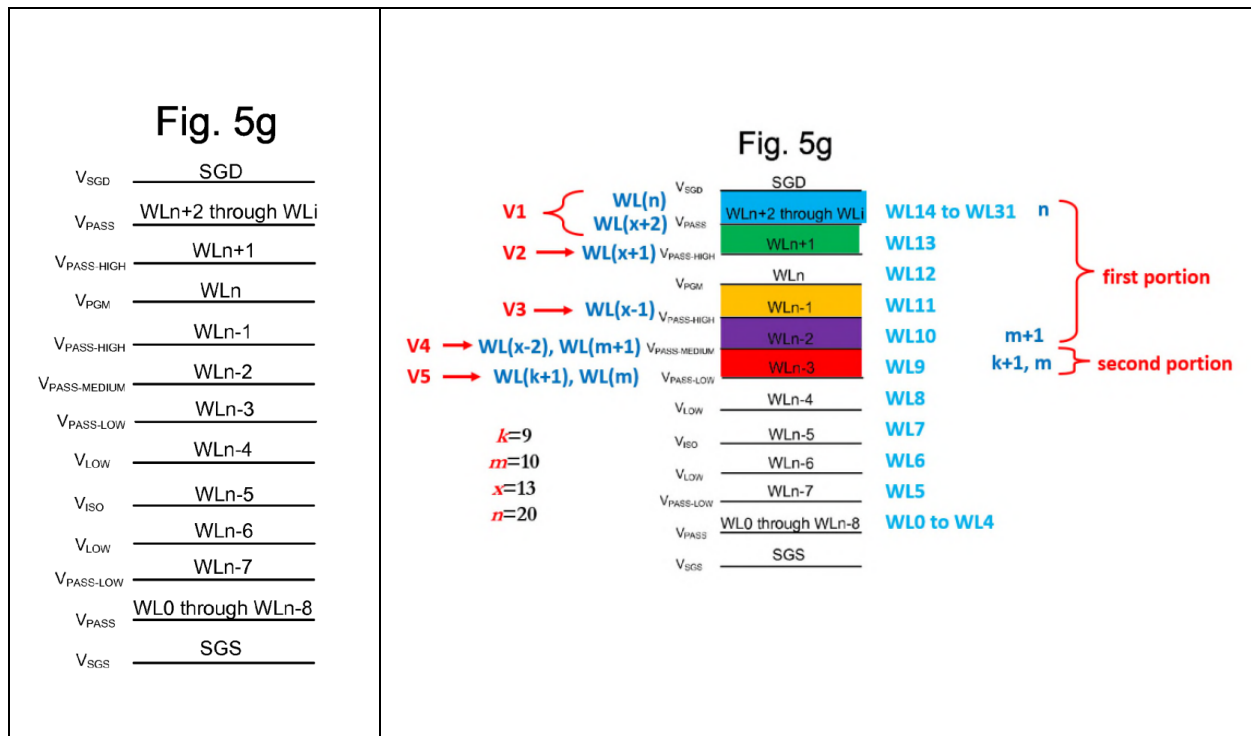
173. I agree with the Board's recognition at institution that “we do not understand Dong Figures 5a-5h to depict the physical structure of a memory cell, but rather to depict a self-boosting mode.” ID, 22 n.6. I also note that despite this finding, the Board, based on my reading of the Board's institution decision, appears to err by relying on Dong's Figure 5a arranged “in a vertical orientation” as support for the physical arrangement of the memory. *See* ID, 24-25. As I explain in my declaration, Dong's Figure 5a (and Figure 5g) are not a representation of physical memory, and a POSITA would not interpret them as disclosing vertically arranged wordlines.

174. For independent claim 5, for example, Petitioner annotates Dong’s voltage chart in Figure 5a as shown below:



Pet. 33 (claim 5); *see id.* at 31 (Petitioner’s sole obviousness position for claim 5 to utilize a 32-cell memory string in Figure 5a).

175. For independent claims 1 and 11, Petitioner similarly annotates Dong’s voltage chart in Figure 5g:



Original Figure 5g

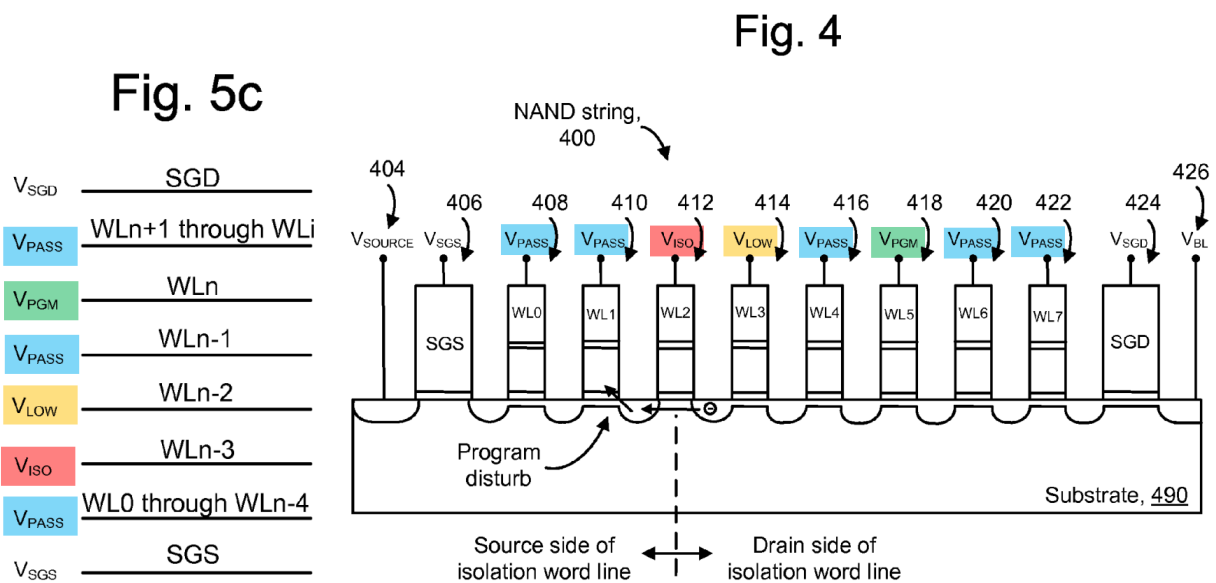
Petitioner's Annotated Figure 5g

Pet. 51 (claim 1); *see id.* at 31 (Petitioner's sole obviousness position for claim 5 regarding Figure 5a to utilize a 32-cell memory string); *id.* at 50 (Petitioner referring back to Petitioner's sole obviousness position for claim 5 at Pet. 31 to allege Dong's Fig. 5g with a 32-cell memory string reads on claim 1); *id.* at 68 (Petitioner addressing claim 11 by referring back to claim 1).

176. In my opinion, a POSITA would understand that Figures 5a and 5g, like all of Dong's voltage charts showing the voltages applied to different word lines in different "self-boosting modes," merely list in two vertical columns which voltages are applied to which word lines. Like tabulated data or box diagrams, these voltage charts do not represent the physical arrangement of any word lines in a memory, let alone word lines arranged "from bottom to top" as recited in the

independent claims of the '941 Patent. *See, e.g.*, Ex. 1005 at ¶¶20, 47, 87. Instead, a POSITA would understand that the physical arrangement of the memory of Dong is shown in Figure 4, which depicts a two-dimensional memory array with word lines arranged in a horizontal plane above the substrate. *Id.* at ¶¶45, 65.

177. As shown below, the voltages applied to wordlines in the voltage chart of Figure 5c correspond to the labeled voltage inputs in the physical memory structure shown Figure 4, which shows the wordlines physically arranged in a horizontal plane. In my opinion, this further reinforces the idea that Figure 4 is the physical memory structure, while Figures 5a-h are just depictions of which voltages are applied to different word lines in different “self-boosting modes.” *Id.* at ¶¶20, 47, 87. I have highlighted like voltages in both figures, to indicate how the arrangement of voltages in both figures match:



Ex. 1005 at Figs. 4, 5c. Ex. 1005 at Figs. 4, 5c.

178. Dong further reinforces the connection between Figures 4 and 5c by stating that in Figure 4, “a revised erased self-boosting (REASB) mode, such as depicted in Fig. 5c, is used.” Ex. 1005 at ¶45. Further, Dong states that “FIG. 5c depicts another ... self-boosting mode. ... This boosting mode is also discussed in connection with FIG. 4.” *Id.* at ¶54.

179. As highlighted in green above, V_{PGM} is applied to WL5 (418) in Figure 4, just as V_{PGM} is applied to WLn in Figure 5c (in other words, $n=5$ in Figure 5c). Ex. 1005 at ¶¶45-46, 54, Figs. 4, 5c. As another example, as highlighted in blue above, V_{PASS} is applied to WL4 (416) in Figure 4, just as V_{PASS} is applied to WLn-1 in Figure 5c. Ex. 1005 at ¶¶45-46, 54, Figs. 4, 5c.

180. Similarly, as highlighted in blue above, V_{PASS} is applied to WL6 and WL7 (420 and 422) in Figure 4, just as V_{PASS} is applied to WLn+1 through WLi in Figure 5c (in other words, $i=7$ in Figure 5c). *Id.* Further, as highlighted in orange above, V_{LOW} is applied to WL3 (414) in Figure 4, just as V_{LOW} is applied to WLn-2 in Figure 5c. *Id.* Also, as highlighted in red above, V_{ISO} is applied to WL2 (412) in Figure 4, just as V_{ISO} is applied to WLn-3 in Figure 5c. *Id.* Finally, as highlighted in blue above, V_{PASS} is applied to WL0 and WL1 (408 and 410) in Figure 4, just as V_{PASS} is applied to WL0 through WLn-4 in Figure 5c. *Id.* In other words, by setting $n=5$ and $i=7$, the voltages of Figures 4 and 5c match one-for-one. *See id.*

181. Importantly, wordlines WL4 (416) and WL5 (418), as well as all of the other wordlines, are physically arranged next to each other horizontally in the memory array, as shown in the “cross-sectional view” of the “NAND string” in Figure 4. Ex. 1005 at ¶19. The wordlines are not arranged “from bottom to top.” The column structure in Figure 5c is only a diagrammatic representation of voltages applied to the wordlines in a particular mode—not a representation of how the wordlines are arranged in the physical memory, which is instead shown in Figure 4. Ex. 1005 at ¶45, Figs. 4, 5c.

182. A POSITA would have thus understood that the voltage scheme of Figure 5c is not a physical representation of memory. Instead, Dong discloses that the voltage scheme of Figure 5c is implemented in the 2D NAND physical memory array of Figure 4, as depicted above.

183. In my opinion, the same is true of Dong’s Figures 5a and 5g relied on in the Petition. *See* Pet. 29-44 (relying on Fig. 5a for claim 5), 50-66 (relying on Fig. 5g for claim 1), 68-70 (referring back to Fig. 5g for claim 11). That is, a POSITA would understand that Figures 5a and 5g are charts of how voltages are applied to the word lines that are physically arranged horizontally, as shown in Figure 4.

184. Like Figure 5c, a POSITA would understand that Dong describes Figures 5a and 5g in the context of Figure 4’s 2D NAND string. Dong, ¶¶ 47

(“FIGS. 5a-h depict different examples of self-boosting modes.”), 52 (“FIG. 5b depicts a revised erased area self-boosting mode.”), ¶54 (“FIG. 5c depicts another revised erased area self-boosting mode.”), ¶55 (“FIG. 5d depicts another revised erased area self-boosting mode.”), ¶56 (“FIG. 5e depicts another revised erased area self-boosting mode.”), ¶58 (“FIG. 5f depicts another revised erased area self-boosting mode.”), ¶59 (“FIG. 5g depicts another revised erased area self-boosting mode.”), and ¶60 (“FIG. 5h depicts another revised erased area self-boosting mode.”). Dong relies on physical structures of Figure 4, like “substrate 490” and “word line 412,” to describe the operation of the “revised erased area self-boosting mode” (“REASB”) described in Figure 5g, confirming to a POSITA that the Figure 5 diagrams correspond to the physical arrangement of Figure 4. *Id.* ¶¶59, 65 (“With the EASB or REASB boosting modes, ... a channel area of the substrate 490 on a source-side of the isolation word line 412 is isolated from a channel area of the substrate on a drain-side of the isolation word line 412.”); *see also id.* ¶67 (recognizing a “hot carrier injection” program disturb occurring with “EASB and REASB” is depicted in Figure 4 “where the arrows depict electrons moving across the channel under the isolation storage element 412 and into the floating gate of storage element 410”), ¶65 (describing that for EASB or REASB modes, “V_{ISO} is applied to one or more source-side neighbors of the selected word line”).

185. Thus, in my opinion, a POSITA would understand that the voltage charts of Figures 5a and 5g refer to the word lines that are physically arranged in a horizontal plane above a substrate, as shown in Figure 4. *See* Ex. 1009, 52-54 (describing self-boosting schemes for 2D NAND). A POSITA would find no other conclusion is reasonable, because Figure 4's "cross-sectional view of a NAND string" is the only depiction in Dong of how its word lines are physically arranged. Ex. 1005 ¶45. In my opinion, Dong's voltage charts (i.e., Figures 5a and 5g) cannot meet the Petitioner's burden to demonstrate the existence of word lines physically arranged "from bottom to top" as claimed.

186. I also think that the Board was correct at institution when it stated that "[b]ecause we did not adopt Petitioner's proposed construction of 'from bottom to top' as meaning from source end to drain end, we disagree that Dong's method applied to a 2D memory, which has wordlines arranged horizontally from source to drain end, teaches these limitations [of claim 5]." ID, 24.

B. *Dong's Passing Reference To "Three Dimensional" Storage Does Not Disclose Or Suggest Vertically Arranged Wordlines As Claimed In The '941 Patent*

187. Beyond Dong's voltage charts (e.g., Figures 5a and 5g), Petitioner points only to a single sentence in Dong referencing three-dimensional storage—"In some embodiments, the array of storage elements can be three dimensional"—and simply assumes, without explanation, that this refers to vertically arranged

word lines. Ex. 1005 ¶95; *see* Pet. 35. But a POSITA would not view this as a reference to vertically arranged wordlines relative to a substrate. In my opinion, this cited sentence in Dong refers to those arrangement of wordlines that are 2D NAND-based, and cannot disclose the claimed invention, which requires “[a] memory” with a “first portion” having wordlines vertically arranged “from bottom to top,” a “second portion formed below the first portion” having wordlines vertically arranged “from bottom to top,” and applying specific voltages to particular wordlines. *See, e.g.*, Ex. 1001, 6:55-7:2 (cl. 1).

1. *No Anticipation*

188. In my opinion, Petitioner’s anticipation argument (Ground 1) fails because Dong’s single mention of “three dimensional” does not disclose each and every recited element of the claims of the ’941 Patent as recited. A POSITA would have understood that the reference to “three dimensional” storage is insufficient to disclose the specific three-dimensional memory as arranged in the claims, with wordlines arranged vertically “from bottom to top,” and therefore does not anticipate the claims.

189. In my opinion, Petitioner does not explain, for example, why a vague and ambiguous reference to “three dimensional” storage would necessarily have taught arranging wordlines vertically from bottom to top, rather than horizontally. A POSITA would have understood that this sole mention of “three dimensional”

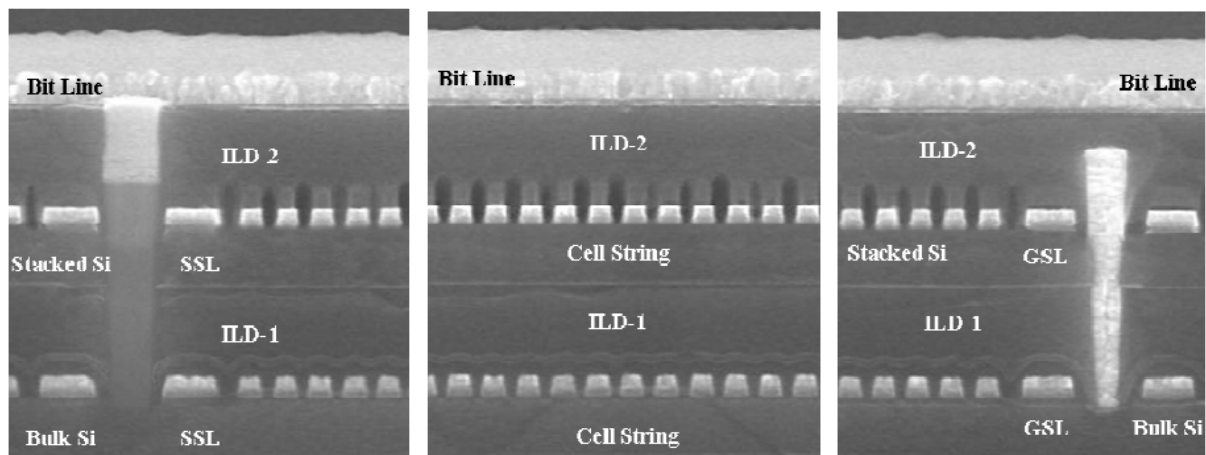
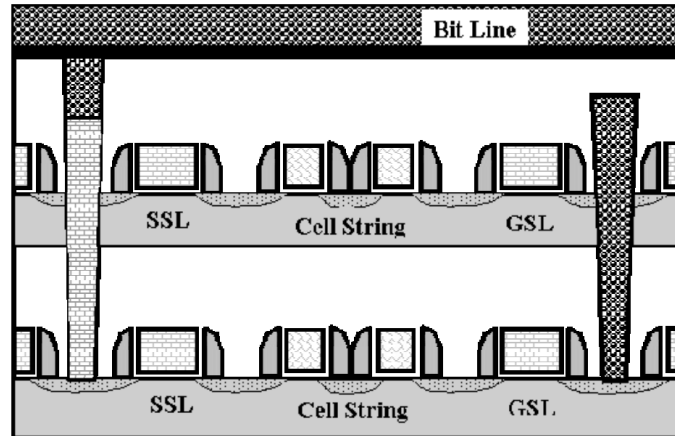
does not mean that vertically arranged wordlines as recited are necessarily present or disclosed in Dong. As I explain in the following section, a POSITA would have understand Dong's reference to "three dimensional" storage as not disclosing arranging wordlines vertically as recited.

a. *A POSITA Would Not Interpret Dong's "Three Dimensional" Disclosure To Refer To Vertically Arranged 3D NAND*

190. In my opinion, Petitioner relies on a hindsight interpretation of Dong's single mention of "three dimensional" memory to try to make it disclose the claimed vertical wordlines arranged "from bottom to top." Petitioner provides no evidence or basis for this assumption. In my opinion, a POSITA would not have understood Dong's disclosure in this manner. That is, a POSITA would not have understood Dong's mention of "three dimensional" to disclose the specific memory structure with wordlines arranged vertically "from bottom to top" as recited.

191. In my opinion, a POSITA would have interpreted Dong's mention of "three dimensional" memory arrays as naturally referring to 3D memory arrays that were known as of Dong's May 7, 2007 date, like Stacked and Multi-layer TFT 3D NAND that did not have vertically arranged wordlines as recited. Those three dimensional memory arrays had stacked layers of *horizontal* 2D NAND arrays,

with wordlines arranged *horizontally* as shown below (as in Dong), not arranged vertically “from bottom to top” as recited.



Ex. 2008, 3, Figs. 3, 4; Ex. 2009, 4.

192. It is also notable that Petitioner provided no evidence or support that Dong’s disclosure of “three dimensional” would be interpreted by a POSITA to disclose the vertical 3D NAND implementation over the non-vertical arrangements like Stacked and Multi-layer TFT NAND.

193. In my opinion, a POSITA would interpret Dong's mention of "three dimensional" as applying to 3D memory arrays to which Dong's 2D NAND voltage schemes (e.g., Figures 5a and 5g) are applicable like Stacked and Multi-layer TFT NAND, which include multiple layers of 2D NAND.

194. Moreover, in my opinion, Dong's single reference to a "three dimensional" array of storage elements does not provide enough information for a POSITA to make and use a three dimensional memory as claimed with wordlines arranged vertically "from bottom to top." A POSITA, in my opinion, would require an excessive and unreasonable amount of experimentation, including much trial and error, to make and use a vertically arranged 3D NAND memory as claimed based on Dong's two word mention of "three dimensional." For example, a POSITA would have understood that designing a 3D NAND memory was very complicated—indeed initial 3D cells did not effectively decrease bit cost due to complications in fabrication, process steps, and large unit cell size. Ex. 1009, 292-294.

195. A POSITA would also not understand Dong's disclosure of "three dimensional" to refer to vertically arranged 3D NAND because a POSITA would not apply Dong's 2D self-boosting voltage schemes to 3D NAND. *See infra* Section VII.B.2.c

2. *No Obviousness*

a. *Petitioner Did Not Argue That A POSITA Would Apply Dong's 2D Program Disturb Method In 3D NAND*

196. It is important to note, in my opinion, that Petitioner *never argued in its Petition* that it would be obvious to apply Dong's voltage schemes of Figures 5a and 5g in a 3D NAND context.

197. Despite that fact, in my opinion, upon reading the papers in this proceeding, the Board appeared to raise a new position that is not disclosed in the Petition: "We understand the Petition to assert that a POSITA would have understood Dong's method could be applied to a 3D NAND memory device having vertically oriented wordlines." ID, 25. In my opinion, Petitioner and Dr. Liu made no such argument that I can find.

198. In my opinion, Petitioner also *did not argue* that it would have been obvious to modify Dong's horizontally arranged wordlines into the vertically arranged wordlines as recited. Petitioner instead relied on Dong's disclosure, stating:

Regardless, to the extent bottom to top is interpreted to require vertical strings in a 3D NAND memory, *Dong discloses* its "array of storage elements can be three dimensional" and shows Fig. 5a in a vertical orientation which satisfies the claim. Dong, [0095]; Liu, ¶ 120.

Pet. 35. And as discussed, Dong's sole mention of "three dimensional" does not disclose vertical wordlines. *See supra* Section VII.B.

199. In my opinion, while Petitioner does use obviousness to modify Dong in one instance, that modification has nothing to do with the claim requirement that wordlines are arranged “from bottom to top.” Pet. 30-31. Instead, that sole obviousness modification attempts to extend Dong’s disclosure to include a 32-cell memory string. Petitioner states that “it would have been obvious to a POSITA to utilize a 32-cell memory string,” argues doing so was “well-known to POSITAs,” and provides three reasons why a POSITA would “utilize a 32-cell memory string.” Pet. 31; *see* Liu, ¶¶109-110. In my opinion, with respect to the claim limitation “from bottom to top,” Petitioner’s Grounds 1 and 2 are identical and fail for the same reason—there is no teaching of wordlines arranged from “bottom to top” in Dong. And as explained above in Section VII.B, a POSITA would not have interpreted Dong’s mention of “three dimensional” as disclosing vertical 3D NAND.

200. In my opinion, because Petitioner never raised an obviousness argument for the claim limitation “from bottom to top” in its Petition, no such theory is available to the Petitioner or the Board in this proceeding.

**b. *Conclusory Expert Testimony Does Not Remedy
Petitioner’s Fatal Flaw***

201. Petitioner’s expert Dr. Liu provides no explanation or support for his statement that “given the similarities between 2D and 3D NAND discussed in the Technology Background section, even a 2D memory string would at a minimum

render obvious the *bottom to top* requirement, even if narrowly construed.” Liu, ¶120. Dr. Liu also fails to provide any sufficient motivation to combine or explanation as to a reasonable expectation of success regarding this statement. In my opinion, even if Dr. Liu’s conclusory testimony in his declaration could be considered (which I understand it should not be considered because this argument is not in the Petition), it does not help Petitioner. *Compare* Pet. 35, *with* Liu, ¶120.

202. In my opinion, neither Petitioner, nor its expert Dr. Liu, rely on the Technology Background section to support the idea (not present in the Petition) that a POSITA would have been motivated to modify Dong’s specific program disturb mechanism to apply to 3D NAND. See ID, 25. Instead, in my opinion, a POSITA would understand Petitioner’s Background section as merely describing the generic development from 2D NAND to 3D NAND, stating “there are many similarities between 2D and 3D NAND flash memory devices.” Pet. 14.

203. I have reviewed Petitioner’s actual Grounds alleging unpatentability (Pet. 28-84) in detail, and Petitioner does not refer to Petitioner’s Technology Background section to support an obvious modification to apply Dong’s voltage schemes to 3D NAND. Petitioner also does not rely on mentioned “similarities” between 2D NAND and 3D NAND to support an articulated rationale to apply Dong’s 2D NAND program disturb schemes in a 3D NAND context. And even if they did, in my opinion, a mere statement that 2D NAND and 3D NAND are

similar is not a sufficient motivation to apply Dong's 2D NAND program disturb schemes of Figures 5a and 5g in a 3D NAND context. Nor is a statement that 2D NAND and 3D NAND are similar, as Petitioner presents, an articulated rationale as to why a POSITA would modify Dong to arrive at the claimed invention absent hindsight.

204. In fact, Petitioner's Background section describing the generic development from 2D NAND to 3D NAND is not unique to this IPR—it is mere boilerplate inserted into numerous other Micron Petitions. *Compare* Pet. 11-14, with, e.g., IPR2025-00189, Paper 1 at 14-17; IPR2025-00035, Paper 1 at 13-15; IPR2025-00117, Paper 1 at 15-17; IPR2025-00228, Paper 1 at 16-17; IPR2025-00294, Paper 1 at 12-13; and IPR2025-00245, Paper 1 at 14-15.

205. In my opinion, as I understand it from discussions with counsel, it is improper to incorporate an obviousness argument not made in the Petition by citing to an expert's declaration. That is exactly the case here, given that Dr. Liu's following statement is nowhere in the Petition: "given the similarities between 2D and 3D NAND discussed in the Technology Background section, even a 2D memory string would at a minimum render obvious the *bottom to top* requirement, even if narrowly construed." Liu, ¶120.

206. In my opinion, even if Petitioner had relied on Dr. Liu's conclusory testimony (it did not), the Petition is still fatally flawed because it offers no

rationale or articulation as to how or why a POSITA would have been motivated to modify Dong's voltage schemes in Figures 5a and 5g to apply to the claimed vertically arranged 3D NAND, let alone have had a reasonable expectation of success in doing so. In my opinion, Petitioner fails to explain why a POSITA would have combined elements from Dong (such as Figures 5a and 5g) with 3D NAND to meet the claims of the '941 Patent. Moreover, a POSITA would not be motivated to apply Dong's 2D voltage schemes (Figures 5a and 5g) to 3D NAND because 2D and 3D NAND are very different both structurally and electrically, so their disturbs are very different as a result (*see infra* Section VII.B.2.c).

**c. *A POSITA Would Not Apply Dong's 2D NAND
Program Disturb Method In A 3D NAND Context***

207. In my opinion, Dong's 2D NAND isolation voltage scheme is a planar solution that a POSITA would not apply in vertical 3D NAND with word lines arranged from top to bottom as recited as of the priority date of the '941 Patent.

208. As Petitioner's exhibit recognizes: "The program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed." Ex. 1009, 354; *see id.*, 356 ("The program disturb conditions and characteristics of 3D cells are greatly changed from that of 2D cells."), 362 ("Program disturb phenomena and mechanisms of a 3D NAND cell are much different from that of a 2D NAND cell."). A POSITA would understand that "3D NAND flash memory has a

different structure from 2D NAND flash memory, so new phenomena occur.” Ex. 2024, 1. I have described the structural and fabrication differences between 2D NAND flash and 3D NAND flash, along with the resulting implications on program disturb modes, in Section VI.A, *supra*.

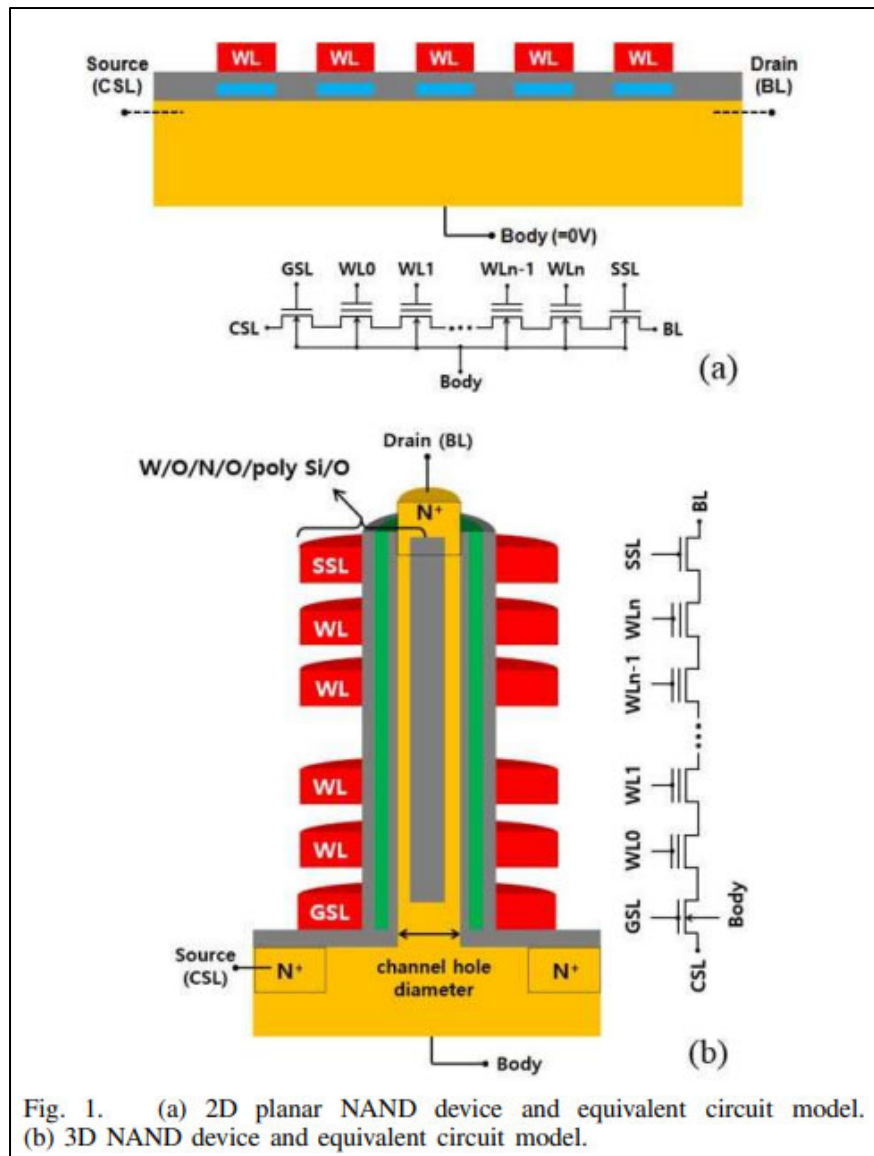
209. A POSITA would not have been motivated to apply Dong’s program disturb methods for 2D NAND cells to vertical 3D NAND cells at least because vertical 3D NAND cells have vertically stacked cells that exhibit more complex disturb mechanisms that can lead to increased errors during programming. Ex. 1009 pt. 2 at 354 (recognizing “[t]he program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed”), 356 (“The program disturb conditions and characteristics of 3D cells are greatly changed from that of 2D cells.”), 362 (“Program disturb phenomena and mechanisms of a 3D NAND cell are much different from that of a 2D NAND cell.”).

210. As I described in Section VI.A, in 2D NAND, program disturb primarily occurs along the wordline (X disturb). When high voltage is applied to a selected wordline to program a cell, the voltage is capacitively coupled via the selected wordline and the channels of the unselected (inhibited) cells on the same wordline. If this coupled voltage is not high, it can cause electrons to be unintentionally injected into the floating gates of these neighboring cells, altering

their threshold voltage and resulting in a program disturb. To mitigate program disturb in 2D NAND, voltages are applied to the wordlines and bitlines in the planar arrangement to shield the unselected cells from the unintended V_t shifts.

211. A POSITA would be aware of the differences between 2D and 3D NAND flash program disturb due to differences in circuit structure and topology, and also due to electrical properties of the channel which arise from manufacturing differences between 2D and 3D NAND flash. These differences were described supra in Section VI.A.

212. A POSITA would have understood that vertically arranged 3D NAND experiences different electrical phenomena that are not addressed by Dong's program disturb methods designed for 2D NAND. Vertical 3D NAND strings have floating bodies, i.e., the channel is not directly connected to a substrate like a 2D NAND planar string. For example, as seen in the below comparison between 2D and 3D NAND structures and circuit models, each floating gate in 2D NAND structure is connected to the body (i.e., substrate).



Ex. 2025, 1, Fig. 1.

213. A POSITA would have understood that the memory cells of the 3D NAND arrangement are on an ultra-thin body structure instead of a traditional substrate. Ex. 2025, 1, Fig. 1; Ex. 2026, 1 (“The structure of 3D NAND flash memory is based on an ultra-thin body (UTB) structure in which the channel of the

main cell is not connected to the body, and body bias is not applicable to the channel of the main cell.”). As a result, “body bias cannot be applied to the channels of main cells during read and program operations.” Ex. 2025, 1. That is, unselected channels (i.e., inhibited channels) in the 3D NAND structure “can easily be in the floating state [(i.e., it has a high impedance)], because its channel is not directly connected to its body.” *Id.*; Ex. 2027, 1; Ex. 2024, 1.

214. Moreover, a POSITA would have understood that “during program operation, the inhibited channel becomes a floating node and the **natural local self-boosting (NLSB)** effect occurs.” Ex. 2024, 1; Ex. 2027, 1; Ex. 2026, 1 (“This can cause the channel to float, resulting in the down coupling phenomenon (DCP) and natural local self-boosting (NLSB) phenomena.”). NLSB localizes channel boosting for inhibited channels near the selected wordline rather than uniformly along the string. Ex. 2024, 1. A POSITA would have understood that this means that when the selected wordline is driven with V_{PGM} , the inhibited channel is locally boosted to a high voltage near the selected wordline, due to the ultra-thin body (floating) which results in a significantly reduced program disturb.

215. A POSITA would have also understood that this NLSB effect in 3D NAND prevents program disturb of inhibited strings without 2D NAND self-boosting techniques (which are required in 2D NAND due to the fact that the entire channel is fabricated on a substrate). In 3D NAND, boosting occurs naturally due

to the vertical 3D NAND structure and the NLSB effect caused by the high-impedance ultra-thin body (i.e., substrate). In other words, “the selected WL cell is *localized automatically* during the program pulse application.” Ex. 2024, 1. A POSITA would understand that “[t]he NLSB effect does not require the local boosting scheme used in conventional 2D NAND, because it can achieve a sufficiently high potential even if the number of stacks is increased.” Ex. 2027, 1. In other words, “[t]he NLSB effect allows a sufficiently high boosted potential of an inhibited string to be achieved *without* a local self-boosted program-inhibit (SBPI) scheme” that includes an isolation wordline to isolate the selected wordline. See Ex. 2024, 1, Fig. 1; *id.*, 2, Fig. 3.

216. In my opinion, a POSITA would not have been motivated to apply Dong’s local self-boosting methods shown in Figures 5a and 5g—which both include an isolation voltage applied to specific wordlines—to a vertical 3D NAND context as of the priority date of the ’941 Patent. Put simply, since NLSB occurs without any local-boosting tricks, a POSITA would not have been motivated to look to Dong to try to solve any problem in vertical 3D NAND. Ex. 2024, 3, Fig. 3.

217. In Dong’s 2D NAND architecture, the local self-boosting method of Figures 5a and 5g drives an isolation voltage (V_{ISO}) to a source side wordline to mitigate program disturb. See, e.g., Ex. 2024 (Kang) at 1, Fig. 1 (showing local

self-boosted program-inhibit (SBPI) scheme with isolation voltage); Ex. 1009, 52-54, Fig. 2.23 (depicting local-self boosting and EASB schemes applying isolation voltage). Since the isolation voltage is low, it localizes a voltage boost on the drain side of the selected cell (raising it higher), reducing program disturb for those cells on the drain side of the selected cell. *See, e.g.*, Lutze (Ex. 1015), 3:65-4:1 (“Both LSB and EASB attempt to isolate the channel of previously programmed cells from the channel of the cell being inhibited.”)

218. A POSITA would also have not been motivated to implement an isolation voltage (i.e., applying V_{ISO}) in 3D NAND (as done in Dong and in Exhibit 2024’s Figure 1b) because such a measure would be counterproductive during a program operation. In vertical 3D NAND, V_{PASS} is driven to unselected wordlines (Ex. 2024, 3), boosting the high-impedance channel voltage of inhibited strings, and reducing program disturb. However, if an isolation voltage was applied to an unselected wordline (as suggested in Dong’s Figure 5a, and also illustrated in Exhibit 2024’s Figure 1b), a reduced voltage is coupled to the high-impedance channel, which reduces the boost voltage, and worsens program disturb.

219. Moreover, when the potential difference between the selected wordline (receiving V_{PGM}) and its neighbor (receiving V_{ISO}) increases, a larger voltage is impressed across the channel, and hot carrier injection occurs, which causes program disturb. *See* Ex. 2027, 1 (“When the channel potential of the WL

selected by the NLSB is increased, a large difference is generated in the channel potential of the adjacent WL, which results in a HCI phenomenon.”). A POSITA would therefore avoid applying V_{ISO} to wordlines near the selected wordline (receiving V_{PGM}) in vertical 3D NAND. As a result, a POSITA would not have been motivated to apply Dong’s voltage schemes of Figures 5a and 5g in a 3D NAND context. I note that, as I mentioned above, the argument to apply Dong’s voltage schemes of Figures 5a and 5g in a 3D NAND context is not in the Petition nor Dr. Liu’s declaration.

220. A POSITA would further understand that the NLSB phenomenon is unique to 3D NAND. A POSITA would also understand that local self-boosting and erase area self-boosting (EASB) schemes (i.e., those that apply little to no voltage to a wordline adjacent to the programming wordline) are limited to 2D NAND. *See* Ex. 2027, 1 (“The NLSB effect does not require the local boosting scheme used in conventional 2D NAND.”); Ex. 2024 at 3; Ex. 1009, 52-54 (showing local self-boosting and EASB schemes with applied isolation voltages). To address program disturbance in 3D NAND, a POSITA would have understood that other methods are used, including “(1) high V_t of DSL, (2) applying negative bias to DSL, and (3) inserting dummy wordlines between DSL and edge wordline.” Ex. 1009, 363-64.

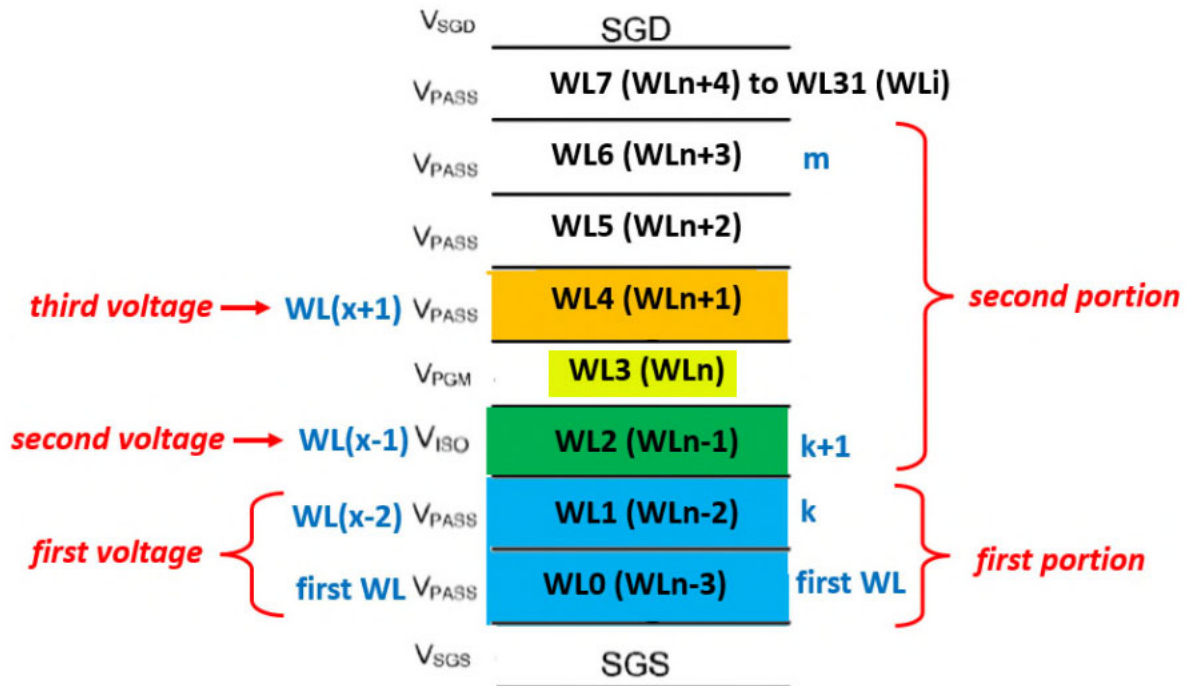
VIII. Ground 3: Dong In View Of Costa Fails To Render Obvious Claims 8-9**A. *Dong And Costa Fail To Render Obvious Wherein “The First Voltage Has A First Level If The Xth Wordline Is In The First Portion.”***

221. In my opinion, Petitioner’s application of Dong to independent claim 5 fails when carried forward to address claims 8 and 9. In other words, for example, Petitioner’s position for claim 5 places the xth wordline in the “second portion,” but claims 8 and 9 require the xth wordline to be in the “first portion.”

222. Claim 8 depends from claim 7, which depends from claim 5. Claim 9 also depends from claim 5. Claims 8 and 9 both recite wherein “the first voltage has a first level if the xth wordline is in the *first portion*.” Claim 5, from which claims 8 and 9 depend, defines “a *first portion*” as “comprising a first wordline to a kth wordline from bottom to top.” Claim 5 also requires an “xth wordline,” defining “x” as positive integer wherein “ $3 \leq x$.”

223. For claim 5, Petitioner maps the recited “first portion” to the first two wordlines shown in Dong’s Figure 5a—defining “WL0 (WL_{n-3})” as the “first WL” and “WL1 (WL_{n-2})” as the “kth wordline” (both in blue highlight below):

Fig. 5a



Pet. 33 (yellow highlighting added); *see also id.*, 36-37. Petitioner also argues the “claimed *xth* wordline corresponds to the selected wordline WLn in Dong Fig. 5” (Pet. 38), which is highlighted in yellow above. Pet. 33. As seen above, Petitioner depicts the *xth* wordline in the “second portion.” Pet. 33.

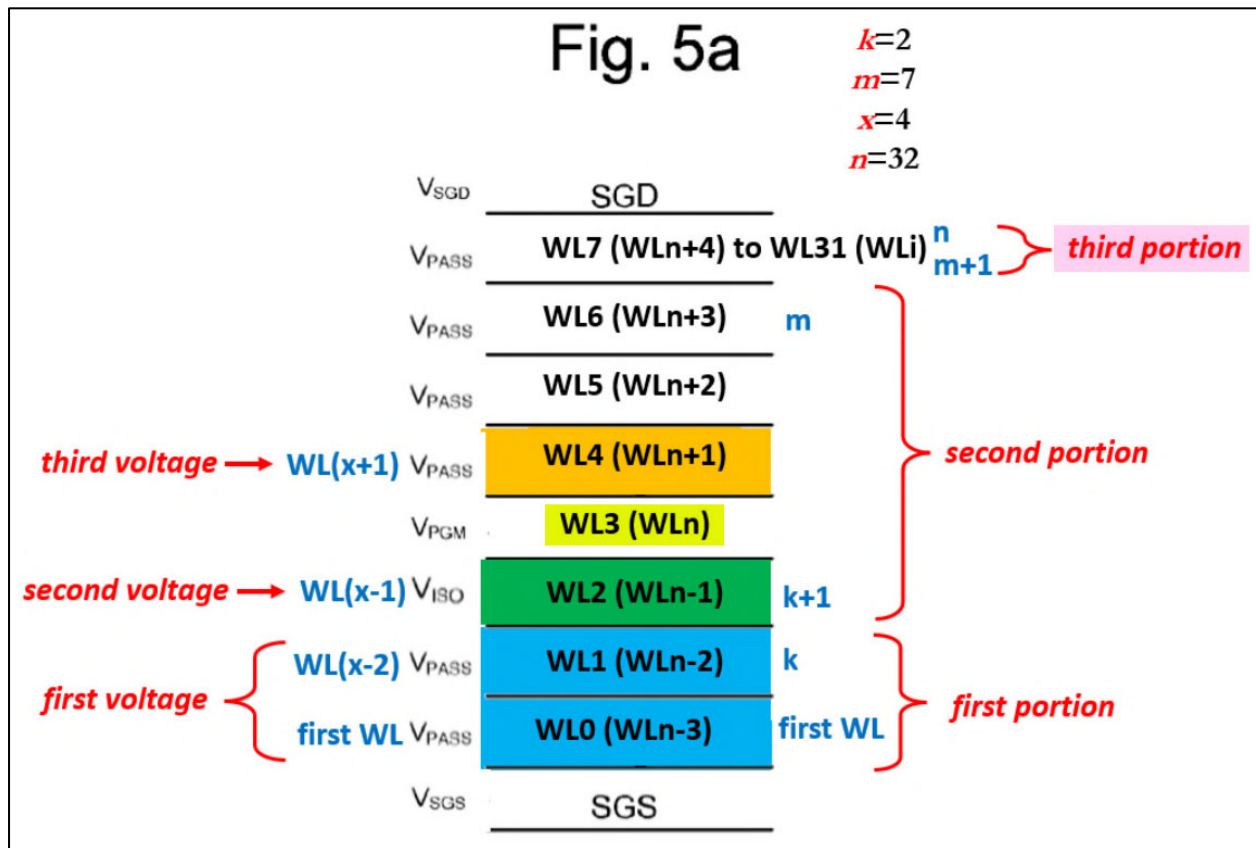
224. Petitioner assigns to “*x*” a value of “4,” which means the *xth* wordline is the 4th wordline from SGS (i.e., “WL3 (WLn)” in yellow highlight above), to meet the additional requirement of claim 5 that “*x*” is a positive integer wherein “ $3 \leq x$.” Pet. 33; *see also id.*, 43-44.

$k = 2$	$WL(m) = WL6$	$WL(x+1) = WL(n+1) = WL4$
$m = 7$	$WL(k+1) = WL2$	$WL(x) = WL(n) = WL3$
$x = 4$	$WL(k) = WL1$	$WL(x-1) = WL(n-1) = WL2$
	$first\ wordline = WL0$	$WL(x-2) = WL(n-2) = WL1$

Pet. 33; *see also id.*, 43-44. As shown above, the fourth wordline is in the “second portion.”

225. In my opinion, Petitioner’s arguments fail for claims 8 and 9 because these claims require the xth wordline to be in the “*first portion*,” which is impossible given Petitioner’s positions for claim 5. Specifically, both claims 8 and 9 recite that “the first voltage has a first level *if the xth wordline is in the first portion*.” Petitioner’s arguments for claim 5 ensure the xth wordline will *never* be in the first portion. As described above, Petitioner defined the “first portion” as the first two wordlines (WL0 and WL1) and defined “x” as 4. Pet. 33. To be in the “first portion” as Petitioner defines it and as required by claims 8 and 9, the xth wordline would need to be one of the first two wordlines. But the xth wordline cannot be in Petitioner’s “first portion,” as required by claims 8 and 9, because “x” cannot be less than 3, as required by claim 5. In my opinion, Petitioner and its expert provide no basis for how the xth wordline can be in the recited “first portion.”

226. Petitioner similarly fails to show how Dong and Costa meet the limitation of claim 8 that requires the “xth wordline” to be “in the third portion,” which is “formed above the second portion.” Ex. 1001, cls. 7-8. Petitioner defines the “third portion” (highlighted below in pink) as extending from “an (m+1)th wordline [WL7] to an nth wordline [WL31] from bottom to top.” Pet. 47.



Pet. 46-47. Petitioner also defined “x” as 4, placing the xth wordline at WL3 (highlighted in yellow) in the “second portion.” *Id.*, 43, 49. To be in the “third portion” as Petitioner defines it, the xth wordline would need to be within the range of WL7 to WL31. As with the above example regarding “a first portion,” Petitioner

and its expert fail to show or explain how the *xth* wordline can be in the recited “third portion,” despite recognizing claim 8 requires that “the wordline used for programming (*i.e.*, the *xth wordline*) moves up the memory string from the *first portion* to the *second portion*, to the *third portion*.” See Pet. 74; Liu, ¶214.

227. In my opinion, that Costa does not resolve these deficiencies because Petitioner relies on Dong to disclose the recited positioning of the *xth* wordline relies, not Costa. See Pet. 74 (“Dong satisfies the underlying elements of claims 5 and 7.”); *id.*, 75-77.

B. *Dong And Costa Fail To Disclose “Applying A First Voltage” In Recited Portions During “A Program Operation”*

228. Petitioner argues that Dong combined with Costa renders obvious claims 8-9. Pet. 70. But Petitioner admits that “Dong is silent” on these claims (Pet. 2), including “regarding how V_{PASS} (and other programming voltage values) change as the cell being programmed advances from the source end of a memory string to the drain end.” Pet. 72; *see also* Liu, ¶215. In my opinion, Costa does not disclose the missing limitations. But even if it did, a POSITA would not have been motivated to combine Dong with Costa as Petitioner suggests.

229. Petitioner alleges for claims 8 and 9 that the “claimed V_1 voltage (*viz.*, Dong’s V_{PASS} voltage)” is modified by Costa such that it is “applied to the previously programmed cells in a memory string” and increases “as the cell being

programmed moves” upward from the first portion to the third portion. Pet. 76-77; Liu, ¶¶220-221.

230. But during Dr. Liu’s deposition, Dr. Liu changed his position regarding how Dong and Costa are applied to claims 8 and 9. Rather than modifying “Dong’s V_{PASS} voltage” as set forth in the Petition (Pet. 76-77; Liu, ¶¶220-221), Dr. Liu testified that Dong and Costa are combined as *two separate processes*: Dong discloses applying a program voltage to transfer charge to change a cell’s threshold voltage and Costa discloses a subsequent verification phase. Liu Dep., 159:17-161:18, 152:20-155:13; *see also id.*, 158:2-20. As with Dr. Liu’s new claim construction position regarding “a program operation,” this new position is improper and was not disclosed in his declaration or the Petition.

1. *Dong And Costa Fail To Disclose “Applying A First Voltage” In Recited Portions During “A Program Operation” Under Patent Owner’s Correct Interpretation*

231. I understand that the claims require that “a first voltage” is applied during a program operation. Claim 5, from which claims 8 and 9 depend, requires a “program method of a memory ... comprising: *applying a first voltage* to the first wordline to an (x-2)th wordline *when an xth wordline is used to perform a program operation.*” Ex. 1001, cl. 5. Claims 8 and 9 further recite that “*the first voltage*” has a specific level depending on whether the xth wordline is in the first, second or third portion. In my opinion, a POSITA would understand that these

claims do not focus on a verify phase but instead recite “applying a first voltage” *during* a distinct program operation (i.e., an operation performed by applying a program voltage to a selected wordline to program a selected memory cell). *See* Pet. 38-39; *see supra* Section VI.F.3.

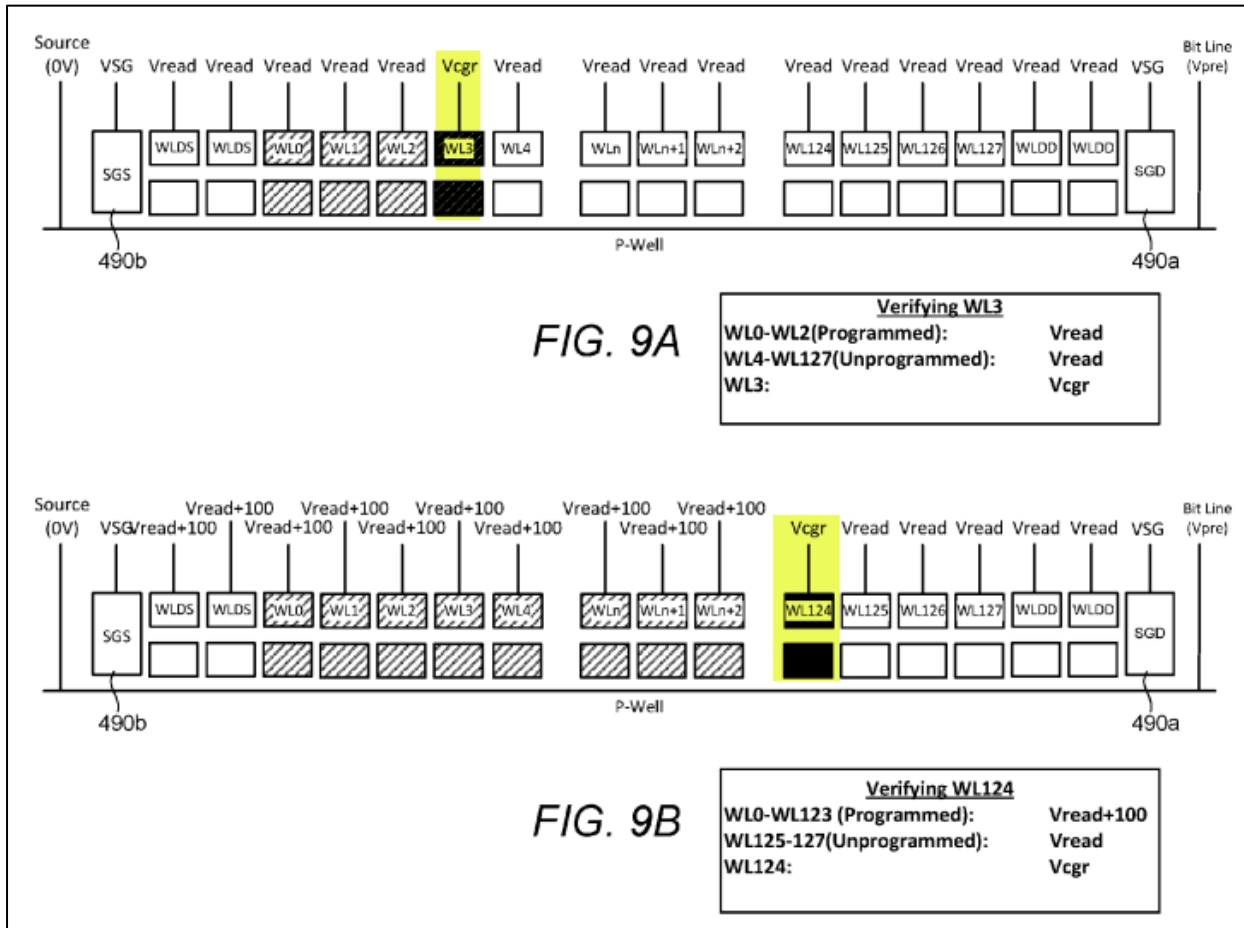
232. In my opinion, Costa does not disclose “applying a first voltage” *during a program operation* as claimed because Costa describes applying read voltages *during a verify operation*. Petitioner implies that Costa discloses “a variable pass voltage” during a program operation (Pet. 72-73, 75; Liu, ¶¶210, 212, 217). In my opinion, Petitioner appears to misrepresent Costa by stating it “specifically discloses that V_{PASS} increases (for wordlines below the cell being programmed) as programming proceeds up the memory string.” Pet. 74. Costa does not disclose or mention a “ V_{PASS} .” Instead, Costa discloses a read/verify waveform and adjusting read/verify pass voltage (e.g., V_{read})—*after* “a program operation.” *See e.g.*, Costa, ¶31 (“[T]he pass voltage applied *when reading* the earlier programmed memory cells is higher relative to the pass voltage applied *when reading* the later programmed memory cells.”), ¶29 (“The disclosed technology is directed to reducing errors *when sensing* in non-volatile memory... During sensing ... the remaining memory cells receive a read or verify pass voltage.”). A POSITA would therefore understand Costa’s mention of “pass voltage” as referring to a “read or verify pass voltage,” not a “pass voltage” used

on inhibited strings during a program operation (i.e., simultaneously with application of a program voltage on the selected wordline).

233. In my opinion, to put it in other words, Costa's "variable pass voltage" is a variable read/verify pass voltage applied to "cells that have already been subject to programming," not a variable program V_{PASS} . Costa, ¶¶32-33 (describing use of "**the** variable pass voltage" in reference to read voltage applied to "unselected memory cells that have already been subjected to programming"), ¶28 (describing that Costa is "directed to reducing errors *when sensing* in non-volatile memory," and that "[d]uring sensing ... the remaining memory cells receive a read or verify pass voltage"), Figs. 8-10 (depicting application of pass voltage V_{read}); *see also id.*, ¶¶96, 104, 110-111, 114-116; Liu, ¶¶90-91. As Dr. Liu previously testified about this Costa reference: "Costa teaches adjusting voltages for verify operations *alone*." Ex. 2023, ¶72; *see also* Pet. 71 (Costa "focuses on addressing program disturb impacts arising from the verification phase."); Ex. 2022, ¶248 ("Costa discloses using its read operations to verify programming."). In short, neither Dong nor Costa teach the limitations of these claims.

234. In my opinion, Petitioner's error is reflected in its reliance on Costa's "simple example," which focuses on the verification/read process. *See* Pet. 75-76 (citing Costa, ¶115 which refers to Figures 9A and 9B); Costa, ¶105 (describing

Figures 9A and 9B as depicting “variable bias conditions for a program verification operation”). As shown below in Figures 9A and 9B, a “read reference voltage” (V_{cgr} highlighted in yellow below) is “used during a sense operation.” Costa, ¶98.



Costa, Figs. 9A-9B.

235. Costa discloses applying a read pass voltage (V_{read}) when “**verifying** a wordline such as wordline WL3 in a lower or earlier programmed zone” (Figure 9A) and another read pass voltage ($V_{read}+100$) when “**verifying** a wordline such as wordline WL124 in an upper or later programmed zone” (Figure 9B). Costa,

¶¶114-115; *see also id.*, ¶¶107, 110, 115 (“When verifying a selected wordline in the first zone (e.g., WL3), a lower read pass voltage (e.g., Vread-100) is applied to a subset of unselected wordlines on the *already programmed* (source) side of the selected wordline.”). *Applying a read pass voltage during a verification process is not “applying a first voltage” during “a program operation” as claimed.*

a. *A POSITA Would Not Have Been Motivated To Modify Dong’s Programming Waveform*

236. In my opinion, Petitioner provides no articulated rationale to explain how or why a POSITA would modify Dong as Petitioner proposes:

Taking each claimed portion in Dong as one of Costa’s “zones,” the claimed V1 voltage (viz., Dong’s V_{PASS} voltage) applied to the previously programmed cells in a memory string will increase as the cell being programmed moves from the first portion (first zone) to the second portion (second zone), and from the second portion (second zone) to the third portion (third zone).

Pet. 76. Instead, without a specific motivation as required, Petitioner’s modification of Dong is inspired purely by hindsight.

237. In other words, when addressing claims 8 and 9, Petitioner provides no motivation to modify Dong such that Dong’s V_{PASS} voltage (i.e., Petitioner’s “first voltage,” Pet. 41) increases as programming advances up the memory string. *See* Pet. 76. Instead, Petitioner states that “[t]he reasons for combining Dong and Costa are discussed in §XI.A” (i.e., Pet. 70-74). Pet. 74. But Petitioner’s high-level, generic motivation in the referenced §XI.A (Pet. 70-74) fails to explain why

a POSITA would have combined elements from Dong and Costa to meet the claimed invention. In my opinion, Petitioner provides an *entirely different combination* of Dong and Costa in §XI.A, whereby Dong provides the program phase and Costa provides the verify phase. Petitioner describes how Dong focuses on “program disturb ... from ... the actual programming pulse,” while Costa focuses on “disturb impacts arising from the verification phase.” Pet. 71.

238. Moreover, in my opinion, even though Petitioner argues that Dong “lend[s] itself to Costa’s ‘variable pass voltage’ technique” (Pet. 71-72), a POSITA would not have been motivated to modify Dong’s program disturb schemes designed for a *program* phase when considering Costa’s disclosure of a *verify* phase. Pet. 73. In other words, a POSITA would not have been motivated to modify Dong’s V_{PASS} voltage (Petitioner’s “first voltage”) as Petitioner suggests when addressing claims 8-9 (Pet. 76), because Costa’s disclosure is focused on the verification/read operation of wordlines already programmed—not the program operation as recited.

239. **First**, as Petitioner admits, Dong and Costa address “two different ... phenomena.” A POSITA would have understood that Dong addresses program disturb during programming and Costa addresses verification of cells already programmed. Pet. 71-72. A POSITA would also have known that program disturb occurs during programming of cells, not during read or verification. *See* Pet. 1, 15,

23. In my opinion, a POSITA would not modify the program disturb method disclosed in Dong with the read or verification method of Costa because both describe different voltage applications for distinct purposes. In my opinion, neither Dong nor Costa disclose the recited limitation of “a first voltage” that increases as programming advances up the memory string during a program operation. *See* Pet. 76.

240. **Second**, Petitioner alleges that a POSITA would “investigate and apply techniques (like Costa’s) to address *program disturb/errors* that occur as function of the location of a cell being programmed within a memory string” because “Dong describes a program disturb issue that occurs as programming advances along a memory string.” Pet. 73 (citing Dong, ¶11); Liu, ¶¶211-212. But, in my opinion, this statement refers to Petitioner’s generic motivation regarding joining the “mutually compatible” program and verify phase disclosures of Dong and Costa respectively (Pet. 73), not modifying Dong’s “first voltage” as programming progresses (*see* Pet. 76 where Petitioner actually addresses claims 8-9). A POSITA would understand that Costa does not address program disturb errors because, as I explained, Costa discloses errors during a verify operation.

241. As described above, a POSITA would have understood that Costa addresses a read/verification issue regarding increased channel resistance for programmed cells (i.e., “back-pattern effect”)—not program disturb. Pet. 25-26;

see Liu, ¶¶82, 89, 209. Petitioner provides no rationale as to why Costa's disclosure regarding a verify phase would apply to Dong's program phase, much less that there would be a reasonable expectation of success in doing so.

242. **Third**, in my opinion Petitioner's combination of Dong and Costa is purely based on hindsight. Nothing in Dong or Costa teaches increasing a pass voltage for wordlines below the cell being programmed during the program phase, much less that this reduces program disturb or errors as programming advances along a memory string.

2. *Dong And Costa Fail To Disclose “Applying A First Voltage” In Recited Portions During “A Program Operation” Under Petitioner’s Incorrect Interpretation*

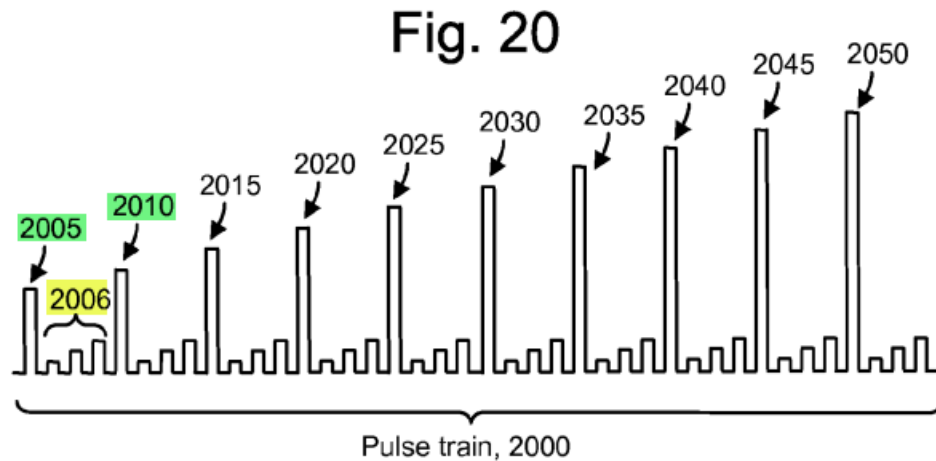
243. In my opinion, Petitioner's position also fails under Dr. Liu's new interpretation of “a program operation” (as including both a programming phase and a verify phase). This new interpretation does nothing to address the fatal flaws raised in the previous section. *See supra* Section VIII.B.1. Under this new interpretation, Petitioner still applies Dong's V_{PASS} —used in a program phase—as the “**first voltage**.” Pet. 38-39. Even if Petitioner added Costa's verify disclosure after Dong's program disclosure to address claims 8 and 9 (Petitioner did not as seen at Pet. 76), Petitioner still fails to meet claims 8 and 9 which require “**the first voltage**” (i.e., Dong's V_{PASS}) to increase as the selected wordline moves up the memory string. Neither Costa nor Dong disclose that limitation. And a POSITA

would not modify Dong according to Costa for the reasons explained above. *Supra* Section VIII.B.1.a.

a. *A POSITA Would Not Have Been Motivated To Supplement Dong's Programming Process With Costa's Verification Process*

244. Petitioner's motivation to combine Dong and Costa (Pet. 70-74) focuses on supplementing Dong's programming process with Costa's verification process: "[c]ombining both teachings would address memory cell errors introduced during *both* phases of the program operation (*viz.*, the *programming* pulse and the *verification* pulse)." Pet. 73; *see id.*, 71 ("Dong and Costa focus on two different (but complementary) phenomena that impact memory device reliability during programming."); Liu, ¶211 (describing a POSITA would have been motivated "to employ Costa's technique with Dong"); *id.*, ¶¶212-213.

245. In my opinion, a POSITA would not have been motivated to combine Dong and Costa as Petitioner proposes because Dong already discloses a verification operation separate from its programming operation, which Petitioner did not address. Dong discloses that "[i]n between the program pulses are verify pulses" as seen in verify pulse set 2006 (yellow) between program pulses 2005 and 2010 (green).



Dong, ¶132, Fig. 20. Dong discloses how boost voltages “are applied to wordlines to implement a boost mode are applied *when* programming occurs, e.g., prior to and during a program pulse,” but that “during the verify process, ... the boost voltages are not applied.” Dong, ¶133. Dong discloses that during verification, “read voltages, which are typically less than the boost voltages, are applied to the unselected wordlines.” *Id.*; see also *id.*, ¶¶9, 50, 71.

246. I recognize that Petitioner’s expert Dr. Liu argues that a POSITA would have been motivated by the fact that “Dong says nothing about increased channel resistance or how to address it.” Liu, ¶211. But, in my opinion, a POSITA would not have been motivated by Dong’s silence on this issue, let alone be motivated to “investigate techniques that could address programming disturb or programming errors,” as Dr. Liu suggests. *Id.* And even if a POSITA were motivated to seek out such a solution, a POSITA would not look to Costa which

does not focus on program disturb. Instead, as I explained, Costa focuses on disturb issues that occur during a verify phase.

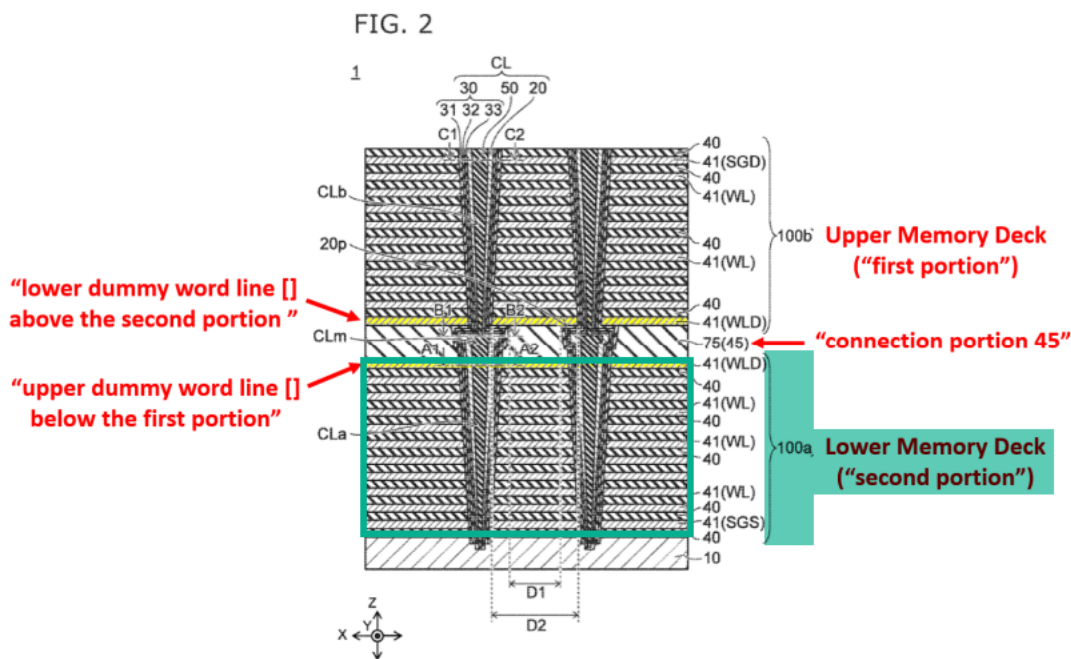
247. For all these reasons, I conclude that Petitioner fails to allege that this combination renders obvious claims 8 or 9. *See* Pet. 74-77.

IX. Ground 4: A POSITA Would Not Have Been Motivated To Modify Dong With Shirai's Disclosure

248. Petitioner alleges Dong and Shirai render obvious claims 4, 10, and 14, which depend from respective claims 1, 5, and 11. Pet. 77.

A. *A POSITA Would Not Have Applied $V_{PASS-LOW}$ To The Entire Lower Memory Deck of Shirai*

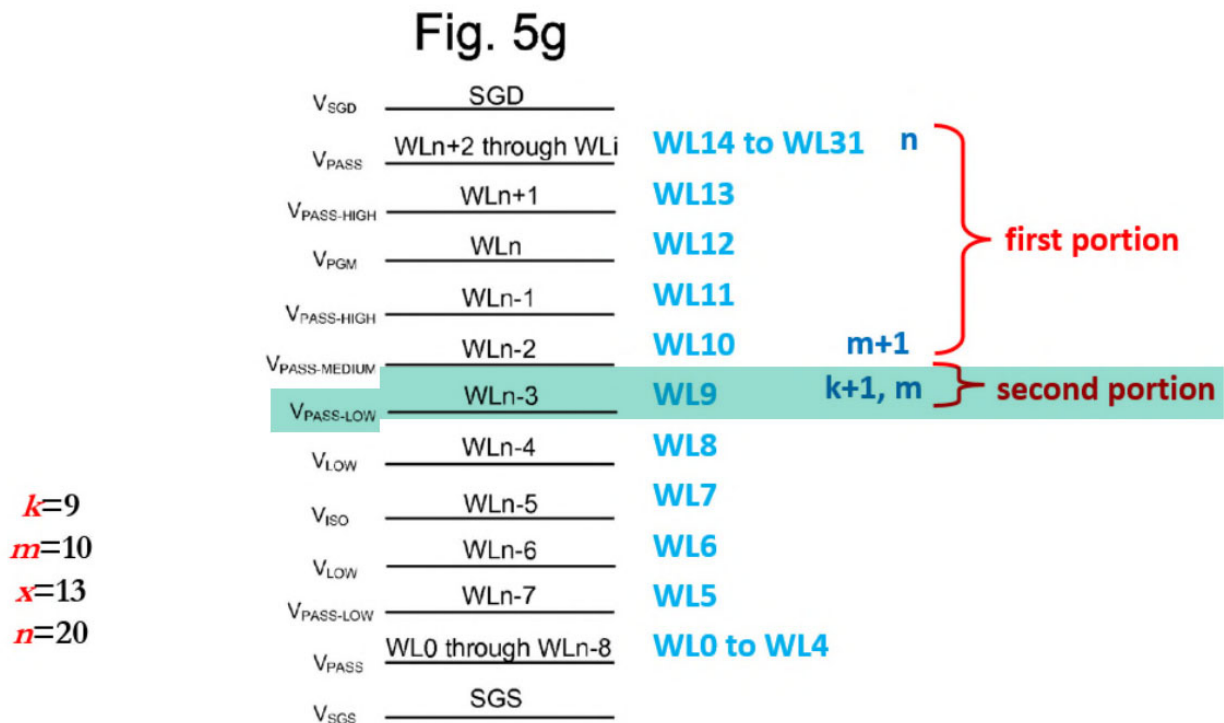
249. Petitioner relies on the below annotated Figure 2 of Shirai to represent its position regarding claim 4:



Pet. 80-83 (annotating Shirai Fig. 2; teal annotations added by Patent Owner); Liu at 121; Liu Dep., 167:1-7.

250. Petitioner states, “[r]ecall that in base claim 1, the second portion [is] formed below the first portion,” and admits that “Dong’s second portion corresponds to Shirai’s bottom deck 100a.” Pet. 82; Liu, ¶232; *see also* Liu Dep., 178:7-179:17.

251. But Petitioner identifies a *single wordline* for Dong’s “second portion” of claim 1 (highlighted in teal below):



Pet. 54 (annotating Dong’s Fig. 5g; teal annotation added by Patent Owner); *see also* Pet. 84. And the “second portion” of Dong relied on by Petitioner receives a

voltage of $V_{\text{PASS-LOW}}$. Pet. 53-54. According to Petitioner's interpretation, the entire second portion in Shirai (see Figure 2 above) is driven with a voltage $V_{\text{PASS-LOW}}$. But Petitioner fails to explain how or why a POSITA would apply $V_{\text{PASS-LOW}}$ to Shirai's Lower Memory Deck 100a (which appears to comprise WL0 through WL8 based on the number of wordlines in Shirai's Figure 2) instead of, for example, V_{PASS} as disclosed in Petitioner's mapping of Dong (according to Petitioner, V_{PASS} is applied to WL0 through WL4). *See* Dong, Fig. 5g; Pet. 54.

252. In my opinion, there are multiple discrepancies here: **First**, the “second portion” consists of one wordline in Petitioner's annotated Figure 5a of Dong, but the equivalent “second portion” in Shirai's Figure 2 consists of the entire Lower Memory Deck 100a. **Second**, Petitioner's annotated version of Dong's Figure 5g shows the entire second portion driven with $V_{\text{PASS-LOW}}$. As applied in Shirai's Figure 2 showing the equivalent “second portion” as the entire Lower Memory Deck 100a, the entire Lower Memory Deck 100a is driven with $V_{\text{PASS-LOW}}$. Accordingly, no wordlines in Shirai's Lower Memory Deck 100a are driven with V_{LOW} , V_{ISO} , V_{PASS} (the remaining voltages of the Dong's Figure 5a which drive lines WL0 through WLn-4). **Finally**, Petitioner's annotated Figure 5a of Dong states that “n=20,” but Petitioner's annotated Figure 2 of Shirai completely ignores WL0 through WLn-4.

253. Moreover, a POSITA would not have been motivated to apply Dong's voltage scheme for a single wordline ($V_{\text{PASS-LOW}}$) to the entire Lower Memory Deck 100a of Shirai, including WL0 through WLn-8. Dong discloses that " V_{PASS} is applied to a first group of storage elements associated with WL0 through WLn-8, where the first group is adjacent to the source side select gate, and on a source side of the isolation wordline WLn-5." Dong, ¶58;³ *see id.*, ¶51 (describing pass voltages applied to unselected wordlines near source and drain "reduce program disturb").

254. Dong also discloses "increasing the number of wordlines in between the selected wordline and the V_{ISO} wordline" and "*gradually* reducing the bias voltage on those wordlines" in order to reduce "the electric field in between the selected wordline and the V_{ISO} wordline," thereby reducing program disturb (by reducing hot carrier injection (HCI) based program disturb). Dong, ¶57. This is because the drain-to-source voltages of cells are reduced, diminishing HCI and reducing program disturb. But Petitioner's combination goes against this disclosure by applying a single bias voltage ($V_{\text{PASS-LOW}}$) to every wordline of Shirai's Lower Memory Deck 100a. A POSITA would not be motivated to make

³ Petitioner admits that the description for Figure 5f "applies equally" to Figure 5g. Pet. 58 n.7.

this combination because it would actually increase program disturb, a problem Dong aims to avoid.

255. And Dong discloses that, “[i]f V_{pass} is too low, boosting in the channel is insufficient to prevent program disturb.” Lutze (Ex. 1015), 4:19-21;⁴ Dong, ¶44 (“[I]f a pass voltage, V_{PASS} , is low, the channel of the inhibited NAND string is not well boosted, and a selected wordline of the unselected NAND string can be unintentionally programmed.”). This is because, as a POSITA would have known, the difference between the gate voltage and the channel voltage is higher when the channel voltage is not sufficiently boosted, which causes program disturb. Petitioner’s combination results in exactly that—applying a low V_{pass} (i.e., $V_{PASS-LOW}$) reducing the boosting in the channel, thereby increasing program disturb. As a result, a POSITA would not be motivated to implement Petitioner’s proposed combination.

256. In my opinion, Petitioner also never explains how or why a POSITA would omit V_{ISO} (or V_{LOW}) from the self-boosting mode as applied to WL7 (or WL6 and WL8) in Dong’s Figure 5g when combining it with Shirai. Note that Dong discloses that $V_{PGM} > V_{PASS-HIGH} > V_{PASS-MEDIUM} > V_{PASS-LOW} > V_{LOW} > V_{ISO}$. Dong, ¶57. The elimination of V_{LOW} and V_{ISO} from Petitioner’s combination of

⁴ Petitioner recognizes Dong incorporates Lutze (Ex. 1015) by reference. Pet. 30.

Dong and Shirai will result in a more abrupt change in channel voltage, and therefore an increased propensity toward program disturb due to HCI. Moreover, as a POSITA would have understood, Dong discloses that the isolation wordline is the mechanism that enables prevention of program disturb. Dong, Abstract; *see id.*, ¶¶67-68. That is why, in my opinion, Dong discloses relying on an isolation wordline in every self-boosting mode to “isolate programmed and erased channel areas in the substrate.” *Id.*, ¶65; *see id.*, ¶¶66-67, Figs. 5a-5g, Title, Abstract. This isolation wordline increases the resistance of the channel on the drain side of the isolation wordline, thereby increasing channel boost on the drain side, and reducing program disturb.

257. Dong explains that “[b]oth [Local Self Boosting] and [Erased Area Self Boosting] attempt to isolate the channel of previously programmed cells from the channel of the cell being inhibited.” Lutze (Ex. 1015), 3:65-4:1; *id.* at 4:1-19; Dong, ¶10 (incorporating Lutze by reference); Pet. 30 (admitting same). Dong discloses that “[w]ith the EASB or REASB boosting modes, V_{ISO} is applied to one or more source-side neighbors of the selected word line at some point after boosting is initiated, and is sufficiently low to isolate programmed and erased channel areas in the substrate.” Dong, ¶¶65-66.

258. Without an isolation wordline, this key mechanism of Dong is removed, resulting in degraded program disturb characteristics. A POSITA would

thus not have been motivated to omit Dong's isolation wordline (i.e., the one receiving V_{ISO}) whose sole purpose is to reduce program disturb.

259. In my opinion, Petitioner's positions for claim 14 fail for the same reasons as claim 4 explained in this section. *See* Pet. 84 ("Claim 14 is identical to claim 4 and is met for the same reasons.").

B. *Petitioner Fails To Apply Prior Art To Claim 10*

260. In my opinion, Petitioner also fails to clearly explain and show with particularity why claim 10 is unpatentable. Instead, Petitioner provides a conclusory statement that "[c]laim 10 is substantively the same as claim 4 and is met for the same reasons." Pet. 83. But claim 10 is not substantively the same as claim 4. Claim 4 depends from claim 1 and claim 10 depends from claim 5. As Petitioner recognizes in its Petition, claims 1 and 5 recited distinct limitations. *See* Pet. 29-44 (applying Dong's Figure 5a to claim 5); Pet. 50-66 (applying Dong's Figure 5g to claim 1). For example, Petitioner cites different sections of distinct figures of Dong to correspond to the recited "first portion" and "second portion" in these two claims. As Petitioner recognizes, claims 4 and 10 are "not worded identically" (Pet. 83)—i.e., they recite different limitations.

261. I understand that it is Petitioner's burden to map prior art in a way to meet each recited limitation. Here, for claim 10, Petitioner fails to do so. Petitioner never explains how or why a POSITA would apply Dong's voltage scheme of

Figure 5a—which is completely different than in Dong's Figure 5g which Petitioner applied to claim 4—to Shirai's architecture. *See* Pet. 83-84. Petitioner instead describes the differences between claims 4 and 10—without ever showing how the voltages of Dong's Figure 5a would be applied to Shirai's architecture in the context of claim 10. *Id.*

C. *Petitioner Improperly Modifies The Value For The Recited “K” Limitation Used For Respective Independent Claims*

262. In my opinion, Petitioner's combinations addressing claims 4 and 14 are also flawed because they each use a different interpretation for the variable “k” than independent claims 1 and 11, respectively.

263. For example, Petitioner fails to explain how or why variable k equals 9 when addressing claim 1, but the same variable k equals 0 when addressing claim 4. *Compare* Pet. 53 (“k can be taken as 9” for the recited “second portion ... comprising a (k+1)th wordline to an mth wordline from bottom to top”), *with id.*, 82-83 (depicting the recited “second portion” as the lower deck, extending from the first wordline to the wordline just below the “upper dummy wordline,” resulting in k equal to 0). Petitioner never maps claim 1 to Dong when k is 0. *See* Pet. 50-51; Liu, ¶154 (p. 79); Liu Dep., 67:2-19.

264. Petitioner's allegations for claim 10 fail for the same reason. Petitioner fails to explain how or why variable k equals 2 when addressing independent claim 5, but the same variable k equals 9 when addressing claim 10.

Compare Pet. 43 (“k can be taken as 2” for the recited “first portion ... comprising a first wordline to a kth wordline from bottom to top”), *with id.*, 83-84 (Patent Owner assuming, without Petitioner explaining, that the “first portion” refers to Shirai’s Lower Memory Deck 100a, in which case k equals 9, since claim 5 requires the first portion to “compris[e] a first word line to a kth word line,” and the lower deck in Shirai consists of 9 wordlines); Shirai, Fig. 2 (showing 9 wordlines in the Lower Memory Deck 100a between “41(SGS)” to “41(WLD)”).

265. Petitioner never provides a mapping for claim 5 assigning k a value of 9, much less explains how the variable k can be 9 and still satisfy the limitation in claim 5 that “ $k < m$ ” when Petitioner defined m as 7. *See* Pet. 34-38; Liu, ¶154 (p. 79); Liu Dep., 67:2-19.

266. Similarly, Petitioner never explains how m can equal 7 when addressing claim 5 but equal 18 for claim 10. *Compare* Pet. 38 (“m=7”), *with id.*, 83-84 (again, assuming, without Petitioner explaining, that the “second portion” refers to Shirai’s Upper Memory Deck 100b, in which case m equals 18); Shirai, Fig. 2 (showing 9 wordlines in the Lower Memory Deck 100a between “41(SGS)” to “41(WLD)” and 9 wordlines in the Upper Memory Deck 100b between “41(WLD)” and “41(SGD)”).

267. In my opinion, Petitioner’s theories of the prior art for claims 4, 10, and 14 contradict its positions for respective independent claims. Even if Petitioner

were correct that “it was well-known that 3D NAND strings often exceed 100 cells by the Priority Date” (Pet. 77), it is unclear how that has anything to do with Petitioner’s mappings. Petitioner fails to explain how the recited variables of the independent claims are accounted for in its allegations regarding claims 4, 10, and 14.

D. *A POSITA Would Not Have Been Motivated To Combine Dong’s 2D Disclosure With Shirai’s 3D Disclosure*

268. Petitioner’s motivation to combine rests on the assumption that Dong’s vague mention of “three dimensional” refers to vertical channel 3D NAND. Pet. 77-80. That is not the case, as explained above. *Supra* Section VII.B. Petitioner’s motivation to combine relies solely on etching issues unique to vertical 3D NAND as described in Shirai, but these do not apply to Dong. A POSITA would recognize, in my opinion, that Dong does not have “challenges imposed by limitations on forming anisotropic vertical etch profiles” (Liu, ¶223) because Dong does not disclose vertical 3D NAND. Nor would a POSITA be motivated to apply Dong’s voltage schemes in a 3D NAND context like Shirai’s for the reasons I explain above. *See* Section VII.B.2.c.

X. CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed November 10, 2025 in Boulder, Colorado.



Dr. Sunil Khatri