

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case No. IPR2025-00190
U.S. Patent No. 11,568,941
Issue Date: January 31, 2023

Title: MEMORY INCLUDING A PLURALITY OF PORTIONS AND USED
FOR REDUCING PROGRAM DISTURBANCE AND PROGRAM METHOD
THEREOF

PETITIONER'S REPLY BRIEF

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1001	U.S. Patent No. 11,568,941 to Song et al. (the “’941 patent”)
1002	File History for U.S. Patent No. 11,568,941
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1004	Declaration of David Kuan-Yu Liu, Ph.D. (“Liu”)
1005	U.S. Patent Publication No. 2008/0279008 (“Dong”)
1006	U.S. Patent Publication No. 2008/0159003 (“Dong II”)
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1015	U.S. Patent No. 6,859,397 (“Lutze”)
1016	U.S. Patent No. 10,269,570 (“Lee IV”)
1017	U.S. Patent Publication No. 2012/0163096 (“Futatsuyama”)
1018	U.S. Patent Publication No. 2019/0214405 (“Shirai”)
1019	U.S. Patent No. 10,438,671 (“Chen”)
1020	U.S. Patent No. 9,589,978 (“Yip”)

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1042	YMTC, <i>Yangtze Memory Technologies Co. Ltd. Officially Established</i> (Aug. 1, 2016) (https://www.ymtc.com/cn/news/28.html) ("YMTC Press Release")
1043	Certified English Translation of Ex. 1042 (YMTC Press Release)
1044	Testimony of Stephen Ezell (VP, Global Innovation Policy – Information Technology & Innovation Foundation) Before the U.S.-China Economic and Security Review Commission (Apr. 14, 2022)
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1048	YMTC's Rule 7.1 Corporate Disclosure Statement, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , Case No. 5:23-cv-05792-VKD (N.D. Cal. Nov. 9, 2023)
1049	Lianhe Credit Rating Co., Ltd., Wuhan Optics Valley Financial Holding Group Co., Ltd., 2024 Tracking Rating Report (Jun. 28, 2024) ("2024 Tracking Rating Report")
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1057	Wuhan University of Science and Technology, <i>Yangtze Memory Technologies Co., Ltd. 2020 Campus Recruitment Introduction</i> (Sept. 10, 2019) (https://wust.91wllm.cn/teachin/view/id/97310) (“Wuhan Univ. of Sci. and Tech., YMTC 2020 Campus Recruitment Introduction”)
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1061	Yoko Kubota et al., <i>U.S. Chip Equipment Suppliers Suspend Business Activities at Yangtze Memory</i> , WALL STREET JOURNAL CHINA (Oct. 13, 2022) (https://cn.wsj.com/articles/美国供应商暂停在中国长江存储科技的业务活动-11665617406) (“WSJ China Article”)
1062	Certified English Translation of Ex. 1061 (WSJ China Article)
1063	Letter from Michael T. McCaul, Member of Congress, and Bill Hagerty, U.S. Senator, to the Honorable Gina Raimondo, U.S. Commerce Secretary (July 12, 2021)
1064	Demetri Sevastopulo, <i>Bipartisan Group Urges US Blacklist for “Beijing-Directed” Chipmaker</i> , FINANCIAL TIMES (Sept. 20, 2022) (https://www.ft.com/content/173eb5b7-c211-4fa8-af8e-93382ed12836) (“Financial Times Article”)
1065	U.S. Senator Charles E. Schumer, <i>With Chinese Chip Companies Threatening National Security And Jobs, Schumer Announces President Has Heeded His Call And Will Add YMTC - One Of China’s Leading Chip Makers - To A Trade Blacklist; Administration Action Will Strengthen National Security And Protect The Domestic Chip Industry</i> (Dec. 16, 2022) (“Schumer Statement”)
1066	U.S. Department of Defense, <i>DOD Releases List of People’s Republic of China (PRC) Military Companies in Accordance with Section 1260H of the National Defense Authorization Act for Fiscal Year 2021</i> (Jan. 31, 2024) (https://www.defense.gov/News/Releases/Release/article/3661985/dod-releases-list-of-peoples-republic-of-china-prc-military-companies-in-accord/)

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1067	U.S. Department of Defense, <i>Entities Identified as Chinese Military Companies Operating in the United States in accordance with Section 1260H of the William M. (“Mac”) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Public Law 116-283)</i> (https://media.defense.gov/2024/Jan/31/2003384819/-1/-1/0/1260H-LIST.PDF)
1068	<i>Oversight of the USPTO: Hearing Before the Subcomm. On Intellectual Property</i> , 118th Cong. (2023) (Testimony of Katherine Vidal, Undersecretary of Commerce for IP and Director of USPTO)
1069	China's State Council, <i>Notice of the State Council on Issuing Policies to Promote the High-quality Development of the Integrated Circuit Industry and Software Industry in the New Era</i> (Aug. 4, 2020) (https://www.gov.cn/zhengce/content/2020-08/04/content_5532370.htm) (“State Council Notice on Policies to Promote Development of IC”)
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1075	Tanaka et al., <i>Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory</i> , VLSI Symposium Technical Digest, 2007, pp. 14-15

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1083	U.S. Patent No. 9,230,658 ("Han")
1084	U.S. Patent No. 9,530,492 ("Lee 492")
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1093	U.S. Patent No. 10,438,671
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1095	U.S. Patent No. 11,581,322
1096	U.S. Patent No. 10,861,872
1097	U.S. Patent No 10,658,378
1098	U.S. Patent No 10,950,623
1099	U.S. Patent No 10,672,711
1100	District Court Declaration of Dr. Sunil P. Khatri, Ph.D., dated January 31, 2025
1101	<i>Novel Ultrahigh-Density Flash Memory With a Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell</i> , Tetsuo Endoh et al., IEEE Transactions on Electron Devices, Vol. 50, No. 4, April 2003 (“Endoh1”)
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1103	NAND Memory Market Tracker – Q2 2020, https://omdia.tech.informa.com/-/media/tech/omdia/legacy-ih/asset-families/nand-memory-market-tracker-q2-2020.pdf
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1109	https://news.samsung.com/global/samsung-starts-mass-producing-industrys-first-3d-vertical-nand-flash
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LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 1:	
[1.PRE]	A memory comprising:
[1.A]	a first portion comprising an (m+1)th wordline to an nth wordline from bottom-to-top; and
[1.B]	a second portion formed below the first portion and comprising a (k+1)th wordline to an mth wordline from bottom-to-top; and
[1.C]	a controller configured to apply
[1.D]	a first voltage to an (x+2)th wordline to the nth wordline,
[1.E]	a second voltage to an (x+1)th wordline,
[1.F]	a third voltage to an (x-1)th wordline,
[1.G]	a fourth voltage to the (m+1)th wordline to an (x-2)th wordline, and
[1.H]	a fifth voltage to the (k+1)th wordline to the mth wordline when an xth wordline is used to perform a program operation;
[1.I]	wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.
Claim 3:	
[3.PRE]	The memory of claim 1, further comprising
[3.A]	a third portion formed above the first portion and comprising a plurality of wordlines
[3.B]	wherein the controller is further configured to apply the first voltage to the plurality of wordlines when the xth wordline is used to perform the program operation.

Ref. #	Listing of Challenged Claims
Claim 4:	
[4]	The memory of claim 1, further comprising:
[4.A]	an upper dummy wordline formed below the first portion;
[4.B]	a lower dummy wordline formed above the second portion; and
[4.C]	a joint oxide layer formed between the upper dummy wordline and the lower dummy wordline;
[4.D]	wherein the memory has a two-deck structure.
Claim 5:	
[5.PRE]	A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first wordline to a kth wordline from bottom-to-top, the second portion formed above the first portion and comprising a (k+1)th wordline to an mth wordline from bottom-to-top, the program method comprising:
[5.A]	applying a first voltage to the to the first wordline to an (x-2)th wordline when an xth wordline is used to perform a program operation;
[5.B]	applying a second voltage to an (x-1)th wordline; and
[5.C]	applying a third voltage to an (x+1)th wordline;
[5.D]	wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.
Claim 6:	
[6.PRE]	The program method of claim 5, further comprising:
[6.A]	applying a fourth voltage to an (x+2)th wordline to the mth wordline; and
[6.B]	wherein $x < (m-1)$.

Ref. #	Listing of Challenged Claims
Claim 7:	
[7.PRE]	The program method of claim 5, wherein the memory further comprises a third portion formed above the second portion, the third portion comprises an (m+1)th wordline to an nth wordline from bottom-to-top, and the program method further comprises:
[7.A]	applying a fourth voltage to the (x+2)th wordline to the nth wordline;
[7.B]	wherein $m < n$, and $x < (n-1)$.
Claim 8:	
[8.PRE]	The program method of claim 7, wherein:
[8.A]	the first voltage has a first level if the xth wordline is in the first portion;
[8.B]	the first voltage has a second level if the xth wordline is in the second portion;
[8.C]	the first voltage has a third level if the xth wordline is in the third portion; and
[8.D]	the first level is lower than the second level, and the second level is lower than the third level.
Claim 9:	
[9.PRE]	The method of claim 5, wherein:
[9.A]	the first voltage has a first level if the xth wordline is in the first portion;
[9.B]	the first voltage has a second level if the xth wordline is in the second portion; and
[9.C]	the first level is lower than the second level.

Ref. #	Listing of Challenged Claims
Claim 10:	
[10.PRE]	The program method of claim 5, wherein the memory further comprises:
[10.A]	a lower dummy wordline formed above the first portion;
[10.B]	an upper dummy wordline formed below the second portion;
[10.C]	a joint oxide layer formed between the lower dummy wordline and the upper dummy wordline;
[10.D]	wherein the memory has a two-deck structure.
Claim 11:	
[11.PRE]	A program method of a memory, the memory comprising a first portion and a second portion formed below the first portion, the first portion comprising an (m+1)th wordline to an nth wordline from bottom-to-top, the second portion comprising a (k+1)th wordline to an mth wordline from bottom-to-top, the program method comprising:
[11.A]	applying a first voltage to an (x+2)th wordline to the nth wordline when an xth wordline is used to perform a program operation;
[11.B]	applying a second voltage to an (x+1)th wordline;
[11.C]	applying a third voltage to an (x-1)th wordline;
[11.D]	applying a fourth voltage to the (m+1)th wordline to an (x-2)th wordline; and
[11.E]	applying a fifth voltage to the (k+1)th wordline to the mth wordline;
[11.F]	wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

Ref. #	Listing of Challenged Claims
Claim 13:	
[13.PRE]	The program method of claim 11, wherein the memory further comprises a third portion formed above the first portion, the third portion comprises a plurality of wordlines, and the program method further comprises:
[13.A]	applying the first voltage to the plurality of wordlines of the third portion.
Claim 14:	
[14.PRE]	The program method of claim 11, wherein the memory further comprises:
[14.A]	an upper dummy wordline formed below the first portion;
[14.B]	a lower dummy wordline formed above the second portion; and
[14.C]	a joint oxide layer formed between the upper dummy wordline and the lower dummy wordline;
[14.C]	wherein the memory has a two-deck structure.

ABBREVIATIONS

Abbreviation	Description
'941 or '941 patent	U.S. Patent No. 11,568,941 (Ex. 1001)
Aritome	Aritome, "NAND Flash Memory Technologies" (Ex. 1009)
Costa	U.S. Patent Publication No. 2018/0012667 (Ex. 1012)
Dong	U.S. Patent Publication No. 2008/0279008 (Ex. 1005)
Kito	U.S. Patent Publication No. 2007/0252201 (Ex. 1087)
Liu	Declaration of David Kuan-Yu Liu, Ph.D. (Ex. 1004)
Liu_Supp	Reply Declaration of David Kuan-Yu Liu, Ph.D. (Ex. 1089)
Shirai	U.S. Patent Publication No. 2019/0214405 (Ex. 1018)
Tanaka	Tanaka et al., Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory, VLSI Symposium Technical Digest, 2007, pp. 14-15 (Ex. 1075)
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,568,941 (Paper 1)
ID	Institution Decision (Paper 22)
POPR	Patent Owner's Preliminary Response (Paper 11)
POR	Patent Owner's Response (Paper 33)
PO or Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.

I. INTRODUCTION

Ground 1 (anticipation) and 2 (obviousness): PO does not dispute that Dong Figs. 5a/g disclose the programming voltages for “reduc[ing] program disturb” (Dong, [0012]) recited in claims 1, 3, 5-7, 11, and 13. Instead, PO uses the wrong date (*i.e.*, 2007 instead of 2020) to assess validity vis-à-vis the **bottom-to-top** limitation. Doing so is legal error, but Petitioner prevails under either date. Likewise, Dong’s “three dimensional” memory disclosure and vertically-oriented memory string figures (which parallel those in the ’941 patent) render the claims unpatentable under either party’s **bottom-to-top** construction. §§III.A-B.

Ground 3: PO artificially restricts the ways in which the Dong/Costa combination satisfies claims 8-9. §IV.A. And the Dong/Costa combination renders claims 8-9 obvious under the correct **program mode** interpretation. §IV.B.

Ground 4: Dong combined with Shirai renders claims 4, 10, and 14 obvious. PO’s smorgasbord of arguments fail because they are premised on assertions Petitioner never made, improper bodily incorporation, and restrictions not present in the claims. §V.

II. CLAIM CONSTRUCTION

PO construes three terms. POR, 12-35. Petitioner disputes two. Liu_Reply, ¶¶4-37.

A. “*Bottom-to-top*” (Liu_Reply, ¶¶5-26)

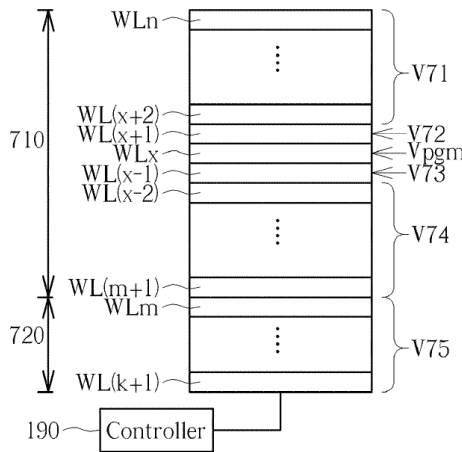
The claims generically recite *a memory*, which the parties agree covers 3D memories with vertical memory strings. The parties dispute whether the claims are *limited to* vertical 3D memory strings. POR, 12-29. Petitioner says no; PO says yes. Liu_Reply, ¶¶5-6. While Petitioner is correct, Petitioner prevails under either interpretation (§III.A-B), so no construction is necessary.

The claims recite *bottom-to-top* to establish a reference scheme (using variables *x*, *k*, *m*, etc.) for identifying wordline groups (called *portions*) for applying voltages, not to require a physical memory string architecture. EX1094, 174:24-175:10; Liu_Reply, ¶¶13, 15. The *above* and *below* claim language simply reflects relative locations in a memory string *already indexed from bottom-to-top*. *Id.*, ¶¶7-11, 14.

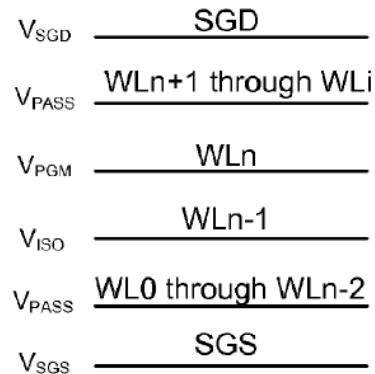
PO contends Petitioner's construction fails because the '941 specification (and claims) make “no reference” to “source or drain.” POR, 15-16. But neither do they mention the “substrate” that PO's construction requires. Liu_Reply, ¶12. Numerous references confirm Petition's source-to-drain construction. *Id.*, ¶¶24-26; EX1082, 1:59-63; EX1083, 3:25-33; EX1084, Fig. 1D EX1085, 121:41-46; EX1086, [0018].

In a double-standard vis-à-vis the prior art, PO contends the '941 figures restrict the claims to vertical memory (POR, 16-18), but Dong's vertically-oriented

Figs. 5a/g exclude vertical strings. The Board invited the parties to address this issue. ID, n.6. Petitioner does so in §III.B. In summary, if the '941 figures connote vertical strings, so do Dong's vertically-oriented figures, as the side-by-side comparison below shows. Liu_Reply, ¶¶17-23. '941 Figs. 1-11 show voltages ("V1," "V2," etc.) assigned to wordlines. Dong Figs. 5a/g depict similar voltage assignments (V_{PASS} , V_{ISO} , etc.).



'941, Fig. 8



Dong, Fig. 5a

B. "Program Operation"

[P]rogram operation should be afforded its plain meaning—*i.e.*, the steps necessary to program a data value. A POSITA would understand this includes two iterative steps: charge injection (sometimes called programming phase) where a programming pulse is applied, and verification (*i.e.*, determining if additional charge is needed). Liu_Reply, ¶¶27-37. Both the intrinsic and extrinsic evidence confirm

this. The Board should reject PO's artificial restriction limiting **program operation** to charge injection. POR, 29-34.

PO's procedural argument that Dr. Liu's deposition "revealed a new position" (viz., that **program operation** "include[s] both a program [and verify] phase," POR, 29-30) fails the red-face test. Dr. Liu's opening declaration states "[t]he other phase of a typical programming operation is the verify phase." Liu, ¶60; Pet., 71 (similar); Liu_Reply, ¶37.

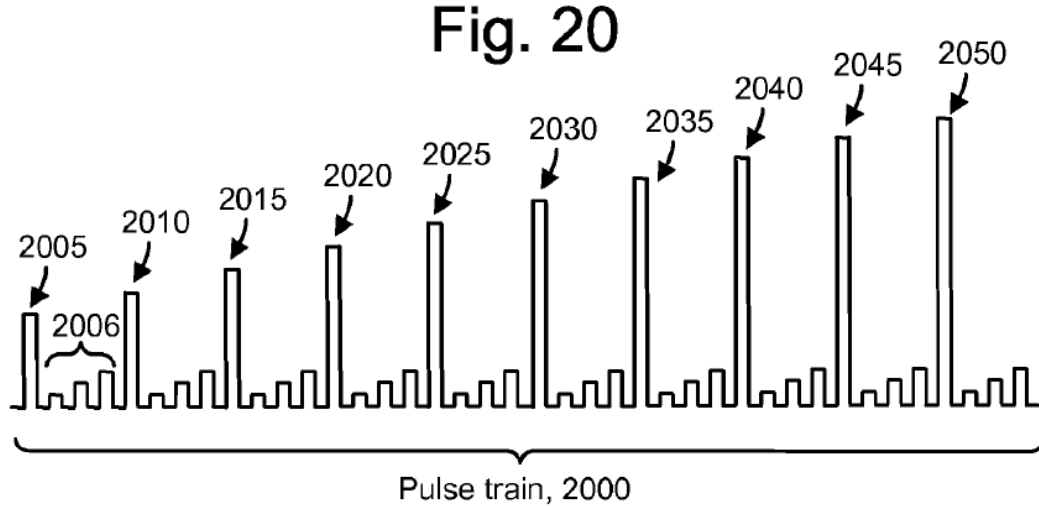
The intrinsic evidence supports Petitioner. The '941 patent states "program operation" refers to "programming a memory cell." '941, 3:6-7. It was (and is) well-known that flash memory stores values representing logic "1s" and "0s." Liu_Reply, ¶29. Even if a single pulse injecting *de minimis* charge constituted a **program operation** (per PO's construction), that does not restrict **program operation** from **also** including programming a memory cell to a desired logic state (Petitioner's construction). *Id.*, ¶30.

PO argues the '941 patent's "voltages only ... reduce program disturb if applied **during** a program operation." POR, 31 (emphasis by PO). But that is consistent with Petitioner's construction (which includes verification) and the '941 specification's disclosure regarding reducing "program disturbance **and pass voltage disturbance**" ('941, 6:39-43; *id.*, 1:39-41), which occurs during verification/reading. EX1012, [0122]; Liu_Reply, ¶¶31-32; EX1094, 197:4-22.

Numerous references show pass voltages (*e.g.*, V_{pass}) applied to unselected cells during verification. EX1012, Fig. 14, [0033] (unselected cells “receive[] variable pass voltage”); EX2024, Fig. 2 (“ V_{PASS} ” applied during “Verify Phase”); EX2027, Fig. 2 (similar). Thus, PO’s argument that “the ’941 patent does not describe [verification]” (POR, 32) is misleading.¹

Claims 8-9 require programming cells in different memory string **portions** (*viz.*, increasing the **first voltage** as programming progresses). Thus, programming advances when the previous **program operation** finishes, which requires both charge injection and verification. Liu_Reply, ¶34. Numerous references (including Dong) confirm this. Dong Fig. 20 shows “pulse train 2000 applied ... **during programming**” includes both charge injection (program) pulses 2005, 2010, etc. **and** “verify pulses 2006.” Dong, [0132].

¹ PO’s attempt to paint Dr. Liu as inconsistent fails. POR, 33-34. Read in context, Dr. Liu described the same two-part process in both proceedings. *E.g.*, Liu_Reply, ¶36; EX2022, ¶203 (“Suzuki discloses a program loop comprising a program operation followed by a verify operation”).



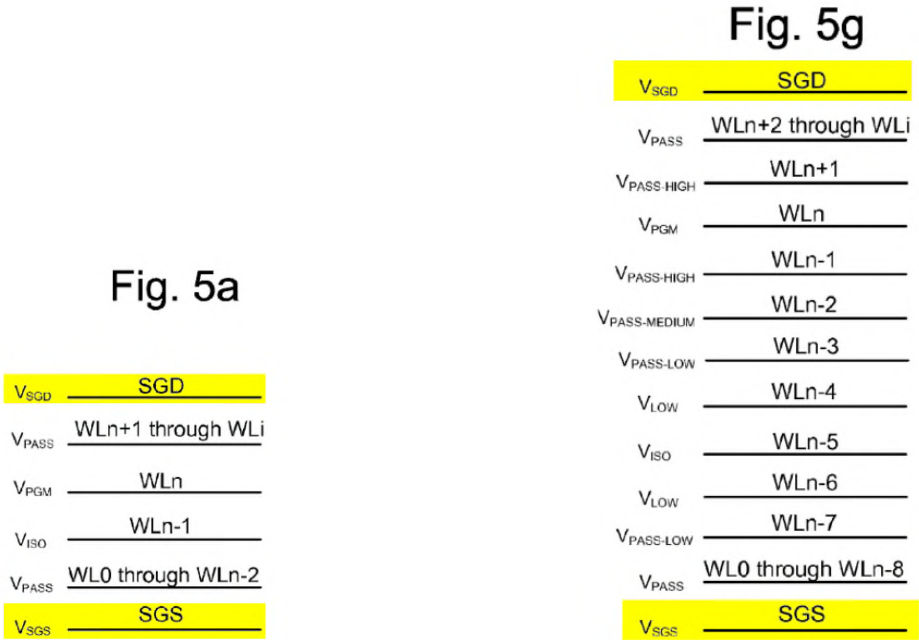
Dong, Fig. 20; *id.*, Fig. 19, [0128]-[0133]; EX1090, 9:14-16 (“program operation ha[s] ... alternat[ing] program and verify phases”); EX1091, 21:1-11 (“program operation [includes] ... verify phase.”); EX1092, 5:7-9; EX1093, 27:22-29; Liu_Reply, ¶¶34-35.

III. GROUNDS 1 AND 2

A. Dong Satisfies “*bottom-to-top*” Under Petitioner’s Construction

PO does not dispute that Dong satisfies the *bottom-to-top* requirement under Petitioner’s construction. See POR. While the parties dispute whether Dong discloses and/or renders obvious 3D memory strings (it does), the parties agree Dong discloses 2D memory strings. POR, 36-39. Describing Figs. 5a-h, Dong states “the *source-side select gate control line is SGS* and the *drain-side select gate control line is SGD*,” and that programming proceeds from source to drain. Dong, [0048]. Dong Figs. 5a/g show this, with wordlines indexed and programmed from the

source/SGS (bottom) to drain/SGD (top). Even if rotated/read “horizontally,” Figs. 5a/g satisfy **bottom-to-top** under Petitioner’s construction.



Dong, Fig. 5a (annotated)

Dong, Fig. 5g (annotated)

B. Dong Satisfies PO’s Narrow “bottom-to-top” Construction

Dong anticipates and renders obvious **bottom-to-top** under PO’s construction.²

² Even if the Petition had not presented vertical 3D-memory arguments, Petitioner may do so now under PO’s construction. *Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1374, 1383 (Fed. Cir. 2023).

1. Anticipation Under PO's Construction

Dong meets PO's narrow **bottom-to-top** construction (*i.e.*, vertical memory strings). Referring to Fig. 12 (generally applicable vis-à-vis Fig. 5), Dong discloses "the array of storage elements can be **three dimensional**." Dong, [0095]. A POSITA reading Dong in 2020 would readily envisage vertical 3D-memory. Liu_Reply, ¶¶38-56. PO denigrates Dong for its "passing" 3D-memory disclosure. POR, 2, 40. But the Federal Circuit has rejected this argument because "a reference is prior art for all that it teaches," even "passing mention" to "less preferred embodiments." *Guardant Health, Inc. v. Univ. of Wash.*, 2026 U.S. App. LEXIS 1651, at *18-20 (Fed. Cir. 2026) (citing cases and vacating patentability finding).

Nevertheless, PO contends that on "Dong's May 7, 2007 filing, 'three-dimensional' memory would not have been understood by a POSITA to disclose [vertical memory strings]." POPR, 47-49; POR, 42-43 (similar). PO's argument fails for two independent reasons.

First, PO erroneously analyzes anticipation using Dong's filing date instead of the '941 priority date. POR, 42-43. This contradicts black-letter law that "the effective filing date of the claimed invention" controls. 35 U.S.C. §102(a). The analysis turns on POSITA knowledge/understanding in 2020, not 2007. *Sage Prods., LLC v. Stewart*, 133 F.4th 1376, 1384 n.5 (Fed. Cir. 2025).

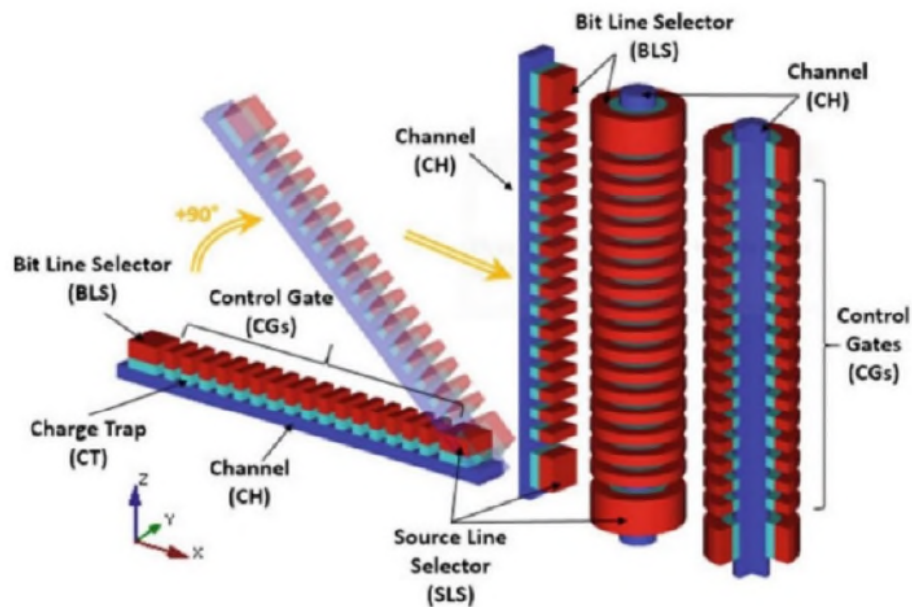
Accordingly, the Board rejected PO's assertion that Dong's "three-dimensional" memory disclosure excluded vertical strings. ID, 26-27. Nevertheless, the Board "invited [PO] to address this issue" if it "dispute[d] that [POSITA knowledge] should be assessed as of February 10, 2020." ID, n.7.

PO maintains that Dong's filing date controlled (POR, 42-43), but cited no supporting statute, regulation, or case. *Id.* Nor could it. Per §102, anticipation is assessed at "***the effective filing date of the claimed invention.***" 35 U.S.C. §102(a). This is dispositive, as PO does not dispute a POSITA would understand 3D-memory in 2020 to connote vertical strings. POR, §§II.A.2, III.B (arguing only that "three dimensional" NAND in 2007 "***[i]ncluded***" horizontal strings, not that it excluded vertical strings in 2020); EX1094, 103:6-15. Nor could it, given that vertical strings were the prevailing 3D architecture in 2020. Pet., §V; EX1095-1099 (YMTC patents circa 2020 showing/discussing vertical 3D strings); Liu_Reply, ¶¶40-47. The Board can take notice from IPRs involving 3D-NAND patents before the same panel that YMTC regularly described "three-dimensional" memory as having vertical strings.³ IPR2023-01401, Paper 17, 12 ("Board may consider and make of

³ IPR2025-00117, Paper 27, 1 ("3D NAND memory [] addresses the challenges of forming ***vertical wordline[s]***"); IPR2025-00191, EX2029 ("3D NAND resembles a

record any evidence in a related [Office] proceeding”). Only now does PO change position that “three dimensional” NAND excludes vertical strings.

Pre-2020 textbooks explained that “3D-NAND structure[s] could be conceived by starting from the 2D-NAND string building block and turning the 2D-NAND string upside, resulting in a 3D structure with a vertical channel.” Pet., 12-13 (quotes omitting) (citing EX1010, 122, EX1011, 3).



Pet., 13 (excerpting EX1010, 122). Nor does PO dispute that a POSITA in 2020 “would have been aware of and generally knowledgeable about NAND memory’s structure and fabrication.” Pet., 22-23; POR, 9; Liu_Reply, ¶¶48-49.

vertical skyscraper”); IPR2024-00788, Paper 17, 1 (“3D NAND memory devices generally involve[] ... vertical structures”); IPR2024-00794, Paper 12, 4.

Given the well-developed state of 3D-memory in 2020, a POSITA would “at once envisage” the ’941 patent’s claimed **bottom-to-top** wordline arrangement upon reading Dong’s “three dimensional” NAND disclosure. Pet., 35; *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015); *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022). Numerous industry reports and market data confirm the prevalence of vertical 3D NAND. EX1103, 34; EX1104-EX1107; Liu_Reply, ¶¶41-46.

This distinguishes *Net MoneyIN* (POR, 41) and disposes of PO’s argument that Petitioner needed to argue obviousness. POR, §III.B.2. Regardless, Petitioner did so. §III.B.3. The reference in *Wasica* (POR, 41-42) generically disclosed “any modulation scheme,” but here Dong specifically disclosed “three dimensional” memory, not any generic “memory.” *Guangdong* (POR, 42) is inapposite because Petitioner is not arguing inherency (and need not do so because Dong discloses “three dimensional” memory).

PO asserts Dong “teaches wordlines arranged horizontally” (POR, 36) and cites Dong Fig. 4 (POR, 10, 37, 39). But Petitioner did not cite Fig. 4 because it

lacks the requisite voltages.⁴ Dong Fig. 4's 2D-NAND string in no way restricts the scope of Dong's additional "three dimensional" memory disclosure (Dong, [0095]). PO contends that Dong Fig. 5 is necessarily 2D because Fig. 4 is 2D. POR, 2, 10, 37, 39. But Fig. 4's horizontal orientation contrasts with Dong Fig. 5, which shows vertically-oriented wordlines (like the '941 patent). Further, PO's contention disregards that Dong's "storage elements can be three dimensional" (Dong, [0095]), and divorces that disclosure from Fig. 5a/g.

PO faults Petitioner for citing Dong's vertically-oriented Figs. 5a/g. POR, 37. But these diagrams show the claimed wordline arrangements and programming voltages. PO characterizes Dong Figs. 5a-h as "voltage diagrams" which "do not show [] physical structure," and thus cannot "disclose vertical wordlines." Paper 10, 23-24; *see* POR, §§III.A-B (similar). But these are precisely the types of voltage diagrams in the '941 patent, which PO contends disclose a **bottom-to-top** arrangement. POR, 17. The side-by-side figures below compare representative images from the '941 patent (left) and Dong (right).

⁴ PO's argument that Dong Figs. 5a-h are vertically-oriented solely "for ease of reading" (POR, 37) is belied by Fig. 4 which legibly lists programming voltages horizontally.

Fig. 5a

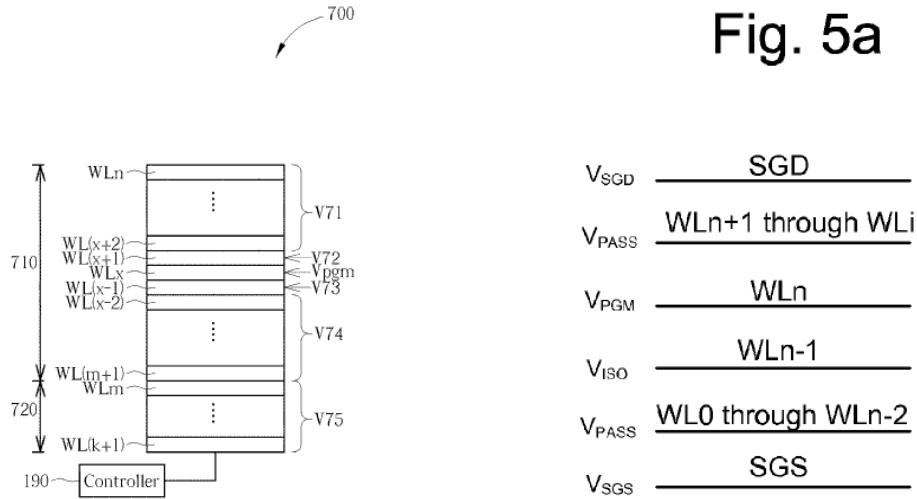


FIG. 8

'941, Fig. 8

Dong, Fig. 5a

Dong's use of voltage names (*e.g.*, V_{ISO}) instead of numbers (*e.g.*, $V71$) is irrelevant. '941, 4:37-61.

At Institution, the Board observed Dong described Figs. 5a-h as "self-boosting modes," but '941 Fig. 8 depicted "memory 700" and "invited [the parties] to address this issue." ID, fn.6. The presence or absence of generic "memory" labels should not determine patentability as no magic words are required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) ("[anticipatory] reference need not satisfy an *ipsissimis verbis* test").

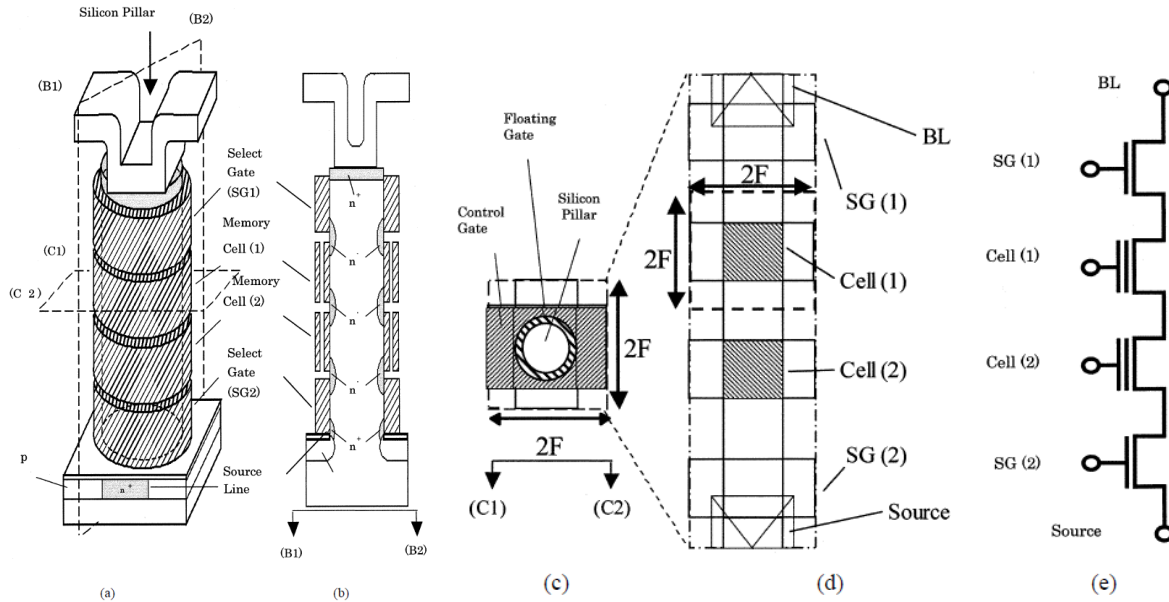
The '941 specification statement that the figures "illustrate a memory" ('941, 2:37-55) is of no moment. The '941 figures exist to establish an indexing scheme and provide voltage mappings (like Dong Figs. 5a/g). EX1094, 174:24-175:10. Dong would be substantively no different if Figs. 5a-5h included a generic

“memory” label.⁵ Nor would the '941 patent change by labelling its figures “programming approach for a memory” instead of “memory ... operated in another condition.” '941, 2:38-39.

Dong Fig. 4's purpose is to “show[] a program disturb mechanism,” not limit Dong to any particular memory architecture. Dong, [0045]-[0046]. And Dong Figs. 5a-h depict “storage elements which are being programmed ... [in] selected NAND strings.” Dong, [0047]-[0048]. Certainly, in conjunction with Dong's “three dimensional” memory disclosure, a POSITA in 2020 would fairly read Dong's vertically-oriented Figs. 5a/g as disclosing vertical memory strings. Liu_Reply, ¶¶50-56. Regardless, 3D drawings are not required. *In re Bode*, 550 F.2d 656, 661 (C.C.P.A. 1977).

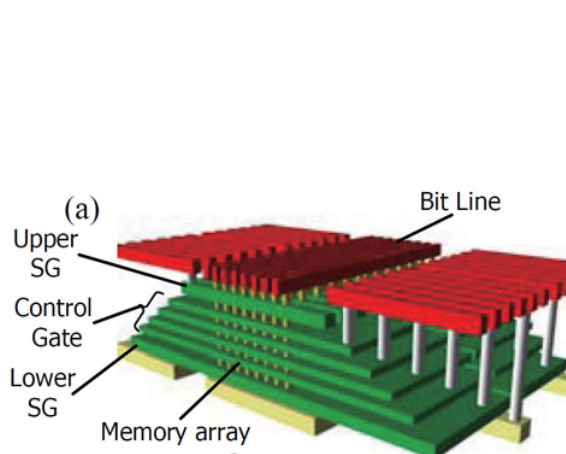
Second, even assuming POSITA knowledge/understanding vis-à-vis anticipation was assessed in 2007 (instead of 2020), PO loses because a POSITA in 2007 would have understood Dong's 3D disclosure to include vertical strings. Liu_Reply, ¶¶57-64. Multiple references confirm this. Endoh1 and Endoh2 show vertical strings in 2003 and 2001, respectively.

⁵ Regardless, Dong is replete with references to “memory.” See Dong.

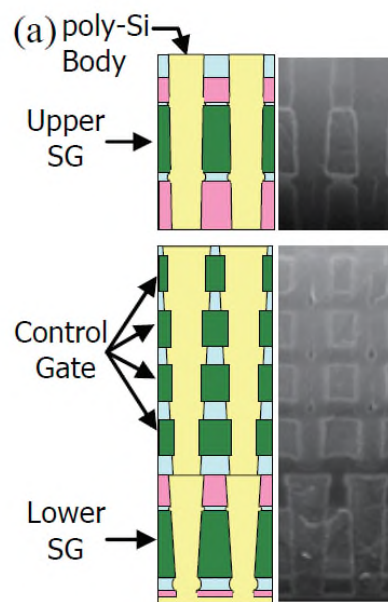


EX1101, Fig. 3(a)-(e), 2 (cells arranged “vertically in one silicon pillar”); EX1102 (similar).

Tanaka (from 2007) discloses vertical strings in 3D-memory (left), including a chip cross-section (right).

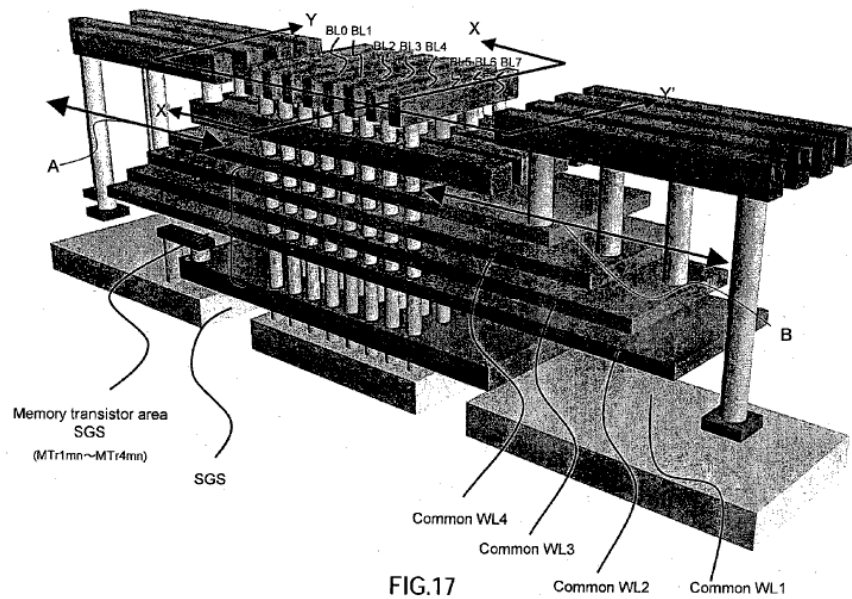


EX1075, Fig. 3(a)



EX1075, Fig. 7(a)

See *id.*, Figs. 4-6. Kito—filed in 2007—discloses a “semiconductor memory device ... in which memory cells are laminated in a ***three dimensional state***.” EX1087, Abstract.



EX1087, Fig. 17; *id.*, Figs. 1, 2-3 (vertical strings); EX1009, 28-29.

The notion that “three dimensional” vertical strings were unknown in 2007 is unsupported. It is irrelevant whether “Three-Dimensional (3D) NAND At The Time Of Dong ***Included*** Stacked 2D-NAND.” POR, 5-7, 42-44. What matters is that “three dimensional” memory included vertical strings.

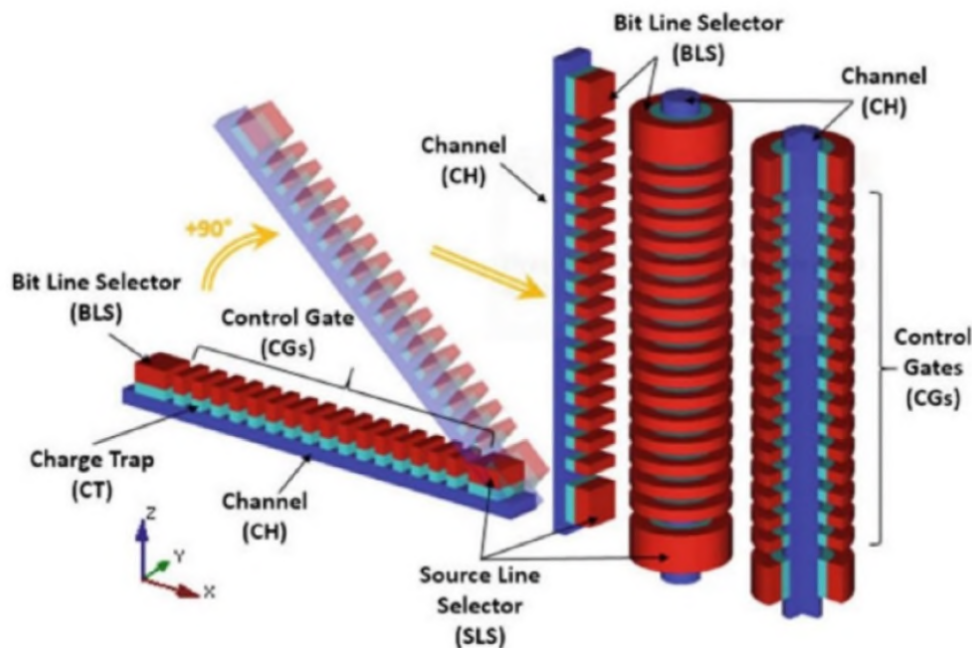
2. Obviousness Under PO’s Construction

a. PO’s Procedural Argument Fails

PO asserts that Petitioner “does not even contend that it would have been obvious” to use vertical 3D-NAND memory strings (POR, 2; *id.*, 45-47) and that “the Board improperly raised a new position.” POR, 45. PO’s accusations are

baseless. Although unnecessary, Petitioner argued obviousness anyway (as the Board properly recognized).

Ground 2 is “Dong renders obvious claims 1, 3, 5-7, 11, and 13 under §103.” Pet., 7. Quoting textbooks, the Petition explains 2D-to-3D NAND evolution, including the “many similarities between 2D- and 3D-NAND ..., including the techniques and algorithms used to program memory cells.” *Id.*, 12-14. The Petition quotes references explaining that “3D-NAND [] could be conceived by starting from the 2D-NAND string building block” and “turning the 2D-NAND string upside,” “resulting” in a “3D structure” with “vertical channel[s].” *Id.* (quoting EX1011, 3).

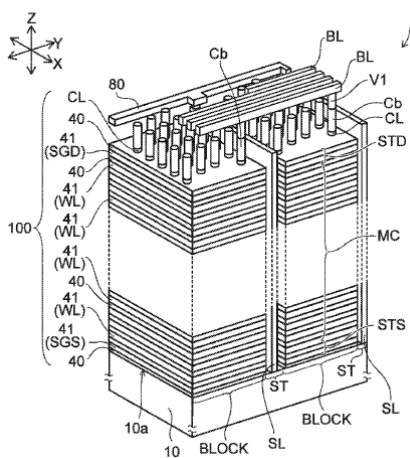


Pet., 13 (EX1010, 122); *id.*, 35 (citing Liu, ¶120 (“2D memory string would at a minimum render obvious the **bottom to top** requirement, even if narrowly construed”))).

Nevertheless, PO contends Petitioner did not argue obviousness. POR, 48. The Board already rejected this argument, and the Petition has not changed. ID, 20, 25-27. Moreover, if Petitioner never argued obviousness, PO would not have rebutted it. POR, 50-54.

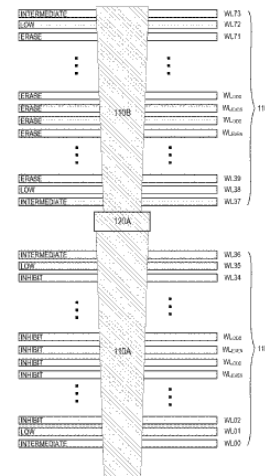
PO's assertion is belied by the Petition's holistic discussion of how "Dong anticipates and/or renders obvious claim 5." Pet., 29-33. The Petition explains it "would have been obvious" to use long memory strings, citing vertical 3D-NAND references like Sharai and Righetti. *Id.*, 31.

FIG. 1



Shirai, Fig. 1, [0019]

FIG. 6



Righetti, Fig. 6.

PO ignores this disclosure, which distinguishes 3M (POR, 48-49).

b. PO's Merits Arguments Fail

PO Focuses on the Wrong Disturb Modes. PO asserts a "POSITA would not apply [Dong's programming techniques] in vertical 3D-NAND" because "[p]rogram

disturb phenomena and mechanisms of [2D- and 3D-NAND] cell[s] are much different.” POR, 50 (quoting EX1009, 362). In relevant part, PO could not be more incorrect. Liu_Reply, ¶¶65-82. The Aritome textbook PO cites (EX1009) directly contradicts PO’s conclusion that Dong is inapplicable to 3D memory strings. Aritome §8.4.1 explains/compares/contrasts four program disturb modes—two “[c]onventional” modes present in both 2D and 3D memory, and two “[a]dditional” disturb modes only present in 3D-memory. EX1009, §8.4.1.

Conventional modes

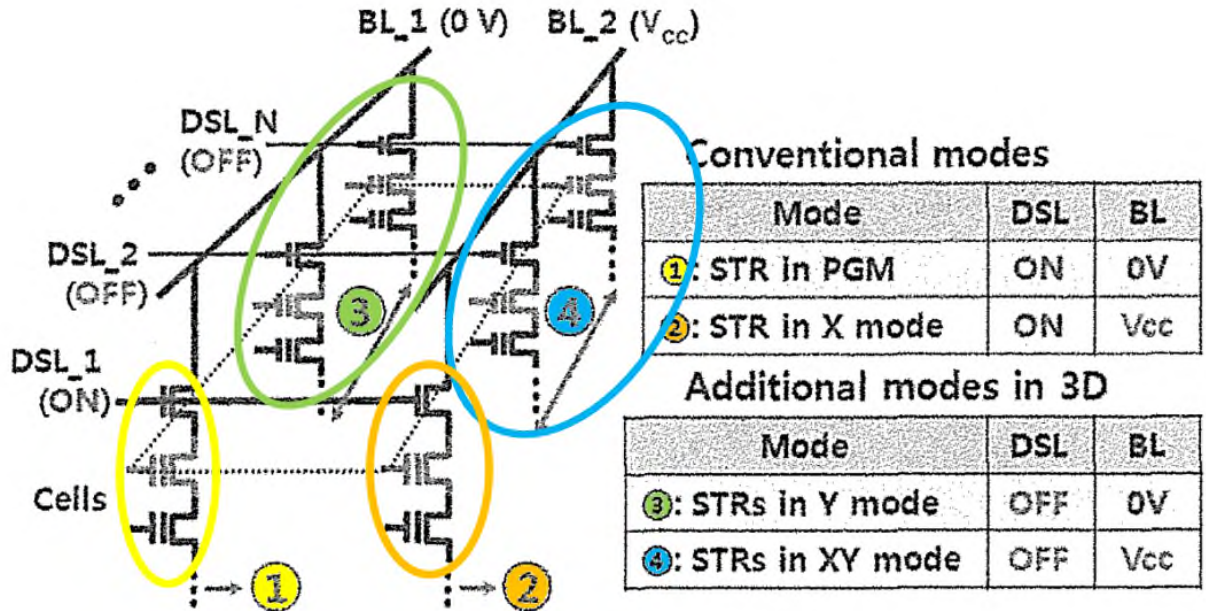
Mode	DSL	BL
①: STR in PGM	ON	0V
②: STR in X mode	ON	Vcc

Additional modes in 3D

Mode	DSL	BL
③: STRs in Y mode	OFF	0V
④: STRs in XY mode	OFF	Vcc

EX1009, Fig. 8.11 (excerpted). Aritome labels the four program disturb modes ①(PGM), ②(X-mode), ③(Y-mode), and ④(XY-mode), based on which memory

string(s) are affected. EX1009, 363, Fig. 8.11.⁶ Fig., 8.11 shows the string(s) where each mode manifests. Liu_Reply, ¶¶67-68.



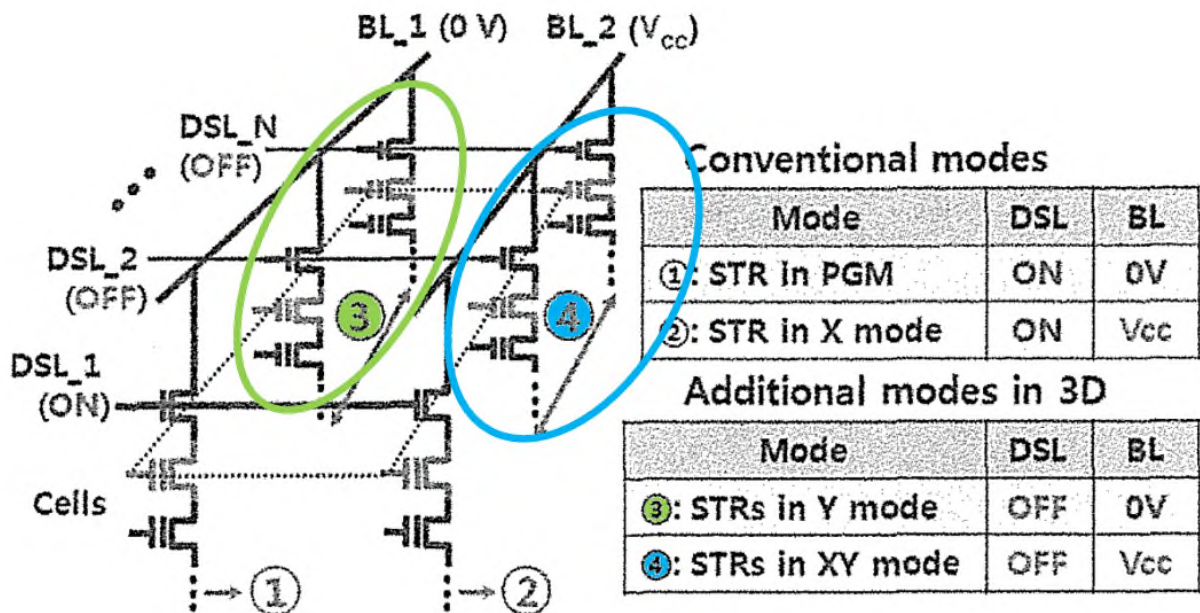
EX1009, Fig. 8.11 (annotated). Fig. 8.11's caption explains 3D-NAND adds "two new modes [called] Y-mode and XY-mode." in 3D-NAND. *Id.*

Per Aritome, "[c]onventional" disturb modes (①PGM and ②X modes) exist in 2D- and 3D-memory. EX1009, Fig. 8.11; *id.*, 363 ("Disturb X-mode is the same as a conventional program disturb mode in a 2D-NAND cell."); Fig. 2.22 (showing 2D-NAND "V_t shift of program disturb" in selected and unselected strings); Liu_Reply, ¶¶69-70. Dong addresses both modes. *Id.*, ¶72; Dong, [0011] ("Program

⁶ "STR" refers to "NAND [memory] string," "BL" is bitline, and DSL is drain select line/transistor. EX1009, 362.

disturb can occur at inhibited NAND string ... [and] the programmed NAND string itself"). Accordingly, even if Dong's program disturb solutions were made in the 2D-NAND context, they apply with equal (or greater) force to 3D-NAND to address the "[c]onventional" "PGM"① and "X-mode"② disturb. EX1009, 363; Liu_Reply, ¶71.

PO erroneously focused on *the wrong program disturb* modes (i.e., modes ③ and ④). Liu_Reply, ¶¶75-77. Aritome Fig. 8.11 shows Y-mode③ and XY-mode④ memory strings (where drain select line (DSL) is "OFF").



EX1009, Fig. 8-11 (annotated).

The Y-mode③ and XY-mode④ disturb solutions in 3D-NAND are **complementary** to (not replacements for) Dong's PGM① and X-mode② solutions, as Aritome Fig. 8.15 below shows. EX1009, 363-364; Liu_Reply, ¶¶66-77.

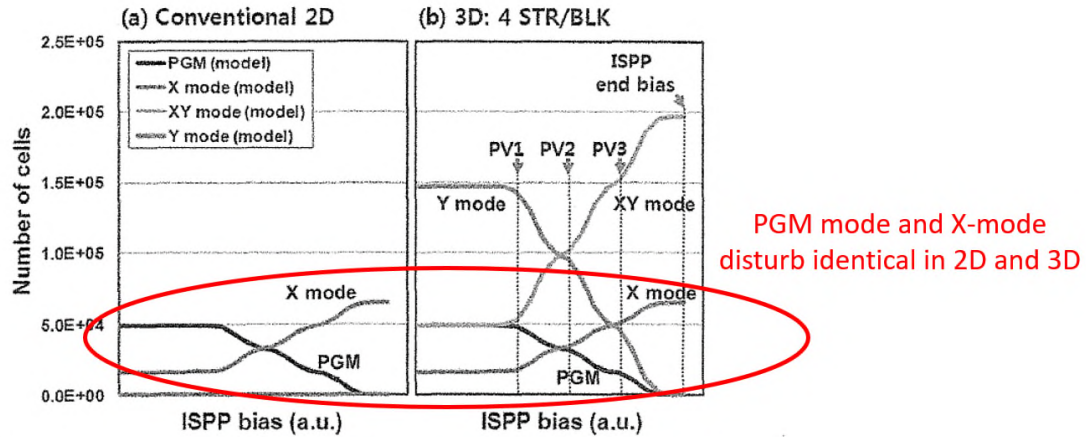


FIGURE 8.15 Probability (number of cells) of each program disturbance mode with increasing ISPP bias.

EX1009, Fig. 8.15 (annotated).

This is clear from Aritome, which proffers three solutions for the new disturb modes: “(1) high V_t of DSL, (2) applying negative bias to DSL, and (3) inserting dummy wordlines between DSL and edge wordline.” EX1009, 363-364. Because neither Dong nor the '941 patent disclose disturb solutions based on DSL (drain select) lines (or nearby dummy wordlines) (see EX1094, 297:14-23), they self-evidently address PGM^① and/or X-mode^②. Moreover, if Aritome's Y-mode^③ and XY-mode^④ solutions solved program disturb, the '941 patent would serve no purpose.

PO's "floating" body/channel/node arguments regarding EX2024-EX2027 fare no better.⁷ POR, 50-54. In fact, they support obviousness. In unselected memory strings sharing DSL with the selected memory string, the 2D and 3D disturb mechanism (*i.e.*, X-mode^② disturb) is the same, as Aritome states. EX1009, 363. But the lack of a grounded substrate (which PO's exhibits call "floating" body/channel/node) exacerbates program disturb. Liu_Reply, ¶¶78-81. Enhanced X-mode^② disturb makes Dong's teachings more (not less) applicable to 3D-NAND. *Id.* Moreover, if Dong Figs. 5a/g did not mitigate 3D program disturb, neither would the '941 patent's claimed programming schemes (which are identical to Dong Figs. 5a/g).

This also disposes of PO's nominal challenge that Petitioner's motivation to combine is too generic. POR, 47. But Petitioner discussed the "many similarities between 2D and 3D-NAND flash memory devices, including ***the techniques and algorithms used to program memory cells.***" Pet., 14-15; Liu, ¶¶56-62. As elaborated above, Aritome confirms the relevant disturb mechanisms (*viz.* "[c]onventional" PGM^① and X-mode^②) are the same for 2D- and 3D-memory. Liu, ¶¶61-62.

⁷ In relevant part, these exhibits (sharing Myounggon Kang as an author) are substantively similar.

PO Uses the Wrong Date for Evaluating Obviousness. PO's assertion that obviousness is assessed in 2007 (Dong's filing date) instead of 2020 ('941 priority date) contradicts the obviousness statute, which states that obviousness (including the scope and content of prior art and POSITA knowledge) is assessed at "the effective filing date of the claimed invention to a [POSITA]." 35 U.S.C. §103. The case law also squarely contradicts PO. *Amarin Pharma., Inc. v. Hikma Pharms. USA Inc.*, 449 F. Supp. 3d 967, 991 (D. Nev. 2020); IPR2016-00488, Paper 11, 29 (PTAB, July 18, 2016) ("obviousness is based on what the references would teach or suggest to POSITA at the time of the [challenged] patent filing—not at the time of filing of the [prior art] reference"). Thus, even if "three dimensional" memory did not connote (or render obvious) vertical strings in 2007 (which it did), it would have in 2020. Liu_Reply, ¶¶38-56.

PO Fails to Analyze Dong as a Whole. PO's obviousness section (POR, 50-54) is silent regarding Dong's "three dimensional" disclosure, which plainly suggests application to vertical strings. Dong, [0095]; *In re Snow*, 471 F.2d 1400, 1403 (C.C.P.A. 1973).

3. Enablement/Reasonable Expectation of Success

PO's nominal enablement/reasonable expectation of success argument (POR, 44; EX2028, ¶194) is woefully underdeveloped and fails at the outset. PO does not

even assert that 2D-NAND was not enabled or a POSITA lacked a reasonable expectation of success for 2D-NAND under Petitioner's **bottom-to-top** construction.

Regarding vertical memory strings, PO ignores POSITA knowledge—which is assessed in 2020, not 2007. *Oracle Am., Inc. v. Google, Inc.*, 606 F. App'x 990, 995 (Fed. Cir. 2015). Here, PO does not dispute Petitioner's level of skill in the art. Pet., 22-23; POR, 9; EX2028, ¶46; EX1100, ¶¶25-26. Any assertion that applying wordline voltages in vertical strings instead of horizontal ones requires undue experimentation lacks credibility. Liu_Reply, ¶¶83-87. Moreover, Dong is presumptively enabled. *In re Antor Media Corp.*, 689 F.3d 1282, 1288-89 (Fed. Cir. 2012). Although manufacturing vertical 3D-memory is not at issue (only programming a memory string is), the '941 patent itself presumes a POSITA can construct vertical 3D-memory. EX1087 (extensive manufacturing disclosure); EX1075, Fig. 7(a)-(c) (manufactured device).

IV. GROUND 3

A. Ground 3 Renders Obvious **“the first voltage has a first level if the xth word line is in the first portion”** (Liu_Reply, ¶¶88-96)

Tellingly, PO does not dispute that Costa discloses that the pass voltage applied to unselected cells “depend[s] upon the position of the selected memory cell,” and increases “[a]s programming progresses” across the string. Costa, Abstract; Liu_Reply, ¶¶88-90.

Instead, PO asserts that “Petitioner’s application of Dong to independent claim 5 fails when carried forward to address claims 8 and 9.” POR, 55. This argument fails because PO ignores that Petitioner’s invalidity analysis was not limited to programming the fourth wordline (viz., $x=4$).⁸ Pet., 33 (“[T]hese mappings are merely exemplary and other mappings also satisfy [claim 5]”).

Dong discloses that “programming continues sequentially until all memory cells ... are programmed.” Pet. 31; *id.*, 62, 34 (quoting Dong, [0048]); Dong, Fig. 10, [0089]. Costa teaches the same. Costa, Abstract (“programming progresses [through all memory string cells]”). Thus, all cells/wordlines in the Dong/Costa combination would be programmed. This necessarily includes all cells in the *first*, *second*, and *third portion[s]*. Nor would it make sense to constrain Petitioner’s analysis to just the example provided for claims 5 and 7 (where $k=2$, $m=7$, $x=4$, and $n=32$) when claims 8-9 refer to programming wordlines in each of the *first*, *second*, and/or *third portion[s]*.

Regardless, numerous examples satisfy claims 5 and 7-9. As the Petition explained, “Costa’s zones/range correspond to the claimed portions in the ’941

⁸ Cabining Petitioner’s invalidity theory as PO proposes creates a double standard because the ’941 patent lacks any concrete examples. *In re Epstein*, 32 F.3d 1559, 1568 (Fed. Cir. 1994).

patent” and “Costa provides ‘a simple example,’ where ‘a NAND string [is divided] into two equal-sized zones.’” Pet., 75 (quoting Costa, [0115]). Applying this arrangement from the Petition to Dong (Pet., 75-76), the *first* and *second portion[s]* each have 16 wordlines (meaning *k*=16 and *m*=32) as shown below, with one exemplary wordline programmed in each portion (viz., *x*=4 (*first portion*) and *x*=20 (*second portion*)).

		VSGD			
Second Portion	WL31	(Vpass)	(Vpass)	m=32	
	WL30	(Vpass)	(Vpass)		
	WL29	(Vpass)	(Vpass)		
	WL28	(Vpass)	(Vpass)		
	WL27	(Vpass)	(Vpass)		
	WL26	(Vpass)	(Vpass)		
	WL25	(Vpass)	(Vpass)		
	WL24	(Vpass)	(Vpass)		
	WL23	(Vpass)	(Vpass)		
	WL22	(Vpass)	(Vpass)		
	WL21	(Vpass)	(Vpass)		
	WL20	(Vpass)	V3 (Vpass)		X+1
	WL19	(Vpass)	VPGM		X=20
	WL18	(Vpass)	V2 (Viso)		X-1
	WL17	(Vpass)	V1 (Vpass)		X-2
First Portion	WL16	(Vpass)	V1 (Vpass)	k=16	
	WL15	(Vpass)	V1 (Vpass)		
	WL14	(Vpass)	V1 (Vpass)		
	WL13	(Vpass)	V1 (Vpass)		
	WL12	(Vpass)	V1 (Vpass)		
	WL11	(Vpass)	V1 (Vpass)		
	WL10	(Vpass)	V1 (Vpass)		
	WL9	(Vpass)	V1 (Vpass)		
	WL8	(Vpass)	V1 (Vpass)		
	WL7	(Vpass)	V1 (Vpass)		
	WL6	(Vpass)	V1 (Vpass)		
	WL5	(Vpass)	V1 (Vpass)		X+2
	WL4	V3 (Vpass)	V1 (Vpass)		X+1
	WL3	VPGM	V1 (Vpass)		X=4
	WL2	V2 (Viso)	V1 (Vpass)		X-1
	WL1	V1 (Vpass)	V1 (Vpass)		X-2
	WL0	V1 (Vpass)	V1 (Vpass)		
		VSGS			

Dong, Fig. 5a (modified and annotated). The red text shows the applied voltages (per Dong Fig. 5a) when $x=4$ (viz., *first portion* wordline programmed) and the blue text shows the applied voltages (per Dong Fig. 5a) when $x=20$ (viz., *second portion*

wordline programmed). This satisfies all conditions of claims 5 and 9, as do other examples. Liu_Reply, ¶¶91-94.

Claim 8 (via dependency on claim 7) requires a *third portion* that *comprises an (m+1)th word line to an nth word* and *applying a fourth voltage to the (x+2)th word line to the nth word line*. As the Petition discussed, “Costa expressly discloses that ‘the size of the zones may not be equal ... [and] more than two zones may be used.’”). Pet., 76 (quoting Costa, [0116]). Designating another “zone” in Dong Fig. 5a (per Costa’s teachings) results in a *third portion*, shown below (where *k*=16, *m*=24, and *n*=32). Here, one exemplary wordline is programmed in each portion (viz. *x*=4 (*first portion*), *x*=20 (*second portion*), and *x*=29 (*third portion*)). This satisfies all conditions of claim 8 (and base claims 5 and 7), as do other examples. Liu_Reply, ¶¶95-96.

VSGD			
WL31	(Vpass)	(Vpass)	V4 (Vpass) n=32
WL30	(Vpass)	(Vpass)	V4 (Vpass) X+2
WL29	(Vpass)	(Vpass)	V3 (Vpass) X+1
WL28	(Vpass)	(Vpass)	VPGM X=29
WL27	(Vpass)	(Vpass)	V2 (Viso) X-1
WL26	(Vpass)	(Vpass)	V1 (Vpass) X-2
WL25	(Vpass)	(Vpass)	V1 (Vpass)
WL24	(Vpass)	(Vpass)	V1 (Vpass)
WL23	(Vpass)	(Vpass)	V1 (Vpass) m=24
WL22	(Vpass)	(Vpass)	V1 (Vpass)
WL21	(Vpass)	(Vpass)	V1 (Vpass) X+2
WL20	(Vpass)	V3 (Vpass)	V1 (Vpass) X+1
WL19	(Vpass)	VPGM	V1 (Vpass) X=20
WL18	(Vpass)	V2 (Viso)	V1 (Vpass) X-1
WL17	(Vpass)	V1 (Vpass)	V1 (Vpass) X-2
WL16	(Vpass)	V1 (Vpass)	V1 (Vpass)
WL15	(Vpass)	V1 (Vpass)	V1 (Vpass) k=16
WL14	(Vpass)	V1 (Vpass)	V1 (Vpass)
WL13	(Vpass)	V1 (Vpass)	V1 (Vpass)
WL12	(Vpass)	V1 (Vpass)	V1 (Vpass)
WL11	(Vpass)	V1 (Vpass)	V1 (Vpass)
WL10	(Vpass)	V1 (Vpass)	V1 (Vpass)
WL9	(Vpass)	V1 (Vpass)	V1 (Vpass)
WL8	(Vpass)	V1 (Vpass)	V1 (Vpass)
WL7	(Vpass)	V1 (Vpass)	V1 (Vpass)
WL6	(Vpass)	V1 (Vpass)	V1 (Vpass)
WL5	(Vpass)	V1 (Vpass)	V1 (Vpass) X+2
WL4	V3 (Vpass)	V1 (Vpass)	V1 (Vpass) X+1
WL3	VPGM	V1 (Vpass)	V1 (Vpass) X=4
WL2	V2 (Viso)	V1 (Vpass)	V1 (Vpass) X-1
WL1	V1 (Vpass)	V1 (Vpass)	V1 (Vpass) X-2
WL0	V1 (Vpass)	V1 (Vpass)	V1 (Vpass)
VSGS			

Dong, Fig. 5a (modified and annotated).

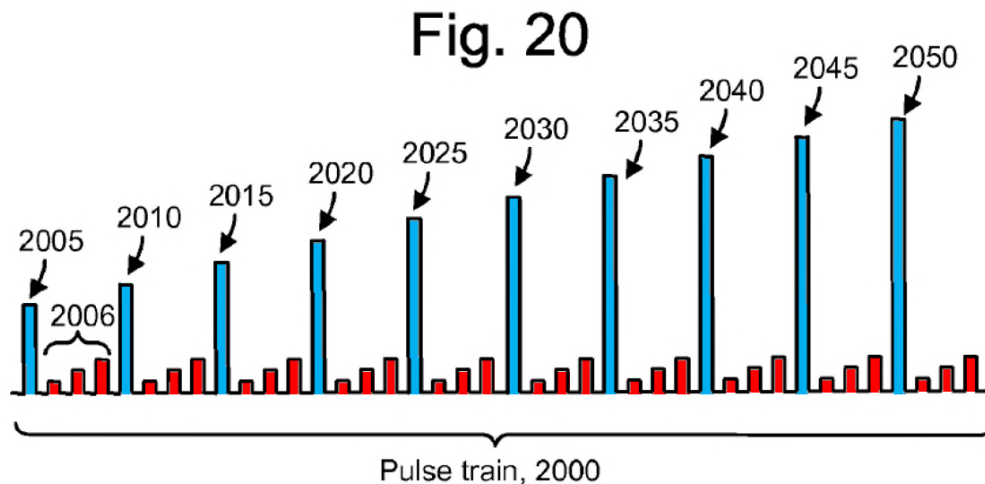
Although the '941 patent provides no concrete examples (and the claims do not require one), Petitioner did. The Board should reject PO's attempt to artificially cabin Petitioner's invalidity theory. PO ignores numerous assertions in the Petition

(regarding both Dong and Costa) to construct a strawman argument that “Petitioner’s application of Dong to independent claim 5 fails when carried forward to address claims 8 and 9.” POR, 55. PO has it backwards—the question is not whether the claim 5 example “carr[ies] forward” (*id.*), but whether Petitioner’s invalidity assertions for claims 8-9 satisfy base claims 5 and 7. They plainly do.

B. Ground 3 Satisfies “*Applying a First Voltage*” Under the Correct “*Program Operation*” Interpretation (Liu_Reply, ¶¶97-103)

Costa undisputedly discloses that the pass voltage applied to unselected cells “depend[s] upon the position of the selected memory cell,” and increases “[a]s programming progresses.” Costa, Abstract. Under PO’s construction, this satisfies the *first voltage* requirement (viz., that *the first [voltage] level is lower than the second [voltage] level, and the second [voltage] level is lower than the third [voltage] level*. ’941, cl.8.

Dong Fig. 20’s “pulse train 2000”—applied to Dong’s wordlines “*during programming*”—includes charge injection pulses 2005, 2010, etc. (blue) *and* “verify pulses 2006” (red). Dong, [0132]. The pulse sequence below programs one cell and constitutes one *program operation*, not ten. Liu_Reply, ¶99.



Dong, Fig. 20 (annotated), [0132].

Faced with this, PO argues no motivation to combine “because Dong already discloses [] verification.” POR, 65. Under PO’s flawed logic, the mere existence of one approach in a primary reference forecloses obviousness. That is not the law. *Univ. of Md. Biotechnology Inst. v. Presens Precision Sensing GmbH*, 711 F. App’x 1007, 1011 (Fed. Cir. 2017).

PO misframes Petitioner’s argument by stating that Petitioner relied on “silence” for motivation to combine. POR, 66. Not so. Petitioner relied on Costa’s disclosure of an improved programming method that mitigates channel resistance increase. Pet., 72-73; Liu_Reply, ¶¶100-13. This is quintessential application of *KSR*. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 405 (2007). The Petition noted “Dong is silent regarding how V_{PASS} ... change[s]” (Pet., 72) to dispel any notion that Dong teaches away.

Even if PO were correct that Costa “does not focus on program disturb” (POR, 66), a POSITA would still combine Costa’s channel resistance solution to improve Dong’s **verification phase**. Pet., 70-74. Petitioner’s head-in-the-sand approach that ignores verification is not credible.

PO erroneously contends that Petitioner “applie[d] Dong’s V_{PASS} —used in a program phase—as the ‘first voltage.’” POR, 64. Even if true, this is irrelevant. V_{pass} is applied both during charge injection (Dong, Fig. 5a) and verification (Costa, Abstract). Even if Dong’s V_{pass} voltage (during charge injection) differed from Costa’s (during verification), nothing in the claim prohibits that (or requires they be the same). What matters is that at any given point during a **program operation**, the specified wordlines (i.e., **the first wordline to an $(x-2)$ th wordline**) have a common **first voltage** applied to them (not that the voltage never change).

V. GROUND 4

A. PO’s “ $V_{PASS-LOW}$ ” Arguments Fail (Liu_Reply, ¶¶104-114)

PO’s “ $V_{PASS-LOW}$ ” argument cannot apply to claim 10 because Petitioner’s claim 10 analysis relies on Dong Fig. 5a, which lacks “ $V_{PASS-LOW}$.” Dong, Fig. 5a; Liu_Reply, ¶104. PO’s “ $V_{PASS-LOW}$ ” arguments for claims 4 and 14 are premised on assertions Petitioner never made, improper bodily incorporation, and non-existent claim limitations. *Intel Corp. v. Pact XPP Schweiz AG*, 2023 U.S. App. LEXIS 4436, at *6 (Fed. Cir., 2023) (“test for obviousness is not ... bodily incorporat[ion]”).

PO argues Petitioner “never explains how or why a POSITA would omit V_{ISO} (or V_{LOW})” in the Dong/Shirai combination. POR, 70. That is because Petitioner never proposed doing so. POR, 70; EX2028, ¶256 (both lacking cites). But even if V_{ISO} and/or V_{LOW} were omitted as PO suggests (such that $V_{PASS-LOW}$ extended through all wordlines in the lower deck of the Dong/Shirai combination), that mapping still satisfies claims 4 and 14 (and their underlying independent claims) and is consistent with Dong’s teaching to “gradually reducing the bias voltage” over the channel of multiple wordlines. Dong, [0057]; Liu_Reply, ¶105. In such a circumstance, the “gradual” voltage reduction would still be accomplished by the $V_{PASS-HIGH}$ (on WL11), $V_{PASS-MEDIUM}$ (on WL10), and $V_{PASS-LOW}$ voltages (on WL9 to WL0). *Id.*

Next, like Ground 3, PO attempts to cabin Petitioner (POR, 66-69) by carrying forward a singular example from independent claims 1 and 11 (with single-wordline **second portion[s]**) to dependent claims 4 and 14 (with multi-wordline **second portion[s]**). But, as the Petition noted, the single-wordline analysis was “exemplary and other mappings also satisfy the claim.” Pet., 51. Elsewhere, PO swings to the other extreme, admitting that “Shirai’s Figure 2” “appears to comprise [9 wordlines],” and contending the combination’s **second portion** is necessarily exactly 9-wordlines (*i.e.*, bodily incorporation). POR, 68-69. PO’s arguments are

inconsistent and cannot limit Petitioner's analysis. Shirai, [0030] (disclosing "any number of stacked layers").

Like the claims, Petitioner's invalidity theory applies more broadly. Claims 4 and 14 (and their base claims) do not recite a minimum or maximum wordline count for the *second portion*, nor did Petitioner impose such a restriction on Dong/Shirai. EX1094, 233:16-19. Claims 4 and 14 do not require the *second portion* and memory deck be co-extensive, only that *the memory has a two-deck structure* (e.g., the *second portion* could be a subset of the lower memory deck). '941, cls. 4, 14. At bottom, PO's gripe is that it claimed too broadly.

Even in figures reflecting a multi-wordline *second portion* (Pet., 83), Petitioner was not bodily incorporating Shirai Fig. 2 (or any specific number of wordlines), but showing dummy wordlines and an oxide layer between *portions*. Regardless, the single-wordline *second portion* example (left, Liu_Reply, ¶¶106-108) and multi-wordline *second portion* example (right, Liu_Reply, ¶¶109-113) for claims 4 and 14 satisfy their base claims, as do other examples (Liu_Reply, ¶114).



Dong, Fig. 5g (modified and annotated).

PO's assertion against "apply[ing] Dong's voltage scheme for a single wordline ($V_{\text{PASS-LOW}}$) to [Shirai's Lower Memory Deck 100a]" (POR, 68-69) rehashes previous arguments and fails for the same reasons. Putting aside that Dong expressly discloses applying $V_{\text{PASS-LOW}}$ precisely as claimed (*viz.*, to the **second portion**), PO's assertion against applying $V_{\text{PASS-LOW}}$ is premised on bodily incorporation. And it contradicts Dong's teaching that "increasing the number of wordlines in between the selected wordline and the V_{ISO} wordline" reduces program disturb "by gradually reducing the [] voltage." Dong, [0057] (" $V_{\text{PGM}} > V_{\text{PASS-HIGH}} > V_{\text{PASS-MEDIUM}} > V_{\text{PASS-LOW}} > V_{\text{LOW}} > V_{\text{ISO}}$ "); *id.*, [0080]-[0084] (describing "even

more gradual transition from V_{PGM2} to V_{ISO} over one or more intermediate wordlines"); Fig. 5g.

A wordline voltage mapping with multiple adjacent $V_{\text{PASS-LOW}}$ wordlines (*e.g.*, in the **second portion**) would achieve Dong's "even more gradual" voltage transition. Liu_Reply, ¶¶109-113. Thus, Dong fully supports applying $V_{\text{PASS-LOW}}$ to multiple wordlines. Any stricture PO imposes on minor adjustments like this runs headlong into *KSR*'s teaching that "[a POSITA] is also a person of ordinary creativity, not an automaton." *KSR*, 550 U.S. at 421.

B. Ground 4 Renders Claim 10 Unpatentable

PO's argument that Petitioner did not "apply [the] prior art" to claim 10 is disingenuous. POR, 71. Petitioner's statement that claims 10 and 4 are "met for the same reasons" (Pet., 83) plainly referred to the **new limitations** of those claims, not the base claims. PO's suggestion that Petitioner swapped Figs. 5a and 5g is baseless.

C. PO's Strawman "k**" Argument (Liu_Reply, ¶¶115-118)**

PO argues Ground 4 fails because it uses "different interpretation[s]" of **k** for the dependent claims. POR, 71-73. This argument misreads the Petition and relies on the same false premise (debunked in §§IV.A, V.A) that Petitioner's independent claim analysis was limited to one specific example. Liu_Reply, ¶115. Requiring Petitioner to provide **k**, **m**, and **x** values when the '941 patent does not would create a double standard. *In re Paulsen*, 30 F.3d 1475, 1481 n.9 (Fed. Cir. 1994).

Regardless, the §V.A example above for claims 4 and 14 where $k=9$ debunks PO's argument that Petitioner mixed-and-matched different k values (*i.e.*, “ k equals 9” for base claims 1 and 11 and “ k equal to 0” for dependent claims 4 and 14). POR, 71; Liu_Reply, ¶116. Further, in the example above for claims for 4 and 14 where $k=8$ (with $V_{\text{PASS-LOW}}$ applied to WL8), carrying that analysis back to the underlying independent claims 1 and 11 works just fine. Liu_Reply, ¶¶117-118. The same rationale explained for claims 4 and 14 defeats PO's substantially similar mix-and-match argument for claim 10. *Id.*; POR, 71-72.

D. Dong/Shirai Are Properly Combined

PO's argument against combining Dong/Shirai (POR, 73) fails because: (1) it depends on the false premise that Dong “does not disclose vertical 3D-NAND” (POR, 73), which §III.B.1 explains is incorrect; and (2) even if Dong did not disclose 3D-NAND, Dong's techniques for reducing program disturb (*viz.*, PGM and X-mode) apply equally to 3D-NAND (Pet., 12-15, 77-80; §III.B.2.b).

VI. CONCLUSION

The Board should find the Challenged Claims unpatentable.

Respectfully submitted,

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Dated: February 10, 2026

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITIONER'S REPLY BRIEF complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 5,599 words.

Dated: February 10, 2026

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