UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

vs.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case No. IPR2025-00190
U.S. Patent No. 11,568,941

REMOTE DEPOSITION OF DR. SUNIL KHATRI

Tuesday, January 27, 2026

8:59 a.m. (MST)

Reported by:

Jaclyn Urzia, RPR, CRR

Job No. 2025-1008399

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Deposition of STEPHEN CAMPBELL, held remotely via Zoom, before Jaclyn Urzia, a Registered Professional Reporter, Certified Stenographic Realtime Reporter and Notary Public.

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SUNIL KHATRI,

called as a witness, having been duly sworn/affirmed by a Notary Public, was examined and testified as follows:

EXAMINATION BY

MR. JENSEN:

Q Good morning, Doctor.

My name is Travis Jensen, and I represent the petitioner in the IPR proceeding at issue today, which is captioned IPR 2025-00190, and I will be taking your deposition.

A Okay.

Q Could you state and spell your name, please?

A My name is Sunil Khatri, and that's spelled S-U-N-I-L, and the last name is Khatri, K-H-A-T-R-I.

MR. LOWRY: And, Travis, sorry to interrupt, but I just wanted to make an appearance on the record.

My name is Rich Lowry of Latham & Watkins on behalf of patent owner YMTC.

Thank you.

BY MR. JENSEN:

Q Dr. Khatri, where do you normally reside?

A I normally reside in College Station, Texas.

Q Where are you located today?

A I am in Boulder, Colorado today.

Q Is anyone else with you physically?

A No. I'm by myself.

Q Now, approximately how many times have you been deposed as an expert witness?

A I would say that it's probably in the range of 30 to 40 times.

Q Were those primarily patent cases?

A I'd say maybe they'll all patent cases. It's just a guess. I'm almost sure that that's the case, yeah.

Q And we had sent over a set of exhibits so you could have them available locally.

Were you able to download a copy

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of those?

A Yes. I did download the -- you know, the bundle of exhibits that you all sent, and I have them open in a folder on my computer.

Q Okay.

A So in other words, I have in my computer the Zoom screen, and to the right of it, I have, you know, the folders where all the -- you know, where the exhibits are.

Q Okay. Great. Thank you for confirming that.

Let's just look at one of those and I can show it on the screen as well, but I'd like to pull up Exhibit 1001, which is US Patent 11,568,941.

A Let me see. I've doubled clicked it. I guess I'm waiting for it to open.

It just opened. And just one second, my PDF app wants me to log in. So I'll just do that.

Just one second.

Q Sure.

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A Just a second. Oops.

I'll just log in so that it won't bother us for the rest of the day.

All right. I'm logged in, and I have a local copy of it open, and I also see your copy on the screen.

Q Okay. Yeah, I was going to ask you about that as well, I just wanted to test and see if the screen share was working as well, so --

A Yeah.

Q -- that -- we may use that throughout the deposition, but I wanted to make sure you had access to a local copy as well.

A You're certainly welcome to use that screen share. I'll be -- you know, I'd like to follow it -- follow along on my local copy, so...

Q All right. So looking at Exhibit 1001, do you recognize Exhibit 1001 as the challenged patent in this IPR?

A Yes, I do see this exhibit, the '941 Patent, and it's the challenged patent.

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Q Have you ever been deposed on the '941 Patent before?

A So I was deposed, you know, some months ago about -- you know, in relation to this IPR for a claim construction sort of situation.

Q Okay. You can put that exhibit to the side for the moment.

A Okay.

Q Dr. Khatri, do you understand that you are giving testimony today for an IPR proceeding?

A That's correct. I understand that.

Q Is there any reason you cannot give truthful testimony today?

A No, there is not.

Q Even though you've been deposed a number of times before, I'd like to just briefly review a few basics of how the deposition works so we're on the same page.

Today's deposition is being conducted virtually.

Will you let me know if you experience any technical difficulties so we

can work those out?

A Absolutely.

Q And you said you got the copy of the local exhibits that we had provided?

A Yes. I got a copy of the local exhibits. It had two folders, which one of them said Micron exhibits, I think, and the other was YMTC exhibits.

Q Yeah. And if we end up using any other exhibits that aren't in those folders, I'll share them in the Zoom chat feature.

A Okay.

Q For the benefit of the court reporter, can you provide oral questions -- or, excuse me, oral answers to my questions?

A Yes, I can do that.

Q If you find any of my questions unclear, will you let me know so I can try to clarify it or rephrase?

A I can do that.

Q Throughout the course of the deposition, counsel for patent owner may object.

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If he does so, he's objecting to my question, not your answer. However, unless you are instructed by your counsel not to answer on the basis of privilege, you must still answer the question.

Do you understand that?

A Yes, I do understand that.

Q Perhaps most importantly, we'll be taking periodic breaks today. If at any time you'd like a break, just let me know, and we'll do our best to accommodate as long as there's not a question pending.

A That sounds fair.

Q Apart from the Zoom program and the folder with the exhibits, do you have any other applications open on your computer?

A No. Let me just double-check, but no, I can confirm there's nothing else open on my computer.

Q Do you have any hard copy files or materials with you?

A Yes. So what I did is, I think just like the last time I was deposed in a YMTC matter, I have a copy of the '941

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Patent, which is unmarked and clean.
That's one hard copy document on my table.
The other hard copy document on my table is my declaration in support of the patent owner response.
So I have these two documents on my table in front of me.
Q And you mentioned a company called YMTC.
Do you recognize them as the patent owner in this case?
A Actually, if I looked at the patent and I looked at the assignee, it lists Yangtze Memory Technologies Company, which is the YMTC, the owner of the patent, I guess.
Q Before being contacted about this case, had you ever heard of YMTC?
A I mean, I -- you know, in my general reading about technology and where things are going and memory technology in particular, you know, I had come across the name, but I wasn't intimately familiar with what they did.
Q Before being contacted about

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this case, had you ever heard of the '941 Patent?

A No, I was not aware of the '941 Patent before the case started.

Q So there are three prior art references that form the basis of the challenge or the grounds in this patent. So let's just make sure we've got all those in hand here.

Can you pull up Exhibit 1005, which is the Dong reference?

A Let me do that. Hold on.

Okay. I have the Dong reference open. I think it's a patent ending in '008.

Do you want me to keep it open or do you want me to just open it and check if it opens?

Q No, we can look at this for just a moment here.

Do you see where it lists the inventors on the Dong reference?

A Yes. Let me see, the inventors are Yingda Dong from Sunnyvale and Jeffrey Lutze from San Jose, Shih-Chung Lee from

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Yokohama City in Japan and Gerrit Jan Hemink in Yokohama, Japan again and Ken Oowada in Kanagawa, Japan.

Q Do you know any of those individuals?

A No, I do not know them, any of them.

Q Do you know any of the inventors listed on the face of the '941 Patent?

A I'm sorry, can you repeat the question?

Q Do you know any of the inventors listed on the face of the '941 Patent?

A Oh, of the '941 Patent, okay.

I don't believe so, but let me double-check. So I'm going to open the '941 Patent really quick. And then I'll close it back after that, of course.

The inventors are Yali Song from Wuhan, China and then XiangNan Jhao from Wuhan again and Ying Cui from Wuhan, and I don't know any of them.

Q Next let's go to Exhibit 1012.

A Okay. I'm going to close these two. Is that good?

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Q That's okay.
A Okay. I mean, to the extent possible, I'll just close them so that there's less clutter on the desktop, you know.
And now you said what, 1000 what, 2?
Q 1012.
A 12. Hold on.
Okay, 1012 is -- I'm opening it.
And I have 1012 open now.
Q And do you recognize Exhibit 1012 as the Costa reference used in the -- to challenge the '941 Patent?
A Let me double-check really quick and look at it, if there are some portions of it that will trigger my recollection.
Yeah. Okay. So yes, this, Exhibit 1012, is the Costa reference, which is a patent ending in '667.
Q And you said this is one of the references that is used as part of the combination to challenge the '941 Patent?
MR. LOWRY: Objection to form.
A This reference was used by the

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petitioner, you know, in the petition and also by Dr. Liu.

Q Okay. Do you know the named inventor on the Costa reference?

A In the Costa reference, there is one inventor, and their name is Xiying Costa from San Jose, and I do not know them.

Q Can you open Exhibit 1018?

A Just one second.

Okay. Yes, I have Exhibit 1018 open.

Q And the first named inventor on that reference is Kaito Shirai, is that correct?

A Let me see.

Yes, it's Kaito Shirai from Japan.

Q Do you know that individual or any of the other inventors listed on the Shirai reference?

MR. LOWRY: Objection to form.

A I'm looking at all the names. I'm just going to read them all, like Kaito Shirai from Japan, Hideto Takekida from

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Nagoya, Tatsuo Izumi, Reiko Shamoto from Nagoya again, and Takahisa Kanemura from Yokohama, and Shigeo Kondo from Yokkaichi, Japan.

So I don't know of -- I don't know any of these individuals, you know, either professionally or personally.

Q Okay. You can put those exhibits to the side for now.

A Okay.

Q Other than your work on this proceeding, do you know Dr. David Liu, the Micron expert?

A No, I don't believe I know him. I might have met him in passing or something, but I don't know him as such.

Q Are you aware that there is a related district court case involving the '941 Patent?

A I mean, you know, generally, whenever there's an IPR, I kind of -- you know, usually there's a related district court case.

So I am assuming there is a case. You know, I don't know further

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details about it.

Q Have you done any work in the district court case on the '941 Patent?

MR. LOWRY: Objection to form.

A So if you -- I mean, I think I had mentioned that I had done -- I had been deposed for the claim construction, you know, for the '941, and I assume that that was for a third district court case.

Now, that was several months ago, so I don't recall the details, but I'm assuming it was a district court case which it was -- you know, which it was for.

Q Give me just a moment.

Okay. Thank you for your patience.

A Of course.

Q I just dropped an exhibit into the chat. It starts with the file name Exhibit 1100.

A Let me open that really quick.

I see the realtime thing. I don't see anything else in the chat.

Am I looking in the right place?

In the chat, I see something

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that says: "Click link below to join" --
oh, there we go. Now I see something.
Q Yeah, it might have taken just a moment to upload.
A Yeah, it probably did take a little while.
Okay. Let me open that and see if it opens.
I have clicked it, but it's -- hold on. Let's see...
Okay. It wants me to save this, and I'm going to try to save it in the same -- in a folder that's relating to this.
If you don't mind, I'm just going to create a folder for any new exhibits.
Q Yeah, that's fine.
A And if you give me a minute, I'll just do that. And then hopefully all of the exhibits you point me to will drop into that folder.
Let's try this again.
Just one second. I'm having some troubles, you know, with my computer.

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All right. I did -- all right. I got this new exhibit, and I have put it in my -- in this little area -- in this little folder that I have for new exhibits.

Now -- and I also have this new exhibit open.

May I -- I mean, did you have a question about it?

Q Yeah. So my question is: What is the Exhibit 1100?

A So Exhibit 1100 is the declaration -- is the declaration I was mentioning to you a little bit earlier, the declaration in support of that claim construction.

And if you look at the last page of it, this was about a year ago, on the 31st of January 2025.

Q And what is the date that you signed your declaration in Exhibit 1100?

A So if I go to the last page of this exhibit, it says executed on the 31st day of January 2025.

That's about a year ago.

Q Was Exhibit 1100 submitted for

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the purpose of claim construction in the '941 Patent?

MR. LOWRY: Objection to form.

A So if you look at -- I mean, if you look at the first line, I guess -- I mean, sorry, the first paragraph of the Exhibit 1100, it says that I've been retained on behalf of YMTC and its counsel, Latham & Watkins LLP, to serve as a technical expert and provide expert opinions relating to U.S. Patent 11,568,941, the asserted patent.

And so, you know, it's certainly relating to the '941 Patent.

Q And could you read paragraph 2 out loud?

A Sure.

Paragraph 2 says: "I have been asked to provide testimony and my opinions regarding certain disputed claim construction issues with respect to the '941 Patent."

Q What claim terms did you construe in Exhibit 1100?

MR. LOWRY: Objection to form.

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A So if we look at this exhibit, we kind of go down the exhibit, you know, it's -- you know, it has a Section II, which says: "Legal Principles."

And then a section of III -- Section III, which is "Level of Ordinary Skill in the Art."

Section IV is "Materials Considered."

And then Section V says: "Claim Construction." And Section VA talks about the claim -- the construction for "from bottom to top" that is listed here.

And that's the only section which has a claim construction -- I mean, that's the only section under -- subsection under Section V.

Q Is the claim term "from bottom to top" that you construed in Exhibit 1100 one of the claim terms that is at issue in the IPR proceeding on the '941 Patent?

A Well, you know, if you -- if I -- I'm going to like open my '941 Patent -- I'm sorry, my '941 Patent declaration, if you give me one second.

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Let's see...

That's -- I forget what exhibit that is.

Okay. Hold on. It's not in the Micron exhibits.

I think it's 2006, if I'm not mistaken -- no, it's not 2006.

Sorry, I'm kind of navigating my way through these exhibits here.

Q Let's come back to this question. Let me maybe help you out here.

How many declarations did you prepare for this IPR proceeding?

A Sorry, when you say, "prepare," do you mean, you know, did I prepare, you know, for today's deposition on? Or you mean just produce or write?

What did you --

Q Yeah, how many declarations did you submit for this IPR proceeding?

A I see.

The number of declarations I submitted is -- for the IPR proceedings in particular would have been first the declaration for the POPR, the patent owner

preliminary response, and then a second deposition, which would be the more recent one, which is for the patent owner response, or the POR, after the Board instituted the IPR.

Q Okay. Could you open Exhibit 2006, please.

A Okay. Let me do that. Hold on.

Can I close the other one, the -- which one did I have -- 1100?

Q Why don't you leave that one open --

A Okay.

Q -- but you can close anything else.

A Okay. Let's see, what else is -- okay. That's the only one open. Good.

And now you say open 2006, correct?

Q Yes.

A Okay. I just opened it.

Q Okay. What is Exhibit 2006?

A I'm sorry, please repeat the question?

Q What is Exhibit 2006?

A I see.

So Exhibit 2006, as it says on the cover, right, it says the "Declaration of Dr. Sunil P. Khatri, Ph.D. in Support of Patent Owner's Preliminary Response."

So this is the declaration I filed, you know, in support of the patent owner preliminary response, or the POPR.

Q Would it be okay if I refer to this as your POPR declaration?

A I think that would be nice. That would be compact and unambiguous.

Q What date did you sign your POPR declaration?

A Let's see. Let me go to the -- let me go to the end of this file.

So on the last page, page 67, it says it -- that I executed April 28, 2025 in College Station, Texas.

So that was the date this was submitted.

Q Could you open Exhibit 2028?

A Hold on one second.

Now, was this -- you want me to

keep 2006 open or can I close some of the previous things?

Q You can close anything except the declarations and Exhibit 1100 and 2006.

A Okay. So I -- you want me to keep 1100 and 2006 open, correct?

Q Yes.

A Okay. I've got them open still.

And then the new one you mentioned is -- sorry, can you repeat, please?

Q Yeah, 2028.

A 28. Okay. I'm opening that one. And let's see...

That is -- I have it open now.

Q What is Exhibit 2028?

A So Exhibit 2028 on the front says: "Declaration of Dr. Sunil P. Khatri, Ph.D. in Support of Patent Owner's Response," or what would be the POR.

Q Would it be okay if I referred to Exhibit 2028 as your POR declaration?

A That would be good.

Q Okay.

What date did you sign your POR

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declaration?

A Let me look at the bottom of this document.

Okay. Yeah. So it says here on the last page of page 138 that -- it says: "Executed November 10, 2025 in Boulder, Colorado."

So that's the date it was signed.

Q Now, back to my original question about the claim term "from bottom to top" that you construed in Exhibit 1100, your district court declaration, is the term "from bottom to top" that you construed in Exhibit 1100, your district court declaration, one of the terms that you construed in this IPR proceeding?

A So to answer that question, I'm going to look a little more carefully at the new -- sorry, the last of the declarations, which is the -- what I think you called the POR declaration.

And in this declaration, there's a Section F, which -- sorry, a Section VIF, which starts, you know, on page 52.

So I'm just going to go there to -- before I answer your question.

So if I go to page 52, which is a claim construction section, you know, it explains the -- you know, in paragraphs like 94 to like 99. It just talks about how -- what I understand about claim construction.

And then from 99, it gives an overview of my opinions about claim construction.

And then starting 106, you know, it -- paragraph 106, sorry, it talks about construction for -- from bottom to top for -- from paragraphs 106 down through -- I think it's relatively longish.

106 to -- past -- well, past 126.

126 is where it talks about the intrinsic support for this thing, and then there is a section for extrinsic support, which begins in paragraph 1 -- let's see...

The whole thing ends at 141. So there's several paragraphs devoted to this, but yes, this is a term that I have

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construed.

I'm trying to look for the extrinsic section -- oh, yeah, that starts at paragraph 126.

So there's basically a section -- subsection for intrinsic support, subsection for extrinsic support, but the whole thing goes from something like paragraph 96 -- no, I'm sorry. Scratch that. From 106 to like 141.

It's one of the terms that I have construed for the IPR.

Q And you construed that term in both the IPR and in the district court declaration?

A Yes. I've construed this term in both, and, you know, it's -- the construction's consistent.

Q When you submitted your respective declarations in Exhibits 1100, 2006, and 2028, did each contain a complete and accurate statement of your opinions regarding the claim construction and validity of the challenged claims?

MR. LOWRY: Objection to form.

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A I would like -- I don't know what -- I frankly don't understand your question. So if you point me to a portion of the respective declarations and ask the question from that, I'd be happy to answer it.

Q Well, let me just break it out separately.

When you submitted your POR declaration, did it contain a complete and accurate statement of your opinions regarding the validity of the challenged claims in the '941 Patent?

MR. LOWRY: Objection to form.

A Again, I think that's -- you know, again, it's quite clear, and I say that in my declaration, that -- you know, I'm not an attorney, and I think it just sounds like a very legal question.

So I don't know how to answer that. I mean, I'm not able to grasp your question.

So again, like I said, if you point me to a portion in the -- in my declaration where you're focusing -- you

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know, where you would like me to focus and in answering your question, I'm happy to do it, but I need assistance from you in answering the questions because I'm not an attorney.

Q Well, let me try it again, maybe coming at it in a different way. I don't think it's a legal question at all. Let me try to ask it this way.

Have any of your opinions regarding the validity of the challenged claims in the '941 Patent changed since you submitted your POR declaration?

MR. LOWRY: Objection to form.

A So, you know, I mean, I have -- you know, from the POPR to the POR I've added new arguments, but, you know, there -- the opinions are all the same, and the arguments are -- they're additional arguments because I was responding to certain new information that has -- that had come up.

So there may be new arguments, but there's no new opinions as the opinions and -- you know, are unchanged and are

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consistent across all my declaration.

It's just that, I mean, there are three reports, so certainly there are differences in the words in those reports, and those differences pertain to, you know, certain new arguments or certain new facts that are brought up.

Q Yeah, and -- let me try that question again because there may have been, I don't know, some miscommunication there.

What was -- when did you submit your POR declaration --

MR. LOWRY: Objection to form.

MR. JENSEN: -- Exhibit 2028?

Rich, what's the objection.

MR. LOWRY: You're asking him when he submitted the POR declaration, and we already went through when he executed it.

MR. JENSEN: You can answer --

(Simultaneous crosstalk.)

MR. LOWRY: You can answer, Dr. Khatri.

A Sure.

So if I look at page 138 of the

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POR declaration, it says it was executed November 10, 2025.

Q Since you executed your POR declaration on November 10th of 2025, have any of your opinions regarding the validity of the challenged claims changed?

A You know, I mean, I do think that the claims of the '941 Patent are valid, and that's something that I thought, you know -- when I submitted the -- you know, Exhibit 2028, the POR declaration, and, you know, after it as well.

Q So let me try to ask the question this way.

Are there any errors, apart from typos, that you'd like to correct in your POR declaration?

A So there are a few typos. I don't remember them exactly. They're small ones.

I mean, in terms of substantive, you know -- errors that might be construed substantive, there would be one, and that's I think in paragraph 252.

If we go there real quick --

it's towards the end. And in -- I'm just going there to look.

In paragraph 252, you know, on the second line, it talks about Figure 5a, and then -- let's see...

In the last but the fourth line, it also talks about Figure 5a, and that should say Figure 5g.

So that's a typo that, you know -- I mean, it's inadvertent, but it's basically -- all the references to Figure 5a in paragraph 252 should say Figure 5g, you know.

And as far as I can see right now, there's -- well, there's three of them, right? But there may be more. But any time it says 5a in paragraph 252, that should be changed to 5g.

That's in line two and the last but third line and the last but fourth line as I can see right now.

But that's basically one change that might be substantive.

Q Apart from the typos in paragraph 252, are there any other errors

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that you'd like to collect in your POR declaration?

A I mean, there are a few other -- I mean, there were typos that were -- I got less significant than this, but I don't know where they are exactly.

If you want me to give you a list, I have it, you know, and in a break, I can make a list and -- you know, on a piece of paper and then read them out to you.

Q If you think they're just typographical in nature, then I don't think we should waste our time on that.

A I --

Q Let me -- just to be clear, apart from the correction that you identified in paragraph 252, are there any substantive errors that you'd like to correct in your POR declaration?

A I do not believe that there are any substantive errors in my declaration. And, therefore, you know -- other than any typos. So...

Q Were there any materials you

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would like to have reviewed when forming your opinions in your POR declaration but did not have access to?

MR. LOWRY: Objection to form.

A Can you repeat that again, please?

Q Were there any materials you would like to have reviewed when forming your opinions in your POR declaration but did not have access to?

MR. LOWRY: Same objection.

A No. I did have access to any materials that -- you know, that I wanted to -- that I needed -- that I thought I needed or asked for.

Q All right. Who else, if anyone, assisted in preparing your POR declaration?

MR. LOWRY: Objection to form.

A You're referring to the POR, the last one, correct?

Q Yes.

A Okay.

So in the -- for the POR declaration, I had some assistance from -- you know, from the attorneys. This would

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be in the form of, you know, making the language and the citations clean, and -- you know, so there was some assistance from attorneys.

And from my own side, I worked on it myself.

Q Did anyone such as a grad student or other assistant help you in preparing your report?

MR. LOWRY: Objection to form.

A I, you know, do not have any grad student or other help, you know, for my reports.

Q Can you go to paragraph 4 of your report?

A And which report are we talking about?

Q The POR declaration.

A I see.

And at this point, should I close the others or keep them around?

Q You can close the other ones for now.

A Okay. So hang on a second. I'm going to close the other two, and all I

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have open there is -- okay. Yeah, it says Exhibit 2028.

And you're talking about paragraph 4?

Q Yes.

A Okay.

Q And in that paragraph, you say: "I am being compensated for my time at my standard hourly rate."

A Correct.

Q What is your standard hourly rate, Dr. Khatri?

A I believe it's 800 an hour, but I might be forgetting -- I might be a little inaccurate because for different cases it's slightly different, and I don't know exactly what the rate is for this case.

Q Would it be approximately $800 an hour?

A I think that would be a fair statement.

Q What did you do to prepare for today's deposition?

A So for today's deposition, I --

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you know, I read the -- I read the POR declaration, and then I read, you know, references that I had cited -- you know, any material that I had cited in the POR declaration and, you know, any other material that were -- that is mentioned in my -- you know, in my POR declaration.

Q Did you meet with anyone to prepare for today's deposition?

MR. LOWRY: Objection to form.

And I just caution the witness not to reveal any privileged communications or attorney-client -- or attorney privileged work product in his answer.

But go ahead and answer, Dr. Khatri.

THE WITNESS: Okay.

A And can I ask you to please repeat that question?

Q Did you meet with anyone to prepare for today's deposition?

A Yes. I did meet with the -- you know, with attorneys for YMTC.

Q Which attorneys?

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A Well, one attorney, which is Richard Lowry.
Q How many times did you meet with Mr. Lowry to prepare for today's deposition?
A I think we met two times and possibly three, but I think it's two.
Q All right. In total, approximately how long did those meetings last?
A Those meetings would have lasted -- like each one was about two hours and change, two hours or a little bit more, a little bit less maybe every time, so a few hours in total.
Q Apart from Mr. Lowry, did you speak with anyone else to prepare for today's deposition?
MR. LOWRY: Objection to form.
A No. I only spoke with Mr. Lowry.
Q All right. Could you turn to paragraph 2 of your POR declaration?
A I'm there.
Q And could you just read that

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aloud, please?

A Certainly.

So paragraph 2 of Exhibit 2028, which is my POR declaration, reads: "I have previously rendered my opinion in support of the Patent Owner's Preliminary Response."

That would be the POPR.

"While I believe that declaration is accurate, this new declaration represents my considered opinion and supersedes my previous declaration. Any ambiguities between the two should be resolved in favor of this declaration."

Q In view of that paragraph, was there anything that was wrong or incorrect with your POPR declaration?

MR. LOWRY: Objection to form.

A I do believe that -- you know, the last line says any ambiguities should be resolved in favor of this declaration.

I do believe there aren't any, but I thought I would write this paragraph to be safe, to be -- you know, to

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essentially say that the new declaration, that's Exhibit 2028, or the POR declaration, supersedes any previous declarations that I have submitted.

Q Are there any ambiguities that you're aware of between your POPR declaration and your POR declaration?

A Yeah, so like I just said, I don't believe there are any ambiguities between them. I think there's complete consistency.

But this statement in this paragraph is there to be -- you know, to resolve any ambiguities that might have inadvertently crept in, which I doubt there are.

Q Could you turn to paragraph 22 of your POR declaration?

A Of the POR. Okay. Hold on.

Paragraph 22 coming up. Oh, there it is.

Yes, I am there now.

Q And that paragraph falls under the heading III, "Understanding of Legal Standards," correct?

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A Yes. This paragraph 22 is part of Section III of my declaration, which is titled: "Understanding of Legal Standards."

Q And that Section III spans paragraphs 22 to 38, correct?

A Let me verify. Let me double-check.

So Section III starts on paragraph 22. And let's see where it ends.

And, yes, it ends at paragraph 38.

So both 22 and 38 are inclusive as parts of this section.

Q All right. Who informed you of the legal standards set forth in Section III of your POR declaration?

A So the legal standards that are mentioned in Section III were conveyed to me by -- you know, by the counsel from -- you know, from Latham & Watkins, the YMTC counsel.

Q Could you turn to paragraph 41 of your POR declaration?

A Let me see, hold on.

Yes, I'm at that paragraph.

Q Could you just read that aloud, please?

A Certainly.

So this is paragraph 41 of Exhibit 2028, my POR declaration. And it reads: "My opinions are guided by my appreciation of how a person of ordinary skill in the art (defined in Section V) would have understood the claims of the '941 Patent at the time of invention, which I have been asked to assume is February 10, 2020."

Q Do you understand the date February 10, 2020 to be the priority date for the '941 Patent?

A So, you know, I'm --

MR. LOWRY: Objection to form.

A -- I'm always confused about the technical -- I mean, the legal sort of slash legal-ish name for this date.

But I think in -- on another part of my declaration, you know, it's referred to as the important date, or something like this. I -- let me look for

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that.

Q I can direct you --

(Simultaneous crosstalk.)

A We want to be careful about -- we want to be careful about using some term which is a legal term and has some weird, legal ramifications, which, you know, I don't understand.

So, therefore, I want to be careful in using this language.

And, sorry, you said something about you could help me with finding the other...

Q Yeah. I was going to suggest maybe looking at paragraph 98.

A Okay. Let me do that really quick. Thank you.

Paragraph 98.

Yeah, so it's -- for paragraph 98, it reads: "I further understand that the relevant timeframe for assessing the '941 Patent for purposes of this declaration is around February 10, 2020, the earliest priority date."

So this is the priority date

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that's referred to.

Q So you understand February 10, 2020 to be the earliest priority date for the '941 Patent?

MR. LOWRY: Objection to form.

A You know, so let's see. So February 10, 2020, if I look at the '941 Patent, if I go to Exhibit 1001 -- let's see...

If I look at -- if I open Exhibit 1000 -- I'm sorry, Exhibit 1001, which is the '941 Patent, you know, it talks about -- and under the section called "Related U.S. Application Data," it says that this thing is a division of application number 16/827,734, filed March 24, 2020, now Patent 11,195,590, which is a continuation of the application number PCT/CN2020/074580, filed on February 10, 2020.

So I think that's the genesis of this February 2020 date.

And, quite frankly, I don't understand the fine details of how -- you know, how you lawyers sort of figure out

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this date, but this is the date I've been asked to consider.

Q And to consider for what purposes?

A So for various things. You know, for various things.

So, for example, if you look at -- hold on, let me go there -- let me go to paragraph 41.

Regarding to paragraph 41, you know, it says: "My opinions are guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the '941 Patent at the time of invention, which I've been asked to assume is February 10, 2020."

So the purpose of this date, February 10, 2020, is for me to assume that this is the -- you know, according to this line, this is the time of the invention.

And in other locations where this occurs -- you know, this occurred also in paragraph 47 where I talk about the level of ordinary skill in the art, and in that paragraph, once again, this date

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reoccurs, and it says that in view of my education, background and experience working with the semiconductor industry -- and I'm paraphrasing a little bit -- I was at least a person of ordinary skill in the art as of February 10, 2020 under Dr. Liu's interpretation of the level of ordinary -- of a POSITA, you know.

And it also says that the '941 Patent claims priority to a patent cooperation treaty, PCT, application filed on February 10, 2020.

So again, it's basically for purposes of seeing what a -- according to this paragraph, which I just read to you, for purposes of understanding what a POSITA would be, this date would be important as well.

And there's another place where this date is important, which I think you just pointed out to me. I'm trying to search for that.

And that was for -- in paragraph 98, where I say that "I further understand that the relevant time frame for

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assessing the '941 Patent for purposes of this declaration is February 10, 2020."

So again, that's the purpose of this date, for me to assess the '941 Patent for the purposes of this declaration, that's the February 10, 2020 date.

So essentially, that's basically the -- you know, that's -- that's sort of the purposes for which I use this date, February 10, 2020.

At this point, I'm going for about an hour. Would it be a good time for me to take a break?

Q Could I maybe do one or two more questions?

A Certainly.

Q Just to round out this topic, and if you need to take a break, that's fine, but --

A Okay. Yeah.

Q Yeah, let me just ask you to go to paragraph 42 of your POR declaration and --

A Yes.

Q -- can you read that aloud,

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please?

A Certainly.

So paragraph 42, which is under -- the first paragraph of a Section V, whose title is: "Level of Ordinary Skill in the Art.

It reads as follows: "I have been informed and understand that the level of ordinary skill in the" art -- sorry -- "the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA might have for combining references."

Q And in that paragraph, when you refer to the "time of the invention," are you referring to that February 2020 time frame?

A That's correct.

Q And so the February 2020 time frame is the date you would use to ascertain the meaning of disclosures found in the prior art?

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MR. LOWRY: Objection to form.

A I'll answer that more carefully.

The 2020 time frame, as this sentence reads, right, is -- and I'll repeat this portion again.

I have been informed and understand that the level of ordinary skill in the art at the time of the invention.

So in some sense, this is saying, you know, that I'm using this time frame to understand what a level of ordinary skill in the art and not what your question asks.

So I think your question was perhaps misleading.

Q Well, let me just ask this.

Do you stand by your assertion in paragraph 42 that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references?

A So if I read this paragraph, I

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stand by it. It's just the paragraph says that I've been informed and understand that the level of ordinary skill of the relevant art at the time of the invention, you know, is relevant to inquiries such as meanings of claim term, meanings of disclosures found in the prior art, and the reasons a POSITA would have -- may have for combining references.

MR. JENSEN: Let's take a break.

THE WITNESS: Okay. Thank you.

(Whereupon, a brief recess was taken from 10:02 a.m. to 10:11 a.m.)

BY MR. JENSEN:

Q Dr. Khatri, I'd like to direct you back to Exhibit 1100, which is your district court declaration on the '941 Patent.

A Okay. Let me go ahead and open that really quick.

You said 1100, right?

Q Yes.

A Oh, wait, that was the new thing, the new one you gave me, I think.

No, it was not part of the

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bundle that you --

Q That's correct.

A I see. I see.

Okay. Let me open that.

And I have opened it.

Q And could you turn to Section III in that declaration that's at paragraph 23?

A Section III, paragraph 23, hold on.

Yes, I am there.

Q What is the title of that section?

A The title of Section III in this declaration, which is Exhibit 1100, is "The Level of Ordinary Skill in the Art."

Q And that's where you set forth your opinion regarding the level of ordinary skill in the art for the '941 Patent?

A Let me read this really quick before I give you an answer. So if you give me a few minutes. One second.

Okay. I have read this.

Did you have any questions about

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it?

Q Yeah. So my question was, is Section III in Exhibit 1100 where you set forth your opinions regarding the level of ordinary skill in the art for the '941 Patent?

MR. LOWRY: Objection to form.

A Yes, Section III here, right, it has multiple paragraphs.

But first of all, you know, paragraph 23 just says, you know, that the level of ordinary skill in the art is relevant for various things. And in considering that level of ordinary skill in the art, paragraph 24 says what are some of the things you consider.

And then in paragraph 25, I defined the -- based on the previous paragraphs, I defined the person -- you know, the level of ordinary skill in the art.

And then I also say in paragraph 27 that -- you know, that I was a person at least of that skill.

So basically, this is -- this

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section talks about, you know, what is a person of ordinary skill in the art, why is it important, how does one come up with -- you know, what are the considerations in coming up with the level of skill in the art.

And for the purposes of that declaration, which is Exhibit 1100, what I use as a person of ordinary skill in the art, which is abbreviated here as POSA, otherwise also sometimes abbreviated as POSITA.

Q Could you read paragraphs 25 and 26 aloud?

A Yes.

Let's see. Paragraph 25 says: For the purposes of this declaration, a POSA in the field of the '941 Patent would have had a bachelor's degree -- let's see -- in electrical engineering or a similar discipline, along with 2 to 3 years of professional working experience with, example, researching, designing or teaching NAND flash memory devices (including issues relating to the operation, for example,

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programming, of said devices), or an equivalent level of skill, knowledge or -- and experience, for example, an advanced degree may replace some of the professional experience.

Q And paragraph 26 as well?

A Paragraph 26 says: "In my opinion, this POSA would have been aware of and generally knowledgeable about NAND flash memory's structure and fabrication, its component parts, how it operates and how it is controlled."

Q Has your opinion of the level of ordinary skill in the art for the '941 Patent changed since you submitted your declaration, Exhibit 1100?

MR. LOWRY: Objection to form.

A So, you know, if I look at the -- if I look at -- so I have two answers to that.

My first answer is, if I -- if you go to the POR declaration -- sorry, I kind of get mixed up with these, so -- but if you look at the POR declaration, paragraph 2, you know, we've gone over this

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paragraph, but I'd just like to repeat this paragraph, and I'll read it.

Paragraph 2 of my POR declaration, Exhibit 2028, it says: "I have previously rendered my opinion in support of the Patent Owner's Preliminary Response. While I believe that declaration is accurate, this new Declaration represents my considered opinion and supersedes my previous Declaration. Any ambiguities between the two should be resolved in the favor of this declaration."

So, you know, for the POR, you know, this statement holds true.

Now, further, if I look at the POR for the person of -- for the definition of "person of ordinary skill in the art," if I'm not mistaken, it substantially matches what you see in the -- in paragraph 25 of the 1100 -- of the 1100 -- of Exhibit 1100.

Q Let me direct your attention to paragraphs 39 to 41 of your POR declaration.

A 39 to 41, let me see that...

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And this is Section IV relating to summary of material -- oh, by the way, sorry, I just deleted the 1100 exhibit.

Is that okay?

Q Yeah, that's fine.

A Okay. Just because I like to have few exhibits because my desktop gets cluttered pretty quickly.

Okay. Sorry. You know what, refresh me where we were -- and now we're back to Exhibit 2028, the POR declaration, is that correct?

Q Yes, in Section IV that spans paragraphs 39 to 41.

A I see. Section IV.

I am there now. And yes, it does span paragraphs 39 to 41 both inclusive.

Q Do those paragraphs contain a complete list of the materials you considered when forming your opinions in your POR declaration?

A Let me read that really quick. So...

I think this -- you know,

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this -- these paragraph -- these paragraphs -- sorry -- list the -- give you the summary of materials that I've reviewed and considered.

And, you know, and as paragraph 40 says, right: "All the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment."

So I have applied my knowledge and my professional judgment in this exercise as well, of course.

And also, in reviewing these documents, you know, I would have searched for documents, and some documents I might not have, you know, used.

So there may have been other documents that are not listed here because I have not used them or not cited to them in my declaration.

So there would be, you know, those as well, but those are not part of what -- they're not used in my declaration as such.

Q All right. Let me direct your

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attention now in your POR declaration to Section V spanning paragraphs 42 to 47.

A Okay. I am right there, but let me double-check. So Section V, yes, and it does span paragraphs for eight paragraphs, 42 to 47 both inclusive.

Q And what is the title of this section?

A So Section V of my POR declaration, which is Exhibit 2028, is titled: "Level of Ordinary Skill in the Art."

Q And what is the level of ordinary skill in the art that you used to form your opinions in your POR declaration?

A So the level is described in these paragraphs. So very quickly I'll sort of, you know, go over them and I'll sort of zoom in on one or two that are important.

So the first paragraph like says that, you know, the level of ordinary skill in the art is relevant for inquiries such as meanings of claims terms and meaning of disclosures and reasons a POSITA would have

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for combining references.

Paragraph 43 says what are the factors one would use in coming up with, you know, the level of ordinary skill in the art.

And it lists six factors, but I won't read them out because they're not completely -- I mean, unless you wish for me to do that.

And paragraph 44 says that under this -- under the definition of a POSITA, you know, the petition, it does not show that the challenged claims are anticipated or obvious. And, of course, it also says that in forming my opinions, I've drawn on my academic background and professional experience.

Now, paragraph 45 is the paragraph in which it defines Dr. Liu's definition -- sorry, it mentions Dr. Liu's definition of a POSITA, and it's a quote that is several lines, which basically a quote from Dr. Liu's declaration, paragraph 40, as to what he defines as a person of ordinary skill in the art.

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Excuse me, I'm losing my voice a little bit. Not a good sign this early in the day, I think, yes, but let's see...

So now, in paragraph 47 importantly, it says that I'm informed by counsel that patent owner does not dispute petitioner's definition of a POSITA for the purposes of these proceedings.

And that's the -- you know, in other words, that's the definition of a POSITA that I use for my analysis.

And then finally, paragraph 47 says that based on my experience and my education and my work in the semiconductor industry, you know, in various topics including 3D NAND, nonvolatile flash -- NAND flash, that I was at least a person of ordinary skill in the art as of February 10, 2020, which is a date that has come up in our discussion.

And it says that, you know, that under Dr. Liu's interpretation of the POSITA, you know, I was at least a person of ordinary skill in the art.

And I also note in paragraph 46

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that patent owner does not dispute the petitioner's definition of a POSITA.

So -- and finally, paragraph 47 also says that, you know, I have drawn on my own background and my own professional experience, you know, in coming up with my analysis.

But in all my analysis, you know, the last line of paragraph 47 says that my opinions are formed by taking into account the perspective of a person of ordinary skill in the art, or also called an ordinary skilled artisan, also called a POSITA.

So I'm putting myself in their shoes while I'm doing my analysis.

Q Did you render any opinions in your POR declaration under a definition of a POSITA different from that in paragraph 45?

A May I ask you to please repeat that question?

Q Did you render any opinions in your POR declaration under a definition of a POSITA different from that in

paragraph 45?

A Yeah. So in this section, you know, Section V, the level of ordinary skill in the art, I'm essentially saying that, you know, I'm -- I'm mentioning that in paragraph 45 Dr. Liu's definition of a POSITA.

And then I'm saying in paragraph 46 that I understand that patent owner does not dispute that definition, and that's -- you know, for the purposes of these proceedings, that's the definition that's been used.

And finally, I'm just saying that, you know, in paragraph 47, that I'm at least a person of ordinary skill in the art as of the February 10, 2020 date based on my knowledge and background and experience and such.

Q I'm not quite sure if that -- if I followed your answer. Let me just maybe ask the question one more time.

Did you render any opinions in your POR declaration under a definition of a POSITA different from that in

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paragraph 45?

MR. LOWRY: Objection to form.

A So I guess, you know, my answer was trying to say that the definition of a level of person -- sorry, a level of ordinary skill in the art and the person embodying that would be the POSITA, that's described in Section V. And in Section V, there's no other definition of a POSITA that I present.

So you can see pretty clearly the paragraphs of, you know, Section V, which go from paragraph 42 to 47 both inclusive. And they describe the person of ordinary skill in the art that was, you know, defined by Dr. Liu, which is shown in -- which is written in paragraph 45.

And then 46 -- paragraph 46 says that the patent owner does not dispute it. And that I am using -- you know, I'm myself a person of ordinary skill in the art by that definition.

So it basically pretty clearly answers your question, I think, but...

Q Let's go back to Exhibit 1100

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for a moment.

A Excuse me. One second. I'm going to find where -- oh, there it is.

Exhibit 1100. It just opened, yes.

Okay. I'm there.

Q Okay. And turn to paragraph 25.

A Let me go there really quick.

Okay. I'm there.

Q Okay.

And in that paragraph, kind of in the middle of the paragraph, maybe the third of fourth line down, you mention, you know, professional experience working with, the e.g., researching, designing, or teaching NAND flash memory devices.

Do you see that section?

A I do see that.

Q Okay. When you refer to "NAND flash memory devices," what do you mean?

A So this is, you know, the kind of memory devices that -- you know, that use a NAND -- you know, that use a NAND circuit structure, and they're memory devices, and they use flash for this right

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now.

This is basically something that, you know, a person of ordinary skill in the art would understand.

And if you want further clarification, there are -- you know, in my -- in my POR declaration, I've described NAND flash devices, you know, pretty extensively.

And so that is described in the -- Section VI of the POR declaration at exhibit 2028 starting around paragraph 48 inclusive through -- I don't know, let's see...

They go for pretty long, I guess -- and then going through paragraph -- well, I -- 48 to 64, which it talks genetically about -- you know, about these devices.

And then it continues in 65 going on through to -- it's a somewhat long section, sorry, but it goes on up to paragraph 83.

So paragraph 83 is where this discussion ends, but paragraph 48 is where

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it begins, where I described, you know, the whole business of different kinds of memories and then significant focus on NAND flash memory devices.

Q When you refer to "NAND flash memory devices" in paragraph 25 of Exhibit 1100, does that include both a 2D and 3D NAND flash memory?

A So again, you know, if you look at -- you know, I kind of focus my attention back to the Exhibit 2028, my POR declaration, and where I -- you know, Section VI, which is a -- VIA, which is technical background, you know, it talks in general about flash memory in the beginning, and then Section VIA1 starts to talk -- let me see, hold on...

VIA1 starts to talk about 2D NAND, or planar NAND flash.

And then Section VIA2 talks about 3D NAND flash.

And then Section VIA3 talks about differences between them from a program disturb point of view.

And what else, let's see...

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Yeah, so that's kind of the breakdown. In other words, right, like from the -- as you can see from my POR declaration, Section VI, which is the background section, talks about NAND flash in general, and then talks about, you know, 2D NAND flash, 3D NAND flash and their differences.

Q Okay. Let's go to Exhibit 2006, which is your POPR declaration, at paragraph --

A Just a quick question.

May I -- I mean, may I close 1100?

Q Sure.

A Okay. Let me do that.

And now you said -- can you please repeat -- you want me to go to...

Q Exhibit 2006, your POPR declaration, at paragraph 36.

A Okay. I'm right there.

Okay. And you said paragraph 36, correct?

Q Yes.

A Okay. Let's see, sorry, I'm

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kind of traversing that.

36, there it is. Okay.

Q And could you just read aloud the first sentence?

A Yeah.

The first -- so I'm reading from Exhibit 2006, which is my POPR declaration, and this is Section VI titled "Background."

And the first paragraph in that section, which is paragraph 36, is what I'll read next.

So it says: "The NAND flash memory landscape has developed significantly from 2000 to today."

Q What do you mean when you say that the "NAND flash memory landscape has developed significantly from 2000 to today"?

A I mean, I don't know what you mean by that really because, you know, it's -- it's kind of self-evident to me.

So maybe you could rephrase your question or something to help me understand what you mean to ask?

Q Well, yeah, so how has the NAND

flash memory landscape developed significantly from 2000 to today?

A I see.

So some ways in which it has developed significantly are described in the remainder of this section.

Q And what are those ways?

A And first of all, you know, I'll just remind you really quick that in my POR declaration, paragraph 2 of the POR declaration says that, you know -- that I have previously rendered my opinion in support of the POPR. That is by way of Exhibit 2006, which we are discussing.

And of course, it says while I believe that that declaration is accurate, and that refers to Exhibit 2006, it says, this new declaration, referring to Exhibit 2028, the POR declaration, represents my considered opinion and supersedes and -- you know, my previous declaration.

So the discussion we're having, which is about, you know, Exhibit 2006, if there's anything in here -- I mean, I have

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considered more material for the next exhibit and so it -- you know, this is superseded by the subsequent Exhibit 2028, which is the POR declaration.

Now, with that sort of preamble, you know, let me talk about -- I think your question was in what ways has the NAND flash memory landscape changed, is that correct?

Q Yeah, how has the flash memory -- the NAND flash memory landscape developed significantly from 2000 to today?

A Yeah. It has developed in multiple ways.

And of course, you know, just like any technology that, you know, is, you know, cutting-edge technology in the world of semiconductors and electronics, you know, from 2000 to now, which is something like 26 years, is an eternity. There's been many, many, you know, developments, improvements, changes and such.

And some of the changes, you know -- and there's a vast number of changes which, you know, at this point -- I

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mean, sitting here, you know, without any reference or without any sort of direct, you know, reference in front of you, you know, I wouldn't be able to give you a comprehensive list of.

But relevant to this '941 Patent and the IPR, the ways that in -- you know, in which it has developed significantly -- sorry, the ways in which the NAND flash memory landscape has developed significantly relevant to the '941 Patent and its IPR are listed in this Section VI.

And those ways are, you know, when it talks about 2D NAND flash and then talks also about 3D NAND flash and such.

So those are the -- you know, the -- you know, one vector, if you will, along which the NAND flash memory landscape has developed significantly.

And there are multiple other vectors, you know, which are not directly relevant to the '941 Patent at hand.

And so a comprehensive list of that I couldn't give you sitting here today.

But if you had a reference, you know, which listed them, I -- you know, I could -- yeah, you know -- if it's one of the references that I've reviewed, I'd be happy to give you a more detailed and more general, if you will, description.

Q So you mentioned a transition from a 2D NAND to 3D NAND that I want to follow up on.

In the year 2000, did 3D NAND exist?

MR. LOWRY: Objection to form.

A So, you know, once again, right, this is something that I would -- you know, the historical sort of evolution of these -- of this -- you know, of evolution from 2D to 3D NAND, you know, it's something that, you know, I would lean on and reference to, you know, before I give you an opinion.

And, you know, I wouldn't just give you -- I mean, I just wouldn't know off the bat, you know, what -- at what time frame 2D NAND sort of transitioned to 3D NAND.

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But I've used reference in my declaration, and I've used, you know, certain references to help me, you know, come up with that answer.

Q Do you know if 3D NAND existed in the year 2000?

MR. LOWRY: Objection to form.

A As far as I can tell -- you know, again, if you have a -- if you have a reference by which you want to show me and then you want me to sort of opine on that, I mean, I'd be happy to opine on that as you may need, so the reference I've reviewed and considered.

But, you know, the exact historical transition and whether, you know, 3D NAND existed in a particular year I wouldn't be able to sit here and give you a direct answer to.

Q Why was there a transition over the years from 2D NAND to 3D NAND?

MR. LOWRY: Objection to form.

A So let's see...

So in some -- some of the -- I don't remember which one, but some of the

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references that I have cited, you know, talk about the -- talk about the reason why 3D NAND was something that, you know, was a -- you know, was a step that was desirable because it led to more density.

And these citations are in certain exhibits that I've -- you know, that I have cited to in my declaration, which are in the range of that 2020-ish -- Exhibit Number 2020, you know, 4, 5, 6, 7 but I don't have that citation in my head off the bat.

But I'd be happy to look through those exhibits to answer your question.

Q Could you read the second sentence in paragraph 36 of your POPR declaration?

A In the POPR, sorry, hold on. I want to make sure I'm in the right one.

That's 2006, correct?

Q Yes.

A I believe -- sorry, did you answer that question?

I didn't hear you.

Q I said, "Yes."

A Oh, sorry. So let's see...

Paragraph 36 of Exhibit 2006, which is my POPR declaration.

And the second sentence of it, it says: 3D NAND memory devices are "memory arrays" with memory cells stacked on top of each other.

Q What do you mean by "memory cells stacked one on top of the other?"

A So, you know, when you read this sentence, this is just an introductory paragraph for the background section.

And if you wanted to give it -- you know, if you wanted to give it more light, I would point you to the -- you know, and again, since my POR declaration supersedes Exhibit 2006, you know, I'll point you to paragraphs in the POR declaration that describe what it means to have memory cells stacked on top of each other.

And these paragraphs are -- let me just see where they go -- you know, they were the -- I think I alluded to them already. These are in Section VI of

Exhibit 2028, which is titled "Background."

And if you look at Section VIA -- let me see, should be 3 -- 2 I think. That's a mouthful already.

VIA2 talks about what it would mean for cells to be stacked on top of each other, you know, and basically -- let's see...

Yeah, VIA2 as well as VIA3. For example VIA3, yeah, it talks about memory cells stacked on top of each other, and it talks about the architectures you might have for that, and also, the electrical implications of such architectures.

Q And is that in Exhibit 2028, your POR declaration --

A Yes. I was citing you -- sorry, I was pointing you to Exhibit 2028, which is my POR declaration.

And as I said earlier, you know, paragraph 2 in that declaration says that, you know -- you know, that that declaration supersedes, you know, the POPR declaration, which is Exhibit 2006.

Q Yeah, so let me go to where you

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were pointing, I believe, which is Section VIA2.

A If I may correct you really quick, it's not just Section VIA2 but it's Section VIA2 and VIA3. It's sort of the combination of these but --

Q Sure. I can only look at one of them at a time, so let's look at Section VIA2.

Can you read the title of that section?

A Most certainly.

VIA2, which is -- just to double-check this is on paragraph 66.

Are we in sync on that?

Q Yes.

A Yeah. So VIA2 talks -- I mean, the title of VIA2 is "Three-Dimensional NAND At The Time Of Dong's Filing Date Included Stacked 2D NAND," right?

So VIA2 is sort of specific to 3D NAND around the time when Dong was filed.

And that's the title, and now I forgot your question.

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Did you say to read the title of the section or the first paragraph? I forget what your --

Q No, my -- yeah, just the title.

My follow-on question has to do with kind of nomenclature and what you mean by, you know, three-dimensional NAND.

And you identify in the -- you know, paragraph 66 and the following paragraphs I think what you call stacked 2D NAND as a form of 3D NAND, is that correct?

A Correct.

MR. LOWRY: Objection to form.

THE WITNESS: I'm sorry, I didn't hear that.

I kind of got caught -- I kind of got lost in the question and the objection.

Can you please repeat the question?

BY MR. JENSEN:

Q Yeah.

So what -- when you use the term "3D NAND," what do you mean?

MR. LOWRY: Objection to form.

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A So again, when I use the word "3D NAND," it means -- you know, it means something in VIA2 because VIA2 is responsive to -- as the title suggests -- 3D NAND at the time of Dong's filing, which includes stacked 2D NAND.

And then VIA3 talks about, you know, program disturb differences between 2D and 3D NAND, and this is, you know, talking about 3D NAND once again.

So 3D NAND is described in these two sections.

Q Does 3D NAND include NAND memory devices with vertical memory strings?

MR. LOWRY: Objection to form.

A So once again, this is kind of a broad question and, you know, it's important to put a timeline to it, right?

Like, for example, at the time of -- so it would not be possible to answer that question without -- you know, in the way it's posed basically.

Q Why not?

A Because there's no time frame.

So if you said to me like in the

years, for example -- I mean, I'm not -- I mean, you know, to be somewhat facetious, but if you asked me like in the year 1680 like what a 3D NAND mean, you know, that's kind of -- you know, it's a completely different answer than in the year 2025 what does 3D NAND mean.

So that's why if you just say does 3D NAND include something without assigning a time frame to it, it's not really a question that can be answered with any accuracy.

Q Let me lay a little foundation first then.

Do you have an understanding of what a vertical NAND memory string is?

A Again, repeat the same question, please?

(Simultaneous crosstalk.)

A -- the question being very, you know, delicately for power framed. So I need to hear it more carefully.

Q Do you have an understanding of what a vertical NAND memory string is?

A Again, I would ask -- excuse

me -- in what context are you talking about, you know, a vertical -- I need that question to be fleshed out because it's too -- again, it's too broad, like the previous questions.

Q I mean, Dr. Khatri, you purport to be an expert in NAND flash memory, correct?

A That's correct.

Q Okay. What is a vertical NAND flash memory string?

A So again, if you give me a specific reference or a paragraph, I can talk to that, but in the -- in just the abstract, it's hard to describe.

So if you looked at it, you know, for example, the -- you know, if you looked at -- let me see. Let me just point you to a paragraph in my declaration where -- let's see...

Yeah, let's look at page 40 of Exhibit 2028, where I show a figure -- let me see if there's a better place to answer this question from, but let me look around a little bit to see if I have a better sort

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of reference to lean on.

Sure, we can do this. If you look at exhibit -- sorry, page 40, Exhibit 2028, which is my POR declaration, and there's a figure on there, which is Figure 8.11 from a reference called Aritome, which is a -- which is Exhibit 1009, which is a reference from the -- it's a petitioner's reference.

So you see that figure on the right of your screen basically.

If you look at this figure, it says -- let's just first read the caption on this figure. It says: "Program disturbance mode of 3D NAND flash" memory.

So this figure establishes that -- you know, that it's relating to 3D NAND flash memory.

Now, in this 3D NAND flash memory, you can see on the left -- figure on the left, which is Figure (a), you can see several vertical strings. These are NAND strings.

So you see, you know, the NAND string, which has a numeral 1 with a little

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circle around it, another NAND string which has a numeral 2, a third with a numeral 3, a fourth with a numeral 4, and then there's other NAND strings also behind these, which -- you know, which are not labeled with a circle around them.

But these are vertical NAND strings.

Now, why would I conclude they're vertical NAND strings? Because the caption of this figure says this pertains to 3D NAND flash memory.

So it's establishing context, and it's saying, you know, this is a 3D NAND flash memories, and it says, you know, end strings are connected to the same bit line on the same blocks, again, establishing what a string is.

So again, I want to root my answer in something that's concrete and -- you know, rather then just sort of -- rather than just respond with the -- you know, some kind of abstract for an abstract question.

So this is essentially an

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example of -- this figure shows an example of four numbered vertical NAND flash strings. And in total, the drawing literally shows six vertical NAND flash strings.

And they're in a 3D context, which the caption clearly described.

Q Let me see if I can bring up maybe another example.

A At this point, may I close one of these references I had? Because I have like -- I think I have two of them opened right now, 2006 and 2028.

Q You can close 2006.

A Okay. I'll do that. Thank you.

Q Yeah, let me ask you to turn -- maybe just as another example to make sure we're on the same page here -- to paragraph 212 in your POR declaration.

A In the POR. Okay. Let's go to that. 212. Let's see, 212.

I'm trying to get there.

212, I'm there now -- wait, one second. It's on page 107, right? Yeah.

Q Yeah.

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And you include a figure on page 108 that has a -- you know, part A on top and a part B below it.

A Yeah. So let me -- let's see, is that 212? No.

Are you referring to paragraph 212 or the figure?

Q Paragraph 212, in which the figure appears.

A Oh, oh, oh, I see. Okay. Hang on.

Let me read that paragraph and sort of subparagraphs in its neighborhood. Give me a second, please.

Okay. I think I've looked at that paragraph, and I'm happy to answer any questions you have on 212 and the figure below it.

Q Yeah, so can you just read the caption for the figure?

A Yeah, let's see.

So Figure 1 from Exhibit 2025, which is shown below paragraph 212 of my POR declaration on page 108 of it, it shows two sub-figures. And so the caption talks

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about both these sub-figures.

So the first sub-figure, which is sub-Figure (a), the caption for that reads: "2D planar NAND device and equivalent circuit model."

Now, if I look at Figure 1 of -- which is sort of excerpted in my declaration on page 108, Figure 1 has the -- you know, a cross-section of the 2D planar NAND device as well as the equivalent -- electrically equivalent circuit model.

And then it has a sub-Figure (b), for which the caption is: "3D NAND device and equivalent circuit model."

And once again, Figure B shows two objects -- I mean, it shows on the left the 3D NAND device and cross-section, and on the right, it shows the equivalent circuit model, like a circuit diagram of the same.

Q Is the colored image on the bottom of the figure an example of a 3D NAND memory string?

MR. LOWRY: Objection to form.

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A I did not understand your question.

Can you repeat your question, please?

Q Yeah.

Is the colored figure on the bottom an example of a 3D NAND memory string?

MR. LOWRY: Objection to form.

A I do not know what you mean by the "colored figure on the bottom."

So, I mean, clearly, as the caption says, you know, Figure 1(b), you know, is a 3D NAND device along with its equivalent circuit model.

So if I look at the Figure -- the sub-Figure 1(b), it has two components -- I mean, it has two -- the figure has two parts to it.

On the left is a cross-section of a -- of the 3D NAND device, based on the caption, and on the right is the equivalent circuit model, once again, based on the caption.

And the equivalent circuit model

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uses the circuit symbols for NMOS devices, which are the two devices driven by SSL and GSL, and, also, multiple NAND flash -- NAND -- sorry, multiple flash transistors, which are driven by WL0 through WLn.

And these symbols, the symbols for the NMOS devices and the flash devices, in both equivalent circuit models for Figure 1(a) as well as 1(b) are as I described in my declaration as well, and these come from exhibits, I believe, 2009 and 2010, but I'll just verify that real quick.

So if you'll go to my declaration on page -- sorry, let's not go page. Let's do paragraphs.

On paragraphs 113, there's a figure below paragraph 113 in my declaration that shows the electrical symbol of a flash transistor, and then -- oh, sorry, no, I didn't mean 113. Sorry, that was a mistake.

On paragraph -- sorry.

Let's just do page numbers. Sorry, let's scratch all that.

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If you look at page 69 of my POR declaration, Exhibit 2028, it shows a figure of a -- the equivalent symbol -- the equivalent circuit symbol of a flash transistor or it's schematic symbol.

And then if you look on the next page, page 70 of my POR declaration, Exhibit 2028, it shows the -- you know, the three terminal device, the equivalent circuit symbol for the NMOS transistor.

Now, if we go back to where we were -- sorry, I forget where we were. Can you please point me to the paragraph that you had pointed -- that we were looking at?

Q I believe it was --

A 212.

Q -- paragraph 66.

A No, 212, I think. I don't recall a 66.

I think we were talking about paragraph 212, which was, you know, some colored figures and the equivalent circuit models thereof.

Q Oh, yeah. That's the one.

A So if you look at the equivalent

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circuit model in sub-Figure 1(a) and the equivalent circuit model in sub-Figure 1(b), a POSITA would look at that and readily recognize that the circuit symbols in both these equivalent circuit models match with the flash transistor equivalent circuit that -- you know, the symbol that I showed you from paragraph -- from pages 69 and 70.

And then also, the NMOS transistor symbol is also present in both of these, again, matching the symbols I pointed out from pages 69 and 70 of my declaration.

And those symbols in page 69 and 70, they come from Exhibits 2017 and 2019 respectively.

Q So yeah, let's go back to paragraph 66 of your POR declaration.

A Paragraph 66, let me go there. Hold on, please.

66. I think we -- by the way, we've been going for about an hour, so I'd like to request a little break at this point. And I probably need to get some

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lozenges or something.

MR. JENSEN: Let's take a break.

THE WITNESS: It's a good time? Okay.

All right. Thank you.

(Whereupon, a brief recess was taken from 11:05 a.m. to 11:15 a.m.)

BY MR. JENSEN:

Q Dr. Khatri, we're looking at paragraph 66 in your POR declaration.

And the heading just above that paragraph, it says: "Three-Dimensional (3D) NAND At The Time Of Dong's Filing Date Included Stacked 2D NAND."

What is stacked 2D NAND?

A Let me see. Hold on. Let me just go to -- you said paragraph 66, yes?

Yeah. Sorry, I'm going to -- let me just orient myself.

Were you reading from 66?

Q I read the heading.

A Oh, I'm sorry.

Yeah, the heading of -- what is it -- of this -- let's see. This is VIA2, I believe, Section VIA2.

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Yes, the heading of Section VIA2 of my declaration, which begins on page 34, reads: "Three-Dimensional NAND At The Time Of Dong's Filing Included Stacked 2D NAND."

And I believe your question was, what is stacked 2D NAND.

Q Yes.

A Okay. So stacked 2D NAND, you know, is basically, as the rest of this section describes, you know, multiple layers of 2D NAND stacked on top of each other.

For example, you know, as paragraph 66 says, you know, one such example is stacked NAND -- and I'll describe that in a second -- and the second is multi-layered thin-film transistor, or multi-layered TFT, NAND designs.

And these are horizontally arranged 2D NAND memories that are stacked on top of each other creating a three-dimensional memory array, but such a memory array does not have vertically arranged word lines.

So as an example, you can see,

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you know, the stacked NAND -- excuse me -- example, which is Exhibit 2008, and a figure from that is described or shown on the next page, page 35.

And you can clearly see that there are essentially, you know, two -- in this picture, there are two layers of 2D NAND that are just like, you know, stacked on top of each other, but the word lines of these are horizontal still. You can see the word lines being horizontal in these two figures that are shown on page 35.

So if you're looking now at paragraph 67, I've describe the stacked NAND further. It says: "A person of ordinary skill in the art would have understood that stacked NAND" -- for which the figure was on page 35 -- "uses the same structure as the traditional 2D NAND."

You can literally see that these are -- you know, that these pictures have a source select line, so side select transistor, like that is a GSL, or grand select line, near the source side of this -- you know, of the NAND string.

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And then a drains side select transistor, or the SSL, which is also abbreviated as -- for -- I mean, which stands for string select line, which is near the drain side of this string.

And then also has multiple word lines, which are referred to as cell string in the figure.

So a person of ordinary skill in the art would readily understand that this is a stacking of multiple duty NANDs. That why I -- you know, that's why this -- they're called stack NAND.

And so instead of having just one level, like a normal duty NAND would have, stacked NAND, which is shown below, for example, on page 35 of my example, it uses multiple layers of duty horizontally arranged NAND strings that are just stacked on top of each other, sort of like a pancake, if you will, like layers of a -- you a bunch of pancakes sitting on top of each other in a 2D manner.

So that's stacked NAND, and in a similar way, the second kind of -- you

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know, stacked 3D NAND is what is described in -- you know, in paragraph 69.

And by the way, in both these paragraphs, the word lines are still arranged in a horizontal plane about the substrate, as I say in paragraph 68. They're not vertically arranged. You know, and there's support for that from the -- from the exhibit.

Now, if you look at paragraph 69, it describes the other example of a stacked NAND, which is the multi-layer, you know, TFT, again, very similar to the stacked NAND, as you can see in the example on page 36 of my declaration, Exhibit 2008.

And this shows basically, again, two -- two-dimensional NAND layers was what the caption in the figure calls as top and bottom layers, and these are, again, arranged horizontally on a substrate.

So basically these are, again -- you know, word lines again in this case are arranged horizontally and not vertically, as I say in paragraph 69.

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So finally, I kind of, you know -- you know, paragraph 70 sort of summarizes what we just -- what I just described, and it says that these -- that, you know, the 2D NAND based, you know, stacked NAND and multi-layer TFT NAND designs are not the same as vertical 3D NAND that is stored in the '941 Patent because cells are not arranged vertically from bottom to top.

And this first line of paragraph 70 has a little typo. It should say multi-layer TFT NAND. It's missing the word "TFT."

But, you know, in context, you know, we're talking about TFT, so that's -- it's not a -- it's just a minor typo.

Q So in the bottom of paragraph 66, you refer to vertically arranged word lines.

Do you see that?

A Yes.

Q Okay. Is it your opinion that NAND memory structures in 2007 did not include vertically arranged word lines?

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MR. LOWRY: Objection to form.

BY MR. JENSEN:

Q Strike that. Let me ask a separate question.

Were vertically arranged word lines known to POSITAs in 2007?

MR. LOWRY: Objection to form.

A So again, I think this is a question that's -- you know, that's posed in a way that's hard to answer.

First of all, what I'm talking about is, you know, three-dimensional NAND at the time of Dong's filing.

So I'm specifically talking about the time of Dong's filing, which is, you know -- which, you know, is, as we can see in the front page of Dong -- I'll just really quickly double-check it...

But -- I forget what was -- is Dong Exhibit 20 -- 1005? Let me know, I think.

Yes, it is. Okay.

So if you look at the time of filing of Dong -- excuse me, that's on the front page of Dong, which is patent

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2008/0279008, which is also Exhibit 1005. If you look at the filing date of it, it's May 7, 2007.

So I'm sort of talking about that date rather than just broadly the year 2007.

So therefore, you know, I wouldn't answer your question as -- you know, for a broad date of 2007. To be more accurate, I would use the time of filing of Dong -- the time of filing Dong's date -- sorry, the time of Dong's filing date, which is basically part of the title of Section VIA2, and that happens to be May 7th of 2007.

Sorry, May 7, is that correct? Let me just double-check that. I think that's right. May 7th -- I just don't want to make -- give me one second, I'll double-check. I think it's right, but I closed the file.

Yes, May 7, 2007. That's the time that I'm interested in in my inquiry, not just the general time of 2007. That's just too broad.

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Q Yeah, so I'm not here to quibble over -- you know, we can use the phrase "at the time of Dong's filing," if that is an important distinction for you.

So at the time of Dong's filing, is it your testimony and opinion, Dr. Khatri, that vertical NAND memory strings were not known to POSITAs?

A At the time of Dong's filing, you know, the -- what I'm trying to say here is that -- you know, if, again, we can look carefully at the title, right? The title of Section VIA2 says: "Three-Dimensional NAND At The Time Of Dong's Filing Date Included Stacked 2D NAND."

So I am saying that, you know, as of Dong's filing date, 3D NAND included this technology, which I have described in this section using the examples of Exhibit 2008, which is the stacked NAND, and Exhibit 2009, which is the multi-layer TFT NAND, which is also very similar to a stacked 2D NAND.

Q At the time of -- strike that.

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At the time of Dong's filing, did 3D NAND also include NAND memory devices with vertical memory strings?

A You know, I mean, if you show me an example, I can basically look at that and give you an opinion.

But the statement I'm making in exhibit -- I mean, in Section VIA2 of my declaration, Exhibit 2028, is that 3D NAND at the time of Dong's filing included stacked 2D NAND.

Q Right.

And I'm asking what else it included, in particular, did 3D NAND at the time of Dong's filing include NAND memory devices with vertical memory strings?

A So if you give --

MR. LOWRY: Objection. Form.

A Again, if you give me a specific example, I can give you an opinion on that, but, you know, like the statement that I have in Section VIA2 is accurate, which is: "3D NAND At The Time Of Dong's Filing Date Included Stacked 2D NAND."

Q Did 3D NAND at the time of

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Dong's filing date exclude NAND memory devices with vertical memory strings?

A I mean, again, you know, like you're looking at -- if you're looking at -- I mean, you know, the statement that I make in the title of Section VIA2 is quite precise. It says: "3D NAND At The Time Of Dong's Filing Date Included Stacked 2D NAND." And that's exactly what it says.

Q Right. And that's not my question, right?

My question is: Did 3D NAND at the time of Dong's filing date exclude NAND memory with vertical memory strings?

A Yeah. So --

MR. LOWRY: Objection to form.

A -- what, you know, what is important here for me -- you know, what is important is that -- you know, the fact that 3D NAND at the time of Dong's filing includes stacked 2D NAND.

And, you know, in that sense essentially, you know, that's, you know, more than what basically, you know -- I mean, that's sufficient in some sense for

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me to make -- do my analysis and, you know, that's sufficient to do my analysis for ground 1, which is, you know, an anticipation ground, and for ground 2, which is an obviousness ground.

Q Do you have an opinion one way or another, Dr. Khatri, whether 3D NAND at the time of Dong's filing excluded vertical 3D NAND memory strings?

MR. LOWRY: Object to form.

A Again, I have not said that. My statement is simply that -- you know, the title of Section VIA2 is that, you know, 3D NAND at the time of Dong's filing includes stacked 2D NAND.

And that's important because that's the extent to which the -- that's -- you know, that's the precise statement that is important and sufficient for me to refute ground 1, which is, you know, an anticipation ground that uses Dong. And then ground 2, which is an obviousness ground that uses Dong again.

Q Let me introduce an exhibit, 1087, into the chat.

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A Is this a new one?
Q Yes.
A Okay. Let me see. Let me hold on a second. I'm going to first save it, move it to that folder that I have.
Just give me one second.
All right. There is 1087 and I'm going to now -- give me one second, please. I'm going to move this around and...
Which folder did it move into?
Okay. I think I found it. And now I'm going to open it to -- from my folder. Okay.
All right. I think I see the exhibit you're talking about.
Q Yeah. And can you confirm that Exhibit 1087 is the U.S. Patent Publication Number 2007/0252201?
A Yes, I see that this is Patent 2007/0252201 by Kito, et al.
Q And feel free to take a moment to peruse the figures, if you'd like.
But my question is: Do Figures 1, 2, and 3 in Exhibit 1087

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represent a stacked 2D NAND architecture or a NAND architecture with vertical memory strings?

MR. LOWRY: Object to form.

A Sorry, I need a little time to read this patent.

And, you know, again, this is the first time I'm seeing this patent, and therefore, in some sense, it's going to take me a while to sort of read through it and make an opinion.

And because it's the first time, you know, my opinion would be just limited and I -- you know, I stand -- you know, I may need to correct it if I read more item -- more things about it.

So this is basically a preliminary -- my opinion would be preliminary, but it would be based on having a look at it, which might take me a while. So if you give me some time, please.

Q Go ahead.

A Okay. So my response is around several vectors, or several sort of points,

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right?

So I'll start with the first point, item 1, is that, you know, I've always had -- you know, as a -- I'm not a lawyer, and so I don't know how these priority dates and such are computed.

So first of all, I couldn't look at this and be assured -- you know, not being a lawyer -- as to whether this reference is prior or for the -- you know, as of the date of Dong.

So that's the fist comment that I have.

The second comment I have is that this reference has something like 50 claims and 300 paragraphs and something like 95 or 97 figures.

So it's completely impossible for me doing -- you know, sitting here in front of you, you know, in the duration of this deposition to look at it in a sort of a tunnel and in an informed way to give you a solid opinion that -- you know, in either direction.

So that's basically something

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that -- this is an overly large patent, you know, which I haven't seen before, and -- with a large number of claims, 50, with a large number of figures, about 100, and a large number of paragraphs of spec, which is something like 300, just an overwhelming -- an overwhelming amount of data to process in any reasonable way in the time I have.

And that's my second comment.

My third comment is that, you know, it's -- based on my current read of this -- and like I said before, I want to make sure that it's understood that my comments here are preliminary based on a brief reading of a voluminous patent with a lot of claims and a lot of paragraphs of spec and a lot of figures.

But with that caveat, you know, I only see the word "NAND" in this once, and I only see the word "flash" -- yeah, I think one flash occurs only twice.

So there's basically -- it's not completely clear that this is basically, you know, like relevant to the technology

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we're talking about because it's also talking about -- as you see in the abstract, it's talking about memory cells laminated and so on.

So I need to look into that in more detail. Again, I don't have enough time to actually look at it in -- you know, in a solid, informed way, which is what I usually do, in this short time that we have.

So that was item 3.

Item 4, let's just say, arguendo, right, let's -- and I'm not saying that this is the case, but arguendo, let's say that this is something that, you know, predates Dong, you know, in terms of priority date and such. And let's also say that, you know, it teaches a vertical -- you know, vertical NAND -- you know, vertically arranged NAND cells.

So let's say all that is true. Again, I'm not saying it's true. I'm saying, arguendo, let's assume that that's the case.

If that's the case even, right,

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it doesn't change the opinion that I have in my declaration, which is Exhibit 2008.

So if you look at Section VIA2, you know, I have said, three-dimensional NAND at the time of Dong's filing included stacked 2D NAND.

So the fact that you, arguendo -- let's say this is a -- you know, a vertical 3D NAND structure, it does not contradict, you know, any of my findings in this -- in my declaration.

But yet further, if you look at my -- if you look at my arguments against Dong's ground 1 and ground 2 -- and I'll point you to that portion of my declaration. Let's go to that portion. I'm going to have to find it. Give me a second. It's like in the low -- it's in the low 90s, I think. Give me one second, please.

Oh, there we go.

So if you look at my declaration, which is responsive to Dong's -- so to the first two grounds, ground 1 and ground 2, which is in

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Section -- sorry, Section like VII.
VIIB -- VIIB1 and VIIB2.
VIIB1 talks about -- the title of Section VIIB1, in which I refute ground 1 of Dong, is titled "No Anticipation."
VIIB2 -- sorry, and VIIB1 begins in paragraph 188.
VIIB2 begins in paragraph 196, and it's title is "No Obviousness," in which I respond to the ground 2 of Dong, which is the obviousness ground of Dong.
So let me attack these one at a time and show that the arguments that I have in VIIB1 and VIIB2 are unaffected by this arguendo discussions we had, which is assume arguendo that this reference --

Q Yeah, let me -- let me pause you right there, Dr. Khatri, because your counsel can follow up and ask you whatever questions they want to ask you to explain other things in your declaration.
My question is about Exhibit 1087. So let me direct you back to Exhibit 1087, and let's look at Figure 2 in that exhibit?

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A If you'd let me, you know, I can sort of give you a brief closing argument to this because it's important for me to --

Q Dr. Khatri, you've had about ten minutes to talk and answer a simple question.

MR. LOWRY: Counsel, please let him finish his answer --

BY MR. JENSEN:

Q Your counsel can follow up and ask you for your closing argument. I have a factual question about the reference to Exhibit 1087. Your answer is completely nonresponsive. We only have seven hours for this deposition, and I need to pull you back to the question that I asked.

A So I --

Q And your counsel, again, he can follow up and he can ask you all of those things that you might like to say, but your answer has gone on for a very long time, and given the limited time, and in the interest of getting everybody on the way -- on their day, let me just pull you back to the exhibit that I asked about.

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A I'm going to gently request -- I mean, mention that you -- you said this was a simple question. I really don't think honestly it's a simple --

Q I'm not going to quibble whether it's a similar question or not. I'd like to --

A It's a question about --

(Simultaneous crosstalk.)

Q -- direct your attention back to Exhibit 1087.

A Yeah, then that -- it's not a simple question because it's a question about a patent that has 300 paragraphs, 100 block figures and 50 claims.

It's not a simple thing to read that in a short time.

Q And I'm not asking you to read the whole thing, and I'm not asking you about the claims. I didn't ask you anything about the claims. I asked you a question about three figures.

So let me pull you back to the figures, and I'll try to ask maybe a different question that hopefully is easier

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to answer.

Do you see Figure 2 in Exhibit 1087?

A Let me open that figure on my copy and see.

I do see Figure 2, yes.

Q Okay. And you see there's a -- sort of dotted oval on the left-hand side?

A I see that.

Q What is the label for that oval in the figure?

A You know, the label says: "Memory strings."

And once again, I'm going to stop you right there and say, listen, if you're just going to point me to individual labels in a patent that's, you know -- you know, that has 95 paragraphs -- sorry, 95 figures and you're going to point me to one label in one of the figures that I've never seen before, along with 50 claims, along with 300 -- you know, along with 300 paragraphs in the spec, I mean, that's just an impossible burden.

I can read things for you from

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the patent, but I don't think that that's going to be something that will allow me to form an opinion about this -- about this patent.

Q Are the memory strings 10 in Figure 2 of Exhibit 1087 oriented vertically or horizontally?

MR. LOWRY: Objection. Form.

A Now, once again, you know, I don't know -- like I've said before, you know, this is basically a patent with, you know, something like 100 figures and, you know, 300 paragraphs in the spec and 50 claims.

So, you know, without just basically reading this in some -- in a thorough manner, for me to give you an opinion about this patent and any details about it is not going to be possible in the short time I have.

Q Can you tell by looking at Figure 2, Dr. Khatri, whether the memory strings 10 are oriented vertically or horizontally?

MR. LOWRY: Objection to form.

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A You know, like I've said, you know, this is basically a patent that's been put before me in the first -- for the first time, and, you know, it has -- again, as I've said -- and I hate to be repetitive, but the question is repetitive. So I'm going to, you know, have to repeat myself as well.

But, you know, it has something like -- let's see...

You know, it has like 50 claims and, you know, about 100 figures and 300 paragraphs of spec and a total of 115 pages.

Now, a patent which has 115 pages, I mean, that would take me a while to go through and make any conclusive comments about. 115 pages of patentees is something that I -- ordinarily would take a long time to read, and I just -- and form any opinion about.

So sitting here, I'm not going to be able to give you, you know, an answer that you want, you know, without thoughtful consideration for such a large patent with

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115-odd pages and, you know, 50 claims, 300 paragraphs of spec and about 100 figures.

Q All right. As an expert in this field, Dr. Khatri, I will accept your testimony that you cannot tell by looking at Figure 2 whether that is a vertical memory string, and we can move on.

A So --

MR. LOWRY: Objection to form. There's no pending answer -- or question.

BY MR. JENSEN:

Q Well, let me ask the question and be very clear.

Dr. Khatri, as a purported expert in the field of NAND flash memory, including 2D NAND and 3D NAND, can you tell by looking at Figure 2, without having to resort to anything else in this document, whether the memory strings 10 are oriented vertically or horizontally?

MR. LOWRY: Objection to form.

Counsel, this has been asked and answered multiple times. It's

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bordering on badgering the witness. You can't put a document that's over 115 pages and ask --

MR. JENSEN: Counsel, limit your objection to objection to form.

This goes to the heart of Dr. Khatri's credibility as an expert in this area. If he cannot look at Figure 2 and say whether that is a vertical or a horizontal memory string -- it takes someone who is not even a POSITA about 1 second to answer that question -- we're going to put this in front of the Board. It is going to be immediately apparent, and I want to give Dr. Khatri every opportunity to answer the question whether, as an expert in the field of NAND flash memory, he can tell by looking at Figure 2 whether the memory string 10 is oriented vertically or horizontally.

MR. LOWRY: Go ahead and ask your question. That's been asked and answered multiple times, counsel.

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A Can you please repeat your question?

Q Yeah. So I'll ask a clean question, Dr. Khatri.

As someone who is an expert in the NAND flash memory area, can you tell by looking at Figure 2, without having to resort to anything else, whether the memory strings 10 are oriented vertically or horizontally?

MR. LOWRY: Objection to form.

A In my answer, may I request that I not be interrupted?

Will that be something that you will be able to allow me to finish an answer before you -- you know, before you -- and not cut me off.

Is that fair?

Q It's a yes-or-no question. If you can answer that with a yes or no, then I won't interrupt or cut you off.

If you're going to go on a diatribe or a dialogue for ten minutes, I may have to interrupt so we can move on.

But I'm asking you a yes-or-no

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question, Dr. Khatri.

A So I'll repeat my answer, and if you feel like, you know, you want to cut me off, I also reserve the right to say, you know, what I had wanted to say but you didn't allow me to is something that I, you know, have not been allowed to speak. All right?

You --

Q Let me ask a clean question. Let me ask the clean question so we have it on the record.

As a purported expert in the field of NAND flash memory, Dr. Khatri, can you tell by looking at Figure 2 of 1087, without having to resort to any other materials, whether the memory strings 10 are oriented vertically or horizontally?

MR. LOWRY: Objection to form.

A Is your question completed?

Q Yes.

A Okay.

My response is going to be that this is a large patent. I have 115 pages, 300 paragraphs of spec, 90 figures and

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50 claims.

For me to sit here -- and when I do my work, I do it with thoroughness and with clarity.

So if -- you know, in the short time I have here, it is simply not possible for me to look at everything in this patent and see if, for example, the question you're asking is negated or modified by some other patent -- some other figure in the specification or some other paragraph, you know.

It's not enough to just look at a figure and make a conclusion because that would be slipshod because there may be other figures that modify the conclusion that one makes or that might augment some information about the Figure 2 that you talk about that gives me a different conclusion. Or there might be something in the spec that says something different. There may be something in the claim that modifies it.

And so therefore it's simply not possible for me to give you an answer.

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And like I said, arguendo. So therefore I'm not able to say whether this is -- you know, this predates Dong in terms of --

Q And I am going to cut you off right there, Dr. Khatri, because I'm not asking you to assume anything or argue arguendo. So --

(Simultaneous crosstalk.)

MR. LOWRY: It's inappropriate --

MR. JENSEN: Let's move on to another topic --

MR. LOWRY: -- it's inappropriate to not let him finish --

(Simultaneous crosstalk.)

THE COURT REPORTER: I'm sorry, I can only take one at a time.

MR. LOWRY: Thank you. I'll go ahead.

I'm just going to put a standing objection here for counsel -- petitioner interrupting the witness after, you know, about less than a minute of his -- of supplying an

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answer to a question he asked.

That's inappropriate and borders on badgering the witness.

MR. JENSEN: I disagree.

Let's move on.

BY MR. JENSEN:

Q Let's fast forward, Dr. Khatri, to the 2020 time frame.

Who were the major companies in the nash -- strike that.

Who were the major companies in the NAND flash memory market around the 2020 time frame?

A You know, I'm not an expert in the business side of things, so I wouldn't be able to give you an answer.

But, you know, I can give you a -- you know, some companies. There may be more that might be there that I might not be aware of, but, you know, I mean, the obvious ones are the ones that we can go to Best Buy when we got -- buy NAND flash memory, but there will be others as well.

So I mean, I -- this answer I cannot give you not being a businessperson.

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Q Yeah, but from a technical perspective, who were the companies that were active in the NAND flash memory space around 2020?

A I mean, this would be a subset. I really couldn't give you -- I mean, I don't follow market trends like that. I follow the technology and not the market trends.

So I couldn't give you an answer that -- you know, like who all these -- you know, all the players in the NAND flash technology would be at that time in the -- I think you said in the 2020 time frame.

Q Yeah. Can you name any?

A Yeah. I mean, there's -- you know, there would be KIOXIA -- I mean, and this is a subset, so really, I don't purport to suggest that this list is complete in any -- by any stretch of the imagination.

But there's YMTC, there's Micron, basically the parties in this lawsuit. There's others as, you know, KIOXIA. There's, you know, High Links.

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There may be others as well.

And, again, I'm not trying to suggest that this is a comprehensive list. This is just some names that come to the -- you know, come to me at the top of my head.

Q You mentioned KIOXIA.

Is that the company -- strike that.

Was KIOXIA formerly known as Toshiba?

A I don't know the exact business genetic -- you know, the business genealogy of KIOXIA or basically the provenance of KIOXIA.

So, again, I mean, you know, I've given you some names. These are not complete. These are just some names that come to the top of my head when you asked me that question.

Q Would Samsung be another company that you're familiar with as a participant in the NAND flash memory industry around 2020?

A I would say --

MR. LOWRY: Objection to form.

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A Again, you know, like I don't want to sort of give you -- or suggest that I'm trying to give you a complete list, but Samsung, yes, was also a player.

THE WITNESS: I think it's around noon for me. So it would be a good time if I could take a break for lunch, you know, maybe about an hour?

MR. JENSEN: Yeah, did you want to break now or -- I mean, we can, if you'd like.

THE WITNESS: Now is a good time.

Now is -- sorry, I'll say that again. Now is a good time.

MR. JENSEN: Okay. Let's take a break then.

THE WITNESS: Okay. Thank you.

(Whereupon, a brief recess was taken from 12:02 p.m. to 1:00 p.m.)

BY MR. JENSEN:

Q Welcome back, Dr. Khatri.

A Thank you.

Q Did you speak with your counsel during the break?

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A Yes. I mean, just checked in and, you know, how -- he was asking how I was feeling and stuff.

Q Did you discuss the substance of your deposition with him?

A None. We did not.

Q Okay.

So before the lunch break, we were talking about some of the companies who were, you know, active in the flash memory space, you know, in the 2020 time frame, and then you mentioned several companies.

Let me start with YMTC.

Are you aware of YMTC selling a stacked 2D NAND product in 2020?

MR. LOWRY: Object to form.

A Yes. Like I said, right, I don't follow the business side of things. I don't follow like which company is releasing what product in what year and, you know, like in this so encyclopedic way.

So I guess, you know -- and I sort of prefaced my answer to your question saying that -- you know, with exactly that

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statement, that I don't follow the -- you know, the business side of things and the -- you know, product releases and stuff.

So I wouldn't be able to answer that question, you know, because it's going to hyper sort of business -- business related, and I guess that's not something I follow in that manner.

Q Well, let me rephrase the question slightly.

Are you aware of YMTC making a stacked 2D NAND device in 2020?

MR. LOWRY: Objection to form.

A Again, my answer would be unchanged. I'm saying I don't follow product releases of different companies, you know, and in particular what time frame they're released, what product and stuff.

You know, that would take, you know, research to do, and that's -- you know, my research and my sort of -- you know, my research and, you know, my efforts are more directed towards the technical side of things.

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Q Yeah, so I'll rephrase it again.

Are you aware of YMTC developing a stacked 2D memory device in 2020?

MR. LOWRY: Object to form.

A I guess -- you know, I mean, I can repeat my answer, but I'll sort of say like, you know, I'm not following -- I don't follow YMTC or any other company at that level to know whether internally they're making a certain product or not making a certain product.

I mean, that would require me to be privy to internal YMTC company strategies and details, and I'm not privy to that.

Q Are you aware of YMTC offering a vertical 3D NAND memory product in 2020?

MR. LOWRY: Object to form.

A You know, again, like I said, I've been aware of YMTC as a player in the NAND flash, you know, space, and, you know, I mean, again, I do not follow their individual products or their internal strategies or an internal, you know, product releases or their internal

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development details. I just -- I'm not privy to those details.

I am aware generally that they are a player in the 3D -- I mean, in the flash memory space, so just like the other names that I gave you.

So that's something I -- you know, I really sort of mentioned, some of the names. And then those -- the list of names of companies that I gave you wasn't necessarily comprehensive at all. There might be others that, you know, I might have either sort of omitted to mention or that they are players and I don't happen just to know how to know that.

Q In the 2020 time frame -- in the 2020 time frame, what was the prevalent NAND flash memory technology?

Was it stacked 2D NAND or vertical 3D NAND?

MR. LOWRY: Object to form.

A You know, once again, I don't know the fine details of that.

My guess, based on the evolution of technology and the fact that, you know,

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certain 3D -- certain styles of 3D NAND were, you know, were heavily researched at that time, based on some of the references that I have included in my declaration, I mean, I would think that they would have been, you know, a large number of 3D NAND offerings by that time frame.

And many of them, you know, are mentioned in my declaration -- I mean, as citations in my declaration.

Q Would that include vertical 3D NAND?

MR. LOWRY: Objection to form.

A I don't know what you mean by "vertical 3D NAND." I don't know if that's -- you know, well-formed technical sort of, you know, term.

Q I'm using that term the same way that you use it in paragraph 70 of your declaration.

A Let me look at the declaration really quick.

Q This is your POR declaration.

A Okay. I'm trying to reorient myself.

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What exhibit was that?

Q That's 2028.

A 2028, oh, yeah, of course. I remember now.

So let's see...

And I'm opening it now, and what paragraph did you mention?

Q Paragraph 70.

A Paragraph 70, let me go there.

Paragraph 70. Let's see...

Right. So see, if we just say vertical 3D NAND by itself in isolation, that's kind of ambiguous.

But here, you know, the paragraph 70 -- if I read the first line of paragraph 70, it says: "The 2D NAND-based Stacked and Multi-layer NAND designs are not the same as vertical 3D NAND as recited in the '941 Patent because the cells are not arranged vertically from bottom to top."

So this paragraph -- so first of all, right, I'll reemphasize that, you know, this was a minor typo in this line, which I mentioned to you earlier, where in

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the first line it should say multi-layered TFT NAND designs, as opposed to multi-layer NAND designs.

With that said, you know, the -- to answer your question, the, quote, vertical 3D NAND language that's used in this sentence is qualified. It's qualified by the following, you know, language which makes it pretty unambiguous in context.

And that follow-up language is: "As recited in the '941 Patent because the cells are not arranged vertically from bottom to top."

So that's the qualification I gave to that -- to that -- you know, to that text, which is vertical 3D NAND.

Q Yeah. So using the definition that you just provided for vertical 3D NAND, my question is: Was vertical 3D NAND known to POSITAs in 2020?

A In 2020, to POSITAs, you know, there was -- I wouldn't use the word "vertical 3D NAND" in isolation, but I would say, you know, there was vertical -- you know, there was 3D NAND in which cells

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were arranged vertically from bottom to top.

But there were also other topologies, and so it was not the only topology. There were multiple sort of competing, if you will, 3D NAND -- 3D, you know, NAND flash topologies.

Q What was the prevalent topology -- strike that.

What was the prevalent NAND flash topology in 2020?

A There were many based on the research I've done. I've seen multiple of -- you know, multiple of these, and some of them I've cited in my declaration.

I could sort of point them to you, if you wish.

Q No, that's not necessary. I just want to know was any one of those more common than the others?

A You know, in -- I mean, there would have been multiple of these. There have been -- a lot of them were, you know, like produced from different research groups, you know, and different companies.

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And for the different applications, there was different 3D technologies that would have been favored by -- you know, for different applications.

So one could not make a universal statement that this was the -- you know, the only technology or the only 3D NAND flash technology or something like that.

Q Yeah. So I want to drill down on that a little bit.

My question wasn't, you know, was vertical 3D NAND the only NAND flash technology in 2020.

And my question is: Do you have any basis to dispute, Dr. Khatri, that vertical NAND flash memory was the prevalent NAND flash memory technology in 2020?

MR. LOWRY: Objection to form.

A So, again, you know, the use of the question as posed is ill-formed because to use the language "vertical NAND technology" by itself, right, is ambiguous, you know, and therefore that question is

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not -- does not really make complete sense.

Q What's ambiguous about it?

A Because when it says vertical, it doesn't say what is vertical. What is arranged vertically.

Q Okay.

A What is being arranged vertically, I mean, that needs to be clearly stated in the question.

Q Yeah, let me clarify then.

Do you have any basis to dispute that the prevalent NAND flash technology in 2020 used vertical memory strings?

MR. LOWRY: Object to form.

A Let's see...

If you -- again, this is not terminology that's commonly used in the literature of, you know, NAND flash.

So basically I'm hesitant to answer this because you may mean something by "vertical memory strings."

And that's not completely a term that's a term in the art, and therefore it leaves, you know, an opening -- I mean, if I answer it in either direction, then it

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could be that we -- you know, that we understand different things by "vertical memory strings."

Q Let me rephrase then and I'll use the same term that you use in your declaration in paragraph 75.

A Let me go there real quick.

Q You can go there.

You use the phrase "vertical 3D structure," and this is the example you pointed to me before in the morning when we were clarifying, you know, some terminology.

So I'll ask the question using your own words to make sure there isn't any ambiguity in the question.

A Okay.

Q Do you have any basis to dispute that in 2020, the prevalent NAND flash memory technology implemented a vertical 3D structure?

A Yes. So again, you know, there was -- and when you say the vertical 3D structure, you, I think, mean -- the vertical 3D structure that I'm referring to

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in paragraph 75 of my declaration -- my POR declaration, is this correct?

Q Yes.

A Okay.

So using the -- let's say using the "vertical 3D structure" of paragraph 75 of my declaration, yeah, and your question is, was that "vertical 3D structure" the prevalent 3D structure in 2020.

Is that a correct understanding of your question?

Q Well, let me just ask the question cleanly because I think it's a little bit different.

In 2020, was the prevalent NAND flash memory -- strike that.

In 2020, did the prevalent NAND flash memory use a vertical 3D structure?

MR. LOWRY: Object to form.

A May I ask you to repeat that question, please?

Q Yeah.

In 2020, did the prevalent NAND flash memory devices use a vertical 3D structure?

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A I see.

So in this time frame, you know, in this -- around the 2020 time frame, they were -- you know, by this time, there were a large number of, you know, 3D -- you know, of 3D NAND technologies that had been explored and were actively being explored as well.

So, you know, just like anything else in the technology space, in the semiconductor space and in the semiconductor memory space, you know, there's really no -- you know, there's no sort of sitting target or there's no -- not sitting target, but there's no sort of static, you know, approach that everybody ends up using.

You know, the companies that design, you know, flash -- you know, 3D flash memory have -- you know, have technologies that they, you know, rarely disclose.

So it's, first of all, not very possible for a person outside the company to know what internal approaches that

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they're using are because this is a highly competitive marketplace, and even releasing the -- so the architecture or any electrical details of their internal technology that they use would be something that will be a competitive disadvantage to a company in the space.

So first of all, with the space being so competitive, it was -- you know, companies kept things very close to their chest, and therefore it was hard to know this.

Secondly, as I said before, you know, there were many competing vertical 3D NAND topologies and architectures, and there's extensive, you know, literature in the academic -- you know academic literature in this and many, many, you know, publications that describe some of these with varying levels of detail.

But it's -- but there are many different topologies and architectures that are described, you know, and so therefore it is not something that -- there were a lot of choices.

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And it's not completely clear that, as you're suggesting or asking, whether the vertical -- you know, vertical 3D structure, as I show in paragraph 75 of my POR declaration, whether that vertical 3D structure was the prevalent 3D structure.

Q So you simply can't say one way or the other what was the prevalent memory architecture in 2020?

MR. LOWRY: Objection to form.

A Like I said, there were many competing structures, and there was active research, and just like there is in -- you know, in the VLSI and semiconductor space.

There's active research going on all the time about these structures. There were many structures that were available, and the specific structure that the particular company uses for its product is something they don't reveal regularly and this is kept close to their chest.

So that question is hard to definitively answer because there were a lot of choices and the -- you know, and the

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specific structure that individual companies use is not something that they -- that they regularly disclose or reveal.

Q Is it your testimony, Dr. Khatri, that companies such as Samsung, Micron and YMTC do not issue press releases informing the public whether they use vertical 3D NAND memory strings in their products?

MR. LOWRY: Objection to form.

A So certainly companies, you know, do release press releases and do have publications.

But it's from -- you know, it's not clear whether that's the prevalent design that they're using. They may be using other sort of topologies in their -- you know, in their 3D NAND flash that they didn't release.

So just a press release, which is basically a -- you know, a public-facing document, is not something one can readily make a conclusion on about -- you know, make an accurate sort of estimation on to answer your question.

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I mean, certainly, yes, there are press releases, but if I relied only on a press release to answer your question, I don't think that would be a very sound way to -- you know, a sound and sort of completely objective way to answer your question.

Q Have you seen any market share or market data reports that identify the percentage of the NAND flash memory market that is vertical 3D NAND?

MR. LOWRY: Objection to form.

A So, you know, like I've said before, right, you know, I don't follow the marketing side of these -- you know, of the industry. I don't -- I think that I've said this more than once in this deposition before.

And your question is literally asking like do I follow the marketing technology -- you know, the marketing side of the 3D NAND technology and, you know, what fraction is used and, you know, what is more prevalent or not.

So that's literally a marketing

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question, which I've already testified to as something I don't follow.

I follow the technology and I'm -- you know, I mean, that's basically my -- you know, that's basically what I'm interested in.

Q And you're not aware of what technology has been accepted in the marketplace?

MR. LOWRY: Objection to form.

A I'm absolutely interested in the technologies that are available to the marketplace and the pros and cons of them, why one is better than the other, the electrical details of these different options, you know, the susceptibility of these of different electrical effects, the relative metric -- electrical and performance metrics, like speed and, you know, susceptibility to disturbs and power consumption, energy and so on.

So these -- this is the -- this is where, you know, as a technologist and as a professor and as a person, you know, interested in this space, right, you know,

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that's basically the -- sort of the part of the technology that I -- that I follow.

And in following that, I mean, I see the different options. I see the rapid, you know, evolution of different technologies and topologies of this, and I see a continuous movement there. I see a movement -- I mean, I see changes happening -- I mean, changes that yield better memory in various different, you know, metrics. I see those changes happening all the time, you know.

And that's basically, you know, what I follow, not the really -- not the marketing side of the whole thing.

Q Do you know whether vertical 3D NAND products have been accepted in the market?

MR. LOWRY: Objection to form.

A I don't know what you might mean by "accepted."

Q I would say, you know, purchased, bought?

A Purchased? Sorry?

Q Purchased -- let me just ask a

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clean question.

Has vertical NAND flash memory succeeded in the marketplace?

MR. LOWRY: Objection to form.

A Yeah. See, again, you know, the nomenclature, right, vertical NAND flash memory, that's -- like I've said, there are many flavors of, you know, 3D NAND flash.

Now, when you say vertical NAND flash, really, again, I'm sort of way what do you mean by vertical NAND flash?

For a while, we were talking about "the vertical 3D structure" that is cited in paragraph 75 of my declaration.

But now if the --

Q That's what I mean, is -- let me just ask it using that verbiage.

A Yeah.

Q Do you know if the marketplace has accepted vertical 3D structures for NAND memory devices?

MR. LOWRY: Same objection.

A Using the topology structure that I cite in paragraph 75, which is basically something that, you know, is

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shown in the figure on the next page, the figure at the bottom of paragraph 76, that topology is -- you know, is used in industry.

And there are others as well. This is a completing -- this -- you know, like, these different topologies have different electrical metrics. And so, you know, companies would be using -- I mean, it might even be possible that a single company has multiple topologies or multiple architectures, not just the "vertical 3D structure."

But these different topologies and architectures are targeted towards different market segments or different sort of customer bases and such because they have -- they have different electrical characteristics and different performance -- electrical performance metrics.

So this is a rich space. There are a lot choices for the companies in terms of how they implement 3D NAND flash. And, you know, and they do use those

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different options that they have on the table.

Q Let me direct you to paragraph 16 of your POR declaration?

A 16, let me go there.

Hold on, please. 16. Okay. There it is.

Yeah, I'm there.

Q Yeah.

And in the first part of that paragraph, you say: "At Texas A&M I teach classes that cover memories extensively."

Do you see that?

A Yes.

Q How long have you been teaching memory -- or courses that cover memories as a professor?

A So, you know, I started my first in 2000, so that's 26 years ago. And, you know, I've been covering, you know, memories of various forms in multiple courses as I list, you know, in this paragraph 16, you know, from that time.

So, you know, this is basically something that I've been doing from the

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start of my academic career.

Now, sorry, one more thing.

So the courses listed here -- let me just double-check. That's ECEN 752, and I just upgraded this course to have a lot of more flash in it.

But, yeah, 752 and then 449/749 and then there should be -- yeah, there is 454 also at the bottom of the paragraph.

All these are courses that I've taught and some of them developed at Texas A&M, you know, and they all have various, you know, aspects of, you know, memories and also flash memories in them in various different -- you know, viewed from different angles, if you will, different technical angles.

But, you know, my first academic -- so this -- sorry, all I want to say is this is basically the listing of courses I teach at Texas A&M, and I've been at Texas A&M since 2004.

Before that, I was at the University of Colorado Boulder, and I did have -- and, you know, and right from the

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first academic appointment, which was in 2000, I did have a circuit design course, a grad -- what was it graduate -- yes, it was a graduate circuit design course in Boulder as well.

And that also had extensive coverage of memories and, you know, all -- circuits in general and also memories, basically the whole circuit design semiconductor VLSI space.

Q As part of your -- the courses you mentioned, did you teach students about NAND flash memory?

A Yes. So, you know, I've always taught that, you know NAND flash and NOR flash and general flash memory is just a fascinating technology in a lot of ways and, you know, I guess I could talk about it for a long time, but I won't.

But, you know, it uses a flash memory cell, which is -- you know, which fails after a small number of writes. You know, it's just a few hundred thousand writes and the cell is broken.

But despite that, you know, we

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as electrical engineers have used this to design NAND flash and NOR flash memories, which could be used in many different applications, and somehow worked that out well, you know, with very clever, you know, circuit and cryptography techniques, worked around the limitations of the cell and made it a product -- I mean, made from it products that are industry grade. And I think that's just fascinating.

So there's -- I teach, you know, NAND flash and NOR flash from that point of view because I think they're a marvelous invention. And that continues to evolve and continues to grow and, you know, in many interesting and technically, you know, interesting ways.

So NAND flash memory is something I talk about. I think I even say that somewhere in one of these paragraphs, that I talk about NAND flash memory, but if I didn't, because this is just sort of a general background, then, you know, I'll clarify that, yeah, I do talk about NAND flash in my courses.

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Q Do you teach students about NAND flash with a vertical 3D structure in your courses?

A So vertical, various different -- let's say again, vertical 3D structure, are you referring to the structure from Figure 70-- at paragraph 70 I take it, yes?

Q Yes.

A So I teach in my -- in my research program, you know, I have an extensive number -- I mean, an extensive number of papers and a number of students even currently working on flash -- you know, flash transistors or flash devices for non-traditional applications, for non-memory applications.

I do talk about that somewhere in this as well I think.

So anyway, in that discussion, we've done some extensive work on different 3D structures, not just the 3D structures shown -- not just the 3D structures cited in paragraph 70, which is the -- you know, which is the 3D NAND flash structure in

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which the transistors are placed in the vertical direction, as you see in the figure following the paragraph 70.

But we talk about other 3D topologies that are actively being researched as well and that are being published, and we see if those 3D topologies or architectures can be more useful, you know, to our particular use of flash technology.

And our particular use of flash technology -- let me see as I think it's described in one of these paragraphs. I'll just sort of go to that. Yeah, let's see...

Right. If you look at paragraph 16, towards the end, it says: "Some specific recent research topics include circuit design using floating gate of flash devices."

You know, and this -- let's see. So -- and we use these flash devices for many non-memory applications, such as wireless, you know, power delivery, battery-less electronics, machine learning

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architectures, secured computing.

And, you know, also, if you see later in that paragraph, you know, been working on artificial intelligence and machine learning signal systems, which will be used in large language models.

And we're doing flash-based realizations of these, and when we do that, we've been extensively looking at 3D NAND -- 3D flash approaches, and even modifying some existing manufacturing approaches for 3D flash to sort of show on that topology for our applications, which are pretty vast, you know, in this space.

So --

Q How long --

A -- the short answer is yes, I've been extensively looking in the -- you know, our research program with my Ph.D. students how to use 3D flash -- various forms of 3D flash and, you know, not just the one that is shown in paragraph 70, but various other, you know, topologies and architectures as well.

Been using those to apply to our

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applications and, you know, for the Ph.D. research that my students have been doing.

Q How long have you been teaching students about NAND flash with vertical 3D structures?

MR. LOWRY: Object to form.

A That's a hard question to answer really, but, you know, because what happens is that, you know, I have many students come to me during office hours, for example, and then, you know, they'll bring up something about memory, and I'll be excited about let's say NAND flash, and I'll, you know, tell them about the most recent paper I read about 3D NAND flash, right, or, you know -- you know, different kinds of NAND flash or NOR flash or flash technologies in general and, you know -- and even how people do error correction for memories and stuff.

So this become as spontaneous discussion. This is not a discussion that necessarily is -- you know, is cryptic, you know.

So when you asked me when that

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happened, I wouldn't really know because I do have a lot of students drop in for office hours because I guess they enjoy it and I enjoy it, too, so...

Q Yeah, let me just maybe narrow the question in terms of, you know, the actual course material that you present in the classroom.

In that regard, you know, how long have you been teaching students about NAND flash with vertical 3D structures?

A So in terms of the course material for my courses, right, the -- you know, the course material is -- you know, like the PDF notes or something that I might have, those are, you know, frequently augmented by papers that I might, you know, ask them to read or papers that I might present spontaneously and so on.

So the course material is not necessarily the best -- what would I say -- a guide to go by, you know.

In my courses, I discuss, you know, NAND flash, which would include the different ways of doing 3D NAND flash, you

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know, in spontaneous meetings during office hours when things come up like that or also papers that I might assign to students to review or papers that I might present in my class and such.

So there's a variety of ways that this gets disseminated.

And a lot of this is also in my research group. We've -- you know, we are actively interested in the use of 3D flash for all these applications that I mentioned to you from paragraph 15 because I have an extensive focus -- in fact, a majority of my research focus is on flash memory for non-traditional, non-memory applications using both 2D and 3D NAND flash.

Q I did see one of your patents directed to that in preparing for the deposition.

A I see. And there may be a couple more on their way, yeah.

Q Well, congratulations in advance.

A Well, I hope they get through.

Q Let's go to the '941 Patent,

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which is Exhibit 1001.

A Just one second.

May I close the declaration, or you need it around?

Q I think we'll come back to that. So I would just leave that one open, but anything else you can close.

A Okay. I'll do that. I'll leave it open and close everything else.

And now, sorry, you said let's open what?

Q The '941 Patent.

A The '941 -- that's 1001, yes. Okay.

Q Yes.

A Excuse me.

Q Have you read the '941 Patent, Dr. Khatri?

A Just one second. Let me open it.

Okay. I have the '941 Patent open, yeah.

And your question was?

Q Yeah, have you read the '941 Patent?

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A Yes, so I've read -- in coming up with my opinions, I have read the '941 Patent.

Q Did you understand the '941 Patent?

MR. LOWRY: Objection to form.

A I mean, I don't understand that question.

I mean, I don't know if that's -- you know, like if I hadn't understood it, then I would not be able to provide opinions on it, I would suspect.

So my answer to that is yes, I understand this patent.

Q Okay.

Is there anything you did not understand in the '941 Patent?

A You know, if you have a specific aspect of it and you want to ask me if I understand it or not, I can answer that to the best of my ability.

Q I didn't have anything in particular in mind. I just was wondering if there was anything that you read and didn't understand about the patent.

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MR. LOWRY: Objection to form.

A So I have read the patent and, you know, to me, the patent is understandable.

Q Okay.

A And I've read it with the view, you know, of the mindset of a person of ordinary skill in the art.

Q Let's look at Figure 1 of the '941 Patent.

A Let me go there real quick. Oh, Figure 1. Okay.

All right. I have it in front of me.

Q And you see on kind of the bottom, there's a box that's labeled "Controller" with the numeral 190?

A Yes, I do see that box.

Q Okay. And then there's an arrow that connects that box to another one, a kind of a taller rectangle.

Do you see that?

A I don't see an arrow there. I don't know what you're talking about.

Q Well, I didn't say an arrow.

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There's a line connecting the controller?

A Yeah. So then if you look at Figure 1, you know, through the -- sort of the left and the bottom of Figure 1 is a box labeled "Controller" and its numeral is 190.

And to the right of the box is sort of like this -- is this wire that connects it to, you know, a larger rectangle, you know, which is sort of -- which is in the -- which is in that figure as well.

Q What is the larger rectangle that you refer to?

A So, you know, I mean, this larger rectangle -- let's go to the -- I'll go to the specification, you know, and then basically read from there. So that's the most -- you know, the most definitive way to look -- you know, to talk about this.

So I will look at -- let me just see real quick.

So again, let's look at the detailed description that is described in the specification of the patent so that we

stay with the intrinsic evidence.

And the detailed description on page 2 at the bottom, line 63 onwards-ish, it says: "Figure 1" -- which is what we're talking about -- "illustrates a memory 100" -- so the entire structure of Figure 1 is memory 100 because it has a label 100 there -- "according to an embodiment. The memory 100 may include a first portion 110, a second portion 120 and a controller 190."

So again, if we look at Figure 1, you know, we see a numeral 110, which is, you know, beside an arrow on the left side of Figure 1.

So that is, according to the specification of the patent, a first portion 110.

And we also see a numeral 120 next to an arrow on the left side of Figure 1, and that is thought to be a second portion 120.

And then the specification continues and says: "And a controller 190."

So the controller we just saw is

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a controller which is, you know, part of the memory 100.

So the memory 100 so far from my reading of this portion of the patent has a controller 190, and a first portion 110, and a second portion 120.

Q And with respect to the first portion 110 and second portion 120, those are portions of what?

A So I mean, as the -- as the -- I mean, I'll read the line again.

"The memory 100 may include a first portion 110 or second portion 120."

Now, this tells me that the first portion 110 is -- you know, is part of memory 100, and the second portion 120 is also part of the memory 100.

Q Does Figure 1 depict a memory string?

A So to answer that, let's look further.

The next line, which is starting column 2, line 65, says: "The first portion 110" -- which we just talked about -- "may include a first word line WL1

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to a kth word line WLk from bottom to top."

So now this spot is disclosing that there is a verticality to this structure that if you look at the first portion 110 and match it in the figure with the specification, we see that includes -- it includes a first word line WL1, and you can see that WL1 in the bottom of the big rectangle in Figure 1.

And then it says: "To a kth word line WLk" -- you can look at the kth word line WLk, which is towards the -- sort of higher than the halfway up the -- you know, up the two -- up the two portions.

And so the specification now says, you know, this first portion includes a first word line WL1 to a kth word line WLk from bottom to top.

So this tells me when I read it, and it tells a POSA from the plain and ordinary meaning of bottom and top, that WL1 is arranged at the bottom and WLk is arranged towards the top.

Q Yes. But so my question is: Would a person of ordinary skill in the art

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understand that Figure 1 in the '941 Patent depicts a memory string?

MR. LOWRY: Object to form.

A So a person of ordinary skill in the art would know that when you have word lines, word lines connect to memory strings. So -- you know, otherwise the memory wouldn't be functional.

A person of ordinary skill in the art also knows from the description of the -- you know, a description of the patent and this motivation that the patent applies to 3D -- like, you know, to three-dimensional memory structures.

So they know that this is a 3D structure, and if it has word lines, it must have -- you know, it must have flash memory because the patent is thought to be about flash memory, and if it has flash memory and it has a word line, then it would have -- because flash memories are reinstate -- the NAND flash memories are reinstated strings, it must have a NAND string.

You know, the description of the

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patent from lines 20 -- sorry, column 1, lines 26 to like 41 says that to a person of ordinary skill in the art.

The ordinary skill in -- person of ordinary skill in the art realizes that this memory is about a three-dimensional structure or -- you know, because that's in line 27.

Also, it relates to three-dimensional stack of NAND flash memory because that's in line 28.

And also, it talks about, in line 30, that the three-dimensional structure of a memory can include many layers to be more -- to store more data.

And more -- further, let's see...

Yeah. So again, if you look at again the last part of this, which is lines 39 to 41, it talks about, you know, that in the context of three-dimensional memory, there is a need for techniques to reduce program -- you know, to reduce disturbances like program disturbance and password disturbance.

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So from all this, a person of ordinary skill in the art knows that the context of this -- you know, of this figure and the rest of the patent is three-dimensional NAND flash memory, and, you know, that's corroborated by the fact that the description we just read talks about the first portion and the second portion and then these -- both these portions, the first portion having word lines WL1 to WLk from the bottom to top.

So one can see that wherever the controller connects to this figure is where -- what is the bottom of the memory -- of the 3D memory.

And the same is described for the second portion 120 at the bottom of column 2, which it says is formed above first portion 110.

So we can see Figure 1 and see that portion 120 is, you know, above portion 110, and now we can -- a person of ordinary skill in the art knows that this is basically referring to the physicality of these word lines.

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And finally, on, you know, this description of the second portion 120 says that it includes the k+1 word line, WL(k+1) to an mth word line, WLm, from bottom to top.

And again, in the figure, if a person of ordinary skill in the art looked at portion 2, they see that the bottommost word line is WL(k+1) in the figure and topmost word line WLm in the figure.

Q Do you see the label WLx in Figure 1?

A Just one second.

Do I see the label WLx, you said?

Q Yes.

A Yes, I do see it.

Q And what does the W -- what does acronym "WL" stand for?

A So WL, if you -- again, if you go back to the specification just to be, you know, precise in our, you know, interpretation of the acronym WL, you -- if we go to column 2, line 66, it says: "A first word line WL1." And then it also

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says at the end of that line: "A kth word line WLk."

Similarly, if we go to column 3 in the first and second lines, it says: "A (k+1)th word line WL(k+1)" and "an mth word line WLm."

So from all these disclosures of the word "word line" being used, you know, together with the name WLm or WL(k+1), you know, a person of ordinary skill in the art would conclude that "WL" stands for word line.

And this is a common electrical signal in memories, and so this would make sense to a person of ordinary skill in the art.

Q And what does WLx refer to?

A So if I read further on column 3 of the patent, let me see, what line we're talking about...

If you look around line 9, it says: "When an xth word line WLx" -- so it's sure telling us that WLx is the word line whose index is x, it's the xth word line -- "is used to perform program

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operation, the controller 190 may apply a program voltage Vpgm" -- which would be like reprogram -- "to the xth word line WLx."

So if I stop there and if I'm a person of ordinary skill in the art and I'm reading this, I'm understanding that WLx is the xth word line from what I just read in column 3, line 9, and that it is used to perform a program operation. And during that program operation, the controller 190 will apply a program voltage Vpgm to this particular word line WLx.

Q What is being programmed by the word line WLx?

MR. LOWRY: Object to form.

A What is being programmed is a -- let's see...

I want to be sort of -- you know, sort of close to the language of the patent. So I'm going to be -- so I'm going to look for where that -- where I can find you some -- you know, the -- where in the specification I can find you what is being programmed.

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Q You can look at column 3, line 7. It refers to a memory cell, if that's helpful.

A Okay. Let me see that and maybe I'll see something else as well if there is something useful, so...

Okay. Let's see. So I think -- if you look at column 3, I think you meant line 6, right?

Q Well, line -- yeah, whatever, 6?

A I'll read the whole sentence just for context so that it's not just fragmented, but column 3, line 6 to 8 reads: "A program operation said in the text" -- or like that means mentioned in the text -- "may be an operation for programming a memory cell formed using, for example, a set of transistors."

So basically this makes clear that from -- in the intrinsic description of the patent that when the patent talks about a program operation, quote-unquote -- or let me repeat that.

It makes it clear that when the patent talks about, quote -- sorry, let me

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start again.

Now, it makes it clear that when the patent talks about a "program operation" in the rest of the patent, it means an operation for programming a memory cell. That's basically what they mean by a program operation.

Q And is there a memory cell associated with each of the word lines in Figure 1?

A May I ask you to repeat the question?

Q Is there a memory cell associated with each of the word lines in Figure 1?

A I think that there would be -- you know, from -- there would be at least a memory cell associated with each word line, otherwise you wouldn't have a memory.

And a person of ordinary skill in the art would readily understand that.

Q On the right side of Figure 1 --

A May I briefly interrupt?

Q Oh, go ahead.

THE WITNESS: So we've been

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going for close to an hour now, so -- and I think as the day goes -- as the day gets longer, you know, I might request a little more frequent breaks because I like to be fresh during my deposition.

So I would maybe at this point, if you're close to the end of this line of questions, I'd like to request a break.

MR. JENSEN: We can break now.

THE WITNESS: Okay. Thank you.

(Whereupon, a brief recess was taken from 1:53 p.m. to 2:03 p.m.)

BY MR. JENSEN:

Q Dr. Khatri, does Figure 1 of the '941 Patent show a substrate?

A So the Figure 1 of the '941 Patent -- let me look for that language just to be sure first. But -- let's see...

And then -- let's see. So I don't see the word "substrate" on there, you know.

But I can see how a person of ordinary skill in the art would just look

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at the language of this that I just read to you, right, which is that the -- that there's the first portion 110, a second portion 120, you know, with word lines going from WL1 to WLk from bottom to top for the first portion, and then word lines WL(k+1) to WLm going from bottom to top for the second portion where the second portion is formed above the first portion.

So this, you know, a person of ordinary skill in the art readily sees, you know, and, you know, just like in NAND memory -- you know, in 3D NAND memory, you know, there is basically -- the substrate is -- I mean, the substrate is basically a plane on which all of this is built.

So a person of ordinary skill in the art would readily know that.

Q Does -- yeah, so I appreciate that response.

Just so my question is clear, does Figure 1 of the '941 Patent illustrate a substrate?

MR. LOWRY: Object to form.

A You know, like I said, Figure 1

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doesn't show the substrate, but a person of ordinary skill in the art, knowing that this is a VLSI -- this is a VLSI chip or a -- you know, a semiconductor that's a 3D memory would know that there is a substrate because that's, you know, commonly understood.

Q Does Figure 1 of the '941 Patent illustrate a source select gate?

A Does Figure 1 -- sorry, can you repeat the question?

Q Does Figure 1 of the '941 Patent illustrate a source select gate?

MR. LOWRY: Object to form.

A So the purpose of Figure 1 is to illustrate the relative orientation of these -- you know, of the first -- sorry, of the first portion 110 and the second portion 120. And to -- you know, and to sort of assign variable names to their word lines -- that's WL1 through WLk -- for the first portion 110 and WL(k+1) to WLm for the second portion 120.

So the purpose of this is to describe the word lines and their -- you

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know, their numerals of their variable names and their relative orientations, right. WL1 through WLk is from bottom to top and WL(k+1) through WLm is from bottom to top.

So that's the purpose of the -- that's the purpose of this figure because the figure is -- you know, I mean, the patent is interested in the voltages you would apply to the word lines.

And so for that reason, there's no -- a person of ordinary skill in the art would not see a need for it to show other, you know, specific, you know, structures like you're mentioning. The structures it mentions are complete, the structures and variables that it mentions. That is the word line, the first portion, the second portion and their orientation from bottom to top.

All of that is complete for a person of ordinary skill in the art to understand the patent and the voltages that are applied to the word lines.

Q With respect to the voltages

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that are applied to the word lines, let me direct your attention to the right-hand part of Figure 1.

And do you see the labels V1, V2, V3 and V4?

A Excuse me. I do -- on the right side of Figure 1 -- just one second. Let me -- I'm trying to track or follow along on my -- on the patent specification so that basically I can sort of describe or read the specification that's relevant here and show how it matches.

But -- so if I see Figure 1, on the right-hand side of Figure 1 are labels V1, you know, which from the figure seems to be -- let's see, I can't see too clearly, but let me try to see it in my diagram, in my PDF.

So V1 is applied to WL1 through WL(x-2) from the trigger, and V2 is applied to WL(x-1).

Vprogram is applied to WLx, as we discussed.

V3 is applied to WL(x+1).

And V4 is applied from WL(x+2)

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to WLm.

And this is basically what is also clearly, you know, stated in the specification, which I'll sort of go through.

So in the specification that I already described to you where from lines three -- column 3, lines 9 to 11, it talks about WLx -- sorry, Vprogram being applied to WLx. So that matches the figure. We've already gone over that text.

Then from the -- in columns 3, lines 11 through like 17, it talks about the remaining voltages, so that a first voltage V1 is applied to -- from the first word -- from WL1 through WL(x-2). So you can see in the figure that V1 is applied from WL1 to WL(x-2).

And then also it says a second voltage is applied to WL(x-1). If you look at the figure, you see that V2 is applied to WL(x-1).

And then the spec says the third voltage V3 is applied to the (x+1) word line WL(x+1).

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Once again, we can see V3 being applied to WL(x+1) in Figure 1.

Then finally, the specification says that -- let's see -- that all these voltages -- you know, that x, k, m, et cetera, are positive integers.

And frankly, actually, column 3 again lines 18 to 21, it talks about a fourth voltage V4 being applied from WL(x+2) to WLm.

And once again, we can see WL(x+2) through WLm are driven by V4 in Figure 1.

So in some sense, the specification and the figure are matching, and essentially, the specification is adding clarity saying these V1, V2, et cetera, are voltages that are being applied, and they're being applied by the controller, which you see at the -- you know, which is the controller 190, which you see in Figure 1.

Q Let's go to column 1, line 39 of the '941 Patent.

A Okay. I am -- let's see,

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column 1, line 39. I'm there.

Q And could you just read that aloud, lines 39 to 41?

A Okay. Lines 39 to 41 say that: "Hence, a solution for reducing program disturbance and pass voltage disturbance when operating a three-dimensional memory is in need in the field."

Q What is pass voltage disturbance?

A So let's see. I kind of want to see that I -- or let me read -- let me go into my spec where I believe I've talked about pass voltage -- I'm sorry, my declaration.

So give me a second while I look for -- if I look for the correct language.

Let's see, there's many occurrences of it, and -- give me one second. I'm looking through my declaration, please.

So I think -- I guess the best way to describe it is that figure from -- let me see -- I'm going to open exhibit -- hold on, let me see.

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So there was that figure we described a little while ago from Aritome, which was those six -- you know, those six NAND strings, and they were labeled 1, 2, 3, 4. I'm trying to find it in my declaration real quick.

Q Yeah, I think that's shown in a couple of places. The first one is at paragraph 76?

A 76, thank you. Let me look for it at there. 76...

Give me one second, please.

Oh, yeah. There we go. 76.

Okay. So this is -- you know, this figure talks about program disturbances and in particular, it talks about disturbances in a 3D NAND array.

So if you look -- in this figure basically what's going on -- let's see, where is my mouse? Sorry.

My mouse froze. This is a good time for it to freeze. Give me one second.

So if you look at this figure, the -- if you look at the numeral 1 in a circle, that's the string -- numeral 1

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refers to the string. That's the vertical set of transistors.

And if you look at the table on the -- in the middle of this figure, it says one is a string that's being programmed.

So this string is being programmed. In other words, the -- there's a target cell in this string, a target flash cell that we are programming.

Now, when we try to program the cell, we are forced to leave other cells in the string above and below it on for the string to conduct.

And when that happens -- I mean, sorry, in order for that to happen, we're forced to apply what's called a pass voltage nominally on the other cells in the string.

Now, these cells over time, they're not being programmed but they're just being driven with a pass voltage. And when they get driven with a pass voltage repeatedly, they get programmed very slightly into the -- due to the

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Fowler-Nordheim tunneling phenomenon.

And that's what is called as the pass voltage system. That is you apply a pass voltage to a cell. You didn't mean to program it. It had a certain threshold voltage. You didn't mean to program it. But by repeatedly applying a pass voltage because you're programming some other cell in that string, it has -- its threshold voltage slowly increases, i.e., slowly gets disturbed, and that's what's called as pass voltage disturb.

Now, this disturb is slow because Fowler-Nordheim tunneling is -- you know, is exponential in the electric field. So the formula for tunneling is -- you know, that the tunneling current is -- let's see, is A times the square of the electric field times exponential in minus B divided by the electric field.

So this is a really small disturb that you get but over the number of times that you apply the pass voltage to these cells, their threshold voltage gets changed, gets increased slowly and slightly

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and in an accumulative way, or in a cumulative way, and that's what's called as pass voltage disturb.

I don't know if that was clear -- that's sufficiently clear, but...

Q Looking at the Figure 8.11 from Aritome that you were just discussing, does pass voltage disturb occur on any of the other memory strings besides the one being programmed?

A So, you know, pass voltage disturb would occur on -- you know, on memory strings that are not -- you know, that have a Vpass -- a pass voltage on them. That's basically how that would work.

So if a transistor in a string had a pass voltage applied to it, or actually any voltage applied to it, there would be a small amount of disturb that it incurs, and that's basically just a, you know, electrical fact of life due to this -- the Fowler-Nordheim tunneling, which is the mechanism by which programming occurs in these technologies -- in most of

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these technologies.

Q Could pass voltage disturb occur on the memory string with the label 2 in Figure 8.11.

A So pass voltage disturb would occur on any transistor that has a pass voltage applied to it.

And like I said, you know, even if it's a variation of a pass voltage, like, you know, a slightly different value than the pass voltage, any voltage applied to the gate of a flash transistor, you know, that voltage would induce an electric field in the -- between the gate of that flash transistor or the substate or the body, right, on the -- you know, the ultra thin body or whatever the kind of body it is.

But there would be a voltage -- there would be a voltage across the gate to the body, and that voltage would induce an electric field, which would be the voltage divided by the thickness of the -- of the distance between the two terminals.

That electric field would induce

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a -- you know, a Fowler-Nordheim tunneling current, which I just described to you in words, I guess, and that electric field would cause electrons to get trapped inside the floating gate of these transistors.

And that trapping of electrons was unintended. We didn't mean to program those transistors. We only meant to program the transistors on which we've applied VP -- Vprogram, the programming voltage.

So all these other transistors, all these other flash and disturbs we each are getting that non-programming voltage, i.e., the pass voltages, they're getting slightly disturbed in their threshold voltage and that's the disturb mechanism of pass voltage system.

It will happen to any transistor that gets a pass voltage applied to it.

Q Going back to the '941 Patent at column 1, lines 39 to 41, it refers both to a program disturbance and pass a voltage disturbance, correct?

A Let me go back there, sorry.

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You said the '941 Patent and what lines?

Q Column 1, lines 39 to 41.

A Column 1 -- okay. There we are.

And please repeat your question. I was looking for the...

Q Yeah. It refers both to "program disturbance" and "pass voltage disturbance," correct?

A Yes, I do see that.

Q What is the difference between a program disturbance and pass voltage disturbance?

A Okay. So to answer that, I'll go back to the figure we were just looking at, which is Figure 8.11 of Aritome, and that's shown on page 40 below paragraph 76 of my declaration -- of my POR declaration, Exhibit 2028.

If you look at this figure -- you know, let's look at the figure on the left, that's the memory. That's the 3D NAND flash memory, as it's described in the caption.

And let's also assume that

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string 1, which is one with the circle around it, that's the one being programmed. That's confirmed by the fact that the table in the middle says string in program for the string number 1.

Okay. So that's the string being programmed.

Now, what is it that's being programmed in the string?

The thing that's been -- well, the flash transistor being programmed in the string is among the two flash transistors that are sort of, you know, schematically drawn. It's the top one. Okay. It's the one that's above the other one when it's depicted in this picture.

So if you -- and I think -- I don't know how to describe it because I don't see this in any color -- and I'm color blind anyway, but it's the one that's in lighter ink, the two flash transistors, there's the lower one, which is -- the lower one as depicted, which is in dark ink, and there's the one above it as depicted in a lighter font -- lighter ink.

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So the lighter ink transistor is the one we are trying to program let's say in string 1. That's the one guy they're trying to program.

But the -- but all the transistors that are the light-colored transistors among all six strings, they receive the same program voltage. And -- let's see...

That's confirmed by -- no, that's not the person of ordinary skill in the art, but it is confirmed by the statement in the caption that says: "End strings are connected to the same bit line in the same block" -- that's different, sorry, scratch that.

So all the six lightly colored flash transistors are connected to the same -- same word line, but we are only trying to program string number 1.

So all the other strings, they should not get programmed. String 2, 3, 4 and the other unlabeled strings, the two unlabeled strings should not be programmed.

So we are going to use boost

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modes to not program them. We're going to use what I describe in my declaration as MLSB and such.

But those boost modes, basically they're going to still cost some programming -- some small amount of programming to the lightly shaded flash transistors in string 2, 3, 4 and the two unlabeled strings.

Does that so far making sense -- I mean, am I -- okay.

So those remaining five transistors, they are receiving a program voltage at their gate, but we do not want them to be programmed because we only want string 1's light-colored transistor to be programmed.

So to the extent that the other five flash transistors whose gate is driven by Vprogram that are programmed, that's called program disturb.

We -- the transistors that -- they got disturbed because we didn't want to program them, but they were receiving the program voltage. And their threshold

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voltage will increase slightly because of the programming of the intended transistor, which is the light-colored transistor in string 1.

So that's program disturb. That's one thing that the '941 Patent is trying to minimize, and that was basically coming back to, you know, lines 39 to 41. That's the program disturbance of line 39 of the '941 Patent.

Now, let's come to the second kind of disturb that's mentioned in lines 39 to 41 which is pass voltage disturbance.

Once again, I'll explain it with Figure 8.11.

Now, if you look again at 8.11, all other flash transistors other than the lightly shade ones, the six lightly shaded ones, which all receive reprogram, the other transistors will be receiving a pass voltage so that all that they do is conduct, but we don't want to program them.

So for example, the dark-colored transistors in each of the strings. In

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string 1, there's a dark-colored transistor. In string 2, there's a dark-colored transistor. All six strings that we see, the four labeled strings, 1, 2, 3 and 4, but also, the two unlabeled strings, they all have one dark-colored transistor that's depicted here.

There will be others in a real design, for example, but that's why there are dots shown at the bottom of each string, to indicate that there are more flash transistors.

But these -- let's say these -- the six dark-colored transistors that are shown, they will all have one word line which will have some flavor of a pass voltage applied to it.

Now, when a pass voltage is applied to it, as I described earlier, there will be -- you know, there will be created an electric -- there will be a voltage between the gate of any flash transistor and its body, and that voltage that's -- you know, that voltage is going to induce an electric field in that flash

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transistor, and there will be Fowler-Nordheim tunnelings current, which I described to you as, you know, the current as being, you know, sub-constant A times, you know, the electric field squared times A to the minus, sub-constant B divided by the electric field, if I recall correctly.

So that electric -- I'm sorry, that Fowler-Nordheim tunneling will cause electrons to get trapped in the floating gate of the dark-colored cells. Even though we were not trying to program them, a small current will flow, an unintended current, which will cause electrons to be trapped.

And once they get trapped, that will change the threshold voltage of the dark-colored transistors, and that's going to be a disturbance because the threshold voltage of a transistor got unintentionally changed or disturbed, and because it got disturbed for transistors on which we apply the pass voltage, we call it a pass voltage disturbance.

So that's the pass voltage

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disturbance that is referred to in lines 39 to 41 of the '941 Patent.

Q Can pass voltage disturbance occur when you're reading a memory cell?

A So the -- you know, a pass voltage -- you know, when we're reading a memory cell, we would also apply a pass voltage to the memory cell, and the important thing is that the -- you know, that basically this patent explicitly talks about the programming time -- the programming of it because, for example, if you looked at columns -- let's see...

So if you look at basically, you know -- there's two portions of this patent, the '941 Patent, that describe that.

The first would be line -- column 1, lines like 24 to 41, you know, and I'll read from there the -- you know, it says -- it says, for example, however, program disturbance will become more significant when the number of layers increases, and that, you know, program disturbance will lead to a higher failure

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rate of programming a memory.

So this is clear. When a person of ordinary skill in the art reads this, a person of ordinary skill in the art understands that the focus of this patent is program disturbance.

In the next line, the patent continues to say: "In addition, pass voltage disturbance also occurs when using a memory with a plurality of layers."

Again, a person of ordinary skill in the art would realize that this is sort of like a -- an attendant defect when you're getting -- when you're trying to program and getting the program disturb.

Further on in columns 3, you know, it's very clear for a -- again, for a person of ordinary skill in the art, column 3, lines 4 to 8 talk about, you know -- and I'll read it first.

In a text -- sorry, in the text, when a word line has been programmed, it may mean a word line is used to perform a program operation.

Again, setting the stage and

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describing that this patent is about the programming and the programming operation. And then it defines the programming operation in saying that it may be an operation for programming a memory cell in the event of this.

Further again, you know, the next line, which is line 9 of column 3, says when an xth line of WLx is used to perform a program operation, you know, the controller drives Vprogram through WLx.

Again, a person of ordinary skill in the art reading this understands that this patent is teaching what happens during the programming operation.

Further again, if one -- if a person of ordinary skill in the art reads the figures from Figure 1 through Figure -- what is it, 10? No. 11 even.

From Figure 1 to Figure 11, every figure that's described in the patent has some word line that has the voltage reprogram applied to it.

Figure 11 does, as I can see, Figure 9, Figure 10, Figure 7 and 8, 5 and

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6, all of them show, you know, what -- you know -- well, in Figure 7 -- sorry, 5 shows WLx having a Vprogram on it. Figure 3 and 4 have that -- I'm just making sure, yes -- and Figure 1 and 2 have it.

So once again, when the person of ordinary skill in the art sees all the figures of the '941 Patent, they know quite clearly that the -- you know, that the programming -- that this patent is about the programming phase as well as when they look at the text I just described.

So they know it's about the programming -- you know, the programming operation, and the figures support that. Every one of the figures that I described supports it.

Q Yeah, so my question wasn't about the programming of a memory cell. My question is directed at when you're reading a memory cell.

Are you familiar, Dr. Khatri, with what it means to read a memory cell?

A Of course -- yes, I am.

Q Okay.

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And so my question was with respect to reading a memory cell -- and I'll just repeat the question so you have it clear -- can pass voltage disturb occur by reading a memory cell?

A And --

MR. LOWRY: Objection to form.

A Again, you know, the pass voltages are applied when we're reading a memory cell or programming a memory cell. And any time you apply a voltage to a flash transistor, it will cause some amount of disturb.

So that's something that, you know, that's inevitable.

And I'm trying to sort of say that the '941 Patent talks about the program disturb, which occurs when you program, and the pass voltage disturb that also occurs during the programming phase based on the evidence I just described to you in my last answer.

Q Let's go to your POR declaration, Dr. Khatri.

A Okay. Where would you like to

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point my attention to?

Q Let's go to paragraph 106.

Let me know when you're there.

A I'm there, but I would like to just read a little bit about the paragraph and its neighbors really quick before I'm ready to answer your question.

Okay. Let's see, I'll go back to every word, and I think I'm ready to answer your questions.

Q Yeah. So this is the section of your report starting at paragraph 106 and the following paragraphs where you render your opinions on the claim construction of the term "from bottom to top," correct?

A Yes.

Q Okay. And I'll direct you to paragraph 107, and could I have you read aloud the second sentence of that paragraph?

A The second -- wait, 107. The one that starts: "In my opinion," yeah?

Q Yes.

A Okay.

That says: "In my opinion,

based on the intrinsic evidence, as well as my knowledge and experience, a POSITA would understand the ordinary meaning of 'bottom' and 'top' controls." And then there's a dash: "Bottom means lowest point and top means highest point relative to the substrate."

Q Is that the proposed construction that you give for the claim term "from bottom to top"?

A I think, you know, the term "from bottom to top," you know, for me -- I think I've said, you know, in my declaration -- and, in fact, if you look at just the next paragraph, it says, you know -- the beginning of paragraph 108, it says: "In my view, the term 'from bottom to top' has no special meaning in" semiconductor -- "in the semiconductor manufacturing context or in the context of the '941 Patent."

Further, the '941 Patent and its prosecution history has no special definition for that phrase "from bottom to top" and that there is no prosecution

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history disclaimer that would impact or -- you know, impact the meaning of "from bottom to top."

So therefore, in my opinion, the '941 Patent, which assigns word lines arranged from bottom to top, use that phrase in its plain and ordinary sense simply referring to where lines were arranged vertically from the lowest, or the bottom, to the highest, or the top, as the intrinsic evidence confirms.

And I've provided much intrinsic as well as extrinsic evidence to support this.

Q Sorry, are you giving a different construction in paragraph 108 than you are in paragraph 107?

A No. I mean, again, if you look at paragraph 109 further, right, it says: "In my opinion, the terms of the '941 Patent claims do not require further construction and can be afforded their plain and ordinary meanings for the purpose of analysis of the prior art that I'm conducting."

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So it says in that many words that, you know, I'm using the plain and ordinary meaning for the terms for my analysis.

And that same comment was made in paragraph 108 where I'm saying that, you know, the -- the -- that, you know, if I read this last fragment of paragraph 108, I say, In my opinion, the '941 Patent claims which recite -- recite word lines arranged from bottom to top use that phrase in its plain and ordinary sense.

So I said in paragraphs 108 and 109 that, you know, I'm using the words "from bottom to top" or "bottom to top" in their plain and ordinary sense.

Q In paragraph 107, in the second sentence, you refer to a substrate.

Do you see that?

A Yes. I see that.

Q And that's part of your opinion in that paragraph, that "bottom" means lowest point and "top" means highest point relative to the substrate, correct?

A So as I said, right, a person of

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ordinary skill in the art -- I think this came up before as well -- a person of ordinary skill in the art knows that, you know, in an integrated circuit or in a semiconductor circuit or in a semiconductor memory, there is a substrate, and everything is referred to -- relative to that substrate.

So basically, you know, that's why it says, you know, "bottom to top" means highest point relative to substrate.

This is something that a person of ordinary skill in the art readily understands.

THE WITNESS: Incidentally, I think -- well, let's see, we've been going around 40 minutes, and I'm sort of getting a little tired. So I'd like to request maybe a 5-minute break.

MR. JENSEN: Sure.

THE WITNESS: Okay. Thank you.

(Whereupon, a brief recess was taken from 2:43 p.m. to 2:50 p.m.)

BY MR. JENSEN:

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Q All right. Welcome back, Dr. Khatri.

A Thank you.

Q Let me point you to paragraph 100 of your declaration.

A Let's see, 100.

Okay. I'm there.

Q And in this section, you refer to Dr. Liu or petitioner's construction of the term "bottom to top."

Do you see that?

A I'll just really quickly look at this. Just one second, please.

Okay. So this is part of the claim construction section, and it talks more about it in the paragraphs you're mentioning. So let me look really quick at this...

All right. So this one -- this is for like the summary section. I get it.

Okay. May I -- I'm ready to answer your questions, assuming it's just about this local region of the paragraphs.

Q Yeah. So what was petitioner's proposed construction of the phrase "from

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bottom to top"?

A So the petitioner said -- I mean, I'm trying to remember now exactly. So I'll have to start looking in the -- in Dr. Liu's declaration and the petition, but they said something about -- and I want to be more accurate, so I'll just sort of make sure I cite that correctly.

So let me see --

Q Well, I can shortcut this. I'll represent to you, Dr. Khatri, that what you stated in paragraph 100, the phrase "from source to drain," is the interpretation that petitioner used in --

A Sorry? I didn't hear that.

May I ask you to repeat the question, please?

Q Yeah. So I'll represent to you, Dr. Khatri, in the interest of time that the interpretation that petitioner used was -- for the phrase "from bottom to top" was "from source to drain."

A Okay. And you're sort of representing that to me?

Q Yeah. And you say it in

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paragraph 100 as well, but just so we don't have to go look at it in five places.

A Okay.

Q My question is this: Did you render any opinions in your report of whether the challenged claims are invalid using petitioner's construction of the phrase "from bottom to top"?

MR. LOWRY: Object to form.

A You know, I have, you know, provided evidence that, you know, if you used -- if you -- if you interpreted it from bottom to top as from source to drain, that it would simply be an absurd proposition.

So any construction -- any conclusions relating from that would be necessarily absurd.

Let me tell you some of the arguments that I've made in that regard.

So further from bottom to top, you know, I have shown -- let me run through, for example, the summary of the arguments I make for the term "bottom to top."

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Q Where in your report -- can you point me to where your report you render any opinions under petition's construction from bottom to top?

A That's what I'm trying to do, and I would like you to --

Q All right. Well, yeah, I just didn't -- but where in your report are you looking?

MR. LOWRY: Object to form.

A So I was beginning to start looking but I didn't have the -- you know, I was sort of scrolling down --

Q Oh, you haven't found it yet.

A Yeah, I was in the middle of scrolling and talking.

So I'd like the courtesy of some -- you know, letting me finish, please.

Q Yeah, yeah, just go ahead and point me to -- go ahead and find it, and then you can just point me to where you render the opinion under petitioner's instruction.

A Yeah.

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So I'm saying that the interpretation of bottom to top being from source to drain would lead to absurd conclusions based on intrinsic evidence. And, for example, if you look at -- let's see -- paragraph 118, which refers to Exhibit 2011 -- no, actually, let me scratch that.

Let me go to paragraph 119 referring to Exhibit 2012, which is cited in the '941 Patent, which shows a NAND string in a U shape. In other words, now there's no source to drain -- you know, now the interpretation of from bottom to top if treated as from source to drain, it simply becomes absurd because it follows a U-shaped trajectory, and U-shaped trajectory has no signal direction.

So this is basically how the interpretation of from bottom to top as from source to drain would be observed. This is evidence number 1.

Q Yeah, let me -- this is not my question.

A I would like to finish this.

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Q Yeah, you're not answering my question, so I want to reask my question --

(Simultaneous crosstalk.)

A I'm saying --

(Simultaneous crosstalk.)

Q Because --

A -- absurd, so any conclusions from an absurd premise are not valid. That's kind of what I'm trying to say.

So if a premise is absurd, there is no reason for me to sort of follow the -- you know, follow the arguments that are made from a false or absurd premise.

There are other citations -- or there are other -- you know, again, intrinsic documents that I follow -- that I sort of cite to, and they are Exhibit 2015 on paragraph 133, which, again, now show the -- from bottom to top as an inverted proposition because now the from bottom to top, according to petitioner's read, would now become from bottom -- from top to bottom, and so it would sort of flip the direction because the source is on the top here and the drain is at the bottom.

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This is on page 73.

Similarly, let's see...

Q Let me just -- I'm not asking -- this is all in the claim construction section of your declaration, and I'm not asking about which claim construction is right or why it is right or wrong.

My -- I'm asking a totally different question. So that's why I wanted to pause you, right? I'm not -- I can read your report, and I understand you have a different opinion on what the correct claim construction is of the term "bottom to top."

My question is different, which is: In your report when you analyze the Dong reference in grounds 1 and 2, for example, do you analyze the Dong reference using petitioner's proposed construction?

Putting aside that you think that construction is wrong, I understand you think it is wrong.

My question is: Is there anywhere in your report that you explain why the Dong reference does not meet

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petitioner's construction?

MR. LOWRY: Object to form.

A So, again, like I said, the petitioner's construction is facially absurd. So if -- you know, if they make a facially absurd statement and decide -- and make a whole sort of theory based on that facially absurd assertion, that theory or that line of argument that is based on the facially absurd statement is basically absurd to begin with, and there was therefore no need for me to drain dollars in that particular exercise.

Q Okay. Thank you.

A And, you know, and the Board has agreed with that, and that's stated in my deposition as well.

And I have multiple, you know, intrinsic evidence to show that -- you know, that the construction that's used by the petitioner is an absurd -- is an absurd construction, including that, you know -- let's see, what was the number that -- including Exhibit 2016, including Exhibit 2012, and exhibit -- and these are

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sort of discussed in paragraphs 137 and 138 as well as in paragraph 133, which is Exhibit 2015.

So there are many intrinsic sort of -- intrinsic evidence which suggests that the petitioner's construction is absurd.

In fact, it would write -- it would rewrite the claims. To use petitioner's construction would basically rewrite the claims of the patent.

Q And for that reason, you didn't compare petitioner's construction to the Dong reference, correct?

MR. LOWRY: Object to form.

A So it's a facially absurd construction, and therefore it did not warrant, you know -- it did not warrant sort of -- I mean, it's basically saying from bottom to top is from source to drain but as -- intrinsic evidence states otherwise.

Q You don't dispute, do you, Dr. Khatri, that a memory string has a source end and a drain end?

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MR. LOWRY: Object to form.

A You know, as -- can you give me an example of this?

Q I mean, we can look at examples in your report if we need to, but let me just ask the basic question.

Would a person of ordinary skill in the art understand that a memory string has a drain end?

A So, for example, if a person of ordinary skill in the art -- I'm going to refer back to my part.

If a person of ordinary skill in the art, you know, read the -- saw the figure and read the patent relating to paragraph 133 that's shown on Figure 73, they would see a source end and a drain end, but they will see the source end on top in this case and the drain end at the bottom.

This is completely the opposite of what the petitioner's construction is.

Similarly, if a person of ordinary skill in the art looked at the figure that I -- and the intrinsic evidence

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patent -- I think, hold on, this is also intrinsic -- let me double-check this...

Cited by the '941 Patent, so yes, if they looked at the paragraph 137 and the figure relating to that on page 76, they would see that the source end and the drain end are both at the same level in this case because it's a U-shaped channel.

So again, this would break the -- you know, this would break the petitioner's construction.

And then, finally, if they looked at Exhibit 2016, you know, also intrinsic evidence cited on the '941 Patent, this is on -- under paragraph 138 and on page 77, they again would see that the source and the drain are at the same level and that it's a U-shaped channel.

So there's so much intrinsic evidence that basically just says that, you know, yes, there's a source end and a drain end, but the way the source end and the drain end are oriented can be quite different and the -- therefore the construction that the petitioner posits is

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an incorrect construction.

Q Yeah. So we'll strike that as nonresponsive.

Let's go to paragraph --

MR. LOWRY: Object to that striking.

(Simultaneous crosstalk.)

BY MR. JENSEN:

Q -- of your report.

Of your POR declaration, paragraph 59?

A I'm sorry, I did not, you know, catch that. Can you repeat this, please?

Q Yeah. Let's go to paragraph 59 of your POR declaration?

A 59 of POR. Okay, let me do that. Hold on.

59. And I'm going to take a few minutes to read a little bit above and below that. Give me a second, please.

Okay. I've looked at that, and I'm ready to answer any questions relating to this.

Q Yeah. Can you read the second and third sentences aloud in paragraph 59?

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A Second and third. Okay. I see.

The second --

Q Why don't you read the first one. Read the first three sentences.

A Give me one sec.

So the first sentence through the third sentence is stating as follows: "In a NAND flash memory, several floating gate transistors are connected in a series configuration, as shown in the figure below (from Exhibit 1009, page 18.)"

Let's see, sorry, I got lost.

"The source end of the string is depicted at one end of the figure. The drain end of the string is depicted at the other end of the figure, and is connected to a bit line BL."

So this figure is a depiction. It's the figure that's shown on page 30 right below this paragraph. It's a depiction of a circuit schematic using circuit symbols and it's not got any physicality to it.

Q What do you mean when you say, "source end of the string"?

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A So if you look at -- you know, if you look at the figure that is -- that it's -- that paragraph 59 is talking about, which is on page 30, if I look at that figure, it's -- yeah, the figure that's on the right of your screen, if you look at the -- if you look at this figure, it says on one end in the depiction of the circuit diagram, at one end, it uses -- it shows the word "source."

So that would be what a person of ordinary skill in the art would consider the source end of the string.

And then on the other end of the string, there is a label called "bit line" and in parentheses "BL." So that would be the bit line end of the string.

But the bit line end is the opposite of the source end, so that's also called the drain end of the string.

Q Would a person of ordinary skill in the art understand that the memory structures in the '941 Patent had a source end and drain end of the memory string?

MR. LOWRY: Object to form.

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A A person of ordinary skill in the art looking at the '941 Patent, as we've said, you know, they would understand that they were -- in the '941 Patent, there were word lines arranged from top to -- I'm sorry, from I believe -- I want to use the right language.

So if I look at, you know, column 2, lines let's say 63 to column 3, lines 3, they would understand that there were word lines that were, you know, oriented from bottom to top and also that there were first portions and second portions wherein the second portion might be formed above the first portion.

So that's something that they would readily understand.

Q Yeah, and that didn't answer my question.

My question is: Would a person of ordinary skill in the art understand that the memory strings in the '941 Patent had a source end and a drain end?

MR. LOWRY: Object to form.

A Let me just look for the -- let

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me look for that language in the patent really quick, the source and drain language.

So I don't see the language source as in the source terminal of a flash transistor, and I'm going to look for drain right now.

And I don't see drain as well.

So the fact is that there is no occurrence of the word "drain" in the '941 Patent, and there's no occurrence of the word "source" in the context of the counterpart of the drain of a flash transistor, which makes it even more absurd to create a construction which says from top to bottom -- sorry, from bottom to top means from source to drain because source and drain aren't even referred to in the '941 Patent.

So this is basically wholesale rewriting of the '941 Patent.

Q Yeah. So that's not my question.

I agree that the '941 Patent doesn't use the word "source" or "drain,"

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and you testified earlier that it doesn't use the word "substrate" either, but you said a person of ordinary skill in the art would understand that there's a substrate.

So my question is --

A Yeah.

Q -- would a person of ordinary skill in the art understand that the memory strings in the '941 Patent had a source end and a drain end?

MR. LOWRY: Same objection.

A Can you repeat the question?

MR. JENSEN: Could the reporter read that back, please.

(The requested portion was read back by the Court Reporter.)

MR. LOWRY: Same objection.

A So -- excuse me. So I think, you know, this question has sort of a prior question as in does the -- you know, does the '941 Patent disclose, you know, memory strings.

And I think we've gone over that question before, so we -- you know, we established that, you know, the '941 Patent

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does not explicitly describe source -- you know -- sorry -- memory strings.

So given that the case -- you know, given that it's already the case that the '941 Patent does not disclose, you know, memory strings, somehow it becomes more terse to talk about whether it discloses memory -- whether it discloses a source end of a string or a drain end of a string.

So therefore in some sense, I see this question as sort of moot because of the previous question that was asked relating to memory strings about the '941 Patent.

Q Is it your testimony, Dr. Khatri, that a person of ordinary skill in the art would understand that the figures and disclosure in the '941 Patent do not convey a memory string?

MR. LOWRY: Object to form.

A I mean, I didn't say that. All I'm saying is that this question was asked before and that, you know, the -- you know, as I see this patent, there is no -- you

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know, there's no explicit sort of statement in the patent that says memory string, or string even for that matter, which doesn't mean that it doesn't talk about a memory string because it talks about memories, which -- you know, which do have strings.

Q Yeah. So I'll repeat my question, and if, you know, you're hung up on the word "string," we can use whatever term you want to use for what is described in Figure 1 of the '941 Patent.

Does the memory structure in the '941 Patent include a source and a drain end?

MR. LOWRY: Object to form.

A Are you referring to a specific figure?

Q You could refer to any of the figures.

A So maybe just to make it more sort of specific, let's refer to a figure.

Would you tell me which figure would you like to ask this question about?

Q We can look at Figure 1.

Would a person of ordinary skill

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in the art understand that the Figure 1 of the '941 Patent includes a source?

A I think that's an ill-formed question as posed.

Q You can't say one way or the other, Dr. Khatri, whether the memory structure in Figure 1 of the '941 Patent has a source?

MR. LOWRY: Object to form.

A The question does not make sense electrically.

A figure does not have a source.

Q Would a person of ordinary skill in the art understand that the memory structure depicted in Figure 1 has a source?

MR. LOWRY: Object to form.

A I don't know how to say this, but -- you know, say this politely, but that is an electrically malformed statement.

A memory does not have a source. A string has a source. So a memory may have multiple sources.

It makes no sense to say a

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memory has a source is what I'm trying to say.

It's electrically ill-formed to say it like that.

Q Does the collection of word lines shown in Figure 1 have a source end?

MR. LOWRY: Object to form.

A Word lines connect to the gates of flash transistors and have nothing to do with source ends or drain ends.

I think these questions are -- you know, I mean, they're hard to answer because they don't make electrical sense.

Q Do the memory cells connected to the word lines in Figure 1 of the '941 Patent have a drain end and a source end?

MR. LOWRY: Object to form.

A Can you repeat that question slower, please?

Q Do the memory cells connected to the word lines shown in Figure 1 have a source end and a drain end?

MR. LOWRY: Same objection.

A So if I look at Figure 1 and the specification for Figure 1, which I've read

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to you, you know, at some -- you know, once I think, which goes from -- excuse me, column 2, lines like 63 to column 2 -- column 3, lines 25, this specification just talks about the word lines and their relative orientation, and -- you know, and also the portions, the first portion and the second portion, and their relative orientation and the labelings of all of these entities.

So basically, this describes the relative orientation of word lines and the first portion and second -- of the portions of the memory.

That's the purpose of Figure 1.

Now, a person of ordinary skill in the art not -- you know, seeing this figure and knowing that this entire patent, the '941 Patent, is about three-dimensional memory, so a person of ordinary skill in the art knowing that, would certainly know that -- you know, that there were -- you know, that, for example, that there would be, you know, NAND memory strings in -- as part of this memory. There would be a

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memory array because, for example -- let's see...

Because, you know, the Figure 1 -- I'm sorry, the label 100 of Figure 1 is referred to as the memory 100.

So a person of ordinary skill in the art would know that this is basically a memory. And if it's a memory, they would -- and it's also thought to be a three-dimensional NAND flash memory.

So if they knew that, they would know that there would be memory strings associated with it, arrays in a 3D manner, all of these things is something, and that there would be a substrate, and these would be things that a person of ordinary skill in the art would understand.

Q Would they also understand that there would be a source and a drain associated with the memory strings?

MR. LOWRY: Object to form.

A You know, a person of ordinary skill in the art would understand that a memory string has a -- you know, has a ground end, you know, which is typically

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called a source end, and a bit line end, which is also called the drain end of the memory string.

Now, how they're oriented, whether they're oriented from -- you know, the source and drain, how they're oriented is not something that -- you know, for all possible orientations, the teachings of this patent will apply.

Q Let's turn to Exhibit 1005, which is the Dong reference.

A Let me open that.

Okay. At this point, what may I close? Because I have a lot of open windows -- I mean, open --

Q You can close everything except the Dong reference.

A Okay. Let me do that. Give me a second.

Okay. I have the Dong reference open.

THE WITNESS: I just wanted to point out, at this point, I think -- I'm just looking, and we've been going for about 30 minutes. And I know

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that's relatively short, you know, but I -- it would be good to take a break perhaps after the Dong reference.

I want to sort of stretch the sessions a little bit so that we finish earlier in consideration of everyone else, but at the same time, I also need some breaks at this point.

MR. JENSEN: Well, we can take a -- if you want to take a short break now, that's fine.

THE WITNESS: Okay. We can do that real quick. Maybe five minutes.

Thank you.

(Whereupon, a brief recess was taken from 3:18 p.m. to 3:26 p.m.)

BY MR. JENSEN:

Q Welcome back, Dr. Khatri.

A Thank you.

Q Let's turn to the Dong reference, which is Exhibit 1005.

A Yes, I have it open.

Q Okay. And do you recognize this as the primary reference for the petitioner's invalidity challenge?

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A Correct, it is.

Q Okay. And let me direct your attention to Figure 5g of the Dong reference.

A Okay. I see it.

Q Is that one of the figures that petitioner uses as part of the invalidity analysis?

A Yes. The petitioner uses two figures in the invalidity. One of them is 5g and the other figure is 5a.

Q Thank you.

What did the acronyms "WL" stand for in Figure 5g?

A So let me -- you know, I mean, I can -- I have done my guess, but I'll just double-check it to see if there's intrinsic support for what I'm trying to say.

I think they're word lines, but we'll just confirm it by looking at the -- the specification. Give me one second, please.

So, you know, even right in the -- right up in the abstract, there's a discussion of isolation word line and, you

know, more than once. It's referred to at least four times.

And, you know, so basically, it's suggesting that there are the -- this is notion of word lines in this patent.

And further, if you look at Figure 4, which is basically the physical -- it's basically a cross-section of the -- you know, of the NAND memory that's the teaching of Dong, you can see in Figure 4 that it talks about a dotted line in the bottom with a little arrow. And to the left of the arrow, it says: "Source side of isolation word line." And to the right, it says: "Drain side of the isolation word line."

And again, by looking at this, we can see that the isolation word line is WL2, and it's labeled with its voltage as Viso.

So we know that the word line now refers to -- the WL2 label refers to a word line. That's the isolation word line.

And we can also see the -- you know, the source side and then the drain

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side of that isolation word line.

And then if I just want to -- just to make sure that our -- you know, that our analysis is not incorrect, if I look at the summary of the invention, it talks about many occurrences of the word "word line" in there as well.

So, you know -- and then finally, I guess if you -- you know, like what seals the conclusion in some sense is if you look at paragraph 37 maybe where it talks about -- towards the bottom of that paragraph on page 2, it talks about word line WL3 and word line WL2 and word line WL1, et cetera.

So now we know from that that WL stands for word line.

Q So turning back to Figure 5g, how many word lines are shown in Dong Figure 5g?

A Let's see. So in Figure 5g, if I look at the SGS side of Figure 5g -- and Figure 5g is simply -- sort of like a tabular, if you will, you know, like a diagram which illustrates the -- a list of

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word lines and what voltage that they're applied to.

So they're just -- the purpose of Figure 5g is just to say which word line gets which voltage.

So the word lines are represented in the -- on the right side of the Figure 5g, and there are corresponding voltages on the left.

So if I look at the word lines and their labels, you know, we see word lines WL0 through WLn-8, and then there's WLn-7 and n-6, n-5. And then it goes all the way up to n+1 and then n+2 through WLi.

So in other words, the number of word lines in this -- in this -- you know, in this sort of tabular diagram of word line versus their voltage is i+1 in total.

Q Is Figure 5g limited to any particular number of word lines?

A Let me look at the specification for Figure 5g to confirm or reject that -- or to answer that question accurately.

So I'm going to sort of scan -- sort of scroll -- hold on a second. I will

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scroll down the patent to look for Figure 5g. Give me one second, please.

They're kind of not arranged in a completely -- oh, there we go -- and now I find it. 5f, g, g, here we go.

Let's see. So the language associated in Figure 5g says Figure 5g depicts another -- I'm sorry, I'm reading paragraph 59.

It says it "depicts another revised erased area self-boosting" -- also called an REASB -- "mode."

This defers from 5f in that the drain-side word line, which is WLn+1 -- which one is that -- okay. The drain-side word line receives a voltage Vpass-high and the VLn-3 receives Viso in one -- I'm sorry. I'm sorry, I'm reading the wrong one.

"The drain-side word line adjacent to the selected word line (WLn) receives Vpass-high," so Vpass.

So essentially, the description of Figure 5g is basically expressed in terms of its difference with respect to

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Figure 5f, which is described in the prior paragraph.

I don't -- I mean, actually, I don't think -- I don't know if I answered your question because I got sort of lost when reading this, but did that answer your question or did I -- or maybe you can re-ask your question, if you don't mind.

MR. JENSEN: Yeah, could you reporter -- I think I lost the question as well. Could the reporter read the question back.

(The requested portion was read back by the Court Reporter.)

THE WITNESS: I see. Thank you.

A So Figure 5g in its brief description does not talk about any limit on the number of word lines, and let me do one more.

THE COURT REPORTER: I think he's frozen.

MR. JENSEN: Yeah, he's frozen on my end as well.

MR. LOWRY: Let me -- let's go off the record and I'll give him a

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call.

MR. JENSEN: Okay.

(Whereupon, a brief recess was taken from 3:35 p.m. to 3:37 p.m.)

BY MR. JENSEN:

Q Let me direct your attention, Dr. Khatri, to a figure that you had mentioned in the Dong reference, which is Figure 4.

A Let me see. Hold on. I'm going to -- let me do one thing. I'm going to go back -- so, I'm sorry, but I was in the middle of talking about Figure 5 and -- sorry, 5f and 5g, correct?

I'm sort of forgetting where we were in the last -- when my Internet crashed.

Q Yeah, I think we were talking about Figure 5f and 5g?

A Yeah. So if I look at Figure 5f, which Figure 5g is based on, it has the same maximum number of word lines, which is i+1 based on the figures themselves.

And then really quickly, based

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on the specification, I'm going to look at the description for Figure 5f. And I'm trying to find it again.

There it is.

So that's described in paragraph 58, and it doesn't say anything about the, you know, value of i. So i could be -- the i is not specified to have a specific value.

And I think that was your question.

Q Thank you.

Turning to Figure 4 in Dong -- let me know when you're ready and have that in front of you.

A Okay. I'll go there in a minute.

Yes, I'm at Figure 4.

Q How many word lines are shown in Figure 4?

A So if I look at Figure 4, you know, I -- and I look for labels that are like WL, you can see that there's WL0 near SGS, and then there's WL1, and going all the way to WL7.

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So there's 0 through 7, which is 7 plus 1, or 8 WLs in Figure 4.

Q In Figure 5g, do you see a voltage labeled Vpass high?

A I do see Vpass high in Figure 5g, yes.

Q Do you see a voltage labeled Vpass medium?

A Figure 5g also has a Vpass medium, yes.

Q And there's also a voltage in Figure 5 called Vpass low?

A Yes, Figure 5g has a voltage called Vpass low in the depiction of the figure which is just a -- you know, like an association of word lines and their -- and their voltages assigned to them with no physicality to it.

Q Does Dong Figure 4 have any voltages labeled Vpass high, Vpass medium or Vpass low?

A Dong Figure 4 actually matches, you know, voltage for voltage with Figure 5c.

And in my declaration, I

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describe, you know, how that occurs.

In other words, Dong Figure 5 -- 4 is the physical orientation of the memory that is in the Dong disclosure, which is two dimensional as a person of ordinary skill in the art would see based on Figure 4, because Figure 4 shows the substrate, shows the word lines, shows the gates and the floating gates and also the -- you know, the channels below that.

So Figure 4 in Dong is the key -- which is a two-dimensional flash memory, is the key physical structure that's shown. And all the other figures, Figure 5a, b, c, et cetera, up to g, are the voltages that you apply to -- you know, to the physicality of Figure 4 based on the corresponding figures.

So there are a large number of figures, 5a through 5H, I think, and they all correspond to voltages that one would apply to an exemplary physical structure, which is Figure 4.

And there's much evidence that all of this -- you know, this teaching is

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about 2D NAND flash.

And I'm going to open my declaration really quick. Just one second.

Please give me a minute. I'm kind of looking for this region.

So, for example, if I look at my declaration on page 92, it shows the 141 association of the voltages shown in Figure 4, which is the physical structure of Dong, with Figure 5c, which is just a tabular representation of what word line gets driven with what voltage.

So that's kind of a one-to-one match.

And then also further down, you know, I describe how all the figures which have a label 5, like 5a through 5h, are all related, and this is in paragraph 184, where it shows that, you know -- where it describes that Figures 5 to 5a -- 5a to h, they all describe self-boosting modes, and there's citations that I have in paragraph 184.

And it also then, at the later half of paragraph 184, talks about Figure 4

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describing, you know, substrate 490, word line 412, et cetera, to talk about -- to describe the operation of the REASB of Figure 5g.

So 5g also is now associated with Figure 4.

You know, so this is basically connecting all the five figures with 5a through 5h to Figure 4 in the Dong disclosure.

And there's also in some sense in the Dong disclosure, if you look at paragraph -- I forget which one this is, but paragraph 90 something. I'm just going to take a second to find it.

Yeah, if you look at figure -- sorry, paragraph 94, it talks about -- if you look -- if I'm reading paragraph 94, it tells: "Memory storage elements are erased in one embodiment by raising the P-well to an erase voltage."

And then it again talks about electrons being transferred from the floating gate to the P-well later in this paragraph.

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So person of ordinary skill in the art reading this knows that a P-well is a structure in two-dimensional memory, and they would further know that, you know, that Dong is related to or teaching two-dimensional memory.

Also in paragraph 111 of Dong, there's a disclosure of a P-well where it talks about -- and also in 112 -- both of these talk about, you know, raising the P-well to a raised voltage, for example.

You know, and so in some sense, there's ample evidence in this disclosure that Dong is a 2D memory whose physicality matches Figure 4, which you're asking me about right now.

Q Yeah, so we'll strike that as nonresponsive.

I'll repeat my question, which is, do the voltages Vpass high, Vpass medium or Vpass low appear in Dong Figure 4?

A So, you know, I think --

MR. LOWRY: Object to form.

A -- my answer was responsive to

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your question because I said Figure 4 is the physical structure, and Figure 4 is the structure that's used to -- where the voltages of all the different Figure 5 variants, 5a through 5h, are applied.

So Figure 4 corresponds to just one of them, 5c, but it also can correspond to all the others, but it's -- you know, they didn't have like, you know, eight copies of Figure 4. But they're just trying to show that Figure 4 is this physical structure to which all the voltages are Figure 5a through 5h, you know, are applied.

And I was just trying to present you evidence that -- further evidence inside the -- you know, inside the Dong reference that supports this argument.

Q Yeah, can you show me in Dong Figure 4, Dr. Khatri, where is Vpass high?

A Again, like I said, Figure 4 corresponds to, as you saw -- let me -- let's see.

As I just told you from my declaration -- now let me look for it --

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here we go.

On page 92 below paragraph 177, Figure 4, the voltages that are applied in Figure 4 -- the Figure 4 shows the physicality of the memory structure.

The actual voltages that are shown applied in Figure 4 match what the four voltages shown in Figure 5c, one for one, as you can see in -- on page 92 below paragraph 177.

And once again, they -- it would be sort of -- you know, the patent doesn't show eight copies of Figure 4, one -- you know, one for Figure 5a, one for Figure 5b, one for Figure 5c, et cetera, through Figure 5f, or whatever -- of 5h. It shows one copy of Figure 5 -- 4 showing the physicality of the memory structure and laying the ground there.

And then there's other evidence, like the P-well evidence I discussed from paragraph 90 and paragraphs 111 and 112, which further support the idea that this is 2D memory.

Q Yeah, and that's not my

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question.

My question is simply, where in Figure 4 is the Vpass high -- Vpass high voltage?

MR. LOWRY: Object to form.

BY MR. JENSEN:

Q What word line is it connected to?

A Yeah. So again, I mean, you know, since the question is repeating and I've answered it, I'll repeat the answer that I had.

Figure 4 is the physical structure of the memory, which is a 2D memory. That's the first comment.

Figure 5 are multiple variations of using this, you know, modified EASB, or erased area self-boost, you know, teaching.

So Figure 5a through Figure 5h all have slightly different voltages that you would apply to the physical memory of 5 -- of Figure 4.

Now, one of these physical -- sorry, one of these Figure 5s -- Figure 5 variants, which is Figure 5c, happens to

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actually match one for one in terms of word lines and voltages to the figure of -- to the physical figure of Figure 4.

But it would be tedious and repetitive to make multiple copies of Figure 4 for every Figure 5a, 5b, 5c, et cetera.

So only one of them is described, which is 5c, which matches with the Figure 4. And the others, a person of ordinary skill in the art would readily understand would be, you know, other voltages that you would apply to the case of Figure 4.

Q What is the voltage that's applied to WL0 in Figure 4?

MR. LOWRY: Object to form.

A Let me see. Let's go back to...

So WL -- I'm referring to the page 92, paragraph 177. There's the little figure I have in my declaration below paragraph 177, which shows Figure 4, and on its side, it shows Figure 5c.

And in this Figure 4, let's see...

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If I chose -- let me just verify.

Yes, if I choose n=5, which is described -- which is mentioned in paragraph 179, if I choose n=5, then the voltages that are shown on Figure 4 match exactly with the voltages that are shown on Figure 5c.

So for that choice of n, Figure 4 and Figure 5c, you know, match exactly.

Now, in a real-life memory, Figure 4 might have more word lines, you know, that a person of ordinary skill in the art would readily understand, but Figure 4 is showing eight word lines. And WL0 is connected to Vpass, and according to Figure 5c on the left on page 92, WL0 is also connected to Vpass.

And the word lines connected to Vpass continue through WLn-4, but recall that paragraph 179 says n=5.

So that would be WL0 through WL5-4, which would be WL1.

So Vpass is driven to WL0 and

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WL1, as you can see in Figure 4 on the right of page 92.

Then on WLn-2, which would be WL2, we have Viso. Again, Figure 4 shows the same Viso on WL2.

And then WLn-2 with n=5, which would be WL3, has connected to it Vlow, and you can see WL3 is connected to Vlow in Figure 4.

Similarly then, WLn-1, which would be WL5-1, that's WL4, has a Vpass on it based on Figure 5c. And Figure 4 also shows that WL4 has a Vpass connected to it.

WLn, which would in our case be WL5, has Vprogram connected to it. So you can see WL5 has Vprogram connected to it in Figure 4.

And finally, Vpass is connected to WLn+1, which would be WL6 through WLi, which would be WL7 in our case if we chose i=7. And that's described -- I mean, the choice of i=7 is mentioned in paragraph 180.

So that means WL6 and WL7 should be connected to Vpass according to

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Figure 5c, which matches Figure 4.

So there's this one-for-one correspondence because -- between the voltage descriptions of Figure 5c and the physical memory of Figure 4.

And this could be for -- you know, there could be a different Figure 4 that a person of ordinary skill in the art would readily contemplate which would match with each of the Figure 5a, b, c, d, et cetera, up to 5h.

Q Let me try to ask the question another way because I still don't think I got an answer.

Does Figure 5c in Dong contain a Vpass high, Vpass medium or a Vpass low voltage?

MR. LOWRY: Object to form.

A So once again, you know, figure -- okay. Let's try it this other way.

Q It's a yes-or-no question, Dr. Khatri.

Is there --

(Simultaneous crosstalk.)

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A I'm trying to give you a clear answer, and I've already given you this answer. I'm trying it a different way because I'm trying to express it in a way that -- you know, that's more clear.

Q Yeah, what would be clear is to say yes or no. I can't tell if you're answering yes or no to the question.

So I think I'll just ask it again --

MR. LOWRY: Object to form.

BY MR. JENSEN:

Q -- because I want to give you every opportunity to provide a simple yes-or-no answer, which I'm sure the Board would appreciate and would order, frankly, if they were on this call.

MR. LOWRY: Object to form.

BY MR. JENSEN:

Q Is there a Vpass high, Vpass medium or a Vpass low label that appears in either of Dong Figures 4 or 5c?

MR. LOWRY: Object to form.

A In Figure 5a through 5h, there are multiple variations of voltages that

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are applied to the word lines of the physical memory that's -- that's shown as an example in Figure 4.

There are multiple voltages in Figure 5a through 5h, and they have different voltages.

Figure 4 is a rendition of the physical memory, and it has voltages assigned to it which match, as I just described to you, the voltages shown in 5c.

As I also said, it would be repetitive to just draw the physical structure of Figure 4 again and again for each of the voltage assignments of Figure 5a through 5h, and that's not done.

But a person of ordinary skill in the art would readily understand that the voltages of Figure 5a through 5h could be applied to Figure 4, and that's not something that they would find difficult to do.

Q Yeah, that's nonresponsive. We'll move to strike that and reserve our rights to compel an answer to that very, very, very basic question that's now been

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asked several times.

But in the interest of time, we'll move on here.

Let me take you, Dr. Khatri, to the Shirai reference --

A Okay.

Q -- which I believe is Exhibit 1018.

A May I close the Dong reference at this point?

Q If you'd like.

A Okay.

And you said you'd like me to open the Shirai reference. So what's the number for that?

Q That's Exhibit 1018.

A 18, okay. There we go.

I am there.

Q And let's go to Figure 2.

A Okay. I'm seeing Figure 2 in front of me.

Q And what is shown in Figure 2 of Shirai?

A So to -- you know, to accurately describe what's shown in Figure 2 of

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Shirai, I'm going to go to the specification of that figure.

Now, when I go scroll to the specification, I won't have the figure in front of me, so I might have to sort of bounce back and forth. But let's see, Figure 2 as described in Shirai...

Here we go. It's on page 2, and it starts -- well, it just starts -- it's a brief description on paragraph 27. It says it's a "schematic cross-sectional view of the semiconductor device of the first embodiment."

So this is a cross-sectional view. It's a physical view of the -- you know, of the semiconductor device.

Now, I'm looking for a more detailed description of Figure 2, and if you would like me not to do that, just please let me know. But I'm trying to answer thoroughly.

Q Yes. Does Figure 2 of Shirai show a 3D memory structure?

MR. LOWRY: Object to form.

A So, you know, I'm going to sort

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of read the description of Figure 2 on paragraph 30. It says: "The stacked body 100 includes a first stacked portion 100a, connection portion 45, and a second stacked portion 100b." The first stacked portion is provided on the substrate 10, and the connection portion is on top of the first stacked portion.

Let's see. The second stacked portion is provided on the connection portion.

So there's a first stacked portion on the substrate, which is 10, and that portion is 100.

Then there's a connection portion and then there's a -- which is 45, and then there's a second stacked portion 100b that's provided on top of the connection portion 45.

It also says that each of the stacked portions 100a and 100b may have any number of stacked layers.

You know, and then it says the thickness of portion 45 in the Z-direction is greater than the thickness of one layer

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of insulator.

So now, this is basically the description of the -- you know, of two stacks, you know, of memory, you know, in this semiconductor device that is taught by Shirai.

Let me see, so I'll go back to Figure 2 and just verify those labels. And the labels look like they match from what I read out in the specification.

THE WITNESS: Incidentally, I think it's been another 45 or maybe 40 minutes or something like this. So if there's a good time to take a break, I would like to request one.

MR. JENSEN: Yeah, I accommodate you, so we can take a break.

THE WITNESS: Okay. Thank you.

(Whereupon, a brief recess was taken from 4:02 p.m. to 4:09 p.m.)

BY MR. JENSEN:

Q Welcome back, Dr. Khatri.

A Thanks.

Q So we're looking at the Shirai reference, Exhibit 1018, at Figure 2.

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A Hold on. Exhibit 1018, yep, Figure 2. Let me go there again. Sorry.

Figure 2, yes, I'm there.

Q Okay.

And would you agree with me, Dr. Khatri, that Figure 2 of the Shirai patent is a cross-section, that it corresponds to a 3D memory device with a vertical memory arrangement?

MR. LOWRY: Object to form.

A Again, you know, the term "vertical memory arrangement" is, you know, not completely parsable. So I will request you to rephrase that question.

Q Well, let me ask it this way: Is Figure 2 of the Shirai reference depicting a stacked 2D NAND memory structure?

A Did you say, "a stacked 2D NAND memory structure"?

Q Yes.

A So Figure 2 of the Shirai reference, you know, if I look at -- hold on, I'm sorry.

As I was sort of reading when we

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stopped -- sorry, I'm going to go back to where we were.

Yeah, it says: As shown in Figure 2 -- this is paragraph 30 -- the stacked body 100 includes a first stacked portion 100, connection portion 45, second portion 100b, and partly the first stacked portion is provided on a substrate 10.

So if I look at the Figure 2 again, you know, there's a substrate 10, which is like at the bottom, and the first stacked portion is provided on top of it, as you can see, the first stacked portion being labeled 100a.

And it has multiple word lines that are depicted, and these are depicted as label 41.

So there are word lines that are arranged on top of a substrate 10. And so this is basically, you know, 3D memory which involves word lines that are stacked on -- I mean, that are placed on top of a substrate 10.

And this is further supported in the specification of Shirai in paragraph 3

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where it talks about "a semiconductor storage device having a three-dimensional structure in which memory cells are three-dimensionally disposed."

That's basically saying that the topic of this patent -- because this appears in the background -- the topic of this background is a semiconductor device which has a 3D structure, and it pertains to memory cells, and these memory cells are three-dimensionally disposed.

And we were able to confirm that by looking at Figure 2, because as we just discussed, Figure 2 has a substrate 10 and multiple word lines 41 that are disposed on top of the substrate in the 100a element, which is disposed on top of the substrate as well.

Q Is Shirai Figure 2 limited to any particular number of word lines?

A So, you know, I mean, let's see again on Figure 2.

In general, the number of word lines would be, you know -- would be -- I mean, first of all, if someone cites to

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Figure 2 in a combination, for example, right, and now in this other reference, for example, Dong has -- you know, has labels of word lines like, you know, labels I through J or something, then those I through J would be inferred based on the number of -- and let's say that was being mapped to Shirai Figure 2 or for Shirai's teaching, then those word lines would be matched to the number of word lines that are depicted here in Shirai.

So that's what would be the -- you know, in that situation, a number of word lines would be induced by counting the number of word lines in this figure or in any figure of Shirai.

In general, I would like to verify if Shirai, you know, has any language that limits the number of word lines in Figure 2 or any other figure.

Q I'll direct you to paragraph 30, which I think you had mentioned previously.

A Okay. I can look at paragraph -- 30, you said?

Oh, yeah, 30 describes Shirai in

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some detail. And let me read that...

Well, there's also paragraphs after that.

Let me just quickly read that and confirm.

So paragraph 30, as we said, is talking about the two stacked portions, 100a and b.

Oh, and paragraph 30 literally says: "Each of the stacked portions 100a and 100b may have any number of stacked layers."

But like I also said -- so Shirai is stating that the number of stacked layers in Figure 2 may be variable.

But if I'm using Shirai as a secondary reference to do some mapping of -- you know, of indices of -- you know, of word lines, then the word lines that -- you know, that I would use is the number of word lines I can literally count on Figure 2, unless there was a mention of -- unless there was an explicit mention of a modification drawing about -- of Shirai, a modified version of Shirai with a different

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number of word lines.

Q All right. Let's -- you can put that to the side, and let's go back to your POR declaration --

A Okay. I'll close that. Yeah.

Q -- at paragraph 76.

A Okay. Let me go there really quick.

I'm going to really quickly read that, the region around that paragraph, before I answer.

Wait, did you say the POR reference?

Q Your POR declaration, Exhibit 2028.

A Oh, sorry, yeah. I'm there now. 76, got it.

Q Sorry, are you there?

A I'm there, yes.

Sorry. I'm just reading around that paragraph just to orient myself.

Q And this is where you reproduce the Figure 8.11 from the Aritome textbook, correct?

A Yes.

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But if you don't mind, can you give me one second? I'm just reading a couple of paragraphs above and below that just to orient myself.

All right. I'm ready to answer your question about paragraph 76.

Q And so my question will be about the Aritome Figure 8.11.

Do you see in the middle of that figure there's a couple of boxes, or tables? One of them is called "Conventional modes," and the second one is called "Additional modes in 3D"?

A Yes, I see those boxes.

Q What does conventional modes refer to?

A So this figure is talking about program -- as seen in the caption, it's talking about program disturbance modes of a 3D NAND flash memory array.

And the table in the middle is comparing the disturbed modes in a conventional setting versus the additional modes in 3D, which is the caption of the lower table.

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So conventional modes here would mean the modes that you encounter in a 2D memory -- in a 2D NAND flash memory.

And it's well-known that in 2D flash memory, the disturb modes are -- there's one disturb mode, which is the X mode.

But what this figure is -- sorry, what this Figure 8.11 below paragraph 76 is depicting is that in 3D NAND flash memory, as shown in -- as arranged in Figure 8.11(a) on the left, there are additional disturb modes that occur, and these are called X mode and XY mode disturbs.

Q Did you say -- I guess could you repeat, what are the two additional modes present in 3D?

A Yeah. So the additional modes of disturb -- because this -- both these tables are talking about disturb modes because the caption in Figure 8.11(a) says program disturbs modes for 3D flash array.

So the disturb modes are described here. There are four rows in the

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two tables.

The table on top, which says, "Conventional modes," corresponds to 2D NAND flash.

And in this, the first row, that's numeral 1, is basically the one that's being programmed. That is a string that is being programmed.

The second one is a disturb mode, which is a disturb mode in the X direction, which is traditionally called the X disturb.

So X disturb already existed in 2D NAND flash. So that is -- that mode of disturb is inherited by 3D NAND flash.

But in 3D NAND flash, there are additional -- there are two additional modes of disturb that are depicted, and they're in the lower table where it says: "Additional modes in 3D." And these are modes that are called the Y mode and the XY mode of disturb.

And Aritome has, you know, in some sense a -- you know, a detailed description of these modes and how some of

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these are more problematic than the traditional X mode that you had in -- that you had in the 3D NAND flash.

Q So you mentioned that the conventional modes are labeled with the -- you know, 1 circle and 2 circle exist in 2D NAND.

Did those disturb modes also exist in 3D NAND?

MR. LOWRY: Object to form.

A Can you repeat that, please?

Q Yeah.

So you mentioned that the conventional modes labeled 1 and 2 are present in 2D NAND, and my question is: Are those two modes -- disturb modes also present in 3D NAND?

A So the -- so I'll correct the question a little bit.

The item 1 is basically the string that's being programmed. So that's not a disturb situation. That's the string that you actually want to program. There's no disturb that happens -- there's no program disturb that's happening on the

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string number 1.

It's string -- you know, string number 2 and its cohorts, if you will, right, they are undergoing X mode disturb. And that's the only kind of disturb you have -- only kind of program disturb you have in 2D NAND.

This X mode disturb is inherited by 3D NAND as well. So X mode disturb does exist in 3D NAND. But in additional -- in addition, 3D NAND has -- 3D NAND flash has additional modes, as the second table describes.

So in 3D NAND, you have new modes in addition to the X mode, which are called X mode -- sorry, Y mode and XY mode.

And if you open Aritome part 2, it shows you the relative, if you will, badness of these modes in Figure 8-13, which is just a couple of figures below the one that's cited, you know, in this figure.

And it shows here that, you know, the XY mode and the -- XY mode is just slightly worse in terms of its badness, if you will, or its -- of its --

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if it -- of the amount of disturb it generates than the X mode.

But the Y mode is much more -- or creates much more disturb. And this is based on Figure 8.13(b) of Aritome.

So this is a relative comparison of how bad these modes are. And as it turns out, the new modes in 3D are more problematic than the existing modes that used to be there in 2D but are still inherited in 3D.

Q Did I understand you correctly to say, Dr. Khatri, that there is only one conventional mode of program disturb?

MR. LOWRY: Object to form.

A I believe that question was incomplete. So could you complete it?

Because you just said there's only one mode of program disturb, but were you referring to -- what kind of memory?

Q In 2D memory.

A May I request you to complete the question again so I can answer it cleanly?

Q So let's just look at the table

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in Figure 8.11 underneath the heading "Conventional modes."

Do you see that?

A Yes, I see that.

Q And it uses the term "modes" in the plural.

Do you see that?

A Yes, I see that.

Q So my question is: How many conventional disturb modes are being shown in the Aritome Figure 8.11?

MR. LOWRY: Object to form.

A I would request you to repeat the question. I didn't catch the last part.

So you said your question is, and then I couldn't understand the rest.

Q How many conventional disturb modes are being shown in Aritome Figure 8.11?

A I see.

MR. LOWRY: Same objection.

A Okay. So Figure 8.11, as the caption says, talks about program disturbance modes.

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In Figure C -- you know, 8.11, the caption under -- below -- I mean, sorry, to the right of (a) -- to the right of the sub-figure labeled (a) says, Program disturb modes of 3D NAND flash cell array, where it says also N strings are connected to the same bit line in the same block, which basically Figure 8.11(a) visually describes as well.

Then it describes Figure 8.11(b). And for that, the caption is Comparison of program disturb modes in a 3D NAND flash array, and it says: "In a 3D NAND cell, two new modes of Y-mode and XY-mode are added."

So it is essentially saying that in 3D NAND, based on the table that's the lower table, the table that's below, which is captioned as "Additional modes in 3D," two new modes are appearing, which are labeled as code strings in Y-mode and strings in XY-mode.

So those are the two new modes, quote/unquote, of Y-mode and XY-mode, which the captions, you know, depicts as well.

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And the conventional modes are basically the X-mode, because this is talking about program disturbance.

Q Yeah. So I'm confused by your answer.

Does the table in Aritome Figure 8.11 titled "Conventional modes" disclose one conventional disturb mode or two disturb modes?

MR. LOWRY: Object to form.

A Sure. The table -- you know, the top table labeled "Conventional modes" in Figure 8.11 -- first of all, I'll just clarify, it sort of corresponds to program disturbance modes. It's talking -- specifically about program disturb.

And if you look at the top table, it says, "Conventional modes" in plural, but the two items that it lists are item 1 and 2, and item 2 says: "String in X-mode." That's a specific mode.

And item 1 says: "String in program."

That's the string being programmed. That's not a disturb.

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So there is one disturb -- there is one program disturb mode in 2D that's described in Figure 8.11. And that one program disturb mode for 2D, based on the top table, is "SDR in X-mode." That's the X-mode that's been described.

Q Can program disturb occur on the string being programmed?

A The string being programmed is being programmed. So that's the one that you're trying to program.

So it's not the one that's being disturbed. It's the one that you're targeting to program.

Disturb happens on -- sorry, disturb happens on cells that you don't intend to program, but they get accidentally programmed or they get accidentally elevated in their threshold voltage, which is what disturbance means.

Q So let me clarify my question.

Can a cell that is not being programmed but is connected to the same string as a cell that is being programmed suffer from program disturb?

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A May I ask you to repeat the question because it seemed like an important and sort of long question.

Q Well, let's just look at the image in Aritome Figure 8.11 on the left.

Do you see the memory string with the number 1 by it?

A Okay. Yes, I see it.

Q And that's the string being programmed, correct?

A You know, that's the -- the string number 1, as depicted in the table on the right that's labeled as "Conventional mode," has a -- has as sort of a caption that says: "String in program."

So that's the string being programmed.

And I'll also point out that this entire table -- I mean, this entire Figure 8.11 is only about program disturb. It's not about other disturbs. It's talking about specifically program disturb.

Q And in the string number 1 that's being programmed, at any given time,

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how many cells are being programmed?

MR. LOWRY: Object to form.

A In the string -- I mean, please repeat that question. I couldn't -- you know, again, I lost it.

So in the string being programmed...

Q Yeah, how many cells are being programmed at a given time?

A Okay. In string 1 -- sorry, in the string labeled 1, that's the string being programmed.

A specific cell in that string is being programmed, and that's the cell that's shown in the lighter font, the light-colored font. That's the target cell that's been programmed.

So we don't talk about disturb for that cell because that's a cell we want -- we need to change to a specific value. That's what we want to program in it because that's the value we want to store in it.

Now, that shaded -- that lightly shaded cell in string 1 shares a word line

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with a whole bunch of other cells. And those cells are sort of indicated by this dotted outline -- this sort of dotted outline which is like a trapezoid.

That dotted outline touches the lightly shaded cell of string 2, of string 3, of string 4, and the two strings in the back of the figure as well.

So with there being a total of six strings, one of those strings has its light-colored transistor being programmed. That's string number 1. And all the other strings don't want that -- their light-colored transistor to be programmed.

So string 2, 3, 4, and then the two back strings, they don't want their transistor to be -- their light-colored transistors to be programmed or to be minimally programmed or for it to be sort of modified in their programming because that's what is defined as a disturb -- a program disturb.

So the light-colored cell of string 1 is what they're programming.

The light-colored cells of

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string 2, 3, 4, and the two strings in the back will accidentally get a little bit of increase in their threshold voltage because these all share the word line. The word line connection is shared between the light-colored transistors of all six strings.

So the five strings that we don't want to program will get affected, and the way they get affected has a name.

The way string 2 is affected is called X-mode, as the -- you know, the table called "Conventional mode" suggests.

The string labeled 3 will be affected or program disturb in a Y-mode. And string number 4 will have a program disturb in XY mode.

So these are how the disturbs of these different strings, which we didn't intend to program, when they get disturbed, or when they got modified slightly and their VT increases, we give that disturb a name.

And this disturb name is called X-mode for strings like string 2, Y-mode

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for strings like string 3, and this would also be for the string behind 3 on the back on the left.

And then also strings -- other strings would be getting a disturb in what's called XY-mode, and that would include string 4, and also the string to the back of 4 on the right side of this figure.

Q Yeah. So my question is about the string with the number 1 by it.

A Correct. Okay.

Q Right?

And you said the light-colored transistor is the cell that's being programmed, correct?

A Correct.

Q Okay. And beneath that in string 1 is a dark-colored transistor that's connected to the cell above it, correct?

A That's correct.

Q Okay. Is the dark-colored transistor on string 1 susceptible to program disturb?

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A So the dark-colored transistor below string 1 has a word line, which is shared with all the other five dark-colored transistors in this figure.

So there's six transistors which are dark colored that all share a word line.

None of those six transistors is being -- is intended to be programmed because they're all dark, and -- you know, and therefore they don't get affected by program disturb. They're not subject to program disturb.

They may be program -- subject to other disturbs, but they're not subject to program disturb, which is the -- which is the subject of Figure 8.11.

Q Is it your testimony that none of the dark-colored transistors shown in Figure 8.11 are subject to program disturb?

MR. LOWRY: Object to form.

A So the -- you know, the transistors that are subject to program disturb are the light-colored ones.

The dark-colored ones may be

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subject to other disturbs, but they're not program disturbs.

Q What would you call those other type of disturbs?

A So those other disturbs are typically called a pass voltage disturb that happens during the programming of cells in the array.

And we've talked about those at some length in the -- in an earlier portion of this deposition.

Q Would you agree with me, Dr. Khatri, that the first program disturb, the one labeled "STR in PGM" in Figure 8.11, can affect the transistors in the memory strings selected for programming?

MR. LOWRY: Object to form.

A I would like to hear that question again.

Q Yeah.

Would you agree with me that the first program disturb mode, number 1, labeled "STR in PGM," can affect transistors in the selected memory string?

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A Transistors in the selected memory string, you mean string 1?

Q Yes.

A Okay. So -- and first of all, you called this a disturb mode, right?

You said the first disturb mode which is labeled "STR in PGM."

The disturb modes are -- the program disturb modes -- because remember that's the title of this figure. The title of this figure is Program Disturb Modes of 3 NAND Flash Array.

If we actually go to Aritome where it's actually described, that's on page 362 of Aritome, and the section that this belongs to is Section 8.4. It's called "Program Disturb."

It's all about -- program disturb means program disturbs that happen to cells that are sharing the word line with the cell that's being programmed.

Again, Section 8.4.1, its title is "New Program Disturb Modes," talking about new program disturb modes, and then it specifically says: "Program disturb

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phenomena and mechanisms of a 3D NAND cell are much different from that of a 2D NAND cell."

And slightly below that is described the Figure 8.11 that we are talking about.

So again, if you're reading this, a person of ordinary skill in the art realizes that this entire section is about program disturb modes, not about other disturb modes. It's only ever talking about program disturb because that's the topic of the Section 8.4 and the subsection of 8.4.1, which talks about new program disturb modes, which happened to be in 3D because that's what it says in the next line, that it's comparing the program disturb phenomenon and mechanisms of a 3D NAND cell with a 2D NAND cell.

And then it goes on to describe in text the figures that we are -- that we are talking about. It describes Figure 8.11(a), you know, and it talks about -- let's see...

I'm trying to see the

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significant parts of it, I guess. It's mostly a repetition of what I had said. So I guess I don't really see a need to read that again.

Let's see...

Let's see...

I mean, it's describing what I've described in my deposition -- let's see -- around -- the deposition describes these different X-mode, the Y-mode and the XY-mode I believe in paragraphs 76, and there should be -- 77 and 78.

So basically, you know, I've described the different disturb modes in the paragraph 76, 77 and 78, and these are sort of describing different words in Aritome on page 363.

Let's see...

I'm trying to see if there's anything significant to add from here.

Well, it just describes the electrical bias conditions for these different modes.

And so if you look at, for example -- you know, if you look at, you

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know -- let's see...

If you look at Figure 8.13(b), 8.13(b), which is on page 365 of Aritome, it talks about the relative disturb values of these, you know, three disturb modes.

Now, the three disturb modes are, you know, the X-mode, the XY-mode and the Y-mode. Those are shown on the -- sort of the right side of Figure 8.13.

And the actual programming -- I mean, some that's actually being programmed, it happens to be labeled as PGM mode, because that's the threshold mode that's changing it for the cell that you're targeting.

It happens to be called a mode in this case.

But if you look at the caption of Figure 8.13, if you look at 8.13(b), it says: "Cell VT shift in ISPP program operation of program mode, PGM."

So PGM is the program mode. It is not a disturb. And it literally says: "N3 program disturb modes of X, XY and Y."

So this caption of 8.13(b) is

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clearly delineating that what is called the PGM mode is actually the program mode. It is not a disturb. And the disturb modes are three in number, and their names are X, XY, and Y.

So if we apply this back to Figure 8.11, we see that the table that we've been referring to has string number 1 that says, String in Program," that's not a disturb mode. That's just a program mode.

And then, you know, number 2 is string in X-mode, which is a disturb. And the new disturb modes for 3D are number 3 and 4, which are strings in Y-mode and strings in XY-mode.

So in some sense, this table as read together with table -- sorry, with Figure 8.13 illustrates that Aritome is talking about all four strings, 1, 2, 3, 4, as modes.

But among these modes, number 1 is just a program mode. It's not a disturb. And 2 -- and then number 2, 3 and 4, which are labeled X, Y, and XY, are disturb modes as indicated by the caption

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of Figure 8.13(b).

Q So you say in the second sentence of paragraph 77 -- and I'll just read this aloud -- "The first program disturb (labeled as 'STR in PGM' in the figure above) can occur in flash transistors in the selected string (a string selected for programming, such as string 1), for flash transistors that have a pass voltage Vpass applied on their control gates."

A Yeah. So I'm glad you brought this up because this is an error, and I had missed it.

When it says: The first program disturb mode labeled star -- STR in PGM, that's not a disturb mode, as we just confirmed from Figure 8.13 caption -- the caption of 8.13(b).

This should just say the first -- you know, let's say the first mode -- instead of saying the first program disturb mode, it should say the first mode labeled as STR in PGM in the figure above can occur in flash transistors in the

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selected string, and it should just say the flash transistors that are being programmed.

So it should say for flash transistors in the selected string that have the program voltage applied to their control gates.

I'm glad you pointed this out because, you know, when I was preparing, I didn't really read this because I assumed they were right, but this was an error that has crept in.

Q Let's go to Exhibit 1005, which is the Dong reference, and look at Figure 4.

A Just one second. Let me -- may I close the -- what can I close? Sorry.

Is there anything I close right now or you'd like me to keep the other --

Q Just keep your POR declaration open.

A Okay. I'll do that.

And now we're going to -- let's see...

Did you say -- I forgot, sorry.

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We're going to Dong, yeah?

Q Yeah, Dong Figure 4.

A Dong Figure 4, let's go to that. Okay, hold on. Dong Figure 4, let me see. Just let me move to that.

Yeah, I'm in Dong Figure 4 now.

Q And do you see where it says: "NAND string, 400"?

A Do I see where it says: "NAND string"...

Yes, I see that. Yeah, the label, yeah.

Q And there is a voltage Vpgm being applied to word line 5.

Do you see that?

A I see that, yes.

Q Does Dong Figure 4 illustrate a memory string that is being programmed?

MR. LOWRY: Object to form.

A So in Dong Figure 4, you see that WL5 has a voltage Vpgm applied to it. So a person of ordinary skill in the art seeing that would understand that -- let's see...

It doesn't say what the bit line

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voltages are.

So it's not clear whether this is an inhibited string or a string that's being programmed, but a person of ordinary skill in the art looking at Figure 4 would know that something, some -- how do you say it -- some string that shares WL5 is being programmed.

THE WITNESS: Actually, if you don't mind, we've been going for about 45 minutes or something. May I take a little break and then we can come back?

MR. JENSEN: We can take a break.

THE WITNESS: Thank you.

(Whereupon, a brief recess was taken from 4:51 p.m. to 5:00 p.m.)

BY MR. JENSEN:

Q All right. Let me direct your attention, Dr. Khatri, to paragraph 220 in your POR declaration?

A 220, let's see. Let me go there really quick.

220 -- okay. I'm at 220, yeah.

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Q Yeah. And could you read aloud the last sentence in paragraph 220, please?

A The last -- let me see...

Okay. The last sentence in paragraph 220 is cited from Aritome pages 363 and 364, and it reads: "To address program disturbance in 3D NAND, a POSITA would have understood that other methods are used, including '(1) high VT of DSL, (2) applying negative bias to DSL, and (3) inserting dummy word lines between DSL and the edge word line.'"

And this is cited from Aritome pages 363 and 364, which I think we were talking about a minute ago -- I mean, that range of pages.

Q Yes.

What does the acronym "DSL" stand for?

A So let me see. Let's go back to that Figure 8.11, and if you don't mind if you can tell me where it resides because the DSL is described in that.

Q I think we were looking at paragraph 76.

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A Okay. I'll go back to 76 then. Thank you. And we can talk about the DSL in that context.

76, here we go.

So if you look at 76 -- you know, remember we had talked about these strings, 1, 2, 3 and 4, and then there were the two strings in the back -- if you look at each of these six strings, they have a transistor which is an NMOS transistor, which connects to the bit line BL_1 and BL_2, which are shown as diagonal lines.

Those diagonal lines connect to each of these strings, 1, 2, 3, 4 and then the two back ones, by way of this NMOS transistor whose gate is driven by DSL_1, DSL_2, DSL_3, et cetera, to DSL_N with the dots.

So what that really means is exactly one DSL will be on at a time, and the DSL that's on, that's high, is the one that -- you know, all the -- all the strings whose DSL is 1 will be connected to the bit line, and all other strings will be turned off.

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So in this picture 8.11(a), the -- if you will, the front most plane of strings, which in -- you know what, picture so far includes strings 1 and 2, are driving their bit line, or driven by their bit line depending on whether you're doing a read or a write, because DSL_1 is on, as depicted in the picture.

But as you can see, DSL_2 through DSL_N are turned off. So in other words, all those -- all the strings which correspond to -- which are connected to DSL_2, 3, 4, blah, blah, blah, all the way up to DSL_N are turned off and they're not being read or written or accessed.

So DSL is this device, the NMOS device, that's depicted in the figure.

And now to close the discussion and close the loop, the diagram -- sorry, the paragraph we were reading from, if you remind me where it was again?

Actually, I can find it from Aritome, that way I don't have to move from this figure. Just give me one second. It's in Aritome page 368, or something,

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360 -- give me a second. I'll find it.

Oh, there it is, yeah. So it's at the bottom of Aritome 363.

And I'm just going to shrink -- I'm just going to make this PDF smaller so I can fit both on the screen.

Yeah, the last paragraph -- the last incomplete paragraph of page 363 of Aritome says: "In order to suppress a program disturbance in a 3D NAND cell, several approaches to reduce leakage current through the DSL are proposed."

So what's going on here is, there's a large leakage current through the DSL, which is basically causing, you know, a strong -- as it's described above -- let me see...

Is causing a large -- let's see -- or I'm just trying to read the paragraph before that. Sorry.

Yeah, yeah, the paragraph before that in the last line says: "However, in a 3D NAND cell, the leakage current of DSL cannot be easily suppressed because we T off the surrounding A transistor of DSL

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does not become high due to a weak body effect due to program disturb conditions."

So essentially what's happening is the leakage current through the DSL transistor is not something that can be controlled. So the techniques that are described in the following paragraph to fix that are all techniques that will address leakage current.

For example, the first technique, 1, says: "High VT of DSL."

And it's well-known that a high threshold voltage transistor, which is an NMOS transistor, which is high VT, would have exponentially lower leakage current.

So by increasing the VT of DSL in item 1, one would exponentially reduce the leakage current, which is cited as a problem in the last paragraph.

The second item, item 2, applying a negative bias to DSL, accomplishes the same thing because when you apply a negative bias, that turns off the DSLs that are -- you know, that are supposed to be turned off more strongly,

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and once again -- and if I'm not mistaken, that effect is also an exponential effect, you know. The VGS, if it's a negative bias, that would exponentially reduce the leakage current of the DSL.

So both steps 1 and step 2 would cause an exponential reduction in the leakage because that's seen for 3D NAND as the problematic scenario based on the sentence in the last paragraph, which says that "the leakage current of DSL cannot be easily suppressed."

It is being suppressed by doing items 1 and 2, which is using a high threshold voltage device that causes an exponential reduction, and also applying a negative bias, which is item 2, also causes an exponential reduction.

And then finally, it says -- item 3 says: "Inserting dummy word lines between DSL and the edge word line."

So that would indicate -- if we looked at our Figure 8.11, that would mean that we inserted dummy word line between, for example, what is depicted as the DSL

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transistors in the six strings and the transistor below them, which is shown as shaded -- lightly shaded.

So the teaching here is in item 3, let's insert a dummy word line between them.

That dummy word line will not be -- you know, might be used for a real memory cell. But essentially, it will reduce the voltage gradient and reduce this leakage current.

And, you know, that's basically what the teaching of these three steps is.

Q So my question is much simpler.

What does the acronym "DSL" stand for?

A Yeah. So the DSL -- well, I don't know what it -- I guess it must say what it stands for.

But it's basically -- irrespective of the acronym -- and I'll look for it in a second -- it is essentially an -- you know, it is a voltage that's driven to these NMOS transistors, right, which are shortened as DLS_1, DSL_2,

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et cetera.

And it essentially enables or disables an entire plane of cells, you know, and -- sorry, the entire plane of strings in this 3D memory array.

So this 3D memory array is accessed in planes, if you will. So if it accesses the front most plane, we will turn off all those planes below -- behind that.

And now that you asked what does "DSL" specifically stand for, I think it should stand for maybe drain select line or something. I don't know exactly. And I'm not sure it specifically -- oh, there we go.

If you look at page 362 of Aritome, and if you look at the last incomplete paragraph there, the third lane thereof, and I'll read it. It says: "The NAND string STR is located at the intersection point of the drain select transistor (DSL) and the bit line, BL."

So that's kind of weird because its acronym is DSL, but the name it gives is D drain select transistor, which would

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sort of translate to the drain DST.

But reading this, a person of ordinary skill in the art would recognize this as a small typo, and they'd realize that DSL corresponds to the transistors we were just talking about. There are six NMOS transistors that are shown in Figure 8.11(a) that are shown connected to DSL_1, DSL_2, DSL_N, et cetera.

That's basically what "DSL" stands for in there. There's a voltage that an entire plane of these DSL transistors share, and that voltage would be like DSL_1 or 2 or something or up to N.

Q Does the '941 Patent disclose applying any voltages to a DSL line or transistor to reduce program disturb?

MR. LOWRY: Object to form.

A Can you repeat that question, please?

Q Yeah.

Does the '941 Patent disclose applying any voltages to a DSL line or transistor to reduce program disturb?

A You know, the '941 -- first of

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all, the description in my report, the discussion I have of, you know, Figure 8.11 of Aritome, you know, the purpose of it is twofold, to show -- and, you know, and there are multiple other citations from Aritome that I use in my report, all of which show -- and Aritome is, of course, a reference from the petitioner.

So this is petitioner's own reference, which actually shows, you know, conclusively that in 3D NAND, the program disturb modes are quite different than shown in Figure 8.11, and the electrical effect are quite different, you know, and that's shown in Figure 8.13.

So, you know, I'm bringing up Figure 8.11 and 8.13 as support for the comment that I -- I mean, for the section that I have in my declaration which says that the disturb mechanisms in 3D are quite different from the disturb mechanisms of 2D.

That's basically the purpose of Aritome for my -- you know, for my use of Aritome.

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In other words, when someone was designing a 3D memory, they would actually look at, you know, from something like Aritome and realize that the disturb mechanisms are quite different. There are two new disturb mechanisms, the Y and the XY.

And this is described in my declaration in paragraphs like 76 through 83.

But yet further, when I describe the Dong reference, you know, I actually show conclusively that -- you know, that there's this mechanism called NLSB, or natural local self-boosting, that happens in 3D but doesn't happen in 2D NAND flash.

And for that reason, again, disturb mechanisms are quite different, and I cite to several papers for that.

So the whole point is that I'm citing these references to show that 2D NAND and 3D NAND have completely different mechanisms, and the voltage teachings of Dong, which is in 2D, would not -- a person of ordinary skill in the art would not look

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to Dong, which is a 2D reference, to learn about disturb mechanisms in 3D, which is the '941.

And, therefore, Dong would not, you know, be either anticipating or -- you know, would not be a good ground -- would -- I mean, would not anticipate or render obvious the '941 Patent.

So that's the purpose, you know, and in particular, the '941 Patent shows voltage, you know, assignments to actual word lines, not to NMOS transistors, which are select transistors.

So if we -- as we've discussed, if we look at the '941 Patent -- and I'll just open it real quick -- you know, its figures are all talking about voltages applied to word lines, like WL something, you know, various WLs.

But it's not talking about the additional transistors, the select transistors, like DSL, for example, because that's not the focus of the '941 Patent.

Q Let me take you to Exhibit 1012, which is the Costa reference.

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A Okay. Let me see. Is there anything -- like I have two or three things open.

Is it possible I might close some of these or --

Q If you'd like.

A Okay. I'm going to close maybe then everything. I'll go and open -- 2012 you said, yes, or 1012?

Q 1012.

A 1012, okay. I'm there now.

Q And are you familiar with this reference?

A Yes. We've talked about it I think early in the deposition.

Q Can you look at the abstract of Costa, and just go ahead and read that to yourself and then I'll have a question.

A Okay. Let me do that.

Q Have you read the abstract?

A Yes, I have. I was actually looking for something else, but I did read the abstract.

Q Do you see at the end of the abstract, it refers to something called

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channel resistance?

A Let me see...

Correct. It talks about an increased channel resistance.

Q What is does channel resistance refer to?

A So now when you have a -- you know, a series connection of -- you know, of many NMOS transistors or even flash transistors, these are built on top of a channel, you know, also sometimes called a body or also called a -- you know...

So this -- this electrical terminal called the channel is if you have a string, or if you have a series connected bunch of transistors, they all share a channel. So that's basically the channel of the string.

So what this is referring to is the resistance or, you know, this is the electrical resistance of this channel that happens to be something that all the transistors in the series connected set of transistors or the string share.

Q And what is it that causes the

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channel resistance to increase in a memory string?

A So, you know, it's not some -- that question I would modify. You know, it's not any memory string that would have an increase of channel resistance, but particularly a NAND memory string because a NAND memory string has a large number of transistors in series. And these are flash transistors.

Now, if each of these flash transistors have some resistance and, you know, without loss of generality, we might say the channel resistance of one transistor is R, like the value R, then if you have many transistors in series, many NAND -- you know, which is what you have in NAND flash because you have a string of transistors, then the string would have a resistance which is multiple times R to the first order, right? And then there's nonlinear effects as well.

But the first order of the string of NAND transistors would have a resistance which is proportional to N times

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R because there are channel resistance pieces of each of the transistors that are sort of -- you know, that are connected in series resulting in an additive channel resistance.

Q Well, why does channel resistance matter in a NAND memory string?

MR. LOWRY: Object to form.

A You know, I mean -- you know, in a circuit, you know, resistance matters, you know, and then there are different ways of addressing it.

You know, in some situations, you know, channel resistance is not the dominant electrical effect that one has to control. In other situations, channel resistance might be the dominant electrical effect that one has to control.

So in some sense, channel effect is a -- sorry, channel resistance is a physical sort of reality. But depending on what I'm designing, depending on how I'm designing it, depending also on how I'm using that particular design object, that channel resistance may be of concern or may

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not be of concern.

It's not necessarily always a bad thing. It may be something that can be benign or something that, you know, in certain conditions, one might even -- one might even exploit it for certain circuits.

I don't know if I've seen that, but now that gives me some ideas.

But channel resistance is a physical reality, like in an electrical circuit or, you know, when you have a series connection of devices.

Now, depending on what you're doing with the devices and how you're driving them and such, it may be, you know, a bad thing, and it may be actually a benign thing, and it actually may be something that I can make use of.

So, you know, general resistance in this case, you know, is shown to be -- I mean is considered a bad thing, and so they're trying to do techniques to address it, but it's not universally a bad thing.

Q What is Costa's proposed technique for reducing the effects of

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increased channel resistance that occurs as more memory cells are programmed?

A So I'll first start with a -- you know, like a comment. Like Costa talks about channel resistance and, you know, mitigating effects of it specifically in the context of verification.

That's why if you look at this paragraph you just asked me to read, you know, it starts with the word "sensing," and "sensing" means, you know, verification or reading.

So this is pertinent to reading, and there's multiple disclosures in Costa that say it's about verification.

And I've said this in multiple places in my declaration, and actually, so has, you know, the -- you know, the petitioner has also sort of agreed to that as well as Dr. Liu.

So, for example, sensing appears at least twice, you know, in the abstract itself. And in -- you know, in -- and the term "verification" applies as used in Costa as well.

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So that's my preamble, I guess, that is saying Costa is applicable for the sensing operation or the verification operation. I start with that comment.

And the technique that Costa teaches is specific to verification. It's specific to what happens when you read, you know, the threshold voltage of a transistor after having programmed it.

So there's two phases, the programming phase and then there's the verification phase. They are quite distinct, and petitioner as well as Dr. Liu have agreed to that.

Now, what is the specific technique that, you know, Costa teaches?

The technique is described in Figure 9A and 9B, I believe. Let's see...

So if you look at Figure 9A -- if you look at -- hold on a second real quick.

So, yeah, if you look at 9A -- let's see...

I'm just kind of orienting myself because it's sort of sideways and so

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I'm kind of having a hard time like twisting my head when I read it.

Okay. In Figure 9A, you can see that the source terminal, which is at 0 volts, is on the left side of Figure 9A. And the word line that's being verified or sensed in Figure 9A is the dark word line, which is word line labeled as WL3.

So WL3 has this verification voltage that's applied to it, and that verification voltage as shown in Figure 9A, as well as in the little table below it, which is captioned as "Verifying WL3," that shows that WL3 is driven by a voltage called Vcgr. That's sort of the verifying voltage.

But now, if you look at the voltages in -- that are described in the table for word line 0 to -- and also, from 4 to 127, they're all -- they all have applied a voltage Vread to them in Figure 9A.

So 0 to 2 as well as 4 to 127 have a voltage Vread applied to them, and WL3 has a voltage Vcgr applied to them.

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Now, this is in the context of verification. This is not a programming context because the -- you know, nowhere in here it shows a programming voltage, which it doesn't because Costa is about verification, not programming.

Now, in Figure 9B, you know, the solution that Costa proposes is shown, and in this figure, the Vcgr -- I'm sorry, the word line that we are trying to verify is way towards the right in comparison to Figure 9A. In particular, it is on word line 124.

So that's why the little table or the little caption below Figure 9B says: "Verifying WL124."

And when we are verifying WL124, the table shows that WL124 is driven by Vcgr, the read voltage.

But now interestingly, if you look at the voltage that's applied to WL0 through WL123, those voltages from 0 to 123 are assigned a voltage, which is really plus 100 millimoles.

In other words, they're applied

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a slightly higher voltage than what you saw in Figure 9A.

And for word lines 125 through 127, which are to the right of the word line that we are verifying, the read voltage -- the applied voltage is still VE.

So this is essentially the solution of Costa. The Costa solution says that in Figure 9B, since we have a large number of transistors -- that's transistors WL -- sorry, the transistor is connected to WL0 to WL123, that's 124 of them, then we have a large channel resistance due to them.

And to compensate for that, the gate voltage is overdriven by 100 millimoles. That's indicated by the fact that WL0 through WL123 are driven by really the plus 100 millimoles.

But in Figure 9A, you know, the number of transistors to the left of the word line that we are verifying is only 3. That's WL0, WL1 and WL2.

So that doesn't incur a sufficiently large -- that doesn't incur a

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sufficiently large channel resistance. And for that reason, the gate voltages are WL0 through WL3 -- sorry, to WL2 as shown in the table beside Figure 9A is much lower and it's simply Vread.

So essentially, the gist of it is, if you have a large channel resistance because of verifying that you're doing is, you know, for a word line that has a large number of other word lines between it and the ground terminal, then you increase the read -- sorry, you increase the VT voltage for all these lower -- sorry, for all these -- you know, for all the word lines that are to the -- towards the -- towards the source terminal from the word line that we are reading. That's as shown in Figure 9B.

But if we are reading something that's really close to the source terminal, like you see in Figure 9A, then you don't overdrive the gates of the word lines to the source side of the word line that you're verifying.

Q Let's go back to Dong,

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Exhibit 1005.

A Let me see. Sorry, hold on.

Okay. There it is. I'm there.

Q And please turn to Figure 20.

A Okay. I see that.

Q What is shown in Dong Figure 20?

A So I'll kind of answer this in two ways. The first answer is based on, you know, what we see on this figure, and then sort of talk to the -- you know, to what it's doing.

So what we see in this figure are, you know, these pulses labeled 2005, 2010, 2015, and so on, and these are progressively increasing in size.

And between these pulses, which I just mentioned, that have arrows next to them -- that's 2005, 2010, 2015, and et cetera -- are smaller pulses, which are labeled 2006.

So this figure shows a bunch of pulses, so large ones and then small ones between them, that are -- the label is 2006.

Now, this essentially is -- I'm

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going to read from the specification to see what this -- what it says, and then, you know, I might fill in the blanks if it's not completely clear.

So let's see, this is Figure 20, and I'm trying to find it -- oh, there it is.

So Figure 20 is described in paragraph 129.

So in paragraph 129, it says that -- let's see...

You know, that says that we are using "stepped program pulses of the pulse train 2000 of Figure 20 applied to the appropriate selected word line."

So sure we are seeing stepped progressively increasing word line pulses for programming.

These pulses are -- let me just double-check this from the spec, please.

Okay. I think I'm going to switch to paragraph 132, which says: "Figure 20 depicts an example pulse train 2000" -- which we can readily see on the screen -- "applied to the control gates of

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non-volatile storage elements during programming" in the switch -- "and a switch in boost mode which" incurs -- "which occurs during a pulse train."

So now it says: The program -- "The pulse train includes a series of program pulses 2005, 2010, 2015, 2020."

So all these large pulses which have an arrow next to them in Figure 20 are described to be "a series of program pulses."

So these are program pulses and it also says these "are applied to a word line selected for programming."

So a person of ordinary skill in the art now reading this understands that these are program pulses. They will be applied, you know, to the selected word line.

Now, further in this description, it says -- let me see...

Yeah, it says then later in paragraph 132: "In between program pulses are verify pulses."

And these are described as label

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2006.

So once again, person of ordinary skill in the art looking at this Figure 20 sees a pulse train 2000, which contains program pulses with the arrows on them followed by -- you know, followed by these verified pulses 2006.

So the language I just read where it says, "in between the program pulses are verified pulses," clearly indicates that programmed pulses and verified pulses are distinct, as the figure itself shows, and that the program operation and the verify operation are also distinct, as the figure shows, and also as the petitioner and Dr. Liu agree with.

Now, it also says: "For example, verify pulse set 2006 includes three verify pulses," which one can see in this figure, and it also says certain embodiments might have a slightly different verify pulse situation.

So this is essentially -- this figure is a -- so from what we've read and from what we've seen, this figure is a

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pulse train 2000 which contains program pulses 2005, 2010, et cetera, and all these pulses with arrows labeling them.

But in between these program pulses are verify pulses, which are distinct, and that's what this figure shows.

Q What is the purpose of the pulses labeled 2005, 2010, and 2015, et cetera?

A So let me check -- I mean, you know, I'll try to see if I find some language in my specification that speaks to the purpose. So give me a second, please, while I look for that.

I'm trying to see where this should be.

Okay. So I'm not able to find a direct quote, but I also explain how program and verify work.

So as we recall, when we are programming -- when you're programming a cell in a NAND flash memory, what we apply to it is this voltage Vprogram, which we've seen the label called Vpgm in the '941

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Patent.

So that Vprogram is applied to the cell -- you know, is applied to a word line which will be used to target a particular cell which we want to program.

So when we program that -- and I'll now point to Figure 20 of Dong.

When we program that, we start off with the cell being in what's called an erase potential, which is a negative threshold voltage, and we would like to bring this threshold voltage of this cell to a certain positive value.

Now, when we apply the first program pulse from Dong -- let's pretend we're using this in the Dong situation in a 2D NAND flash memory context.

So I'll open Dong really quick, and I'll open it to Figure 20. So I'll speak to the numerals from that.

In Figure 20 of Dong -- where is it...

Oh, thank you.

So we would first apply a program voltage of amplitude and a height

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2005 to the word line of -- or the cell we want to program.

Now, Fowler-Nordheim tunneling would happen, and the threshold voltage of our cell would move from a negative threshold to some other threshold, but we don't know yet whether it has reached the threshold we would like it to reach.

So we're not sure quite yet whether the -- the desired threshold voltage for this transistor has been accomplished.

So the first step we do is programming. That's 2005.

To check whether we got the right threshold voltage, we do a whole different operation.

And this operation is admittedly agreed upon by, you know, petitioner as well as Dr. Liu. It's completely different. It's a different step from the programming step, and it's called a verifying step.

So, for example, you know, in this step, we are going to apply

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Vvoltages -- we are going to apply voltages specifically to the cell we partly programmed.

And we'll read -- we see where it just barely turns on, and when it turns on, we know that that's the threshold voltage that it achieved.

So this is called a verification step. The first step was 2005, 2010, 2015, all these little pulses with the arrow that are the programming step, and there's a separate and distinct step, which is a series of small pulses which would test what threshold voltage we have accomplished, and that's step 2006, which is called a verification step.

Now, I'm going to point to paragraph 233 of my declaration where I say that, you know, Dr. Liu previously testified about the Costa reference in particular and says: "Costa teaches adjusting voltages for verify operations alone."

That is, Dr. Liu is agreeing that Costa focuses on addressing program --

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sorry, on adjusting voltages for the verify operations alone. That would be the 2006 steps, the verify steps.

And also, you know, the petition also says -- and this is, again, I'm reading from paragraph 233 of my declaration.

Petition says that "Costa 'focuses on addressing program disturb impacts arising from the verification phase.'"

And also, you know, Costa -- you know, like I cite Exhibit 2022 says: "Costa discloses using its read operations to verify programming."

In other words, these are separate and distinct steps, and they're used, you know -- and Costa addresses only the verification part and, you know, '941 addresses the programming part.

So they're basically addressing completely different steps. They're completely different phases which are used, you know -- are not done simultaneously.

Q Would Dong's program operation

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in Figure 20 be complete after programming pulse 2005 if the memory cell did not reach the desired voltage?

MR. LOWRY: Object to form.

A So, you know, here, the most important thing is what the definition of, you know, "program operation" is.

So, for example, if we look at the '941 Patent -- let me open the '941 Patent really quick. That's number 1...

And there are several other references I cite, which also agree about what the meaning of "program operation" is.

So, you know, Dong specifically says that, you know -- and then we've gone over this before, but -- sorry, not Dong, the '941 Patent says in paragraph 3, lines 4 to 8, it says: "In the text" -- that is in the spec -- "when a word line is said to be programmed, it may mean that the word line is used to perform a program operation."

And then it defines: "A program operation said in the text may be an operation for programming a memory cell."

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So the -- in the context -- in the intrinsic context of the '941 Patent, the program operation is only concerned with, quote, you know, an operation for programming of memory cell performed using, for example, a set of transistors.

It's not interested in whether the programming operation was complete or incomplete or whatever. It just says the program operation in the context -- in the intrinsic context of the '941 Patent is just defined -- just the part of the operation of programming of memory cell is what it basically teaches.

So, you know, this is clearly showing that, you know, the focus of the '941 Patent is just the programming of a memory cell.

And if I looked at it in the context of the pulse train 2000 of Dong's Figure 10 to 20, that would mean the arrows that were labeled 2005, 2010, 2015, et cetera.

Q But suppose, looking at Dong Figure 20, that it took five programming

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pulses to reach the desired voltage threshold, in your opinion, would that constitute one program operation or five program operations?

MR. LOWRY: Object to form.

A Again, for that, I would basically stick to the intrinsic teaching of the '941 Patent, and the '941 Patent simply says, you know, that -- you know, when a word line is said to be programmed, it may mean that the word line is used to perform a program operation.

And then it defines: "A program operation in the text may be an operation for programming a memory cell."

It is silent about whether it needs five operations or one operations. It is basically just saying the programming of the memory cell is what a program operation is.

And also, if you look at the following set of lines following column 3 -- sorry, let me say from column 3, lines 9 through like 17, it specifies more precisely what the program

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operation is that the '941 Patent is contemplating.

It says: "When an xth word line WLx is used to perform a program operation, the controller may supply a voltage Vprogram to the xth word line WLx."

And I won't read further because I read that to you earlier, but in the subsequent part of the -- of this paragraph, and also in the next paragraph, it specifically says all the particular voltages that are applied, like V1, V2, V3 and V4, to the different word lines that are described, if I'm not mistaken, in Figure 1.

So the intrinsic disclosure of the '941 Patent in lines -- columns -- sorry, in column 3, lines 9 through 21, specifically say that a program operation means that you apply voltages WLx to the word line, you apply voltage V1, V2, V3, and V4 to the appropriate word lines that are described in lines 9 through 21 and also visually described in Figure 1.

So the intrinsic evidence is

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clearly from the -- from the '941 Patent unambiguous, and a person of ordinary skill in the art would not have any doubt reading these lines that I just told you.

Q So how many program operations are shown in Dong Figure 20?

MR. LOWRY: Object to form.

A Again, you know, Dong Figure 20 shows basically, you know, various -- you know, Dong Figure 20 is not basically a complete figure in terms of, for example, what is shown in, you know, column 3, lines 9 through 21 of the '941 Patent.

And since basically I'm talking about the '941 Patent, you know, talking about Dong is basically a different patent, and I haven't looked at Dong's Figure 20 in the context of -- you know, in the context of the -- of this -- you know, of this sort of disclosure of, you know, column 3, lines 9 through 21 of the '941 Patent.

I'm going to -- sorry, go ahead.

MR. JENSEN: I was going to say, why don't we take a short break. I think I'm --

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THE WITNESS: I was going to suggest just that because I'm losing my voice a little bit.

MR. JENSEN: Let's take a five-minute break.

THE WITNESS: Okay. Sounds good. Thank you.

(Whereupon, a brief recess was taken from 5:52 p.m. to 5:59 p.m.)

BY MR. JENSEN:

Q Dr. Khatri, did you speak with your counsel during the break?

A Yeah. I mean I just talked about how I'm doing and stuff. You know, he's basically asking me how I held up because my voice was kind of getting -- I mean I was talking about my voice and losing my voice. He was kind of just checking on me.

Q Did you talk about any potential redirect testimony?

A No.

MR. JENSEN: At this point, reserving all our rights, I'll pass the witness, Rich.

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THE WITNESS: Thank you.

EXAMINATION BY

MR. LOWRY:

Q Okay. Dr. Khatri, during cross-examination, you were asked about Exhibit 1087.

Do you remember that?

A I'm going to -- oh, that's the new exhibit. Yes, I remember that.

I'm going to open it. But that's the one with the very large patent -- the long patent, yeah.

Q Right.

Do you have it up, sir?

A Pardon?

I have it open.

Q Okay.

Before today's deposition, what was your familiarity with Exhibit 1087?

A So before today's deposition, as I mentioned, you know, I had not seen Exhibit 1087.

Q And what is your typical process when rendering an opinion on a patent figure during litigation?

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A Can you repeat that question?
Q Yes.
What is your typical process when rendering an opinion on a patent figure during litigation?
A You mean during a deposition or just during regular...
Q Before preparing --
A Oh --
Q Before providing an opinion like the one you provided in your declaration, what's your typical process?
A So my typical process is to be as thorough as possible. So in other words, I wouldn't just look at a figure or just one excerpt from, you know, a patent and then make conclusions out of it.
I would look at a figure -- I would look at all the figures because sometimes, you know, what is in a figure is informed by other figures.
Also, sometimes what is in a figure is informed by other, you know, intrinsic disclosures in the patent, in the specification, in the words that are used

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in the patent.

And then also they can be informed by what's in the claims. That's why it's -- you know, I mean if I'm just -- if you just put a figure in front of me, it's hard for me to give an opinion because -- especially for a patent like this, which, as I recall, had something like 115 pages and 300 paragraphs and then 50 claims and I think like 100 figures.

So it's -- you know, my process is thorough, and this, I simply did not have enough time to do a thorough job of evaluating this reference, 1087, that was put before me.

Q Okay. Let's turn to paragraph 129 of your declaration, please -- of your POR declaration, Exhibit 2028.

A Okay. Let me go there.

129?

Q Yes, sir.

Do you see the paragraph 129 spans pages 68 and 69?

A Correct, I see that.

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Q Okay. Do you see the sentence on line 3 of page 69 where it begins with "Moreover"?

A Let me read that really quick. Hold on.

Q Sure.

A Yeah, I see that sentence starting "Moreover."

Q Okay. And that sentence reads: "Moreover, the diagram above is not a representation of the physical layout of the memory, as a POSITA would readily understand."

Right?

A I see that, yes.

Q Now, are there circumstances in which a figure's appearance might not reflect the actual physical orientation of memory strings?

MR. JENSEN: Object to form and scope.

A You mean a circuit diagram figure, is that what you're referring to?

Q Yeah, or a figure in general, like the one we saw -- the ones we see in

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Exhibit 1087.

MR. JENSEN: Object to form.

A Yeah. I mean, there are, you know, sort of many times there would be a situation where figures like, you know, the figure in paragraph 129 would be just a depiction of a circuit.

You know, that's what I say, right, like it says in -- in paragraph 129, I say: "On the contrary, as evidenced by its use of circuit symbols for flash and NMOS transistors, it's a symbolic circuit diagram."

So these are circuit diagrams. They're not, you know, indicative of any orientation of transistors when they are physically realized. These are just circuit diagrams that the electrical engineers use to describe the components that I use in the design and how they're connected. There's no physicality to them.

Q Okay. Let's go back to Exhibit 1087. And just pull up Figures 1, 2 and 3.

A Okay. Let me go there real

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quick.

Exhibit 1087, and I'm looking at Figure 1 and Figure 2 and Figure 3.

Q Right.

Now, during the cross-examination by petitioner's counsel, you were asked about these three figures in Exhibit 1087, right?

A Yeah, I think I recall being asked about two of them, I think Figure 1 and 2. I don't recall being asked about Figure 3.

Q And during that line of questioning, were you able to provide a complete and fulsome answer to all of the questions asked by petitioner's counsel?

A No. And I think the reason for that is something I just described, because, you know, my process for, you know, evaluating a new patent, a different patent, and during any litigation days, you know, that I look at the patent, I look at the figures, I look at the text relating to the figures, I look at, you know, the other figures that -- you know, that might inform

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my understanding of a particular figure or that -- or the specification that might inform my understanding of the figure.

And in this particular reference that was put before me, you know, I think -- as I said, it was basically an impossible task, but, you know, in any reasonable length of time in a deposition because, you know, there are 300 paragraphs in the spec and 100-odd figures and 50 -- you know, and 50 claims in this.

So, you know, I was not able to form a reasonable opinion in the time that I was provided.

Q And do you recall your testimony regarding -- assuming for the sake of argument that Exhibit 1087 depicts vertically arranged NAND cells, describing what impact, if any, that may have on your opinion regarding grounds 1 and 2 of the petition?

MR. JENSEN: Objection to form.

A Yeah. I did -- I do recall, you know, beginning to say that and then being stopped.

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Q Okay. Are there any -- what additional information were you attempting to convey when you were stopped?

MR. JENSEN: Object to form. And scope.

A So what I was trying to say is that -- is the following, right?

You know, that -- that I was saying, look, A, I don't have enough time to make a determination of whether Exhibit 1087, you know, discloses vertically arranged, you know, word lines and such, you know. So that was the first thing.

And then I said, B, suppose -- you know, suppose it was true that Exhibit 1087 -- you know, which predates Dong -- suppose Exhibit 27 does disclose vertically arranged -- you know, vertically arranged word line arguendo. It's not that I'm saying it does, but I'm just saying hypothetically, let's assume it does, or arguendo, let's assume it does.

I was going to say -- this is at the point that I got cut off -- I was going

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to say that it would not alter my opinion in my declaration either way, and the reason for that is what I was about to provide, and which is what I'll provide now, if that's okay.

So the reason I want to -- the reason was, you know, Dong, in the petition, is used for grounds 1 and grounds 2.

Ground 1 is an anticipation ground.

Now, if I go to my declaration to see what anticipation requires -- I'm going to go really quick to the legal stuff, the -- I'm trying to remember where that is...

Okay. That's page 15.

So I'm going to see -- so anticipation, according to what I've been told by counsel, is -- let's see. I'll just read that part.

Give me one second, please.

Okay. I'm going to search for this.

Okay. There we go.

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Paragraph 29, it says: "I have been informed by Counsel that determining the anticipation of a patent claim requires a comparison of the properly construed claim language to prior art on an element-by-element basis. As it pertains to IPR proceedings, a claim is 'anticipated' if each and every element of the claim, as properly construed, has been disclosed by a single prior art reference."

So for ground 1, that single prior art reference is Dong.

And then it says: "Either expressly or inherently, and the claimed arrangement or combination of these elements must also be disclosed, either expressly or inherently, in that same prior art reference."

So Dong for claim 1 has the obligation of either expressly or inherently disclosing -- you know, when it says a throwaway sentence of, you know, it can also be used for 3D memory, it needs to expressly or inherently show that this 3D memory has word lines arranged in a -- you

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know, in a -- you know, in a manner that is vertical.

And Dong cannot do that.

First of all, you know, in terms of anticipation, you know, it only uses the word "three dimensional" once without any inherency about whether that's going to be three dimensional using stacked NAND -- stacked duty NAND approaches, which I described, or now with the introduction of this new arguendo hypothetical, you know, Exhibit 1087.

Now it's not even inherent as to which of these two possible NAND approaches would be useful because now inherency with this new patent that got introduced, assuming it's valid, now there's no inherency because, you know, it's not inherent that Dong would assume, you know, the 1087 Patent, you know, or whether Dong would inherently use the -- whether Dong would use the 2D stacked NAND.

And that's why since Dong for sure does not expressly disclose any of this because it just uses the word -- you

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know, the memory can be three dimensional. That's it.

So it's not an express disclosure. But now it's not even an inherent disclosure because if 1087 is prior art, then it's not inherently clear whether you would -- whether Dong would choose 1087 or a 2D array of -- a 2D array of -- yeah, I mean 2D stacked array of NAND like the stacked TFT or the 2D stack that we have.

So this does not, therefore, change my -- you know, my opinion or -- my -- my -- my opinion about, you know -- about the fact that ground 1 is invalid for Dong, you know, even assuming 1087 is valid art.

And then for the ground 2, they use -- the petitioner uses Dong but in an obviousness setting.

So in an obviousness setting, you know, in the year 2020, you know, what I've already described in my responses in my declaration -- and I don't know -- let me point you to the paragraphs about it.

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It's the section that says no obviousness. I'm trying to find it. It should be 90 -- page 90 or -- range.

Q I think it's at page 101.

A 101. Okay. Let me get there real quick.

So if we look at --

MR. JENSEN: I'm going to object to this whole answer as nonresponse and beyond the scope.

I did not ask Dr. Khatri about Dong's disclosure of three-dimensional or paragraph 95.

MR. LOWRY: Right. Your objection was noted when the question was asked.

BY MR. LOWRY:

Q Go ahead and finish your answer, Dr. Khatri.

A Thank you.

So, you know, in the -- in paragraphs 196 onwards, I discuss the situation of the obviousness ground for Dong, which is the second ground.

Now, in this obviousness ground,

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you know, because I'm looking at ground and it's an obviousness ground, I'm looking at in 2020 what would all -- what would be all the options of 3D NAND.

And in 2020, there were already options of 3D NAND in which the -- you know, the word lines were vertical. But -- you know, and I argued why, you know, the second ground of this -- of Dong is invalid because Dong -- you know, for among other reasons, Dong has a 2D NAND teaching, and therefore it doesn't apply to 3D NAND.

And so there's a -- you know, and also the disturb mechanisms for 2D and 3D are different, which is also something I describe.

And so this goes on up to paragraph I think 220.

So my discussion about the invalidity of ground -- I mean, or the inapplicability to ground 2 for Dong already assumes that we're in 2020 at this point, that, you know, there are techniques which have 3D NAND.

So if 1087 was arguendo a 3D --

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you know, a structure in which there's 3D NAND with vertical word lines, it would not make any change to my analysis of the no obviousness ground or the second ground of Dong, which is described starting paragraph 196.

So this is what I was going to try to say, that is arguendo, even if -- you know, if Exhibit 1087 was valid prior to Dong and it taught the appropriate -- you know, it taught the vertical arrangement of word lines, it would not change my argument either for ground 1 or for ground 2, and the fact that ground 1 and ground 2 are invalid would still hold.

Q Okay. Please turn to paragraph 66 of your POR declaration, Exhibit 2028.

A Paragraph 66, let me get there really quick.

Okay. I'm there in paragraph 66.

Q Okay. Can you read the first sentence of paragraph 66, please?

A Yes.

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It says: "To further scale NAND flash memory, a POSITA would understand that some initial 3D NAND designs were available at the time of Dong's filing date, May 7, 2007."

Q And when was Dong's filing date?

A Dong's filing date, as it says here, was May 7, 2007.

Q Okay. Please turn to paragraph 70 of your POR declaration, Exhibit 2028, on page 36.

A Okay. I'm there now.

Q Okay.

Do you see the first sentence of paragraph 70?

A Yes.

Q Can you read that sentence, please?

A Yes.

That sentence says: "The 2D NAND" Stacked -- sorry, "The 2D NAND-based Stacked and Multi-layer" -- it should say TFT -- "NAND designs are not the same as vertical 3D NAND as recited in the '941 Patent because the cells are not arranged

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vertically 'from bottom to top.'"

Q Okay. At the time you submitted your POR declaration, Exhibit 2028, what disclosures, if any, were you aware of as of Dong's filing date of May 2007 that described word lines vertically arranged from bottom to top as recited in the '941 Patent?

MR. JENSEN: Object to form.

A I didn't have any such -- I didn't have any certain references that I was aware of.

Q Let's go to paragraph 143 of your POR declaration, Exhibit 2028, please.

A Okay. I need to go there.

143?

Q Yes.

A Yeah.

Q Can you please read paragraph 143?

A Yes.

143 in my POR declaration reads: "Looking at the claimed phase 'a program operation' as recited in the '941 Patent claims, in my opinion, based on the

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intrinsic evidence, as well as my knowledge and experience, a POSITA would understand" that -- "would understand the '941 Patent claims use this phrase in its plain and ordinary sense, simply referring to 'an operation performed by applying a program voltage to a selected word line to program a'" memory -- "'to program a selected memory cell.'"

Q And sitting here today, what is your opinion regarding the claim construction of a program operation as recited in the '941 Patent?

MR. JENSEN: Object to form.

A So in my opinion, based on this paragraph, you know, the meaning of "a program operation" is what I have written in quotes at the end of this paragraph, paragraph 143, which is "an operation performed by applying a program voltage to a selected word line to program a selected memory cell."

MR. LOWRY: Thank you, Dr. Khatri.

No further questions.

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MR. JENSEN: Nothing further from me.

Thank you for your time, Dr. Khatri.

THE WITNESS: Thank you, Travis.

THE COURT REPORTER: And, Mr. Lowry, would you also like the transcript by Friday?

MR. LOWRY: Yes, by Friday.

THE COURT REPORTER: And would you like a copy of the rough draft?

MR. LOWRY: Yes.

(Time Noted: 6:20 p.m.)

* * *

_____

SUNIL KHATRI

Subscribed and sworn to
before me this day
of , 20__

_____
NOTARY PUBLIC

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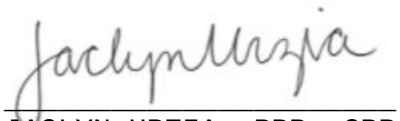
REPORTER CERTIFICATE

I, JACLYN URZIA, do hereby certify:

That said deposition was taken at the time and place herein named; and that the transcript is a true record of the testimony as reported by me, a disinterested person, and was thereafter transcribed.

I further certify that I am not interested in the outcome of the said action, nor connected with, nor related to any of the parties in said action, nor to their respective counsel.

IN WITNESS WHEREOF, I have hereunto set my hand this 30th day of January, 2026.



JACLYN URZIA, RPR, CRR

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Case Caption:

MICRON TECHNOLOGY, INC.
vs.
YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

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I declare under penalty of perjury that I have read the entire transcript of my deposition taken in the captioned matter or the same has been read to me, and the same is true and accurate, save and except for changes and/or corrections, if any, as indicated by me on the DEPOSITION ERRATA SHEET hereof, with the understanding that I offer these changes as if still under oath.

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Subscribed and sworn to on the ____ day of _____, 20__ before me,

_____
Notary Public,
in and for the State of _____

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