

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

**UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION**

YANGTZE MEMORY TECHNOLOGIES
COMPANY, LTD.,

Plaintiff,

v.

MICRON TECHNOLOGY, INC., and
MICRON CONSUMER PRODUCTS GROUP,
LLC.,

Defendants.

MICRON TECHNOLOGY, INC.,

Counterclaim Plaintiff,

v.

YANGTZE MEMORY TECHNOLOGIES
COMPANY, LTD., and YANGTZE MEMORY
TECHNOLOGIES, INC.,

Counterclaim Defendants.

Case No.: 3:23-cv-05792-RFL

**DECLARATION OF DR. SUNIL P.
KHATRI, PH.D**

1 I, Sunil P. Khatri, declare as follows:

2 1. I have been retained on behalf of YMTC, and its counsel, Latham & Watkins,
3 LLP, to serve as a technical expert and provide expert opinions relating to U.S. Patent No.
4 11,568,941 ("Asserted Patent"). I am personally knowledgeable about the matters stated
5 herein and am competent to make this declaration.
6

7 2. I have been asked to provide testimony and my opinions regarding certain
8 disputed claim construction issues with respect to the '941 Patent.

9 3. I am being compensated for my time at my standard hourly rate of \$800 per
10 hour.

11 4. This declaration, including the exhibits hereto and cited materials, identifies
12 my opinions to date, although I may provide further testimony and opinions if asked to testify
13 in court or at a deposition. I also reserve the right to supplement or amend my opinions, as
14 well as the bases for those opinions, if I receive additional relevant information or to respond
15 to opinions offered by other experts in this case. I may rely on demonstrative exhibits,
16 including pictures, figures, and drawings that appear in this declaration and the referenced
17 exhibits and materials.
18

19 **I. BACKGROUND AND QUALIFICATIONS**
20

21 5. I have over thirty-five years of experience with electronics, electrical
22 engineering, and computer engineering. A copy of my latest curriculum vitae (CV) is
23 attached hereto as Appendix A and provides further details regarding my background and
24 qualifications.

25 6. During my career, I have acquired extensive knowledge and experience with
26 VLSI circuits, computer architecture, testing, computer-aided design (CAD) algorithms and
27 algorithm acceleration, logic synthesis, semiconductor memory, redundancy, synchronous
28

1 and asynchronous circuits, and related software and hardware topics. Most relevant to the
2 Asserted Patent my technical expertise includes extensive work with semiconductor memory
3 devices such as DRAM, SRAM and flash. My work with semiconductor memory devices
4 has included work on 3D integration and novel ring-based memory architectures, power and
5 speed tradeoffs using selective body bias, architectures and circuit approaches for processing-
6 in-memory, radiation hardening analysis for memories, the use of flash transistors for
7 designing logic circuits (such as ternary Content-addressable Memories (CAMs), Field
8 Programmable Gate Arrays (FPGAs), and traditional binary-valued as well as ternary-valued
9 digital logic, secure logic circuits, analog circuits like Finite Impulse Response (FIR) filters,
10 Discrete Fourier Transform (DFT) circuits, and in-memory mixed-signal computing
11 architectures like Convolutional Neural Networks (CNNs)), large language models (LLMs)
12 and clocking and source-synchronous design. I recently was awarded a research grant by the
13 Air Force Research Laboratory (AFRL) in Rome, NY, to conduct research in secure digital
14 circuits using flash-based digital design approaches.
15

16
17 7. Another recent research grant from the National Science Foundation (NSF)
18 will fund research on the use of flash transistors for general purpose mixed-signal arithmetic.
19 Additionally, I have led-authored a book chapter on the use of flash transistors in novel Very
20 Large Scale Integrated (VLSI) design applications. My MS thesis involved designing a
21 memory interface for a multi-threaded Reduced Instruction Set Computing (RISC)
22 microprocessor.
23

24 8. The following describes some of my relevant experience. I earned my
25 Bachelor of Science in Electrical Engineering in 1987 from the Indian Institute of
26 Technology, Kanpur, India. After graduating with my B.S. degree, I was a candidate for a
27 Master of Science degree in Electrical and Computer Engineering at the University of Texas
28

1 from 1987–89. At the University of Texas, I held the Microelectronics and Computer
2 Development (MCD) Fellowship from 1987–89. I also conducted my M.S. research and
3 wrote my thesis on the design of the METRIC memory interface and memory system.
4 METRIC was one of the first super-scalar processors that was developed in the world. I
5 earned an M.S. degree in 1989 from the University of Texas, Austin.

6
7 9. After leaving the University of Texas, I worked at Motorola Inc. from 1989–
8 93 as a design engineer for the MC88110 reduced instruction set computing (RISC)
9 microprocessor team. My duties included the design of digital and analog circuitry, test logic
10 and circuits, JTAG boundary scan design, input/output driver design, and clock phase-locked
11 loop (PLL) logic. During my time at Motorola, I was independently responsible for the design
12 of the factory test controller of the MC88110 microprocessor. I performed all attendant tasks
13 in a “vertical” VLSI design methodology, which included high-level modeling, circuit and
14 layout design and verification, as well as global and detailed routing. I also helped in the
15 design of the Translation Lookaside Buffer (TLB) unit, which included a static random-access
16 memory (SRAM) block.

17
18 10. In 1999, I earned a Doctor of Philosophy degree in Electrical Engineering and
19 Computer Sciences from the University of California, Berkeley. While at Berkeley, I held
20 the California Microelectronics (MICRO) Fellowship in 1993.

21
22 11. I joined the faculty at the University of Colorado, Boulder, in 2000 as an
23 Assistant Professor of Electrical and Computer Engineering. At the University of Colorado
24 my research focused on VLSI logic design automation, VLSI layout design automation, and
25 VLSI design methodologies to address Deep Submicron (DSM) issues such as crosstalk and
26 power.

27
28 12. I joined the faculty at Texas A&M University in 2004 as an Assistant Professor

1 in Electrical and Computer Engineering. In 2010 I was promoted to Associate Professor in
2 Electrical and Computer Engineering. In 2015, I was promoted to full Professor in Electrical
3 and Computer Engineering. My research focuses on three primary areas: the first is computer
4 systems, including computer architecture from the circuits up, and algorithm acceleration
5 using GPUs, FPGAs and custom ICs. The second is logic and its applications, while the third
6 area consists of interdisciplinary extensions of the first two. Some specific recent research
7 topics include circuit design using floating gate (flash) devices, wireless power delivery and
8 battery-less electronic systems, machine learning architectures, secure computing approached
9 from both a hardware and software perspective, a formal framework for designing and
10 verifying cryptographic hash functions, and extreme high-speed serial interfaces for Artificial
11 Intelligence / Machine Learning (AI/ML) systems such as those used in Large Language
12 Models (LLMs) like ChatGPT. One of my new focus areas is intelligent and secure
13 computing viewed from the hardware (circuit) as well as the software levels. I have
14 conducted research on tamper-proof memory techniques, as well as multi-row read
15 architectures for SRAM, DRAM and flash memory arrays.

16
17
18 13. At Texas A&M I teach classes that cover memories extensively, featuring
19 thorough discussion of sense amplifiers, row and column decoders, and different types of
20 memory circuits. For example, in Electrical and Computer Engineering (ECEN) 752
21 “Advances in VLSI Circuit Design,” a graduate level course, I cover all aspects of VLSI
22 design, including memory design for various types of memories. In this course, (and also in
23 ECEN 449/749 “Microprocessor System Design,”), I cover memories, including flash
24 memories, the design of flash memory cells, the organization of memories into multiple
25 banks, and the division of data across multiple banks of memory, as well as other design
26 techniques that can be used to optimize and manage memories. The ECEN 449/749 course is
27
28

1 attended by both undergraduate (ECEN 449) and graduate (ECEN 749) students. In ECEN
2 454 “Digital Circuit Design,” a senior undergraduate course, I cover circuit design techniques
3 for memory in detail. The Ph.D. thesis dissertation topic for 3 of my current Ph.D. students
4 covers the use of flash memory transistors for analog and digital applications. The Ph.D.
5 thesis of one of my recent doctoral students dealt with the use of flash transistors to design
6 logic circuits. The research of a recent M.S. student entailed a new ring-based source
7 synchronous architecture for 3D DRAM technologies, which has been published at a
8 conference and in a journal and is being submitted for dissemination as a research monograph.
9 In the past, I have conducted research into new topologies for efficient memory redundancy
10 as part of a course project for my graduate course.
11

12 14. Since 2000, I have earned at least 24 research contracts from funders including
13 Intel, the National Science Foundation, the National Security Agency, Altera Corporation,
14 the National Center for Atmospheric Research, National Semiconductor Corporation, and
15 several private sources. The total amount for these research grants is at least \$17.53 million,
16 of which my portion is at least \$2.85 million.
17

18 15. I have a total of over 289 peer-reviewed publications. Among these papers,
19 five received a best paper award, while seven others received best paper nominations
20 (including one journal best paper nomination). An additional six journal papers and three
21 conference paper are currently undergoing peer review. I have co-authored nine research
22 monographs, one edited research monograph, and four book chapters. Additionally, I have
23 seven awarded U.S. Patents (two of which were filed during my tenure at Texas A&M), two
24 filed provisional U.S. Patents, and another U.S. Patent which is currently under review and
25 was also submitted during my tenure at Texas A&M. I have co-authored one invited journal
26 paper and 13 invited conference or workshop papers (including one from Design Automation
27
28

1 Conference (DAC) and one from Allerton). Moreover, I was invited to serve as a panelist at
2 a conference seven times and have presented four conference tutorials. I received the
3 “Outstanding Professor Award” in the ECE Department at Texas A&M University in 2007
4 and also in 2020. In 2009 and in 2019, I received a university-level and a college-level
5 teaching award respectively, at Texas A&M. My H-index is 36 (per Google Scholar).

6
7 16. Since 2003, I have published numerous research monographs, journal papers,
8 and conference papers on flash transistors and memory systems, as detailed in my CV
9 attached in Appendix A. A few papers on relevant subject areas authored or co-authored by
10 me include:

- 11 • *"Flash - A "Forgotten" Technology in VLSI Design"*. Khatri, Vrudhula, Abusultan,
12 Bharathi, Chu, Lee, Scott, Singh, Wagle. Appears "Frontiers of Quality Electronic
13 Design (QED)". Springer publishers, Sept 2022. Pages 67-136. Ali Iranmanesh, Ed.
14 ISBN: 978-3-031-16344-9;
- 15 • *"Flash – An Overlooked Technology in VLSI Design"*, Khatri, Vrudhula. Monday
16 Tutorial to be presented at the ACM/CEDA Design Automation Conference
17 (DAC), San Francisco, CA, June 2024;
- 18 • *"A Mixed-Signal Quantized Neural Network Accelerator Using Flash Transistors"*,
19 Scott, Lee, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I: Regular
20 Papers, vol. 71, no. 3, pp. 1025-1038, March 2024;
- 21 • *"An ASIC Accelerator for QNN With Variable Precision and Tunable Energy-*
22 *Efficiency"*, Wagle, Singh, Khatri Vrudhula. IEEE Transactions on Computer-
23 Aided Design of Integrated Circuits and Systems, Jan 2024;
- 24 • *"A Digital Low Dropout (LDO) Voltage Regulator Using Pseudoflash Transistors"*,
25 Lee, Khatri. IEEE Transactions on Very Large Scale Integration (VLSI) Systems,
26 vol. 31, no. 12, pp. 1960-1969, Dec. 2023;
- 27 • *"A Novel ASIC Design Flow using Weight-tunable Binary Neurons as Standard*
28

1 *Cells*", Wagle, Singh, Khatri, Vrudhula. IEEE Transactions on Circuits and
2 Systems I (Regular Papers), 69(7): 2968-2981 (Sept 2022);

3 • *"CIDAN-XE: Computing in DRAM with Artificial Neurons"*, Singh, Wagle, Khatri,
4 Vrudhula. Frontiers in Electronics, section Integrated Circuits and VLSI. vol. 3,
5 Feb 2022;

6 • *"An Extremely Low-Voltage Floating Gate Artificial Neuron"*, Scott, Khatri. 2023
7 IEEE International Conference on Circuits and Systems (ISCAS), May 21-25,
8 2023. Monterey, CA;

9 • *"A Novel Pseudo-Flash Based Digital Low Dropout (LDO) Voltage Regulator"*,
10 Lee, Khatri, Vrudhula. 2023 International Symposium on Quality Electronic
11 Design (ISQED), April 5-7 2023. San Francisco, CA;

12 • *"A Flash-based Digital to Analog Converter for Low Power Applications"*, Scott,
13 Khatri. IEEE 40th International Conference on Computer Design (ICCD), October
14 2022. Lake Tahoe, CA. pp 1-8;

15 • *"A Flash-based Current-mode IC to Realize Quantized Neural Networks"*, Scott,
16 Lee, Khatri, Vrudhula. IEEE Design Automation and Test in Europe Conference,
17 Mar 2022, Antwerp, Belgium. pp 1029-1034;

18 • *"CIDAN: Computing in DRAM with Artificial Neurons"*, Singh, Wagle, Vrudhula,
19 Khatri. 39th IEEE International Conference on Computer Design (ICCD) 2021, pp
20 349-356, Oct 2021, virtual conference;

21 • *"A Statistical Methodology for Post-Fabrication Weight Tuning in a Binary
22 Perceptron"*, Azari, Wagle, Khatri, Vrudhula. IEEE 21st International Symposium
23 on Quality Electronic Design (ISQED) 2020. Mar 25-26, 2020, Santa Clara, CA.
24 pp 141-148;

25 • *"Threshold Logic in a Flash"*, Wagle, Singh, Yang, Khatri, Vrudhula. 37th IEEE
26 International Conference on Computer Design (ICCD), 2019. Abu Dhabi, UAE, pp
27 550-558. Nov 17-20, 2019;

28 • Fast, Ring-based Design of 3D Stacked DRAM, IEEE Transactions on Very Large

- Scale Integrated Circuits (TVLSI), IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Vol 27 number 8, Aug 2019. pp 1731-1741.;
- Fast, Ring-Based Design of 3D Stacked DRAM, IEEE International Conference on Computer Design 2017: pp 665-672;
 - Selective Forward Body Bias for High Speed and Low Power SRAMs, Journal of Low Power Electronics, Vol. 5, No. 2, Aug. 2009, pp. 185-95;
 - Low Power and High Performance SRAM Design using Bank-based Selective Forward Body Bias, IEEE/ACM Great Lakes Symposium on VLSI, May 10-12, 2009, Boston, MA, pp. 441-44;
 - Modeling Dynamic Stability of SRAMs in the Presence of Single Event Upsets (SEUs), IEEE International Symposium on Circuits and Systems, May 18-21, 2008, Seattle, WA, pp. 1788-91;
 - "Design of a Flash-based Circuit for Multi-valued Logic", Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI) 2017, pp 41-46, May 10-12, 2017. Banff, Canada.
 - "SAT-Based Optimization for Flash-Based Digital Designs", IEEE/ACM Design Automation Conference (DAC), Jun 18-22 2017, Austin, TX.
 - "A Flash-based Digital Circuit Design Flow", IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2016, Austin, TX, Nov 2016.
 - "Implementing low power digital circuits using flash devices", 2016 IEEE 34th International Conference on Computer Design (ICCD), pp 109-116, Oct 3-5, 2016, Phoenix, AZ.
 - "Exploring Flash Devices to Implement Digital Circuits", IEEE/ACM Design Automation Conference (DAC), June 2016, Austin, TX.
 - FTCAM: An Area-efficient Flash-based Ternary CAM Design, IEEE Transactions on Computers, Vol. 65, No. 8, Aug. 2016, pp. 2652-58;
 - An Area-efficient Ternary CAM Design Using Floating Gate Transistors, IEEE International Conference on Computer Design, Oct. 19-22, 2014, Seoul, S. Kor.,

1 pp. 55-60; and

- 2 • A Fast Ternary CAM Design for IP Networking Applications, International
3 Conference on Computer Communications and Networks, October 22, 2003,
4 Dallas, TX, pp. 434-39 (awarded best paper).

5 17. In addition to my work on the papers listed above, I have also served as an
6 editor for IEEE Transactions on Computers, ACM Transactions on Design Automation of
7 Electronic Systems, and MDPI Journal of Electronics.

8 18. I have served as EDA Track Co-Chair for ICECS 2014, Panel Chair for
9 TexasWISE 2014, Track Co-Chair (VLSI Systems, Applications and Computer Aided Design
10 track) for ICECS 2013, Poster Session Chair for TexasWISE 2013, Advisory Committee for
11 HotPI 2013, Panel Session Chair for SLiP 2013, Track Chair (Logic track) for ICCAD 2009-
12 10, 2015-17, Track Chair (logic track) for DAC 2016-17, General Chair for IWLS 2009,
13 Technical Program Chair for IWLS 2008, Track Co-Chair, Computer Aided Network Design
14 (CANDE) Track, for ISCAS 2008-10, Track Co-Chair, Test and Methodologies Track, for
15 ICCD 2007, Panel Chair for ITSW 2009, Publicity Co-Chair for GLS-VLSI 2009, and as a
16 member of the TPC for several conferences.

19 **II. LEGAL PRINCIPLES**

20 19. I am not an attorney. Counsel for YMTC provided me with the legal principles
21 pertaining to claim construction.

22 20. I understand that claims must be construed in light of and consistent with the
23 intrinsic evidence. In this context, intrinsic evidence includes the claims themselves, the
24 written disclosure in the specification, and the patent's prosecution history, including prior
25 art that was considered by the United States Patent and Trademark Office ("USPTO"). I
26 understand that extrinsic evidence may also be considered when construing claims and may
27 include, for example, technical dictionaries, technical publications and books, treatises, and
28

1 expert testimony.

2 21. I understand that claim terms are assigned their ordinary and customary
3 meaning to a person of ordinary skill in the art (“POSA”), unless the specification or
4 prosecution history provides a special, different meaning. I further understand that a POSA
5 is deemed to read each claim term in the context of the entire patent, including the
6 specification, which is always highly relevant and the single best guide to the meaning of a
7 disputed term.
8

9 22. I further understand that the relevant timeframe for assessing the ’941 Patent
10 for purposes of this declaration is around February 10, 2020, the earliest priority date. If I
11 refer to the time of the invention in this declaration, I am referring to this timeframe.
12

13 **III. THE LEVEL OF ORDINARY SKILL IN THE ART**

14 23. I have been informed and understand that the level of ordinary skill in the
15 relevant art at the time of the invention is relevant to inquiries such as the meaning of claim
16 terms and the meaning of disclosures found in the prior art.

17 24. I understand that the factors that may be considered in determining the level
18 of skill of POSA include, but are not limited to, (1) the educational level of the inventor; (2)
19 type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity
20 with which innovations are made; (5) sophistication of the technology; and (6) the educational
21 level of active workers in the field.
22

23 25. For purposes of this declaration, a POSA in the field of the ’941 Patent would
24 have had a bachelor’s degree in electrical engineering or a similar discipline, along with 2-3
25 years of professional experience working with (*e.g.*, researching, designing, or teaching)
26 NAND flash memory devices (including issues relating to the operation, *e.g.*, programming,
27 of said devices), or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced
28

1 degree may replace some of the professional experience).

2 26. In my opinion, this POSA would have been aware of and generally
3 knowledgeable about NAND flash memory's structure and fabrication, its component parts,
4 how it operates, and how it is controlled.

5 27. In view of my educational background and experience with semiconductor
6 memory, including NAND memory, I was a person of at least ordinary level of skill in the art
7 as the time of invention of the '941 Patent. In forming my opinion, I have drawn on my
8 academic background and professional experiences. My opinions herein, however, were
9 formed taking into account the perspective of a POSA.
10

11 **IV. MATERIALS CONSIDERED**

12 28. My opinions in this declaration are based on my own personal knowledge and
13 experience in the field of the Asserted Patent, its file history, and other materials cited in
14 this Declaration.
15

16 **V. CLAIM CONSTRUCTION**

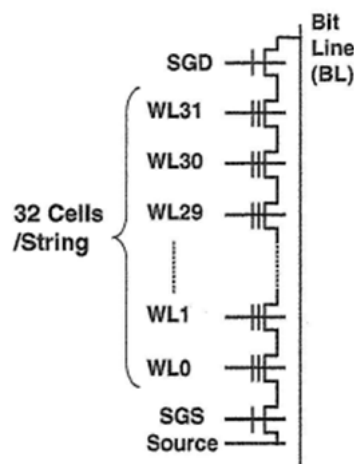
17 **A. "from bottom to top" ('941 Patent)**

18 29. The term "from bottom to top" has no special meaning in the semiconductor
19 manufacturing context or in the context of the Asserted Patent, and simply means from lowest
20 to highest. YMTC-MICRON-PA_0010352, page 83, 752. The '941 Patent or its file history
21 does not provide any special definition to the phrase "from bottom to top" or disclaim its
22 ordinary meaning. Thus, the '941 Patent claim elements that recite word lines "from bottom
23 to top" simply refer to going from a lower word line to a higher word line.
24

25 30. Specifically, the claims refer to sets of word lines "from bottom to top"—e.g.,
26 "an (m+1)th word line to an nth word line *from bottom to top*" (claims 1, 7, and 11), "a first
27 word line to a kth word line *from bottom to top*" (claims 2, 5, and 12), and "a (k+1)th word
28

line to an mth word line *from bottom to top*” (claim 11). In the three-dimensional NAND devices that the ’941 Patent is directed to, word lines are arranged vertically, one on top of another, as shown in Figures 1 to 11 of the ’941 Patent. ’941 Patent at 1:26-41 (“A three-dimensional structure of a memory can include a plurality of layers so as to store more data on a same area.”). The ’941 Patent also refers to “portions” that are “above” or “below” each other, where each “portion” consists of “word lines.” *Id.* at Abst.; 1:45-54; 2:1-12; 2:63-3:3; 3:46-52; 5:4-14, 5:16-19. The claims themselves confirm this vertical word line arrangement, reciting portions of word lines “formed above” other portions (cls. 3, 5, 7, 13) and “dummy word line[s]” formed “above” and “below” other portions (cls. 4, 10, 14).

31. A POSA would be familiar with circuit diagrams that are often used to represent word lines in a memory. For example, the below illustration represents a NAND flash memory consisting of several word lines (“WL0” to “WL31”), and select transistors “SGD” and “SGS” to respectively isolate the bit line (connected at the drain) and the source line (connected at the source):



Aritome, NAND Flash Memory Technologies (2016) (MYM0027804 - MYM0028234) at 18-19.

32. A POSA would, however, understand that while circuit diagrams are helpful

1 to show the circuit and electrical connectivity, they do not necessarily reflect the actual,
2 physical arrangement of components (in this case, the word lines) on a chip. For example,
3 circuit diagrams as shown above may be used to describe traditional two-dimensional
4 (“planar”) NAND flash memory, where word lines are actually arranged horizontally in a
5 planar structure, such that the word lines are arranged in a row from left to right (instead of
6 from bottom to top). Aritome, NAND Flash Memory Technologies (2016) (MYM0027804
7 - MYM0028234) at 18-19. In this planar structure, word lines are not physically arranged
8 “from bottom to top” because they are not arranged in a vertical direction at all. Aritome,
9 NAND Flash Memory Technologies (2016) (MYM0027804 - MYM0028234) at 18-19 (*see*
10 *also* Fig. 2.3, showing word lines arranged from left to right in a planar NAND flash memory).
11 They are physically arranged from left to right.
12

13
14 33. In the type of three-dimensional NAND flash memory that the '941 Patent is
15 directed to, word lines *are* arranged vertically, one on top of the other. '941 Patent at Abst.,
16 1:26-41, 1:45-67, 2:1-11, 2:13-27, 2:63-3:3, 3:22-30, 3:42-52, 4:6-28, 4:29-36, 4:62-67, 5:1-
17 14, 5:15-37, 5:42-50, 5:51-55, 5:56-62, 6:55-7:9, 7:23-34, 7:39-46, 8:15-40, Figs. 1-13. That
18 is why the claims refer to word lines “from the bottom to the top” because, unlike planar 2D
19 NAND flash memories, the word lines in the 3D NAND flash memories that are the subject
20 of the '941 Patent are arranged from a lowest point (at the bottom) to a highest point (at the
21 top). A textbook example of this type of 3D NAND device is shown below, where the
22 “Control Gates” (in red) are the word lines going “from bottom to top”, as taught by the '941
23 Patent. Micheloni, Inside Solid State Drives, 2nd Edition (2018) (MYM0034141 -
24 MYM0034635) at 106-108 (*see also* Figs. 5.2, 5.3, 5.4).
25
26
27
28

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

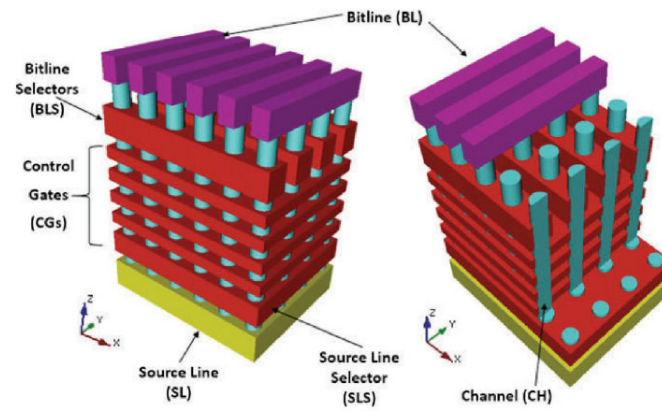


Fig. 5.3 BiCS architecture

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

I declare under penalty of perjury that the foregoing is true and correct.
Executed this 31th day of January 2025, at College Station, Texas.

/s/ 
Sunil P. Khatri