

Novel Ultra High Density Flash Memory with A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell

Tetsuo Endoh¹, Kazushi Kinoshita², Takuji Tanigami¹, Yoshihisa Wada², Kota Sato², Kazuya Yamada²,
Takashi Yokoyama¹, Noboru Takeuchi¹, Kenichi Tanaka², Nobuyoshi Awaya², Keizou Sakiyama²
and Fujio Masuoka¹

1) The Research Institute of Electrical Communication, TOHOKU University 2-1-1 Katahira, Aoba-ku,
Sendai 980-8577, Japan

Phone/FAX: +81-22-217-5479 E-mail: endoh@masuoka.riec.tohoku.ac.jp

2) Process Development Center, Sharp Corporation, 1 Asahi, Daimon-cho, Fukuyama, Hiroshima 721-8522, Japan

Abstract

In order to overcome the limitation of cell area of $4F^2$ per bit in conventional NAND Flash Memory cells, Stacked-Surrounding Gate Transistor (S-SGT) structured cell is proposed. The new structured cell achieves cell area of $4F^2/N$ per bit, where N is the number of stacked memory cells in one silicon pillar, without using multi bit per memory cell technology. The S-SGT structured cell consisting of 2 stacked memory cells in one silicon pillar achieves cell area per bit less than 50% of the smallest reported NAND structured cell. The novel S-SGT structured cells are fabricated by vertical self-aligned processes using a $0.2\mu\text{m}$ design rule. The S-SGT structured cell can be programmed and erased by uniform injection and uniform emission of Fowler-Nordheim (F-N) tunneling electrons over the whole channel area of the memory cell, respectively, the same as conventional NAND structured cell. This high performance S-SGT structured cell is applicable to high-density nonvolatile memories as large as 16G / 64G bit Flash Memory or beyond.

Introduction

With the development of ULSI technologies, bit density of nonvolatile memories, especially Flash Memory, is undergoing revolutionary growth. To realize over Gigabit density memories, current Flash Memories have been simply shrunk by introducing self-aligned floating gate structure, self-aligned STI structure and scaled dielectric. However, the current Flash Memory cell is now beginning to reach limitation in scaling law, because it is hard to reduce memory cell area per bit itself, spacing between neighboring memory cells, spacing between gate electrode and drain contact hole, contact hole size and source line. Therefore, NAND structured Flash Memories had been proposed [1]. However, the conventional Flash Memory have been based on the two dimensional memory array

architecture. This two dimensional memory array architecture doesn't use three dimensional space sufficiently. Moreover, these conventional Flash memories have the limitation of cell area of $4F^2$ per bit, where F is a minimum feature size.

Therefore, Stacked-Surrounding Gate Transistor (S-SGT) structured cell is proposed, in order to overcome the limitation of cell area of $4F^2$ per bit in conventional NAND Flash Memory cells. The S-SGT structured cell consisting of 2 stacked memory cells in one silicon pillar described in this paper achieves cell area per bit less than 50% of the smallest reported NAND structured cell [2]. The novel S-SGT structured cells are fabricated by vertical self-aligned processes using a $0.2\mu\text{m}$ design rule. The S-SGT structured cell can be programmed and erased by uniform injection and uniform emission of Fowler-Nordheim (F-N) tunneling electrons over the whole channel area of the memory cell, respectively, the same as conventional NAND structured cell.

This paper describes the cell structure, fabrication process and operation principle of new S-SGT structured cell.

Cell Structure

The structure of the proposed cell arranges bit line contact, first select gate, 2 SGT type memory cells, second select gate and source line in series vertically in one silicon pillar, as shown in figure 1(A)(B)(C). The SGT type memory cell is structured that floating gate and control gate surround the silicon pillar [3]. All devices for the proposed cell are vertically stacked in one silicon pillar, therefore, the S-SGT structured cell does not need additional area such as bit line contact, 2 select gates and source line, while conventional NAND structured cell [2] needs this additional area.

The new structured cell achieves cell area of $4F^2/N$ per bit, where N is the number of stacked memory cells in one

silicon pillar, without using multi bit per memory cell technology. The S-SGT structured cell consisting of 2 stacked memory cells occupies only an area of $4F^2$ and achieves cell area of $2F^2$ per bit as shown in figure 1(C). Otherwise, conventional NAND structured cell requires cell area of $8F^2$ per bit as shown in figure 1(D). As shown in figure 1(E), the equivalent circuit of S-SGT structured cell is the same as that of conventional NAND structured cell. Figure 2 shows ratio of occupied area per bit as function of number of stacked memory cells in one silicon pillar in comparison with the smallest reported cell area per bit of conventional NAND structured cell. As the number (N) of stacked memory cells in one silicon pillar increases, the S-SGT structured cell can reduce to cell area per bit in proportion to $1/N$. As a result, the S-SGT structured cell can realize a drastically smaller cell area per bit than the smallest reported NAND structured cell.

Fabrication Process

The S-SGT structured cell consisting of 2 stacked memory cells is fabricated using a $0.2\mu\text{m}$ process as shown in Figure 3. The fabrication sequence for the proposed cell is shown in Figure 4. A sidewall mask is formed after first Si etching as shown in figure 4(A). Then, the first memory cell region is formed by the second Si etching. Then a sidewall mask for the third Si etching is formed as shown in figure 4(B). This sequence of Si etching after forming a sidewall mask is additionally two times repeated for forming a second memory cell region and a second select transistor region. After removing all sidewall masks, the gate poly-Si is deposited following gate oxidation. Two select gates and two floating gates are vertically isolated from each other at the steps of the silicon pillar by vertical self-aligned processes with an etch back process for poly-Si as shown in figure 4(C). Phosphorus (P^+) is implanted to form a source and drain. After forming inter-poly-Si insulator, which is composite layer of $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ (ONO), second poly-Si is deposited and etched back similar to the first poly-Si etching. Control gates are vertically isolated from each other at the steps of the silicon pillar as shown in figure 4(D). Then, bit lines, select gates and word lines are formed. A final cross-sectional view of the S-SGT structured cell is shown in figure 4(E). The equivalent oxide thickness of tunnel oxide and ONO are 9.8nm and 16nm, respectively.

Measured Results

Figure 5 shows the programming and erasing characteristics of the fabricated cells. Programming and erasing can be accomplished by uniform F-N tunneling. Figure 6 shows the threshold voltage shifts of the selected memory cell and the unselected one as a function of programming time with all memory cells in the S-SGT structured cell in erased state. The selected memory cell is

programmed and the unselected memory cell is not programmed. Drain current versus control gate voltage characteristics after erasing and after programming are shown in figure 7. In read operation, 0V is applied to the control gate of the selected memory cell and 3.3V is applied to the control gate of the other memory cell and select gates. A drain current flows when the selected memory cell is in erased state, while the drain current does not flow at all when the selected memory cell is in programmed state.

Conclusions

A novel Flash Memory with S-SGT structured cell has been developed. The proposed cell achieves cell area of $4F^2/N$ per bit without multi bit per memory cell technology. The fabricated novel S-SGT structured cell consisting of 2 stacked memory cells achieves a smaller cell area per bit less than 50% of the conventional NAND structured cell.

The novel S-SGT structured cells are fabricated by vertical self-aligned processes using a $0.2\mu\text{m}$ design rule. The S-SGT structured cell can be programmed and erased by uniform injection and uniform emission of Fowler-Nordheim (F-N) tunneling electrons over the whole channel area of the memory cell, respectively, the same as conventional NAND structured cell.

The S-SGT structured cell can be successfully applied to 16G / 64G bit Flash Memory or beyond.

Acknowledgment

The author would like to thank Terumasa Yoneda for his support, encouragement and helpful discussion on this work. The author would like to thank Shigeru Kato, Masaki Shigematsu and Sakae Wada for his helpful discussion on this work.

Reference

- [1] Fujio Masuoka, Masaki Momodomi, Yoshihisa Iwata and Riichiro Shirota, "NEW ULTRA HIGH DENSITY EPROM AND FLASH EEPROM WITH NAND STRUCTURE CELL", Technical Digest, IEDM pp.552-555,1987.
- [2] Akira Goda, Akira Goda, Wakako Moriyama, Hiroaki Hazama, Hirohisa Iizuka, Kazuhiro Shimizu, Seiichi Aritome, and Riichiro Shirota et al., "A Novel Surface-Oxidized Barrier-SiN Cell Technology to Improve Endurance and Read-Disturb Characteristics for Gigabit NAND Flash Memories Technical Digest, IEDM pp.772-775,2000.
- [3] T. Endoh, M. Hioki, H. Sakuraba, M. Lenski, and F. Masuoka, "Floating Channel Type SGT Flash Memory", Meeting Abstracts The 1999 Joint International Meeting (196th Meeting of The Electrochemical Society, 1999 Fall Meeting of The Electrochemical Society of Japan with technical cosponsorship of The Japan Society of Applied Physics), Vol.99-2, Abstract No.1323, Hawaii, October 17 - 22, 1999..

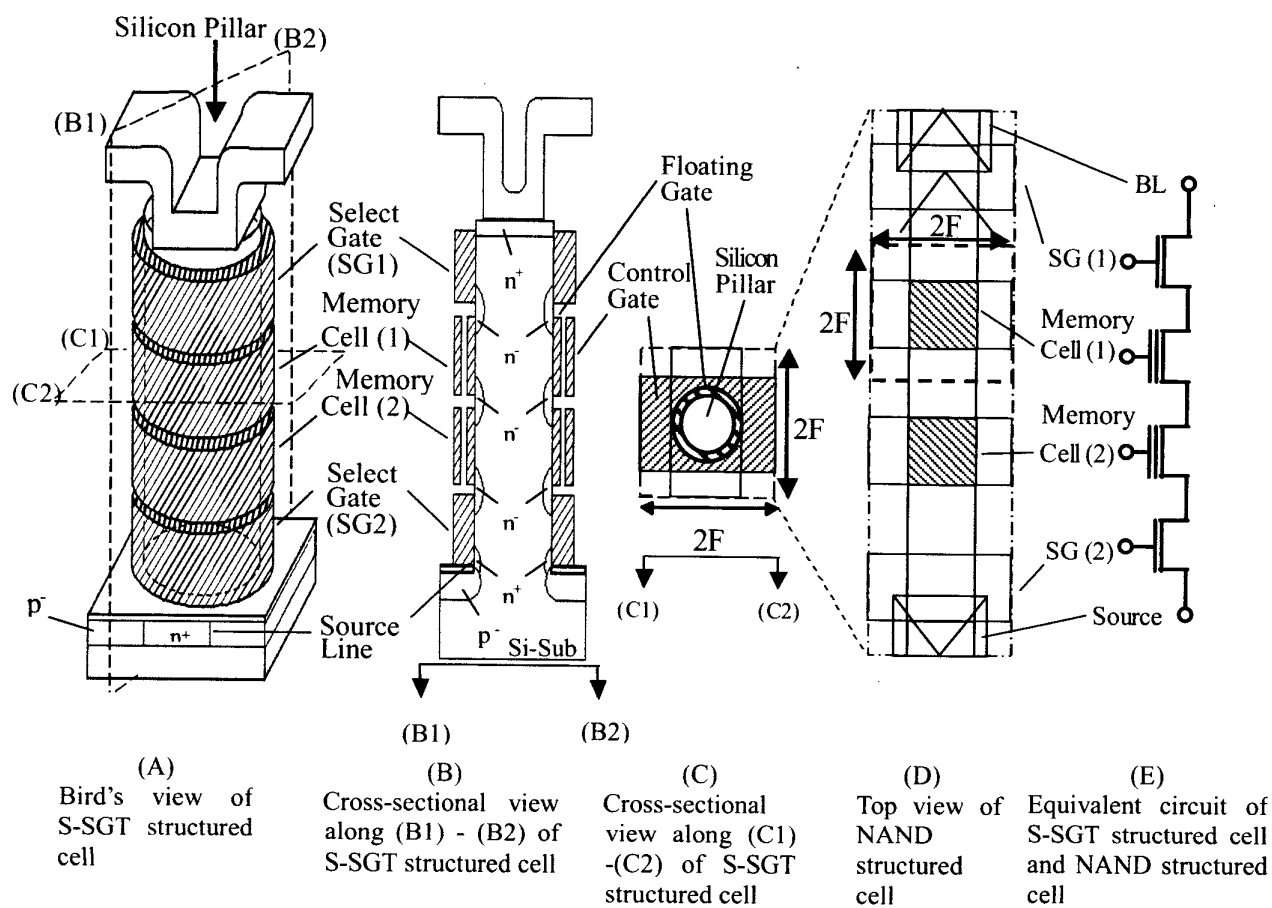


Fig. 1 Concept of S-SGT structured cell.

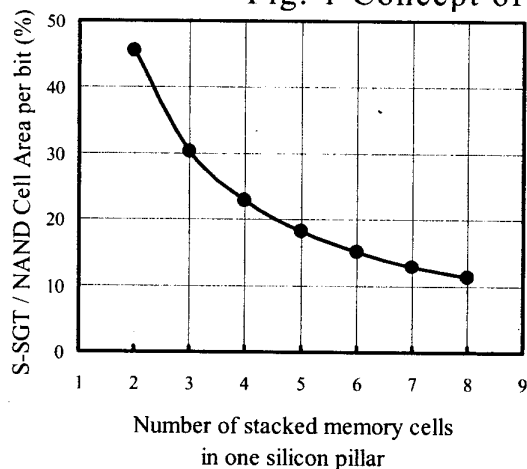


Fig. 2 Ratio of occupied area per bit as function of number of stacked memory cells in one silicon pillar in comparison with the smallest reported cell area per bit of conventional NAND structured cell.

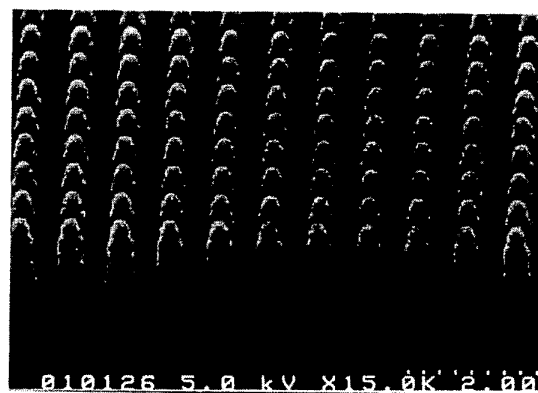


Fig. 3 SEM Photograph of S-SGT structured cell.

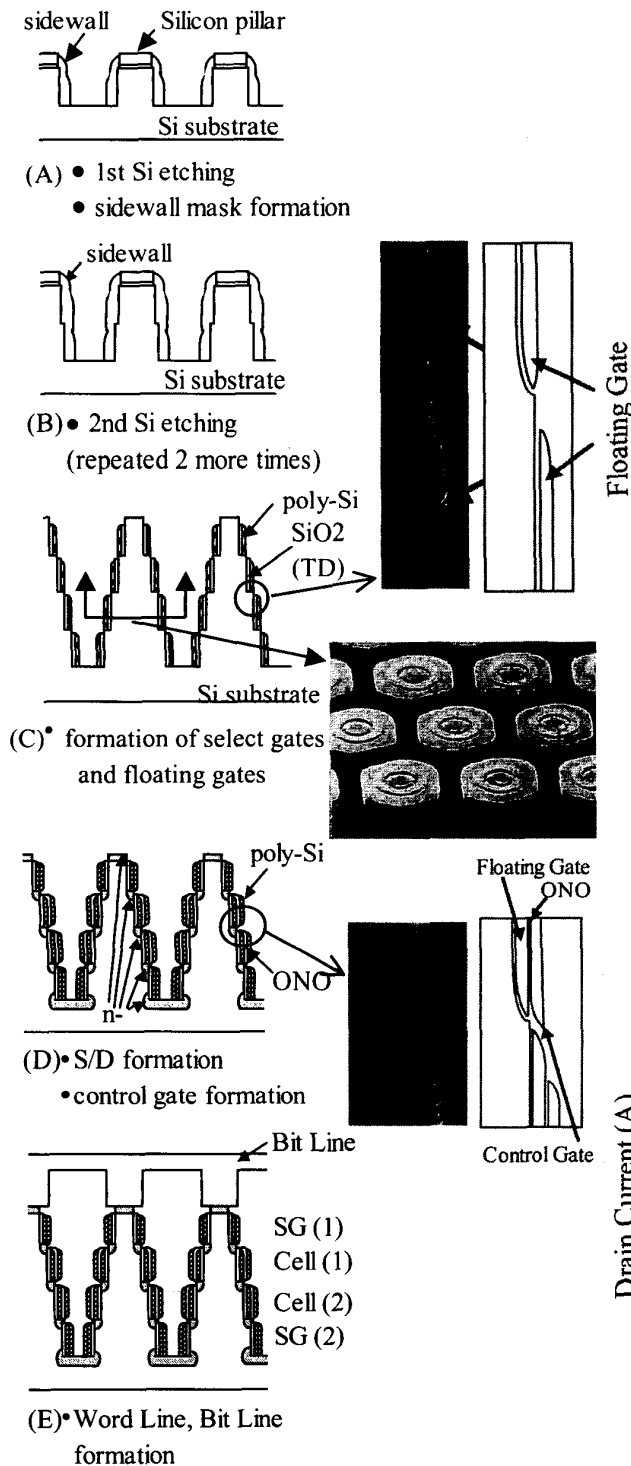


Fig. 4 S-SGT structured cell fabrication sequence.

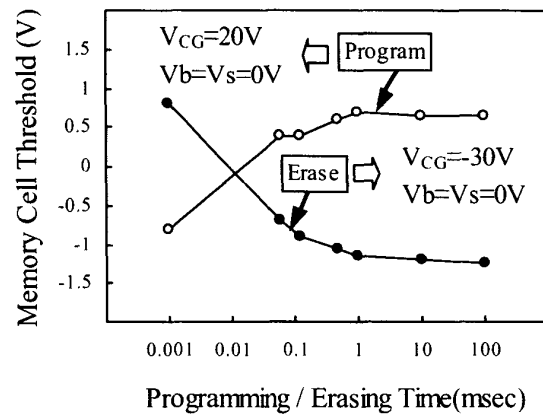


Fig. 5 Cell threshold voltages as a function of programming time and erasing time in the S-SGT structured cell.

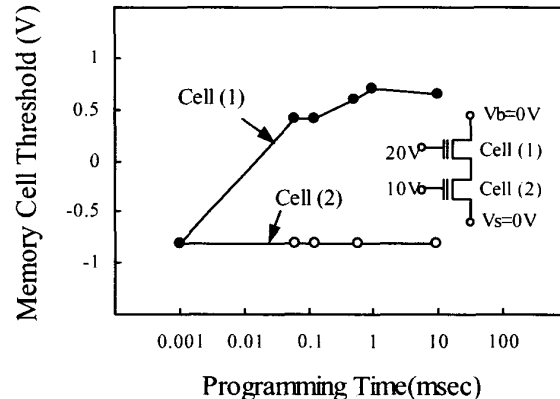


Fig. 6 Cell threshold voltages shifts of the selected memory cell and the unselected one as a function of programming time in the S-SGT structured cell.

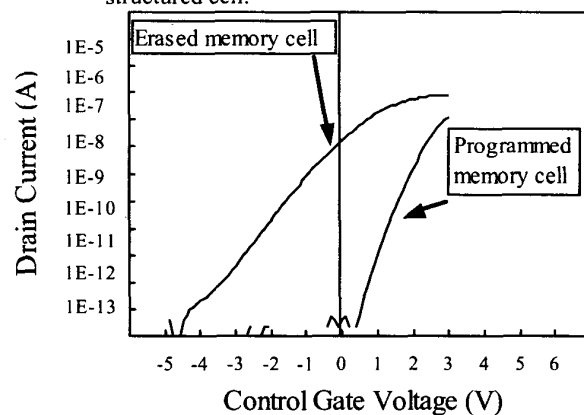


Fig. 7 Drain current versus control gate voltage characteristics after erasing and after programming of the S-SGT structured cell.