

Micron reveals flash roadmap to 500+ layer 3D NAND

By **Chris Mellor** - May 13, 2022



Micron has 232-layer 3D NAND in development and a roadmap out to 500-plus layers.

3D NAND is manufactured by layering groups of cells atop each other in a vertical stack. The more layers there are in a flash die, the higher the capacity. All the manufacturers are currently building 100-plus layer chips with higher layer counts in prospect.

Yesterday [Western Digital](#) revealed it was building 162-layer NAND with a 200+ layer die coming.

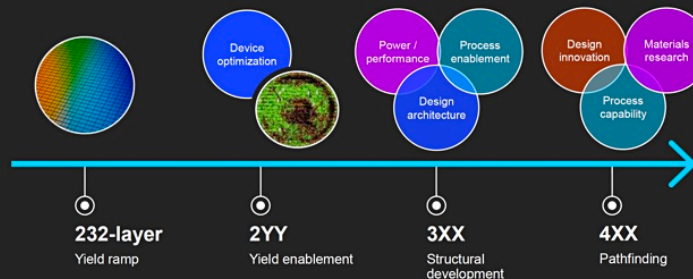
Micron revealed its NAND and DRAM roadmap details at an Investor Day event on May 12. It is manufacturing 176-layer flash chips in volume, its fifth 3D NAND generation, and intends to ramp up manufacturing of sixth-generation 232-layer flash by the end of calendar 2022.



NAND technology roadmap for leadership

Enabling leadership for the next decade

- Advanced CMOS enabling performance
- Extending dual stack technology
- Expanding QLC leadership



Micron

The dual stack technology refers to stacking two 3D NAND dies one above the other, so-called "string stacking." This overcomes semiconductor manufacturing difficulties such as etching connection holes through the layers as the number of layers increases. The sides of such holes can become distorted as hole depth deepens and prevent the NAND cells from operating properly.

Micron said it was focusing on QLC (4bits/cell) NAND and didn't mention increasing the cell bit count to 5 with PLC (penta-level cell), which Western Digital is investigating and Sologdin developing. We think this is because Micron is being cautious and not that it has rejected PLC NAND as infeasible.

Here is a table comparing the NAND manufacturers' 3D NAND layering status, history and plans:

3D Layer Cake

SK hynix		SK hynix Solidigm		Western Digital/Kioxia		Samsung		Micron		YMTC	
Generation	Layers	Generation	Layers	Generation	Layers	Generation	Layers	Generation	Layers	Generation	Layers
V3	48	Gen 1	32	BiCS 2	48	V3	48	Gen 1	32		
V4	72	Gen 2	64	BiCS 3	64	V4	64	Gen 2	64	Xtacking 1	64
V5	96	Gen 3	96	BiCS 4	96	V5 (May 2018)	9x	Gen 3	96		
V6 (Q4, 2019)	128	Gen 4 (Q4 2020)	144	BiCS 5 (Q1, 2020)	112	V6 (June 2019)	128	Gen 4 (Q4, 2019)	128	Xtacking 2	128
V7 (2021)	176	Gen 5? (2023)	196?	BiCS 6	162	V7 (April 2021)	176	Gen 5 (Nov 2020)	176		
V7(2023?)	238			BiCS 7	212	V8 (July 2021)	200	Gen 6 (End 2022)	232		
				BiCS 8	?	V9	3xx	Gen 7	2yy		
V7 (2025)	500+					V10		Gen 8	3xx		
V7 (2030)	800+					V11	5xx	Gen 9	4xx		

The manufacturing start dates are approximate

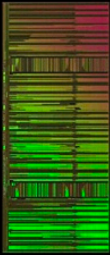
WD would say there is no inherent superiority in having a slightly higher layer count – 238 (SK hynix), 232 vs 212, for example – because it is shrinking its cell size laterally,

There is an implied advantage here as building a layer means making a group of processing steps and, other things being equal, making 232 processing groups takes longer than making 212. But so many other things come into play, such as wafer manufacturing yield, that the end result; manufacturing cost, chip density price, endurance and performance, is not based only on the number of manufacturing steps.

Micron claims that its 232-layer technology represents the world's most advanced NAND:

232-layer: The world's most advanced NAND

Industry leadership sustained – starting ramp in late CY22



1Tb TLC NAND

- Extending CuA and 2 array stack process architecture
- Optimized for leadership in managed NAND and SSD
- Combination of external and optimized internal controllers
- Increased density, power and bandwidth node-over-node



232 Layer, 2 stack, CuA* NAND

*CuA: CMOS Under Array

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CuA = CMOS under Array

This slide showed a 1Tb (128TB) TLC die. Micron did not mention [zoned SSDs](#) in its presentation but it did talk about external controllers, implying NAND/SSD controllers operating in the host system, which is necessary with zoned SSDs. We might expect to see SSDs using the 232-layer NAND to ship in late 2023.

The Investor Day did not cover storage-class memory, such as [3D XPoint](#), which it used to manufacture for Intel. But it did talk about CXL (Computer eXpress Link) and a slide showed something called emerging memory technology at the end of a CXL link:

Another talked about “New Memory architecture” and “CXL roadmap focus on customer co-invention,” whatever that might mean. It could imply possible customer-specific, CXL-linked memory devices. We think emerging memory and new memory architecture could apply to storage-class memory and/or to 3D DRAM.

NAND roadmaps from Solidigm, Western Digital, and Micron testify to the technology health and vitality of the NAND and SSD markets, meaning we can look forward to growing flash data storage capacity and increased application speed.

