

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00190
Patent 11,568,941

PATENT OWNER'S SUR-REPLY

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REGULATIONS

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Ex.	Description
2001	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv- 05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)
2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
2004	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 14, 2025), ECF No. 243
2005	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending <i>Inter Partes</i> Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2006	Declaration of Dr. Sunil P. Khatri, Ph.D. In Support Of Patent Owner's Preliminary Response ("Khatri")
2007	<i>Curriculum Vitae</i> of Dr. Sunil P. Khatri

Ex.	Description
2008	Soon-Moon Jung et al., <i>Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node</i> , 2006 International Electron Devices Meeting Technical Digest (“Jung”)
2009	Erh-Kun Lai et al., <i>A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory</i> , 2006 International Electron Devices Meeting Technical Digest (“Lai 2006”)
2010	Declaration of E. Fred Schubert, Ph.D. in Support of Defendants’ Proposed Claim Constructions (Patent Local Rule 4-3), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv- 05792-RFL (N.D. Cal. Jan. 31, 2025) (“Schubert Decl.”) (excerpts)
2011	U.S. Patent Application Publication No. 2016/0071595 A1 (“Dong III”)
2012	U.S. Patent Application Publication No. 2019/0006021 A1 (“Ghai”)
2013	Excerpts from <i>The Merriam-Webster Dictionary</i> (2016) (“2016 Merriam-Webster Dictionary”)
2014	Excerpts from <i>The American Heritage Dictionary of the English Language</i> (5th ed. 2018) (“2018 American Heritage Dictionary”)
2015	U.S. Patent Application Publication No. 2016/0343414 A1 (“Lee V”)
2016	U.S. Patent Application Publication No. 2016/0099060 A1 (“Yoo”)
2017	Rino Micheloni et al., <i>Inside NAND Flash Memories</i> (2010) (excerpts)
2018	Order Granting Motion to Consolidate, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Aug. 21, 2024), ECF No. 106

Ex.	Description
2019	Jan M. Rabaey et al., <i>Digital Integrated Circuits: A Design Perspective</i> (2003) (excerpts)
2020	<i>3D Flash Memories</i> (Rino Micheloni ed. 2016)
2021	Transcript of the deposition of David Kuan-Yu Liu, Ph.D., taken October 16, 2025 (“Liu-Dep1”)
2022	Declaration of David Kuan-Yu Liu, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2024-00792 (PTAB Apr. 29, 2024), Ex. 1003
2023	Reply Declaration of David Kuan-Yu Liu, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2024-00792 (PTAB Apr. 25, 2025), Ex. 1027
2024	Myounggon Kang & Yoon Kim, <i>Natural Local Self-Boosting Effect in 3D NAND Flash Memory</i> , IEEE (2017) (“Kang”)
2025	Yoon Kim & Myounggon Kang, <i>Down-Coupling Phenomenon of Floating Channel in 3D NAND Flash Memory</i> , 37 IEEE Electron Device Letters 1566 (Dec. 2016)
2026	Sangwoo Han et al., <i>Investigation of Inhibited Channel Potential of 3D NAND Flash Memory According to Word-Line Location</i> , 9 Electronics 268 (Feb. 5, 2020)
2027	Youngseok Jeong, <i>Hot Carrier Injection Phenomenon due to Excessive Natural Local Self-Boosting Effect in 3D NAND Flash Memory</i> , Extended Abstracts 2019 Int’l Conf. on Solid State Devices & Materials 685 (2019) (“Jeong”)
2028	Declaration of Dr. Sunil P. Khatri, Ph.D. in Support of Patent Owner’s Response (“Khatri2”)
2029	Declaration of Richard A. Lowry in Response to Petitioner’s Objections to Evidence, with Appendices A-J [<i>served, not filed</i>]

Ex.	Description
2030	Transcript of the Deposition of David Kuan-Yu Liu, Ph.D., taken March 17, 2026 ("Liu-Dep2")

I. Introduction

Patentability should be confirmed.

Petitioner's Reply does not cure Ground 1's core defect: Dong never discloses the claimed vertical wordline arrangement. Figures 5a/5g depict voltage schemes, not physical structure like the 2D array in Figure 4. Dong's passing reference to "three dimensional" does not supply the recited vertical wordline arrangement in any shape or form. Faced with this gap, Petitioner first recasts "from bottom to top" through a new construction untethered to physical arrangement to retrofit Dong to the claims. Next, Petitioner invokes a new "at once envisage" theory that does precisely what the Federal Circuit prohibited in *Nidec*: it uses POSITA knowledge to fill Dong's structural gaps.

Ground 2 likewise fails. The Petition never supplied a claim-specific obviousness theory or a motivation to modify Dong's 2D structure into the recited vertical wordline arrangement. The Reply's new theories cannot cure that omission. Moreover, a POSITA would not transpose Dong's 2D methods—applicable to *two* program disturb modes—to a 3D NAND environment which requires addressing *four* program disturb modes.

Grounds 3 and 4 still fail for the reasons identified in the POR. The Reply replaces the Petition's mappings with new ones, along with a new claim construction

of “a program operation.” The Board should disregard these untimely theories. Even if considered, they fail on the merits.

A. Claim Construction

1. “From Bottom To Top” Means From Lowest To Highest, Not Source-To-Drain Indexing

The Board construed “from bottom to top” at institution to mean “the word lines of the memory portions are arranged vertically from the bottom end of the memory portion toward the top of the memory portion.” ID 17. Petitioner offers no basis to depart from that finding. Instead, it advances a new “indexing scheme” construction, whereby a memory string is programmed from source to drain regardless of the physical location of the source and drain ends. Reply 2-3; Ex.1089 ¶¶6, 14-15. This is contrary to the Petition, where Petitioner argued that “from bottom to top” means having “the source *end* of the NAND string at the bottom, and the drain *end* of the NAND string at the top” (Pet.35; Ex.1004 ¶¶113, 120).¹ Moreover, Petitioner’s new construction conflicts with the ’941 patent’s claims, specification, and figures. The Board should adopt PO’s construction which aligns with the intrinsic record and reject Petitioner’s new “source to drain” indexing theory, which is indifferent to physical arrangement (Ex.1089 ¶¶13, 15). *See Intelligent Bio-*

¹ Emphases added and citations omitted unless stated otherwise.

Systems, Inc. v. Illumina Cambridge Ltd., 821 F.3d 1359, 1369-70 (Fed. Cir. 2016); POR 30. In any case, Petitioner's new construction fails on the merits.

Petitioner's new construction disregards the plain meaning of "bottom" and "top." Petitioner's construction broadens "from bottom to top" to include "source to drain" programming even where the source is not on the bottom and the drain is not on the top, including (1) U-shaped NAND where both are on top (Ex.1089 ¶¶24, 26), (2) 2D NAND where the source is on the left and the drain is on the right (*id.* ¶11), and (3) drain-to-source configurations where the source is on top and the drain is at bottom (*id.* ¶25). Liu-Dep2 (Ex.2030), 23:18-26:7 ("It has nothing to do with the physical level."), 28:14-29:16. Petitioner's new construction thus renders meaningless the recited terms "bottom" and "top" by disconnecting them from the physical location of the components. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 809-10 (Fed. Cir. 2021) ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous."). Petitioner's effort to reframe "above" and "below" as mere "indexing" that does not "require a physical memory string architecture" renders these terms meaningless too because, for example, "above" could mean "to the left" in a horizontal 2D NAND array or "below" in the U-shaped NAND and drain-to-source configurations. *See, e.g.*, Ex.1089 ¶¶6, 11, 15, 25; Reply 2.

Petitioner's new construction is also inconsistent with intrinsic evidence, which supports "from bottom to top" refers to a vertical arrangement in a physical memory. POR 13-21. Intrinsic evidence confirms that "above" and "below" refer to a physical location relevant to other components, establishing "a relative top and bottom," as the Board correctly recognized. *E.g.*, Ex.1001, cls. 1, 3-5, 2:67-3:3, 4:18-20, 4:34-36; ID 16-17; POR 14-15. The Board also noted the claimed relationships refer to "relative vertical locations of the word lines within the memory portions." ID 16-17. Figures 1-11 depict a memory's wordlines vertically stacked. Ex.1001, Figs.1-11; Ex.2028 ¶116; ID 17-18. The specification supports the phrase "bottom to top" identifies "the location of the word line in relation to its vertical location, not to its location relative to the source or drain," as the Board found. ID 18; POR 16-18 (citing Ex.1001, 5:4-19, 5:38-50 ("lowermost" and "uppermost" portions)). The '941 patent does not describe a "source" or "drain," much less in a context that supports an indexing scheme whereby "bottom" means "source" and "top" means "drain." Ex.2028 ¶127; *Nystrom v. TREX Co.*, 424 F.3d 1136, 1144-46 (Fed. Cir. 2005) (broadening contrary to intrinsic evidence "violates the principles articulated in *Phillips*").

Petitioner's extrinsic citations cannot override the clear intrinsic record, which confirms PO's construction. *See* Reply 2-3; *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996); POR 20-21. Even if considered, Petitioner's

extrinsic evidence supports Petitioner's construction renders meaningless both "bottom" and "top." POR 20-29; *see, e.g.*, Ex.1082, Fig.2B (2D NAND array with source and drain at same level); Ex.1084, Fig.1D (U-shaped array with source and drain both at the top). Petitioner's cited dictionary confirms "bottom" and "top" are used in the plain, vertical sense—as in the claims—not as proxies for source and drain. POR 14; Ex.1001, 6:55-60. Finally, Petitioner's false equivalence of figures from the '941 patent and Dong contradicts the intrinsic evidence, which confirms the '941 figures show vertically arranged wordlines of a memory. *E.g.*, Ex.1001, 4:29-36, Fig.8; *infra* §II.A.1.

Petitioner's expert also contradicts Petitioner's position. Petitioner's expert conceded that in 2020, "three dimensional" memory—as in the '941 patent (Ex.1001, 1:39-41; POR 7-9)—"was practically synonymous with vertical memory strings" and that it "ignores reality" to suggest otherwise. Ex.1089 ¶¶40, 47, 84. Petitioner's expert also recognized that in 2020, 3D NAND manufacturers were not focused on "2D NAND arrays." *Id.* ¶¶41, 43. This confirms PO's construction.

Petitioner's repeated focus on "substrate" misses the point. PO's construction does not depend on an external reference point; it requires only that the claimed wordlines be "arranged vertically from bottom (lowest) to top (highest)." POR 13-15, 29; ID 19; *see, e.g.*, Ex.1001, 6:55-60. Even if PO proposed a construction referencing the substrate (not the case), the Board need only construe "from bottom

to top” “to the extent necessary to resolve the controversy.” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

2. “A Program Operation” Does Not Include A Verify Phase

Petitioner's expansion of “program operation” to encompass verification is both procedurally improper and contrary to the intrinsic record.

First, the Petition never construed “a program operation” to include verify. *See* Reply 4; POR 29-30. The Petition has a “*see also*” cite (Pet.15) to one background paragraph from its expert that does not mention the '941 patent, its claims, or the phrase “a program operation” (Ex.1004 ¶60). POR 30; 37 C.F.R. § 42.6(a)(3) (improper incorporation by reference). That paragraph describes “a typical programming operation” using Dong as an example. Ex.1004 ¶60. The Petition (at 71) similarly fails to mention the '941 patent or “a program operation.”² The Petition's Technology Background implies “a program operation” excludes verify by omitting it and instead stating “a ‘high-voltage V_{pgm} ’ is applied” “[t]o program a particular NAND memory cell.” Pet.14; *see* Ex.1009, 44 (“program operation” is “performed by applying high-voltage V_{pgm} to control gate”). Having

² Nor does it cite the only paragraph Dr. Liu identified as relevant (Ex.1004 ¶60). Liu-Dep1 (Ex.2021), 212:22-213:12, 213:20-214:13.

told the Board no further construction was needed (Pet.22), Petitioner cannot in Reply import a verify-based construction.

Petitioner's new construction also fails on the merits. Nothing in the intrinsic evidence supports "a program operation" includes a verify operation not mentioned in the '941 patent. The '941 patent's statement that "program operation" refers to "programming a memory cell" does not provide license to import any extrinsic function. It is telling that Petitioner never mentions the claims and ignores the other intrinsic evidence supporting PO's construction, including repeated disclosure of applying "a program voltage V_{pgm}" during a charge-injection phase (POR 30-31). *See* Reply 4-5.

Lacking intrinsic support, Petitioner relies on extrinsic evidence to shore up its proposed construction such as Dong, Dr. Liu, and Exs.1090-1093 describing programming in other contexts (*id.* 5-6), but they contradict the intrinsic record, which does not disclose a read/verify phase. *See Vitronics*, 90 F.3d at 1583.

Petitioner's footnote cannot diminish Dr. Liu's contrary testimony. *See* Reply 5 n.1; POR 33-34. Petitioner does not even address Dr. Liu's prior testimony that in Costa, "the read (verify) occurs *after the program operation* to verify whether the program operation was successful." Ex.2022 ¶248. Here, Dr. Liu testifies Costa supports that "a program operation" includes a read/verify phase. Liu-Dep1, 159:17-161:13; POR 33-34.

Petitioner further errs in arguing extrinsic evidence of “pass voltage disturbance” during a verify process supports its construction. Reply 4-5. Petitioner refers to “*read* pass voltage” disturb applied during a read/verify phase, which is not mentioned in the '941 patent. *See* Ex.1012 [0112], Abstract; Ex.2028 ¶235. The '941 patent instead describes applying voltages during the charge-injection phase to reduce program disturb and pass voltage disturb at the same time. *See* Ex.2028 ¶¶84-86, 148; *see also* Ex.1010, 88; Ex.1004 ¶74. Petitioner's verify-based construction is a rewrite driven by references like Costa, not the '941 patent.

Petitioner fails to rebut the remaining arguments of the POR. POR 29-34; *see, e.g., id.*, 31-32 (Dr. Liu's statements supporting PO's construction). The Board should adopt PO's construction and not Petitioner's construction, which has “no basis anywhere in the intrinsic record.” *See Genuine Enabling Tech. LLC v. Nintendo Co.*, 29 F.4th 1365, 1373-75 (Fed. Cir. 2022).

3. Preambles Are Limiting

Petitioner does not dispute that the preambles of claims 5 and 11 are limiting. Reply 1-6; *see* POR 34-35; ID 14-15.

II. GROUND 1 (Anticipation)

Petitioner's argument that Dong anticipates under Petitioner's construction of “bottom to top” fails. Reply 6-7; *supra* §I.A.1. As the Board recognized, Dong's 2D memory arranged horizontally from source to drain does not by itself satisfy the

“from bottom to top” limitation. ID 16-17, 24. Petitioner's remaining arguments also fail under PO's construction.

A. Dong Does Not Anticipate Vertical Wordlines As Recited

Anticipation is a high bar that “requires that every element and limitation of the claim was previously described in a single prior art reference, either expressly or inherently, so as to place a person of ordinary skill in possession of the invention.” *Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1082 (Fed. Cir. 2008). Because Petitioner disclaims inherency (Reply 11), it must show that Dong *expressly* discloses the claimed vertical architecture reciting a “first portion” of wordlines vertically arranged “from bottom to top” (i.e., from lowest to highest) in “first” and “second” memory portions. But Dong's Figures 5a/5g do not disclose this recited vertical arrangement, as the Board correctly recognized (ID 22 n.6). And Dong's single, passing statement that its “array of storage elements can be three dimensional” (Ex.1005 [0095]), falls way short of an anticipatory disclosure of every recited element “arranged as in the claim.” *Net MoneyIN, Inc. v. Verisign, Inc.*, 545 F.3d 1359, 1369-71 (Fed. Cir. 2008); Ex.2028 ¶¶187-195.

Recognizing these deficiencies, Petitioner conjures up a new “at once envisage” anticipation theory—one it could have raised in the Petition but did not. *Broad Ocean Techs., LLC v. Nidec Motor Corp.*, IPR2015-01617, Paper 31, 17-19 (Dec. 21, 2016); *see* Pet.35 (acknowledging that “bottom to top” could “require

vertical strings in a 3D NAND memory”). This theory resembles obviousness, not anticipation. It also fails because a reference missing a limitation (i.e., Dong missing the recited vertical arrangement) cannot anticipate simply because a POSITA would “immediately envision” it. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 851 F.3d 1270, 1274-75 (Fed. Cir. 2017).

Petitioner’s argument that PO “erroneously analyzes anticipation” mischaracterizes the POR. Reply 8. PO did not argue anticipation should be interpreted using Dong’s May 7, 2007 filing date or that a POSITA is confined to 2007 knowledge. *See id.* 8-12. PO argued that a POSITA would determine the scope of Dong’s isolated “three dimensional” language in context of Dong’s own 2007 disclosure and contemporaneous architectures, which only support reference to horizontal-stacked wordline arrangements consistent with Dong’s own 2D structure. POR 42-44; Ex.2028 ¶¶190-195. That is precisely the anticipation inquiry, which asks what a POSITA would “reasonably understand or infer” from a single reference, while allowing extrinsic evidence only to explain—not expand—its disclosure.³ *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1284-85

³ Petitioner’s “effective filing date” argument (Reply 8-9) conflates determination of prior art with sufficiency of disclosure.

(Fed. Cir. 2017); *Galderma Laboratories, L.P. v. Teva Pharms. USA, Inc.*, 799 F. App'x 838, 842-845 (Fed. Cir. 2020).

Petitioner's approach contravenes well-established Section 102 jurisprudence as it improperly relies on "prevailing 3D architecture in 2020" (Reply 9; Ex.1089 ¶¶40-47) to expand Dong's ambiguous "three dimensional" language into disclosure of the claimed vertical structure.⁴

1. Dong's Figures 5a/5g Do Not Anticipate Vertically Arranged Wordlines As Recited

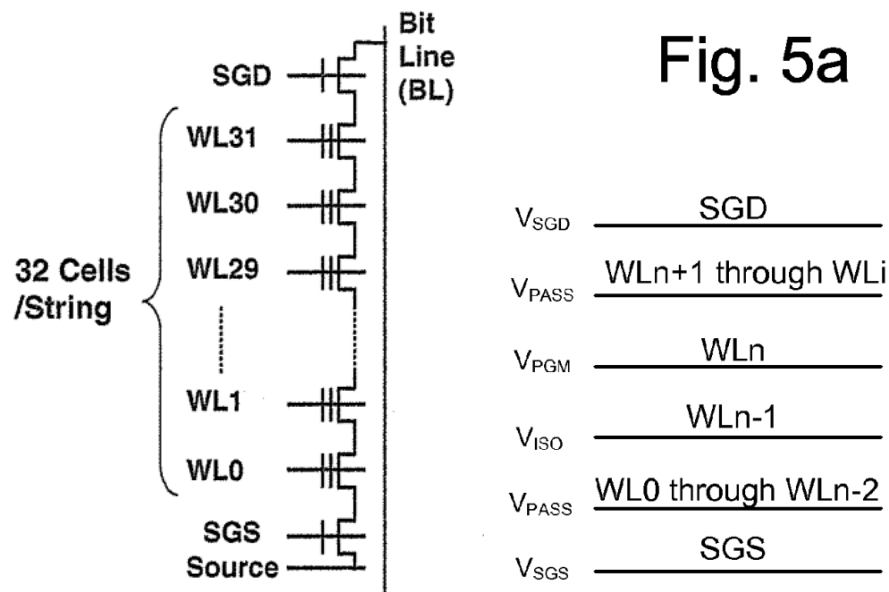
Dong's only structural disclosure is 2D (Figure 4), not the claimed arrangement. Figure 4 illustrates a physical structure of 2D memory with wordlines arranged horizontally from left to right above the substrate, depicting voltages from "one example boosting mode" of Figure 5c. Dong [0045]-[0046], Fig. 4. Dong recognizes that Figures 5a/5g "depict different examples of self-boosting modes." *Id.* [0047]; POR 36-39; *see* Reply 11-13.

Petitioner argues Dong's Figures 5a/5g depict "vertically-oriented wordlines" by superficially comparing them to figures in the '941 patent, but Dong's description confirms Figures 5a/5g depict "self-boosting modes" not physical structure, as the Board correctly found at institution. Reply 11-14; ID 22 n.6. Dong ties Figures

⁴ Petitioner errs in relying on the Board's institution decision addressing obviousness not anticipation. Reply 9 (citing ID 26-27).

5a/5g to Figure 4's 2D structure, describing Figure 4's "substrate 490," "isolation word line 412," and hot carrier injection when referencing the Figures 5a/5g embodiments—a point Petitioner does not dispute. Dong [0047], [0065], [0063]-[0067]; POR 36-40; Ex.2028 ¶¶177-186. Moreover, the '941 patent specification *explains* its figures depict a physical memory where Dong does not. See Reply 12-13; ID 22 n.6. The '941 patent specification and figures confirm Figure 8, for example, depicts a physical "memory" with wordlines vertically arranged, each receiving voltage driven by controller 190. Ex.1001, 2:48-49, 4:29-47, 5:16-21, 5:25-28, Figs.7-8; POR 7-9, 15-18.

Dong's Figures 5a/5g do not disclose vertical wordlines any more than circuit diagrams of 2D NAND flash memory, which also symbolically illustrate wordlines arranged in a vertical manner but do not represent physical structure:



Ex.1009, 39 (Fig.2.2); Ex.1004 ¶113 (confirming 2D); Dong, Fig.5a; POR 23-26.

2. Dong's "Three Dimensional" Language Does Not Anticipate Vertically Arranged Wordlines As Recited

Dong does not expressly disclose vertically arranged wordlines as recited. Dong's single mention of "three dimensional" does not supply the missing limitation and thus fails to anticipate. POR 40-44.

First, Dong never links the generic "three dimensional" language to the self-boosting modes of Figures 5a/5g. Dong [0095]. Instead, Dong describes "memory die 1298" architecture at a high level. *Id.*

Second, Dong's mere statement of "three dimensional" does not necessarily suggest the recited "memory" portions of wordlines vertically arranged "from bottom to top," the "second portion formed below the first portion," or application of specific voltages to particular wordlines. *See, e.g.*, Ex.1001, 6:55-7:2 (cl. 1); POR 42-44. A POSITA would understand Dong's "three dimensional" concept as stacking horizontal 2D NAND dies to form a 3D NAND structure (e.g., Stacked and Multi-layer TFT) consistent with Dong's disclosure directed to 2D-based program disturb. Ex.2028 ¶¶190-195.

In *Wasica*, the Federal Circuit found that a prior art reference disclosing a genus of "any modulation scheme," which includes a constant frequency, does not anticipate the recited species of "constant frequency." *Wasica*, 853 F.3d at 1285-86. So too here: a broad genus of "three dimensional" memory does not disclose with

particularity the species of vertically arranged wordlines as recited. And even if it did (it does not), Petitioner failed to define any genus or species. *See id.*

Third, Dong's mention of "three dimensional" is ambiguous at best, and "[a]mbiguous references do not anticipate a claim." *Id.* at 1284; *see* Reply 11.⁵ It is **undisputed** that Dong's "three dimensional" includes these 2D-based structures that are not arranged "from bottom to top" as claimed. POR 42-44; Reply 16; Ex.1089 ¶58. Petitioner's argument that "three dimensional" includes vertical wordlines only further supports ambiguity. Like the Federal Circuit's holding in *Wasica* that prior art disclosing a "common" frequency did not anticipate a "constant" frequency because "common" was ambiguous and could mean "constant or nonconstant frequency," Dong's "three dimensional" reference does not anticipate because it is ambiguous and could mean 2D-based NAND structures as PO proposes. *Wasica*, 853 F.3d at 1284-85.

Dong's ambiguity creates a significant gap between the prior art and the claims, which Petitioner aims to improperly fill with the knowledge of a POSITA. *See, e.g.*, Ex.1089 ¶¶38-56 (19 paragraphs of expert testimony); Exs.1095-1099, 1103-1107. But "differences between the prior art reference and a claimed invention,

⁵ *Guardant Health, Inc. v. University of Washington*, 2026 WL 184334, *6 (Fed. Cir. Jan. 23, 2026) is inapposite because Dong's issue is lack of disclosure. *See* Reply 8.

however slight, invoke the question of obviousness, not anticipation.” *Net MoneyIN*, 545 F.3d at 1371; *Topliff v. Topliff*, 145 U.S. 156, 161 (1892) (finding insufficient “that the device relied upon might, **by modification**, [be] made to accomplish the function”). By invoking POSITA knowledge to fill in what Dong does not explicitly disclose, Petitioner crosses the line from anticipation to obviousness (an argument not in the Petition, *infra* §III).

3. Petitioner’s New “Envisage” Theory Fails To Anticipate Vertically Arranged Wordlines As Recited

Unable to locate the claimed structure in Dong itself, Petitioner’s Reply pivots to a new argument—that a POSITA would “at once envisage” the claimed invention from Dong’s “three dimensional” language. But that theory underscores the problem by assuming the very structural disclosure missing from Dong, an approach squarely foreclosed by Federal Circuit precedent.

Petitioner invites the same error the Federal Circuit identified in *Nidec*, 851 F.3d at 1274-75. There, the court recognized that the “at once envisage” framework cannot be used to “fill in missing limitations simply because a skilled artisan would immediately envision them.” *Id.* The *Nidec* court recognized that *Kennametal* “does not stand for the proposition that a reference missing a limitation can anticipate a claim if a skilled artisan viewing the reference would ‘at once envisage’ the missing limitation,” but rather whether the reference expressly spells out a definite and limited class enabling a POSITA to at once envisage each member thereof. *Id.*

(citing *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381-82 (Fed. Cir. 2015)); see Reply 11.

Unlike *Kennametal*, where the reference disclosed using any of five binding agents with any of three coatings such that a POSITA would “at once envisage” the recited combination, Dong’s “three dimensional” mention is open-ended, ambiguous, and undefined. And Petitioner fails to identify “a definite and limited class” of 3D memory, opting instead to assume disclosure of the claimed arrangement. See *Nidec*, 851 F.3d at 1274-75; *SMA Solar Tech. Am., LLC v. Tigo Energy, Inc.*, IPR2023-00879, 2024 WL 4590767, *6-8 (Oct. 28, 2024) (finding no “envisage” anticipation where Petitioner failed to provide “discussion of any genus” or “limited class” despite recognizing that a claimed “micro-controller” is ““ubiquitous”” and “commonplace”).⁶

Petitioner’s expert confirmed he did not understand the *Kennametal* “at once envisage” standard and applied a different test—what a POSITA would “right away” visualize—so his testimony is “entitled to *very* little weight.” See Liu-Dep2, 29:24-36:21, 38:5-39:16; *Interactive Commc’ns Int’l, Inc. v. Blackhawk Network Inc.*,

⁶ Petitioner errs in citing *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022) because that case addresses obviousness.

IPR2023-01235, Paper 34, 43-44 (Feb. 6, 2025) (original emphasis); *Nidec*, 851 F.3d at 1274-75.

Petitioner's separate 2007 disclosures only underscore the gap in Dong. *See Galderma*, 799 F. App'x at 842-845. Those disclosures show, at most, short silicon-pillar structures—a far cry from **Dong** disclosing 32 wordlines vertically arranged to *anticipate* the recited claims. Exs.1101-1102 (two-cell); Ex.1075 (four-cell); Ex.1087 (four-cell); *see* Pet.31-33, 50-51; ID 23 (“32-cell NAND string”). At best, they confirm Dong's “three dimensional” is not self-defining. PO's expert testimony—not materially disputed (Reply 16)—supports it refers to stacked layers of horizontal 2D NAND arrays (like Dong's 2D array). Ex.2028 ¶¶66-70, 190-195; POR 42-44; *see Wasica*, 853 F.3d at 1284; *see also* Ex.1009, 322 (vertical gate 3D NAND with 2D-based arrays). Petitioner asks the Board to supply through POSITA knowledge a vertical architecture Dong never discloses. That is obviousness, not anticipation. *Nidec*, 851 F.3d at 1274-75.

Dong also fails on enablement. Dong's two-word nod to “three dimensional” does not equip a POSITA to make and use Dong's 2D self-boosting schemes in the recited vertical 3D context without undue experimentation. *In re Morsa*, 713 F.3d 104, 110-11 (Fed. Cir. 2013); POR 44; Ex.2028 ¶¶194-195.

III. GROUND 2 (Obviousness)

The Petition never argued it would have been obvious to apply Dong's Figures 5a/5g voltage scheme in a 3D NAND context, much less explain why a POSITA would do so. POR 45-50; *see In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016). The Reply cannot cure that omission by stitching together scattered portions of the Petition. *See* Reply 16-18.

First, Petitioner's generic obviousness theory in Ground 2 (*id.* 17-18) and regarding claim 5 (Pet.29) does not provide carte blanche to raise obviousness for any limitation. Petitioner's obviousness theory is limited to using a memory string length of 32 cells in Dong's horizontal structure (*id.* 31; *supra* §II.A.1), unrelated to the limitation "from bottom to top." POR 46-47.

Second, Petitioner's Technical Background section describing "similarities" between 2D and 3D NAND fails to mention Dong, falling well short of providing a motivation for the specific modification at issue here. *See* Reply 17, 23; POR 47-48.

Third, expert testimony that a "2D memory string would at a minimum render obvious the bottom to top requirement" is a conclusion, not a motivation. Petitioner fails to provide the requisite motivation or reasonable expectation of success. Reply 17; POR 47-48; *see In re Van Os*, 844 F.3d 1359, 1361 (Fed. Cir. 2017); POR 48-50.

Fourth, the Petition referenced Shirai and Righetti to support obviousness regarding “utiliz[ing] a 32-cell memory string” as confirmed by Petitioner’s expert—not for a vertical wordline arrangement. Liu-Dep1, 78:20-80:13; Pet.31 (citing Righetti’s Figure 6 regarding “74 wordlines”; Shirai’s Figure 1 not cited); *see* POR 46; Reply 18.

A. A POSITA Would Not Apply Dong’s 2D NAND Self-Boosting Schemes In Vertically Arranged Wordlines As Recited

Petitioner’s arguments also fail on the merits.

Petitioner now argues that because 2D NAND and 3D NAND overlap in conventional program disturb modes (PGM and X), Dong’s 2D program disturb alleviation methods equally apply to 3D NAND (PGM, X, XY, and Y). This argument fails as it ignores that Dong’s 2D program disturb modes fail to address at least two new modes in vertical 3D NAND.

First, program disturb modes 1 (PGM), 2 (X-mode), 3 (Y-mode), and 4 (XY-mode) “occur simultaneously” (Ex.1009, 364) in vertical 3D NAND arrays. *Id.* 363-366. Petitioner’s expert recognized these modes “occur in the program injection phase” and “*all need to be addressed* in order to reliably operate a 3D NAND during programming.” Liu-Dep2, 47:9-16; Ex.1089 ¶68.

Second, it is undisputed that Dong’s program disturb methods address only two *conventional* modes (i.e., PGM and X-modes). Reply 20; Ex.1089 ¶69.

Third, a POSITA would not be motivated to apply Dong's program disturb methods in a vertical 3D NAND environment, because Dong's methods would not address the Y- and XY-modes. Ex.2028 ¶¶75-83; Ex.1089 ¶69.

Aritome does not “proffer three solutions for the *new* disturb modes” as Petitioner claims (Reply 22), it describes three solutions “to suppress a program disturbance in a 3D NAND cell.” Ex.1009, 363-364. Rather than suggest using conventional 2D NAND methods (like Dong's), Aritome discloses that these three solutions effectively address X- and Y-mode program disturb in 3D NAND. *Id.* Fig.8.12; Ex.2028 ¶¶209, 220.

Petitioner tries to minimize the significance of 3D NAND's floating-channel behavior and NLSB (Reply 23), but that technical distinction is exactly why Dong's 2D approach does not carry over. Petitioner ignores that “[t]he NLSB effect *does not require the local boosting scheme used in conventional 2D NAND*, because it can achieve a sufficiently high potential even if the number of stacks is increased.” Ex.2027, 1; Ex.2028 ¶215; POR 52-53. Petitioner points to HCI (Ex.2027), but that is solved by Aritome's three solutions (none of which are 2D self-boosting schemes like Dong). Ex.1009, 363-364. Petitioner also points to local SBPI out of context, ignoring “[t]he NLSB effect allows a sufficiently high boosted potential of an inhibited string to be achieved *without* a local [SBPI]” (like Dong). Ex.2024, 1, 3; Ex.1089 ¶¶79, 81 (“boost[s] to a higher channel voltage”); POR 52-53; *see* Ex.2024,

2-3, Fig.3; Ex.2028 ¶¶81. A POSITA would not be motivated to use Dong's 2D methods in a 3D NAND context because NLSB already addresses the X, Y, and XY modes. Ex.2028 ¶¶80-83.

B. No Reasonable Expectation of Success

Petitioner did not address reasonable expectation of success in the Petition; doing so for the first time on Reply is improper. *3Shape A/S v. Align Tech., Inc.*, IPR2019-00150, Paper 43, 41-42 (June 17, 2020); *see* POR 49-50. Petitioner still fails to address why a POSITA would have a reasonable expectation of success in applying Dong's 2D NAND program disturb methods in a vertical 3D NAND context.⁷ *See* Reply 24-25; Ex.2028 ¶¶201-206.

IV. GROUND 3 (Claims 8-9)

If the Board adopts PO's construction of "a program operation," it need not reach these arguments which assume adoption of Petitioner's construction.

A. Petitioner's New Mappings Do Not Disclose The Recited "Levels" Of "The First Voltage"

Rather than defend the mappings in the Petition, Petitioner shifts to new ones, despite Petitioner's expert testifying he was not aware of any:

⁷ PO never argued that obviousness should be assessed at Dong's filing date instead of the critical date. *See* Reply 24.

Q. Sitting here today, are you aware of any other mappings to satisfy Claim 5?

A. Not at the moment, no.

Liu-Dep1, 64:19-65:7, 67:2-19 (cl. 1).

The Petition defined the claimed variables as $k=2$, $m=7$, and $x=4$ to address claims 5 and 7. Pet.33. The Reply improperly provides new mappings with $k=16$, $x=20$, and $m=32$ (Reply 28), as well as $k=16$, $x=29$, $m=24$, and $n=32$ (*id.* 30). *See also* Ex.1089 ¶¶91-96 (new mappings). These new mappings and arguments are forfeited, as are the unidentified “other examples” Petitioner references. *Intelligent Bio-Systems*, 821 F.3d at 1369. Moreover, Petitioner’s new mappings are deficient in their own right.

Petitioner’s new mapping for claim 9, which allegedly “satisfies ***all*** conditions of claims 5 and 9” (Reply 26-29), fails because it shows a “first voltage” (V_{PASS} “per Dong Fig. 5a”) having ***identical*** “first” and “second” levels regardless of location of the x th wordline (i.e., $V1 (V_{PASS})$ in red identical to $V1 (V_{PASS})$ in blue). *Id.* 26-28.

Similarly, Petitioner’s new mapping for claim 8, which allegedly “satisfies all conditions of claim 8 (and base claims 5 and 7)” (*id.* 29), similarly fails because it also discloses the “first voltage” (V_{PASS} of “Dong, Fig. 5a”) having ***identical*** “first,” “second,” and “third” levels (i.e., $V1 (V_{PASS})$ in red, blue, and green are identical). *See* Reply 29-30; Ex.1001, 3:35-41, 3:63-4:5.

B. Petitioner's New Costa Mapping Contradicts the Petition and Fails To Disclose "First Voltage" Limitations

The Reply now argues that Costa's verify-phase V_{PASS} satisfies the recited "first voltage." *See* Reply 31-33 (ignoring claim 9). That theory is not in the Petition. Pet.38-39, 76. The Petition mapped Dong's charge-injection V_{PASS} to this limitation, foreclosing substitution of Costa's distinct verify-phase V_{PASS} for claims 8-9. *Id.*; Liu-Dep2, 39:22-40:13; POR 59-60, 64-65. Moreover, Petitioner fails to explain, much less map, how Costa discloses the base "first voltage" requirement in claim 5, for example. Even if Costa's verify-phase solution were combined to "improve Dong's *verification* phase" (Reply 33 (original emphasis)), that does not cure the Petition's failure. POR 65-66; Dong [0133] ("boost voltages are not applied" during verify).

Even if Petitioner could switch between Dong's charge-injection V_{PASS} and Costa's distinct verify-phase V_{PASS} (it cannot), the new position fails. Petitioner points to Costa's disclosure that "[d]uring sensing, a selected memory cell receives a reference voltage *while the remaining memory cells* receive a read or verify pass voltage"—i.e., read V_{PASS} from the first wordline up to an *(x-1)th* wordline. Costa (Ex.1012), Abstract, Figs.9A-9B, ¶¶98, 105, 115; Pet.75-76 ("simple example"); POR 60-61; Ex.2028 ¶¶233-235. But the claims require applying "a first voltage to the first word line to an *(x-2)th* word line" and "a second voltage to an *(x-1)th* word line."

Petitioner also fails on motivation to combine. *See* Reply 32. Petitioner still fails to address how or why a POSITA would modify Dong's already-existing verify process. *See* POR 65-66. Mere compatibility of references is insufficient. *Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993 (Fed. Cir. 2017). To the extent Petitioner argues that Dong's charge-injection voltages (e.g., V_{PASS} identified for "first voltage"; Pet.38-39) are modified according to Costa's verify-phase disclosures (Reply 31-33), Petitioner provides no motivation to combine—a point Petitioner ignores. *See* POR 59-65; Pet.73-76.

V. GROUND 4 (Claims 4, 10, and 14)

A. The Petition's Application Of " $V_{\text{PASS-LOW}}$ " To Shirai's Lower Deck Increases Program Disturb And Contradicts Dong

The Petition addressed claims 4 and 14 by equating Dong's "second portion" (Fig.5g)—which receives $V_{\text{PASS-LOW}}$ —with Shirai's lower memory deck (Deck 100a), as confirmed by Petitioner's expert. Pet.80-83 (citing "[1.B]"); POR 66-68; Liu-Dep1, 184:6-185:2, 185:11-186:13, 167:1-7, 178:7-179:17. Petitioner argues that it never proposed omitting V_{ISO} or V_{LOW} (Reply 34), but that is a direct consequence of its mapping.

The Reply's attempt to reframe this as consistent with "gradual" reduction fails. *See id.* Dong discloses reducing program disturb "by gradually reducing the bias voltage" on wordlines "between the selected word line and the V_{ISO} wordline," which Petitioner omits in its combination. *See* Dong [0057]. Petitioner fails to

address, much less rebut, the real issue: a POSITA would not apply $V_{\text{PASS-LOW}}$ as Petitioner suggests, without further gradual reduction through V_{LOW} and V_{ISO} contemplated by Dong, because it reduces boosting in the channel and increases program disturb. POR 69-70; Ex.2028 ¶¶252-259.

B. Petitioner's New "Second Portion" Mappings Contradict The Petition And Fail On The Merits

Petitioner argues it cannot be limited by its Petition under the guise of "exemplary" mappings and "bodily incorporation." Reply 34-35; Ex.1089 ¶114 (unidentified "numerous *additional* examples of mappings" meet the claims).⁸ But the Petition guides this proceeding. *Acceleration Bay, LLC v. Activision Blizzard Inc.*, 908 F.3d 765, 775 (Fed. Cir. 2018). The Board should disregard Petitioner's new mappings as improper and untimely. *Id.*; see Reply 35-37; Ex.1089 ¶¶106-114; Liu-Dep1, 64:19-65:7 (cl. 5), 67:2-19 (cl. 1). Even if considered, Petitioner's new mappings fail on the merits.

First, Petitioner and its expert provide no motivation to support why a POSITA would make the modifications shown in the two new mappings. Reply 35-37; see POR 73. Petitioner does not even reference the alleged motivation regarding

⁸ Petitioner errs in citing PO's expert testimony (Reply 35), which recognizes Dong's Figure 5g does not limit the number of wordlines. Ex.1094, 231:19-233:19.

Dong and Shirai in the Petition. Reply 33-37. Petitioner instead relies on hindsight to try to backfill failures in the Petition.

Second, Petitioner's assertion that Dong "expressly discloses applying $V_{\text{PASS-LOW}}$ precisely as claimed (*viz.*, to the second portion)" is incorrect. *Id.* 36. According to the Petition, Dong's Figure 5g shows applying V_{LOW} to WL8 and $V_{\text{PASS-LOW}}$ to WL9. Pet.50; Dong, Fig.5g. But in Petitioner's new multi-wordline "second portion" mapping, Petitioner applies $V_{\text{PASS-LOW}}$ to both WL8 and WL9. Reply 36.

Third, Petitioner's multi-wordline mapping fails to explain why it would modify Figure 5g's voltage application for WL8 of V_{LOW} to $V_{\text{PASS-LOW}}$, and for "WL n -8" of V_{PASS} to $V_{\text{PASS-LOW}}$ (WL4 in new mapping). *See* Pet.51; Reply 36. It also contradicts the Petition's identified variables. *E.g.*, compare Pet.53 (k=9), with Reply 36 (k=8).

Fourth, Petitioner's new variable assignments for claims 4 and 14 contradict the Petition's assignments for these claims, where, for example, Petitioner identified k=0 for claim 4 (not k=9 or k=8 as in new mappings). POR 71-72. There's no "double standard" (Reply 37) here—the Reply cannot cure the Petition's failure to map with particularity each claimed element to cited references.⁹

⁹ *In re Paulsen* is inapposite (Reply 37) as the '941 patent describes vertically arranged wordlines but Dong does not. 30 F.3d 1475, 1481, 1483 (Fed. Cir. 1994).

C. Petitioner Still Fails To Provide Claim-Specific Analysis For Claim 10

Petitioner still does not provide a claim-specific analysis for claim 10. Petitioner says claim 10 is met for the same reasons as claims 4 and 14, but those are Figure 5g-based theories. Reply 37-38. Claim 10 depends on claim 5 and requires Figure 5a-based analysis, which the Petition never provided.¹⁰ POR 71-72. Nor did Petitioner address the change in “k” from claim 5 to claim 10. POR 72.

VI. Conclusion

The Board should confirm patentability.

Respectfully submitted,

Dated: March 23, 2026

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¹⁰ If the Board considers Petitioner's arguments for claims 4/14 to apply to claim 10, they fail for the reasons in §V.A, §V.B, and POR 66-70.

CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Sur-Reply complies with the word count limitation of 37 C.F.R. § 42.24(c)(4) because the Patent Owner's Sur-Reply contains 5,598 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Sur-Reply exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 23rd day of March, 2026, a true and correct copy of the foregoing **Patent Owner's Sur-Reply and Exhibit 2030** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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