

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No. IPR2025-00190
U.S. Patent No. 11,568,941
Issue Date: January 31, 2023

REMOTE DEPOSITION

Tuesday, March 17, 2026

CROSS-EXAMINATION

DAVID KUAN-YU LIU, Ph.D.

1 Remote Cross-Examination of Dr. David Kuan-Yu
2 Liu, a witness herein, called for examination by counsel
3 for Patent Owner in the above-entitled matter, pursuant to
4 notice, the witness being duly sworn by SUSAN L. CIMINELLI,
5 CRR, RPR, a Notary Public in and for the District of
6 Columbia, taken remotely, commencing at 9:56 a.m.

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1 APPEARANCES:

2 On behalf of the Patent Owner:

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16 ALSO PRESENT:

17 Dr. Sunil Khatri

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1 C O N T E N T S

2 DAVID KUAN-YU LIU, Ph.D.

3 EXAMINATION PAGE NO.

4 By Mr. Lowry 5

5

6 E X H I B I T S

7 LIU EXHIBIT NO. PAGE NO.

8 1 - VLSI Technology Digest of Technical
9 Papers 2007 VLSI 4910 2 - Bit Cost Scalable Technology with Punch
11 and Plug Process for Ultra High Density
12 Flash Memory/IEEE Conference Publication
13 IEEE Xplore 59

14

15 (Previously marked exhibits referred to.)

16 EXHIBIT NO. PAGE NO.

17 1089 8

18 2012 17

19 2015 22

20 1009 45

21 1075 48

22

23

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1 P R O C E E D I N G S

2 Whereupon,

3 DAVID KUAN-YU LIU, Ph.D.

4 was called as a witness, and having been duly sworn, was
5 examined and testified as follows:

6 MR. LOWRY: Let's start with appearances. My
7 name is Rich Lowry, on behalf of Patent Owner YMTC, and I
8 am from the law firm Latham and Watkins.

9 MR. JENSEN: This is Travis Jensen from Orrick,
10 Herrington & Sutcliffe, representing the Petitioner Micron.
11 And I think later in the morning will be joining, my
12 colleague, Shane Andersson, also from Orrick, on behalf of
13 Petitioner.

14 CROSS-EXAMINATION

15 BY MR. LOWRY:

16 Q Good morning, Dr. Liu. Nice to see you again.

17 A **Good morning. Nice to see you again.**

18 Q Can you please state your full name for the
19 record?

20 A **Yes, my full name is David Kuan-Yu Liu, and**
21 **that's spelled K-u-a-n, Y-u, and the last name is L-i-u.**

22 Q And can you please state your home address for
23 the record?

24 A **I believe the last -- I believe during the last**
25 **deposition, I stated I have relocated to Arlington,**

1 **Virginia due to my wife's work situation. So I'm in 2055**
2 **15th Street, North Arlington, Virginia. Zip code is 22201.**

3 Q And where are you right now?

4 A **I'm right now in my apartment. I have a little**
5 **space where I can be isolated and then do this and be**
6 **deposed. Yes.**

7 Q Okay. I know we talked about this last time,
8 but I'm just going to go through some of the ground rules
9 very briefly to just refresh your recollection, if that's
10 okay with you. Do you understand your testimony today is
11 under oath and under penalty of perjury?

12 A **Yes, I do.**

13 Q And you understand you're under the same
14 obligation to tell the truth as if you were testifying
15 before a judge and jury?

16 A **Yes, I do.**

17 Q And like last time, we have a court reporter
18 here, and it's important that she be able to transcribe our
19 answers. So can you please try to provide verbal answers
20 to my questions?

21 A **Yes, I will try.**

22 Q Okay. And if you don't understand or are
23 confused by any question, please let me know, and I can try
24 to rephrase it, okay?

25 A **Okay. Yes, sounds good.**

1 Q And your attorney may state an objection to the
2 form of some questions, but unless your attorney instructs
3 you not to answer, you still need to answer the questions.
4 Do you understand?

5 A **Yes, I do.**

6 Q Okay. And during the deposition, you're not to
7 communicate with your counsel while we are on the record.
8 This includes verbal and nonverbal cues as well as any
9 electronic means. Do you understand that?

10 A **Yes, I do.**

11 Q Any reason you cannot provide full and truthful
12 testimony today?

13 A **No.**

14 Q Just for housekeeping, any time I reference this
15 case or this IPR or this proceeding, I'm referring to
16 IPR2025-00190 regarding the '941 patent, okay?

17 A **Okay.**

18 Q Okay. Based on what I can see, it doesn't look
19 like you have any materials in front of you, is that
20 correct?

21 A **No, I don't. I actually made a point to close**
22 **all the files and everything. Now they are just blank and**
23 **I will rely on you to download any document that we may**
24 **be -- or exhibit that we may be using.**

25 Q Okay. And there is no one else in the room with

1 you?

2 A No, but I do -- I do have my black cat with me.

3 Q Did you say your cat?

4 **A** **Yes, my cat is with me.**

5 Q That's fine. And do you have your cell phone in
6 front of you?

7 A No, cell phone is not in front of me. It's on
8 the bed by -- far away from me now.

9 Q Okay. Let's talk about your declaration. I'm
10 going to go ahead and drop it in the chat. One second,
11 please. I've dropped into the chat, Exhibit 1089, which is
12 Dr. Liu's reply declaration.

13 (Exhibit No. 1089 was referred
14 to.)

15 THE WITNESS: Due to the weather, my Internet
16 here has been very flaky, so I hope I can download it
17 quickly.

18 BY MR. LOWRY:

19 Q Okay. Well, while it's downloading, I think I
20 have some questions that I don't believe you need your
21 declaration for.

22 **A** **Okay.**

23 Q Since you signed your second declaration,
24 Exhibit 1089, that you submitted in this IPR, have you
25 changed any of your opinions?

1 **A No, I have not.**

2 **Q Have you formed any new opinions since you**
3 **submitted your second declaration, Exhibit 1089?**

4 **A Can you please clarify your question, please?**

5 **Q Yes. Have you formed any new opinions that are**
6 **not expressed in Exhibit 2089 since you submitted your**
7 **second declaration, Exhibit 1089?**

8 **A I'm sorry, for some reason, my -- my video is**
9 **not -- it's not doing it correctly. Hang on a second. I**
10 **should mention that the -- the reply declaration is fully**
11 **the opinion I'm representing. But there are other opinions**
12 **which I have not put in there.**

13 **And so my declaration, I think, indicated that**
14 **I'm not trying to address every opinion. So to that**
15 **extent, I do have opinions consistent with what I have said**
16 **all throughout my initial declaration, as well as second**
17 **declaration. So I don't -- I don't know the definition of**
18 **new opinion.**

19 **But there are -- I mean, I should just say that**
20 **the reply declaration is not all-inclusive of my opinions.**
21 **I do not put all the opinions I need to put down in there.**
22 **I'm only addressing the critical points that I need to**
23 **make. I'm not sure if that answers your question.**

24 **Q Well, let me ask this another way. Is the**
25 **extent of your opinions in this proceeding encapsulated in**

1 your first and second declarations?

2 A I believe so. To the extent that it is
3 necessary to address the issue, yes, I believe so.

4 Q Okay.

5 A And just for any opinion that will be in any way
6 contradictory to my declaration, I'm just trying to say
7 that the declaration -- the two declarations are not
8 all-inclusive. Obviously, nothing can be all-inclusive of
9 all the opinions. But you don't try to put everything
10 down, of course.

11 Q Okay. And do you have any edits or errors you'd
12 like to address in your second declaration regarding
13 supporting the reply?

14 A There was something very minor, which I
15 overlooked, and reading it in the context, perhaps I -- it
16 was very minor, very benign. Basically, I put down
17 Petitioner, and in fact, it should be Patent Owner, so that
18 was it.

19 Q Are you able to download the reply declaration?

20 A Yes, it just came up. It just came up.

21 Q Okay, great. Can you point me to where that
22 minor error was?

23 A Yes. Let me take a look at it. I believe -- I
24 believe it's on paragraph 24. The second line of paragraph
25 24. I believe when I was trying to refer to Exhibit 2011,

1 **2022, where these exhibits, I believe by Patent Owner**
2 **regarding certain U-shaped -- and I'm trying to say that**
3 **Patent Owner's reliance on these references is misplaced.**
4 **I believe that's the only -- that's something I noticed.**

5 Q Okay. Anything else?

6 A **I believe that's it.**

7 Q Can we go to paragraph 103 of your declaration,
8 please?

9 A **Sure. Counsel, I'd like to mention that because**
10 **my computer is being very, very -- acting very strange,**
11 **sometimes the video might go out. I just want to point out**
12 **that that's -- and I'll try to get it back right away.**
13 **That's in no way I'm trying to not show my face or show**
14 **disrespect.**

15 **It's just that sometimes it's very flaky and it**
16 **tends to go out, so I just want to let you know. And I'm**
17 **not trying to show any disrespect. It's just the nature of**
18 **my laptop right now.**

19 Q Understood, Dr. Liu. That shouldn't be a
20 problem. Thank you for letting me know.

21 A **You said 103, right?**

22 Q Yes, sir.

23 A **I'm there.**

24 Q Here in the first sentence of paragraph 103, you
25 stated, Petitioner combined Costa with Dong for the express

1 purpose of Costa's Vpass disclosure (Vpass increases as
2 programming proceeds to counter increased channel
3 resistance), which applies to the verify pulses (shown in
4 blue in Dong figure 20 above) of Dong's programming
5 operation. Do you see that?

6 **A Yes, I do.**

7 **Q** Here you say that the verify pulses are shown in
8 blue in Dong's figure 20 above, right?

9 **A Yes. Just -- verified pulses showing blue.**
10 **Hold on a second. That might be the voltage that's**
11 **applying to the selective word line during the very final**
12 **step should be in red, and the voltage applying to**
13 **selective word line during programming should be in blue.**

14 **Q** So did you mean to refer to the verify pulses as
15 shown in red in Dong's figure 20 above, instead of what was
16 written, which says shown in blue?

17 **A I think regardless of the color, and I think the**
18 **Dong's figures speak very clear for itself. In the**
19 **programming operation is incremental ISPP. Therefore, you**
20 **have the -- obviously, this figure 20 is showing the**
21 **voltage as being applied on the selective word line, so you**
22 **have incremental programming.**

23 **In between, you verify whether the voltage of**
24 **the selected memory style has achieved the special voltage.**
25 **And then if not, you keep on going until you have reached**

1 the proper threshold voltage.

2 And of course, figure 20 is showing the --
3 trying to convey that the programming operation consists of
4 the complete programming operation for giving selective
5 word line consists of programming pulses followed by
6 verification pulses, and then additional programming pulses
7 followed by verification pulses.

8 And of course, the selective word line
9 throughout this whole unique step of programming, you will
10 have pass voltage for both the programming phase, as well
11 as the verification phase.

12 Q Dr. Liu, you said that throughout the whole
13 unique step of programming, you will have pass voltage for
14 both the programming phase, as well as the verification
15 phase, right?

16 A That's correct.

17 Q And are you saying that the pass voltage applied
18 in the programming phase is the same voltage as the pass
19 voltage applied in the verification phase?

20 A I did not say that. I said that, in general,
21 for both programming phase and the verification phase of
22 the programming operation, you need to have pass voltage.
23 There is nothing prohibiting them from being the same. Or
24 for certain cases, they could be different. It's strictly
25 just pass voltage to program and verify. They could be the

1 same. They could be slightly different.

2 There is no restriction. And I think the -- in
3 both cases, these are pass voltage, and you need to
4 carefully engineer them during the whole programming
5 operation to avoid pass voltage disturbs and also program
6 disturbs.

7 Q Okay. So just circling back to my question,
8 which is much more simpler than that, because it appears
9 that there could be a typo in paragraph 103. So what I'm
10 asking is, when you reference the verify pulses, and then
11 you say that they are shown in blue in Dong figure 20, did
12 you mean that? Did you intend that the verify pulses
13 should be shown in red?

14 A Again, the point I'm trying to make is that
15 whether there is a typo, or for example, I clearly said
16 that in paragraph 99. It says, a program operation
17 includes voltage charge injection pulse 2005, 2020 in blue,
18 and the verified pulses 2006 being red.

19 So I think -- I think in the context, I'm not
20 sure that the -- I don't want to parse this language here.
21 But it's very clear, even if it's a typo, I don't think I'm
22 misrepresenting anything. I think it simply just means
23 that the program operation has both programming phase,
24 which is charge injection and a verification phase.

25 And a program operation is not complete unless

1 you have both of these. And I think that's also shown in
2 other -- other reference. But I think that it may be that
3 the blue shown in paragraph 103 may be -- may be a typo in
4 red, but I think I said it very clearly in paragraph 99.

5 And there is no dispute that you have the whole
6 pulse trained for the program operation. You have the blue
7 which is the programming pulse on the selective word line.
8 And then you have the red, which are verification, in case
9 you have multilevel verification pulses in red doing that
10 program operation.

11 Q Okay, Dr. Liu. So if you could, and I'm not
12 implying you're misrepresenting anything. All I'm trying
13 to understand is, is this a typo, an accident that we can
14 fix right now? Should it say shown in red in Dong figure
15 20 above in paragraph 103?

16 A It should be, yes, have it shown in red. But I
17 think reading the totality in the context of paragraph 99,
18 I think that's already very clear. And I'm not trying to
19 avoid your question.

20 But looking at this, I don't want to read the
21 sentence very quickly that perhaps they should be showing
22 red, they should be in red if we are referring to the
23 verify pulses part of the program operation.

24 But I think it's clear that in paragraph 99, I
25 actually explain the red and blue, and explain it very

1 well. So perhaps this right here is a mistake and I have
2 to review it after this. I think, in retrospect, it could
3 be a mistake. It could be it should have been red, yes.

4 Q Can we go to paragraph 6 of your reply
5 declaration, Exhibit 1089?

6 A Okay.

7 Q Do you see the last sentence where you say, even
8 a U-shaped 3D NAND string would have a source terminal and
9 drain terminal, and programming would necessarily proceed
10 from one terminal end to the other terminal end, and not
11 from the location closest to the substrate. Do you see
12 that?

13 A Yes, I do.

14 Q Can we go to paragraph 24 of your declaration,
15 please? Your second declaration. In the last sentence of
16 paragraph 24, you stated, a POSITA would not understand
17 that the '941 patent claims to exclude U-shaped 3D memory.
18 Do you see that?

19 A Yes, I do.

20 Q And now early in this paragraph, do you see
21 where you cite Exhibit 2012?

22 A Yes.

23 Q And you reference figure 8 of Exhibit 2012 as a
24 U-shaped 3D NAND string, right?

25 A Would it be helpful to upload the reference,

17

1 because I don't have it with me. I would like to take a
2 look at it.

3 Q I'm happy to upload the reference and I'll do
4 that right now, Dr. Liu. If you could answer the pending
5 question, which I can repeat if it's helpful --

6 A Yes, please repeat your question again.

7 Q In paragraph 24, you reference figure 8 of
8 Exhibit 2012 as a U-shaped 3D NAND string, right?

9 A That's what the declaration says, yes.

10 Q I'm uploading Exhibit 2012.

11 (Exhibit No. 2012 was referred
12 to.)

13 BY MR. LOWRY:

14 0 Please let me know when you have it uploaded.

15 A I've opened it. I'm going to figure 8.

16 Q Okay, great. In figure 8, do you see the box on
17 the top left marked SL?

18 **A** **Yes, I do.**

19 Q And that box represents the source line, right?

20 A I believe so.

21 Q And do you see the box in the top right that is
22 identified by BL?

23 **A** **Yes, I do.**

24 Q And BL means bit line, right?

25 A I believe so.

1 Q In this U-shaped NAND string shown in figure 8,
2 the phrase from bottom-to-top means from source to drain,
3 in your opinion, right?

4 A **Repeat your question again?**

5 Q Yes. In this U-shaped NAND string shown in
6 figure 8, the phrase from bottom-to-top means from source
7 to drain, in your opinion, correct?

8 MR. JENSEN: Object to form.

9 THE WITNESS: In the context of programming,
10 from bottom-to-top, that's my petition says, right? So you
11 would still have to program in the sequence.

12 BY MR. LOWRY:

13 Q Doctor, I think you added a qualifier regarding
14 in the context of programming. My question is more simple
15 than that. In this figure 8 of Exhibit 2012, is it your
16 opinion that the phrase from bottom-to-top means from
17 source to drain?

18 MR. JENSEN: Object to form.

19 THE WITNESS: If you read my opinion in totality
20 in the context, and from bottom-to-top even in the
21 dictionary definition is that you have to have a reference.
22 It's not strictly -- it's not strictly, for example, with
23 respect to a substrate. That doesn't make sense, because
24 in this example of a U-shape simply says from
25 bottom-to-top.

1 If it's not read in the context of going from
2 one end of the string to the other end of the string, then
3 the bottom-to-top would lose its meaning or lose its
4 reference point.

5 So in the context of '941 and as supported by
6 Webster's Dictionary, which Patent Owners have provided, it
7 does not necessarily know a vertical -- a vertical type of
8 a sequence, but rather, it denotes a reference point from
9 one end of the memory string to the other end of the memory
10 string.

11 And this reference is simply an illustration
12 that if you try to program from bottom-to-top, you have
13 this U-shape. And then if it's strictly bound, you lose
14 its meaning, because the word line, obviously, you are
15 coming to two cells. So it really doesn't make sense.

16 So the context from bottom-to-top really is with
17 respect to a reference from the source to drain. And
18 source to drain, the reason that we use source and drain,
19 because that's the most common way of programming.

20 I can go into detail on why going from drain to
21 source would not make as much sense. But again, if you
22 look at my declaration in its totality, from bottom-to-top
23 will only have very meaningful -- will have meaning if it's
24 from one reference point to the next reference point --
25 from one reference point beginning to the other end.

1 BY MR. LOWRY:

2 Q Okay. So is it your opinion that figure 8 -- in
3 the context of figure 8, the phrase from bottom-to-top
4 means from the source reference point to the drain
5 reference point?

6 A Again, I just want my viewpoint to be taken in
7 the proper context. I'm trying to provide an example.
8 Certainly the '941 patent does not exclude 3D implemented
9 in terms of U-shape. And all I'm saying is if you
10 interpret '941 from bottom-to-top strictly with respect to
11 a vertical, as the Patent Owner is trying to opine from the
12 substrate, which is substrate and then go all the way to
13 the top, then in our case, this U-shaped thing would not
14 apply.

15 But certainly '941 does not exclude this
16 U-shaped structure. So in order to interpret from
17 bottom-to-top, especially in the context of programming,
18 from bottom-to-top, you would have to have a reference
19 point. And going from one reference, using that reference
20 point to facilitate your programming and finish your
21 programming. That string could be U-shaped or it vertical,
22 or it could be horizontal. It could be 2D. It doesn't
23 matter.

24 It's a reference point from the bottom-to-top.
25 So from the reference point of bottom, and as you -- we

1 cite examples based on the Webster's Dictionary that top of
2 the key, or bottom of the key for rebound, shows a
3 three-pointer in the basketball sense, obviously nobody is
4 going to argue that you are playing basketball in the
5 vertical direction. You're actually playing basketball in
6 the planar direction.

7 But the bottom key is with respect to a
8 reference. Therefore, saying in the context of '941, if
9 you want to have from the bottom to top, you have to have a
10 reference point. And you have to go from that reference
11 point to facilitate and finish your programming.

12 And a POSITA would know, generally, that is the
13 sequence of programming is from source to drain. Of
14 course, there are some cases that may go from drain to
15 source, but a POSITA seeing that, right away would know
16 from source to drain, unless you specify from drain to
17 source, because drain to source has its own set of issues,
18 though.

19 Q Let's go to paragraph 25 of your declaration.
20 And here in the first sentence, you stated, as noted above,
21 and confirmed by Patent Owner's dictionary, bottom and top
22 are relative terms. Do you see that?

23 A Yes, I do.

24 Q And then the next sentence, you say, a POSITA
25 would understand that the reference point or the source and

1 the drain as demonstrated by numerous references, correct?

2 **A That's what I put down there, yes. Correct.**

3 Q And then the next sentence, you state, Patent
4 Owner does not dispute that some references, in
5 parentheses, including 2D NAND references, end paren, use
6 the source/drain memory string nomenclature, right?

7 **A That's correct.**

8 Q And then you cite POR, Patent Owner's Response,
9 at page 25, right?

10 **A Yes, that's what is written there.**

11 Q Okay. Let's take a look at Exhibit 2015, which
12 I'll represent to you is cited in the POR at page 25. I'll
13 drop it into the chat now.

14 **A Okay.**

15 **(Exhibit No. 2015 was referred**
16 **to.)**

17 THE WITNESS: You might have dropped the wrong
18 one. You dropped a patent application by Lee.

19 BY MR. LOWRY:

20 Q Let me check. I believe this is the right one.
21 Can you turn to figure 2 of Exhibit 2015, please?

22 **A I'm there.**

23 Q In this figure on the left, do you see the
24 letters SSL on the top left?

25 **A Yes, I do.**

1 Q And SSL refers to the source, right?

2 A **Generally referred to source select line, yes,**
3 **that's correct.**

4 Q And on the bottom left of this figure, do you
5 see the letters DSL?

6 A **Yes, I do.**

7 Q And DSL refers to the drain select line,
8 correct?

9 A **Yes, that's correct.**

10 Q Now, in this NAND string shown in figure 2, the
11 phrase from bottom-to-top, in your opinion, means from
12 source to drain, correct?

13 A **Can you repeat your question again?**

14 Q Of course. In this NAND string shown in figure
15 2, the phrase from bottom-to-top, in your opinion, means
16 from source to drain, correct?

17 A **Where did I opine that?**

18 Q Well, Dr. Liu, I'm just looking at your
19 construction as applied in your from bottom-to-top section,
20 including paragraph 25, where you state, a POSITA would
21 understand that the reference points are the source and
22 drain as demonstrated by numerous references. Do you see
23 that?

24 A **Yes, I do.**

25 Q And so I'm asking you, in this context, which is

1 a NAND string shown in figure 2, whether in this NAND
2 string, the phrase from bottom-to-top, as you interpret it,
3 means from source to drain?

4 MR. JENSEN: Object to form and scope. I don't
5 believe Exhibit 2015 is referenced in his declaration. You
6 can answer the question, but I'll make that objection.

7 THE WITNESS: I'd like to point out, there is
8 always a danger of taking things out of context. I also
9 qualify in paragraph 25 at the end. And I think we need to
10 go to that, and I would like to read it to you, if you
11 don't mind, is that whether a handful of references
12 deviated from the accepted convention has no bearing on
13 whether the '941 patent did so. It did not, as reflected
14 in the specification's silence on the topic.

15 I already was very forefront in mentioning that.
16 There are cases where -- I'm not sure in this case with
17 this 2015, how they program it. But looking at -- just
18 casually glancing and looking at the source in common, I
19 would be very -- I will have my opinion how they program.

20 But because it's not part of this, my
21 declaration, the point is that I did not say that there is
22 no one going from drain to source. But typically,
23 programming from drain to source is bottom-to-top, has its
24 own set of issues.

25 And in this case, the '941 patent is addressed

1 in a conventional way of mainstream, in which programming
2 from bottom-to-top is the conventional way to a POSITA from
3 source to drain. There are other cases due to other
4 reasons.

5 People program from, for example, drain to
6 source to perhaps deviate from the accepted convention. It
7 doesn't change the fact that convention, as I cite in
8 numerous references, is programming from source to drain.
9 Therefore, the context of '941 programming from
10 bottom-to-top is programming from source to drain.

11 I never said that there is no exception of
12 programming from drain to source. I'm simply saying that
13 these are exceptions that deviate from the accepted
14 convention. And I have a little footnote, I believe,
15 mentioning some of the drawbacks -- but it's not part of
16 this discussion, not part of '941. So I did not go into
17 detail.

18 But we could go a whole day to explain the merit
19 -- compare and contrast between programming from source to
20 drain and from drain to source. Again, taken in the
21 context of my paragraph 25, I'm simply saying that to a
22 POSITA, in the conventional, unless you mention the
23 deviation or mention special cases, to a POSITA,
24 programming from bottom-to-top simply will have to follow
25 the convention of programming from source to drain.

1 In terms of U-shape, which this conversation is
2 about is also programming from source to drain. It has to
3 program from a reference point to -- from a reference
4 point, includes the conventional source, all the way to the
5 drain. It has nothing to do with the physical level. It
6 has to do with a reference point. And that's the context
7 of my testimony and the context of my reply declaration.

8 BY MR. LOWRY:

9 Q Dr. Liu, can we go to paragraph 3 of your
10 declaration, please?

11 A **You said paragraph 3?**

12 Q Yes, sir. Do you see in this paragraph, you
13 said, I reviewed and considered the materials listed in my
14 opening declaration, the Board's institution decision,
15 Paper 22, POR Paper 33, and exhibits thereto, including the
16 Khatri declaration, the materials listed in Petitioner's
17 reply, and any other materials cited herein. Do you see
18 that?

19 A **Yes.**

20 Q Do you recognize that Exhibit 2015 was cited in
21 the POR and the Khatri declaration?

22 A **I do recall. Yes, it was. It's cited in the --**
23 **as far as guide and the -- and the other reference, Dong 2**
24 **references. Yes.**

25 Q So you reviewed and considered Exhibit 2015 when

1 forming your opinions in your second declaration, correct?

2 A I've taken that into consideration, yes. But I
3 did not -- I did not specifically cite that reference in
4 my -- in this reply declaration. I simply made a point
5 that there are exceptions.

6 And looking at that schematic, I don't want it
7 to be a memory test. I can take the time to review the
8 Exhibit 2015 to see, not just a figure, the source being
9 drawn on the -- on the top of the page versus the bit line.

10 So I have to go in and look at it, that physical
11 structure. And if you give me time, I can certainly go
12 through a quick review. Because this is not a memory test.
13 There is so many documents in this, so many exhibit in this
14 case.

15 So I would have to take a look at it. And I
16 should mention, based on my recollection, that's a
17 schematic. And I don't believe I've seen in that reference
18 that there is any -- any physical structure corresponding
19 to the schematic which is figure 2.

20 And sitting right here, I don't want to use my
21 recollection. I'm sorry, my -- I don't want to use my
22 recollection. I don't know the programming sequence. I
23 have to take a look at it as well.

24 Q Dr. Liu, is your construction for from
25 bottom-to-top as meaning from source to drain limited to

1 any physical structure?

2 **A Repeat that question again?**

3 Q Is your construction for from bottom-to-top as
4 meaning from source to drain limited to any physical
5 structure?

6 **A Is your question referring to what I mentioned**
7 **about physical structure?**

8 Q I'm asking you a different question. I'm asking
9 you if your construction for from bottom-to-top as meaning
10 from source to drain is limited to any physical structure.

11 **A Can you -- I think that question is too broad.**
12 **Can you parse it for me? I don't understand the question.**
13 **It's very broad.**

14 Q I can ask a more specific question. Is your
15 construction for from bottom-to-top as meaning from source
16 to drain limited to any specific physical arrangement of a
17 memory string?

18 **A If I understand your question correctly, and**
19 **please correct me if I don't, if I answer incorrectly.**
20 **From bottom-to-top, as the example I gave with the**
21 **basketball, certainly does not limit it to be a vertical**
22 **string.**

23 **I think the point -- that doesn't limit it to be**
24 **a vertical string. It could be a string that's actually**
25 **planar. And so from bottom-to-top is not restrictive.**

1 Again, when I construct -- construe from bottom-to-top as
2 source and drain, it's very clear in my declaration and the
3 prior declaration, that there are cases where it could be
4 programming from drain to source.

5 But those are exceptions. The conventional way,
6 when a POSITA sees from bottom-to-top, it does not
7 necessarily exclude a two-dimensional array. It does not
8 have to be a vertical main string. Although Dong's
9 teaching equally applied to 3D NAND string, but when you
10 ask me if it's excluded, my answer is, I don't know what
11 exclude -- that's very, very all-inclusive, or very
12 all-encompassing type of question.

13 But from bottom to top, all I can say is, it
14 does not exclude a planar implementation or a typical 3D
15 implementation. That's very common in 2020. They are not
16 excluded, if that's the question you're asking.

17 Q Let's go to paragraph 56 of your declaration.

18 A I'm there.

19 MR. JENSEN: Can you give me the paragraph
20 number again? I missed it.

21 MR. LOWRY: Paragraph 56.

22 MR. JENSEN: Thank you.

23 BY MR. LOWRY:

24 Q Dr. Liu, in the first sentence, you say, in
25 conclusion, in view of the well-developed state of 3D NAND

1 memory in 2020, a POSITA would at once envisage the '941
2 patent's claimed bottom-to-top word line arrangement upon
3 reading Dong's disclosure of three-dimensional NAND. Do
4 you see that?

5 A Yes, I do.

6 Q Do you see the phrase, at once envisage, in the
7 second line there?

8 A Yes, I do.

9 Q What did you mean by, at once envisage?

10 A The point is -- now, you are -- I don't want
11 things taken out of context, okay. The context with
12 paragraph 56 is not just from bottom-to-top all of a sudden
13 exists out of a vacuum.

14 I'm just saying that if when I read Dong, when
15 Dong mentioned the fact that his implementation applies to
16 -- I don't know the exact word, three-dimensional. And in
17 2020, when you talk about three-dimensional NAND flash,
18 right away, as you -- a POSITA would envision that it's a
19 vertical NAND stream. So that statement in paragraph 56 is
20 taken in the context of reading Dong and reading Dong 3D
21 NAND in 2020.

22 Right away, you will see that, then, the context
23 are from bottom-to-top would have a meaning that it's a
24 three-dimensional and vertically oriented memory string, as
25 opposed to stacking the planar type together as P0

1 **proposed.**

2 **No, because in 2020, if I were to read 3D NAND,**
3 **that's, right away, what I would envision. And if I**
4 **envisioned that from bottom-to-top in that case, you would**
5 **have to be applying to -- a summation would be viewing the**
6 **vertically oriented memory string in figure 5A and 5G.**

7 Q Dr. Liu, do you understand the at once envisage
8 standard that you applied in your declaration?

9 MR. JENSEN: Object to form.

10 THE WITNESS: I don't know if there is a
11 question there.

12 BY MR. LOWRY:

13 Q The question is -- and I'll just repeat exactly
14 what I said. Do you understand the at once envisage
15 standard that you applied in your declaration?

16 MR. JENSEN: Object to form. Asked and
17 answered.

18 THE WITNESS: I'm applying the standard of a
19 POSITA. And in 2020, if -- and I cite all these
20 numerous -- even a way of implementing a flash. If I were
21 to read the 3D NAND memory in 2020, and right away, the 3D
22 NAND -- the visual would be a vertical NAND stream, because
23 that's how it was commonly done.

24 And the POSITA right away would think of 3D NAND
25 string. It would not think, right away, go all the way, to

1 think of it as being a 2D stacked together. Because if you
2 look at -- even as much as when TC stacking even by the
3 time of before 2020, all the focus was on stacking a 3D
4 NAND, or developing 3D NAND string, at the most, stack it,
5 or put it into POSA, to put it with -- but the 3D NAND
6 definitely would convey to a POSITA that it's a vertical
7 NAND string.

8 BY MR. LOWRY:

9 Q Dr. Liu, I'm not asking you how you apply that
10 at once envisage in your declaration. I'm asking you what
11 is the at once envisage standard?

12 MR. JENSEN: Object to form. Asked and
13 answered.

14 THE WITNESS: I think I said it very clearly. A
15 POSITA, a POSITA -- a true POSITA at the time, in 2020, if
16 you mention 3D NAND, and I cite it with all the references
17 I have, in terms of how Micron is focusing on developing
18 a -- or BC is developing that, and how Samsung, Kioxia, all
19 these big NAND players in the 3D arena. They are simply
20 increasing the number of layers.

21 So a POSITA, a true POSITA at the time of 2020,
22 when the mention of 3D NAND, such as I am a POSITA, and I
23 would right away -- the thing that would come -- the visual
24 would come across my mind would be a 3D vertical NAND
25 string, as I mention here very clearly.

1 Q Dr. Liu, you're not answering my question, which
2 is not at all about how you're applying in your declaration
3 the -- when you say a POSITA would at once envisage the
4 '941 patent's claim bottom-to-top, I'm asking a completely
5 separate question apart from your application of the
6 standard, which is, what is the at once envisage standard?

7 MR. JENSEN: Object to form. Asked and
8 answered.

9 THE WITNESS: Again, my statement said clearly,
10 a POSITA -- and I'm opining a POSITA -- and I'm certainly
11 qualified as a POSITA. And I'm opining that a POSITA, upon
12 hearing 3D NAND in 2020, and not I alone, but if you look
13 at across all the citations I have of all the development
14 of the major -- I would say the top tier NAND 3D memory
15 offered, right away, you see a picture.

16 So I'm simply saying that as in the paragraph,
17 it says very clearly, a POSITA, such as I am, would at once
18 have a vision of that being a vertically -- I'm sorry,
19 oriented such as figure 5A, 5G was showing a vertically
20 oriented string.

21 BY MR. LOWRY:

22 Q Dr. Liu, what criteria must be met in order to
23 find invalidity under the at once envisage standard?

24 MR. JENSEN: Object to form. Asked and
25 answered.

1 THE WITNESS: I'm not sure I understand your
2 question. Are you trying to -- I'm never trying -- can you
3 please ask your question again? I don't understand your
4 question.

5 And I think, again, I'm just going to refer to
6 my -- it says very clearly, I don't know how else to say
7 it. A POSITA, such as I am, in 2020. We are talking about
8 2020. When he hit upon 3D NAND, across which -- I would
9 actually turn around and say that I don't think anybody
10 would -- I don't think I would be hard pressed to find
11 somebody who would think otherwise, who would disagree that
12 it would be a vertically oriented memory string, so -- and
13 I think that's my answer. And I think it's very clear in
14 that paragraph already.

15 BY MR. LOWRY:

16 Q Well, Dr. Liu, you're not responding to my
17 question. I'm not asking about what's in your paragraph.
18 I'm talking about the standard you applied. I'll repeat my
19 question. What conditions must be met in order to find
20 invalidity under the at once envisage standard?

21 MR. JENSEN: Object to form. Asked and answered
22 like five times.

23 THE WITNESS: I don't believe I opine on
24 invalidity. Can you point to me where I opine that? I
25 mean, I don't understand.

1 Again, I am simply applying the view of a
2 POSITA, such as I am, and with all my industry experience
3 and all my -- all the work I've done in the flash memory
4 space, and applying a survey of the literature which I've
5 shown, and applying the view of a POSITA when 3D NAND is
6 mentioned in 2020, the vision -- or the visual right away
7 is a vertically oriented string of memory cell. And I
8 think that's the statement I simply put down there. I
9 don't -- I think my statement in paragraph 56 is very
10 clear.

11 BY MR. LOWRY:

12 Q Dr. Liu, can you identify anywhere in your reply
13 declaration where you set forth your understanding of the
14 law regarding the at once envisage standard?

15 MR. JENSEN: Object to form.

16 THE WITNESS: Again, I think the answer is that
17 it is -- I'm opining here that a POSITA in 2020 -- and to
18 be sincere and genuine, and when -- when he or she reads
19 the context of 3D NAND memory in 2020, the vision -- the
20 visual will come to mind right away would be a vertically
21 oriented memory string.

22 And that's my statement. And I don't know if
23 you'll be genuine if you say that that's not the case. And
24 I don't know. I don't know if in the IPR process, in terms
25 of invalidity, I need to take your threshold. All I'm

1 simply saying is that it is meant that a POSITA reading
2 this would right away, what genuinely would come to mind
3 would be the 3D -- vertically oriented 3D memory string.

4 BY MR. LOWRY:

5 Q Pardon. Please finish your answer.

6 A **It's okay. Please. I'm opining from the**
7 **perspective of a POSITA, a person of ordinary skill in the**
8 **art.**

9 Q I understand that, Dr. Liu. And I'm not
10 questioning your status as a POSITA in this line of
11 questioning.

12 My question is, what -- what are the legal
13 bounds of the at once envisage standard?

14 MR. JENSEN: Object to form. Asked and
15 answered.

16 THE WITNESS: Again, the statement there is
17 simply that a POSITA in 2020, hitting upon 3D NAND, and a
18 sincere and genuine POSITA, in his view, right away would
19 come to the visual of a vertically oriented memory string.
20 And that's the statement I have in my -- in my -- in
21 paragraph 56 of my declaration. Sorry.

22 BY MR. LOWRY:

23 Q Please go ahead. Pardon me.

24 A **I was just going to say that I drank a lot of**
25 **coffee this morning, so when this line of questioning is**

1 **done, perhaps we can take a bio break. No problem.**

2 Q Sure we can, once we finish this line of
3 questioning. So sitting here today, Dr. Liu, you're unable
4 to identify what the legal standard is for at once
5 envisage, beyond what is stated in your paragraph 56 of
6 your declaration, correct?

7 MR. JENSEN: Object to form. Asked and
8 answered. Misstates testimony.

9 MR. LOWRY: Please limit your objection to
10 object to form, Mr. Jensen, as instructed by the Patent
11 Trial Practice Guide. Thank you.

12 MR. JENSEN: Please stop harassing the witness.
13 Thank you.

14 MR. LOWRY: I'm not harassing the witness. I am
15 asking different questions and I'll repeat my question due
16 to your interruption.

17 BY MR. LOWRY:

18 Q Dr. Liu, you're unable to identify what the
19 legal standard is for at once envisage, beyond what is
20 stated in paragraph 56 of your declaration, correct?

21 MR. JENSEN: Same objections.

22 THE WITNESS: Repeat your question again. I
23 don't understand the context of the question. Please. I'm
24 sorry.

25 BY MR. LOWRY:

1 Q Happy to repeat it. Dr. Liu, sitting here
2 today, you're unable to identify what the legal standard is
3 for at once envisage, beyond what is stated in your
4 paragraph 56 applying -- strike that.

5 Dr. Liu, sitting here today, you're unable to
6 identify what the legal standard is for at once envisage,
7 beyond the mention of the standard in your paragraph 56 of
8 your second declaration.

9 MR. JENSEN: Same objections.

10 THE WITNESS: I don't -- I don't know if that's
11 the right context to put it. I am asked to opine in this
12 case from the viewpoint of a POSITA. And I believe I did
13 that.

14 And that opinion stated in paragraph 56 is the
15 perspective of a POSITA. And I think that's to say that
16 I'm not able to, whatever, I don't know if I necessarily
17 agree with that. But be that as it may, I think that my
18 opinion, again, is stated clearly from the perspective of
19 POSITA, which I'm well qualified.

20 And if viewed from that lens, if in 2020, you
21 were to discuss with me a well developed state of 3D NAND
22 memory in 2020. And you mentioned 3D NAND, you mention
23 from bottom-to-top in the context -- in the context of 3D
24 NAND. Right away, the visual would be vertically oriented
25 memory string.

1 And it could be I don't know if you want to
2 throw in U-shaped or whatever. But the fact is that it's
3 going to be a vertically oriented memory string with, then,
4 many layers. And that's the view -- that's viewing it from
5 the lens of a POSITA, especially me as POSITA, having many
6 years working in the flash memory in a trench of battle,
7 fighting flash memory, improve flash memory, minimize
8 disturb, optimizing operation of the memory cell.

9 From that lens, as a POSITA, that's exactly the
10 statement right there. A POSITA will at once envision that
11 the claim from bottom-to-top in the context of 3D NAND to
12 be a vertically oriented memory string.

13 And I don't know how else I can answer any
14 differently. This is the -- this is the lens I'm viewing.
15 And to opine for this, for this declaration and for the
16 original declaration.

17 MR. LOWRY: Okay, Dr. Liu. Let's go off the
18 record for a quick break.

19 THE WITNESS: Thank you.

20 (Recess.)

21 BY MR. LOWRY:

22 Q Dr. Liu, can we go to paragraph 98 of your
23 declaration -- second declaration, please?

24 A Yes.

25 Q Do you see the first sentence, where you say,

1 Costa says the pass voltage that is applied, in brackets,
2 to unselected memory cells, end brackets, is dependent upon
3 the position of the selected memory cell, and that the pass
4 voltage of unselected cells closer to the source increases,
5 quote, as programming progresses from a memory cell at a
6 first end of a NAND string toward a memory cell at a second
7 end of the NAND string. Do you see that?

8 **A Yes, I do.**

9 Q Okay. And you cite Costa's abstract, right?

10 **A That's correct.**

11 Q Okay. So in the sentence, you're referring to
12 the pass voltage identified in Costa's abstract, right?

13 **A That's correct.**

14 Q Let's go to paragraph 99 of your declaration on
15 the next page. In this paragraph -- well, let's go to
16 paragraph 68. Scratch that. Paragraph 68. Are you there,
17 Dr. Liu?

18 **A 68, you said?**

19 Q Yes.

20 **A I just got there.**

21 Q Okay. And you see 68 spans from pages 42 to 43
22 of your second declaration.

23 **A I'm looking at page 42. I can get 43 open if**
24 **necessary.**

25 Q Let's go to page 43. Do you see the last

1 sentence in paragraph 68?

2 **A Yes, I do.**

3 Q It says, program disturb modes 1 and 2, in
4 addition to program disturb modes 3 and 4, all need to be
5 addressed in order to reliably operate a 3D NAND during
6 programming, right?

7 **A Yes, I see that.**

8 Q And that's because program disturb modes 1, 2,
9 3, and 4 all occur simultaneously in 3D NAND, right?

10 **A Repeat your question again?**

11 Q I said that's because program disturb modes 1,
12 2, 3, and 4 all occur simultaneously in 3D NAND, correct?

13 **A Can you define simultaneously? Did I use that**
14 **word, simultaneously, anywhere in this document?**

15 Q I'm asking you about your testimony in this
16 document, Dr. Liu. You said that -- you identified at
17 least four program disturb modes. And I'm asking you, they
18 occur simultaneously in 3D NAND, correct?

19 **A Again, I don't understand the context of**
20 **simultaneously. Program disturb mode, you have to worry**
21 **about doing programming or doing the actual injection phase**
22 **or verification phase. Now, that's into what is really**
23 **happening.**

24 **So you do have selected string for programming.**
25 **And you have unselected string in the X direction, and**

1 another one in the XY direction, and another one in the Y
2 direction.

3 The voltage you apply on them during the
4 program -- during the programming operation as a whole.
5 You've going to have pass voltage. And you're going to
6 have selective word line. And in such a case, that --
7 let's just take the injection phase for now, and you have
8 this thing going on. And you have boosting, and you have
9 everything that's happening. So any of these 1, 2, 3, 4
10 mode could be a source of disturb to the memory cell.

11 So when you say simultaneously, somehow it's
12 like they all are going up. You try to minimize each and
13 every one of them, and sometimes there is competing
14 mechanisms. So you're trying to optimize it. So I --

15 Q I understand.

16 A So I don't know how you qualify simultaneously.
17 So I don't understand. I don't want to -- I think I don't
18 have that word in there, so I don't know the context of
19 simultaneous. So I want to be very careful.

20 It's fair to say that row 1, row 2, row 3, row 4
21 all exist, and are potential sources of program disturb.
22 And you have to address each and every one of them. And
23 you cannot neglect any one of them, and assume that your
24 memory cell operation will be program disturb free, or pass
25 voltage disturb free, because '941 addressed both.

1 Q Dr. Liu, do you agree that in actual array
2 operation for 3D NAND, all three program disturb modes
3 occur simultaneously?

4 MR. JENSEN: Object to form.

5 THE WITNESS: I don't know why you all of a
6 sudden changed the word to all three. Because there are
7 four modes. 1, 2, 3, 4.

8 BY MR. LOWRY:

9 Q Okay. So do you agree that in actual array
10 operation for 3D NAND, the X mode, Y mode, and XY mode
11 occur simultaneously?

12 A Again, I'm not sure where the word
13 simultaneously comes from. These modes -- by that, you
14 mean that these modes are all sources of program disturb
15 and due to the bias -- this arra, and these forms of
16 program disturb exist.

17 And you're trying to minimize each one of them.
18 You cannot neglect any one of them. You try to minimize
19 each and every one of them. And that requires optimization
20 oftentimes.

21 And as you -- as my declaration cited, you could
22 go one way to try to address one to the extreme of where it
23 caused the other one to occur. So it's an optimization.
24 And to the fact that it was used simultaneously, I would
25 agree that these four modes are sources of program disturb.

1 But you bias the array for programming phase and for
2 verification phase.

3 Q Okay, Dr. Liu. So we are in agreement that
4 these four modes are sources of program disturb, right?

5 A In certain cases, it's program disturb, by --
6 program disturb, by that, it should encompass also pass
7 voltage disturb, because program and verification --
8 injection phase and verification phase inevitably require
9 pass voltage on the unselected word line.

10 So when you say program disturb, I would like to
11 say that it encompassed pass voltage -- so I don't have to
12 keep on repeating both of them. But program disturb should
13 encompass as voltage disturb, because when you program the
14 selected -- when you program and verify the selective word
15 line, selected memory cell, within the string, whether it's
16 X -- whether X mode, Y mode, XY mode, or actually one --
17 you do have pass voltage, and they are a source of overall
18 program disturb. Because it occurred during the
19 programming operation that encompassed both injection and
20 verification phase.

21 Q And, Dr. Liu, the four modes of program, the
22 four modes which are source -- let me strike that.

23 The four modes can be sources of program disturb
24 at the same time, right, in 3D NAND?

25 A You have to define at the same time. Because I

1 mean, same time means at one particular point. I don't
2 know what the same time means, because -- what do you mean
3 by, at the same time?

4 Q Let's look at part 2 of Aritome, which is
5 Exhibit 1009.

6 (Exhibit No. 1009 was referred
7 to.)

8 THE WITNESS: It's taking time. I think it's
9 going to be slow, based on the progress I'm seeing right
10 now. We are not even quite halfway through it, just to
11 give you an update. Almost there. There we go. I have
12 it.

13 BY MR. LOWRY:

14 Q Can we turn to page 364 of Exhibit 1009?

15 A So 364 -- you mean the bottom, not the 364 of
16 the file, right? The bottom?

17 Q Yes.

18 A The page labeled --

19 Q Yes, the stamp on the bottom right, where it
20 says, Micron Exhibit 1009, page 364.

21 A I'm there.

22 Q Okay. Do you see the last paragraph on this
23 page, starting with, in actual array operation?

24 A Okay.

25 Q Do you see that this reference, Aritome, states,

1 in actual array operation, all three program disturb modes
2 occur simultaneously. Do you see that?

3 A Yes, I do.

4 Q Do you disagree with that statement, Dr. Liu?

5 A I don't necessarily disagree with that. I'm
6 simply trying to say that these program disturb modes occur
7 during the array operation. And whether they occurred
8 simultaneously, at the same exact point in time, we can
9 have discussions on that. But they do occur.

10 Just, for example, don't drink and drive. It
11 doesn't mean that you're drinking and driving at the same
12 time. Just don't drink and drive. It doesn't have to
13 occur simultaneously to have the detrimental effect.

14 This is simply saying that during the program
15 operation, these mechanisms, when they say 3, this actually
16 turns out to be 4, of course. That's what you mentioned.

17 But these program disturb mechanisms occur, and
18 you have to deal with it. So I -- I don't necessarily --
19 if the simultaneously were to refer to the -- during the
20 operation occur. But to say some occurs at the exact same
21 snapshot in time, it may or may not. But it's fair to say
22 that regardless that these -- all these modes of operation,
23 all this disturb occurred during the program operation,
24 during the operation of the programming, which included --
25 encompasses injection and verification phase.

1 Q Dr. Liu, is it fair to say that these modes of
2 operation -- strike that.

3 Dr. Liu, is it fair to say that all three
4 program disturb modes occur during the charge injection
5 phase?

6 MR. JENSEN: Object to form.

7 THE WITNESS: Repeat your question again?

8 BY MR. LOWRY:

9 Q I said, is it fair to say that all three program
10 disturb modes occur during the charge injection phase?

11 MR. JENSEN: Object to form.

12 THE WITNESS: The program disturb mode would
13 have -- these disturb modes occur in program injection
14 phase, and also can occur in verification phase, because
15 you also have pass voltage in both programming phase and
16 verification phase.

17 BY MR. LOWRY:

18 Q Okay. Let's turn to paragraph 63 of your second
19 declaration, please.

20 A **I'm there.**

21 Q Okay. Here you state that the 2007 Tanaka
22 article, Exhibit 1075, discloses a vertical memory string
23 architecture for a 3D memory device. Do you see that?

24 A **Yes, I do.**

25 Q Let's take a look at Exhibit 1075.

1 (Exhibit No. 1075 was referred
2 to.)

3 BY MR. LOWRY:

4 Q I'm dropping it into the chat now.

5 A **I got it.**

6 Q Okay. Do you see the title at the top of page
7 1?

8 A **Yes, I do.**

9 Q It says, Bit Cost Scalable Technology with Punch
10 and Plug Process for Ultra High Density Flash Memory,
11 correct?

12 A **That's correct.**

13 Q And the first named author is H. Tanaka?

14 A **That's correct.**

15 Q Do you see the small text at the bottom right of
16 page 1?

17 A **Small text in bottom right.**

18 Q Do you see the text in the bottom right that
19 says, 2007 Symposium on VLSI Technology, Digest of
20 Technical Papers?

21 A **Yes, I do.**

22 Q And on the top of page 1, on the left, do you
23 see the 2-2?

24 A **Yes, I do.**

25 Q Do you know what that means?

1 **A Usually it means session 2, paper 2.**

2 Q I'm going to drop into the chat, what I'll mark
3 as Liu Exhibit 1.

4 (Liu Exhibit No. 1 was marked
5 for identification.)

6 BY MR. LOWRY:

7 Q Please let me know when you have it up, Dr. Liu.

8 **A Okay, I have it.**

9 Q Do you see the date at the top right of the
10 first page listed as June 12 to 14, 2007?

11 **A Yes, I do.**

12 Q Well, let's look at the contents on page 2. Do
13 you see on page 2, under contents, it says, Tuesday, June
14 12th?

15 MR. JENSEN: Object to form.

16 THE WITNESS: So let me -- et me just qualify
17 that a little bit. I don't know if you know how these
18 conferences work. VLSI Symposium along with IDEM are two
19 of the very well-known. And in order to get this paper
20 into the conference, you would have to submit your
21 manuscript at least -- at least, if not more than six
22 months ahead of time.

23 And then -- and then they will publish a
24 program. They will -- even before the conference, they
25 will advertise the program. They will advertise the

1 online. So by the time this paper published, I think you
2 would have come across to a lot of -- a lot of people in
3 the art. So I just want to qualify that a little bit.

4 BY MR. LOWRY:

5 Q Okay, Dr. Liu. Do you have any evidence or
6 anything you can point to in the record to support what you
7 just said?

8 A For example, for these conferences, such as IEDM
9 or VLSI, they were right before -- just use IEDM as an
10 example, which is actually the same.

11 So IEDM actually occurs -- these are two major
12 conferences. One occurred in December and one occurred in
13 the June timeframe. Usually, for example, for IEDM, you
14 would actually get a call for a paper well ahead. Like,
15 six to eight months ahead. You probably get called for a
16 paper by end of April already.

17 And then the paper would be selected around June
18 timeframe. And the program would actually already be
19 decided which paper will be presented. And then the actual
20 paper will be presented in December.

21 So there is a delay when the actual proceeding
22 or the -- or the proceedings published back. Generally
23 speaking, that paper already will be known, and the paper
24 to be published in that field. And that's how you attract
25 people to attend a conference. And VLSI Symposium is the

1 same.

2 But be that as it may, the point here, we are
3 trying to say is that people already working on 3D NAND.
4 And Tanaka is not the only reference we cited. And Tanaka
5 is very extensive, simply because it shows all the process
6 flow. And the process flow don't come out of a vacuum.
7 People have already -- for example, the way to make the
8 connection to the word line, you actually -- at that time,
9 it's actually very novel, and we actually knew about it.
10 Got very excited. It's called trim and -- rim and etch,
11 trim and etch.

12 So you actually -- each layer, you trim a little
13 bit of the resist pattern, and you etch it -- soon the
14 thing is exposed, and then you do it again. It's very
15 novel. It doesn't require photoresist step.

16 These things are well-known. And people have
17 done this. And of course, we have other Endohl reference
18 to show the vertically formed NAND string. The point is
19 saying, simply looking through the lens of 2020, 3D NAND in
20 terms of vertical string is nothing new.

21 In fact, it's taken for granted. And then in
22 2007 -- even in 2007, if I were to look as a POSITA working
23 in the field in 2007, I can also find references that point
24 to 3D NAND now being implemented by so-called stacked 2D,
25 but whether there are 3D NAND string in development as

1 early as 2001.

2 And Tanaka, this paper, a Japanese paper
3 following Endohl, it's just another manifestation of the
4 fact that 3D, in terms of vertical stream, is
5 well-pursued -- well-known and being pursued aggressively
6 at the time of 2007, whether you do four layers or eight
7 layers.

8 And in fact, the process step to implement how
9 to connect the word line, because you can obviously --- the
10 word line has to go. If you look at a graph of the -- bear
11 with me. If you look at the graph of the Tanaka, and you
12 see that the word line has to be connected horizontally
13 gradually.

14 That process, it turns out it's actually
15 happening in figure 8. That sequence is actually almost
16 like a major breakthrough. It turns out that people coined
17 the phrase that etching is the new lithography, because of
18 the way you are actually using -- they call it slimy, but
19 actually call it trimming process.

20 So it's fair to say that these things -- before
21 the date of publish, these things have gotten out, and have
22 gotten out to at least people in the field pursuing flash
23 memory, such as IM, have already gotten out.

24 And I just wanted to put that in the proper
25 context. Don't just look at a date and see June. Even

1 before June, there is a sequence involved, just like a
2 manuscript takes time to be peer-reviewed. It takes time
3 to decide which one to actually make it into their
4 conference and computer digest.

5 Q And, Dr. Liu, during these conferences, and
6 prior to these conferences, when there is a call for
7 papers, those papers are viewed with strict
8 confidentiality, is that correct?

9 A When you say strict confidentiality, I don't
10 know what that means. Because it is out there. It's going
11 out there. And, yeah, it is going out there. And I
12 participate in reviewing. And when I see it, when people
13 see it, they definitely would talk to their colleague and
14 talk to these people. This industry is very -- I'll just
15 say that, just like the photon, information spreads at the
16 speed of light.

17 Q Doctor, the peer reviewers are required to keep
18 the papers confidential, correct?

19 A Let me try to remember my understanding. I
20 don't understand when you say confidential, because the
21 fact that it's going out, and it's being spread out to
22 various reviewers on the committee already. It's being --
23 it's being spread out to people in the field that some
24 would consider POSITA. So I don't know the context of
25 confidential.

1 Q But while these papers are under review, they
2 aren't disseminated to the public, correct?

3 A I don't want to draw on this, but how do you
4 define disseminated in the public? I think the context of
5 this is that in 2007, if I were to view '941 in the lens of
6 2007, which I shouldn't be, because the lens should be
7 viewed -- the lens to view should be in 2020.

8 All I'm simply saying is, even if I were to view
9 it under the lens of 2007, given all the references, this
10 being one of them, not exclusively, only one of them is
11 served to convey that certainly vertical 3D NAND is being
12 pursued. And vertical 3D NAND in the form of vertical
13 string is being pursued.

14 In fact, the infrastructure, such as this, they
15 call it slimming, which we really call it trimming already.
16 Independent of not knowing the paper is trimming and trying
17 to etch the various word line connection, control
18 connection, I think develop and pursue.

19 So I think it's like in my declaration, both
20 initial and reply, people view it as somehow, how can we
21 make this planar and make it erect into a vertical. Then
22 that's the way to pursue. And that's the focus of pursuit
23 at 2007.

24 And even before 2007, as the Endohl reference
25 pointed out. This just serves as another additional

1 reference that is being pursued and actually matured,
2 actually made it to the VLSI Symposium paper, which is
3 published much, much later, compared to when the stuff has
4 been made already.

5 Q Dr. Liu, turning back to Exhibit 2007, do you
6 see on page 2 under contents at the top, it says, Tuesday,
7 June 12th?

8 A I'm trying to understand 2007. Again --

9 Q Sorry, let me strike that. I misspoke.
10 Dr. Liu, turning back to Exhibit Liu 1, which is the 2007
11 symposium on VLSI technology on page 2, do you see under
12 contents, and it says, Tuesday, June 12th?

13 MR. JENSEN: Object to form.

14 THE WITNESS: Where again? 2007, you said?

15 BY MR. LOWRY:

16 Q On page 2 of this document. Do you see that?
17 Page 2 of Exhibit Liu 1.

18 MR. JENSEN: Object to form.

19 THE WITNESS: Repeat your question again. I was
20 at 1075, Tanaka. Sorry.

21 BY MR. LOWRY:

22 Q Okay. On page 2 of Exhibit Liu 1, do you see at
23 the top, it says, contents?

24 MR. JENSEN: Object to form.

25 THE WITNESS: I think I already --

1 MR. LOWRY: Counsel, what is the objection?

2 MR. JENSEN: You are asking about a document
3 that is not allowed in the proceeding, and is not in his
4 declaration.

5 MR. LOWRY: It's about an exhibit that he is
6 claiming is from 2007. So I'm allowed to ask him about it.

7 BY MR. LOWRY:

8 Q Dr. Liu, on page 2 of Exhibit Liu 1, do you see
9 the top, that it says, contents?

10 A Yes, I did.

11 Q And under that, do you see there is a date,
12 Tuesday, June 12th. Do you see that?

13 A Again, I think I have explained very clearly how
14 this conference works, and how that day comes about. And
15 the chronology of that presentation, the actual -- actual
16 delivery of that presentation. So I think I explained the
17 timeframe and chronology. So in that context, I do see
18 Tuesday, June 12th, yes.

19 Q And do you see about a third of the way down the
20 page, it says, 2-2, Bit Cost Scalable Technology With Punch
21 and Plug Process For Ultra High Density Flash Memory,
22 right?

23 A Which page again? I'm sorry.

24 Q Do you see about a third of the way down page 2,
25 it says, 2-2, Bit Cost Scalable Technology With Punch and

1 Plug Process For Ultra High Density Flash Memory.

2 MR. JENSEN: Same objections.

3 THE WITNESS: I do see that. But again, the
4 context of this is as I explained already. I explained
5 there is a chronology, and explained that there is a delay
6 in terms of the actual publication versus paper submission.
7 And that is in the context of this chronology that I just
8 described.

9 BY MR. LOWRY:

10 Q Okay, Dr. Liu. And do you see that the first
11 listed author is H. Tanaka?

12 A I do see that, yes.

13 Q It's fair to say that this is referencing the
14 Tanaka article, Exhibit 1075?

15 MR. JENSEN: Same objection.

16 THE WITNESS: Again -- oh, sorry.

17 MR. JENSEN: Same objections.

18 THE WITNESS: Again, I'm just going to say that
19 is taken in the context of what I testified earlier. There
20 is a chronology and there is -- there is a background that
21 consummated into the publication or the delivery of the --
22 of this presentation.

23 And I believe I testified to that already. And
24 I gave a very clear indication of the sequence. And I also
25 mentioned that this is -- this is one of the supporting

1 evidence, in the context, again, of the lens of 2007, which
2 there were other publications, for example, Endohl which
3 occurred much earlier, and in fact, shared some of the
4 similar figures. I don't know why we don't -- we don't
5 discuss them.

6 But again, there is a chronology to this. And
7 it just is like in 2007, all of a sudden, boom, without any
8 prior knowledge prior to that, this paper shows up. I
9 don't think that's how -- at least as a person of ordinary
10 skill in the art, as a person working on this, I don't
11 think this is how this is done, so --

12 MR. LOWRY: And I'm going to strike that as
13 non-responsive.

14 BY MR. LOWRY:

15 Q Dr. Liu, it's a simple question. I'm asking
16 you, is it fair to say that this -- this portion of this
17 document regarding 2-2, Bit Cost Scalable, by the author H.
18 Tanaka is referring to the article by Tanaka, Exhibit 1075,
19 cited in your second declaration.

20 MR. JENSEN: Same objections.

21 THE WITNESS: I believe it is by giving the same
22 background as 2007, and giving the same background as the
23 chronology. Yes, it is.

24 MR. LOWRY: I'm going to drop in the chat what
25 I'll call -- let me -- another exhibit, which I'll mark as

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1 Liu 2.

2 (Liu Exhibit No. 2 was marked
3 for identification.)

4 BY MR. LOWRY:

5 Q Please let me know when you can pull that up,
6 Dr. Liu.

7 **A I have it.**

8 Q On page 2 of this document, do you see -- well,
9 let me ask you this, Dr. Liu. Are you familiar with IEEE
10 Xplore?

11 **A Yes, I am.**

12 0 And what is it?

13 A It is basically the library for all the
14 different category of different segments of IEEE
15 publications, including certain conferences sponsored by
16 IEEE.

17 Q On page 2 of this document, do you see the
18 title, Bit Cost Scalable Technology With Punch and Plug
19 Process For Ultra High Density Flash Memory?

20 MR. JENSEN: Object to form.

21 THE WITNESS: I see it.

22 BY MR. LOWRY:

23 Q Do you see the first named author is H. Tanaka?

24 MR. JENSEN: Same objection.

25 THE WITNESS: Yes, I do.

1 BY MR. LOWRY:

2 Q And below the abstract on this page, do you see
3 the date of conference indicated as June 12th to 14th,
4 2007?

5 MR. JENSEN: Object to form.

6 THE WITNESS: I see that, but I think I already
7 explained the chronology of how this conference comes
8 about. And you have to take into context a call for papers
9 and then a peer review.

10 BY MR. LOWRY:

11 Q And do you also see the date below that, it
12 says, date added to IEEE Explorer, it says, 08 October
13 2007, right?

14 MR. JENSEN: Object to form.

15 THE WITNESS: I don't -- I see that, but I don't
16 know what relevance that date has, but anyway.

17 MR. LOWRY: No further questions. Pass the
18 witness. Thank you for your time, Dr. Liu.

19 THE WITNESS: Thank you.

20 MR. JENSEN: Let's take maybe, like, a
21 three-minute break.

22 (Recess.)

23 MR. JENSEN: I believe we are back on the
24 record at this point. This is Travis Jensen for
25 Petitioner. I have no questions.

1 MR. LOWRY: Thank you for your time today,
2 Dr. Liu.

3 THE WITNESS: Thank you.

4 (Whereupon, at 11:55 a.m. the taking of the
5 deposition ceased.)

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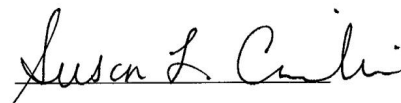
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CERTIFICATE OF NOTARY PUBLIC

I, SUSAN L. CIMINELLI, the officer before whom the foregoing deposition was taken, do hereby certify that the witness whose testimony appears in the foregoing deposition was duly sworn by me; that the testimony of said witness was taken by me in stenotype and thereafter reduced to typewriting under my direction; that said deposition is a true record of the testimony given by said witness; that I am neither counsel for, related to, nor employed by and of the parties to the action in which this deposition was taken; and, further, that I am not a relative or employee of any counsel or attorney employed by the parties hereto, nor financially or otherwise interested in the outcome of this action.



SUSAN L. CIMINELLI

Notary Public in and for

the District of Columbia

My commission expires:

November 30, 2026

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