

Micron Technology, Inc. (Petitioner)
v.
Yangtze Memory Technologies Company, Ltd. (Patent Owner)

IPR2025-00190 (US Patent 11,568,941)

Patent Owner YMTC's Demonstratives

April 28, 2026



Petitioner's Four Grounds

Petition

Petitioner asserts the following grounds:

Ground 1: Dong anticipates claims 1, 3, 5-7, 11, and 13 under §102.

Ground 2: Dong renders obvious claims 1, 3, 5-7, 11, and 13 under §103.

Ground 3: Dong in combination with Costa renders obvious claims 8-9 under §103.

Ground 4: Dong in combination with Shirai renders obvious claims 4, 10, and 14 under §103.

Pet. 7



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14



'941 Patent

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Claims 1, 3, 5-7, 11, 13

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Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14



The '941 Patent

(54) **MEMORY INCLUDING A PLURALITY OF PORTIONS AND USED FOR REDUCING PROGRAM DISTURBANCE AND PROGRAM METHOD THEREOF**

(12) United States Patent
Song et al.

(10) Patent No.: **US 11,568,941 B2**
(45) Date of Patent: **Jan. 31, 2023**

(54) **MEMORY INCLUDING A PLURALITY OF PORTIONS AND USED FOR REDUCING PROGRAM DISTURBANCE AND PROGRAM METHOD THEREOF**

(71) Applicant: Yangtze Memory Technologies Co., Ltd., Wuhan (CN)

(72) Inventors: Yuli Song, Wuhan (CN); XiangNan Zhan, Wuhan (CN); Ying Cai, Wuhan (CN)

(73) Assignee: Yangtze Memory Technologies Co., Ltd., Wuhan (CN)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(58) Field of Classification Search
CPC: G11C 16/3418; G11C 16/06; G11C 16/10
See application file for complete search history.

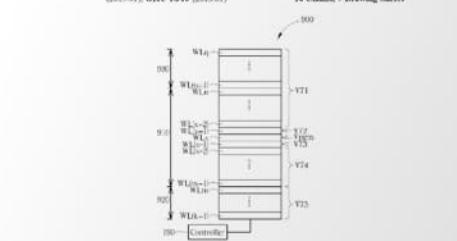
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2013/0103136 A1*
2013/0272067 A1

Patent No.: US 11,568,941 B2
Date of Patent: Jan. 31, 2023

(52) U.S. CL. (2009.01)
G11C 16/3418 (2013.01); G11C 16/06 (2013.01); G11C 16/10 (2013.01)

on (x+1)th word line, and a third voltage to an (x+2)th word line, x, k and m are positive integers.



Micron Ex. 1001, p. 1
Micron v. YMT
IPR2025-00190

Ex. 1001 ('941 Patent)



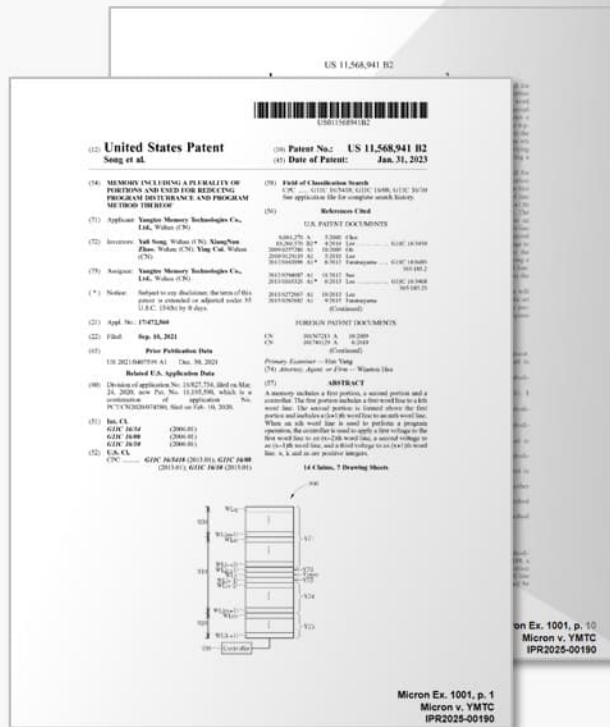
'941 Patent – 3D NAND Problems

In order to increase the capacity of a memory, a memory with a three-dimensional structure has been developed. For example, a three-dimensional stack NAND flash memory can be available presently.

A three-dimensional structure of a memory can include a plurality of layers so as to store more data on a same area. This structure has been proved to be effective for increasing capacity of memory.

However, program disturbance will become more significant when the number of layers is increased. Program disturbance will lead to a higher failure rate of programming a memory. In addition, pass voltage disturbance also occurs when using a memory with a plurality of layers.

Ex. 1001 ('941 Patent), 1:26-38



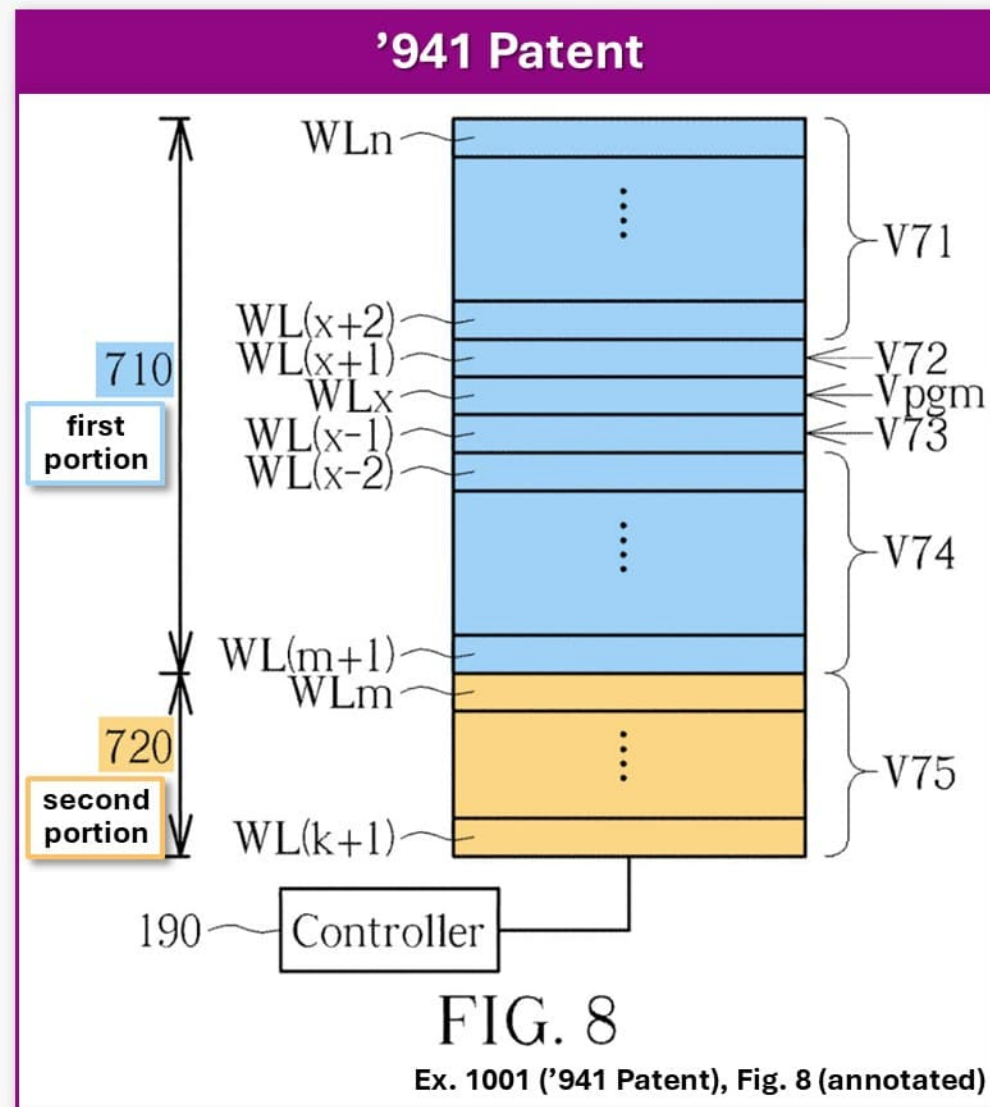
'941 Patent's Solution

Hence, a solution for reducing program disturbance and pass voltage disturbance when operating a three-dimensional memory is in need in the field.

Ex. 1001 ('941 Patent), 1:39-41

In summary, by using a memory sectioned to have a plurality of portions and applying voltages to the word lines of the memory according to the portions, program disturbance and pass voltage disturbance may be reduced according to simulations and experiments. In addition, by using a same voltage source to apply a voltage to word lines of a same portion or word lines of different portions, less voltage sources may be required, and the area of system may be smaller. Hence, problems of the field can be reduced.

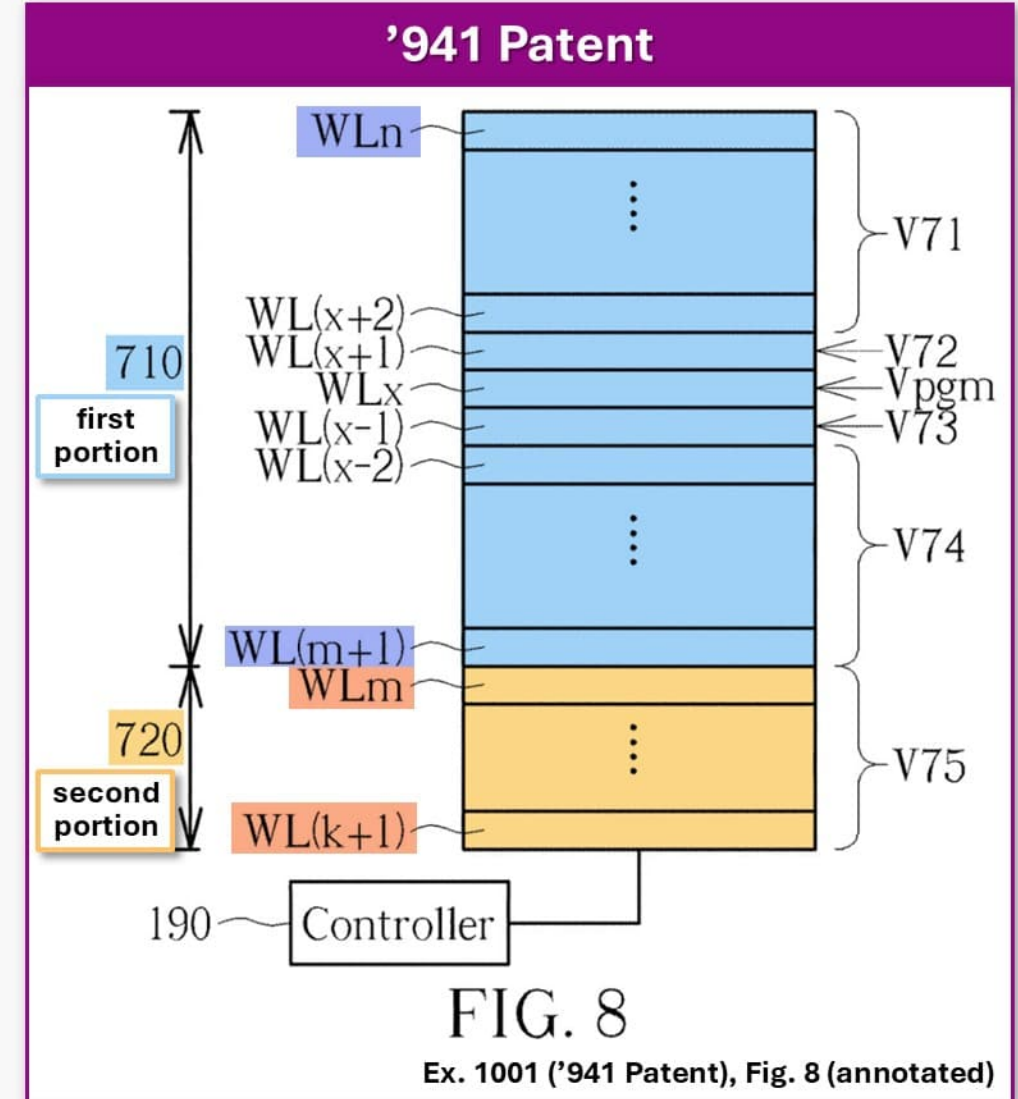
Ex. 1001 ('941 Patent), 6:39-47



'941 Patent's Solution

1. A memory comprising:
 - a first portion comprising an $(m+1)$ th word line to an n th word line from bottom to top; and
 - a second portion formed below the first portion and comprising a $(k+1)$ th word line to an m th word line from bottom to top; and
 - a controller configured to apply a first voltage to an $(x+2)$ th word line to the n th word line, a second voltage to an $(x+1)$ th word line, a third voltage to an $(x-1)$ th word line, a fourth voltage to the $(m+1)$ th word line to an $(x-2)$ th word line, and a fifth voltage to the $(k+1)$ th word line to the m th word line when an x th word line is used to perform a program operation; wherein x , k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

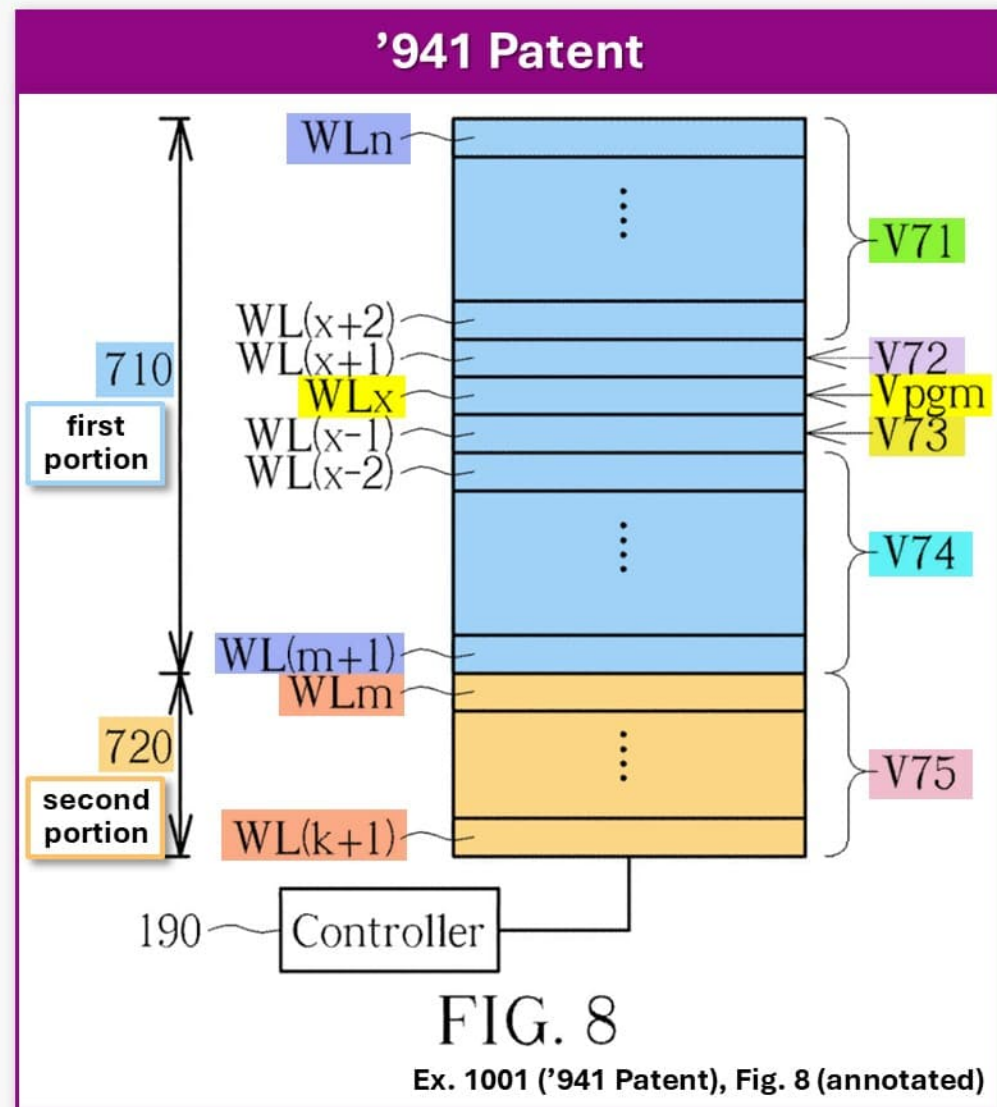
Ex. 1001 ('941 Patent), Claim 1



'941 Patent's Solution

1. A memory comprising:
 - a first portion comprising an $(m+1)$ th word line to an n th word line from bottom to top; and
 - a second portion formed below the first portion and comprising a $(k+1)$ th word line to an m th word line from bottom to top; and
 - a controller configured to apply a first voltage to an $(x+2)$ th word line to the n th word line, a second voltage to an $(x+1)$ th word line, a third voltage to an $(x-1)$ th word line, a fourth voltage to the $(m+1)$ th word line to an $(x-2)$ th word line, and a fifth voltage to the $(k+1)$ th word line to the m th word line when an x th word line is used to perform a program operation;
- wherein x , k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

Ex. 1001 ('941 Patent), Claim 1





'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

- I. “From Bottom To Top” Means From Lowest To Highest
- II. Dong’s Figures Do Not Expressly Disclose Vertically Arranged Wordlines As Recited
- III. Dong’s “Three Dimensional” Language Does Not Expressly Disclose Vertically Arranged Wordlines As Recited
- IV. Petitioner’s New “Envisage” Theory Fails To Anticipate Vertically Arranged Wordlines As Recited

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

I. “From Bottom To Top” Means From Lowest To Highest

II. Dong's Figures Do Not Expressly Disclose Vertically Arranged Wordlines As Recited

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IV. Petitioner's New “Envisage” Theory Fails To Anticipate Vertically Arranged Wordlines As Recited

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Claims 4, 10, 14

“from bottom to top” Means From Lowest To Highest

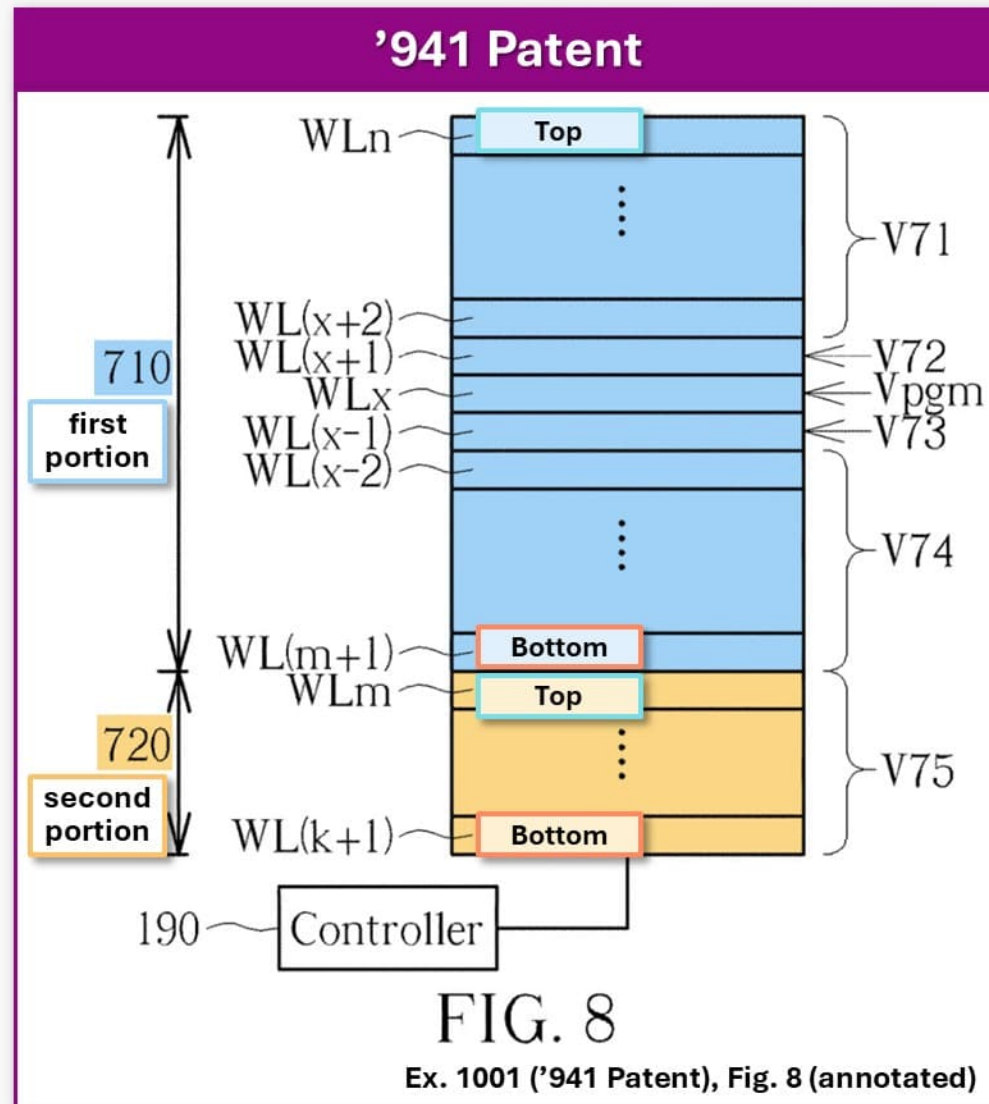
1. A memory comprising:

- a first portion comprising an (m+1)th word line to an nth word line from bottom to top; and
- a second portion formed below the first portion and comprising a (k+1)th word line to an mth word line from bottom to top; and

5. A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first word line to a kth word line from bottom to top, the second portion formed above the first portion and comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:

11. A program method of a memory, the memory comprising a first portion and a second portion formed below the first portion, the first portion comprising an (m+1)th word line to an nth word line from bottom to top, the second portion comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:

Ex. 1001 ('941 Patent), Claims 1, 5, 11





Claim Language Supports PO's Construction

1. A memory comprising:

* * *

a second portion formed **below** the first portion and

2. The memory of claim 1, further comprising a third portion formed **below** the second portion and comprising a

3. The memory of claim 1, further comprising a third portion formed **above** the first portion and comprising a

4. The memory of claim 1, further comprising:
an upper dummy word line formed **below** the first portion;
a lower dummy word line formed **above** the second portion; and

5. A program method of a memory, the memory comprising:
* * *
to top, the second portion formed **above** the first portion and

11. A program method of a memory, the memory comprising a first portion and a second portion formed **below** the first portion, the first portion comprising an (m+1)th word

Specification Supports PO's Construction

FIG. 7 and FIG. 8 illustrate a memory 700 operated in two conditions according to another embodiment. The memory 700 may include a first portion 710, a second portion 720 and a controller 190. The first portion 710 may include an (m+1)th word line $WL(m+1)$ to an nth word line WLn from bottom to top. The second portion 720 may be formed below the first portion 710 and include a (k+1)th word line $WL(k+1)$ to an mth word line WLm from bottom to top.

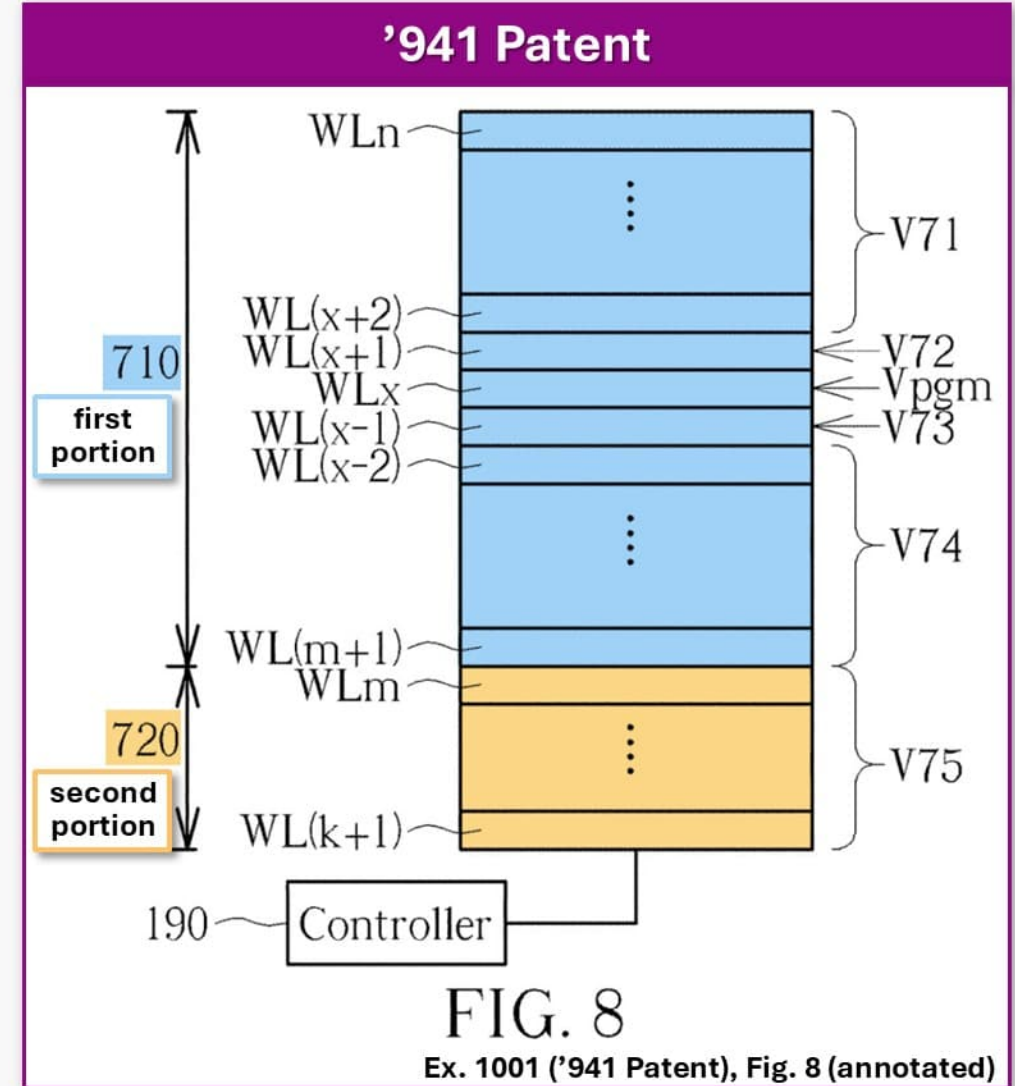
Ex. 1001 ('941 Patent), 4:29-36

In FIG. 9, the word line (e.g., WLx) used to performed a program operation is located in a lowermost portion of the three portions.

In FIG. 10, the word line (e.g., WLx) used to performed a program operation is located in a second lowermost portion of the three portions.

In FIG. 11, the word line (e.g., WLx) used to performed a program operation is located in an uppermost portion of the three portions.

Ex. 1001 ('941 Patent), 5:42-50



Specification Supports PO's Construction

portion, a second portion and a controller. The first portion includes a first word line to a kth word line **from bottom to top**. The second portion is formed **above** the first portion and includes a (k+1)th word line to an mth word line **from bottom to top**. The controller is used to apply a first voltage

Ex. 1001 ('941 Patent), 1:46-50

portion, a second portion and a controller. The first portion includes an (m+1)th word line to an nth word line **from bottom to top**. The second portion is formed **below** the first portion and includes a (k+1)th word line to an mth word line **from bottom to top**. The controller is used to apply a first

Ex. 1001 ('941 Patent), 1:56-60

line to a kth word line from bottom to top. The second portion is formed **above** the first portion and includes a (k+1)th word line to an mth word line **from bottom to top**.

Ex. 1001 ('941 Patent), 2:4-6

and a second portion formed below the first portion. The first portion includes an (m+1)th word line to an nth word line **from bottom to top**. The second portion includes a (k+1)th word line to an mth word line **from bottom to top**. The

Ex. 1001 ('941 Patent), 2:14-17

second portion 120 and a controller 190. The first portion 110 may include a first word line WL1 to a kth word line WLk **from bottom to top**. The second portion 120 may be formed **above** the first portion 110 and includes a (k+1)th word line WL(k+1) to an mth word line WLn **from bottom to top**.

Ex. 1001 ('941 Patent), 2:65-3:3

The third portion 130 may be formed **above** the second portion 120 and includes an (m+1)th word line WL(m+1) to an nth word line WLn **from bottom to top**. As shown in FIG.

Ex. 1001 ('941 Patent), 3:46-48

720 shown in FIG. 7. The third portion 930 may be formed **above** the first portion 910 and include a plurality of word lines WL(n+1) to WLq **from bottom to top**. The condition of

Ex. 1001 ('941 Patent), 5:7-9

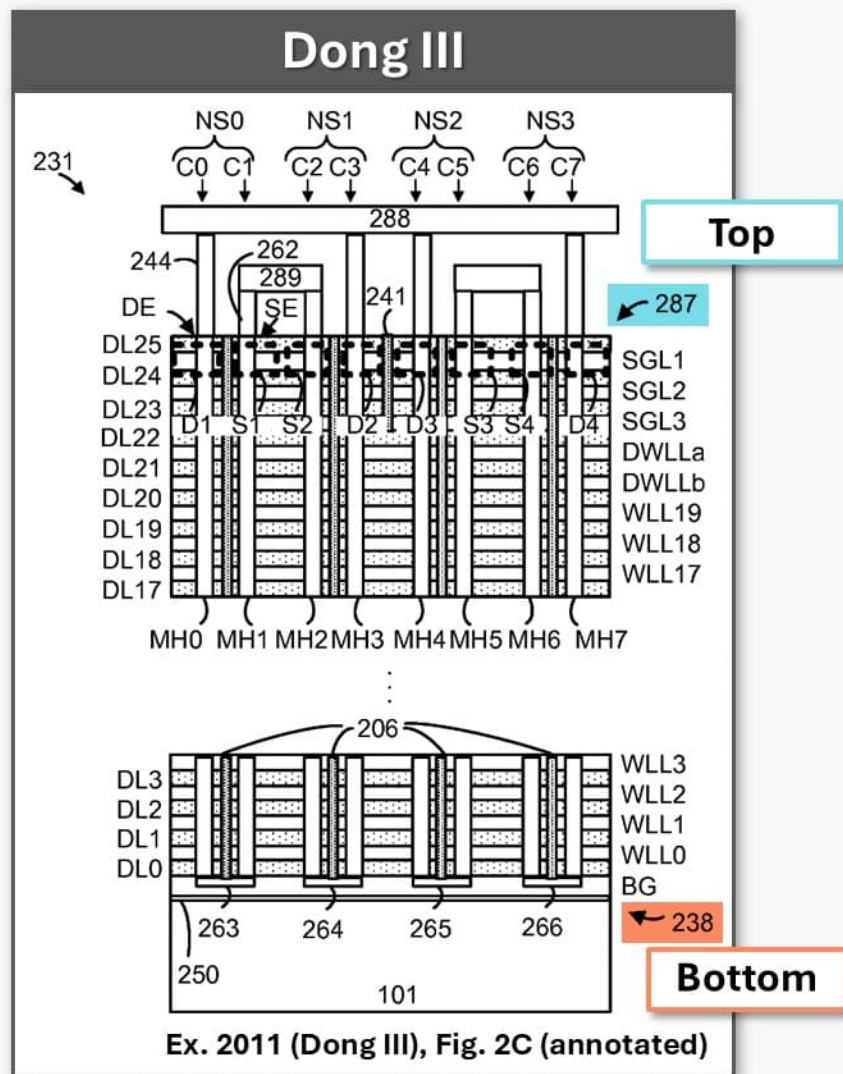
The memory 900 of FIG. 10 may have the same structure as shown in FIG. 9. The condition of FIG. 10 may be similar to FIG. 8 where the word line WLx used to performed a program operation is located in the portion 910 above the **lowermost** portion 920. The voltages applied to the portions

Ex. 1001 ('941 Patent), 5:15-19

FIG. 9 and FIG. 10. As shown in FIG. 11, the third portion 1130 may include a first word line WL1 to a kth word line WLk **from bottom to top**. The controller 190 may apply a six

Ex. 1001 ('941 Patent), 5:32-34

Other Intrinsic Evidence Supports PO's Construction

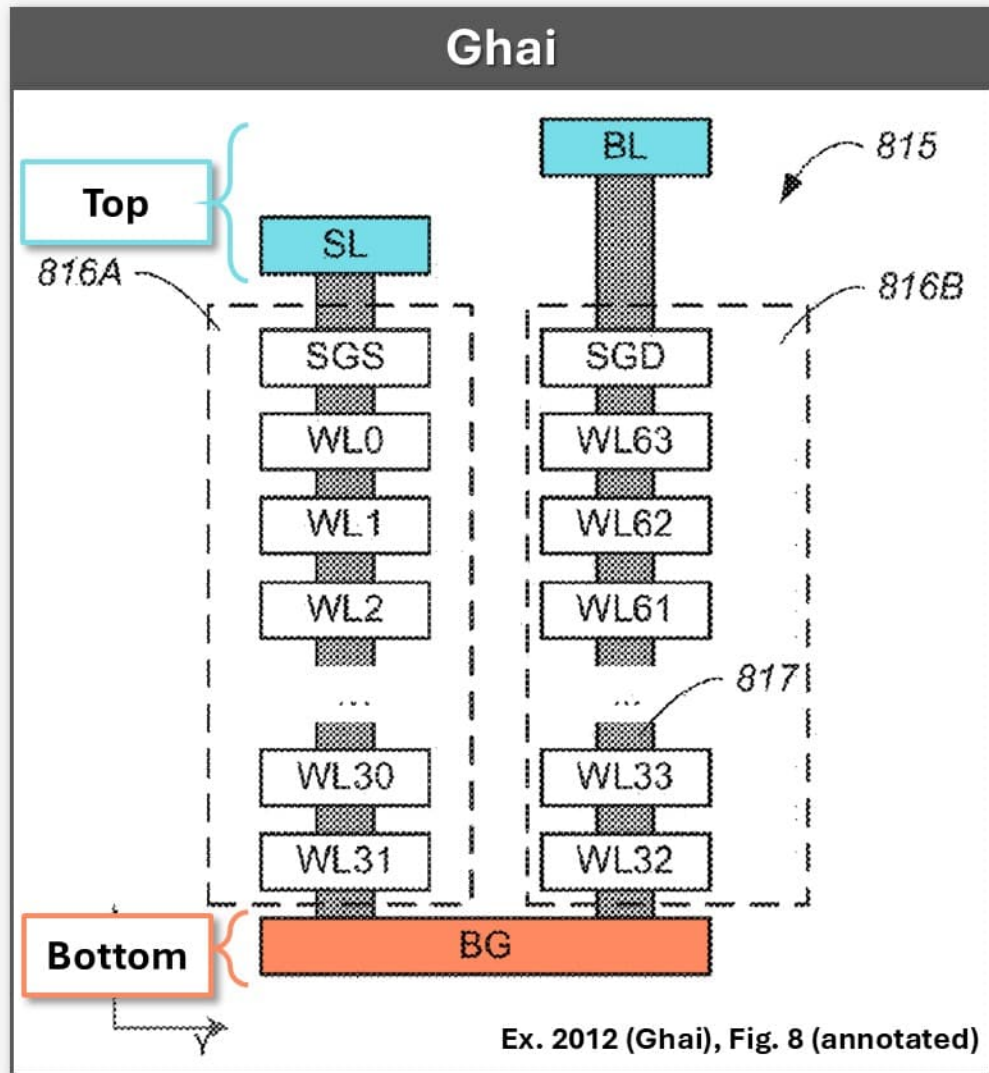


Dong III

[0075] FIG. 2C depicts an embodiment of a stack 231 showing a cross-sectional view of the portion 209 of FIG. 2A, along line 220. This example includes three select gate layers, SGL1, SGL2 and SGL3. In this case, the slit extends down to DL22, so that three separate layers of select gate transistors are formed in each column of each NAND string. The stack has a top 287 and a bottom 238.

Ex. 2011 (Dong III), [0075]

Other Intrinsic Evidence Supports PO's Construction



Ghai

[0084] FIG. 8 shows a second example of a NAND string **815** that extends in a vertical direction (z-direction). In this case, NAND string **815** forms a U-shape, connecting with external elements (source line “SL” and bit line “BL”) located on the top of the structure. At the bottom of NAND string **815** is a controllable gate (back gate “BG”) which connects the two wings **816A**, **816B** of NAND string **815**. A total of 64 cells are formed where word lines WL0-WL63 intersect the vertical local bit line **817** (though in other examples other numbers of cells may be provided). Select gates SGS, SGD, are located at either end of NAND string **815** to control connection/isolation of NAND string **815**.

Ex. 2012 (Ghai), [0084]

Extrinsic Evidence Supports PO's Construction

Definitions of "Bottom"

'bot·tom \ˈbä-təm\ *n* 1 : an under or supporting surface; *also* : BUTTOCKS 2 : the surface on which a body of water lies 3 : the lowest part or place; *also* : an inferior position <start at the ~> 4 : BOT-

Ex. 2013 (The Merriam-Webster Dictionary), 4

bot·tom (böt'əm) *n*. 1. The deepest or lowest part: the bottom of a well; the bottom of the page. 2. The part closest to a reference point: *was positioned at the bottom of the key for a rebound.* 3. The underside: *scraped the bottom of the car on a rock.* 4. The supporting part; the base. 5. The far end or part: *at the bottom of the bed.* 6a. The last place, as on a list.

Ex. 2014 (The American Heritage Dictionary), 3

Definitions of "Top"

'top \ˈtäp\ *n* 1 : the highest part, point, or level of something 2 : the part of a plant with edible roots lying above the ground <beet ~s> 3 : the upper end, edge, or surface <the ~ of a page> 4 : an upper piece, lid, or covering 5 : the highest de-

Ex. 2013 (The Merriam-Webster Dictionary), 5

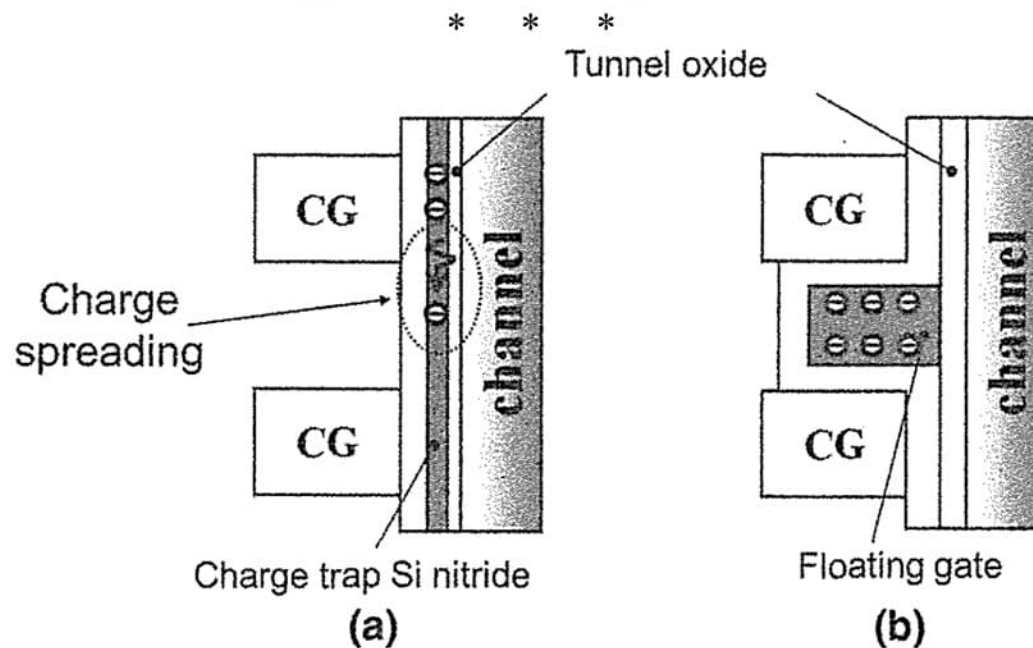
top¹ (töp) *n*. 1. The uppermost part, point, surface, or end: wrote on the top of the box. 2. The part farthest from a given reference point: *took a jump shot from the top of the key.* 3. The crown of the head: *from top to toe.* 4. The part of a plant, such as a rutabaga, that is above the ground. 5. Something, such as a lid or cap, that covers or forms an uppermost part. 6. A garment worn on the upper half of the body. 7. Nautical A platform enclosing the head of each mast of a sailing ship, to which the topmast rigging is attached. 8. The highest degree, pitch, or point; the peak, acme, or zenith: *"It had come at a time when he was not feeling at the top of his form"* (Anthony Powell). 9a. The highest position or rank: *at the top of his career.*

Ex. 2014 (The American Heritage Dictionary), 4

Petitioner's Extrinsic Evidence Supports PO's Construction

Aritome

cells along the charge trap nitride layer. The charge spreading problem in 3D charge trap cell is illustrated in Fig. 7.55a. The stored charges in Si nitride move toward the neighbor cells through a connected nitride layer, because the charge trap nitride layer is physically connected from top to bottom CGs in 3D SONOS/TANOS NAND flash.



Ex. 1009 (Aritome), 327, Fig. 7.55

Petitioner Changed Constructions For “from bottom to top”

Petition

“the source end of the NAND string at the bottom, and the drain end of the NAND string at the top”

Pet. 35; Ex. 1004 (Liu Pet. Decl.) ¶¶ 113, 120



Reply

“indexed and programmed from the source to drain”

Reply 2-3, 6-7; Ex. 1089 (Liu Reply Decl.) ¶¶ 6, 14-15



Petitioner's Constructions Are Inconsistent With Intrinsic Evidence

No mention of “source” or “drain,” much less indexing scheme where “bottom” means “source” and “top” means “drain”

Ex. 2028 (Khatri POR Decl.) ¶ 127

Claims support “from bottom to top” is a vertical arrangement in physical memory, not indexing scheme.

Ex. 1001 ('941 Patent), Claims 1, 3-5; ID 16-17

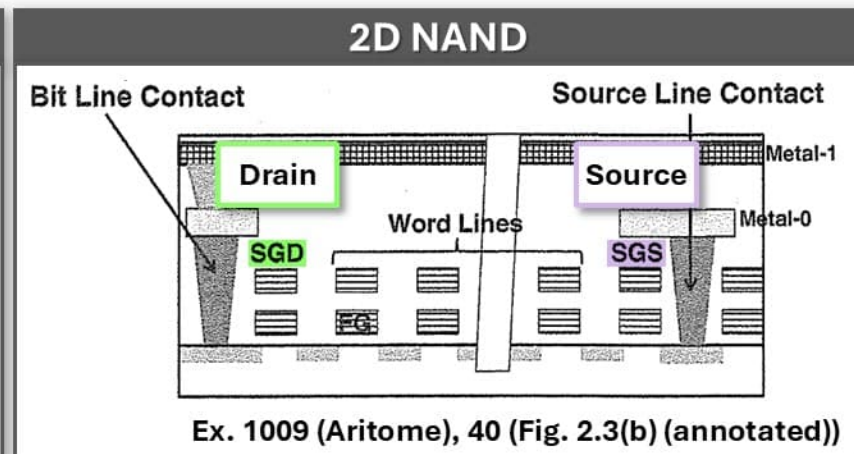
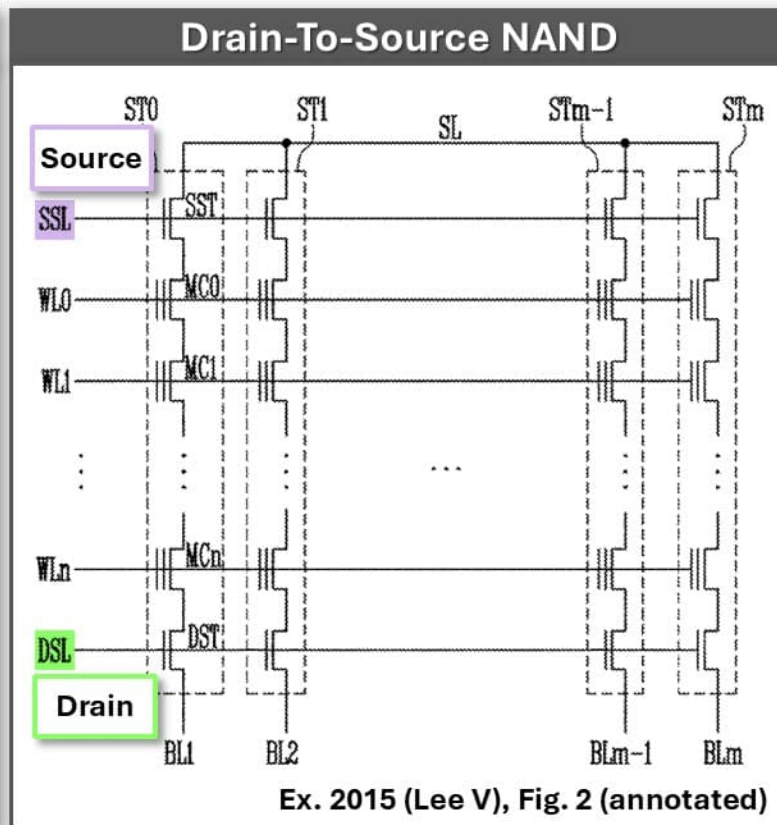
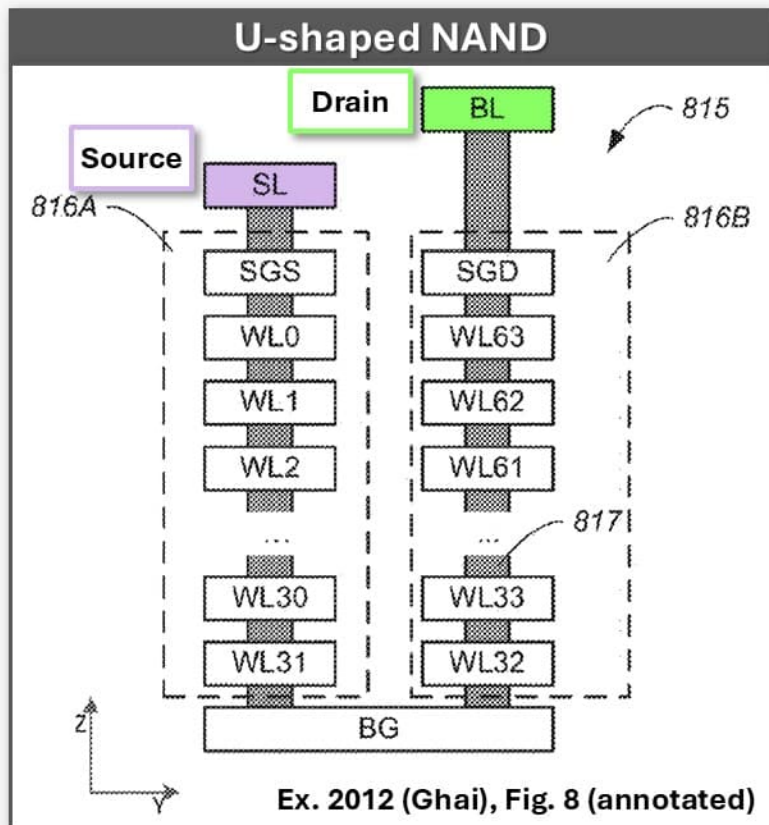
Specification confirms “from bottom to top” refers to relative vertical location of word lines, not relative to the source or drain.

Ex. 1001 ('941 Patent), 2:67-3:3, 4:18-20, 4:34-36; ID 18

Figures 1-11 depict a memory's word lines vertically arranged.

Ex. 1001 ('941 Patent), Figs. 1-11; Ex. 2028 (Khatri POR Decl.) ¶ 116; ID 17-18

Petitioner's New Construction Deprives "bottom" And "top" Of Any Meaning



Petitioner's Expert

A. It has nothing to do with the physical level. It has to do with a reference point. And that's the context of my testimony and the context of my reply declaration.

Ex. 2030 (Liu-Dep2), 26:1-26:7



Petitioner's New Construction Deprives “bottom” And “top” Of Any Meaning

Petitioner's Expert

the forest for the trees. As noted, the reason the claims recite *bottom to top*, *above*, and *below* is to establish an indexing scheme (using the variables *x*, *k*, *m*, etc.) for specifying wordline locations/groupings (e.g., *portions*) to which different voltages are applied, not to require a physical memory string architecture. In other words,

* * *

sensible. A POSITA would not understand the '941 patent claims to exclude U-shaped 3D memory.

Ex. 1089 (Liu Reply Decl.) ¶¶ 15, 24



Petitioner's Expert Says 3D Means Vertical In 2020

'941 Patent

In order to increase the capacity of a memory, a memory with a **three-dimensional structure** has been developed. For example, a three-dimensional stack NAND flash memory can be available presently.

A **three-dimensional structure** of a memory can include a plurality of layers so as to store more data on a same area. This structure has been proved to be effective for increasing capacity of memory.

However, program disturbance will become more significant when the number of layers is increased. Program disturbance will lead to a higher failure rate of programming a memory. In addition, pass voltage disturbance also occurs when using a memory with a plurality of layers.

Hence, a solution for reducing program disturbance and pass voltage disturbance when operating a **three-dimensional memory** is in need in the field.

Ex. 1001 ('941 Patent), 1:26-41

Petitioner's Expert

in the vertical string corresponding to the number of layers in the stack). In fact, in

2020, "three dimensional" (3D) memory was practically synonymous with vertical

memory strings. Regardless of how well-known **vertical 3D NAND** was in 2007

(which I discuss below), it **was ubiquitous in 2020**. As such, in view of a POSITA's

* * *

work. Patent Owner suggestion that a POSITA in 2020 would not think of vertical

memory when reading Dong's "three dimensional" disclosure ignores reality. Even

* * *

41. A simple survey of the state of technology and market trends around the time of the '941 invention would have shown that **virtually all the major 3D NAND flash memory makers were focusing on increasing the number of layers on a vertical string of NAND memory cells, not on stacking different 2D NAND arrays on top of each other.**

Ex. 1089 (Liu Reply Decl.) ¶¶ 40, 47, 41

Petitioner's Reliance On Extrinsic Evidence Is Improper



Vitronics

In most situations, an analysis of the intrinsic evidence alone will resolve any ambiguity in a disputed claim term. In such circumstances, it is improper to rely on extrinsic evidence....

In those cases where the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper. The claims, specification, and file history, rather than extrinsic evidence, constitute the public record of the patentee's claim, a record on which the public is entitled to rely.

Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1583 (Fed. Cir. 1996) (citations omitted)

Undisputed That Preambles Of Claims 5 And 11 Are Limiting

5. A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first word line to a kth word line from bottom to top, the second portion formed above the first portion and comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:

applying a first voltage to the to the first word line to an (x-2)th word line when an xth word line is used to perform a program operation;

applying a second voltage to an (x-1)th word line; and
applying a third voltage to an (x+1)th word line;

wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

Ex. 1001 ('941 Patent), Claim 5

11. A program method of a memory, the memory comprising a first portion and a second portion formed below the first portion, the first portion comprising an (m+1)th word line to an nth word line from bottom to top, the second portion comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:

applying a first voltage to an (x+2)th word line to the nth word line when an xth word line is used to perform a program operation;

applying a second voltage to an (x+1)th word line;

applying a third voltage to an (x-1)th word line;

applying a fourth voltage to the (m+1)th word line to an (x-2)th word line; and

applying a fifth voltage to the (k+1)th word line to the mth word line;

wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

Ex. 1001 ('941 Patent), Claim 11



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

I. “From Bottom To Top” Means From Lowest To Highest

II. Dong’s Figures Do Not Expressly Disclose Vertically Arranged Wordlines As Recited

III. Dong’s “Three Dimensional” Language Does Not Expressly Disclose Vertically Arranged Wordlines As Recited

IV. Petitioner’s New “Envisage” Theory Fails To Anticipate Vertically Arranged Wordlines As Recited

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14

Ground 1: Petitioner Argues Anticipation By Express Disclosure



Sanofi

Anticipation “requires that every element and limitation of the claim was previously described in a single prior art reference, either expressly or inherently, so as to place a [POSITA] in possession of the invention.”

Sanofi-Synthelabo v. Apotex, Inc., 550 F.3d 1075, 1082 (Fed. Cir. 2008) (citations omitted)

Petitioner's Reply

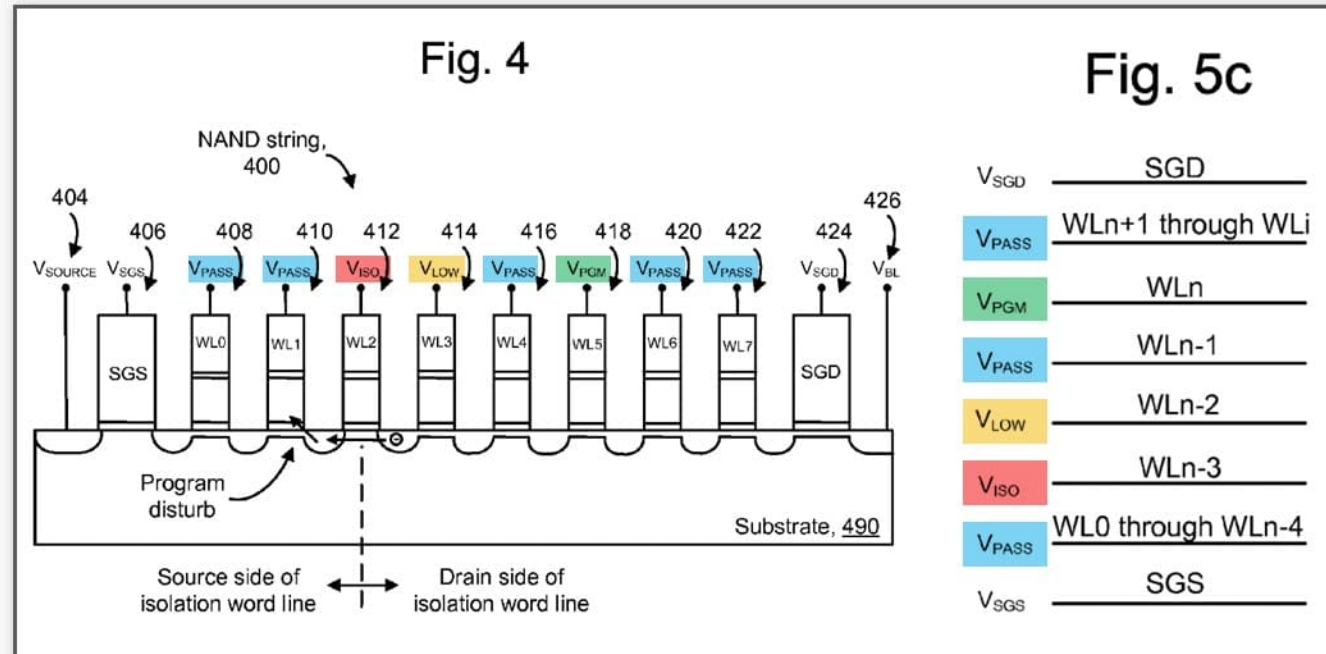
Petitioner is not arguing inherency (and need not do so because Dong discloses “three dimensional” memory).

Reply 11

Dong's Only Structural Figure Is 2D With Horizontal Wordlines

Dong

[0045] FIG. 4 depicts a cross-sectional view of a NAND string showing a program disturb mechanism. Here, a revised erased area self-boosting (REASB) mode, such as depicted in FIG. 5c, is used. The view is simplified and not to scale. The



Ex. 1005 (Dong), [0045], Figs. 4, 5c

Figures 5a/5g Depict Voltage Schemes, Not Physical Structure

Dong

[0047] FIGS. 5a-h depict different examples of self-boosting modes. Note that the voltages depicted indicate the volt-

[0059] FIG. 5g depicts another revised erased area self-boosting mode. This case differs from that of FIG. 5f in that

Fig. 4

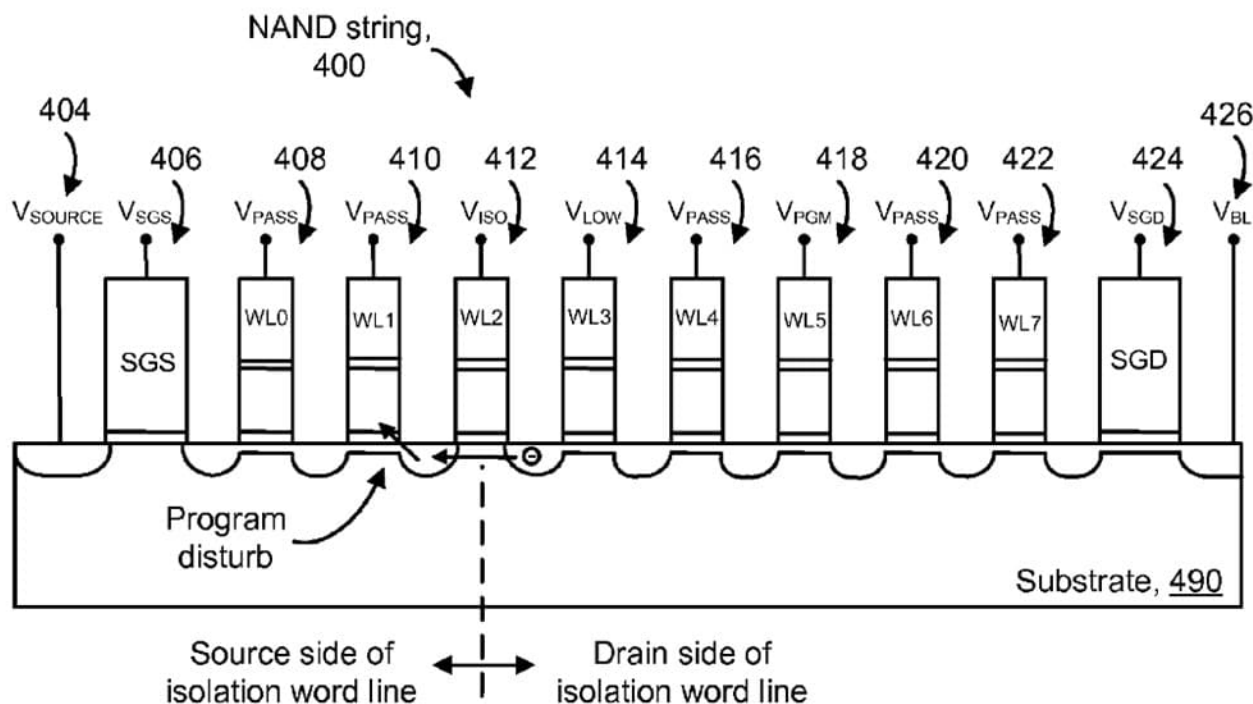


Fig. 5a

V_{SGD}	SGD
V_{PASS}	WLn+1 through WLi
V_{PGM}	WLn
V_{ISO}	WLn-1
V_{PASS}	WL0 through WLn-2
V_{SGS}	SGS

Ex. 1005 (Dong), [0047], [0059],
Figs. 4, 5a, 5g

Fig. 5g

V_{SGD}	SGD
V_{PASS}	WLn+2 through WLi
$V_{PASS-HIGH}$	WLn+1
V_{PGM}	WLn
$V_{PASS-HIGH}$	WLn-1
$V_{PASS-MEDIUM}$	WLn-2
$V_{PASS-LOW}$	WLn-3
V_{LOW}	WLn-4
V_{ISO}	WLn-5
V_{LOW}	WLn-6
$V_{PASS-LOW}$	WLn-7
V_{PASS}	WL0 through WLn-8
V_{SGS}	SGS

Dong Ties Figures 5a/5g To Figure 4's 2D Structure

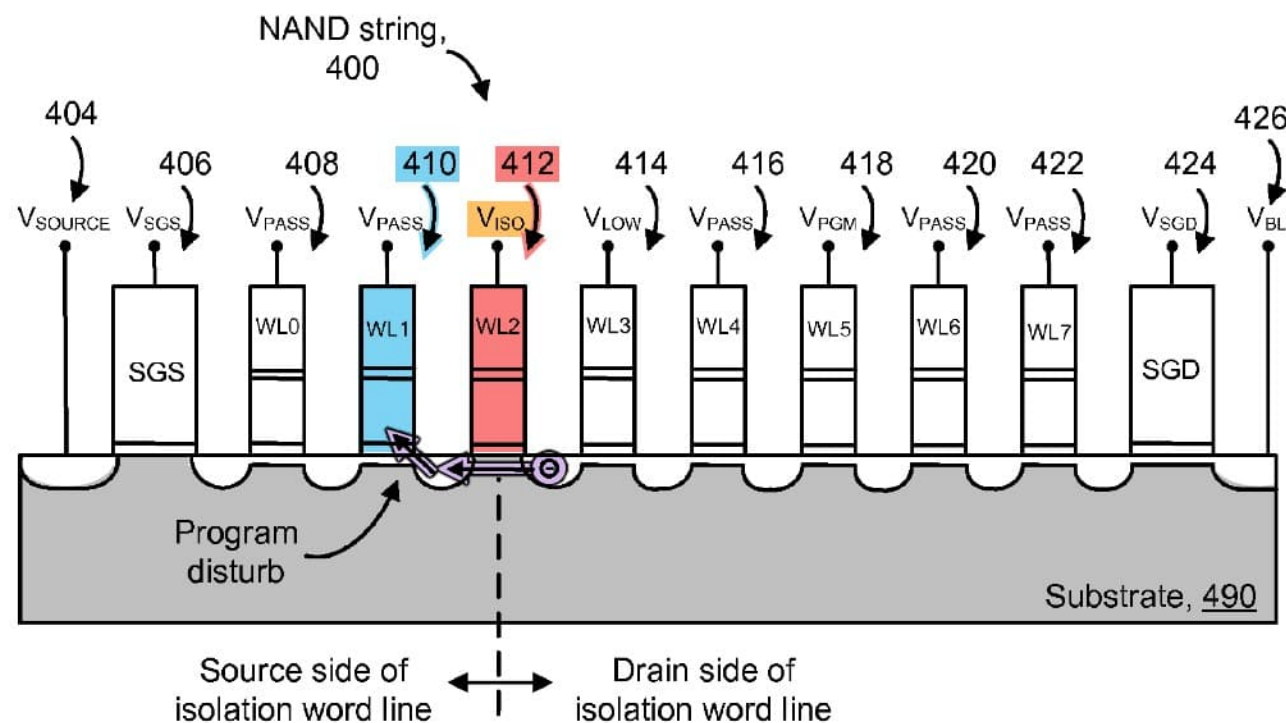
Dong

[0047] FIGS. 5a-h depict different examples of self-boosting modes. Note that the voltages depicted indicate the volt-

[0059] FIG. 5g depicts another revised erased area self-boosting mode. This case differs from that of FIG. 5f in that

[0065] With the EASB or REASB boosting modes, V_{ISO} is applied to one or more source-side neighbors of the selected word line at some point after boosting is initiated, and is sufficiently low to isolate programmed and erased channel areas in the substrate. That is, a channel area of the substrate 490 on a source-side of the isolation word line 412 is isolated from a channel area of the substrate on a drain-side of the isolation word line 412. The source side can also be considered to be a programmed side since most or all of the associated storage elements have been programmed, while the drain side can also be considered to be an unprogrammed side since the associated storage elements have not yet been programmed. Further, the channel area on the source side is a first boosted region of the substrate 490 which is boosted by the application of V_{PASS} on WL0 and WL1, while the channel area on the drain side is a second boosted region of the substrate 490 which is boosted mainly by the application of V_{PGM} on WL5 and V_{PASS} on WL4, WL6 and WL7.

Ex. 1005 (Dong), [0047], [0059], [0065]



Ex. 1005 (Dong), Fig. 4 (annotated)

Dong Ties Figures 5a/5g To Figure 4's 2D Structure

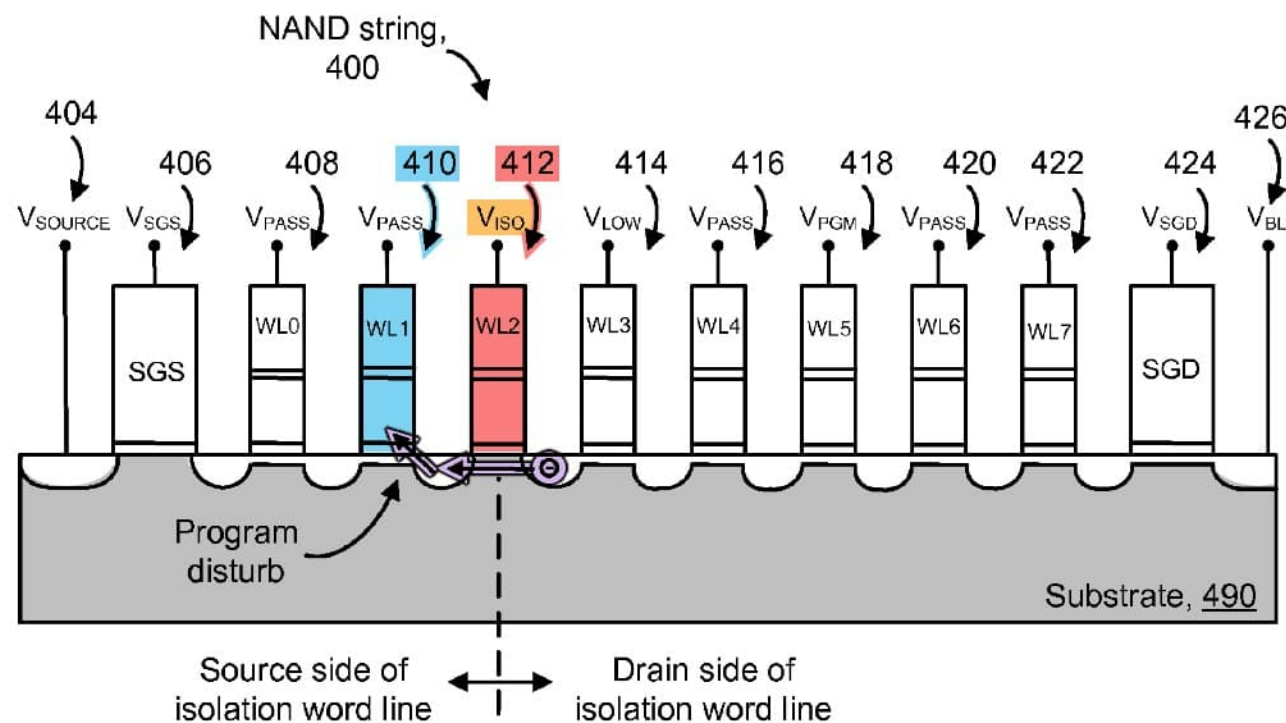
[0067] While the above embodiments can reduce certain program disturb mechanisms, other program disturb mechanisms do exist. One other program disturb fail mode tends to

string channels. This hot carrier injection is induced by a high boosting potential in the source side channel when V_{PASS} reaches a certain level. In particular, with EASB and REASB, as discussed, the NAND string is separated into a source side and a drain side, by applying the isolation voltage V_{ISO} on a word line below the selected word line. In the selected NAND

still boosted up. When the source side boosting potential becomes high and the drain side channel potential remains at 0-1 V, a large lateral electric field is created which can induce hot carrier injection to the storage elements on the source side and cause program disturb fails. This is depicted in FIG. 4, where the arrows depict electrons moving across the channel under the isolation storage element 412 and into the floating gate of storage element 410, raising the threshold voltage of the storage element.

Ex. 1005 (Dong), [0067]

Dong

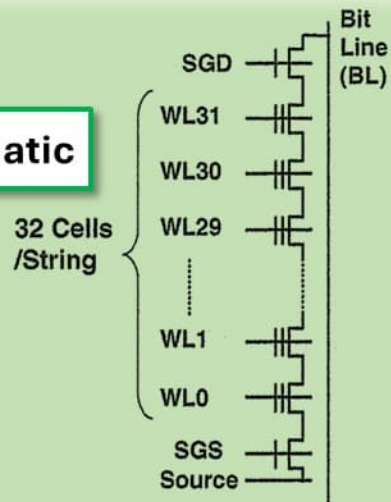


Ex. 1005 (Dong), Fig. 4 (annotated)

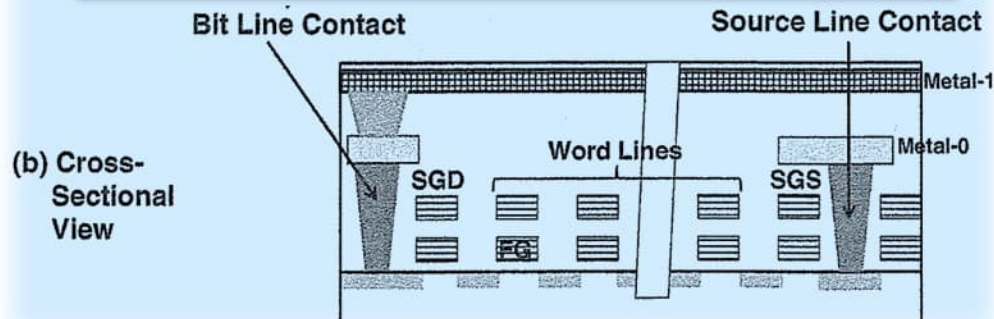
Dong's Figures 5a/5g Depict Voltage Charts, Not Physical Structure

Aritome

circuit schematic



horizontal 2D NAND physical arrangement

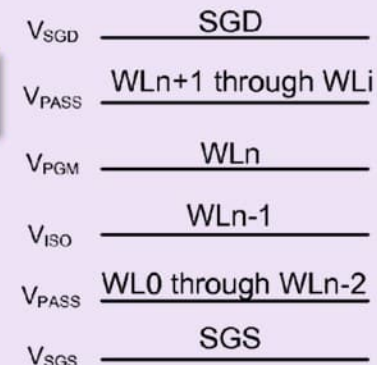


Ex. 1009 (Aritome), 39-40 (Figs. 2.2, 2.3(b))

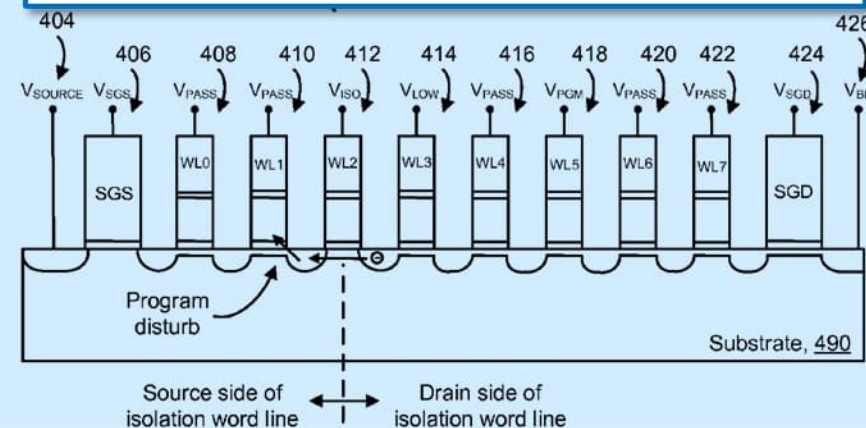
Dong

Fig. 5a

voltage chart

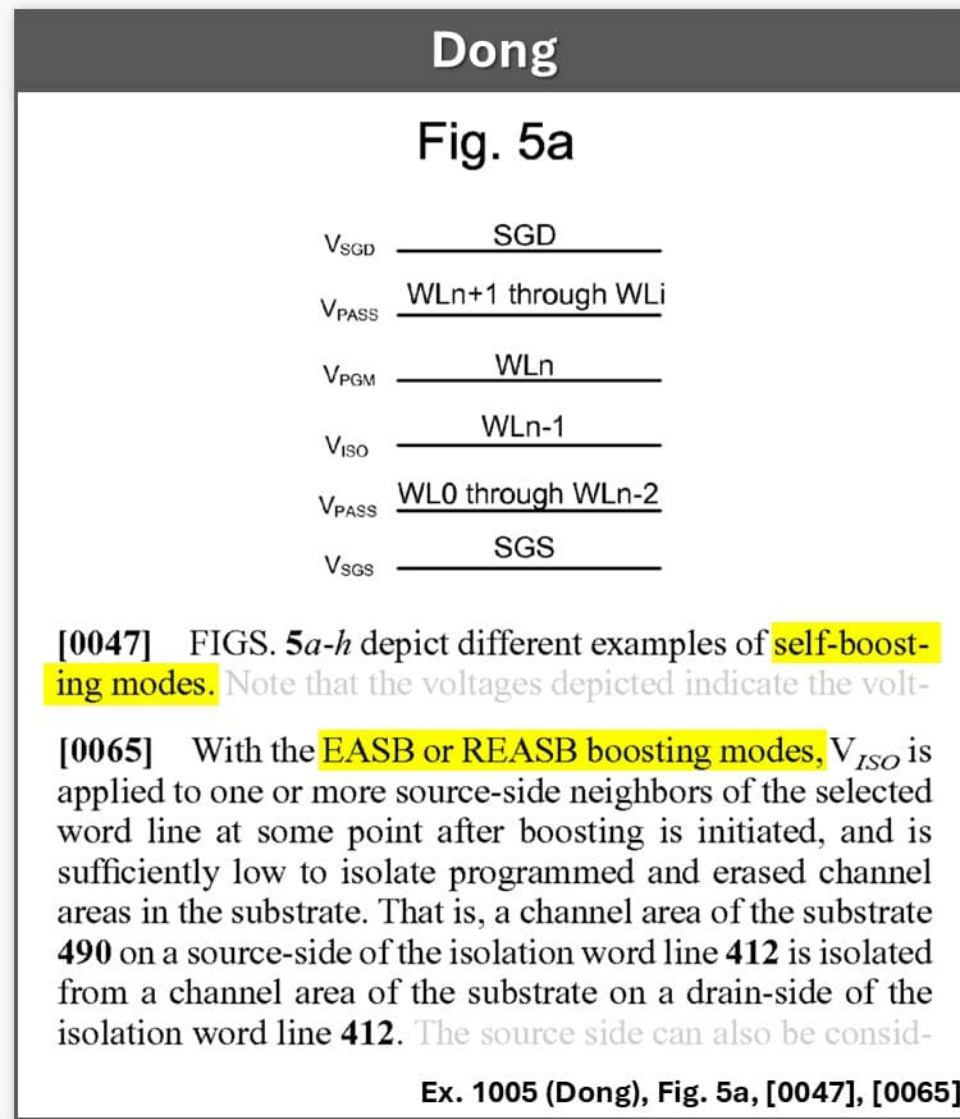
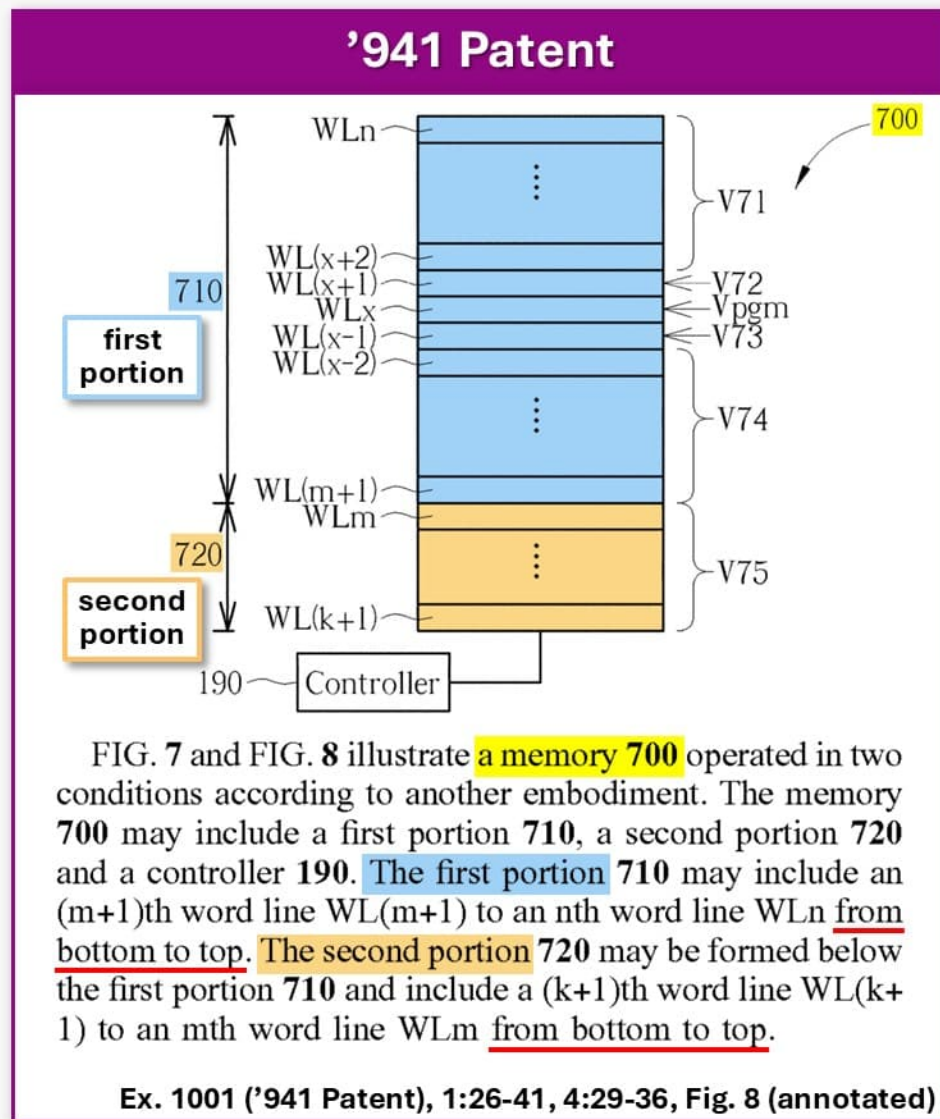


horizontal 2D NAND physical arrangement



Ex. 1005 (Dong), Figs. 5a, 4

Petitioner's False Equivalence Of '941 Patent And Dong





'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

- I. “From Bottom To Top” Means From Lowest To Highest
- II. Dong’s Figures Do Not Expressly Disclose Vertically Arranged Wordlines As Recited
- III. Dong’s “Three Dimensional” Language Does Not Expressly Disclose Vertically Arranged Wordlines As Recited**
- IV. Petitioner’s New “Envisage” Theory Fails To Anticipate Vertically Arranged Wordlines As Recited

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14

Dong's "three dimensional" Language Does Not Expressly Disclose Vertical Wordlines As Recited

Dong

[0095] FIG. 12 is a block diagram of a non-volatile memory system using single row/column decoders and read/write circuits. The diagram illustrates a memory device 1296 having read/write circuits for reading and programming a page of storage elements in parallel, according to one embodiment of the present invention. Memory device 1296 may include one or more memory die 1298. Memory die 1298 includes a two-dimensional array of storage elements 1100, control circuitry 1210, and read/write circuits 1265. In some embodiments, the array of storage elements can be three dimensional. The memory array 1100 is addressable by word lines via a row decoder 1230 and by bit lines via a column decoder 1260. The read/write circuits 1265 include multiple sense

Ex. 1005 (Dong), [0095]

'941 Patent

1. A memory comprising:
 - a first portion comprising an $(m+1)$ th word line to an n th word line from bottom to top; and
 - a second portion formed below the first portion and comprising a $(k+1)$ th word line to an m th word line from bottom to top; and
 - a controller configured to apply a first voltage to an $(x+2)$ th word line to the n th word line, a second voltage to an $(x+1)$ th word line, a third voltage to an $(x-1)$ th word line, a fourth voltage to the $(m+1)$ th word line to an $(x-2)$ th word line, and a fifth voltage to the $(k+1)$ th word line to the m th word line when an x th word line is used to perform a program operation;
- wherein x , k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

Ex. 1001 ('941 Patent), Claim 1

Dong's "three dimensional" Language Does Not Expressly Disclose Vertical Wordlines As Recited

Dong

[0095] FIG. 12 is a block diagram of a non-volatile memory system using single row/column decoders and read/write circuits. The diagram illustrates a memory device 1296 having read/write circuits for reading and programming a page of storage elements in parallel, according to one embodiment of the present invention. Memory device 1296 may include one or more memory die 1298. Memory die 1298 includes a two-dimensional array of storage elements 1100, control circuitry 1210, and read/write circuits 1265. In some embodiments, the array of storage elements can be three dimensional. The memory array 1100 is addressable by word lines via a row decoder 1230 and by bit lines via a column decoder 1260. The read/write circuits 1265 include multiple sense

"with vertical wordlines"

Ex. 1005 (Dong), [0095]

'941 Patent

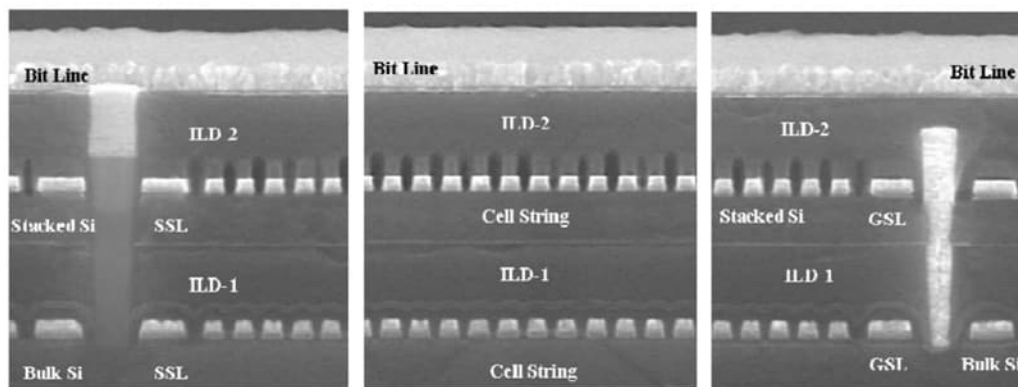
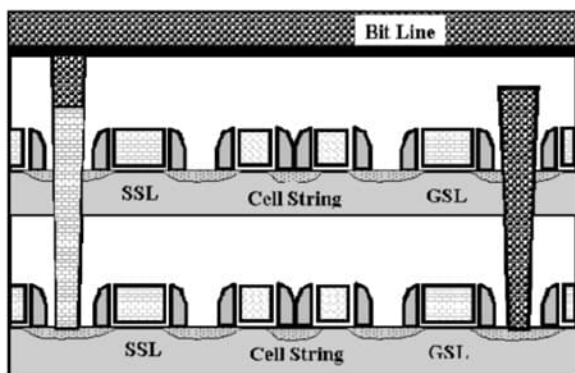
1. A memory comprising:
 - a first portion comprising an $(m+1)$ th word line to an n th word line from bottom to top; and
 - a second portion formed below the first portion and comprising a $(k+1)$ th word line to an m th word line from bottom to top; and
 - a controller configured to apply a first voltage to an $(x+2)$ th word line to the n th word line, a second voltage to an $(x+1)$ th word line, a third voltage to an $(x-1)$ th word line, a fourth voltage to the $(m+1)$ th word line to an $(x-2)$ th word line, and a fifth voltage to the $(k+1)$ th word line to the m th word line when an x th word line is used to perform a program operation;
- wherein x , k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

Ex. 1001 ('941 Patent), Claim 1



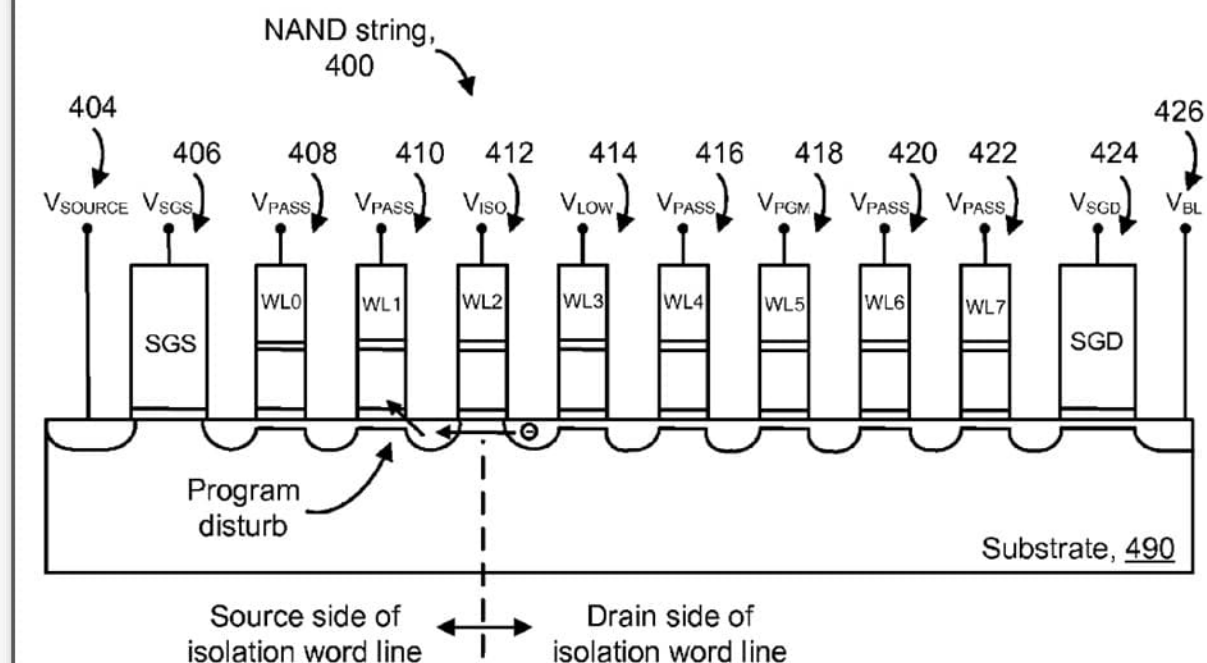
Dong's "three dimensional" Language Discloses Horizontal 3D NAND, Not Vertical

Horizontal 3D NAND



POR 43; Ex. 2008, 3, Figs. 3, 4; Ex. 2009, 4

Dong's 2D NAND



Ex. 1005 (Dong), Fig. 4



Broad Genus Of “three dimensional” Does Not Expressly Disclose Species Of Vertical 3D NAND



Wasica

It is well established that disclosure of a genus in the prior art is not necessarily a disclosure of every species that is a member of that genus.... Here, the Board determined that Oselin's broad invocation of “any modulation scheme” (a genus) does not disclose with sufficient particularity the constant-frequency modulation scheme of claim 6 (a species).

Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc., 853 F.3d 1272, 1285-86 (Fed. Cir. 2017) (citations omitted)

Ambiguous “three dimensional” Language Does Not Expressly Disclose Vertical Wordlines As Recited



Wasica

Anticipation requires that a single reference describe the claimed invention with sufficient precision and detail to establish that the subject matter existed in the prior art.... For this reason, it has long been understood that ambiguous references do not, as a matter of law, anticipate a claim.

* * *

[C]laim 6 requires its carrier waves to have a constant frequency.... Record evidence suggests that Oselin could use signals of either constant or nonconstant frequency. Oselin is thus ambiguous as to whether it discloses the pertinent features of claim 6.

Wasica, 853 F.3d at 1284 (quotations and citations omitted)



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

- I. “From Bottom To Top” Means From Lowest To Highest
- II. Dong’s Figures Do Not Expressly Disclose Vertically Arranged Wordlines As Recited
- III. Dong’s “Three Dimensional” Language Does Not Expressly Disclose Vertically Arranged Wordlines As Recited
- IV. Petitioner’s New “Envisage” Theory Fails To Anticipate Vertically Arranged Wordlines As Recited**

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14



Petitioner's New "envisage" Theory Fails To Anticipate Vertically Arranged Wordlines As Recited

Petitioner's Reply

Given the well-developed state of 3D-memory in 2020, a POSITA would "at once envisage" the '941 patent's claimed *bottom-to-top* wordline arrangement upon reading Dong's "three dimensional" NAND disclosure. Pet., 35; *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015); *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022). Numerous industry reports and

Reply 11

Petitioner's Expert

56. In conclusion, in view of the well-developed state of 3D NAND memory in 2020, a POSITA would at once envisage the '941 patent's claimed *bottom to top* wordline arrangement upon reading Dong's disclosure of "three dimensional" NAND (Dong, [0095]) and viewing the vertically oriented memory strings in Figs. 5a and 5g. Certainly, at an absolute minimum, in conjunction with

Ex. 1089 (Liu Reply Decl.) ¶ 56

Kennametal Is Distinguishable



Kennametal

Kennametal does not contest that, with the exception of combining ruthenium binders with PVD coatings, claim 5 of Grab expressly recites all the elements of pending claim 1. ... Because **all the limitations of Kennametal's claim are specifically disclosed in Grab**, the question for the purposes of anticipation is “whether the number of categories and components” disclosed in Grab is so large that the combination of ruthenium and PVD coatings “would not be immediately apparent to one of ordinary skill in the art.”

Kennametal, Inc. v. Ingersoll Cutting Tool Co., 780 F.3d 1376, 1381-82 (Fed. Cir. 2015) (citation omitted)

Forecloses Petitioner's New “envisage” Theory



Nidec

Kennametal does not stand for the proposition that a reference missing a limitation can anticipate a claim if a skilled artisan viewing the reference would “at once envisage” the missing limitation. Rather, *Kennametal* addresses whether the disclosure of a limited number of combination possibilities discloses one of the possible combinations. As we explained, the relevant question was “whether the number of categories and components disclosed in [the prior art reference] is so large that the combination of ruthenium and PVD coatings would not be immediately apparent to one of ordinary skill in the art.”

Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co., 851 F.3d 1270, 1274-75 (Fed. Cir. 2017) (alteration original) (citations omitted)



Petitioner's Expert Did Not Understand The *Kennametal* “envisage” Standard

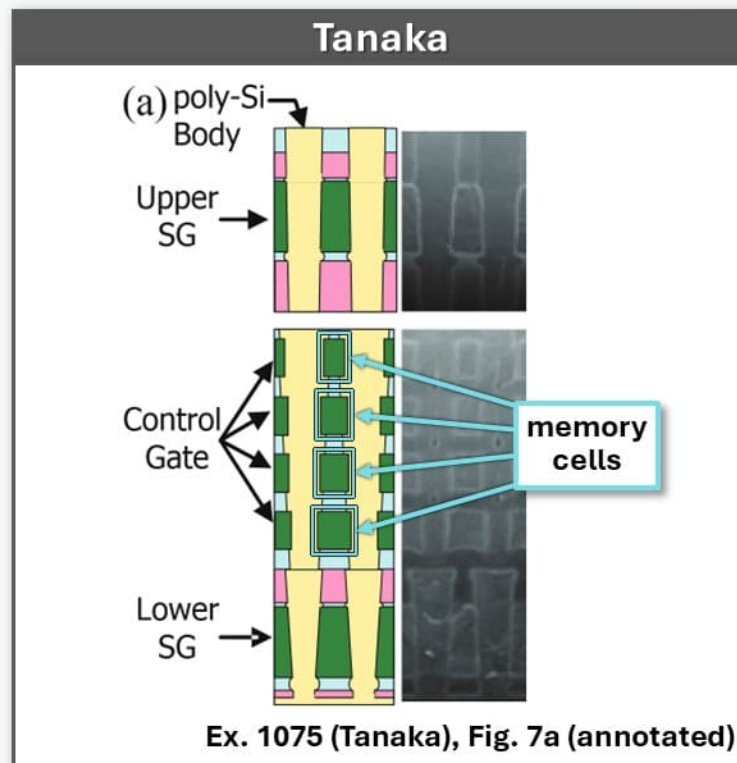
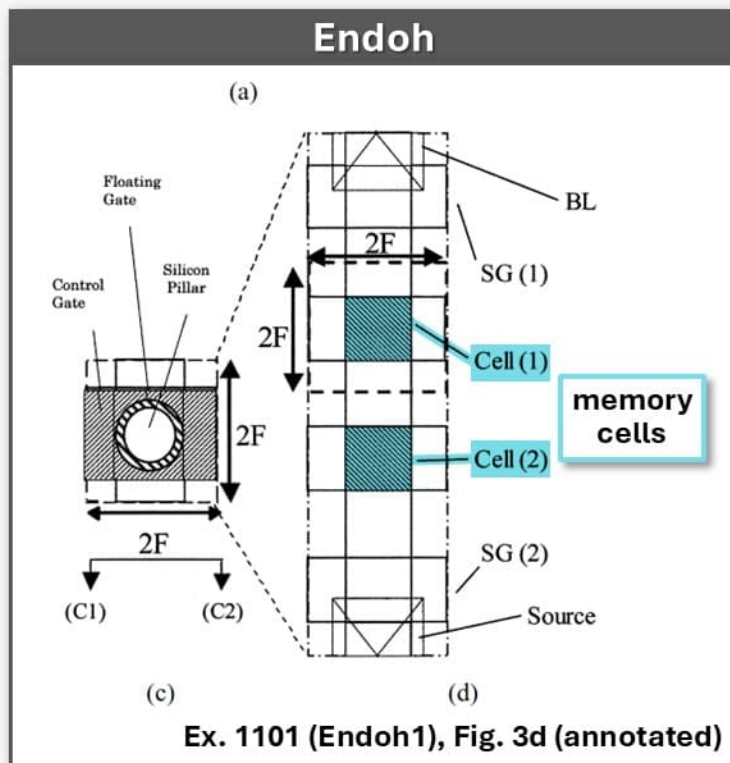
Petitioner's Expert

Q. Dr. Liu, can you identify anywhere in your reply declaration where you set forth your understanding of the law regarding the at once envisage standard?

A. Again, I think the answer is that it is -- I'm opining here that a POSITA in 2020 -- and to be sincere and genuine, and when -- when he or she reads the context of 3D NAND memory in 2020, the vision -- the visual will come to mind right away would be a vertically oriented memory string.

Ex. 2030 (Liu-Dep2), 35:12-21 (objecton omitted)

Petitioner Improperly Relies On Multiple References For Anticipation



Petition

At a minimum, it would have been obvious to a POSITA to utilize a 32-cell memory string given that (1) Dong Fig. 5 is not limited to any particular memory

Pet. 31

Petitioner Improperly Relies On Multiple References For Anticipation



Galderma

Teva's arguments ignore the axiom that a patent claim can only be invalid for anticipation if a single reference discloses each and every limitation of the claimed invention. Turning to another reference "for a very specific teaching" runs afoul of these settled principles.

Here, the district court erred by finding the asserted claims anticipated by the disclosures of McDaniel *and* Manetta, in contravention of settled law.... We refuse to look to Manetta to incorporate a specific disclosure not found in McDaniel...

Galderma Laboratories, L.P. v. Teva Pharms. USA, Inc., 799 F. App'x 838, 843-845 (Fed. Cir. 2020) (emphasis original) (citation omitted)

Petitioner Improperly Relies On Multiple References For Anticipation



Galderma

Though Manetta enables an embodiment of McDaniel, it does not necessarily follow that a POSA reading McDaniel would at once envisage the undisclosed specific Soolantra® formulation that satisfies the claimed efficacy limitations. In any event, we have previously rejected the proposition that “a reference missing a limitation can anticipate a claim if a skilled artisan viewing the reference would ‘at once envisage’ the missing limitation.” *See Nidec Motor Corp. v. Zhongshan Broad Queen Motor Co. Ltd.*, 851 F.3d 1270, 1274–75 (Fed. Cir. 2017). Here, the district court was not permitted “to fill in missing limitations simply because a skilled artisan would immediately envision them.” *Id.*

Galderma Laboratories, L.P. v. Teva Pharms. USA, Inc., 799 F. App'x 838, 844-45 (Fed. Cir. 2020)



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

- I. The Petition Did Not Argue It Would Have Been Obvious To Apply Dong's 2D Program Disturb Method In Vertically Arranged Wordlines As Recited
- II. A POSITA Would Not Apply Dong's 2D Program Disturb Method In Vertically Arranged Wordlines As Recited

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

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Claims 1, 3, 5-7, 11, 13

I. The Petition Did Not Argue It Would Have Been Obvious To Apply Dong's 2D Program Disturb Method In Vertically Arranged Wordlines As Recited

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Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14

The Petition Relied On Dong To Disclose “from bottom to top,” Not Obviousness

Petition

The '941 patent does not define the phrase *bottom to top*, but it was (and is) common in NAND flash memory devices to refer to the source end of a memory string as the “bottom,” and the drain end as the “top.” Liu, ¶¶ 112-113, 120. That common usage will be applied here. Regardless, to the extent *bottom to top* is interpreted to require vertical strings in a 3D NAND memory, Dong discloses its “array of storage elements can be three dimensional” and shows Fig. 5a in a vertical orientation which satisfies the claim. Dong, [0095]; Liu, ¶ 120.

Pet. 35



The Petition's Only Obviousness Position Involved A 32-Cell Memory String, Not Vertical 3D NAND

Petition

Ground 2: Dong renders obvious claims 1, 3, 5-7, 11, and 13 under §103.

Pet. 7

At a minimum, it would have been obvious to a POSITA to utilize a 32-cell memory string given that (1) Dong Fig. 5 is not limited to any particular memory string length; (2) Dong expressly references Lutze which explicitly discloses 32-cell memory strings; and (3) Dong expressly discloses embodiments with 32 cell memory strings (Dong, [0090], [0108]). Liu, ¶¶ 108-111. Moreover, 32-cell (and larger) memory strings were well-known to POSITAs by the Priority Date and would have been obvious to use. Liu, ¶¶ 109-110; Ex. 1006 (“Dong II”), [0010], Fig. 1 (showing 32 wordlines); Costa [0093] (128 cell NAND string); Shirai, [0019] (“Any number of electrode layers 41 may be stacked.”); Ex. 1013 (“Righetti”), Fig. 6 (showing 74 wordlines); Futatsuyama, [0050] (memory string may have “8, 16, 32, 33, 34, 64, 66, 68 or 88” cells).

Pet. 31



The Petition's Only Obviousness Position Involved A 32-Cell Memory String, Not Vertical 3D NAND

Petitioner's Expert

Q. And you mentioned there could be other lengths of memory cells. What did you mean by that?

A. Simple what I said in Paragraph 110. I know that memory string with length of 32, 64, and 128 cells are well-known to a POSITA....

* * *

Q. And in Paragraph 110, you cite numerous other references as support. Right?

A. That's correct.

Ex. 2021 (Liu-Dep1), 79:22-80:13

Petitioner's Expert

110. I note that memory strings with lengths of 32, 64, and 128 cells were well-known to POSITAs and commonplace by the Priority Date and all of them would have been obvious to use, as reflected by a number of references. For

* * * *

string in this example includes 128 data wordlines.” Costa, [0093]. As a third data point, the Shirai reference (discussed further for Ground 4) states that “[a]ny number of electrode layers 41 may be stacked.” Shirai, [0019]. As further example, U.S. Pub. 2019/0102104 (Ex. 1013, “Righetti”) Figure 6 shows a memory device with 74 wordlines. And U.S. Pub. 2012/0163096 (Ex. 1017, “Futatsuyama”) explains that

* * * *

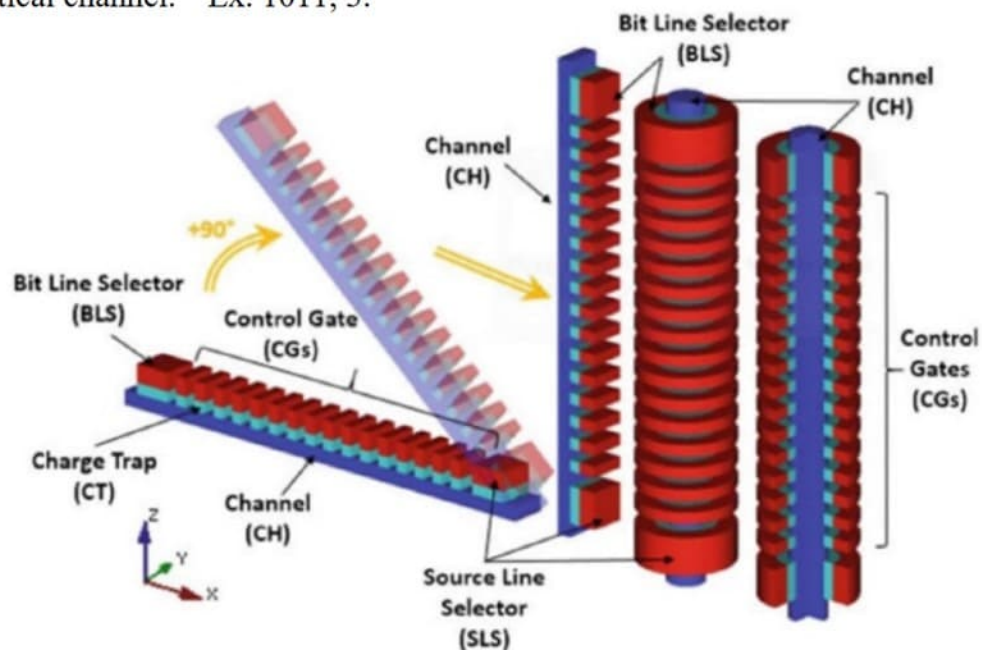
of memory cells in a memory string. Certainly by the 2020 Priority Date, using memory strings with 64 cells or more was common.

Ex. 1004 (Liu Pet. Decl.) ¶ 110

The Petition's Background Section Lacks Specific Motivation To Modify Dong

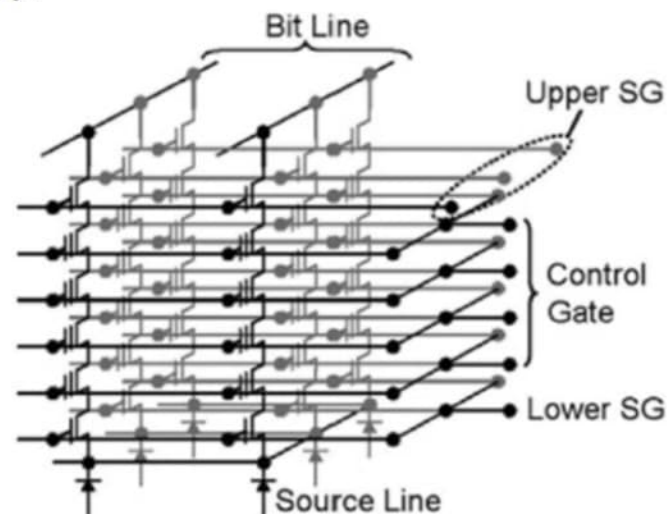
Petition

NAND flash cells” were developed. *Id.*, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1011, 3.



Petition

Ex. 1010, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



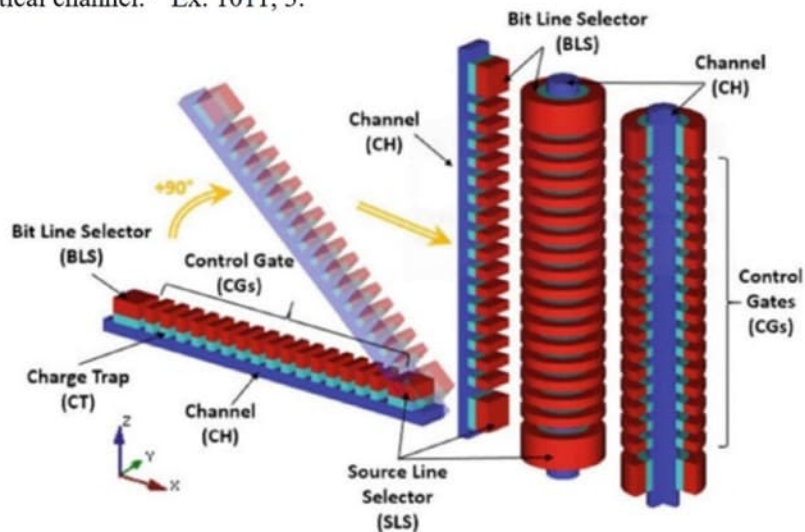
Ex. 1009, 296. Thus, there are many similarities between 2D and 3D NAND flash memory devices, including the techniques and algorithms used to program memory cells. *See* Liu, ¶¶ 49-56.



The Petition's Background Section Lacks Specific Motivation To Modify Dong

Petition

NAND flash cells" were developed. *Id.*, 292. "Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1011, 3.

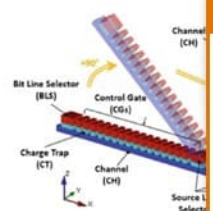


Ex. 1010, 122. Multiple such vertical channels are then repeated in a three-dimensional array:

Pet. 12-13

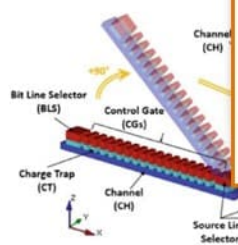
IPR2025-00189

in 2006. *Id.*, 292. "Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside" "resulting" in a "3D structure" with a "vertical channel." Ex. 1012, 3.



IPR2025-00228

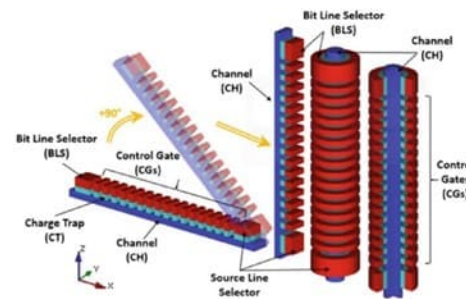
"Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1012, 122 (colors in the original). Multiple vertical channels are repeated in a three-dimensional array:



Ex. 1012, 122 (colors in the original). Multiple vertical channels are repeated in a three-dimensional array: **IPR2025-00228, Paper 1, 16-17**

IPR2025-00245

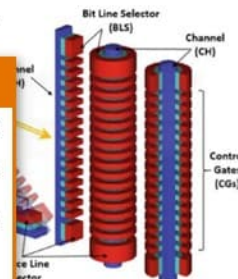
formed as two-dimensional arrays. *Id.*, 58. "Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1009, 3; Banerjee ¶ 43.



Ex. 1010, 122. Multiple such vertical channels are then repeated in a three-dimensional array: **IPR2025-00245, Paper 1, 14-15**

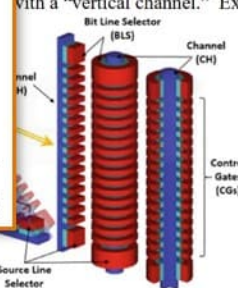
IPR2025-00117

NAND flash cells" were developed. Ex. 1009, 292. "Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1010, 3.



IPR2025-00244

D structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1010, 3.



Ex. 1011, 122. Multiple such vertical channels are then repeated in a three-dimensional array: **IPR2025-00244, Paper 1, 12-13**

Conclusory Expert Testimony Cannot Provide Requisite Motivation

Petitioner's Expert

drain end as the “top.” I apply that common usage here. In any event, even if *bottom to top* were interpreted as requiring vertical memory strings in a 3D NAND device, Dong discloses that its “array of storage elements can be three dimensional.” Dong, [0095]. And Figure 5a itself shows a vertical orientation (consistent with Dong’s disclosure of a “three dimensional” device) which satisfies the *bottom to top* language. Thus, regardless of whether Figure 5a is read as a 2D or 3D memory string it meets the claim language. And, given the similarities between 2D and 3D NAND discussed in the Technology Background section, even a 2D memory string would at a minimum render obvious the *bottom to top* requirement, even if narrowly construed.

POR 48-50; Ex. 1004 (Liu Pet. Decl.) ¶ 120



Conclusory Expert Testimony Cannot Provide Requisite Motivation



KSR

“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”

KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006))



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

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Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14



Petitioner's Own Evidence Says 3D Disturb Is "Much Different" From 2D Disturb

Aritome

The program disturb mechanisms of 3D NAND cells are **much different** from that of 2D NAND cells, because cell structure and array architecture are **totally changed**. The analysis results of program disturb in 3D NAND cells are presented in

Ex. 1009 (Aritome), 354

tunnel oxide during erase. The program disturb conditions and characteristics of 3D cells are **greatly changed** from that of 2D cells, as described in detail in Section 8.4.

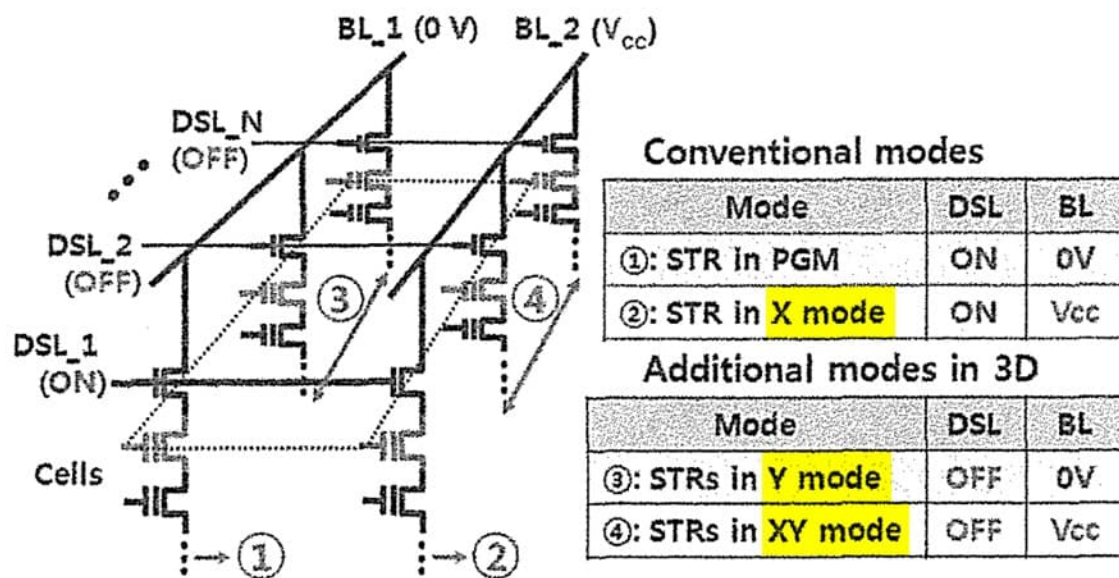
Ex. 1009 (Aritome), 356

Program disturb phenomena and mechanisms of a 3D NAND cell are **much different** from that of a 2D NAND cell.

Ex. 1009 (Aritome), 362

A POSITA Would Not Have Applied Dong's 2D Self-Boosting In Vertical 3D NAND As Recited

Aritome



Ex. 1009 (Aritome), 363 (Fig. 8.11)

In actual array operation, all three program disturb modes occur simultaneously, and thus disturb fail bits appear by statistically complicated circumstance of neighbor cells. Figure 8.14 shows the simulation (model) and measurement (chip) results of the

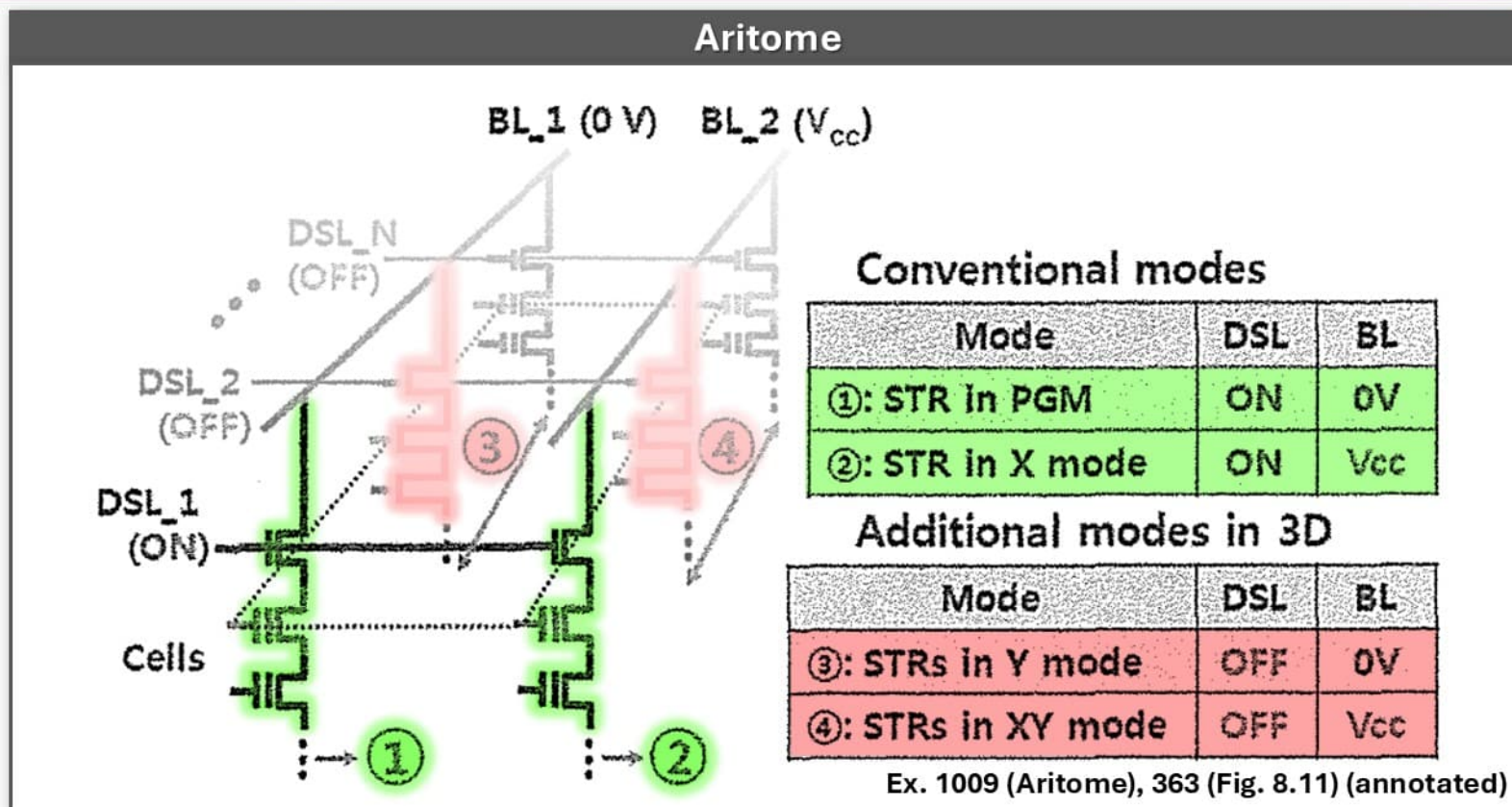
Ex. 1009 (Aritome), 364

Petitioner's Expert

two new modes of Y-mode and XY-mode are added.” *Id.* Program disturb modes ① and ②, in addition to program disturb modes ③ and ④, all need to be addressed in order to reliably operate a 3D NAND during programming.

Ex. 1089 (Liu Reply Decl.) ¶ 68

Dong's 2D Methods Address Only Two Of Four Program Disturb Modes In 3D NAND



Petitioner's Expert

69. The two “new program disturb modes” (*i.e.*, modes ③ and ④) are not the disturb modes Dong was addressing. As Aritome explains, the “[c]onventional”

Ex. 1089 (Liu Reply Decl.) ¶ 69

3D NAND's NLSB Effect Addresses Program Disturb Without 2D NAND Self-Boosting

Jeong

memories. Moreover, the 3D NAND flash memory structure stacks the cells vertically to increase capacity [4-5]. However, the channel can be floating because the channel of a 3D NAND flash memory is not connected to the body. This could lead to a DCP effect [6]. In addition, when a high voltage is applied, the electrons of the cell are collected due to the potential difference, and the NLSB phenomenon occurs [7]. The NLSB effect does not require the local boosting scheme used in conventional 2D NAND, because it can achieve a sufficiently high potential even if the number of stacks is increased.

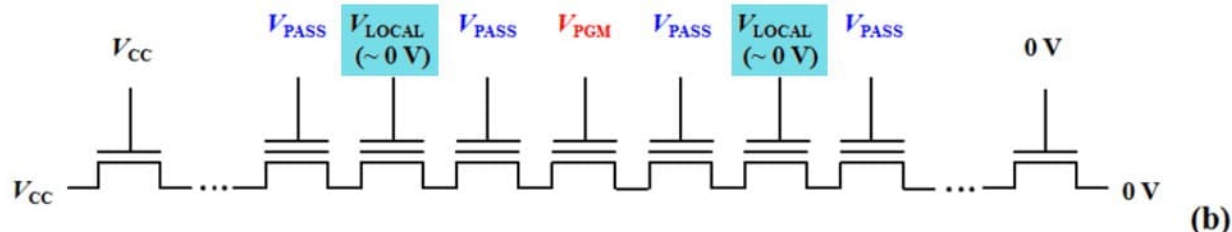
Ex. 2027 (Jeong), 1

Kang

cannot be applied to the channels of the main cells. For the first time, it was found that during program operation, the inhibited channel becomes a floating node and the natural local self-boosting (NLSB) effect occurs. The NLSB effect allows a sufficiently high boosted potential of an inhibited string to be achieved without a local self-boosted program-inhibit (SBPI) scheme, even if the number of stacks increases. This

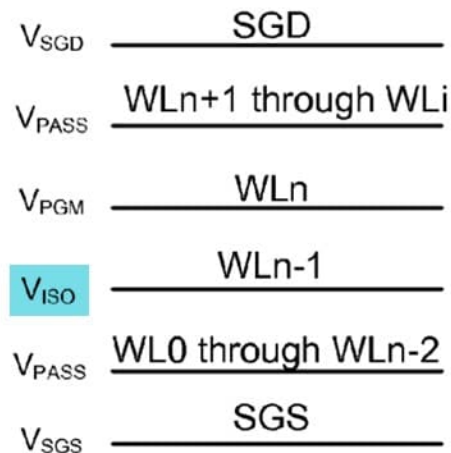
Ex. 2024 (Kang), 1

Local Self-Boosting Scheme



Ex. 2024 (Kang), Fig. 1(b) (annotated)

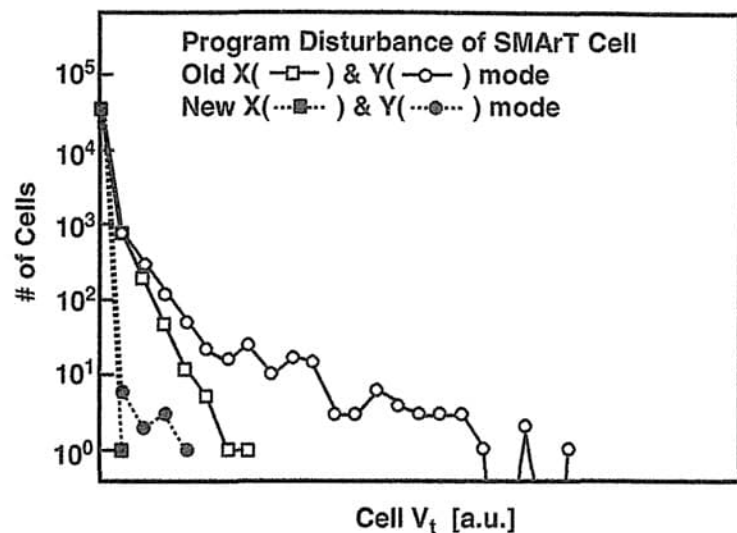
Dong



Ex. 1005 (Dong), Fig. 5a (annotated)

A POSITA Would Not Have Applied Dong's 2D Self-Boosting In Vertical 3D NAND As Recited

Aritome



Ex. 1009 (Aritome), 364 (Fig. 8.12)

Aritome

In order to suppress a program disturbance in a 3D NAND cell, several approaches to reduce leakage current through DSL were proposed [6]. They are (1) high V_t of DSL, (2) applying negative bias to DSL, and (3) inserting dummy word lines between DSL and edge word line. Both (1) and (2) can decrease a large leakage

Ex. 1009 (Aritome), 363

current of DSL in a 3D cell. And (3) can control the potential drop from boosting voltage to the voltage applied on DSL, and (3) can also manage the hot carrier generation at edge word-line region by relaxing a high lateral electric field. Therefore, the dummy WL condition (bias, V_t setting, number of dummy WLs, etc.) have to be carefully designed. Figure 8.12 shows the improvement results of program disturb characteristics of X and Y mode by applying conditions of (1), (2), and (3) [2].

Ex. 1009 (Aritome), 364



A POSITA Would Not Have Applied Dong's 2D Self-Boosting In Vertical 3D NAND As Recited

Jeong

3. Conclusions

In this paper, we analyzed HCI phenomenon due to excessive NLSB effect in 3D NAND flash memory. DCP reduces the NLSB effect and reduces the channel potential during program operation, which results in program disturb. Therefore, to maximize the NLSB effect and reduce the occurrences of program disturb, it is important to reduce the DCP phenomenon. However, if the NLSB effect is increased and the potential of the program cell becomes higher, the channel potential difference with the adjacent cell increases and HCI phenomenon occurs. That is, when the NLSB effect becomes small, program disturb occurs, and when the NLSB effect becomes too large, the HCI phenomenon occurs. Therefore, it is important to maintain an appropriate channel potential in 3D NAND flash memory.

Ex. 2027, 2



No Reasonable Expectation Of Success

Petition

Reply's Construction

Regarding vertical memory strings, PO ignores POSITA knowledge—which is assessed in 2020, not 2007. *Oracle Am., Inc. v. Google, Inc.*, 606 F. App'x 990, 995 (Fed. Cir. 2015). Here, PO does not dispute Petitioner's level of skill in the art. Pet., 22-23; POR, 9; EX2028, ¶46; EX1100, ¶¶25-26. Any assertion that applying wordline voltages in vertical strings instead of horizontal ones requires undue experimentation lacks credibility. Liu_Reply, ¶¶83-87. Moreover, Dong is presumptively enabled. *In re Antor Media Corp.*, 689 F.3d 1282, 1288-89 (Fed. Cir. 2012). Although manufacturing vertical 3D-memory is not at issue (only programming a memory string is), the '941 patent itself presumes a POSITA can construct vertical 3D-memory. EX1087 (extensive manufacturing disclosure); EX1075, Fig. 7(a)-(c) (manufactured device).

Reply 25



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

I. Petition's Original Mappings Fail

II. "A Program Operation" Does Not Include A Verify Phase

III. Reply's Improper New Mappings Fail Under PO's Construction

IV. Reply's Improper New Mappings Fail Under Petitioner's Construction

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

I. Petition's Original Mappings Fail

II. "A Program Operation" Does Not Include A Verify Phase

III. Reply's Improper New Mappings Fail Under PO's Construction

IV. Reply's Improper New Mappings Fail Under Petitioner's Construction

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14



Claims 8 And 9 Recite “portion” Limitations

5. A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first word line to a kth word line from bottom to top, the second portion formed above the first portion and comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:

applying a first voltage to the first word line to an (x-2)th word line when an xth word line is used to perform a program operation;

applying a second voltage to an (x-1)th word line; and
applying a third voltage to an (x+1)th word line;

wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

9. The program method of claim 5, wherein:
the first voltage has a first level if the xth word line is in the first portion;
the first voltage has a second level if the xth word line is in the second portion; and
the first level is lower than the second level.

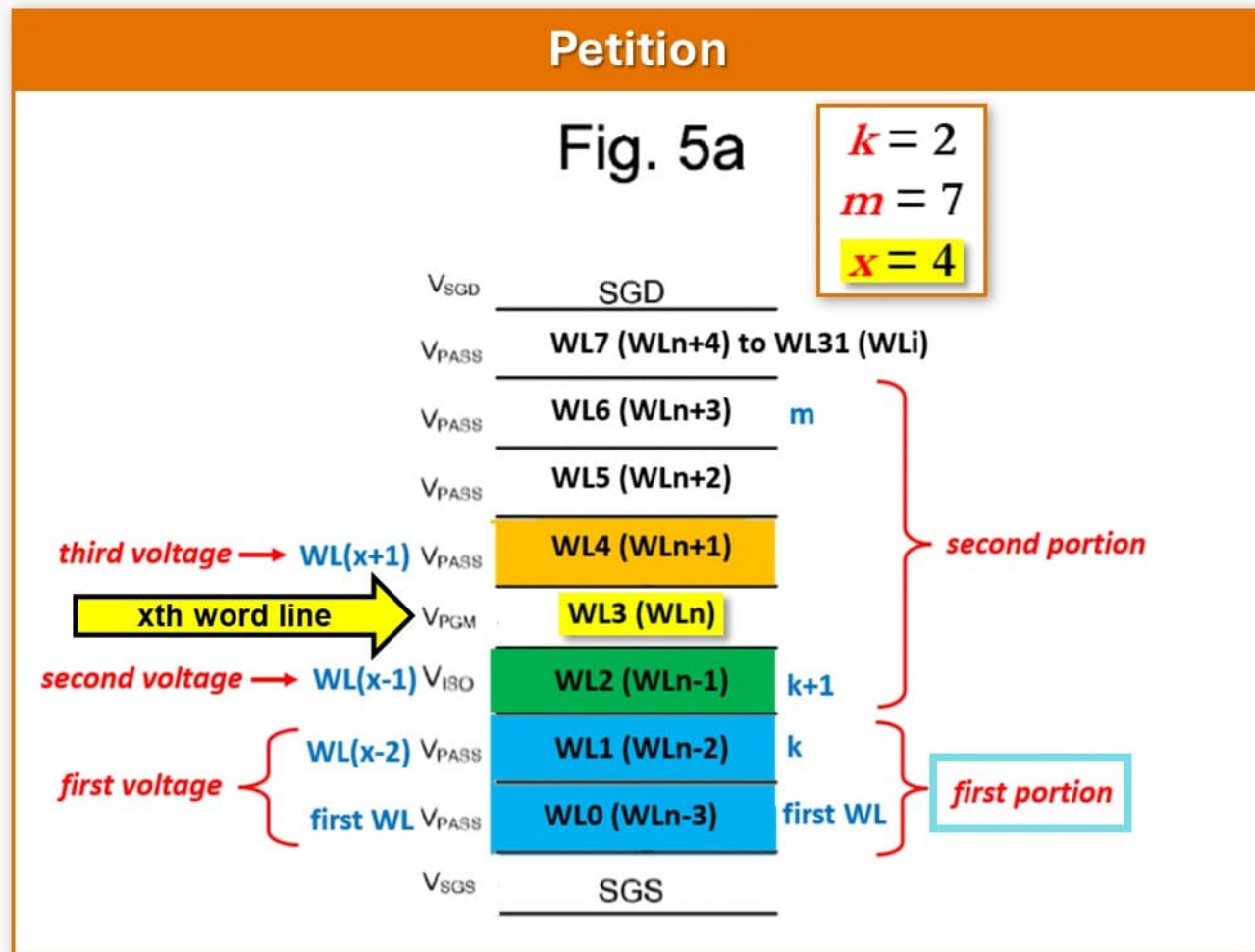
7. The program method of claim 5, wherein the memory further comprises a third portion formed above the second portion, the third portion comprises an (m+1)th word line to an nth word line from bottom to top, and the program method further comprises:

applying a fourth voltage to the (x+2)th word line to the nth word line;

wherein $m < n$, and $x < (n-1)$.

8. The program method of claim 7, wherein:
the first voltage has a first level if the xth word line is in the first portion;
the first voltage has a second level if the xth word line is in the second portion;
the first voltage has a third level if the xth word line is in the third portion; and
the first level is lower than the second level, and the second level is lower than the third level.

Petition's Mappings For Claims 8 And 9 Fail

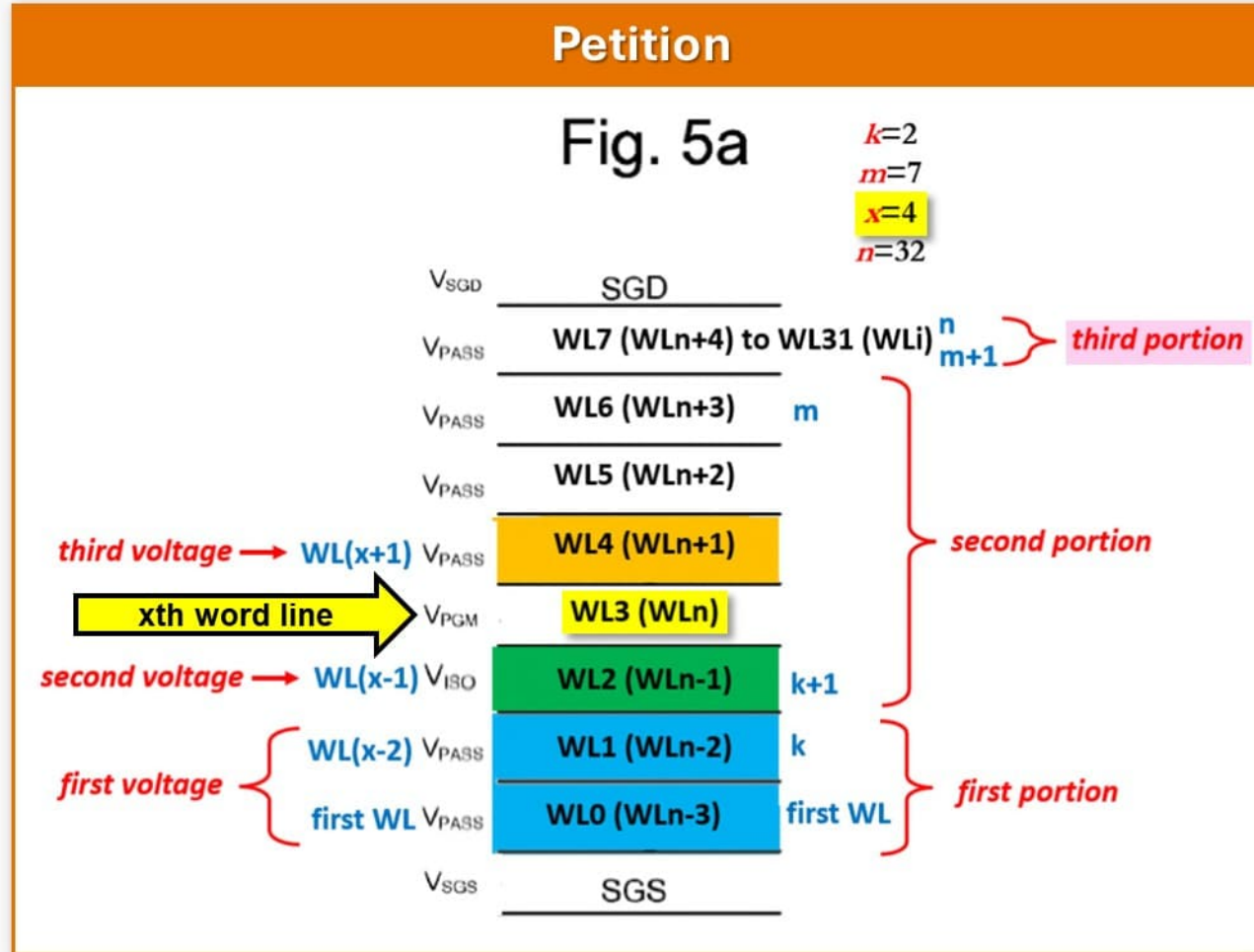


5. A program method of a memory, the memory compris-
 * * *
 wherein x , k and m are positive integers, $1 < k < m$ and $3 \leq x$.

8. The program method of claim 7, wherein:
 the first voltage has a first level if the x th word line is in
 the first portion;
 the first voltage has a second level if the x th word line is
 in the second portion;
 the first voltage has a third level if the x th word line is in
 the third portion; and
 the first level is lower than the second level, and the
 second level is lower than the third level.

9. The program method of claim 5, wherein:
 the first voltage has a first level if the x th word line is in
 the first portion;
 the first voltage has a second level if the x th word line is
 in the second portion; and
 the first level is lower than the second level.

Petition's Mapping For Claim 8 Fails



Pet. 46-47 (annotating Ex. 1005 (Dong), Fig. 5a)

8. The program method of claim 7, wherein:
the first voltage has a first level if the **xth word line** is in the **first portion**;
the first voltage has a second level if the xth word line is in the second portion;
the first voltage has a third level if the xth word line is in the third portion; and
the first level is lower than the second level, and the second level is lower than the third level.

Ex. 1001 ('941 Patent), Claim 8



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

I. Petition's Original Mappings Fail

II. "A Program Operation" Does Not Include A Verify Phase

III. Reply's Improper New Mappings Fail Under PO's Construction

IV. Reply's Improper New Mappings Fail Under Petitioner's Construction

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14

“a program operation”

1. A memory comprising:
a first portion comprising an (m+1)th word line to an nth word line from bottom to top; and
a second portion formed below the first portion and comprising a (k+1)th word line to an mth word line from bottom to top; and
a controller configured to apply a first voltage to an (x+2)th word line to the nth word line, a second voltage to an (x+1)th word line, a third voltage to an (x-1)th word line, a fourth voltage to the (m+1)th word line to an (x-2)th word line, and a fifth voltage to the (k+1)th word line to the mth word line when an xth word line is used to perform a program operation;
wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

5. A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first word line to a kth word line from bottom to top, the second portion formed above the first portion and comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:
applying a first voltage to the to the first word line to an (x-2)th word line when an xth word line is used to perform a program operation;
applying a second voltage to an (x-1)th word line; and
applying a third voltage to an (x+1)th word line;
wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

11. A program method of a memory, the memory comprising a first portion and a second portion formed below the first portion, the first portion comprising an (m+1)th word line to an nth word line from bottom to top, the second portion comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:
applying a first voltage to an (x+2)th word line to the nth word line when an xth word line is used to perform a program operation;
applying a second voltage to an (x+1)th word line;
applying a third voltage to an (x-1)th word line;
applying a fourth voltage to the (m+1)th word line to an (x-2)th word line; and
applying a fifth voltage to the (k+1)th word line to the mth word line;
wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

Ex. 1001 ('941 Patent), Claim 1, 5, 11



“a program operation”

Petition

For purposes of this Petition, Petitioner submits the '941 Patent's claims do not require further construction and should receive their plain and ordinary meaning.

Pet. 22

Reply

“iteratively performing charge injection and verification”

Reply 3-6; Ex. 1089 (Liu Reply Decl.) ¶¶ 27-37

PO's Construction

Plain and ordinary meaning; “an operation performed by applying a program voltage to a selected wordline to program a selected memory cell”

Petition Never Construed “a program operation”

Petition

Due to the close proximity of memory cells—and the application of these various different voltages—NAND is subject to a “phenomenon” known as “[p]rogram disturb.” Ex. 1009, 52. “Program disturb” involves “the threshold

* * *

to either avoid or minimize program disturb. *Id.* For instance, increasing the V_{pass} voltage applied to unselected wordlines increases the so-called “boosting” voltage in adjacent NAND strings—a voltage that is induced in part by wordline voltage—thereby reducing program disturb in those strings. *Id.* But this also has the effect of increasing program disturb in the string that includes the programmed cell. *Id.* A lower V_{pass} has the opposite effect, reducing program disturb in the programmed cell’s string, but increasing it in adjacent strings. *Id.*; *see also Liu*, ¶¶ 59-62.

Pet. 15

Petition Never Construed “a program operation”

Petition

NAND flash programming is an iterative process involving application of a programming pulse followed by program verification pulses. Dong, Figs. 19 (flow chart) and 20 (showing program and verification pulses); Costa, Fig. 6 (showing program and verification pulses). A POSITA knew that a “disturb free” memory programming operation would require both aspects of the operation (*viz.*, application of the program pulse(s) and verification pulses) to be disturb free. Liu, ¶ 208. A POSITA would have recognized that both phenomena should be addressed to improve the reliability of flash devices during the iterative programming operation. Thus, a POSITA would have considered using Dong’s techniques with other techniques for a more comprehensive improvement of memory reliability. Liu, ¶¶ 208-209.

Pet. 71



Petitioner's Construction Was Not Revealed Until Dr. Liu's First Deposition

Petitioner's Expert

Q. [F]or the limitation, "When an Xth wordline is used to perform a program operation," the phrase "a program operation" is interpreted by you to include both of those phases, the program and verifying phase?

A. That's correct.

Ex. 2021 (Liu-Dep1), 211:1-18



Petitioner's Expert's Original Declaration Lacks Any Claim Construction For “a program operation”

Petitioner's Expert

60. During a typical programming operation, the memory cells are programmed according to a wordline programming order as the operation is performed from one end of the string to the other end. NAND memory programming typically involves iteratively repeating two related, but distinct, operations. These operations are applying a programming voltage (sometimes called a “pulse”) to actually programming the memory cell by transferring charge to it to change its threshold voltage. The other phase of a typical programming operation is the verify phase where the memory cell being programmed is read to determine it has been sufficiently programmed (*i.e.*, its threshold voltage has moved to the desired level). If not, additional programming pulses are applied, which may increase in intensity with each iteration. As such, the programming operation iterates through alternating programming pulses and verification/read operations. Many references describe this process, including Dong Figure 20 below. Dong (Ex. 1005), [0132] (describing

Ex. 1004 (Liu Pet. Decl.) ¶ 60

Specification Supports “a program operation” Does Not Include Verify

'941 Patent

In the text, when a word line is said to be programmed, it may mean the word line is used to performed a program operation. A program operation said in the text may be an operation for programming a memory cell formed using, for example, a set of transistors.

When an x th word line WL_x is used to performed a program operation, the controller 190 may apply a program voltage V_{pgm} to the x th word line WL_x ; the controller 190 may apply a first voltage $V1$ to the first word line $WL1$ to an $(x-2)$ th word line $WL(x-2)$; the controller 190 may apply a second voltage $V2$ to an $(x-1)$ th word line $WL(x-1)$; and the controller 190 may apply third voltage $V3$ is applied to an $(x+1)$ th word line $WL(x+1)$. x , k and m are positive integers, $1 < k < m$ and $3 \leq x$.

As shown in FIG. 1, the controller 190 may apply a fourth voltage $V4$ to an $(x+2)$ th word line $WL(x+2)$ to the m th word line WL_m when the x th word line WL_x is used to performed the program operation, and $x < m-1$.

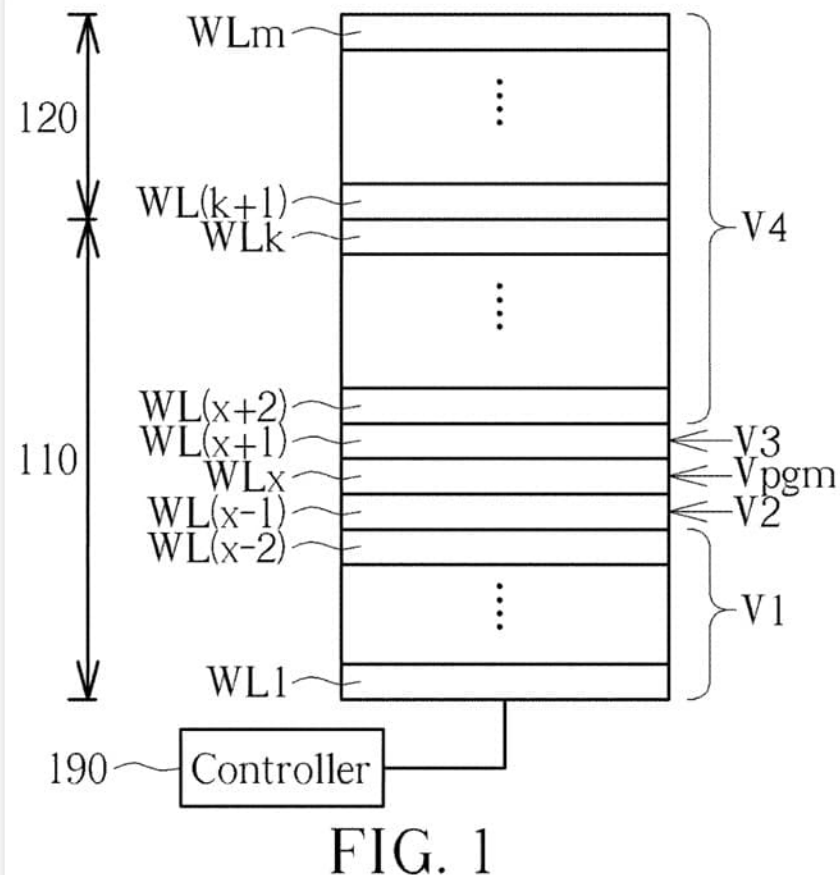


FIG. 1

Ex. 1001 ('941 Patent), 3:4-21, Fig. 1



Claims Support “a program operation” Does Not Include Verify

1. A memory comprising:

a first portion comprising an (m+1)th word line to an nth word line from bottom to top; and

a second portion formed below the first portion and comprising a (k+1)th word line to an mth word line from bottom to top; and

a controller configured to apply a first voltage to an (x+2)th word line to the nth word line, a second voltage to an (x+1)th word line, a third voltage to an (x-1)th word line, a fourth voltage to the (m+1)th word line to an (x-2)th word line, and a fifth voltage to the (k+1)th word line to the mth word line when an xth word line is used to perform a program operation;

wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

5. A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first word line to a kth word line from bottom to top, the second portion formed above the first portion and comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:

applying a first voltage to the first word line to an (x-2)th word line when an xth word line is used to perform a program operation;

applying a second voltage to an (x-1)th word line; and
applying a third voltage to an (x+1)th word line;

wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

11. A program method of a memory, the memory comprising a first portion and a second portion formed below the first portion, the first portion comprising an (m+1)th word line to an nth word line from bottom to top, the second portion comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:

applying a first voltage to an (x+2)th word line to the nth word line when an xth word line is used to perform a program operation;

applying a second voltage to an (x+1)th word line;

applying a third voltage to an (x-1)th word line;

applying a fourth voltage to the (m+1)th word line to an (x-2)th word line; and

applying a fifth voltage to the (k+1)th word line to the mth word line;

wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

Ex. 1001 ('941 Patent), Claims 1, 5, 11



Specification Supports “a program operation” Does Not Include Verify

'941 Patent

A three-dimensional structure of a memory can include a plurality of layers so as to store more data on a same area. This structure has been proved to be effective for increasing capacity of memory.

However, program disturbance will become more significant when the number of layers is increased. Program disturbance will lead to a higher failure rate of programming a memory. In addition, pass voltage disturbance also occurs when using a memory with a plurality of layers.

Hence, a solution for reducing program disturbance and pass voltage disturbance when operating a three-dimensional memory is in need in the field.

In summary, by using a memory sectioned to have a plurality of portions and applying voltages to the word lines of the memory according to the portions, program disturbance and pass voltage disturbance may be reduced according to simulations and experiments. *In addition, by using a*

Ex. 1001 ('941 Patent), 1:30-41, 6:39-43

PO's Expert

148. As I discussed above in Section VI.B, the '941 Patent discloses a solution for reducing program disturb and pass voltage disturb on unselected wordlines when a program voltage is applied to a selected wordline. Ex. 1001, 1:34-41, 1:19-22. A POSITA would understand that these disturbances only occur when applying voltages to intentionally program a cell (to intentionally change its threshold voltage). To implement this solution, the '941 Patent describes “[a] program operation” as “an operation for programming a memory cell.” *Id.* 3:6-8.

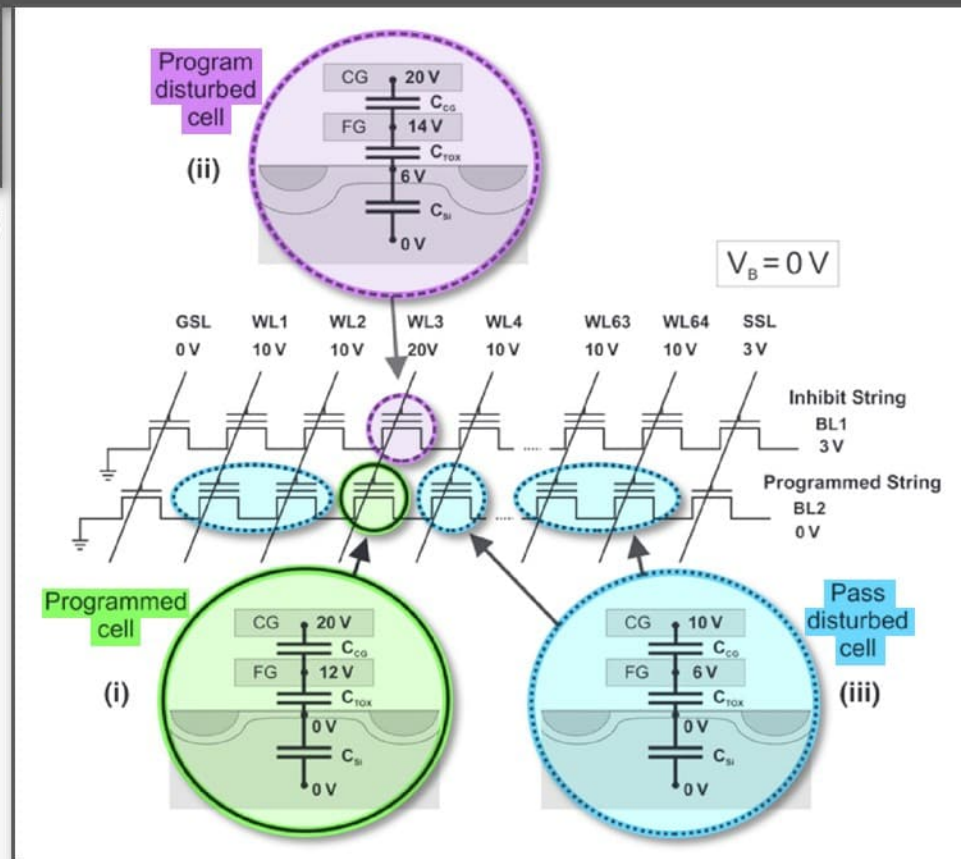
Ex. 2028 (Khatri POR Decl.) ¶ 148

Program And Pass Voltage Disturbances Only Occur During Charge Injection Phase

Michelsoni

Fig. 4.10 Voltage conditions during program operation in the NAND array. The memory cell at the crossing point of WL3 and BL2 is programmed; several other cells are disturbed by either program disturb or pass disturb

Ex. 1010 (Michelsoni), 88 (annotated)



Petition Supports “a program operation” Lacks Verify

Petition

One important aspect of NAND flash memory is “programming,” which refers to “saving” or “writing” data to a memory cell. Liu, ¶ 54. To program a particular NAND memory cell in a memory string, a “high-voltage V_{pgm} ” is applied to the wordline connected to the cell—known as the “selected” wordline—while “keeping” the string’s bit line at “0V.” Ex. 1009, 44. This causes electron movement into the cell and sets the cell’s threshold voltage to a value within a specific range. *Id.*, 45. Because the selected wordline also is connected to cells in other strings, an “inhibit” voltage is applied to these strings’ bit lines to prevent undesired programming. *Id.*, 46. A lower “ V_{pass} ” voltage is also applied to all unselected wordlines. *Id.*, 44-46; Liu, ¶ 57-59.

Pet. 14

Aritome

The program operation of a NAND flash cell is performed by applying high-voltage V_{pgm} to control gate (CG) while keeping substrate/source/drain 0 V, as shown in Fig. 2.10. Electrons are injected to the floating gate (FG) by a Fowler–Nordheim (FN) tunneling mechanism through the tunnel oxide. V_t of cell has a positive shift.

Ex. 1009 (Aritome), 44



Petitioner's Extrinsic Evidence Supports “a program operation” Lacks Verify

Micheloni

The failure mechanism of a read disturb error is similar to the mechanism of a normal program operation. A program operation applies a high programming voltage (e.g., +15 V) to the cell to change the cell's threshold voltage to the desired range. Similarly, a read operation applies a *high pass-through voltage* (e.g., +6 V) to *all other cells* that share the same bitline with the cell that is being read. Although the

Ex. 1010 (Micheloni), 280

Aritome

After the program operation, a verify operation is performed to detect the memory cells which require more time to reach the “1” programmed state. In the verify

Ex. 1009 (Aritome), 119



Petitioner's Expert's Prior Testimony Contradicts Petitioner's Construction

Petitioner's Expert's *Prior* Testimony

The program operation is a pulse that creates charge in the storage region and the verify operation determines whether the pulse was sufficient to properly program the cell.

Ex. 2022 (Liu IPR2024-00792 Pet. Decl.) ¶ 81

248. Costa discloses using its read operations to verify programming.

* * *

(program-read (verify) loop). Again, the read (verify) occurs after the program operation to verify whether the program operation was successful. See Ex. 1008,

Ex. 2022 (Liu IPR2024-00792 Pet. Decl.) ¶ 248

66. The read and verify operations are “virtually identical” operations. Ex. 1003 ¶ 189. Specifically, a verify operation is a read operation executed after a program operation. *Id.* ¶ 192. All that is required is to slightly adjust the read

Ex. 2023 (Liu IPR2024-00792 Reply Decl.) ¶ 66

Petitioner's Expert's *Current* Testimony

28. In either scenario (single-level cell or multi-level cell), A POSITA would understand that a *program operation* includes iteratively performing two steps: a charge injection phase (sometimes called a programming phase) where a programming pulse is applied, and a verify phase (*i.e.*, determining if additional charge is needed). The steps are iterative because, if verification confirms that

Ex. 1089 (Liu Reply Decl.) ¶ 28

would understand that the term. A *program operation* is not complete until the correct amount of charge is stored, which typically requires multiple iterations of charge injection and verification. This is because it is difficult to store just the right

Ex. 1089 (Liu Reply Decl.) ¶ 30

[A] POSITA [would] understand that it include as we see both Costa, Dong, even Aritome, that the program operation as understood by POSITA would include both injecting phase and verification phase.

Ex. 2021 (Liu-Dep1), 216:15-218:16



Costa Discloses *Read* Disturb, Not The Disturbances During Charge Injection

Costa

[0122] A subset of the unselected drain side word lines including $WLn+2$ through $WL127$ receive a lower read pass voltage V_{readL} . V_{readL} is a lowest read pass voltage used in one example. For example, V_{readL} may be several millivolts less (e.g., 5.2V) than the standard read pass voltage V_{read} . The lower read pass voltage V_{readL} may be used because the word lines on the drain side have not undergone programming, and thus the corresponding memory cells should be in the erased state. Accordingly, a lower read pass voltage V_{readL} can be used while still ensuring that these memory cells operate as pass gates. Additionally, the lower level of V_{readL} may cause less read disturb whereby a memory cell is unintentionally programmed by the read pass voltage.

Ex. 1012 (Costa), [0122]



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

I. Petition's Original Mappings Fail

II. "A Program Operation" Does Not Include A Verify Phase

III. Reply's Improper New Mappings Fail Under PO's Construction

IV. Reply's Improper New Mappings Fail Under Petitioner's Construction

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14

Petitioner's Expert Unaware Of New Mappings Until Reply

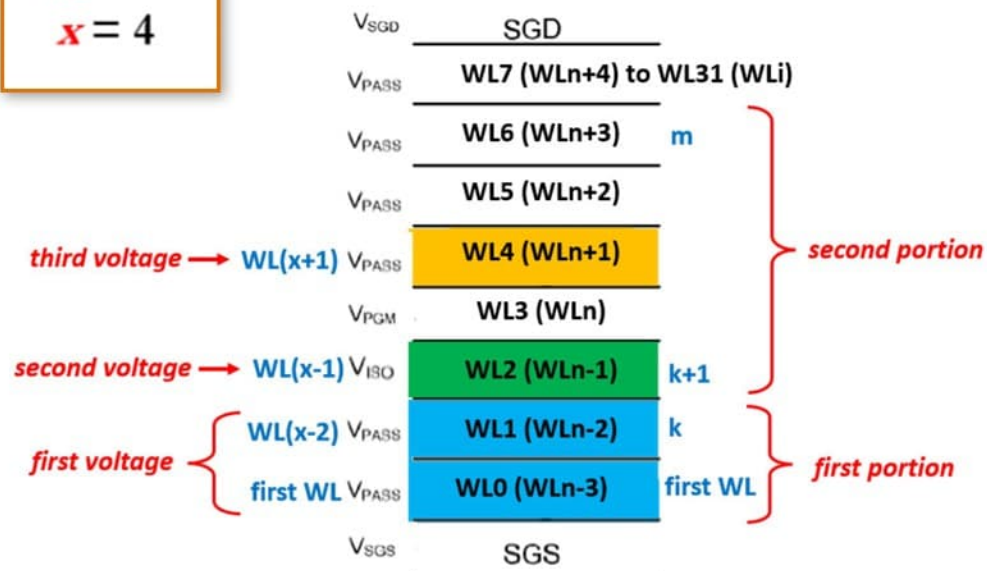
Petition

Fig. 5a

$k = 2$

$m = 7$

$x = 4$



locate all of the variables, etc. being sued in one place for reference. I wish to emphasize that the mappings below are just examples and that other mappings could also satisfy claim 5.

Ex. 1004 (Liu Pet. Decl.), ¶ 115 (Fig. 5a)

Petitioner's Expert

Q. Sitting here today, are you aware of any other mappings to satisfy Claim 5?

A. Not at the moment, no.

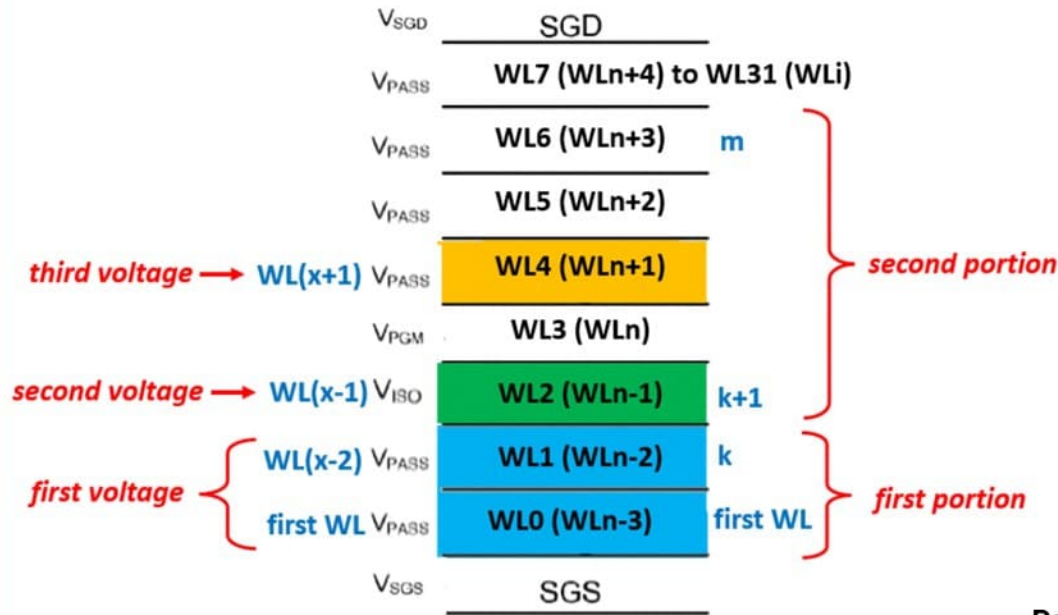
Ex. 2021 (Liu-Dep1), 64:19-65:7; see *id.* 67:2-19 (Claim 1)



Petitioner's New Mapping For Claim 9

Petition

Fig. 5a



Pet. 33

Reply

	VSGD		
WL31	(Vpass)	(Vpass)	m=32
WL30	(Vpass)	(Vpass)	
WL29	(Vpass)	(Vpass)	
WL28	(Vpass)	(Vpass)	
WL27	(Vpass)	(Vpass)	
WL26	(Vpass)	(Vpass)	
WL25	(Vpass)	(Vpass)	
WL24	(Vpass)	(Vpass)	
WL23	(Vpass)	(Vpass)	
WL22	(Vpass)	(Vpass)	
WL21	(Vpass)	(Vpass)	
WL20	(Vpass)	V3 (Vpass)	X+1
WL19	(Vpass)	VPGM	X=20
WL18	(Vpass)	V2 (Viso)	X-1
WL17	(Vpass)	V1 (Vpass)	X-2
WL16	(Vpass)	V1 (Vpass)	
WL15	(Vpass)	V1 (Vpass)	k=16
WL14	(Vpass)	V1 (Vpass)	
WL13	(Vpass)	V1 (Vpass)	
WL12	(Vpass)	V1 (Vpass)	
WL11	(Vpass)	V1 (Vpass)	
WL10	(Vpass)	V1 (Vpass)	
WL9	(Vpass)	V1 (Vpass)	
WL8	(Vpass)	V1 (Vpass)	
WL7	(Vpass)	V1 (Vpass)	
WL6	(Vpass)	V1 (Vpass)	
WL5	(Vpass)	V1 (Vpass)	X+2
WL4	V3 (Vpass)	V1 (Vpass)	X+1
WL3	VPGM	V1 (Vpass)	X=4
WL2	V2 (Viso)	V1 (Vpass)	X-1
WL1	V1 (Vpass)	V1 (Vpass)	X-2
WL0	V1 (Vpass)	V1 (Vpass)	
VSGS			

Reply 28-29

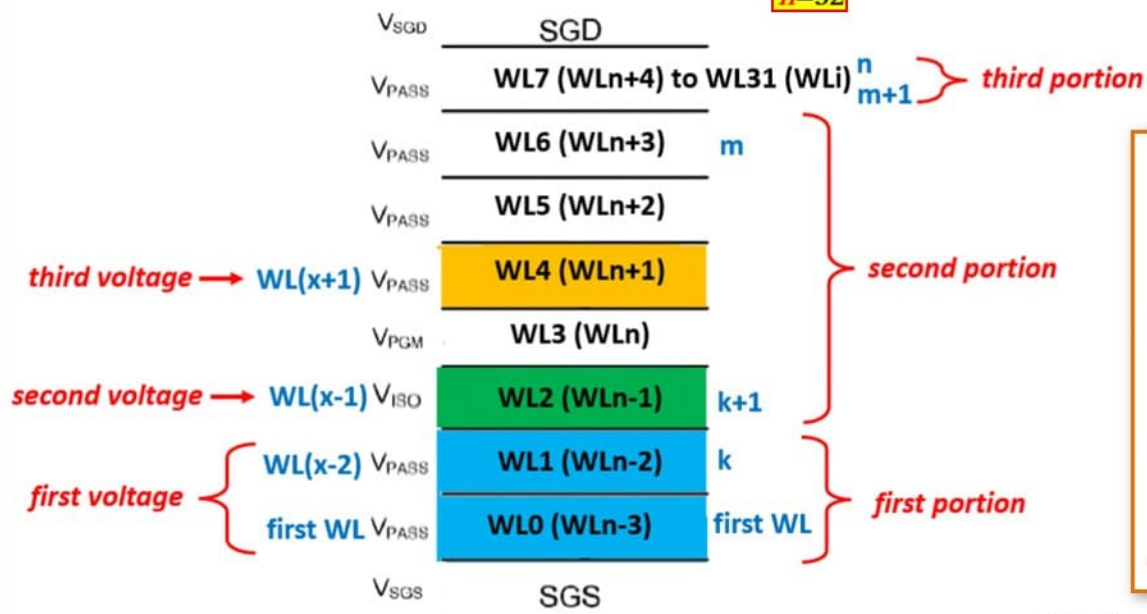


Petitioner's New Mapping For Claim 8

Petition

Fig. 5a

$k=2$
 $m=7$
 $x=4$
 $n=32$



Pet. 47

Reply

	VSGD			
	(Vpass)	(Vpass)	V4 (Vpass)	
WL31	(Vpass)	(Vpass)	V4 (Vpass)	$n=32$
WL30	(Vpass)	(Vpass)	V4 (Vpass)	X+2
WL29	(Vpass)	(Vpass)	V3 (Vpass)	X+1
WL28	(Vpass)	(Vpass)	VPGM	X=29
WL27	(Vpass)	(Vpass)	V2 (Viso)	X-1
WL26	(Vpass)	(Vpass)	V1 (Vpass)	X-2
WL25	(Vpass)	(Vpass)	V1 (Vpass)	
WL24	(Vpass)	(Vpass)	V1 (Vpass)	
WL23	(Vpass)	(Vpass)	V1 (Vpass)	$m=24$
WL22	(Vpass)	(Vpass)	V1 (Vpass)	
WL21	(Vpass)	(Vpass)	V1 (Vpass)	X+2
WL20	(Vpass)	V3 (Vpass)	V1 (Vpass)	X+1
WL19	(Vpass)	VPGM	V1 (Vpass)	X=20
WL18	(Vpass)	V2 (Viso)	V1 (Vpass)	X-1
WL17	(Vpass)	V1 (Vpass)	V1 (Vpass)	X-2
WL16	(Vpass)	V1 (Vpass)	V1 (Vpass)	
WL15	(Vpass)	V1 (Vpass)	V1 (Vpass)	$k=16$
WL14	(Vpass)	V1 (Vpass)	V1 (Vpass)	
WL13	(Vpass)	V1 (Vpass)	V1 (Vpass)	
WL12	(Vpass)	V1 (Vpass)	V1 (Vpass)	
WL11	(Vpass)	V1 (Vpass)	V1 (Vpass)	
WL10	(Vpass)	V1 (Vpass)	V1 (Vpass)	
WL9	(Vpass)	V1 (Vpass)	V1 (Vpass)	
WL8	(Vpass)	V1 (Vpass)	V1 (Vpass)	
WL7	(Vpass)	V1 (Vpass)	V1 (Vpass)	
WL6	(Vpass)	V1 (Vpass)	V1 (Vpass)	
WL5	(Vpass)	V1 (Vpass)	V1 (Vpass)	X+2
WL4	V3 (Vpass)	V1 (Vpass)	V1 (Vpass)	X+1
WL3	VPGM	V1 (Vpass)	V1 (Vpass)	$X=4$
WL2	V2 (Viso)	V1 (Vpass)	V1 (Vpass)	X-1
WL1	V1 (Vpass)	V1 (Vpass)	V1 (Vpass)	X-2
WL0	V1 (Vpass)	V1 (Vpass)	V1 (Vpass)	
VSGS				

Reply 30

Claims 8 And 9 Recite “first voltage” Level Increase Limitations

5. A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first word line to a kth word line from bottom to top, the second portion formed above the first portion and comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:

applying a first voltage to the to the first word line to an (x-2)th word line when an xth word line is used to perform a program operation;

applying a second voltage to an (x-1)th word line; and
applying a third voltage to an (x+1)th word line;

wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

8. The program method of claim 7, wherein:

the first voltage has a first level if the xth word line is in the first portion;

the first voltage has a second level if the xth word line is in the second portion;

the first voltage has a third level if the xth word line is in the third portion; and

the first level is lower than the second level, and the second level is lower than the third level.

9. The program method of claim 5, wherein:

the first voltage has a first level if the xth word line is in the first portion;

the first voltage has a second level if the xth word line is in the second portion; and

the first level is lower than the second level.

Ex. 1001 ('941 Patent), Claims 5, 8, 9

Petition Chose Dong's V_{PASS} As The “first voltage”

Petition

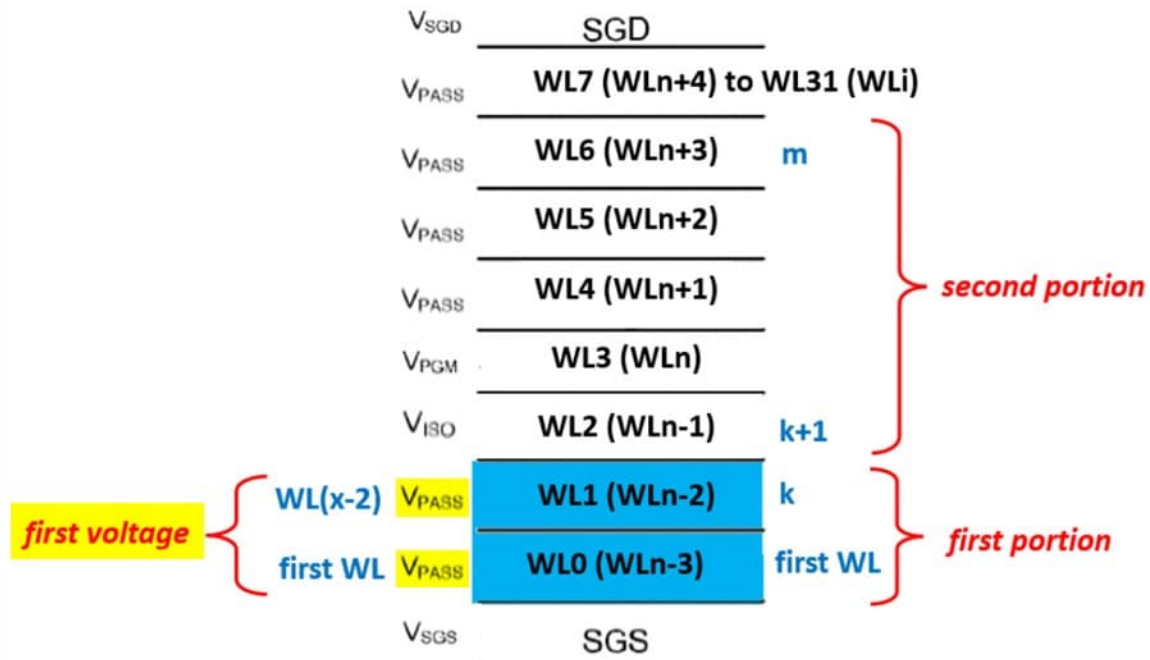
When the x th wordline is used for programming, a *first voltage* is applied to *the first wordline to an $(x-2)$ th wordline*. Dong satisfies this. Liu, ¶ 129. In Dong, because WLn is used for programming, a *first voltage* must be applied to the wordlines from $WL0$ (the *first wordline*) to $WLn-2$ (viz., $WL1$, the $(x-2)$ th wordline). Dong does just this as shown in Fig. 5a below, by applying V_{PASS} to $WL0$ (the *first wordline*) through $WL1$ (viz., $WLn-2$, the $(x-2)$ th wordline). Dong, Fig. 5a; Liu, ¶¶ 129-130.

Pet. 38-39

Petition

Fig. 5a

$k=2$
 $m=7$
 $x=4$



Pet. 39 (annotating Ex. 1005 (Dong), Fig. 5a)



Dong Is Silent Regarding “first voltage” Level Increase Limitations Of Claims 8 And 9

Petition

renders claims 8-9 obvious. Dependent claims 8-9 require that the “first voltage” level increases as programming proceeds up the memory string. Dong is silent on this point, but Costa discloses the same concept and explains that doing so maintains

Pet. 2

string. Costa, Abstract, [0029], [0101]-[0104]. Dong is silent regarding how V_{PASS} (and other programming voltage values) change as the cell being programmed advances from the source end of a memory string to the drain end, thus lending itself

Pet. 72



Petitioner's New Mapping For Claim 9 Fails To Disclose Recited "first voltage" Level Increase Limitations

9. The program method of claim 5, wherein:
 the first voltage has a first level if the xth word line is in the first portion;
 the first voltage has a second level if the xth word line is in the second portion; and
 the first level is lower than the second level.

Ex. 1001 ('941 Patent), Claim 9

Reply

Dong, Fig. 5a (modified and annotated). The red text shows the applied voltages (per Dong Fig. 5a) when $x=4$ (viz., *first portion* wordline programmed) and the blue text shows the applied voltages (per Dong Fig. 5a) when $x=20$ (viz., *second portion* wordline programmed). This satisfies all conditions of claims 5 and 9, as do other examples. Liu_Reply, ¶¶91-94.

Reply 28-29

V1 (Vpass)

=

V1 (Vpass)

Reply

	VSGD		
Second Portion	WL31	(Vpass) (Vpass)	m=32
	WL30	(Vpass) (Vpass)	
	WL29	(Vpass) (Vpass)	
	WL28	(Vpass) (Vpass)	
	WL27	(Vpass) (Vpass)	
	WL26	(Vpass) (Vpass)	
	WL25	(Vpass) (Vpass)	
	WL24	(Vpass) (Vpass)	
	WL23	(Vpass) (Vpass)	
	WL22	(Vpass) (Vpass)	
	WL21	(Vpass) (Vpass)	
	WL20	(Vpass) V3 (Vpass)	X+1
	WL19	(Vpass) VPGM	X=20
	WL18	(Vpass) V2 (Viso)	X-1
	WL17	(Vpass) V1 (Vpass)	X-2
	WL16	(Vpass) V1 (Vpass)	
First Portion	WL15	(Vpass) V1 (Vpass)	k=16
	WL14	(Vpass) V1 (Vpass)	
	WL13	(Vpass) V1 (Vpass)	
	WL12	(Vpass) V1 (Vpass)	
	WL11	(Vpass) V1 (Vpass)	
	WL10	(Vpass) V1 (Vpass)	
	WL9	(Vpass) V1 (Vpass)	
	WL8	(Vpass) V1 (Vpass)	
	WL7	(Vpass) V1 (Vpass)	
	WL6	(Vpass) V1 (Vpass)	
	WL5	(Vpass) V1 (Vpass)	X+2
	WL4	V3 (Vpass) V1 (Vpass)	X+1
	WL3	VPGM V1 (Vpass)	X=4
	WL2	V2 (Viso) V1 (Vpass)	X-1
	WL1	V1 (Vpass) V1 (Vpass)	X-2
	WL0	V1 (Vpass) V1 (Vpass)	
	VSGS		

k=16
m=32
X=4

Reply 28-29



Costa Does Not Disclose “first voltage” Level Increases Under PO’s Construction Of “a program operation”

- Costa describes applying read voltages during a *verify* operation, not during “a program operation”

Costa

(57) ABSTRACT

Sensing in non-volatile memory is performed using bias conditions that are dependent on the position of a selected memory cell within a group of non-volatile memory cells.

During sensing, a selected memory cell receives a reference voltage while the remaining memory cells receive a read or verify pass voltage. For at least a subset of the unselected memory cells, the pass voltage that is applied is dependent upon the position of the selected memory cell in the group. As programming progresses from a memory cell at a first end of a NAND string toward a memory cell at a second end of the NAND string, for example, the pass voltage for at least a subset of the unselected memory cells that have already been subjected to programming may be increased.

[0031] In one embodiment during reading, the pass voltage applied when reading the earlier programmed memory cells is higher relative to the pass voltage applied when reading the later programmed memory cells. The higher pass

[0033] In one embodiment, at least a subset of unselected memory cells that have already been subjected to programming receives the variable pass voltage. A programmed memory cell may refer to a memory cell or word line that has been subjected to programming since a last erase. When

Ex. 1012 (Costa), Abstract, [0031], [0033]

Petition

due to programming of other non-volatile storage elements”). Costa, in contrast, focuses on addressing program disturb impacts arising from the **verification** phase of programming. Costa, [0029]-[0030] (discussing channel resistance impact on

Pet. 71-72

Petitioner’s Expert (Prior Testimony)

to control both operations. Ex. 1031, 101:13-22, 102:18-104:4. Further, Costa teaches adjusting voltages for **verify** operations alone. Ex. 1008, Figs. 5, 7B-7E. It

Ex. 2023 (Liu IPR2024-00792 Reply Decl.) ¶ 72

248. Costa discloses using its read operations to **verify** programming. See §VI.B; Ex. 1008, Fig. 8, [0093]-[0094] (“Sensing may be performed during reading [or] program verification....”). Moreover, the same selected cell is programmed and

Ex. 2022 (Liu IPR2024-00792 Pet. Decl.) ¶ 248

Petition Lacks Any Motivation To Modify Dong's V_{PASS} Voltage

Petition's Motivation To Combine

Dong and Costa focus on two different (but complementary) phenomena that impact memory device reliability during programming. Dong's teachings focus on mitigating the effects of program disturb resulting from the application of the actual programming pulse. Dong, Figs. 4, 19-20, [0042]-[0043] ("Program disturb occurs when the threshold voltage of an unselected non-volatile storage element is shifted due to programming of other non-volatile storage elements"). Costa, in contrast, focuses on addressing program disturb impacts arising from the verification phase of programming. Costa, [0029]-[0030] (discussing channel resistance impact on programming verification).

* * *

A POSITA would have had a reasonable expectation of success in combining Dong and Costa because their respective programming teachings are mutually compatible. Liu, ¶ 213. Combining both teachings would address memory cell errors introduced during both phases of the program operation (viz., the programming pulse and verification pulse). *Id.* Moreover, a POSITA would have

Pet. 71-72, 73

Petition's Application

discusses the three portions in Dong Fig. 5a. Taking each claimed portion in Dong as one of Costa's "zones," the claimed $V1$ voltage (viz., Dong's V_{PASS} voltage) applied to the previously programmed cells in a memory string will increase as the cell being programmed moves from the first portion (first zone) to the second portion (second zone), and from the second portion (second zone) to the third portion (third zone). *Id.* This satisfies the claimed condition that the first [voltage]

Pet. 76



Reply's Improper New Mapping For Claim 8 Also Fails To Disclose Recited "first voltage" Level Increase Limitations

8. The program method of claim 7, wherein:
 the first voltage has a first level if the xth word line is in the first portion;
 the first voltage has a second level if the xth word line is in the second portion;
 the first voltage has a third level if the xth word line is in the third portion; and
 the first level is lower than the second level, and the second level is lower than the third level.

Ex. 1001 ('941 Patent), Claim 8

Reply

(viz. $x=4$ (*first portion*), $x=20$ (*second portion*), and $x=29$ (*third portion*)). This satisfies all conditions of claim 8 (and base claims 5 and 7), as do other examples. Liu_Reply, ¶¶95-96.

Reply 29-30

V1 (Vpass)

=

V1 (Vpass)

=

V1 (Vpass)

Reply

		VSGD		
Third Portion	WL31	(Vpass)	(Vpass)	V4 (Vpass) $n=32$
	WL30	(Vpass)	(Vpass)	V4 (Vpass) $X+2$
	WL29	(Vpass)	(Vpass)	V3 (Vpass) $X+1$
	WL28	(Vpass)	(Vpass)	VPGM $X=29$
	WL27	(Vpass)	(Vpass)	V2 (Viso) $X-1$
	WL26	(Vpass)	(Vpass)	V1 (Vpass) $X-2$
	WL25	(Vpass)	(Vpass)	V1 (Vpass)
	WL24	(Vpass)	(Vpass)	V1 (Vpass)
Second Portion	WL23	(Vpass)	(Vpass)	V1 (Vpass) $m=24$
	WL22	(Vpass)	(Vpass)	V1 (Vpass)
	WL21	(Vpass)	(Vpass)	V1 (Vpass) $X+2$
	WL20	(Vpass)	V3 (Vpass)	V1 (Vpass) $X+1$
	WL19	(Vpass)	VPGM	V1 (Vpass) $X=20$
	WL18	(Vpass)	V2 (Viso)	V1 (Vpass) $X-1$
	WL17	(Vpass)	V1 (Vpass)	V1 (Vpass) $X-2$
	WL16	(Vpass)	V1 (Vpass)	V1 (Vpass)
First Portion	WL15	(Vpass)	V1 (Vpass)	V1 (Vpass) $k=16$
	WL14	(Vpass)	V1 (Vpass)	V1 (Vpass)
	WL13	(Vpass)	V1 (Vpass)	V1 (Vpass)
	WL12	(Vpass)	V1 (Vpass)	V1 (Vpass)
	WL11	(Vpass)	V1 (Vpass)	V1 (Vpass)
	WL10	(Vpass)	V1 (Vpass)	V1 (Vpass)
	WL9	(Vpass)	V1 (Vpass)	V1 (Vpass)
	WL8	(Vpass)	V1 (Vpass)	V1 (Vpass)
	WL7	(Vpass)	V1 (Vpass)	V1 (Vpass)
	WL6	(Vpass)	V1 (Vpass)	V1 (Vpass)
	WL5	(Vpass)	V1 (Vpass)	V1 (Vpass) $X+2$
	WL4	V3 (Vpass)	V1 (Vpass)	V1 (Vpass) $X+1$
	WL3	VPGM	V1 (Vpass)	V1 (Vpass) $X=4$
	WL2	V2 (Viso)	V1 (Vpass)	V1 (Vpass) $X-1$
	WL1	V1 (Vpass)	V1 (Vpass)	V1 (Vpass) $X-2$
	WL0	V1 (Vpass)	V1 (Vpass)	V1 (Vpass)
		VSGS		

$k=16$
 $m=24$
 $X=4$
 $n=32$

Reply 30



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

I. Petition's Original Mappings Fail

II. "A Program Operation" Does Not Include A Verify Phase

III. Reply's Improper New Mappings Fail Under PO's Construction

IV. Reply's Improper New Mappings Fail Under Petitioner's Construction

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14



Claims 8 And 9 Recite “first voltage” Level Increase Limitations During “a program operation”

5. A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first word line to a kth word line from bottom to top, the second portion formed above the first portion and comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:

applying a first voltage to the first word line to an (x-2)th word line when an xth word line is used to perform a program operation;

applying a second voltage to an (x-1)th word line; and

applying a third voltage to an (x+1)th word line;

wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

8. The program method of claim 7, wherein:

the first voltage has a first level if the xth word line is in the first portion;

the first voltage has a second level if the xth word line is in the second portion;

the first voltage has a third level if the xth word line is in the third portion; and

the first level is lower than the second level, and the second level is lower than the third level.

9. The program method of claim 5, wherein:

the first voltage has a first level if the xth word line is in the first portion;

the first voltage has a second level if the xth word line is in the second portion; and

the first level is lower than the second level.

Ex. 1001 ('941 Patent), Claims 5, 8, 9

Dong + Costa Fail To Disclose “first voltage” Limitations Under Petitioner’s Incorrect Construction

- Petitioner’s construction does nothing to remedy Petitioner’s reliance on Dong’s V_{PASS} as the “first voltage” for claim 5.

Petition

When the *x*th wordline is used for programming, a *first voltage* is applied to *the first wordline to an (x-2)th wordline*. Dong satisfies this. Liu, ¶ 129. In Dong, because WLn is used for programming, a *first voltage* must be applied to the wordlines from $WL0$ (the *first wordline*) to $WLn-2$ (viz., $WL1$, the *(x-2)th wordline*). Dong does just this as shown in Fig. 5a below, by applying V_{PASS} to $WL0$ (the *first wordline*) through $WL1$ (viz., $WLn-2$, the *(x-2)th wordline*). Dong, Fig. 5a; Liu, ¶¶ 129-130.

Pet. 38-39

Petition

discusses the three *portions* in Dong Fig. 5a. Taking each claimed *portion* in Dong as one of Costa’s “zones,” the claimed *V1* voltage (viz., Dong’s V_{PASS} voltage) applied to the previously programmed cells in a memory string will increase as the cell being programmed moves from the *first portion* (first zone) to the *second portion* (second zone), and from the *second portion* (second zone) to the *third portion* (third zone). *Id.* This satisfies the claimed condition that *the first [voltage]*

Pet. 76

Petitioner's New Position That Costa Discloses "first voltage" Level Increase Limitations Also Fails

- Petitioner's construction does nothing to remedy Petitioner's reliance on Dong's V_{PASS} as the "first voltage" for claim 5.

Petition

When the *xth* wordline is used for programming, a *first voltage* is applied to *the first wordline to an (x-2)th wordline*. Dong satisfies this. Liu, ¶ 129. In Dong, because WLn is used for programming, a *first voltage* must be applied to the wordlines from $WL0$ (the *first wordline*) to $WLn-2$ (viz., $WL1$, the *(x-2)th wordline*). Dong does just this as shown in Fig. 5a below, by applying V_{PASS} to $WL0$ (the *first wordline*) through $WL1$ (viz., $WLn-2$, the *(x-2)th wordline*). Dong, Fig. 5a; Liu, ¶¶ 129-130.

Pet. 38-39

Reply

Costa undisputedly discloses that the pass voltage applied to unselected cells "depend[s] upon the position of the selected memory cell," and increases "[a]s programming progresses." Costa, Abstract. Under PO's construction, this satisfies the *first voltage* requirement (viz., that *the first [voltage] level is lower than the second [voltage] level, and the second [voltage] level is lower than the third [voltage] level*. '941, cl.8.

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Petitioner's New Position That Costa Discloses “first voltage” Limitations Also Fails

Reply

PO erroneously contends that Petitioner “applie[d] Dong’s V_{PASS} —used in a program phase—as the ‘first voltage.’” POR, 64. Even if true, this is irrelevant. V_{pass} is applied both during charge injection (Dong, Fig. 5a) and verification (Costa, Abstract). Even if Dong’s V_{pass} voltage (during charge injection) differed from Costa’s (during verification), nothing in the claim prohibits that (or requires they be the same). What matters is that at any given point during a *program operation*, the specified wordlines (*i.e.*, *the first wordline to an (x-2)th wordline*) have a common *first voltage* applied to them (not that the voltage never change).

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'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14

- I. A POSITA Would Not Have Applied $V_{\text{PASS-LOW}}$ To Shirai's Entire Lower Memory Deck**
- II. Petitioner's New "Second Portion" Mappings Fail**
- III. Petitioner Fails To Provide Claim-Specific Analysis For Claim 10**



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14

I. A POSITA Would Not Have Applied $V_{\text{PASS-LOW}}$ To Shirai's Entire Lower Memory Deck

II. Petitioner's New "Second Portion" Mappings Fail

III. Petitioner Fails To Provide Claim-Specific Analysis For Claim 10

Claims 4, 10, And 14

4. The memory of claim 1, further comprising:
an upper dummy word line formed below the first portion;
a lower dummy word line formed above the second portion; and
a joint oxide layer formed between the upper dummy word line and the lower dummy word line;
wherein the memory has a two-deck structure.

10. The program method of claim 5, wherein the memory further comprises:
a lower dummy word line formed above the first portion;
an upper dummy word line formed below the second portion;
a joint oxide layer formed between the lower dummy word line and the upper dummy word line;
wherein the memory has a two-deck structure.

14. The program method of claim 11, wherein the memory further comprises:
an upper dummy word line formed below the first portion;
a lower dummy word line formed above the second portion; and
a joint oxide layer formed between the upper dummy word line and the lower dummy word line;
wherein the memory has a two-deck structure.

Petitioner Applies “V_{PASS-LOW}” To Shirai’s Entire Lower Deck

Petition (Annotating Dong)

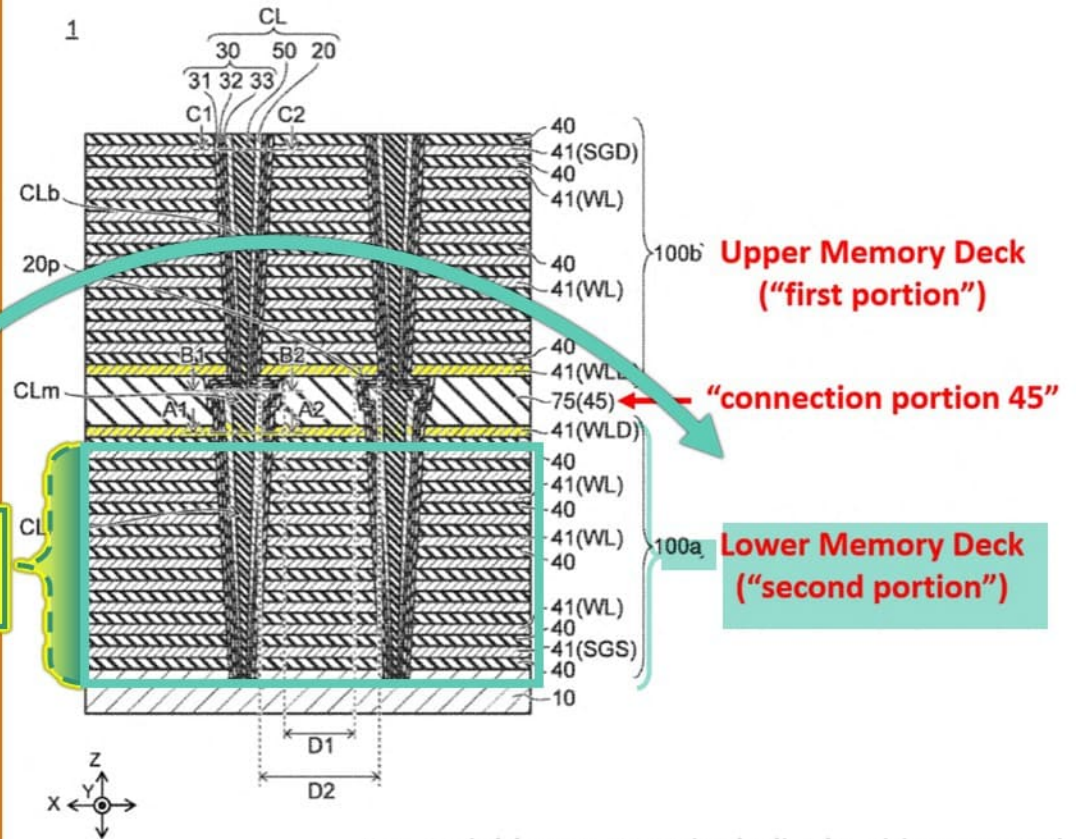
Fig. 5g

[illegible]

Pet. 54 (citing Ex. 1005 (Dong), Fig. 5g) (annotated)

Petition (Annotating Shirai)

FIG. 2



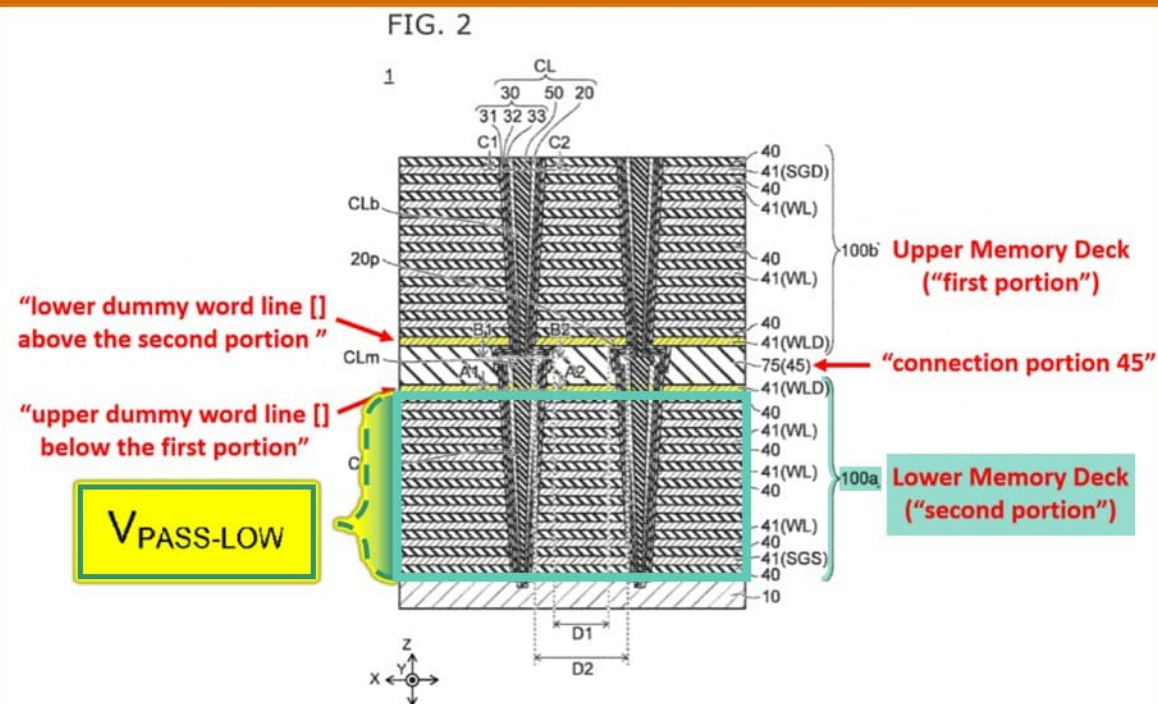
Pet. 83 (citing Ex. 1018 (Shirai), Fig. 2) (annotated)

Petitioner Applies “ $V_{PASS-LOW}$ ” To Shirai’s Entire Lower Deck

Petition

Claim 4 further requires that the *upper dummy wordline [is] formed below the first portion* and the *lower dummy wordline [is] formed above the second portion*. Shirai discloses this. *Id.* The dummy wordline locations relative to stack portions 100a and 100b (*viz.*, the *[memory] decks*) can be seen in Shirai Fig. 2 below. Recall that in base claim 1, the *second portion [is] formed below the first portion*. See element [1.B]. Dong’s first portion corresponds to Shirai’s upper deck 100b, and Dong’s second portion corresponds to Shirai’s bottom deck 100a. Liu, ¶ 232. Thus, Shirai’s dummy wordline 41 in 100a is an *upper dummy wordline[s] formed below the first portion* [*e.g.*, below upper deck 100b]. *Id.* And dummy wordline 41 in 100b is a *lower dummy wordline formed above the second portion* [*e.g.*, above lower deck 100a]. *Id.*

Petition (Annotating Shirai)



Pet. 82-83 (citing Ex. 1018 (Shirai), Fig. 2) (annotated)

Petition's Application Of " $V_{PASS-LOW}$ " To Shirai's Lower Deck Increases Program Disturb

Dong

[0044] For example, if NAND string 320 is inhibited (e.g., it is an unselected NAND string which does not contain a storage element which is currently being programmed) and NAND string 340 is being programmed (e.g., it is a selected NAND string which contains a storage element which is currently being programmed), program disturb can occur at NAND string 320. For example, if a pass voltage, V_{PASS} , is low, the channel of the inhibited NAND string is not well boosted, and a selected word line of the unselected NAND string can be unintentionally programmed. In another possible scenario, the boosted voltage can be lowered by Gate Induced Drain Leakage (GIDL) or other leakage mechanisms, resulting in the same problem. Other effects, such as shifts in the V_{TH} of a charge storage element due to capacitive coupling with other neighboring storage elements that are programmed later, can also contribute to program disturb.

Ex. 1005 (Dong), [0044]

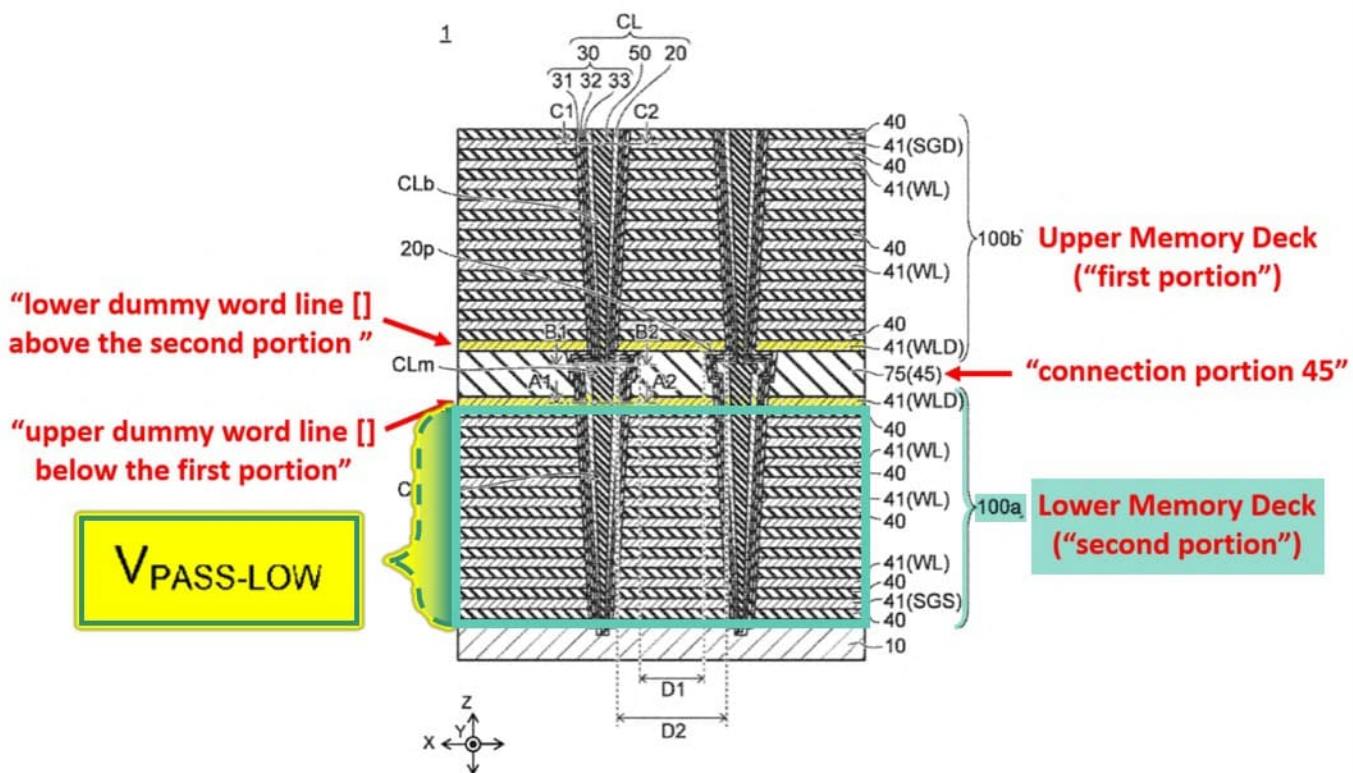
Lutze

EASB is similar to LSB with the exception that only the source side neighbor word line is at zero volts. For example, WL1 would be at zero volts while WL3 would be at V_{pass} . In one embodiment, V_{pass} is 7–10 volts. If V_{pass} is too low, boosting in the channel is insufficient to prevent program disturb. If V_{pass} is too high, unselected word lines will be programmed.

Ex. 1015 (Lutze), 4:16-22

Petition (Annotating Shirai)

FIG. 2



Pet. 82-83 (citing Ex. 1018 (Shirai), Fig. 2) (annotated)

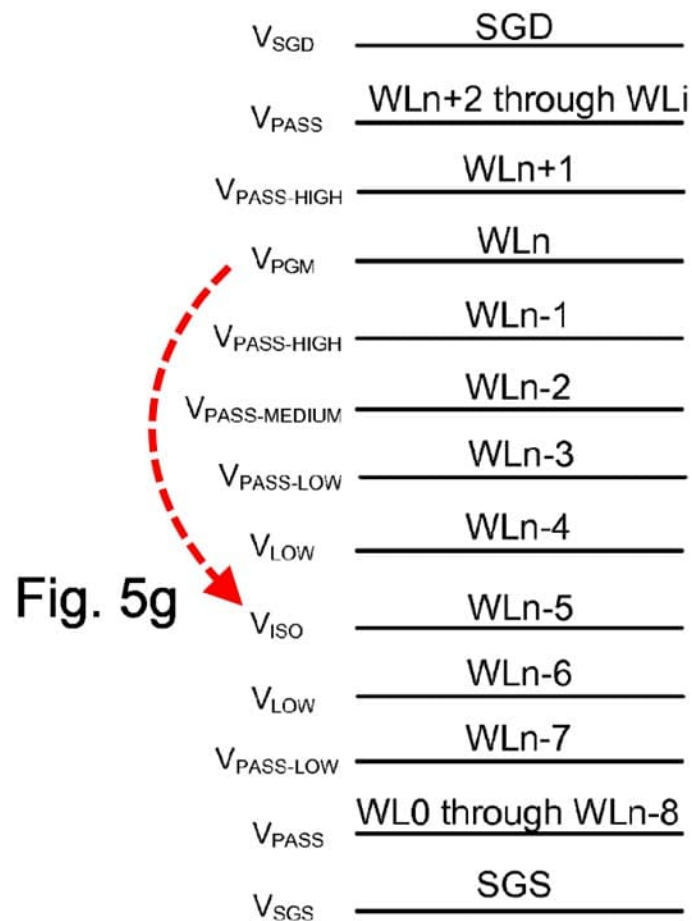
Petition's Application Of " $V_{PASS-LOW}$ " To Shirai's Lower Deck Increases Program Disturb

Dong

[0057] Thus, multiple V_{PASS} voltages can be used at the same time. For example, different V_{PASS} values can be used for the drain and source sides of the NAND string. Further, multiple V_{PASS} voltages can be used at both the drain and source sides. For instance, a higher V_{PASS} , $V_{PASS-HIGH}$, can be used next to the selected word line for programming, as depicted. For the word lines in between the selected word line and the isolation word line, we can have multiple word lines that are biased to different V_{PASS} values, e.g., $V_{PASS-LOW}$, $V_{PASS-MEDIUM}$ and $V_{PASS-HIGH}$. In one implementation, $V_{PGM} > V_{PASS-HIGH} > V_{PASS-MEDIUM} > V_{PASS-LOW} > V_{LOW} > V_{ISO}$. Note that multiple values of V_{LOW} and V_{ISO} are also possible. Generally, all V_{ISO} voltages are less than all V_{LOW} voltages, which in turn are less than all V_{PASS} voltages. By increasing the number of word lines in between the selected word line and the V_{ISO} word line, and by gradually reducing the bias voltage on those word lines, the electric field in between the selected word line and the V_{ISO} word line can be reduced and thus program disturb can be reduced.

Ex. 1005 (Dong), [0057]

Dong



Ex. 1005 (Dong), Fig. 5g (annotated)



Petitioner's Omission Of V_{ISO} Increases Program Disturb

Dong

(57)

ABSTRACT

Non-volatile storage in which program disturb is reduced by preventing source side boosting in selected NAND strings. A self-boosting mode which includes an isolation word line is used. A channel area of an inhibited NAND string is boosted on a source side of the isolation word line before the channel is boosted on a drain side of the isolation word line. Further, storage elements near the isolation word line are kept in a conducting state during the source side boosting so that the source side channel is connected to the drain side channel. In this way, in selected NAND strings, source side boosting can not occur and thus program disturb due to source side boosting can be prevented. After the source side boosting, the source side channel is isolated from the drain side channel, and drain side boosting is performed.

[0065] With the EASB or REASB boosting modes, V_{ISO} is applied to one or more source-side neighbors of the selected word line at some point after boosting is initiated, and is sufficiently low to isolate programmed and erased channel areas in the substrate. That is, a channel area of the substrate

Ex. 1005 (Dong), Abstract, [0065]

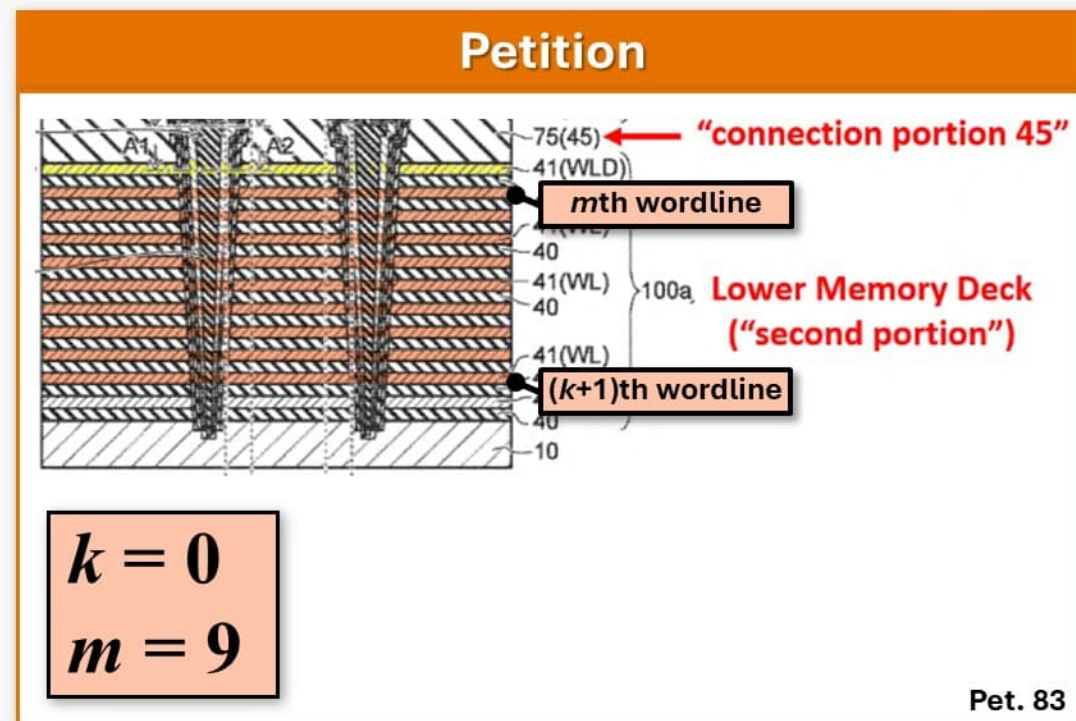
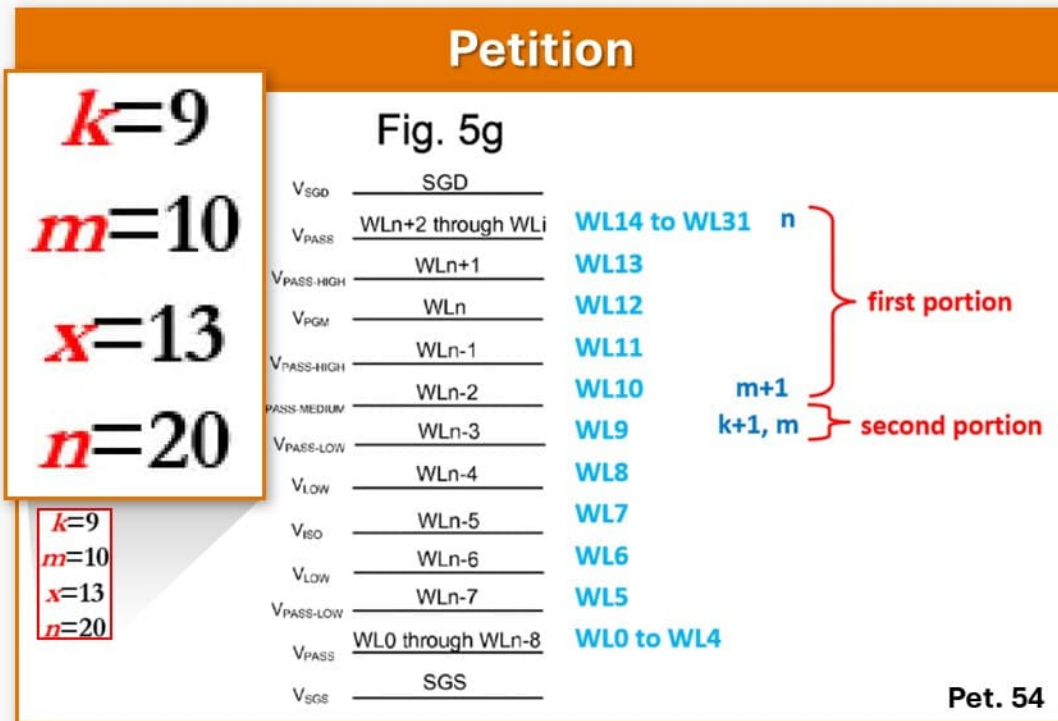
PO's Expert

Dong, ¶57. The elimination of V_{LOW} and V_{ISO} from Petitioner's combination of Dong and Shirai will result in a more abrupt change in channel voltage, and therefore an increased propensity toward program disturb due to HCI. Moreover, as a POSITA would have understood, Dong discloses that the isolation wordline is the mechanism that enables prevention of program disturb. Dong, Abstract; *see id.*, ¶¶67-68. That is why, in my opinion, Dong discloses relying on an isolation wordline in every self-boosting mode to "isolate programmed and erased channel areas in the substrate." *Id.*, ¶65; *see id.*, ¶¶66-67, Figs. 5a-5g, Title, Abstract. This isolation wordline increases the resistance of the channel on the drain side of the isolation wordline, thereby increasing channel boost on the drain side, and reducing program disturb.

258. Without an isolation wordline, this key mechanism of Dong is removed, resulting in degraded program disturb characteristics. A POSITA would thus not have been motivated to omit Dong's isolation wordline (i.e., the one receiving V_{ISO}) whose sole purpose is to reduce program disturb.

Ex. 2028 (Patent Owner's Expert Dr. Khatri Decl.) ¶¶ 256, 258

Petition's Mappings For Claims 4 And 14 Use Different Variables Than Base Claims



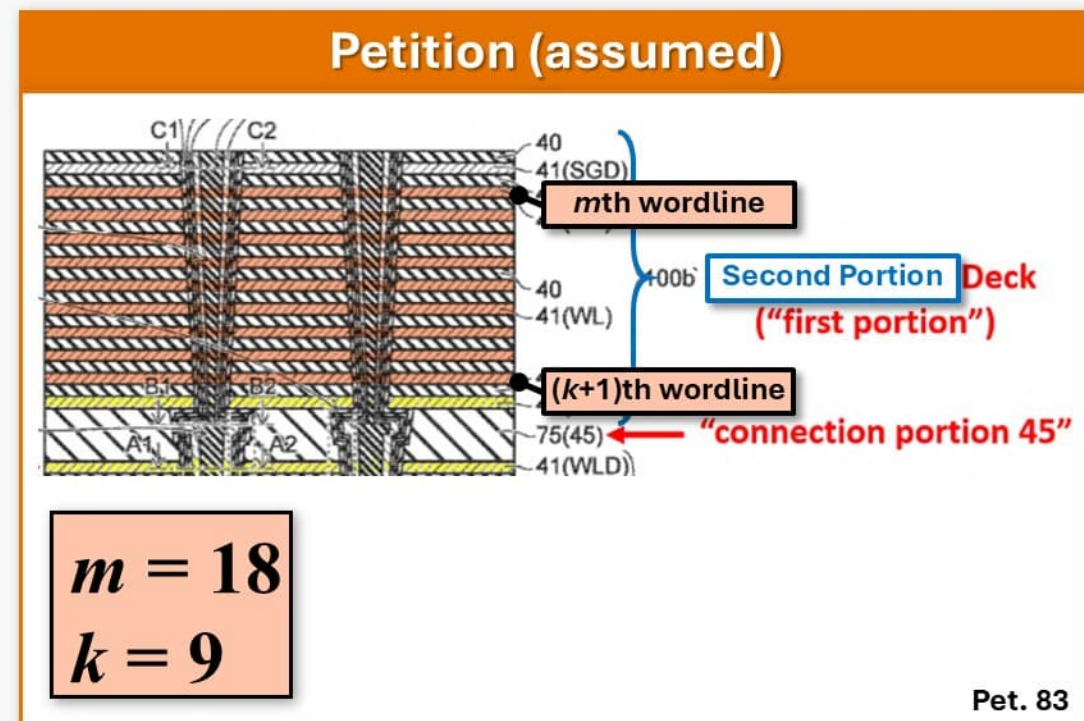
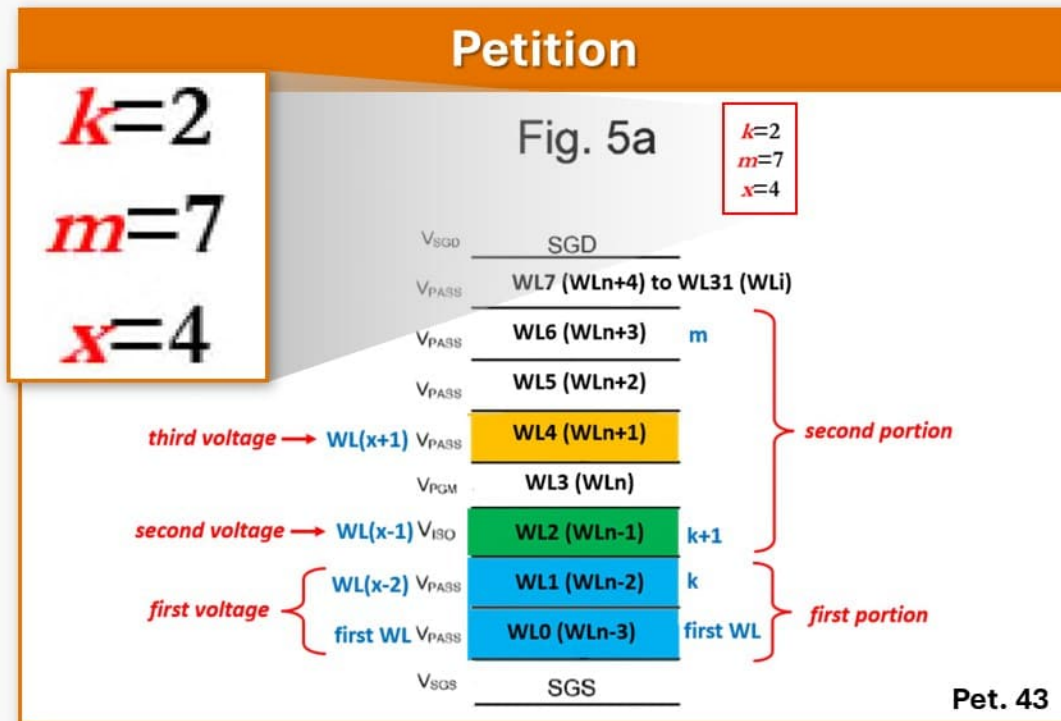
1. A memory comprising:

* * *

a second portion formed below the first portion and comprising a (k+1)th word line to an mth word line from bottom to top;

Ex. 1001 ('941 Patent), Claim 1

Petition's Mapping For Claim 10 Uses Different Variables Than Base Claims



5. A program method of a memory, the memory comprising:

to top, the second portion formed above the first portion and comprising a (k+1)th word line to an mth word line from bottom to top, the program method comprising:

wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

Ex. 1001 ('941 Patent), Claim 5



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14

I. A POSITA Would Not Have Applied $V_{\text{PASS-LOW}}$ To Shirai's Entire Lower Memory Deck

II. Petitioner's New "Second Portion" Mappings Fail

III. Petitioner Fails To Provide Claim-Specific Analysis For Claim 10



Reply's Improper New Mappings For Claims 4 And 14

Petition

Fig. 5g

V _{SGD}	SGD		
V _{PASS}	WLn+2 through WLi	WL14 to WL31	n
V _{PASS-HIGH}	WLn+1	WL13	
V _{PGM}	WLn	WL12	
V _{PASS-HIGH}	WLn-1	WL11	
V _{PASS-MEDIUM}	WLn-2	WL10	
V _{PASS-LOW}	WLn-3	WL9	
V _{LOW}	WLn-4	WL8	
V _{ISO}	WLn-5	WL7	
V _{LOW}	WLn-6	WL6	
V _{PASS-LOW}	WLn-7	WL5	
V _{PASS}	WL0 through WLn-8	WL0 to WL4	
V _{SGS}	SGS		

$k=9$
 $m=10$
 $x=13$
 $n=20$

first portion
 second portion
 $m+1$
 $k+1, m$

Pet. 54

Reply

	VSGD		
WL31	(Vpass)	WL31	(Vpass)
WL30	(Vpass)	WL30	(Vpass)
WL29	(Vpass)	WL29	(Vpass)
WL28	(Vpass)	WL28	(Vpass)
WL27	(Vpass)	WL27	(Vpass)
WL26	(Vpass)	WL26	(Vpass)
WL25	(Vpass)	WL25	(Vpass)
WL24	(Vpass)	WL24	(Vpass)
WL23	(Vpass)	WL23	(Vpass)
WL22	(Vpass)	WL22	(Vpass)
WL21	(Vpass)	WL21	(Vpass)
WL20	(Vpass)	WL20	(Vpass)
WL19	V1 (Vpass)	WL19	V1 (Vpass)
WL18	V1 (Vpass)	WL18	V1 (Vpass)
WL17	V1 (Vpass)	WL17	V1 (Vpass)
WL16	V1 (Vpass)	WL16	V1 (Vpass)
WL15	V1 (Vpass)	WL15	V1 (Vpass)
WL14	V1 (Vpass)	WL14	V1 (Vpass)
WL13	V2 (Vpass-high)	WL13	V2 (Vpass-high)
WL12	VPGM	WL12	VPGM
WL11	V3 (Vpass-high)	WL11	V3 (Vpass-high)
WL10	V4 (Vpass-medium)	WL10	V4 (Vpass-medium)
	Dummy Wordline		Dummy Wordline
	Connection Portion 45		Connection Portion 45
	Dummy Wordline		Dummy Wordline
WL9	V5 (Vpass-low)	WL9	V5 (Vpass-low)
WL8	V5 (Vpass-low)	WL8	(Vlow)
WL7	(Vlow)	WL7	(Viso)
WL6	(Viso)	WL6	(Vlow)
WL5	(Vlow)	WL5	(Vpass-low)
WL4	(Vpass-low)	WL4	(Vpass)
WL3	(Vpass)	WL3	(Vpass)
WL2	(Vpass)	WL2	(Vpass)
WL1	(Vpass)	WL1	(Vpass)
WL0	(Vpass)	WL0	(Vpass)
	VSGS		VSGS

First Portion
 Second Portion
 $n=20$
 $m=10$
 $k+1=9$
 $k=8$
 $x=13$
 $x+2$
 $x+1$
 $x-1$
 $x-2$
 $m+2=12$
 $k=9$

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Petitioner's New Claims 4 And 14 Mappings Conflict With Its Original Base-Claim Mapping

Petition				
Fig. 5g				
V_{SGD}	SGD			
V_{PASS}	WLn+2 through WLi	WL14 to WL31	n	first portion
$V_{PASS-HIGH}$	WLn+1	WL13		
V_{PGM}	WLn	WL12		
$V_{PASS-HIGH}$	WLn-1	WL11		
$V_{PASS-MEDIUM}$	WLn-2	WL10	m+1	
$V_{PASS-LOW}$	WLn-3	WL9	k+1, m	second portion
V_{LOW}	WLn-4	WL8		
V_{ISO}	WLn-5	WL7		
V_{LOW}	WLn-6	WL6		
$V_{PASS-LOW}$	WLn-7	WL5		
V_{PASS}	WL0 through WLn-8	WL0 to WL4		
V_{SGS}	SGS			

$k=9$
 $m=10$
 $x=13$
 $n=20$

Pet. 54

Reply				
	VSGD			
WL31	(Vpass)			
WL30	(Vpass)			
WL29	(Vpass)			
WL28	(Vpass)			
WL27	(Vpass)			
WL26	(Vpass)			
WL25	(Vpass)			
WL24	(Vpass)			
WL23	(Vpass)			
WL22	(Vpass)			
WL21	(Vpass)			
WL20	(Vpass)			
WL19	V1 (Vpass)		n=20	
WL18	V1 (Vpass)			
WL17	V1 (Vpass)			
WL16	V1 (Vpass)			
WL15	V1 (Vpass)			
WL14	V1 (Vpass)	X+2		
WL13	V2 (Vpass-high)	X+1		
WL12	VPGM	x=13		
WL11	V3 (Vpass-high)	X-1		
WL10	V4 (Vpass-medium)	X-2		
	Dummy Wordline			
	Connection Portion 45			
	Dummy Wordline			
WL9	V5 (Vpass-low)	m=10		
WL8	V5 (Vpass-low)	k+1=9		
WL7	(Vlow)	k=8		
WL6	(Viso)			
WL5	(Vlow)			
WL4	(Vpass-low)			
WL3	(Vpass)			
WL2	(Vpass)			
WL1	(Vpass)			
WL0	(Vpass)			
	VSGS			

First Portion

Second Portion

Reply 36



Petitioner's New Claims 4 And 14 Mappings Conflict With Its Original Base-Claim Mapping

Petition

Fig. 5g

V_{SGD}	SGD	
V_{PASS}	WLn+2 through WLi	WL14 to WL31 n
$V_{PASS-HIGH}$	WLn+1	WL13
V_{PGM}	WLn	WL12
$V_{PASS-HIGH}$	WLn-1	WL11
$V_{PASS-MEDIUM}$	WLn-2	WL10
$V_{PASS-LOW}$	WLn-3	WL9
V_{LOW}	WLn-4	WL8
V_{ISO}	WLn-5	WL7
V_{LOW}	WLn-6	WL6
$V_{PASS-LOW}$	WLn-7	WL5
V_{PASS}	WL0 through WLn-8	WL0 to WL4
V_{SGS}	SGS	

Pet. 54

Annotations:

- $k=9$
- $m=10$
- $x=13$
- $n=20$
- first portion (WL14 to WL31)
- second portion (WL0 to WL4)
- $m+1$
- $k+1, m$

Reply

	V_{SGD}	
WL31	(Vpass)	
WL30	(Vpass)	
WL29	(Vpass)	
WL28	(Vpass)	
WL27	(Vpass)	
WL26	(Vpass)	
WL25	(Vpass)	
WL24	(Vpass)	
WL23	(Vpass)	
WL22	(Vpass)	
WL21	(Vpass)	
WL20	(Vpass)	
WL19	V1 (Vpass)	$n=20$
WL18	V1 (Vpass)	
WL17	V1 (Vpass)	
WL16	V1 (Vpass)	
WL15	V1 (Vpass)	
WL14	V1 (Vpass)	X+2
WL13	V2 (Vpass-high)	X+1
WL12	VPGM	X=13
WL11	V3 (Vpass-high)	X-1
WL10	V4 (Vpass-medium)	X-2
	Dummy Wordline	
	Connection Portion 45	
	Dummy Wordline	
WL9	V5 (Vpass-low)	$m=10$
WL8	V5 (Vpass-low)	$k+1=9$
WL7	(Vlow)	$k=8$
WL6	(Viso)	
WL5	(Vlow)	
WL4	(Vpass-low)	
WL3	(Vpass)	
WL2	(Vpass)	
WL1	(Vpass)	
WL0	(Vpass)	
	VSGS	

Reply 36

Annotations:

- $m=10$
- $k+1=9$
- $k=8$
- First Portion (WL14 to WL19)
- Second Portion (WL10 to WL13)
- WL10 to WL13 (X+2, X+1, X=13, X-1, X-2)
- WL9 to WL13 (V5 (Vpass-low), V5 (Vpass-low), (Vlow), (Viso), (Vlow))
- WL4 to WL8 (Vpass-low, (Vpass), (Vpass), (Vpass), (Vpass))



'941 Patent

Ground 1 (Dong anticipation) Fails

Claims 1, 3, 5-7, 11, 13

Ground 2 (Dong obviousness) Fails

Claims 1, 3, 5-7, 11, 13

Ground 3 (Dong + Costa) Fails

Claims 8-9

Ground 4 (Dong + Shirai) Fails

Claims 4, 10, 14

I. A POSITA Would Not Have Applied $V_{\text{PASS-LOW}}$ To Shirai's Entire Lower Memory Deck

II. Petitioner's New "Second Portion" Mappings Fail

III. Petitioner Fails To Provide Claim-Specific Analysis For Claim 10

Dong And Shirai Do Not Render Obvious Claims 4, 10, And 14

Petition

Claim 10 is substantively the same as claim 4 and is met for the same reasons.

Pet. 83

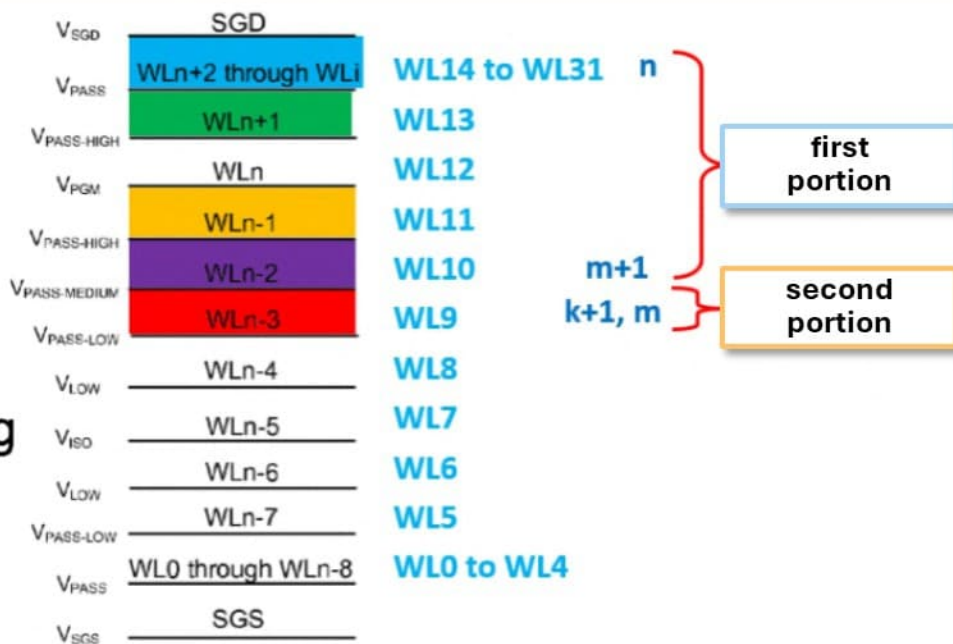
4. The memory of claim 1, further comprising:
an upper dummy word line formed below the first portion;
a lower dummy word line formed above the second portion; and
a joint oxide layer formed between the upper dummy word line and the lower dummy word line;
wherein the memory has a two-deck structure.

10. The program method of claim 5, wherein the memory further comprises:
a lower dummy word line formed above the first portion;
an upper dummy word line formed below the second portion;
a joint oxide layer formed between the lower dummy word line and the upper dummy word line;
wherein the memory has a two-deck structure.

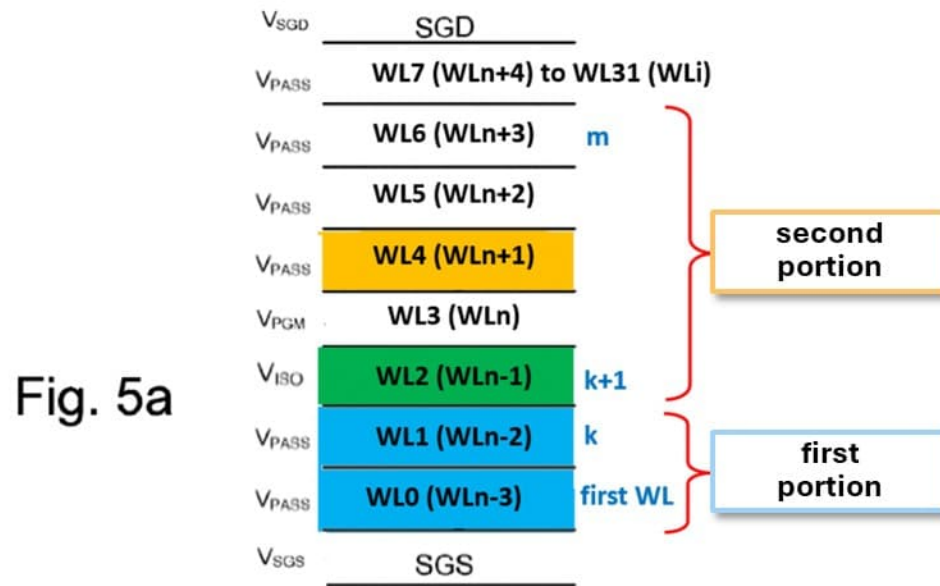
Ex. 1001 ('941 Patent), Claims 4, 10

Petitioner Fails To Provide Claim-Specific Analysis For Claim 10

Petition's Position For Claim 1



Petition's Position For Claim 5



Pet. 33, 51, 83

4. The memory of claim 1, further comprising:
 an upper dummy word line formed below the first portion;
 a lower dummy word line formed above the second portion; and

10. The program method of claim 5, wherein the memory further comprises:
 a lower dummy word line formed above the first portion;
 an upper dummy word line formed below the second portion;

Ex. 1001 ('941 Patent), Claims 4, 10