

Micron Technology, Inc.
Petitioner
v.
Yangtze Memory Technologies Company, Ltd.
Patent Owner

Case No. IPR2025-00190
U.S. Patent No. 11,568,941

Petitioner's Hearing Demonstratives

April 28, 2026

Roadmap

- I. [Introduction and IPR Grounds](#)
- II. [Overview of the '941 Patent and Prior Art](#)
- III. [Ground 1 \(Anticipation by Dong\) \(claims 1, 3, 5-7, 11, 13\)](#)
 - [Under Petitioner's Bottom-to-Top Construction](#)
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- IV. [Ground 2 \(Obviousness over Dong\) \(claims 1, 3, 5-7, 11, 13\)](#)
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- V. [Ground 3 \(Obviousness over Dong+Costa\) \(claims 8-9\)](#)
 - [Program Operation Construction](#)
- VI. [Ground 4 \(Obviousness over Dong+Shirai\) \(claims 4, 10, 14\)](#)

Roadmap

I. Introduction and IPR Grounds

II. Overview of the '941 Patent and Prior Art

III. Ground 1 (Anticipation by Dong) (claims 1, 3, 5-7, 11, 13)

- Under Petitioner's Bottom-to-Top Construction
- Under Patent Owner's Bottom-to-Top Construction

IV. Ground 2 (Obviousness over Dong) (claims 1, 3, 5-7, 11, 13)

- Under Patent Owner's Bottom-to-Top Construction

V. Ground 3 (Obviousness over Dong+Costa) (claims 8-9)

- Program Operation Construction

VI. Ground 4 (Obviousness over Dong+Shirai) (claims 4, 10, 14)

Instituted Grounds

Ground	Prior Art	Claims
1	Dong (anticipation)	1, 3, 5-7, 11, and 13
2	Dong (single reference obviousness)	1, 3, 5-7, 11, and 13
3	Saint + Costa (obviousness)	8 and 9
4	Dong + Shirai (obviousness)	4, 10, and 14

Petition, 7

Instituted Grounds – Two Embodiments of Dong

X. GROUNDS 1 AND 2 (DONG)

Dong anticipates (Ground 1) and renders obvious (Ground 2) claims 1, 3, 5-7, 11, and 13. These claims can be broken into two groups as follows:

Group One: independent claim 5 and its dependent claims 6-7.

Group Two: independent claims 1 and 11, and their respective dependent claim 3 and 13.

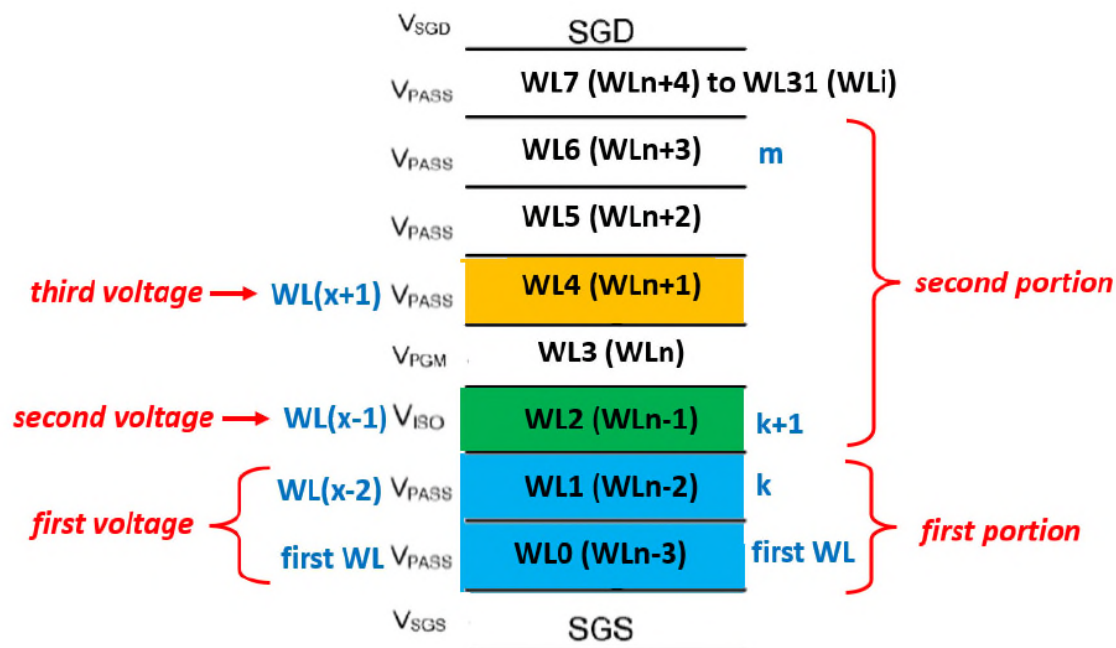
Different embodiments in Dong map to each group. In particular, Dong Fig.

5a maps to *Group One*. And Dong Fig. 5g maps to *Group Two*. The analysis below

Petition, 28

Group 1: Dong Fig. 5a (Claims 5-10)

Fig. 5a



Dong, Fig. 5a (annotated and mapped to claim 1)
Petition, 33

Group 2: Dong Fig. 5g (Claims 1, 3-4, 11, 13-14)



*Dong, Fig. 5g (annotated and mapped to claim 5)
Petition, 51*

Level of Skill in the Art

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '941 patent would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) NAND memory devices (including issues relating to the operation, *e.g.*, programming, of said devices), or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). Liu, ¶¶ 40-42.

This POSITA would have been aware of and generally knowledgeable about NAND memory's structure and fabrication, its component parts, how it operates, and how it is controlled. *Id.*, ¶ 41.

Petition, 22-23

Level of Skill in the Art is Undisputed

D. Person of Ordinary Skill in the Art

YMTC does not dispute Petitioner's definition of a POSITA for purposes of these proceedings. Pet. 22-23; Khatri2, ¶¶42-47.

POR, 10

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V. Ground 3 (Obviousness over Dong+Costa) (claims 8-9)

- Program Operation Construction

VI. Ground 4 (Obviousness over Dong+Shirai) (claims 4, 10, 14)

Overview of the '941 Patent

- **U.S. Pat. 11,568,941**
- **Titled “Memory Including a Plurality of Portions and Used for Reducing Program Disturbance and Program Method Thereof”**
- **Priority Date: February 10, 2020**

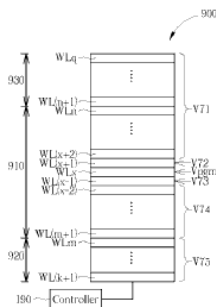
(12) United States Patent		(10) Patent No.: US 11,568,941 B2
Song et al.		(45) Date of Patent: Jan. 31, 2023
<p>(54) MEMORY INCLUDING A PLURALITY OF PORTIONS AND USED FOR REDUCING PROGRAM DISTURBANCE AND PROGRAM METHOD THEREOF</p> <p>(58) Field of Classification Search CPC — G11C 16/3418; G11C 16/08; G11C 16/10 See application file for complete search history.</p> <p>(56) References Cited</p> <p>U.S. PATENT DOCUMENTS</p> <p>6,961,270 A 5/2000 Choi 10,569,570 B2 * 4/2019 Lee G11C 16/3459 2009/0257280 A1 10/2009 Oh 2010/0124119 A1 5/2010 Lee 2012/00163096 A1* 6/2012 Puttasayama G11C 16/0483 365/185.2 2012/0294087 A1 11/2012 Seo G11C 16/3468 2013/0163326 A1* 6/2013 Lee 2013/0272067 A1 10/2013 Lee 2015/0262682 A1 9/2015 Puttasayama (Continued)</p> <p>FOREIGN PATENT DOCUMENTS</p> <p>CN 101567213 A 10/2009 CN 101740129 A 6/2010 (Continued)</p> <p>Primary Examiner — Han Yang (74) Attorney, Agent, or Firm — Winston Hsu</p> <p>(57) ABSTRACT A memory includes a first portion, a second portion and a controller. The first portion includes a first word line to a kth word line. The second portion is formed above the first portion and includes a (k+1)th word line to an mth word line. When an xth word line is used to perform a program operation, the controller is used to apply a first voltage to the first word line to an (x-2)th word line, a second voltage to an (x-1)th word line, and a third voltage to an (x+1)th word line. x, k and m are positive integers.</p> <p>(21) Appl. No.: 17/472,560</p> <p>(22) Filed: Sep. 10, 2021</p> <p>(65) Prior Publication Data US 2021/0407599 A1 Dec. 30, 2021</p> <p>Related U.S. Application Data (60) Division of application No. 16/827,734, filed on Mar. 24, 2020, now Pat. No. 11,195,590, which is a continuation of application No. PCT/CN2020/074580, filed on Feb. 10, 2020.</p> <p>(51) Int. Cl. G11C 16/34 (2006.01) G11C 16/08 (2006.01) G11C 16/10 (2006.01)</p> <p>(52) U.S. CL. CPC — G11C 16/3418 (2013.01); G11C 16/08 (2013.01); G11C 16/10 (2013.01)</p> <p>14 Claims, 7 Drawing Sheets</p>		

Ex. 1001 (164 Patent).

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Overview of the '941 Patent

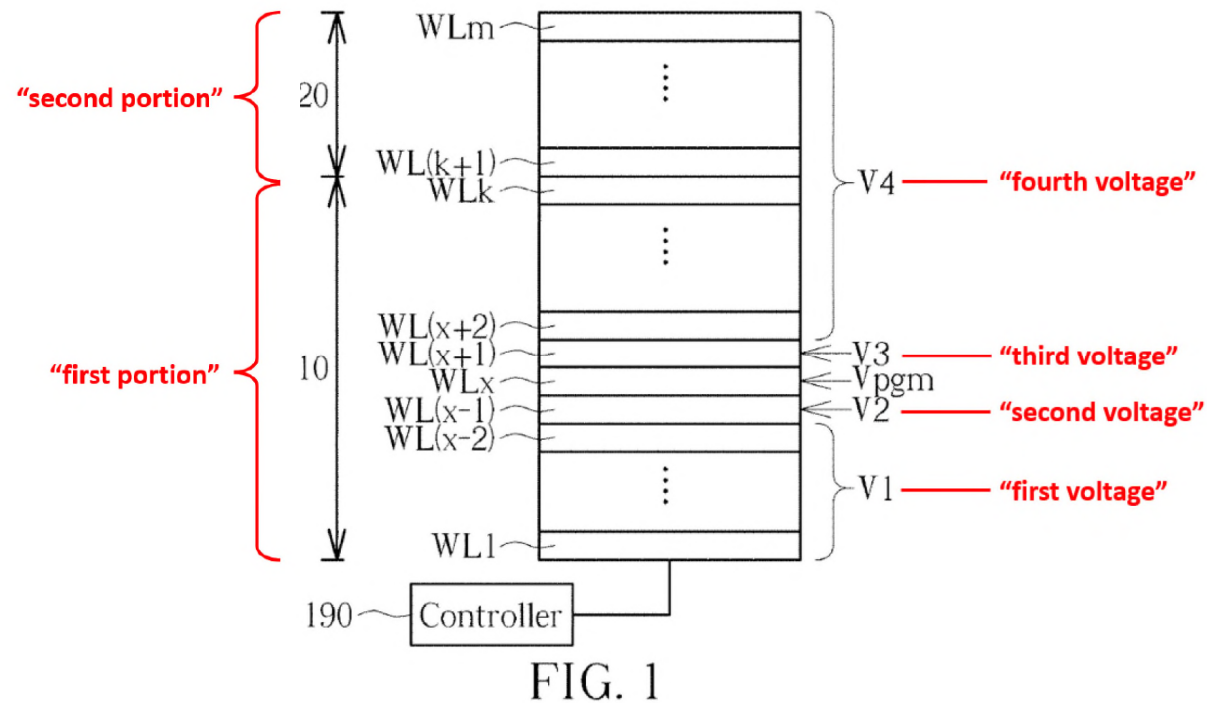
(12) United States Patent Song et al.		(10) Patent No.: US 11,568,941 B2
		(45) Date of Patent: Jan. 31, 2023
(54) MEMORY INCLUDING A PLURALITY OF PORTIONS AND USED FOR REDUCING PROGRAM DISTURBANCE AND PROGRAM METHOD THEREOF		(58) Field of Classification Search CPC G11C 16/3418; G11C 16/08; G11C 16/10 See application file for complete search history.
(71) Applicant: Yangtze Memory Technologies Co., Ltd., Wuhan (CN)		(56) References Cited
(72) Inventors: Yali Song, Wuhan (CN); XiangNan Zhao, Wuhan (CN); Ying Cul, Wuhan (CN)		U.S. PATENT DOCUMENTS
(73) Assignee: Yangtze Memory Technologies Co., Ltd., Wuhan (CN)		6,961,270 A 5/2000 Choi
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.		10,369,570 B2 * 4/2019 Lee G11C 16/3459
		2009/0257280 A1 10/2009 Oh
		2010/0124119 A1 5/2010 Lee
		2012/00163096 A1* 6/2012 Puttasayama G11C 16/0483
		2012/0294087 A1 11/2012 Seo 365/185.2
		2013/0163326 A1* 6/2013 Lee G11C 16/3468
		2013/0272067 A1 10/2013 Lee 365/185.23
		2015/0262682 A1 9/2015 Puttasayama
		(Continued)
(21) Appl. No.: 17472,560		FOREIGN PATENT DOCUMENTS
(22) Filed: Sep. 10, 2021		CN 101567213 A 10/2009
(65) Prior Publication Data		CN 101740129 A 6/2010
US 2021/0407599 A1 Dec. 30, 2021		(Continued)
Related U.S. Application Data		Primary Examiner — Han Yang
(60) Division of application No. 16/827,734, filed on Mar. 24, 2020, now Pat. No. 11,195,590, which is a continuation of application No. PCT/CN2020/074580, filed on Feb. 10, 2020.		(74) Attorney, Agent, or Firm — Winston Hsu
(51) Int. Cl.		(57) ABSTRACT
G11C 16/34 (2006.01)		A memory includes a first portion, a second portion and a controller. The first portion includes a first word line to a kth word line. The second portion is formed above the first portion and includes a (k+1)th word line to an mth word line. When an xth word line is used to perform a program operation, the controller is used to apply a first voltage to the first word line to an (x-2)th word line, a second voltage to an (x-1)th word line, and a third voltage to an (x+1)th word line. x, k and m are positive integers.
(52) U.S. Cl.		
CPC G11C 16/3418 (2013.01); G11C 16/08 (2013.01); G11C 16/10 (2013.01)		
		14 Claims, 7 Drawing Sheets



- Purportedly reduces “program disturb[]” and “pass voltage disturb[]” (col. 1:39-41, 6:39-43)
- Generically discloses wordline “portions” and non-specific “voltages” applied thereto (e.g., Figs. 1-11)
- Asserts that “program disturbance and pass voltage disturbance may be reduced **according to simulations and experiments**” (col. 6:39-43)
- But the specification lacks a single concrete example or any simulation/experiment results

Ex. 1001 ('941 Patent)
Petition, 15-21

Overview of the '941 Patent



Ex. 1001 ('941 Patent), Fig. 1
Petition, 18-21

Claim 5 of the '941 Patent

5. A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first wordline to a kth wordline from bottom to top, the second portion formed above the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top, the program method comprising:

[a] applying a first voltage to the to the first wordline to an (x-2)th wordline when an xth wordline is used to perform a program operation;

[b] applying a second voltage to an (x-1)th wordline; and

[c] applying a third voltage to an (x+1)th wordline;

[d] wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

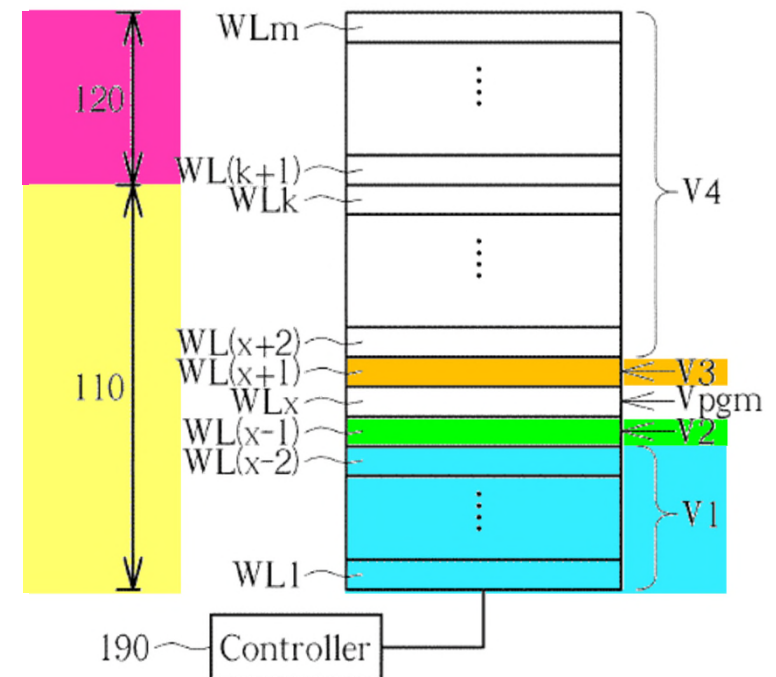


FIG. 1

Ex. 1001 ('941 Patent) Fig. 1, Claim 5
Petition, ix

Claim 1 of the '941 Patent

1. A memory comprising:

[a] a first portion comprising an (m+1)th wordline to an nth wordline from bottom to top; and

[b] a second portion formed below the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top; and

[c] a controller configured to apply

[d] a first voltage to an (x+2)th wordline to the nth wordline,

[e] a second voltage to an (x+1)th wordline,

[f] a third voltage to an (x-1)th wordline,

[g] a fourth voltage to the (m+1)th wordline to an (x-2)th wordline, and

[h] a fifth voltage to the (k+1)th wordline to the mth wordline when an xth wordline is used to perform a program operation;

[i] wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

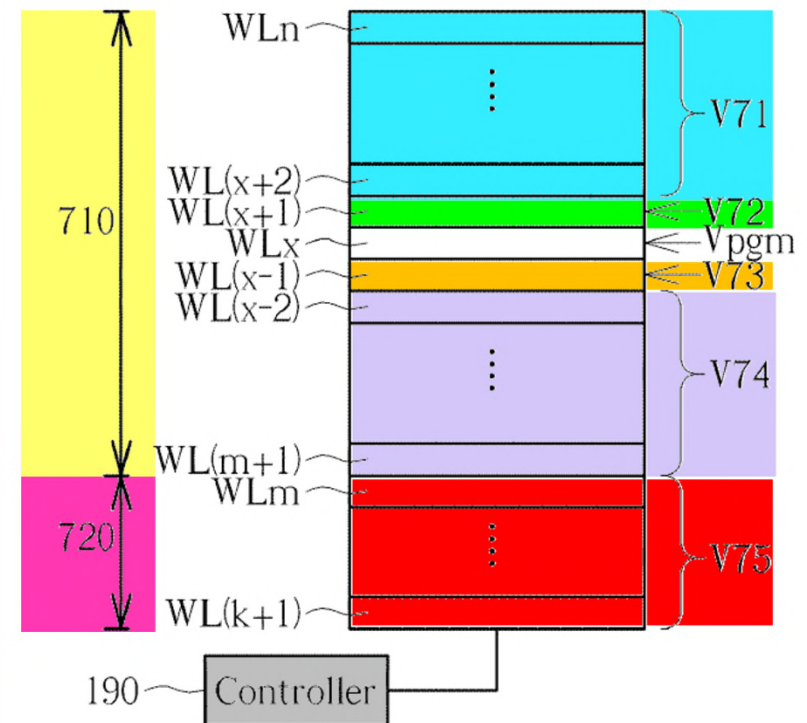
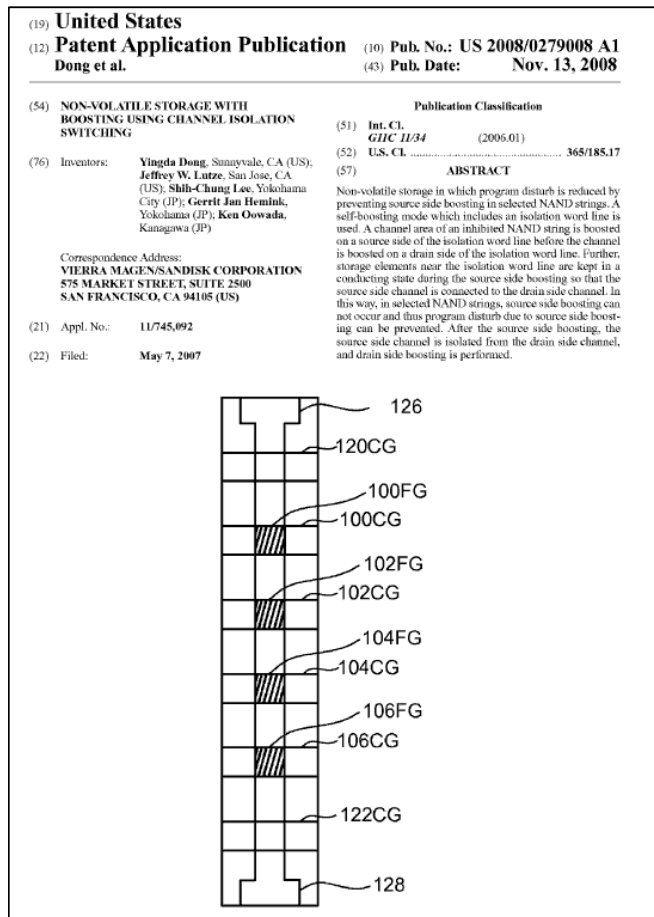


FIG. 8

Ex. 1001 ('941 Patent) Fig. 8, Claim 1
Petition, viii

Overview of Dong (All Grounds)



- **U.S. Pat. Pub. 2008/0279008**
- **Titled “Non-volatile Storage with Boosting Using Channel Isolation”**
- **Assignee:** SanDisk Corp.
- **Publication Date:** November 13, 2008 (more than a decade before the '941 priority date)
- **Prior Art:** 35 U.S.C. §102(a)(1) and (2)

*Ex. 1005 (Dong)
 Petition, 23-25*

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Overview of Dong (All Grounds)—Figs. 5a and 5g

Fig. 5a

V_{SGD}	SGD
V_{PASS}	WLn+1 through WLi
V_{PGM}	WLn
V_{ISO}	WLn-1
V_{PASS}	WL0 through WLn-2
V_{SGS}	SGS

Fig. 5g

V_{SGD}	SGD
V_{PASS}	WLn+2 through WLi
$V_{PASS-HIGH}$	WLn+1
V_{PGM}	WLn
$V_{PASS-HIGH}$	WLn-1
$V_{PASS-MEDIUM}$	WLn-2
$V_{PASS-LOW}$	WLn-3
V_{LOW}	WLn-4
V_{ISO}	WLn-5
V_{LOW}	WLn-6
$V_{PASS-LOW}$	WLn-7
V_{PASS}	WL0 through WLn-8
V_{SGS}	SGS

*Ex. 1005 (Dong), Figs. 5a and 5g
Petition, 25*

Overview of Dong (All Grounds)

[0095] FIG. 12 is a block diagram of a non-volatile memory system using single row/column decoders and read/write circuits. The diagram illustrates a memory device 1296 having read/write circuits for reading and programming a page of storage elements in parallel, according to one embodiment of the present invention. Memory device 1296 may include one or more memory die 1298. Memory die 1298 includes a two-dimensional array of storage elements 1100, control circuitry 1210, and read/write circuits 1265. In some embodiments, the array of storage elements can be three dimensional. The memory array 1100 is addressable by word lines via a row decoder 1230 and by bit lines via a column decoder 1260. The read/write circuits 1265 include multiple sense blocks 1200 and allow a page of storage elements to be read or programmed in parallel. Typically a controller 1250 is included in the same memory device 1296 (e.g., a removable storage card) as the one or more memory die 1298. Commands and Data are transferred between the host and controller 1250 via lines 1220 and between the controller and the one or more memory die 1298 via lines 1218.

*Ex. 1005 (Dong), [0095]
Petition, 19-23, 34-35*

Overview of Dong (All Grounds)

In some embodiments, the array of storage elements can be **three dimensional**.

*Ex. 1005 (Dong), [0095]
Petition, 19-23, 34-35*

Overview of Costa (Ground 3)

(19) **United States**
 (12) **Patent Application Publication** (10) **Pub. No.: US 2018/0012667 A1**
Costa (43) **Pub. Date: Jan. 11, 2018**

(54) **WORD LINE DEPENDENT PASS VOLTAGES IN NON-VOLATILE MEMORY** (52) **U.S. CL.**
 CPC ——— *G11C 16/3445* (2013.01); *G11C 16/28* (2013.01); *G11C 16/10* (2013.01); *G11C 16/0483* (2013.01); *G06F 11/1076* (2013.01)

(71) Applicant: **SanDisk Technologies LLC**, Plano, TX (US)
 (72) Inventor: **Xiyang Costa**, San Jose, CA (US)
 (73) Assignee: **SanDisk Technologies LLC**, Plano, TX (US)
 (21) Appl. No.: **15/204,257**
 (22) Filed: **Jul. 7, 2016**

Publication Classification
 (51) **Int. Cl.**
G11C 16/34 (2006.01)
G11C 16/04 (2006.01)
G11C 16/28 (2006.01)
G11C 16/10 (2006.01)
G06F 11/10 (2006.01)

ABSTRACT
 Sensing in non-volatile memory is performed using bias conditions that are dependent on the position of a selected memory cell within a group of non-volatile memory cells. During sensing, a selected memory cell receives a reference voltage while the remaining memory cells receive a read or verify pass voltage. For at least a subset of the unselected memory cells, the pass voltage that is applied is dependent upon the position of the selected memory cell in the group. As programming progresses from a memory cell at a first end of a NAND string toward a memory cell at a second end of the NAND string, for example, the pass voltage for at least a subset of the unselected memory cells that have already been subjected to programming may be increased. This technique may reduce the effects of an increased channel resistance that occurs as more memory cells are programmed.

- **U.S. Pat. Pub. 2018/0012667**
- **Titled “Word Line Dependent Pass Voltages in Non-volatile Memory”**
- **Assignee: SanDisk**
- **Publication Date: January 11, 2018**
- **Prior Art: 35 U.S.C. §102(a)(1) and (2)**

Ex. 1012 (Costa)
 Petition, 25-26

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Overview of Costa (Ground 3)

(57)

ABSTRACT

Sensing in non-volatile memory is performed using bias conditions that are dependent on the position of a selected memory cell within a group of non-volatile memory cells. During sensing, a selected memory cell receives a reference voltage while the remaining memory cells receive a read or verify pass voltage. For at least a subset of the unselected memory cells, the pass voltage that is applied is dependent upon the position of the selected memory cell in the group. As programming progresses from a memory cell at a first end of a NAND string toward a memory cell at a second end of the NAND string, for example, the pass voltage for at least a subset of the unselected memory cells that have already been subjected to programming may be increased. This technique may reduce the effects of an increased channel resistance that occurs as more memory cells are programmed.

*Ex. 1012 (Costa), Abstract
Petition, 25-26*

Overview of Shirai (Ground 4)

(19) **United States**
 (12) **Patent Application Publication** (10) Pub. No.: **US 2019/0214405 A1**
 SHIRAI et al. (43) Pub. Date: **Jul. 11, 2019**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

(71) Applicant: **TOSHIBA MEMORY CORPORATION**, Minato-ku (JP)

(72) Inventors: **Kaito SHIRAI**, Yokohama (JP); **Hidetaka Takakida**, Nagoya (JP); **Tatsuo Izumi**, Yokohama (JP); **Reiko Shimoto**, Nagoya (JP); **Takahisa Kanemura**, Yokohama (JP); **Shigeo Kondo**, Yokohama (JP)

(73) Assignee: **TOSHIBA MEMORY CORPORATION**, Minato-ku (JP)

(21) Appl. No.: 16/951,832

(22) Filed: **Mar. 13, 2019**

Related U.S. Application Data
 (63) Continuation of application No. PCT/JP2016/077817, filed on Sep. 21, 2016.

Publication Classification
 (51) Int. Cl. **H01L 27/11582** (2006.01)
H01L 27/11565 (2006.01)
H01L 29/51 (2006.01)
H01L 21/28 (2006.01)
 (52) U.S. Cl. **H01L 27/11582** (2013.01); **H01L 21/28282** (2013.01); **H01L 29/517** (2013.01); **H01L 27/11565** (2013.01)

ABSTRACT
 According to one embodiment, the stacked body includes a first stacked portion including a plurality of electrode layers, a second stacked portion including a plurality of electrode layers, and being disposed separately from the first stacked portion in the first direction, and a connection portion including a high dielectric layer provided between the first stacked portion and the second stacked portion and having a dielectric constant higher than a dielectric constant of the insulator. The column-shaped portion includes a first portion provided in the first stacked portion and extending in the first direction of the stacked body, a second portion provided in the second stacked portion and extending in the first direction, and an intermediate portion provided in the connection portion and connected the first portion to the second portion.

- **U.S. Pat. Pub. 2019/0214405**
- **Titled “Semiconductor Device and Method of Manufacturing the Same”**
- **Assignee: Toshiba**
- **Publication Date: July 11, 2019**
- **Prior Art: 35 U.S.C. §102(a)(1) and (2)**

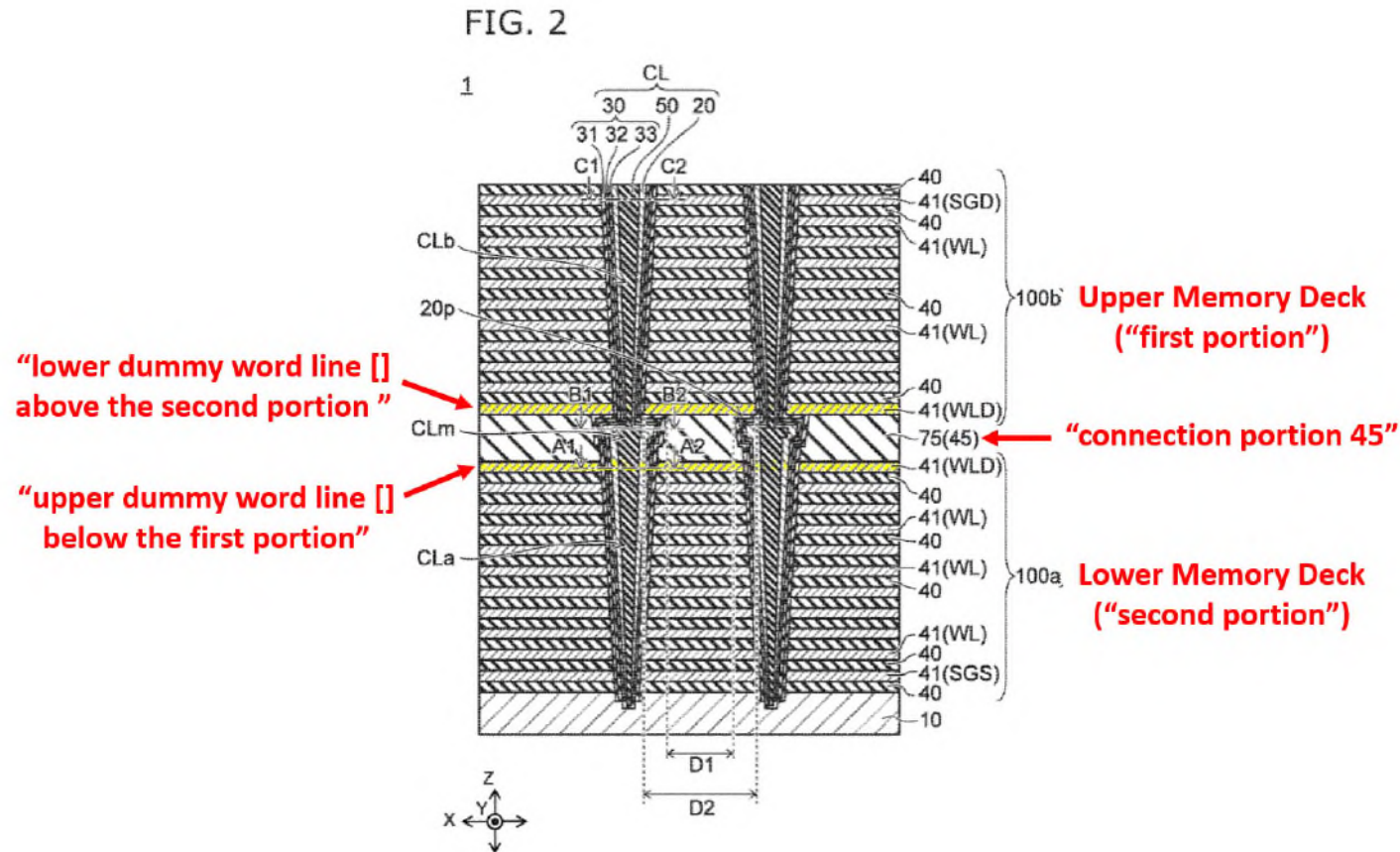
*Ex. 1018 (Shirai)
 Petition, 27-28*

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

22

**Micron Ex. 1112, p. 22
 Micron v. YMT
 IPR2025-00190**

Overview of Shirai (Ground 4)



Ex. 1018 (Shirai), Fig. 2
Petition, 27-28, 81

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 - Under Patent Owner's Bottom-to-Top Construction
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Ground 1 – Dong Anticipates Under Petitioner’s Construction

A. Dong Satisfies “*bottom-to-top*” Under Petitioner’s Construction

PO does not dispute that Dong satisfies the *bottom-to-top* requirement under Petitioner’s construction. *See* POR. While the parties dispute whether Dong discloses and/or renders obvious 3D memory strings (it does), the parties agree Dong discloses 2D memory strings. POR, 36-39. Describing Figs. 5a-h, Dong states “the

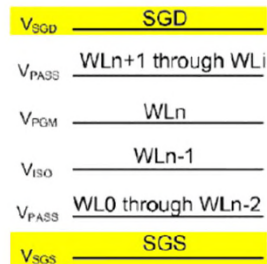
Reply, 6

Ground 1 – Dong Anticipates Under Petitioner’s Construction

source/SGS (bottom) to drain/SGD (top). Even if rotated/read “horizontally,” Figs.

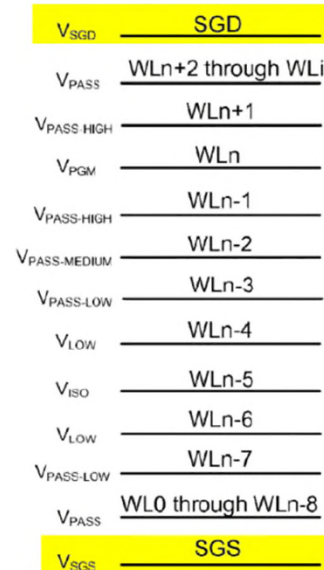
5a/g satisfy *bottom-to-top* under Petitioner’s construction.

Fig. 5a



Dong, Fig. 5a (annotated)

Fig. 5g



Dong, Fig. 5g (annotated)

Ground 1 – Dong Anticipates Under Patent Owner’s Construction

1. Anticipation Under PO’s Construction

Dong meets PO’s narrow *bottom-to-top* construction (*i.e.*, vertical memory strings). Referring to Fig. 12 (generally applicable vis-à-vis Fig. 5), Dong discloses “the array of storage elements can be *three dimensional*.” Dong, [0095]. A POSITA reading Dong in 2020 would readily envisage vertical 3D-memory. Liu_Reply, ¶¶38-56. PO denigrates Dong for its “passing” 3D-memory disclosure. POR, 2, 40.

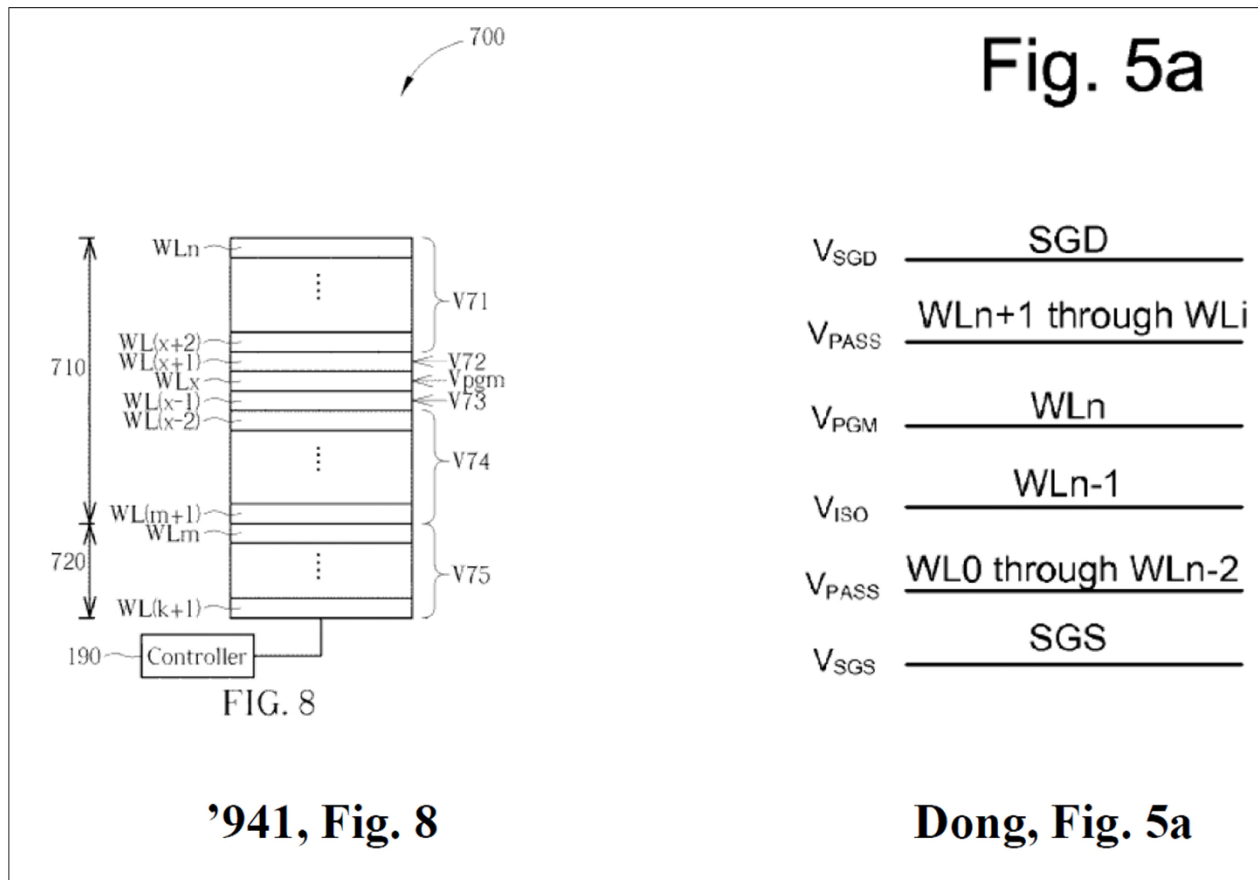
Reply, 8

Ground 1 – Dong Discloses “Three Dimensional” Memory

the present invention. Memory device 1296 may include one or more memory die 1298. Memory die 1298 includes a two-dimensional array of storage elements 1100, control circuitry 1210, and read/write circuits 1265. In some embodiments, the array of storage elements can be three dimensional. The memory array 1100 is addressable by word lines

*Dong, [0095]
Petition, 34-35*

Ground 1 – Dong Discloses Vertically Oriented Wordlines/Memory Strings



'941, Fig. 8 (left) and Dong, Fig. 5a (right)
Reply, 13

The Relevant Date for Evaluating Invalidity is 2020, Not 2007

- Petitioner says the '941 patent priority date in 2020 controls (Paper 39 (Reply), 1, 8, 24)

PO uses the wrong date (i.e., 2007 instead of 2020) to assess validity vis-à-vis the bottom-to-top limitation. Doing so is legal error, but Petitioner prevails under either date.

- Patent Owner says the 2007 filing date of the prior art controls (Paper 33 (POR), 42-43)

A POSITA would have interpreted Dong's mention of "three dimensional" memory arrays as naturally referring to 3D memory arrays that were known **as of Dong's May 7, 2007 date** ... that did not have vertically arranged wordlines.

The Relevant Date for Evaluating Invalidity is 2020, Not 2007

- The anticipation statute refers to the “the effective filing date of ***the claimed invention***”

A person shall be entitled to a patent unless—(1) the claimed invention was patented [or] described in a printed publication ... before the effective filing date of the claimed invention.

35 U.S.C. §102(a)(1)
Reply (Paper 39), 8

- The obviousness statute confirms that the ***claimed invention's*** effective filing date controls

A patent for a claimed invention may not be obtained ... if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a [POSITA].

35 U.S.C. §103
Reply (Paper 39), 24

The Relevant Date for Evaluating Invalidity is 2020, Not 2007

[O]bviousness is based on what the references would teach or suggest to POSITA at the time of the [challenged] patent filing—not at the time of filing of the [prior art] reference.

IPR2016-00488, Paper 11, 29 (PTAB, July 18, 2016)
Reply (Paper 39), 24



DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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The Relevant Date for Evaluating Invalidity is 2020, Not 2007

The determination of obviousness must be done based on the knowledge possessed by [a POSA] at the time the invention was made. The Asserted Claims and the prior art are evaluated at the time of the invention from the standpoint of a POSA. A POSA is a hypothetical person who is presumed to have access to, and be aware of, all of the relevant prior art at the time of the invention.

Amarin Pharma., Inc. v. Hikma Pharms. USA Inc., 449 F. Supp. 3d 967, 991 (D. Nev. 2020)
Reply (Paper 39), 24



The Relevant Date for Evaluating Invalidity is 2020, Not 2007

An anticipation analysis is undertaken from the perspective of [a POSITA] and, therefore, must take account of the knowledge of such a person. See *Arthrocare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1373-74 (Fed. Cir. 2005) (“[E]ven if a piece of prior art does not expressly disclose a limitation, it anticipates if a [POSITA] would understand the prior art to disclose the limitation and could combine the prior art description with his own knowledge to make the claimed invention.”). ... Such a person would have carried that knowledge with her when examining each of the challenged claims.

Sage Prods., LLC v. Stewart, 133 F.4th 1376, 1384 n.5 (Fed. Cir. 2025)
Reply (Paper 39), 8



The Relevant Date for Evaluating Invalidity is 2020, Not 2007

We are also not persuaded by [PO's] argument that because Dong was filed in May 2007, a POSITA would not understand Dong's 3D memory arrays to have vertically arranged word lines or that POSITA would not apply Dong's program disturb methods to vertical 3D NAND cells due differences between 2D and 3D NAND cells, including cell structure, array architecture, and program disturb conditions. [] An obviousness determined is assessed based on the knowledge of a POSITA at the time the challenged patent's effective filing date. See 35 U.S.C. § 103.

Institution Decision (Paper 22), 26-27



3D NAND was Synonymous with Vertical Memory Strings in 2020

vertical strings in 2020); EX1094, 103:6-15. Nor could it, given that vertical strings were the prevailing 3D architecture in 2020. Pet., §V; EX1095-1099 (YMTC patents circa 2020 showing/discussing vertical 3D strings); Liu_Reply, ¶¶40-47. The Board can take notice from IPRs involving 3D-NAND patents before the same panel that YMTC regularly described “three-dimensional” memory as having vertical strings.³ IPR2023-01401, Paper 17, 12 (“Board may consider and make of

Reply, 9

Patent Owner Repeatedly Acknowledged 3D NAND Has Vertical Strings

The Board can take notice from IPRs involving 3D-NAND patents before the same panel that YMTC regularly described “three-dimensional” memory as having vertical strings.³ IPR2023-01401, Paper 17, 12 (“Board may consider and make of

- “**3D NAND** memory [] addresses the challenges of **forming vertical wordline[s]**” – IPR2025-00117, Paper 27 (POR), 1
- “**3D NAND resembles a vertical skyscraper**” – IPR2025-00191, EX2029, 1
- “**3D NAND** memory devices generally involve[] ... **vertical structures**” – IPR2024-00788, Paper 17 (POR), 1
- “**3D NAND** flash memory technology architecture has been developed such that **the vertical NAND memory cell strings** of a same block share a bottom select gate” IPR2024-00794, Paper 12 (POR), 4 (cite omitted)

Reply, 9-10

3D NAND was Synonymous with Vertical Memory Strings in 2020

Given the well-developed state of 3D-memory in 2020, a POSITA would “at once envisage” the ’941 patent’s claimed *bottom-to-top* wordline arrangement upon reading Dong’s “three dimensional” NAND disclosure. Pet., 35; *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015); *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022). Numerous industry reports and market data confirm the prevalence of vertical 3D NAND. EX1103, 34; EX1104-EX1107; Liu_Reply, ¶¶41-46.

Reply, 9

3D NAND was Synonymous with Vertical Memory Strings in 2020

Dong Fig. 4's purpose is to "show[] a program disturb mechanism," not limit Dong to any particular memory architecture. Dong, [0045]-[0046]. And Dong Figs. 5a-h depict "storage elements which are being programmed ... [in] selected NAND strings." Dong, [0047]-[0048]. Certainly, in conjunction with Dong's "three dimensional" memory disclosure, a POSITA in 2020 would fairly read Dong's vertically-oriented Figs. 5a/g as disclosing vertical memory strings. Liu_Reply,

Reply, 14

3D NAND was Synonymous with Vertical Memory Strings in 2020

Samsung
Newsroom

Samsung Electronics Takes 3D Memory to New Heights with Sixth-Generation V-NAND SSDs for Client Computing

Korea on August 6, 2019

New V-NAND breaks through current cell stacking limitation in 3D NAND with the industry's first 100+ layer single-tier design for superior speed and power efficiency

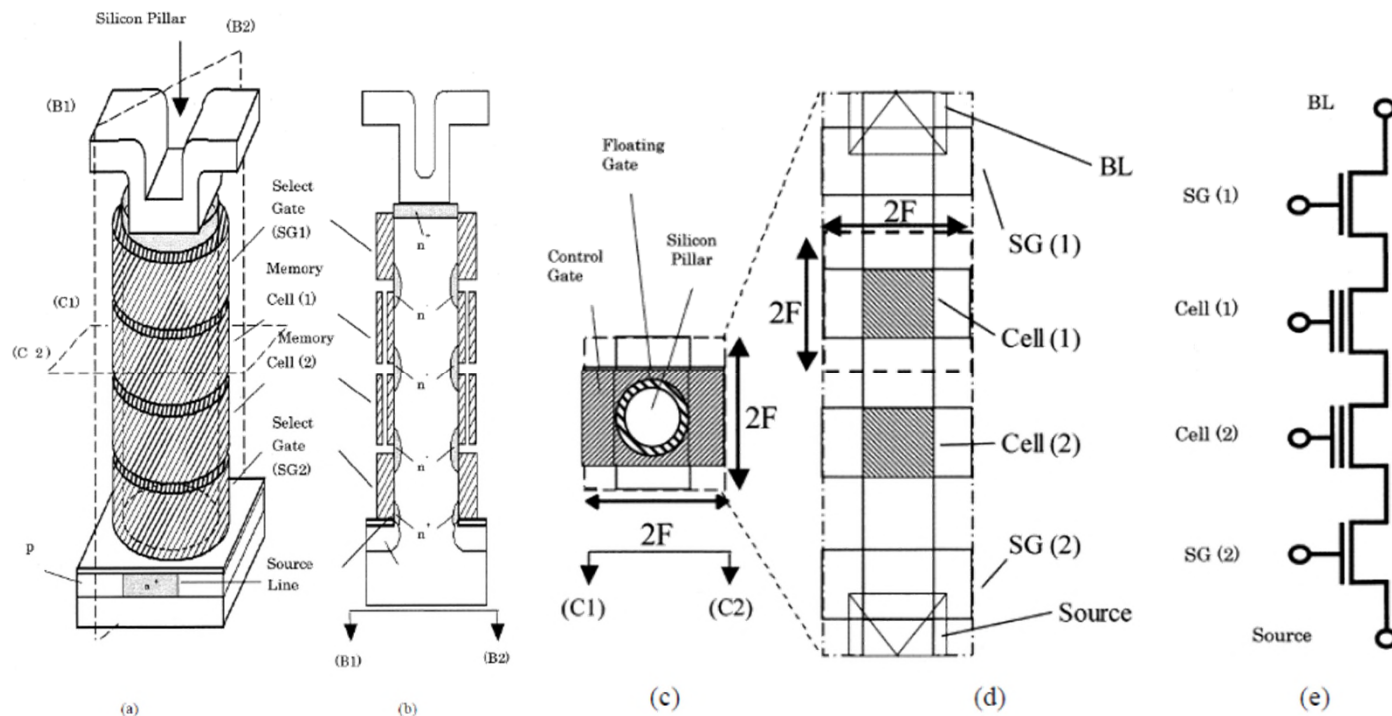
EX1104, 1
Reply, 11

“Three-Dimensional” Flash Included Vertical Memory Strings in 2007

Second, even assuming POSITA knowledge/understanding vis-à-vis anticipation was assessed in 2007 (instead of 2020), PO loses because a POSITA in 2007 would have understood Dong’s 3D disclosure to include vertical strings. Liu_Reply, ¶¶57-64. Multiple references confirm this. Endoh1 and Endoh2 show vertical strings in 2003 and 2001, respectively.

Reply, 14

The Meaning of “Three-Dimensional” NAND Flash Memory in 2007



*Endoh1 (EX1101), Figs. 3(a)-(e) (describing a “3-D memory” in 2003)
Reply, 14-16*

The Meaning of “Three-Dimensional” NAND Flash Memory in 2007

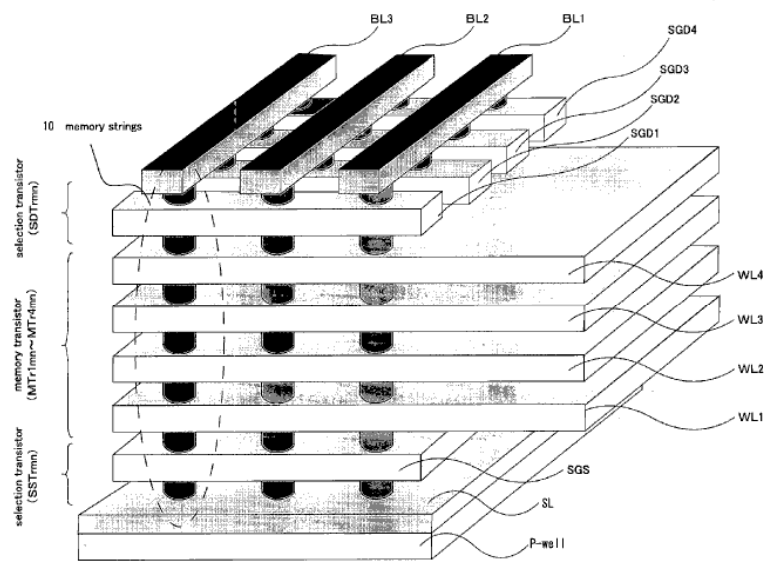


FIG. 2

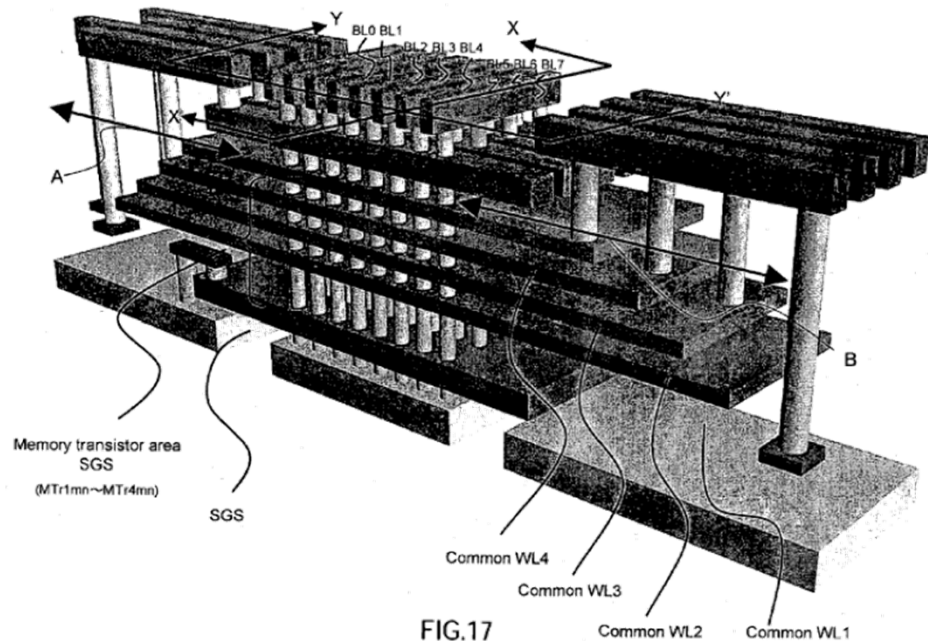
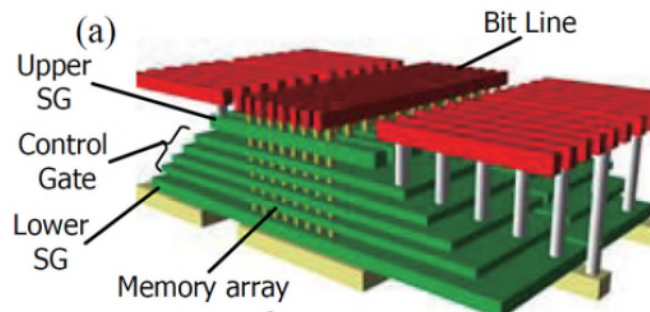


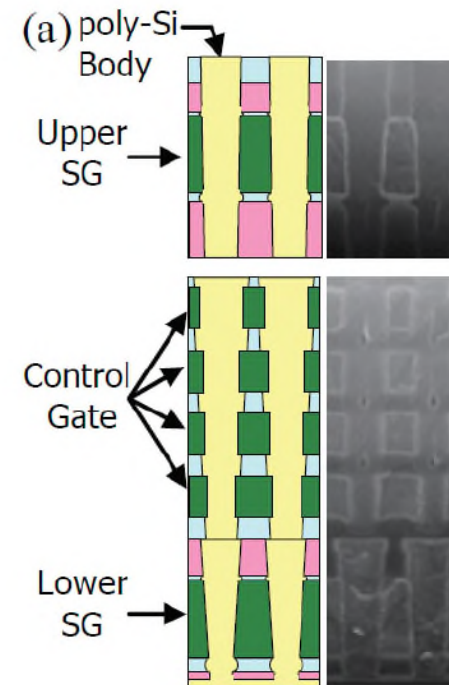
FIG. 17

*Kito (EX1087), Figs. 2, 17 (showing 3-D memory in 2007)
Reply, 14-16*

The Meaning of “Three-Dimensional” NAND Flash Memory in 2007



EX1075, Fig. 3(a)



EX1075, Fig. 7(a)

*Tanaka (EX1075), Figs. 3a, 7a
Reply, 15*

Petitioner Prevails Even If The 2007 Date Is Used

The notion that “three dimensional” vertical strings were unknown in 2007 is unsupported. It is irrelevant whether “Three-Dimensional (3D) NAND At The Time Of Dong *Included* Stacked 2D-NAND.” POR, 5-7, 42-44. What matters is that “three dimensional” memory included vertical strings.

Reply, 16

Dr. Khatri Has No Opinion On Vertical 3D NAND Strings in 2007



- Q. Do you have an opinion one way or another, Dr. Khatri, whether 3D NAND at the time of Dong's filing excluded vertical 3D NAND memory strings?
- A. Again, I have not said that. My statement is simply that -- you know, the title of Section V.I.A.2 is that, you know, 3D NAND at the time of Dong's filing includes stacked 2D NAND.

*EX1094 (Khatri), 103:6-15
Reply, 9*

Enablement and Reasonable Expectation of Success

Regarding vertical memory strings, PO ignores POSITA knowledge—which is assessed in 2020, not 2007. *Oracle Am., Inc. v. Google, Inc.*, 606 F. App’x 990, 995 (Fed. Cir. 2015). Here, PO does not dispute Petitioner’s level of skill in the art. Pet., 22-23; POR, 9; EX2028, ¶46; EX1100, ¶¶25-26. Any assertion that applying wordline voltages in vertical strings instead of horizontal ones requires undue experimentation lacks credibility. Liu_Reply, ¶¶83-87. Moreover, Dong is presumptively enabled. *In re Antor Media Corp.*, 689 F.3d 1282, 1288-89 (Fed. Cir.

Reply, 24-25

Enablement and Reasonable Expectation of Success

- EX1087 (from 2007) includes detailed manufacturing flow spanning dozens of figures
- Endoh1 (EX1101) Fig. 5 and Tanaka (EX1075) Fig. 7 show actual manufactured vertical strings in 2007

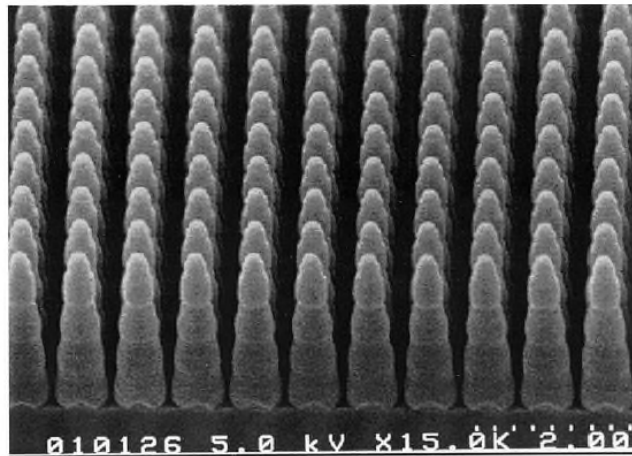


Fig. 5. SEM photograph of S-SGT structured cell.

Endoh1 (EX1101)

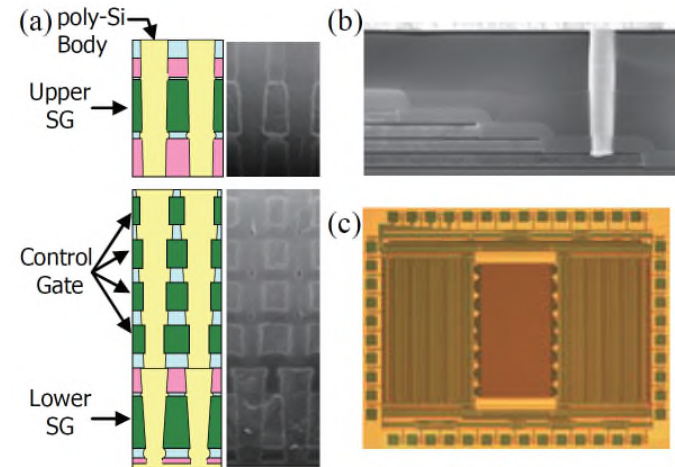


Fig. 7 (a) Cross sectional SEM of BiCS flash memory string, (b) Cross sectional SEM of edge of control gates, (c) n x 512 kbit macro image.

Tanaka (EX1075)

EX1087
Reply, 25

Roadmap

I. Introduction and IPR Grounds

II. Overview of the '941 Patent and Prior Art

III. Ground 1 (Anticipation by Dong) (claims 1, 3, 5-7, 11, 13)

- Under Petitioner's Bottom-to-Top Construction
- Under Patent Owner's Bottom-to-Top Construction

IV. Ground 2 (Obviousness over Dong) (claims 1, 3, 5-7, 11, 13)

- **Under Patent Owner's Bottom-to-Top Construction**

V. Ground 3 (Obviousness over Dong+Costa) (claims 8-9)

- Program Operation Construction

VI. Ground 4 (Obviousness over Dong+Shirai) (claims 4, 10, 14)

Patent Owner's Procedural Argument Fails

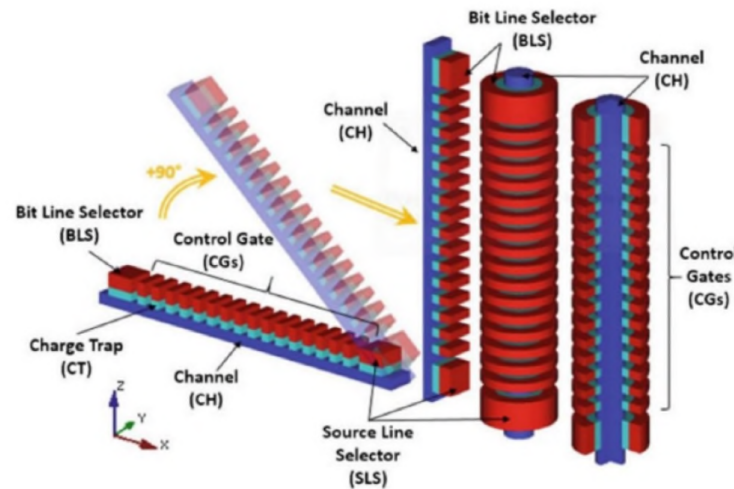
Ground 2 is “Dong renders obvious claims 1, 3, 5-7, 11, and 13 under §103.”

Pet., 7. Quoting textbooks, the Petition explains 2D-to-3D NAND evolution, including the “many similarities between 2D- and 3D-NAND ..., including the techniques and algorithms used to program memory cells.” *Id.*, 12-14. The Petition quotes references explaining that “3D-NAND [] could be conceived by starting from the 2D-NAND string building block” and “turning the 2D-NAND string upside,” “resulting” in a “3D structure” with “vertical channel[s].” *Id.* (quoting EX1011, 3).

Reply, 16-18

Patent Owner's Procedural Argument Fails

Id., 40. “[T]o further scale down the memory cell size,” “three-dimensional (3D) NAND flash cells” were developed. *Id.*, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1011, 3.



EX1010, 12
Petition, 13

Patent Owner's Procedural Argument Fails

Ex. 1009, 393. Given that the origins of 3D NAND came from 2D NAND, there are many similarities between 2D and 3D NAND flash memory devices, including basic principles of operation, memory storage techniques, the techniques and algorithms used to read, erase, and program memory cells and memory cell strings. In this context, the term “program” refers to writing/storing/saving data to a memory cell.

*Liu (EX1004), ¶54
Petition, 14*

Patent Owner's Procedural Argument Fails

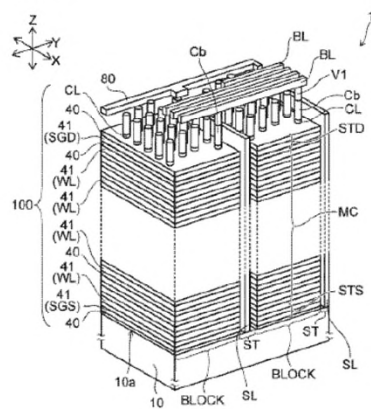
language. Thus, regardless of whether Figure 5a is read as a 2D or 3D memory string it meets the claim language. And, given the similarities between 2D and 3D NAND discussed in the Technology Background section, even a 2D memory string would at a minimum render obvious the *bottom to top* requirement, even if narrowly construed.

*Liu (EX1004), ¶120
Petition, 35*

Patent Owner's Procedural Argument Fails

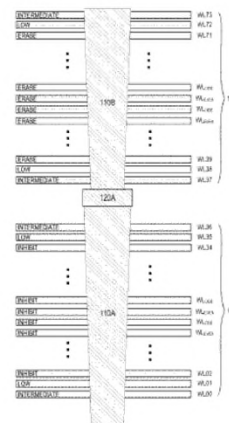
PO's assertion is belied by the Petition's holistic discussion of how "Dong anticipates and/or renders obvious claim 5." Pet., 29-33. The Petition explains it "would have been obvious" to use long memory strings, citing vertical 3D-NAND references like Sharai and Righetti. *Id.*, 31.

FIG. 1



Shirai, Fig. 1, [0019]

FIG. 6



Righetti, Fig. 6.

PO ignores this disclosure, which distinguishes 3M (POR, 48-49).

Reply, 18

Patent Owner's Procedural Argument Fails

We are not persuaded by Patent Owner's arguments at this stage of the proceeding because they fail to address Petitioner's contentions about 3D NAND memory, including that 3D NAND flash devices have strings of memory cells placed in the vertical direction (Ex. 1004 ¶ 56 (citing Ex. 1009, 296)) and the similarities between 2D and 3D NAND flash memory devices, including the techniques and algorithms used to program the cells of such devices. *See e.g.*, Pet. 14.

Institution Decision, 26

Patent Owner Loses on the Merits of Obviousness

incorrect. Liu_Reply, ¶¶65-82. The Aritome textbook PO cites (EX1009) directly contradicts PO's conclusion that Dong is inapplicable to 3D memory strings. Aritome §8.4.1 explains/compares/contrasts four program disturb modes—two “[c]onventional” modes present in both 2D and 3D memory, and two “[a]dditional” disturb modes only present in 3D-memory. EX1009, §8.4.1.

Conventional modes

Mode	DSL	BL
①: STR in PGM	ON	0V
②: STR in X mode	ON	Vcc

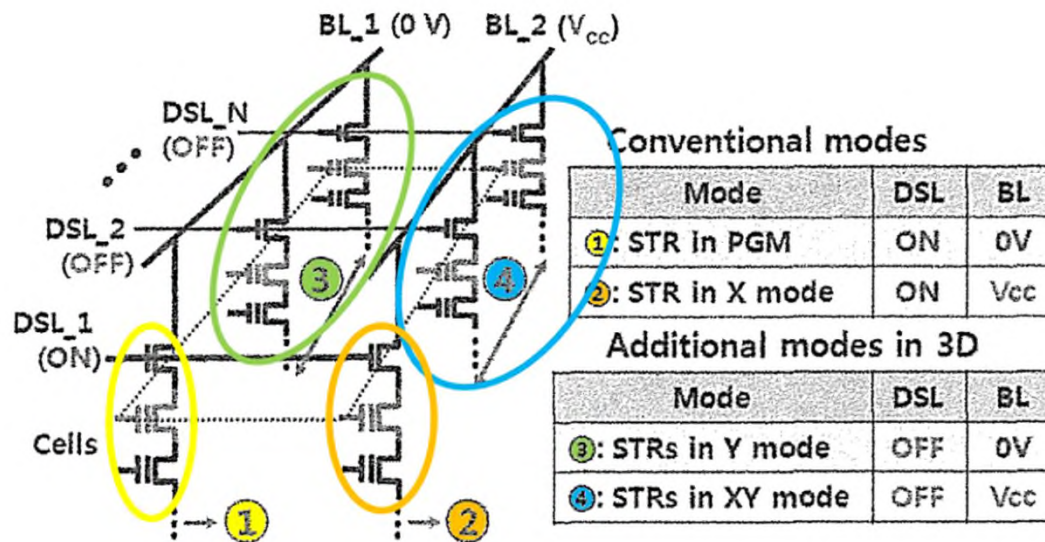
Additional modes in 3D

Mode	DSL	BL
③: STRs in Y mode	OFF	0V
④: STRs in XY mode	OFF	Vcc

*Aritome (EX1009), Fig. 8.11 (excerpted)
Reply, 19*

Patent Owner Loses on the Merits of Obviousness

EX1009, Fig. 8.11 (excerpted). Aritome labels the four program disturb modes ①(PGM), ②(X-mode), ③(Y-mode), and ④(XY-mode), based on which memory string(s) are affected. EX1009, 363, Fig. 8.11.⁶ Fig., 8.11 shows the string(s) where each mode manifests. Liu_Reply, ¶¶67-68.



Aritome (EX1009), Fig. 8.11 (annotated)
Reply, 19-20

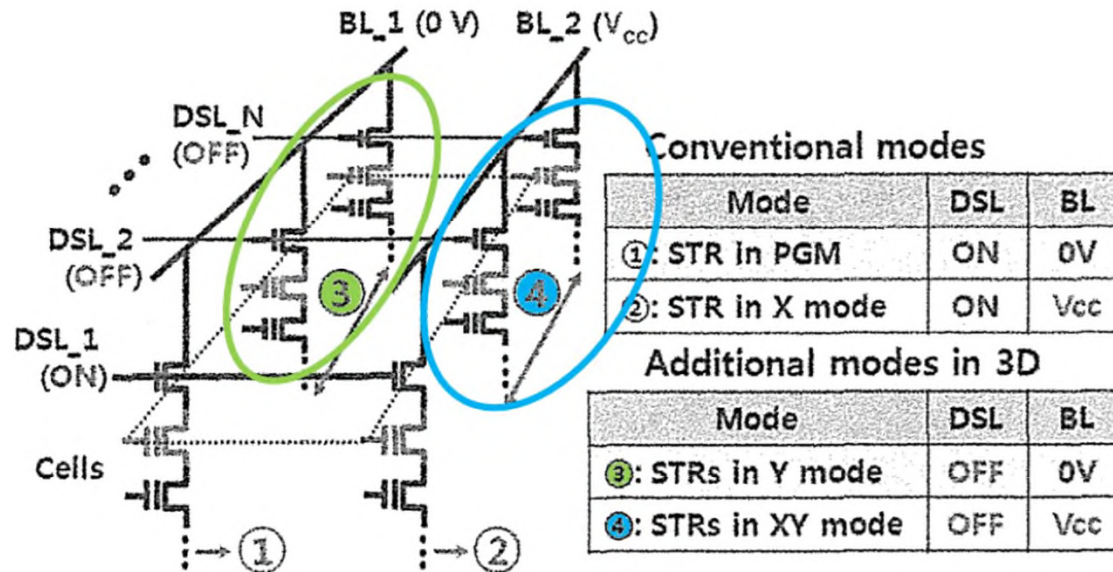
Patent Owner Loses on the Merits of Obviousness

Per Aritome, “[c]onventional” disturb modes (①PGM and ②X modes) exist in 2D- and 3D-memory. EX1009, Fig. 8.11; *id.*, 363 (“Disturb X-mode is the same as a conventional program disturb mode in a 2D-NAND cell.”); Fig. 2.22 (showing 2D-NAND “ V_t shift of program disturb” in selected and unselected strings); Liu_Reply, ¶¶69-70. Dong addresses both modes. *Id.*, ¶72; Dong, [0011] (“Program disturb can occur at inhibited NAND string ... [and] the programmed NAND string itself”). Accordingly, even if Dong’s program disturb solutions were made in the 2D-NAND context, they apply with equal (or greater) force to 3D-NAND to address the “[c]onventional” “PGM”① and “X-mode”② disturb. EX1009, 363; Liu_Reply,

Reply, 20

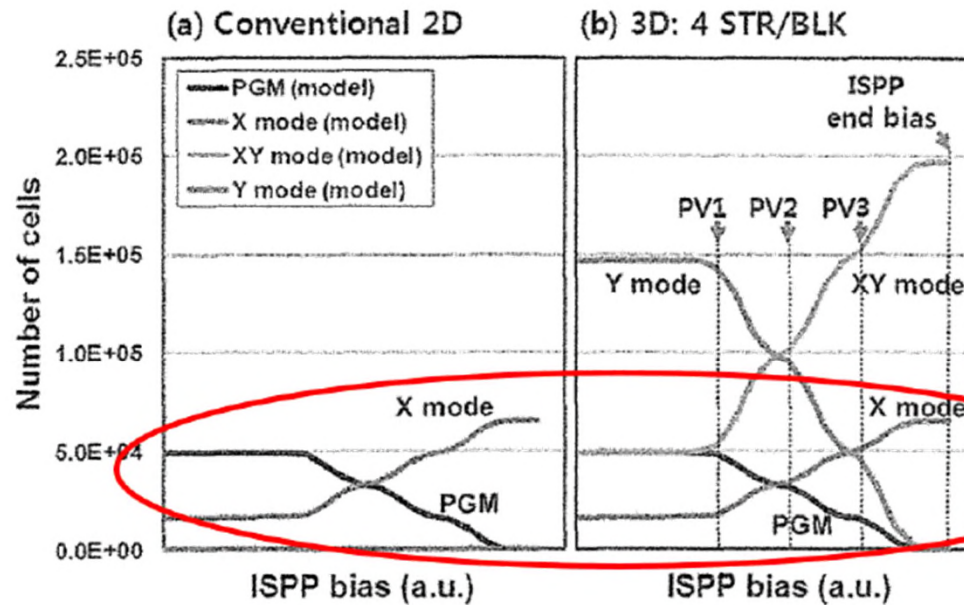
Patent Owner Focused on the Wrong Disturb Modes (3 and 4)

PO erroneously focused on *the wrong program disturb* modes (*i.e.*, modes ③ and ④). Liu_Reply, ¶¶75-77. Aritome Fig. 8.11 shows Y-mode③ and XY-mode④ memory strings (where drain select line (DSL) is “OFF”).



EX1009, Fig. 8-11 (annotated).

Disturb Modes 1 and 2 Exist in Both 2D and 3D NAND



PGM mode and X-mode
disturb identical in 2D and 3D

FIGURE 8.15 Probability (number of cells) of each program disturbance mode with increasing ISPP bias.

Aritome (EX1009), Fig. 8.15 (annotated)
Reply, 22

Neither Dong nor the '941 Patent Addresses Modes 3 and 4

This is clear from Aritome, which proffers three solutions for the new disturb modes: “(1) high V_t of DSL, (2) applying negative bias to DSL, and (3) inserting dummy wordlines between DSL and edge wordline.” EX1009, 363-364. Because neither Dong nor the '941 patent disclose disturb solutions based on DSL (drain select) lines (or nearby dummy wordlines) (*see* EX1094, 297:14-23), they self-evidently address PGM^① and/or X-mode^②. Moreover, if Aritome’s Y-mode^③ and XY-mode^④ solutions solved program disturb, the '941 patent would serve no purpose.

Reply, 22

Dr. Khatri Admits the '941 Solution Ignores Drain/Gate Select Transistors



So if we -- as we've discussed, if we look at the '941 Patent -- and I'll just open it real quick -- you know, its figures are all talking about voltages applied to word lines, like WL something, you know, various WLs.

But it's not talking about the additional transistors, the select transistors, like DSL, for example, because that's not the focus of the '941 Patent.

*EX1094 (Khatri), 297:14-23
Reply, 22*

Roadmap

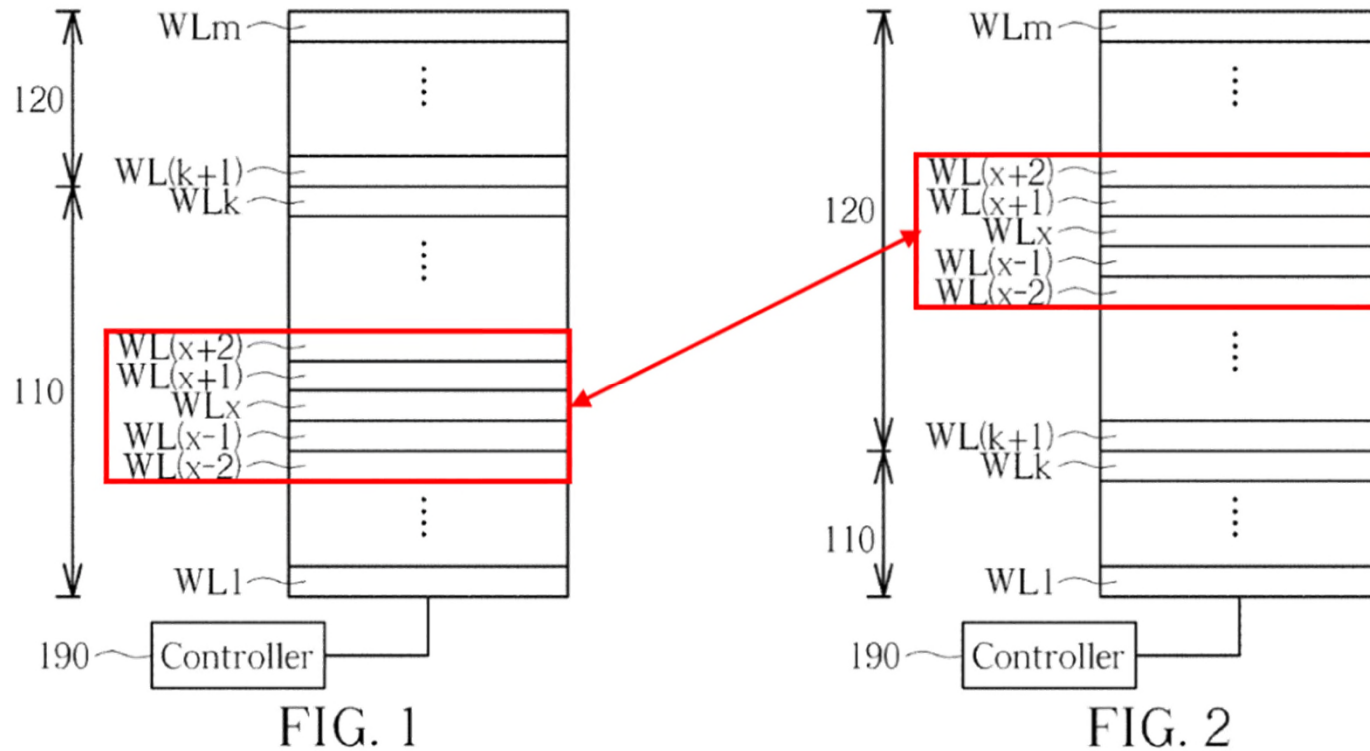
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 - Under Patent Owner's Bottom-to-Top Construction
- V. Ground 3 (Obviousness over Dong+Costa) (claims 8-9)**
 - Program Operation Construction**
- VI. Ground 4 (Obviousness over Dong+Shirai) (claims 4, 10, 14)

Ground 3 – Claims 8 and 9 (Location Dependent Vpass)

9. The program method of claim 5, wherein:
the first voltage has a first level if the xth word line is in
the first portion;
the first voltage has a second level if the xth word line is
in the second portion; and
the first level is lower than the second level.

*EX1001, claim 9
Petition, xi, 70-76*

All Wordlines Are Programmed in the '941 Patent



'941, Figs. 1-2 (excerpted and annotated)
Petition, 19

Costa Discloses Increasing Vpass as More Cells are Programmed

(57)

ABSTRACT

Sensing in non-volatile memory is performed using bias conditions that are dependent on the position of a selected memory cell within a group of non-volatile memory cells. During sensing, a selected memory cell receives a reference voltage while the remaining memory cells receive a read or verify pass voltage. For at least a subset of the unselected memory cells, the pass voltage that is applied is dependent upon the position of the selected memory cell in the group. As programming progresses from a memory cell at a first end of a NAND string toward a memory cell at a second end of the NAND string, for example, the pass voltage for at least a subset of the unselected memory cells that have already been subjected to programming may be increased. This technique may reduce the effects of an increased channel resistance that occurs as more memory cells are programmed.

*Ex. 1012 (Costa), Abstract
Petition, 25-26*

Patent Owner's Argument Fails Because All Cells Are Programmed

Instead, PO asserts that “Petitioner’s application of Dong to independent claim 5 fails when carried forward to address claims 8 and 9.” POR, 55. This argument fails because PO ignores that Petitioner’s invalidity analysis was not limited to programming the fourth wordline (*viz.*, $x=4$).⁸ Pet., 33 (“[T]hese mappings are merely exemplary and other mappings also satisfy [claim 5]”).

Reply, 26

Costa Discloses Increasing V_{pass} as More Cells are Programmed

As Costa teaches (and a POSITA would have known), “[t]he channel resistance increases as each memory cell is programmed, leading to the highest resistance and lowest channel conductance when programming the later programmed memory cells.” Costa, [0029]; *see also id.*, [0101]; Liu, ¶ 210. The increased channel resistance may cause “later programmed memory cells ... to be programmed to higher levels than intended.” Costa, [0029]. Costa combats this adverse impact on memory cell threshold voltages by applying “a variable pass voltage” dependent on the location of the cell being programming in the memory string. Costa, Abstract, [0029], [0101]-[0104]. Dong is silent regarding how V_{PASS}

Petition, 72

Patent Owner's Argument Fails Because All Cells Are Programmed

Dong discloses that “programming continues sequentially until all memory cells ... are programmed.” Pet. 31; *id.*, 62, 34 (quoting Dong, [0048]); Dong, Fig. 10, [0089]. Costa teaches the same. Costa, Abstract (“programming progresses [through all memory string cells]”). Thus, all cells/wordlines in the Dong/Costa combination would be programmed. This necessarily includes all cells in the *first*, *second*, and *third portion[s]*. Nor would it make sense to constrain Petitioner's

Reply, 26

Numerous Examples Satisfy Claims 8 and 9

Claim 9 Example

		VSGD		
Second Portion	WL31	(Vpass)	(Vpass)	m=32
	WL30	(Vpass)	(Vpass)	
	WL29	(Vpass)	(Vpass)	
	WL28	(Vpass)	(Vpass)	
	WL27	(Vpass)	(Vpass)	
	WL26	(Vpass)	(Vpass)	
	WL25	(Vpass)	(Vpass)	
	WL24	(Vpass)	(Vpass)	
	WL23	(Vpass)	(Vpass)	
	WL22	(Vpass)	(Vpass)	
	WL21	(Vpass)	(Vpass)	
	WL20	(Vpass)	V3 (Vpass)	X+1
	WL19	(Vpass)	VPGM	X=20
	WL18	(Vpass)	V2 (Viso)	X-1
	WL17	(Vpass)	V1 (Vpass)	X-2
	First Portion	WL16	(Vpass)	V1 (Vpass)
WL15		(Vpass)	V1 (Vpass)	k=16
WL14		(Vpass)	V1 (Vpass)	
WL13		(Vpass)	V1 (Vpass)	
WL12		(Vpass)	V1 (Vpass)	
WL11		(Vpass)	V1 (Vpass)	
WL10		(Vpass)	V1 (Vpass)	
WL9		(Vpass)	V1 (Vpass)	
WL8		(Vpass)	V3 (Vpass)	
WL7		(Vpass)	V1 (Vpass)	
WL6		(Vpass)	V1 (Vpass)	
WL5		(Vpass)	V1 (Vpass)	X+2
WL4		V3 (Vpass)	V1 (Vpass)	X+1
WL3		VPGM	V1 (Vpass)	X=4
WL2		V2 (Viso)	V1 (Vpass)	X-1
WL1		V1 (Vpass)	V1 (Vpass)	X-2
WL0	V1 (Vpass)	V1 (Vpass)		
		VSGS		

Claim 8 Example

		VSGD			
Third Portion	WL31	(Vpass)	(Vpass)	V4 (Vpass)	n=32
	WL30	(Vpass)	(Vpass)	V4 (Vpass)	X+2
	WL29	(Vpass)	(Vpass)	V3 (Vpass)	X+1
	WL28	(Vpass)	(Vpass)	VPGM	X=29
	WL27	(Vpass)	(Vpass)	V2 (Viso)	X-1
	WL26	(Vpass)	(Vpass)	V1 (Vpass)	X-2
	WL25	(Vpass)	(Vpass)	V1 (Vpass)	
	WL24	(Vpass)	(Vpass)	V1 (Vpass)	
Second Portion	WL23	(Vpass)	(Vpass)	V1 (Vpass)	m=24
	WL22	(Vpass)	(Vpass)	V1 (Vpass)	
	WL21	(Vpass)	(Vpass)	V1 (Vpass)	X+2
	WL20	(Vpass)	V3 (Vpass)	V1 (Vpass)	X+1
	WL19	(Vpass)	VPGM	V1 (Vpass)	X=20
	WL18	(Vpass)	V2 (Viso)	V1 (Vpass)	X-1
	WL17	(Vpass)	V1 (Vpass)	V1 (Vpass)	X-2
	WL16	(Vpass)	V1 (Vpass)	V1 (Vpass)	
First Portion	WL15	(Vpass)	V1 (Vpass)	V1 (Vpass)	k=16
	WL14	(Vpass)	V1 (Vpass)	V1 (Vpass)	
	WL13	(Vpass)	V1 (Vpass)	V1 (Vpass)	
	WL12	(Vpass)	V1 (Vpass)	V1 (Vpass)	
	WL11	(Vpass)	V1 (Vpass)	V1 (Vpass)	
	WL10	(Vpass)	V1 (Vpass)	V1 (Vpass)	
	WL9	(Vpass)	V1 (Vpass)	V1 (Vpass)	
	WL8	(Vpass)	V1 (Vpass)	V1 (Vpass)	
	WL7	(Vpass)	V1 (Vpass)	V1 (Vpass)	
	WL6	(Vpass)	V1 (Vpass)	V1 (Vpass)	
	WL5	(Vpass)	V1 (Vpass)	V1 (Vpass)	X+2
	WL4	V3 (Vpass)	V3 (Vpass)	V1 (Vpass)	X+1
WL3	VPGM	V1 (Vpass)	V1 (Vpass)	X=4	
WL2	V2 (Viso)	V1 (Vpass)	V1 (Vpass)	X-1	
WL1	V1 (Vpass)	V1 (Vpass)	V1 (Vpass)	X-2	
WL0	V1 (Vpass)	V1 (Vpass)	V1 (Vpass)		
		VSGS			

Dong, Fig. 5a (modified and annotated)

Reply, 26-31

70

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Motivation to Combine Costa's Teachings with Dong

A. Motivation to Combine Dong and Costa

NAND flash programming is an iterative process involving application of a programming pulse followed by program verification pulses. Dong, Figs. 19 (flow chart) and 20 (showing program and verification pulses); Costa, Fig. 6 (showing program and verification pulses). A POSITA knew that a “disturb free” memory programming operation would require both aspects of the operation (*viz.*, application of the program pulse(s) and verification pulses) to be disturb free. Liu, ¶ 208. A

Petition, 70-74

Motivation to Combine Costa's Teachings with Dong

POSITA would have recognized that both phenomena should be addressed to improve the reliability of flash devices during the iterative programming operation.

Thus, a POSITA would have considered using Dong's techniques with other techniques for a more comprehensive improvement of memory reliability. Liu, ¶¶ 208-209.

Dong and Costa focus on two different (but complementary) phenomena that impact memory device reliability during programming. Dong's teachings focus on

Petition, 70-74

Claim Construction of “Program Operation”

B. “*Program Operation*”

[P]rogram operation should be afforded its plain meaning—*i.e.*, the steps necessary to program a data value. A POSITA would understand this includes two iterative steps: charge injection (sometimes called programming phase) where a programming pulse is applied, and verification (*i.e.*, determining if additional charge is needed). Liu_Reply, ¶¶27-37. Both the intrinsic and extrinsic evidence confirm

Reply, 3

Claim Construction of “Program Operation” Is Not a “New Position”

NAND flash programming is an iterative process involving application of a programming pulse followed by program verification pulses. Dong, Figs. 19 (flow chart) and 20 (showing program and verification pulses); Costa, Fig. 6 (showing program and verification pulses). A POSITA knew that a “disturb free” memory programming operation would require both aspects of the operation (*viz.*, application of the program pulse(s) and verification pulses) to be disturb free. Liu, ¶ 208. A

Petition, 71

Claim Construction of “Program Operation” Is Not a “New Position”

60. During a typical programming operation, the memory cells are programmed according to a wordline programming order as the operation is performed from one end of the string to the other end. NAND memory programming typically involves iteratively repeating two related, but distinct, operations. These operations are applying a programming voltage (sometimes called a “pulse”) to actually programming the memory cell by transferring charge to it to change its threshold voltage. The other phase of a typical programming operation is the verify phase where the memory cell being programmed is read to determine it has been sufficiently programmed (*i.e.*, its threshold voltage has moved to the desired level).

Liu (EX1004), ¶160

The Intrinsic Evidence Supports Petitioner's Construction

In the text, when a word line is said to be programmed, it may mean the word line is used to performed a program operation. A program operation said in the text may be an operation for programming a memory cell formed using, for example, a set of transistors.

'941, 3:6-7
Reply, 4

A “Program Operation” is Not Complete Until the Cell is Programmed

The intrinsic evidence supports Petitioner. The '941 patent states “program operation” refers to “programming a memory cell.” '941, 3:6-7. It was (and is) well-known that flash memory stores values representing logic “1s” and “0s.” Liu_Reply, ¶29. Even if a single pulse injecting *de minimis* charge constituted a *program operation* (per PO’s construction), that does not restrict *program operation* from *also* including programming a memory cell to a desired logic state (Petitioner’s construction). *Id.*, ¶30.

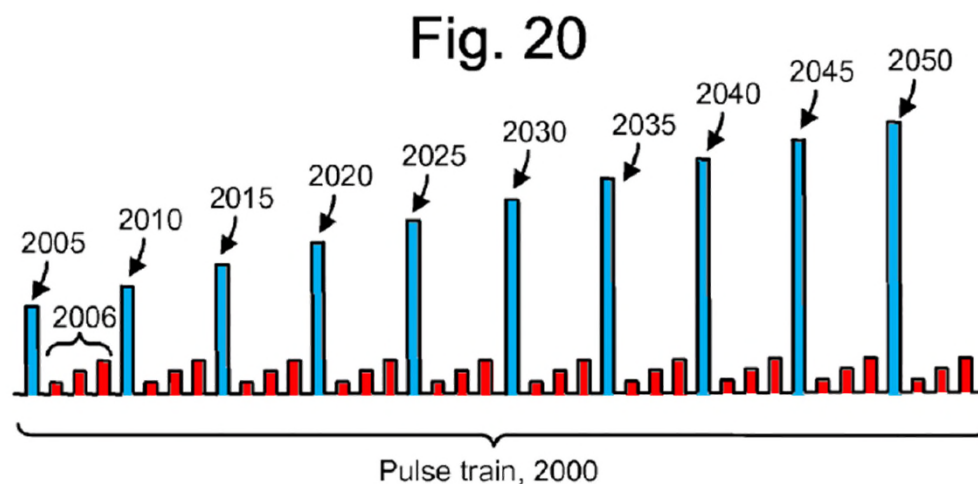
Reply, 4

Claim Construction of “Program Operation” – More Intrinsic Evidence

Claims 8-9 require programming cells in different memory string *portions* (viz., increasing the *first voltage* as programming progresses). Thus, programming advances when the previous *program operation* finishes, which requires both charge injection and verification. Liu_Reply, ¶34. Numerous references (including Dong) confirm this. Dong Fig. 20 shows “pulse train 2000 applied ... *during programming*” includes both charge injection (program) pulses 2005, 2010, etc. *and* “verify pulses 2006.” Dong, [0132].

Reply, 5

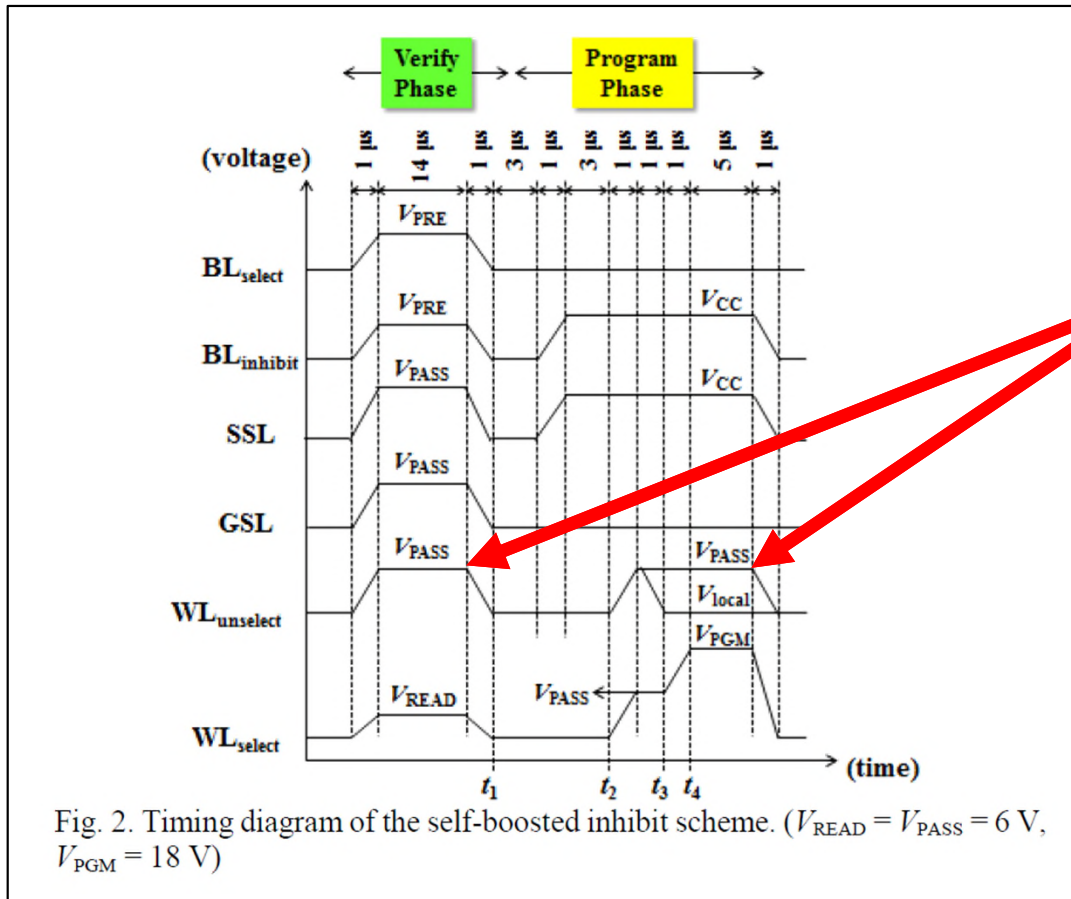
Dong's "Program Operation" Has Both Phases



Dong Fig. 20's "pulse train 2000"—applied to Dong's wordlines "*during programming*"—includes charge injection pulses 2005, 2010, etc. (blue) and "verify pulses 2006" (red). Dong, [0132]. The pulse sequence below programs one cell and constitutes one *program operation*, not ten. Liu_Reply, ¶99.

Dong, Fig. 20 (annotated), [0132]
Reply, 31-32

Patent Owner's Own Exhibit Contradicts Its "First Voltage" Argument



Same "Vpass" voltage level during "Verify Phase" and "Program Phase"

EX2024, 2
Reply, 5

Patent Owner's "First Voltage" Argument Fails

PO erroneously contends that Petitioner “applie[d] Dong’s V_{PASS} —used in a program phase—as the ‘first voltage.’” POR, 64. Even if true, this is irrelevant. V_{pass} is applied both during charge injection (Dong, Fig. 5a) and verification (Costa, Abstract). Even if Dong’s V_{pass} voltage (during charge injection) differed from Costa’s (during verification), nothing in the claim prohibits that (or requires they be the same). What matters is that at any given point during a *program operation*, the specified wordlines (*i.e., the first wordline to an (x-2)th wordline*) have a common *first voltage* applied to them (not that the voltage never change).

Reply, 33

Roadmap

- I. Introduction and IPR Grounds
- II. Overview of the '941 Patent and Prior Art
- III. Ground 1 (Anticipation by Dong) (claims 1, 3, 5-7, 11, 13)
 - Under Petitioner's Bottom-to-Top Construction
 - Under Patent Owner's Bottom-to-Top Construction
- IV. Ground 2 (Obviousness over Dong) (claims 1, 3, 5-7, 11, 13)
 - Under Patent Owner's Bottom-to-Top Construction
- V. Ground 3 (Obviousness over Dong+Costa) (claims 8-9)
 - Program Operation Construction
- VI. Ground 4 (Obviousness over Dong+Shirai) (claims 4, 10, 14)**

Ground 4 – Claims 4, 10, and 14

10. The program method of claim 5, wherein the memory further comprises:

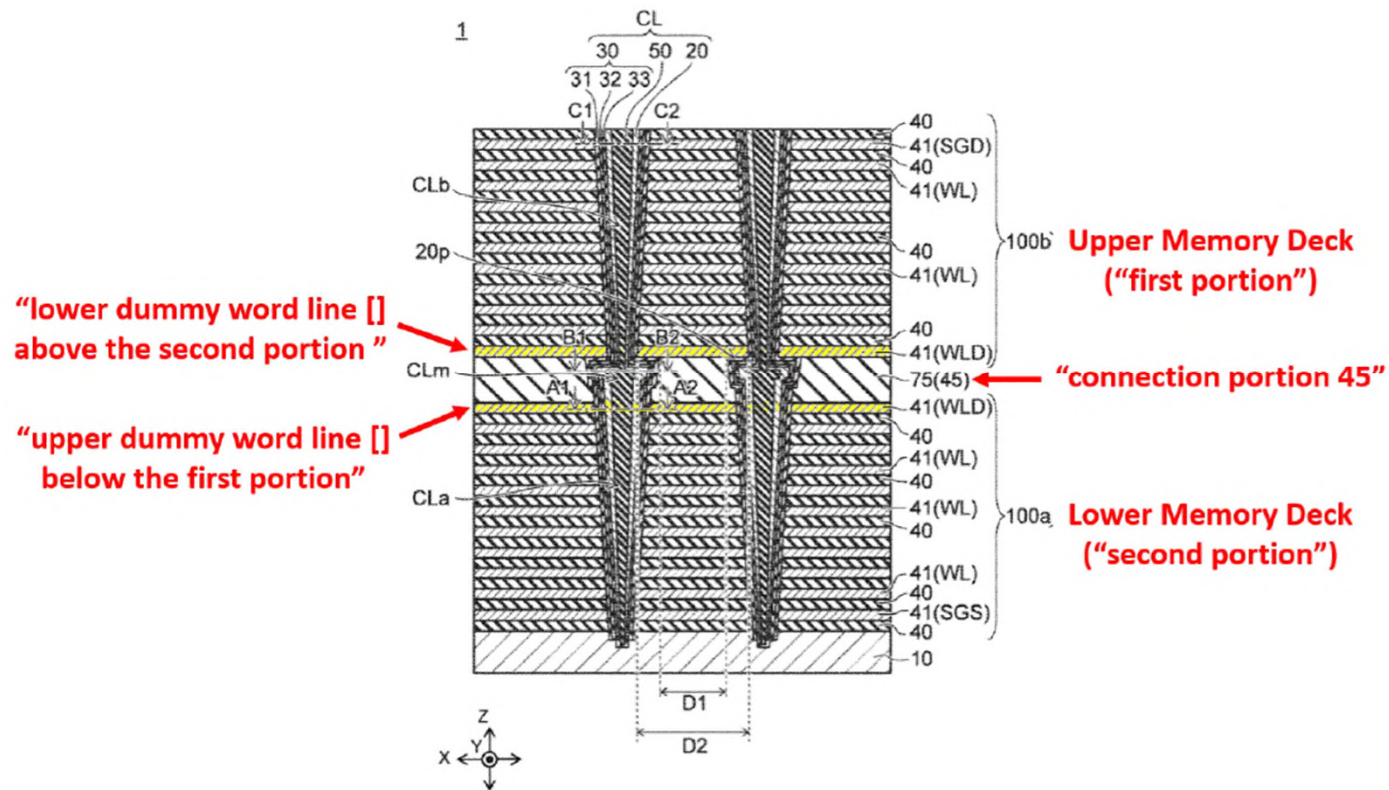
a lower dummy word line formed above the first portion;
an upper dummy word line formed below the second portion;

a joint oxide layer formed between the lower dummy word line and the upper dummy word line;
wherein the memory has a two-deck structure.

*EX1001, claim 10
Petition, xi, 77-84*

Ground 4 – Shirai Reference

FIG. 2



Ex. 1018 (Shirai), Fig. 2 (annotated)
Petition, 27-28, 81

Dr. Khatri Agrees Dong Fig. 5 Does Not Restrict the Number of Wordlines



A. So Figure 5g in its brief description **does not talk about any limit on the number of word lines**, and let me do one more.

*EX1094 (Khatri), 233:16-19
Reply, 35*

Patent Owner’s Ground 4 Counterarguments all Fail

V.	GROUND 4.....	33
A.	PO’s “V_{PASS-LOW}” Arguments Fail (Liu_Reply, ¶¶104-114).....	33
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D.	Dong/Shirai Are Properly Combined.....	38

Reply, i (Table of Contents)

Patent Owner's "Vpass Low" Argument Fails

A. PO's "V_{PASS-LOW}" Arguments Fail (Liu_Reply, ¶¶104-114)

PO's "V_{PASS-LOW}" argument cannot apply to claim 10 because Petitioner's claim 10 analysis relies on Dong Fig. 5a, which lacks "V_{PASS-LOW}." Dong, Fig. 5a; Liu_Reply, ¶104. PO's "V_{PASS-LOW}" arguments for claims 4 and 14 are premised on assertions Petitioner never made, improper bodily incorporation, and non-existent claim limitations. *Intel Corp. v. Pact XPP Schweiz AG*, 2023 U.S. App. LEXIS 4436, at *6 (Fed. Cir., 2023) ("test for obviousness is not ... bodily incorporat[ion]").

Reply, 33-37

Patent Owner's "Vpass Low" Argument Fails (Claims 4 and 14)

		VSGD	
	WL31	(Vpass)	
	WL30	(Vpass)	
	WL29	(Vpass)	
	WL28	(Vpass)	
	WL27	(Vpass)	
	WL26	(Vpass)	
	WL25	(Vpass)	
	WL24	(Vpass)	
	WL23	(Vpass)	
	WL22	(Vpass)	
	WL21	(Vpass)	
	WL20	(Vpass)	
First Portion	WL19	V1 (Vpass)	n=20
	WL18	V1 (Vpass)	
	WL17	V1 (Vpass)	
	WL16	V1 (Vpass)	
	WL15	V1 (Vpass)	
	WL14	V1 (Vpass)	
	WL13	V2 (Vpass-high)	
	WL12	VPGM	
	WL11	V3 (Vpass-high)	
	WL10	V4 (Vpass-medium)	
Second Portion		Dummy Wordline	m=10 k=9
		Connection Portion 45	
		Dummy Wordline	
	WL9	V5 (Vpass-low)	
	WL8	(Vlow)	
	WL7	(Viso)	
	WL6	(Vlow)	
	WL5	(Vpass-low)	
	WL4	(Vpass)	
	WL3	(Vpass)	
	WL2	(Vpass)	
	WL1	(Vpass)	
	WL0	(Vpass)	
		VSGS	

		VSGD	
	WL31	(Vpass)	
	WL30	(Vpass)	
	WL29	(Vpass)	
	WL28	(Vpass)	
	WL27	(Vpass)	
	WL26	(Vpass)	
	WL25	(Vpass)	
	WL24	(Vpass)	
	WL23	(Vpass)	
	WL22	(Vpass)	
	WL21	(Vpass)	
	WL20	(Vpass)	
First Portion	WL19	V1 (Vpass)	n=20
	WL18	V1 (Vpass)	
	WL17	V1 (Vpass)	
	WL16	V1 (Vpass)	
	WL15	V1 (Vpass)	
	WL14	V1 (Vpass)	
	WL13	V2 (Vpass-high)	
	WL12	VPGM	
	WL11	V3 (Vpass-high)	
	WL10	V4 (Vpass-medium)	
Second Portion		Dummy Wordline	m=10 k+1=9 k=8
		Connection Portion 45	
		Dummy Wordline	
	WL9	V5 (Vpass-low)	
	WL8	V5 (Vpass-low)	
	WL7	(Vlow)	
	WL6	(Viso)	
	WL5	(Vlow)	
	WL4	(Vpass-low)	
	WL3	(Vpass)	
	WL2	(Vpass)	
	WL1	(Vpass)	
	WL0	(Vpass)	
		VSGS	

Dong, Fig. 5g (modified and annotated)
Reply, 36

Bodily Incorporation is Not the Test for Obviousness

The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference [W]hether one reference can be incorporated in another is 'basically irrelevant' since the test for obviousness is 'not whether the references could be physically combined but whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole.'

Intel Corp. v. Pact XPP Schweiz AG, 2023 U.S. App. LEXIS 4436, at *6 (Fed. Cir., 2023) (cites omitted)
Reply, 33



Dong Teaches “Gradually Reducing” the Vpass Bias Voltages

[0057] Thus, multiple V_{PASS} voltages can be used at the same time. For example, different V_{PASS} values can be used for the drain and source sides of the NAND string. Further, multiple V_{PASS} voltages can be used at both the drain and source sides. For instance, a higher V_{PASS} , $V_{PASS-HIGH}$, can be used next to the selected word line for programming, as depicted. For the word lines in between the selected word line and the isolation word line, we can have multiple word lines that are biased to different V_{PASS} values, e.g., $V_{PASS-LOW}$, $V_{PASS-MEDIUM}$ and $V_{PASS-HIGH}$. In one implementation, $V_{PGM} > V_{PASS-HIGH} > V_{PASS-MEDIUM} > V_{PASS-LOW} > V_{LOW} > V_{ISO}$. Note that multiple values of V_{LOW} and V_{ISO} are also possible. Generally, all V_{ISO} voltages are less than all V_{LOW} voltages, which in turn are less than all V_{PASS} voltages. By increasing the number of word lines in between the selected word line and the V_{ISO} word line, and by gradually reducing the bias voltage on those word lines, the electric field in between the selected word line and the V_{ISO} word line can be reduced and thus program disturb can be reduced.

*Dong, [0057], [0080]-[0084]
Reply, 36-37*

Patent Owner's Claim 10 Argument is Baseless

B. Ground 4 Renders Claim 10 Unpatentable

PO's argument that Petitioner did not "apply [the] prior art" to claim 10 is disingenuous. POR, 71. Petitioner's statement that claims 10 and 4 are "met for the same reasons" (Pet., 83) plainly referred to the *new limitations* of those claims, not the base claims. PO's suggestion that Petitioner swapped Figs. 5a and 5g is baseless.

Reply, 37

Patent Owner's Strawman "k" Argument Fails

C. PO's Strawman "*k*" Argument (Liu_Reply, ¶¶115-118)

PO argues Ground 4 fails because it uses "different interpretation[s]" of *k* for the dependent claims. POR, 71-73. This argument misreads the Petition and relies on the same false premise (debunked in §§IV.A, V.A) that Petitioner's independent claim analysis was limited to one specific example. Liu_Reply, ¶115. Requiring Petitioner to provide *k*, *m*, and *x* values when the '941 patent does not would create a double standard. *In re Paulsen*, 30 F.3d 1475, 1481 n.9 (Fed. Cir. 1994).

Reply, 37-38

Patent Owner's Strawman "k" Argument Fails

Regardless, the §V.A example above for claims 4 and 14 where $k=9$ debunks PO's argument that Petitioner mixed-and-matched different k values (*i.e.*, "k equals 9" for base claims 1 and 11 and "k equal to 0" for dependent claims 4 and 14). POR, 71; Liu_Reply, ¶116. Further, in the example above for claims for 4 and 14 where $k=8$ (with $V_{\text{PASS-LOW}}$ applied to WL8), carrying that analysis back to the underlying independent claims 1 and 11 works just fine. Liu_Reply, ¶¶117-118. The same rationale explained for claims 4 and 14 defeats PO's substantially similar mix-and-match argument for claim 10. *Id.*; POR, 71-72.

Reply, 37-38

A POSITA Would Have Been Motivated to Apply Shirai's Teachings to Dong

A. Motivation to Combine Dong and Shirai

A POSITA would have been motivated to combine Shirai's teaching of a multiple deck memory structure with Dong for manufacturing purposes to improve yield. Liu, ¶¶ 223-228. Dong discloses its "array of storage elements can be three dimensional." Dong, [0095]. Dong teaches its memory strings are "not limited to any particular number of memory cells," and it was well-known that 3D NAND strings often exceed 100 cells by the Priority Date. Lutze, 2:11-18; *see* §X.A (discussing long memory strings); Liu, ¶ 224. The reason for this was the relentless demand for increased memory capacity at lower cost per bit, which was largely achieved by longer 3D NAND memory strings. Ex. 1009, 292-295; Liu, ¶¶ 223, 49-52.

Petition, 77-80

Patent Owner's MTC Argument Just Repackages Its Flawed "3D" Argument

D. Dong/Shirai Are Properly Combined

PO's argument against combining Dong/Shirai (POR, 73) fails because: (1) it depends on the false premise that Dong "does not disclose vertical 3D-NAND" (POR, 73), which §III.B.1 explains is incorrect; and (2) even if Dong did not disclose 3D-NAND, Dong's techniques for reducing program disturb (*viz.*, PGM and X-mode) apply equally to 3D-NAND (Pet., 12-15, 77-80; §III.B.2.b).

Reply, 38
Petition, 77-80

“Bottom to Top” Claim Construction

Claim Construction of “Bottom To Top”

A. “*Bottom-to-top*” (Liu_Reply, ¶¶5-26)

The claims generically recite *a memory*, which the parties agree covers 3D memories with vertical memory strings. The parties dispute whether the claims are *limited to* vertical 3D memory strings. POR, 12-29. Petitioner says no; PO says yes. Liu_Reply, ¶¶5-6. While Petitioner is correct, Petitioner prevails under either interpretation (§III.A-B), so no construction is necessary.

Reply, 2

The Claim Language

5. A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first word line to a k th word line from bottom to top, the second portion formed above the first portion and comprising a $(k+1)$ th word line to an m th word line from bottom to top, the program method comprising:

applying a first voltage to the to the first word line to an $(x-2)$ th word line when an x th word line is used to perform a program operation;

applying a second voltage to an $(x-1)$ th word line; and
applying a third voltage to an $(x+1)$ th word line;

wherein x , k and m are positive integers, $1 < k < m$ and $3 \leq x$.

EX1001, cl. 5

The Claims Establish Relative Reference Points for Programming

The claims recite *bottom-to-top* to establish a reference scheme (using variables *x*, *k*, *m*, etc.) for identifying wordline groups (called *portions*) for applying voltages, not to require a physical memory string architecture. EX1094, 174:24-175:10; Liu_Reply, ¶¶13, 15. The *above* and *below* claim language simply reflects relative locations in a memory string *already indexed from bottom-to-top*. *Id.*, ¶¶7-11, 14.

Reply, 2

Dr. Khatri Agrees the Figures Provide a Reference/Indexing Scheme



So the purpose of this is to describe the word lines and their -- you know, their numerals of their variable names and their relative orientations, right. WL1 through WLk is from bottom to top and WL(k+1) through WLn is from bottom to top. So that's the purpose of the -- that's the purpose of this figure because the figure is -- you know, I mean, the patent is interested in the voltages you would apply to the word lines.

*EX1094 (Khatri), 174:24-175:10
Reply, 2, 13*

What is the Reference Point – the Substrate or the Memory String Source

PO contends Petitioner's construction fails because the '941 specification (and claims) make "no reference" to "source or drain." POR, 15-16. But neither do they mention the "substrate" that PO's construction requires. Liu_Reply, ¶12. Numerous references confirm Petition's source-to-drain construction. *Id.*, ¶¶24-26; EX1082, 1:59-63; EX1083, 3:25-33; EX1084, Fig. 1D EX1085, 121:41-46; EX1086, [0018].

Reply, 2

Patent Owner's Dictionary Confirms Application to Horizontal 2D Planes

bot·tom (böt'əm) *n.* 1. The deepest or lowest part: *the bottom of a well; the bottom of the page.* 2. The part closest to a reference point: *was positioned at the bottom of the key for a rebound.* 3. The underside: *scraped the bottom of the car on a rock.* 4. The supporting part; the base. 5. The far end or part: *at the bottom of the bed.* 6a. The last place, as on a list.

tion of footsie, diminutive of FOOT.
top¹ (töp) *n.* 1. The uppermost part, point, surface, or end: *wrote on the top of the box.* 2. The part farthest from a given reference point: *took a jump shot from the top of the key.* 3. The crown of the head: *from top to bottom.* 4. The part of a plant, such as a rutabaga, that is above the ground.

EX2014, 3-4
Liu_Reply (EX1089), ¶11

Case Law Citations and Discussion

Patent Owner's Cases are Inapposite

While those elements must be “arranged or combined in the same way as in the claim,” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1370 (Fed. Cir. 2008), ***the reference need not satisfy an ipsissimis verbis test, In re Bond***, 910 F.2d 831, 832-33 (Fed. Cir. 1990).

In re Gleave, 560 F.3d 1331, 1334 (Fed. Cir. 2009)
Reply, 13



Patent Owner's Myopic View of the Art Fails as a Matter of Law

We think that the knowledge which the references evidence was in the hands of one of ordinary skill in the art at the time appellants' invention was made is sufficient to establish - at least prima facie - that ***the claimed subject matter as a whole would have been obvious at that time.***

In re Snow, 471 F.2d 1400, 1403 (C.C.P.A. 2009)
Reply, 24



The Existence of Alternative Approaches Does Not “Teach Away”

But “mere disclosure of alternative designs does not teach away.” *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). Rather, teaching away requires “clear discouragement” from implementing a technical feature.

Univ. of Md. Biotechnology Inst. v. Presens Precision Sensing GmbH, 711 F. App'x 1007, 1011 (Fed. Cir. 2017)
Reply, 32



Dong is Prior Art “For All That It Teaches”

But a reference is prior art for all that it teaches, including less preferred embodiments [and even a “passing mention” suffices]. See *In re Inland Steel Co.*, 265 F.3d 1354, 1361 (Fed. Cir. 2001) (explaining that all disclosures of the prior art, including unpreferred embodiments, must be considered); see also *Beckman Instruments, Inc. v. LKB Produkter AB*, 892 F.2d 1547, 1551 (Fed. Cir. 1989) (“Even if a reference discloses an inoperative device, it is prior art for all that it teaches.” (citation omitted)).

Guardant Health, Inc. v. Univ. of Wash., 2026 U.S. App. LEXIS 1651, at *18-20 (Fed. Cir. 2026)
Reply, 8



Dong Need Not Illustrate Vertical Memory Strings

Finally, appellants point out that neither the Bitzer parent application nor the Bitzer patent shows a drawing of the presently claimed subject matter. However, **a drawing is not required**; also, the reference must be evaluated for all it teaches and is not limited to its specific embodiments. ... In view of the foregoing, **we hold that the Bitzer patent anticipates appellants' claimed invention.**

In re Bode, 550 F.2d 656, 661 (C.C.P.A. 1977)
Reply, 14



Patent Owner Applies a Double Standard re Disclosure

[T]he Board's observation that appellant did not provide the type of detail in his specification that he now argues is necessary in prior art references supports the Board's finding that [a POSITA] would have known how to implement the features of the references and would have concluded that the reference disclosures would have been enabling.

In re Epstein, 32 F.3d 1559, 1568 (Fed. Cir. 1994)
Reply, 26



Patent Owner Applies a Double Standard re Disclosure

We also note that under the enablement standard that AST would have us apply to Yokoyama, the '456 patent itself would be non-enabling. The '456 patent similarly relies on the knowledge and skill of those skilled in the art. If detailed disclosure regarding implementation of known electronic and mechanical components necessary to build a computer were essential for an anticipating reference, then the disclosure in the '456 patent would also fail to satisfy the enablement requirement.

In re Paulsen, 30 F.3d 1475, 1481 n.9 (Fed. Cir. 1994)
Reply, 37



A POSITA Need Only “Envisage” the Limitation for Anticipation

[A] reference can anticipate a claim even if it “d[oes] not expressly spell out” all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would “at once envisage” the claimed arrangement or combination. In re Petering, 301 F.2d 676, 681, 49 C.C.P.A. 993, 1962 Dec. Comm'r Pat. 232 (C.C.P.A. 1962).

*Kennametal, Inc. v. Ingersoll Cutting Tool Co., 780 F.3d 1376, 1381 (Fed. Cir. 2015)
Reply, 11*



Wasica Is Easily Distinguished—Dong Discloses “Three Dimensional” Memory, Not Any Generic “Memory”

To be sure, we have recognized instances where a prior art genus may anticipate a later species For example, we have explained that a disclosed genus may anticipate a claimed species when the genus is so small that one of ordinary skill in the art would “at once envisage each member of this limited class.”

Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc., 853 F.3d 1272, 1284-1286 (Fed Cir. 2017)
Reply, 11



Nidec Is Easily Distinguished: Dong Does Not “Assume” Disclosure of a “Missing” Claim Element–Dong Discloses “Three Dimensional” Memory

The Board held that anticipation can be found even when a prior art reference fails to disclose a claim element so long as a skilled artisan reading the reference would “at once envisage” the claimed arrangement. ... The Board’s misapplication of Kennametal **improperly assumed disclosure of a claim element.**

Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co., 851 F.3d 1270, 1274-75 (Fed. Cir. 2017)
Sur-reply, 10



Net MoneyIN Is Easily Distinguished: Dong's "Three Dimensional" Disclosure is Clearly Linked to the Memory in Figs. 5a and 5g

[T]he district court *[improperly]* “**treated the claims as mere catalogs of separate parts**, in disregard of the part-to-part relationships set forth in the claims ... [and] it “**disclose[d] an entirely different device**, composed of parts distinct from those of the claimed invention ... [B]ecause there was **no link between that figure and the general discussion** of hydrazine as a deoxygenating agent.

Net MoneyIN, Inc. v. Verisign, Inc., 545 F.3d 1359, 1369-71 (Fed. Cir. 2008)
Reply, 11



POSITA Knowledge Must Be Considered

Regardless of the tribunal, the inquiry into whether any 'differences' between the invention and the prior art would have rendered the invention obvious to a skilled artisan necessarily depends on such artisan's knowledge. [] In other words, the assessment of a claim's patentability is inextricably tied to a skilled artisan's knowledge and skill level.

Qualcomm Inc. v. Apple Inc., 24 F.4th 1367, 1376 (Fed. Cir. 2022) (internal cites omitted)
Reply, 11



POSITA Knowledge Must Be Considered

The examiner, however, extensively reviewed the record and found person of ordinary skill would have known how to introduce the “TRANSLATED” instruction to meet the generating and representing steps. J.A. 31—32. Oracle fails to provide any explanation as to how these findings are not supported by substantial evidence.

Oracle Am., Inc. v. Google, Inc., 606 F. App'x 990, 995 (Fed. Cir. 2015)
Reply, 25



Petitioner May Respond Under Patent Owner's Construction in Reply

[T]he petitioner must be afforded a reasonable opportunity in reply to present argument and evidence under that new construction.

Axonics, Inc. v. Medtronic, Inc., 75 F.4th 1374, 1383 (Fed. Cir. 2023)
Reply, 7



THANK YOU