

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES CO., LTD.,
Patent Owner.

IPR2025-00190
Patent 11,568,941 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318; 37 C.F.R. § 42.64

I. INTRODUCTION

We have jurisdiction to conduct this *inter partes* review under 35 U.S.C. § 6, and issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner, Micron Technology, Inc., does not show by a preponderance of the evidence that claims 1, 3–11, 13, and 14 (the “challenged claims”) of U.S. Patent No. 11,568,941 B2 (“the ’941 patent,” Ex. 1001) are unpatentable.

A. *Procedural History*

Petitioner filed a petition for *inter partes* review of claims 1, 3–11, 13, and 14 of the ’941 patent. Paper 1 (“Pet.” or “Petition”). Patent Owner, Yangtze Memory Technologies Co., Ltd., filed a preliminary response. Paper 11. Per the bifurcation process, Patent Owner filed a Brief on Discretionary Denial (Paper 10) to which Petitioner filed an Opposition (Paper 18). The Director denied Patent Owner’s request for discretionary denial. Paper 21.

On July 24, 2025, we instituted an *inter partes* review of all of the challenged claims based on all of the grounds identified in the Petition. Paper 22 (“Inst. Dec.” or “Institution Decision”). Patent Owner filed a Response to the Petition (Paper 33, “PO Resp.”), Petitioner filed a Reply (Paper 39, “Reply”), and Patent Owner filed a Sur-reply (Paper 45, “Sur-reply”). An oral hearing for this proceeding was held on April 28, 2026, and a transcript of the hearing is part of the record.

B. Real Parties in Interest

Petitioner identifies itself (Micron Technology, Inc.) “and its subsidiaries, including Micron Consumer Products Group LLC” as real parties in interest. Pet. 4.

Patent Owner identifies itself (Yangtze Memory Technologies Co., Ltd.) as the real party in interest. Paper 4 (Patent Owner’s Mandatory Notices), 1.

C. Related Matters

The parties identify *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group*, No. 3:24-cv-04223 (N.D. Cal.), which was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, No. 3:23-cv-05792-RFL (N.D. Cal.) as related matters. Pet. 5; Paper 6, 1 (Petitioner’s Updated Mandatory Notice); Paper 4 (Patent Owner’s Mandatory Notice), 1.

Petitioner also identifies twenty-three IPR proceedings that challenge patents that Patent Owner asserted in the District Court Litigation. Pet. 5–6.

D. The ’941 Patent (Ex. 1001)

The ’941 patent, titled “Memory Including a Plurality of Portions and Used for Reducing Program Disturbance and Program Method Thereof,” states that it provides a solution for reducing program disturbance and pass voltage disturbance when opening a three-dimensional (3D) memory. *See* Ex. 1001, codes (54), (57), 1:39–41. The patent explains that by “using a memory sectioned to have a plurality of portions and applying voltages to the word lines of the memory according to the portions, program disturbance and pass voltage disturbance may be reduced.” *Id.* at 6:39–43.

Figure 1 of the '941 patent is reproduced below.

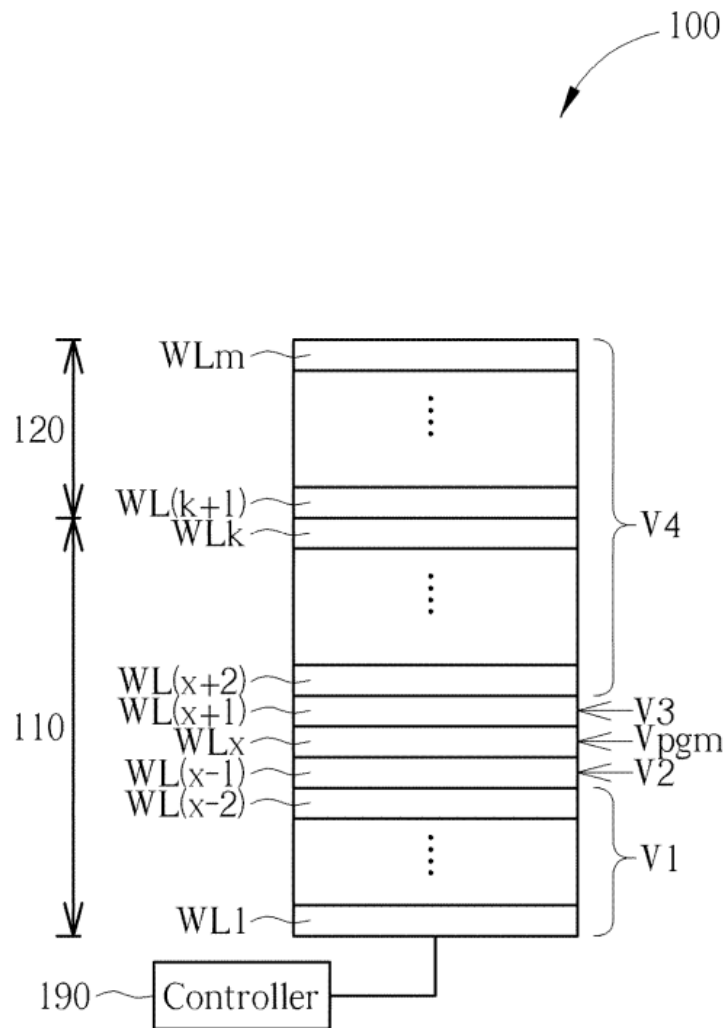


FIG. 1

Figure 1 illustrates memory 100 having first portion 110, second portion 120, and controller 190. *Id.* at 2:64–65. First portion 110 includes first word line (WL1) to kth word line (WLk) from bottom to top; second portion 120, formed above first portion 110, includes a (k+1)th word line WL(k+1) to an mth word line WLM from bottom to top. *Id.* at 2:63–3:3.

The '941 patent states that Figure 1 shows that when an xth wordline WLx is used to perform a program operation, controller 190 applies a program voltage Vpgm to the xth word line WLx. *Id.* at 3:9–11. Controller

190 can also apply voltages to other word lines, such as a first voltage V1 to first word line WL1 to an (x-2)th word line WL(x-2), a second voltage V2 to an (x-1)th word line WL(x-1), and a third voltage V3 to an (x+1)th word line WL(x+1), when k is greater than 1 and less than m and x is greater than or equal to 3. *Id.* at 3:11–17. Additionally, controller 190 can apply a fourth voltage V4 to an (x+2)th word line WL(x+2) to the mth word line WLM when the xth word line WLx is used to perform the program operation and $x < m-1$. *Id.* at 3:18–21.

The '941 patent also discloses additional embodiments in which different voltages are applied to different word lines. *See, e.g., id.* at 1:45–2:27, 3:26–4:61.

E. The Challenged Claims

Petitioner challenges claims 1–3, 5–11, 13, and 14 of the '941 patent. Pet. 7. Claims 1, 5, and 11 are independent. Claims 1 and 5, with Petitioner's bracketed material added, are illustrative of the claimed subject matter and are reproduced below.

[1.PRE] A memory comprising:

[1.A] a first portion comprising an (m+1)th wordline to an nth wordline from bottom to top; and

[1.B] a second portion formed below the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top; and

[1.C] a controller configured to apply

[1.D] a first voltage to an (x+2)th wordline to the nth wordline,

[1.E] a second voltage to an (x+1)th wordline,

[1.F] a third voltage to an (x–1)th wordline,

[1.G] a fourth voltage to the (m+1)th wordline to an (x–2)th wordline, and

[1.H] a fifth voltage to the (k+1)th wordline to the mth wordline when an xth wordline is used to perform a program operation;

[1.I] wherein x, k and m are integers, $0 \leq k < m$, $(m+2) < x < (n-1)$, and the fifth voltage is lower than the fourth voltage.

Ex. 1001, 6:55–7:2; Pet. viii.

[5.PRE] A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first wordline to a kth wordline from bottom to top, the second portion formed above the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top, the program method comprising:

[5.A] applying a first voltage to the to the [sic] first wordline to an (x–2)th wordline when an xth wordline is used to perform a program operation;

[5.B] applying a second voltage to an (x–1)th wordline; and

[5.C] applying a third voltage to an (x+1)th wordline;

[5.D] wherein x, k and m are positive integers, $1 < k < m$ and $3 \leq x$.

Ex. 1001, 7:23–34; Pet. ix.

F. Asserted Grounds of Unpatentability

Petitioner contends claims 1–3–11, 13, and 14 are unpatentable on the following grounds.

Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1, 3, 5–7, 11, 13	102(a)(1) 102(a)(2)	Dong ²

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102, 103. The earliest claimed priority date for the ’941 patent is after the effective date of the applicable AIA amendment. *See* Ex. 1001, (60). Thus, we refer to the AIA version of 35 U.S.C. §§ 102, 103.

² Dong, US Pub. 2008/0279008 (filed May 7, 2008, published Nov. 13, 2008) (Ex. 1005, “Dong”).

Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1, 3, 5–7, 11, 13	103(a)	Dong
8, 9	103(a)	Dong, Costa ³
4, 10, 14	103(a)	Dong, Shirai ⁴

Pet. 7.

In support of its unpatentability arguments, Petitioner relies on a declaration (“Liu Dec.”, Ex. 1004) and a reply declaration (“Liu Reply Dec.”, Ex. 1089) of David Kuan-Yi Liu, Ph.D. Patent Owner relies on a declaration of Sunil P. Khatri, Ph.D. (Ex. 2028). Transcripts of the Depositions of Drs. Liu (Ex. 2021, 2030) and Dr. Khatri (Ex. 1094) have been entered into the record.

II. ANALYSIS

A. *Legal Standards*

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the

³ Costa, US 2018/0012667 A1 (filed July 7, 2016, published Jan. 11, 2018) (Ex. 1012, “Costa”).

⁴ Shirai, US 2019/024405 A1 (filed Mar. 13, 2019, published July 11, 2019) (Ex. 1018, “Shirai”).

challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

Anticipation under 35 U.S.C. § 102 “requires that every element and limitation of the claim was previously described in a single prior art reference, either expressly or inherently, so as to place a person of ordinary skill in possession of the invention.” *Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1082 (Fed. Cir. 2008); *see also Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) (“[T]he dispositive question regarding anticipation [i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference’s] teaching that every claim element was disclosed in that single reference.”). Anticipation also requires that a reference discloses “all of the limitations arranged or combined in the same way as recited in the claim.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008).

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the [relevant time frame] to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence⁵, objective evidence of

⁵ Neither party submitted evidence of secondary considerations. *See* Pet. 85; PO Resp.

obviousness or nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2016) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)).

A. Level of Ordinary Skill in the Art

In determining whether a claimed invention would have been obvious, we consider the level of ordinary skill at the time of filing. 35 U.S.C. § 103; *see also Graham*, 383 U.S. at 17 (discussing pre-AIA obviousness).

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had a bachelor’s degree in electrical engineering or a similar discipline, along with 2–3 years of professional experience working with (e.g., researching, designing, or teaching) NAND memory devices (including issues relating to the operation, e.g., programming, of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). Pet. 22 (citing Ex. 1004 ¶¶ 40–42). Petitioner also asserts that a POSITA would have been aware of and generally knowledgeable about NAND memory’s structure and fabrication, its component parts, how it operates, and how it is controlled. *Id.* at 22–23 (citing Ex. 1004 ¶ 41).

In the Institution Decision, we adopted the assessment offered by Petitioner, which Patent Owner did not contest. Inst. Dec. 13. Following institution, Patent Owner stated it does not dispute Petitioner’s definition of a POSITA.

PO Resp. 9 (citing Khatri Dec. ¶¶ 42–47). Because Petitioner’s definition of the level of skill in the art appears consistent with the ’941 patent and the asserted prior art, we maintain it for purposes of this Final Written Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir 2001).

B. Claim Construction

We construe the ’941 patent claims using the same claim construction standard that would be used to construe a claim in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (en banc). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

1. Preamble

The preamble of claim 5 recites:

A program method of a memory, the memory comprising a first portion and a second portion, the first portion comprising a first wordline to a kth wordline from bottom to top, the second portion formed above the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top, the program method comprising:

Ex. 1001, 7:23–28.

The preamble of claim 11 recites:

A program method of a memory, the memory comprising a first portion and a second portion formed below the

first portion, the first portion comprising an (m+1)th wordline to an nth wordline from bottom to top, the second portion comprising a (k+1)th wordline to an mth wordline from bottom to top, the program method comprising:

Ex. 1001, 8:15–20.

In our Decision, we treated the preambles of claims 5 and 11 as limiting, noting that these preambles provide antecedent basis for the word line limitations recited in the body of their respective claim. Dec. 14–15, 8. Neither party disputes that the preambles of claims 5 and 11 are limiting. *See* PO Resp. 34–35 (agreeing that the preambles are limiting); *see generally* Reply 1–6 (not disputing that the preambles are limiting). We maintain our construction of the preambles in this Decision.

2. *“from bottom to top”*

Each of the independent claims recite a memory comprising a first portion and a second portion having various word lines “from bottom to top.” Ex. 1001, 6:55–60, 7:23–38, 8:15–20. Claims 1 and 11 state the second memory portion is “formed below” the first portion while claim 5 states the second memory portion is “formed above” the first portion. *Id.*

Petitioner asserts that the claims should be construed according their plain and ordinary meaning and that no further construction is required. Pet. 22. However, in its unpatentability arguments, Petitioner asserts that the claimed first and second portions of memory are “defined by the claim itself” such that first portion comprises a “first wordline to a kth wordline from bottom to top; and the second portion formed above the first portion

and comprising a (k+1)th wordline to an mth wordline from bottom to top.”
Id. at 34 (emphasis omitted).

With respect to the “bottom to top” language, Petitioner further asserts that although the ’941 patent does not define the phrase “bottom to top,” it is “common in NAND flash memory devices to refer to the ‘*source end*’ of a memory string of a NAND flash memory device as the “bottom” and the “*drain end*” as the “top”” and applies that common usage in its Petition. Pet. 35 (citing Ex. 1004 ¶¶ 112–113, 120) (emphasis added). Petitioner thus asserts that the claim term “bottom to top” as understood by a person of ordinary skill in the art means from *source side* of the memory string to *drain side* of the memory string. *See id.* at 34–35. For convenience, we refer to this proposed construction as the “source to drain” construction.

To support the “source to drain” construction, Petitioner’s declarant Dr. Liu points to figures in a text book discussing two-dimensional NAND flash memories showing the source end on the bottom and the drain end on the top and states that this “convention applies irrespective of whether the physical device is in a horizontal or vertical direction.” Ex. 1004 ¶ 113 (citing Ex. 1009, Figs. 2.1, 2.2, 2.4).

The Petition also presents a second construction of from “bottom to top,” stating that “to the extent bottom to top is interpreted to require vertical strings in a 3D NAND memory, Dong still satisfies the claim as “Dong discloses its ‘array of storage elements can be three dimensional’ and shows Fig. 5a in a vertical orientation.” Pet. 35(emphasis omitted). For convenience, we refer to this construction as the “vertically arranged wordlines” construction.

In our Institution Decision, we disagreed with Petitioner’s construction that “bottom” refers to the source end of a memory string and “top” refers to the drain end of the string. Inst. Dec. 16–19. We explained, *inter alia*, that because the plain language of the claims identifies the relative vertical positions of the first and second memory portions to each other (i.e., second memory portion is above the first portion), it follows that the claim terms referring to the top and bottom of wordline within the memory portions also refer to location of the wordlines’ vertical location relative to the memory portions and not to the location of the wordlines relative to the source or drain. Inst. Dec. 17–18.

In its Reply, Petitioner asserts that the bottom to top limitations do not require a physical memory string architecture, but rather establish an indexing reference scheme (using variables x, k, m, etc.) for identifying word line groups (called portions) for applying voltages. Reply 2–3 (citing Ex. 1089 ¶¶ 13, 15; Ex. 1094, 174:24–175:10). Petitioner contends that the “above and below language simply reflects relative locations in a memory string already indexed from bottom to top,” i.e., from source to drain. *Id.* at 2 (emphasis omitted).

Based upon our review of the full record, we maintain our understanding that the claim term “from bottom to top” refers to the vertical arrangement of word lines in the memory portions from bottom to top and not from source end to drain end, as asserted by Petitioner. Inst. Dec. 17. In other words, the claim terms describing the first and second portions having word lines “from top to bottom” refer to the relative vertical location of the word lines within the memory portions and not to location of the word lines relative to the source or drain.

Our construction is based on the plain and ordinary meaning of the express language of the independent claims, which states that the second memory portion is *formed* either *above* or *below* the first memory portion. The forming of one memory portion above or below another portion establishes a top and bottom in relation to those portions.

For example, claim 5 is directed to a “program method of memory” that requires a second portion *formed above* the first portion. A second memory portion that is *formed above* a first memory portion is *on top* relative to the first portion. Similarly, claims 1 and 11, which recite a memory having a second portion *formed below* a first portion, establish that the second portion is on the bottom relative to the first portion.

Thus, the claim language itself establishes the vertical locations of the memory portions relative to each other (e.g., a second memory portion that is above the first portion is on top, relative to the first portion). It follows that claim terms referring to the top and bottom of word lines within the memory portions also refer to relative vertical locations of the word lines within the memory portions.

Thus, we understand the plain and ordinary meaning of claim language referring to first and second memory portions that comprise word lines “from bottom to top” to mean that the word lines of the memory portions are arranged vertically from the lower bottom end of its memory portion toward the upper top of its memory portion (i.e., from bottom to top).

Our understanding that the term “from bottom to top” refers to the vertical arrangement of word lines in the memory portions from lower bottom end of the memory portion toward the upper top part of the memory

portion, and not from source end to drain end, is supported by the '941 patent Specification. The Specification does not refer to source or drain side of the word lines. *See generally* Ex. 1001. Rather, the '941 patent illustrates and describes the figures of its inventive memory devices having word lines arranged physically vertically from the bottom to top. For example, Figures 1–11 each depict “a memory” having vertically arranged word lines. *See id.* at 2:37–55, Figs. 1–11. The Specification describes embodiments with first, second, and/or third memory portions as including various word lines “from bottom to top” and that the memory portions are formed above or below each other, thus supporting that the claim term “from bottom to top” is used according to its plain and ordinary meaning of from bottom to top and not from source side to drain side. *See, e.g., id.* at 1:45–50, 1:55–60, 2:1–7, 2:14–18, 2:64–3:3, 3:46–48, 5:4–9, 5:16–19, 5:25–38.

Moreover, the Specification discusses the location of the word lines in terms of their relative vertical location in the first or second portion of memory, not in terms of their location to the source or drain. For example, the '941 patent explicitly states that the word lines are *located* in either the “*lowermost*” or “*uppermost*” portion of a memory portion. *See, e.g.,* Ex. 1001, 5:10–12 (stating word line WLx of Figure 9 “is *located in the lowermost* portion 920”) (emphasis added), 5:15–19 (stating wordline WLx of Figure 10 is located in the portion 910 *above the lowermost portion* 920), *see also id.* at 5:38–50 (describing the operation of the same memory in different conditions and identifying the word lines as located in “lowermost” or “uppermost” portion of the memory portions); *see also id.* at 5:15–16 (stating the memory of Figure 10 “may have the same *structure*” as shown in Figure 9)(emphasis added). The Specification’s identification of the location

of the word lines in relation to the “lowermost” or “uppermost” memory portions shows that the Specification identifies the location of the word line relative to its structural location in the memory, not to its location relative to a source or drain, i.e., source-to-drain indexing. Thus, the ’941 patent’s description of the word lines as located in the “lowermost” or “uppermost” portion of the memory portions supports our understanding that the term phrase “bottom to top” refers to the vertical arrangement of wordlines in the memory portions from lower bottom end of the memory portion toward the upper top part of the memory portion, and not from source end to drain end.

Additionally, we agree with Patent Owner that other intrinsic evidence, such as U.S. Patent Publication No. 2016/0071595 A1 (“the ’595 Publication,” Ex. 2011), which is cited on the face of the ’941 patent, reaffirms that a POSITA would have interpreted word lines arranged “from bottom to top” to mean from lowest to highest, and not from source to drain. Ex. 2028 ¶ 118. Patent Owner explains, with persuasive supporting testimony by Dr. Khatri, that the ’595 Publication describes a 3D NAND memory stack with “a top 287 and a bottom 238” referring to the respective highest and lowest portions of the memory stack. PO Resp. 18–19 (citing Ex. 2011 ¶¶ 75, 77, Fig. 2C; Khatri Dec. ¶ 118).

Finally, the ’941 patent states that there is a need to reduce program disturbance and pass voltage disturbance when “operating a three-dimensional memory” (Ex. 1001, 1:39–41) and that the invention is related to a “memory including a plurality of portions and used for reducing program disturbance and a program method thereof” (Ex. 1001, 1:19–23). The Specification’s reference to three-dimensional memory and to memory having a plurality of portions is consistent with construction of claim

language referring to memory portions that comprise word lines “from bottom to top” to mean that the word lines are arranged vertically from bottom to top. Indeed, Dr. Liu testified that as of the 2020 filing date of the application giving rise to the ’941 patent, “‘three dimensional’ (3D) memory was practically synonymous with vertical memory strings.” Ex. 1089 ¶ 40; *see also id.* ¶¶ 47, 84.

We considered, but are not persuaded by, Petitioner’s argument and evidence that “from bottom to top” means from source to drain. *See, e.g.*, Pet. 34–35 (citing Ex. 1004 ¶¶ 112–113, 120; Ex. 1005 ¶ 95); Reply Br. 2–3 (citing Ex. 1004 ¶¶ 5–7, 11, 13, 15, 17–26; Exs. 1082–1086). Dr. Liu testifies that “a POSITA would be familiar with the convention that a memory array, consisting of many memory strings, would have the source end of the NAND string at the bottom, and the drain end at the top.” Ex. 1004 ¶ 113 (citing Ex. 1009, 39–40, Figs. 2.1, 2.2, 2.4); *see also id.* ¶ 112 (stating that it was “well-known” that memory string programming typically proceeded, either from source to drain or from drain to source) (citing Ex. 1005 ¶ 89, Fig. 10. Neither Petitioner nor Dr. Liu persuasively explain how the cited extrinsic evidence uses the term “from bottom to top” to refer to “from source to drain.” Nor does Petitioner persuasively explain how figures depicting a source on the bottom end/lower portion of the figure and a drain on the top end/upper portion of the figure, means that the *term* “*from bottom to top*” means from source end to drain end. *See also* Ex. 1009, 39–40, Figs. 2.1, 2.2, 2.4 (not using the terms “bottom” or “top” to refer to source end or drain end).

We are persuaded by Dr. Khatri’s persuasive testimony to the contrary that a POSITA looking at the extrinsic evidence identified by Petitioner

supports a construction of from bottom to top as referring to a physical location of from lowest to highest, and not from source to drain. *See, e.g.*, Ex. 2006 ¶¶ 68–69 (citing Ex. 1009). Dr. Khatri explains that when the reference uses the terms “top” and “bottom,” the reference is describing the vertically highest and vertically lowest physical components of the NAND memory and not as describing locations of the source or drain. *See, e.g., id.* ¶ 68 (citing Ex. 1009, 327 (stating “the charge trap nitride layer is physically connected from top to bottom [control gates] in” a 3D flash memory)).

Petitioner also argues that Patent Owner’s proposed construction requires a “substrate,” which is not recited in either the ’941 patent Specification or its claims. Reply Br. 2. This argument is not persuasive. Even if the ’941 patent does not recite “substrate,” as noted above, the claims and the Specification discuss the physical location of the first and second portions and their wordlines in a vertical direction relative to each other, i.e., in a vertical direction either above or below each other and the wordlines from bottom to top. This establishes a “top” and “bottom” relative to the memory portions and the wordlines contained therein that is not dependent upon a substrate.

Thus, for the foregoing reasons, we construe the claim language referring to first and second memory portions that comprise word lines “from bottom to top” to mean that word lines of the memory portions are arranged vertically from the bottom end of its memory portion toward the top of its memory portion.

We determine that no other terms require construction to resolve the issues in dispute.

C. Asserted Unpatentability of Claims 1, 3, 5–7, 11 and 13 over Dong

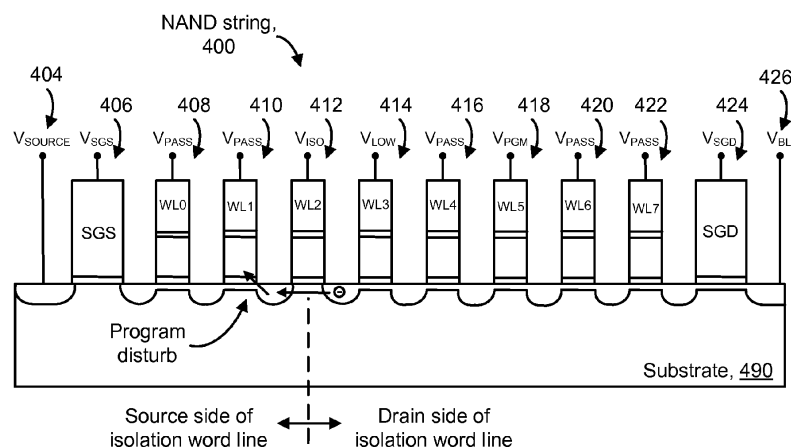
Petitioner contends that independent claims 1, 5, and 11 and dependent claims 3, 6, 7, and 13 are either anticipated by or would have been obvious over Dong. Pet. 28–70; Reply Br. 6–25.

1. Overview of Dong

Dong, titled “Non-volatile Storage with Boosting Using Channel Isolation Switching,” is directed to non-volatile storage “in which program disturb is reduced by preventing source side boosting in selected NAND strings.” Ex. 1006, codes (12), (43), (54), (57). Dong states that “program disturb” occurs when the threshold voltage of an unselected non-volatile storage element is shifted due to the programming of other non-volatile storage elements. *Id.* ¶ 11.

Dong Figure 4, reproduced below, depicts a cross-sectional view of a 2D NAND string showing a program disturb mechanism. *Id.* ¶ 19.

Fig. 4

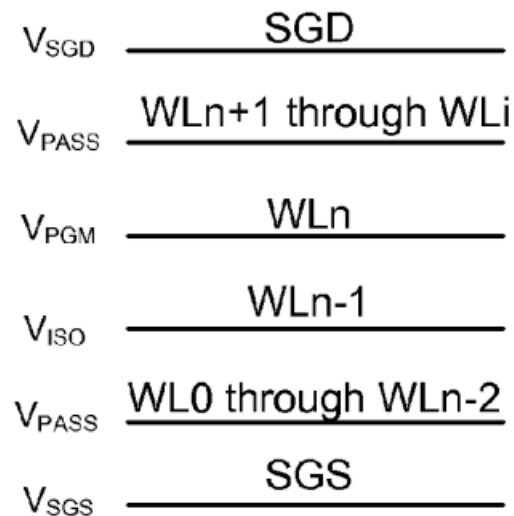


Dong Figure 4 depicts a cross-sectional view of a NAND string showing a program disturb mechanism. *Id.* ¶¶ 19, 45.

The 2D NAND string includes a source side select gate 406, a drain side select gate 424, eight storage elements (408, 410, 412, 414, 416, 418, 420, 422) formed on substrate 490, source supply line 404, and bit line 426. *Id.* ¶ 45.

Dong Figures 5a (reproduced below) through 5h depict different examples of self-boosting modes. *Id.* ¶¶ 20, 47.

Fig. 5a



Dong Figure 5a above depicts an example of a self-boosting mode. *Id.* ¶ 49.

In the self-boosting mode example shown in Figure 5a, various voltages (V_{PASS} , V_{PGM} , V_{ISO} , V_{SGS} , V_{SGD}) are applied to the word lines (WL0–WLi) and gate control lines (SGS, SGD). *Id.* ¶ 49. More

particularly, the voltage VSGS is applied to the source-side selected gate control line SGS; a pass voltage VPASS is applied to each of the unselected word lines, WL0 through WLn-2 and WLn+1 through WLi; a program voltage VPGM is applied to the selected word line WLn; isolation voltage VISO is applied to WLn-1, the word line which is adjacent to the selected word line on the source side; and VSGD is applied via the drain-side select gate control line SGD. *Id.* ¶ 49. These voltages are used during the drain side boosting, which occurs after source side boosting. *Id.* ¶ 47.

2. *Asserted Unpatentability of Independent Claim 5*⁶

The parties focus their arguments on, *inter alia*, whether the first and second portions of Dong discloses or suggests wordlines that are arranged from bottom to top as required by each of the independent claims. Claim 5 recites:

“program method of a memory, the memory having a first portion and a second portion, wherein

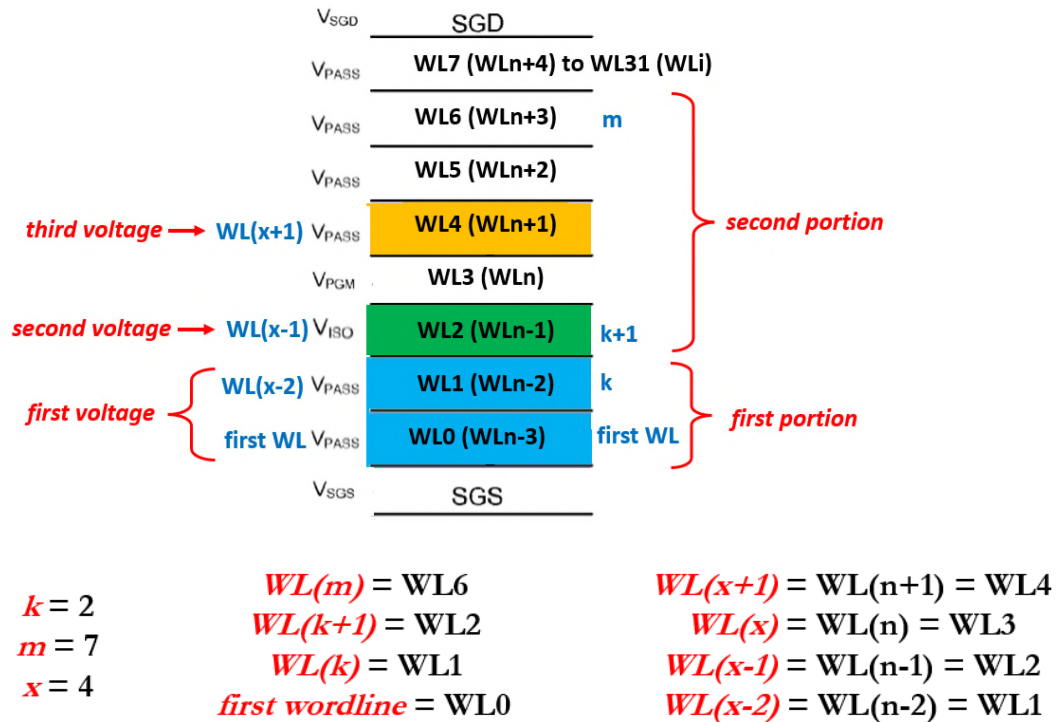
the first portion comprising a first wordline to a kth wordline from bottom to top, the second portion formed above the first portion and comprising a (k+1)th wordline to an mth wordline from bottom to top”

Petitioner maps Dong Figure 5a to claim 5. To support its contentions, Petitioner provides a color annotated, modified version of Dong Figure 5a (top) and a chart (bottom), reproduced below, to show how Petitioner maps the word lines, portions, and voltages of Dong Figure 5a to

⁶ We address the independent claims in the same order as set forth in the Petition.

claim 5 in a 32-cell memory string having 32 word lines (i.e., word lines W0 through WL31). Pet. 32–33 (citing Ex. 1004 ¶ 115; Ex. 1005, Fig. 5a).

Fig. 5a



Petitioner’s modified Dong Figure 5a above depicts an example of self-boosting mode in which various voltages (V_{PASS} , V_{PGM} , V_{ISO} , V_{SGS} , V_{SGD}) are applied to the wordlines (WL0–WL32) and gate control lines (SGS, SGD) of a 32-cell memory. Pet. 33; Ex. 1005 ¶ 49.

(a) Asserted Anticipation or Obviousness under a “from Source to Drain” Construction

Petitioner states Dong either anticipates or renders claim 5 obvious under its “from source to drain” construction. See Pet. 29–38; Reply 6–7. In particular, Petitioner asserts that Dong discloses 3D memory strings, and, as

described in Figures 5a–h, the *source-side select gate control line is SGS* and the *drain-side select gate control line is SGD* and programming proceeds from source to drain. Reply 6–7 (citing Ex. 1005 ¶ 48); Pet. 29–30, 37 (citing Ex. 1005 ¶ 48, Fig. 5a). Petitioner asserts that Dong’s wordlines WL0 through WLn-2 (*viz.*, WL1) correspond to the claimed first portion, and that wordlines WL2 to WL6 corresponds to the claimed second portion; Petitioner further states that within Dong’s first portion, wordline WL0 corresponds to the claimed first wordline from bottom to top and that wordline WLn-2 (*viz.*, WL1) corresponds to the claimed kth wordline; that within the second portion, Dong’s wordline WLn-1 (*viz.*, WL2) corresponds to the claimed (k+1)th wordline and WLn+3 (*viz.* WL6) corresponds to the mth wordline. Pet. 36–38 (citing Ex. 1004 ¶¶ 107, 127, 127, Fig. 5a).

Petitioner further states that “as is apparent from Fig. 5a, Dong’s second portion (from WL2 to WL6) is *formed above the first portion* (WL0 to WLn-2).” Pet. 38; *see also* Ex. 1004 ¶ 127 (same).

This argument is not persuasive because it relies on Petitioner’s proposed construction of “from bottom to top” as meaning from source end to drain end, which we did not adopt. Pet. 34–35 (citing Ex. 1004 ¶¶ 112–113, 120). As noted above, we determine that the term “from bottom to top” refers to the vertical arrangement of word lines in the memory portions from lower bottom end of the memory portion toward the upper top part of the memory portion, and not from source end to drain end.

(b) Asserted Anticipation or Obviousness Under a
“Vertically Arranged Wordlines” Construction

Petitioner also asserts that Dong discloses or teaches claim 5 under the “vertically arranged wordlines” construction. See e.g., Reply 7–16; Pet. 29–38. Petitioner asserts that “to the extent bottom to top is interpreted to require vertically arranged strings in a 3D NAND memory, Dong discloses its ‘array of storage elements can be three dimensional’ and shows Fig. 5a in a vertical orientation which satisfies the claim.” Pet. 35 (citing Ex. 1005 ¶ 95; Ex. 1004 ¶ 120).

We disagree and find that Dong’s Figure 5a does not depict wordlines in a physical vertical orientation, but rather depicts voltage diagrams. We agree with Patent Owner’s argument, supported by persuasive testimony by Dr. Khatri, that a POSITA would have understood that Dong’s voltage charts (e.g., Fig. 5a) simply represent which voltages are applied to which word lines and do not depict the physical orientation of the wordlines. *See, e.g.*, Ex. 2028 ¶ 171 (citing Ex. 1005 ¶ 20; Ex. 1009 ¶¶ 52–54). As Dr. Khatri explains, Dong Figures 5a–5h depict different examples of self-boosting modes showing voltages applied differently to the wordlines and are not intended to depict the physical orientation of these word lines. Ex. 2028 ¶ 171; *see also* Sur-reply 11–12 (citing Ex. 1005 ¶¶ 47, 65, 63–67; Ex. 2028 ¶¶ 177–186). We agree with Dr. Kahtri’s persuasive testimony that a POSITA would understand that Figures 5a–5h are illustrated vertically, but do not represent the actual physical arrangement of the word lines in memory, which are shown to be horizontal in Dong’s Figure 4. *See, e.g.*, Ex. 2028 ¶ 172 (citing Ex. 1005 ¶¶ 20, 45, 47, 87).

Petitioner argues that Dong's voltage diagrams "are precisely the types of voltage diagrams" depicted in the '941 patent. Reply 12–13 (comparing Dong Fig. 5a *with* Ex. 1001, Fig. 8). Petitioner further asserts that the '941 patent figures "exist to establish an indexing scheme and provide voltage mappings (like Dong's Figures 5a/5g)." *Id.* at 13. Petitioner also asserts that Dong would be substantively no different if Figure 5a included a generic memory label, and that the '941 patent would not change by labelling its figures as a "programming approach for a memory" instead of a memory. *Id.* at 13–14.

Significantly, however, the '941 patent explicitly states that Figure 8 depicts the physical structure of a memory, not program modes, as stated in Dong. *See* Ex. 1001, 2:37–55 (stating that the Figures "illustrate a memory"). The '941 patent explains that Figure 8 illustrates a memory that includes a "first portion 710," a "second portion 720," and a controller 190, that the second portion is formed below the first portion, and that the first and second portions contain wordlines "from bottom to top." Ex. 1001, 4:29–36. In contrast, Dong states that its Figure 4 depicts memory and Figures 5a–5h depict self-boosting modes, not physical structures. Ex. 1005 ¶¶ 19, 20. Thus, Dong's Figures 5a–5h do not disclose vertical wordlines any more than circuit diagrams of 2D NAND flash memory that symbolically illustrate wordlines arranged in a vertical manner, but do not represent physical structure. Sur-reply 12–13 (citing Ex. 1009, 39 (Fig. 2.2); Ex. 1004 ¶ 113; PO Resp. 23–26).

As such, Petitioner has not persuasively shown that there is no substantive difference between figures depicting structures and figures depicting voltage charts. We agree with Patent Owner that the '941 patent

explicitly explains that its figures depict a physical memory whereas Dong does not. *See, e.g.*, Sur-reply 12 (citing Ex. 1001, 2:48–49, 4:29–49, 4:29–47, 5:16–21, 5:25–28, Figs. 7–8). The fact one figure may depict a structure as well as voltage mapping does not mean that that the figure is substantively no different from another figure that depicts voltage mapping but not any physical structure.

Thus, we determine that Dong’s voltage charts (i.e., Figs. 5a–5h) do not disclose the physical, vertical arrangement of wordlines, and thus do not disclose wordlines arranged from bottom to top as required by claim 5. Ex. 2028 ¶ 176.

We recognize that Dong states that in “some embodiments, the array of storage elements can be three dimensional.” Dong ¶ 95. Petitioner, however, has not sufficiently shown that a POSITA would have understood, from this sentence, that Dong’s program disturb methods could be applied to vertical strings having a first portion located above or below a second portion and wordlines arranged from bottom to top.

In its Reply, Petitioner asserts that a POSITA, reading Dong in 2020, “would readily envisage 3D memory.” Reply 8 (citing Ex. 1086 ¶¶ 38–56), *see also id.* at 11 (stating given the “well-developed state of 3D memory in 2020, a POSITA would ‘at once envisage’ the ’941 patent’s claimed *bottom-to-top* wordline arrangement upon reading Dong’s ‘three dimensional’ NAND disclosure) (emphasis altered). Petitioner states that a skilled artisan would have been aware and knowledgeable about NAND memory structure and fabrication, and that 3D-NAND structures “could be conceived” by starting from the 2D-NAND string building block and turning the string upside, resulting in a 3D structure with a vertical channel. Reply 9–10; Pet.

12–13, 22–23. Petitioner further asserts that, given the prevalent and well developed state of 3D memory in 2020, a skilled artisan would “at once envisage” the claimed bottom to top wordline arrangement upon reading Dong’s “three dimensional” NAND disclosure. Reply 10–11.

This argument is not persuasive. The claims are not simply directed to NAND memory. Thus, the issue is not whether a skilled artisan would have recognized in 2020 that a three-dimensional dimensional array of storage elements could refer to a 3D vertical NAND structure. Rather, the issue is whether a skilled artisan, looking at Dong in 2020, would have understood that Dong disclosed all of the elements recited in the claims.

A reference does not anticipate unless it discloses within the four corners of the document all of the limitations arranged or combined in the same way as recited in the claim. Patent Owner persuasively argues, with supporting evidence, that Dong’s reference to three dimensional storage in paragraph 95 does not necessarily disclose arranging wordlines vertically from bottom to top as recited in claim 5. PO Resp. 41–44.

Petitioner does not persuasively explain how Dong’s paragraph 95 relates to the self-boosting modes of Figures 5a–5h. We agree with Patent Owner that Dong’s mention of a “three dimensional array” is ambiguous and does not sufficiently support Petitioner’s anticipation argument.

“Ambiguous references do not anticipate a claim.” *Wasica Fin GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1284 (Fed. Cir. 2017). We agree with Patent Owner that Dong’s “three dimensional” statement could mean 3D memory that does not include vertically stacked memory strings, but rather refers to horizontal stacking of 2D NAND dies to form a 3D NAND structure. *See, e.g.*, Sur-reply 13 (citing Ex. 2028 ¶¶ 190–195).

Thus, for the foregoing reasons, Petitioner has not sufficiently shown that Dong anticipates claim 5 under the “vertically arranged wordline” claim construction of the “from bottom to top” limitations.

In our Decision on Institution, we determined that Petitioner sufficiently showed that claim 5 would have been obvious for purposes of institution. Upon review of a full record, however, we determine that Petitioner has not sufficiently shown that Dong would have rendered claim 5 obvious. In particular, we determine Petitioner has not sufficiently shown that a skilled artisan would have applied the disturb mode methods of Dong’s Figures 5a–5h’s to a vertical 3D NAND string with a reasonable expectation of success. Pet. 28–44; Reply 16–25.

Citing Dr. Liu’s testimony, the Petition states that “to the extent ***bottom to top*** is interpreted to require vertical strings in a 3D NAND memory, Dong discloses its “array of storage elements can be three dimensional” and shows Fig. 5a in a vertical orientation which satisfies the claim.” Pet. 35 (citing Ex. 1005 ¶ 95; Ex. 1004 ¶120). Dr. Liu explicitly addresses whether Dong’s 2D memory string would have rendered the vertically arranged wordlines from bottom to top obvious, stating “given the similarities between 2D and 3D NAND discussed in the Technology Background section, even a 2D memory string would at a minimum *render obvious the bottom to top* requirement, even if narrowly construed.” Ex. 1004 ¶ 120 (emphasis altered).

Neither the Petitioner nor Dr. Liu, however, sufficiently address whether a skilled artisan would have had reason to apply the program disturb methods of Dong’s Figure 5a-5h to a 3D NAND having vertically arranged

wordlines with any reasonable expectation of success. Pet. 11–15, 28–44; Reply 16–25.

We recognize that the “Background Section” of the Petition and Dir. Liu’s opening declaration discusses the generic development from 2D NANDs to 3D NANDs and techniques used to program memory cells. Pet. 11–15; Ex. 1004 ¶¶ 49–62. In particular, Petitioner asserts that conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block and turning the 2D NAND string upside, resulting in a 3D structure with a vertical channel. Pet. 12–13. Petitioner further states that “there are many similarities between 2D and 3D NAND flash memory devices, including the techniques and algorithms used to program memory cells” and mentions the problem of program disturb. *Id.* at 14–15 (citing Ex. 1009, 52–53; Ex. 1004 ¶¶ 49–62). Neither Petitioner nor Dr. Liu clearly address how or why a skilled artisan would have been motivated to modify Dong’s program disturb methods for 2D NAND to 3D NANDs having vertically arranged wordlines.

Patent Owner argues, with persuasive supporting testimony by Dr. Khatri, that Dong’s 2D NAND isolation voltage scheme is a planar solution that a POSITA *would not apply* in a vertical 3D NAND as of the priority date of the ’941 patent. PO Resp. 50 (citing Ex. 2028 ¶¶ 48–83, 207–220. As the Aritome textbook recognizes, the “program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed.” Ex. 1009, 354; *see also id.* at 356 (“The program disturb conditions and characteristics of 3D cells are greatly changed from that of 2D cells.”), 362 (“Program disturb

phenomena and mechanisms of a 3D NAND cell are much different from that of a 2D NAND cell.”); Ex. 2028 ¶ 208.

Dr. Khatri provides persuasive testimony that a skilled artisan would not have been motivated to apply Dong’s program disturb methods for 2D NAND cells to vertical 3D NAND cells at least because vertical 3D NAND cells have vertically stacked cells that exhibit more complex disturb mechanisms that can lead to increased errors during programming. Ex. 2028 ¶ 209 (quoting Ex. 1009 pt. 2 at 354 as recognizing “[t]he program disturb mechanisms of 3D NAND cells are much different from that of 2D NAND cells, because cell structure and array architecture are totally changed”), 356 (“The program disturb conditions and characteristics of 3D cells are greatly changed from that of 2D cells.”), 362 (“Program disturb phenomena and mechanisms of a 3D NAND cell are much different from that of a 2D NAND cell.”).

Petitioner responds that because both 2D NAND and 3D NAND have overlapping program disturb modes, that Dong’s 2D program disturb alleviation methods equally apply to 3D NAND. Sur-Reply 19–21. This argument, however, still fails to adequately address why a POSITA would have had a reasonable expectation of success in applying Dong’s 2D NAND program disturb methods in a vertical 3D NAND context. Indeed, Dr. Liu’s first declaration acknowledges that there have been “many techniques and approaches developed over the years” since the days of 2D NAND to mitigate the effects of program disturb. Ex. 1004 ¶ 61. Dr. Liu does not indicate how a skilled artisan would determine which 2D NAND program disturb methods could be successfully employed with a 3D NAND, instead only stating that “many techniques for mitigating program disturb originally

developed for 2D NAND are of equal applicability to 3D NAND devices.”
Id.

Given the differences between the program disturb mechanisms of 2D and vertical 3D NAND strings, Petitioner has not sufficiently shown that a skilled artisan would have reason to employ Dong’s method for mitigating program disturb with a vertical 3D NAND with a reasonable expectation of success. Thus, Petitioner has not sufficiently shown that claim 5 would have been obvious over Dong.

3. *Asserted Unpatentability of Independent claims 1 and 11 and Dependent Claims 3, 6, 7, and 13*

Petitioner asserts that Dong anticipates or renders obvious claims 1 and 11 and presents argument and evidence mapping Dong Figure 5g to these claims. *See* Pet. 50–66 (addressing claim 1), 68–70 (addressing claim 11). Petitioner states that the “same preliminary comments about Dong Fig. 5a (provided in §X.A for claim 5) apply here.” Pet. 50 (discussing claim 1); *see also* Pet. 52 (stating the same discussion regarding the preamble of claim 5 (§ X.A.1) applies to claim 1 regarding the meaning of bottom to top); *id.* at 68 (discussing claim 11).

Based upon a complete record, we determine that Petitioner has not shown by a preponderance of the evidence that Dong either anticipates or renders obvious independent claims 1 or 11, or dependent claims 3, 6, 7, or 13, for the same reasons set forth regarding claim 5.

D. Asserted Unpatentability of Dependent Claims 8 and 9 over Dong and Costa and of Claims 4, 10, and 14 over Dong and Shirai

Petitioner asserts claims 8 and 9 (which depend indirectly from claim 5) would have been obvious over Dong in combination with Costa, and that claims 4 (which depends from claim 1), 10 (which depends from claim 5), and 14 (which depends from claim 11), would have been obvious over Dong in combination with Shirai. Pet. 70–84; Reply Br. 25–38.

Petitioner’s arguments regarding these dependent claims do not remedy the deficiencies regarding the independent claims set forth above. See Pet. 70–84; Reply Br. 25–38. Accordingly, we find that Petitioner has not shown by a preponderance of the evidence that claims 8 and 9 would have been obvious over Dong and Costa or that claims 4, 10, and 14 would have been obvious over Dong and Shirai.

III. CONCLUSION

After reviewing the parties’ arguments and weighing the evidence offered by both parties, we determine that Petitioner does not show, by a preponderance of the evidence, that claims 1, 3–11, 13, or 14 of the ’941 patent are unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1, 3, 5–7, 11, 13	102(a)(1) 102(a)(2)	Dong		1, 3, 5–7, 11, 13
1, 3, 5–7, 11, 13	103	Dong		1, 3, 5–7, 11, 13
8, 9	103	Dong, Costa		8, 9
4, 10, 14	103	Dong, Shirai		4, 10, 14

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
Overall Outcome				1, 3–11, 13, 14

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not established by a preponderance of the evidence that claims 1, 3–11, 13, and 14 of the '941 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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