

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

IPR2025-00190
Patent 11,568,941 B2

Record of Oral Hearing
Held: April 28, 2026

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and MICHAEL
T. CYGAN, *Administrative Patent Judges*.

IPR2025-00190
Patent 11,568,941 B2

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P R O C E E D I N G S

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JUDGE CYGAN: Good morning. This is Judge Cygan. Judges McGraw and Kokoski are present by video. We will now hear argument in case number IPR2025-00190 concerning U.S. Patent number 11,568,941. This is between Petitioner Micron Technology and Patent Owner Yangtze Memory Technologies. Counsel for the party, starting with Petitioner, please introduce yourself.

MR. JENSEN: Your Honor, may it please the Board, Travis Jensen for Petitioner Micron. With me today is lead counsel, Jason Lang, and we also have Micron representative, Jan Bissey in person.

MR. LOWRY: Good morning, Your Honors. My name is Richard Lowry of Latham & Watkins, on behalf of YMTC, the Patent Owner, and with me is my colleague, Ms. Inge Osman, who is also lead counsel.

JUDGE CYGAN: Thank you, and welcome to the Board. Prior hearing order, each party was provided with 60 minutes oral argument. Patent Owner's lead request for Mr. Lowry was granted. So Patent Owner will have an additional 15 minutes of oral argument for a total of 75 minutes.

The parties need not use the entirety of that time. Petitioner will argue first and may reserve time for a rebuttal. Patent Owner will respond to Petitioners discussion and may reserve time for surrebuttal. We have the demonstratives for each party. Please remember to identify the number of the demonstrative slide you're referencing as you present your argument. Petitioner, how much time would you like to preserve for rebuttal?

MR. JENSEN: Twenty minutes please.

1 JUDGE CYGAN: Okay. So we'll start you with 40 minutes for
2 your main case, and you can begin when ready.

3 MR. JENSEN: Good morning, Your Honors. The parties have a
4 number of IPR disputes in front of this same panel, many of those deal with
5 NAND flash memory technology and manufacturing processes for those
6 technologies, the structural aspects of those devices like staircase structures
7 and the relative order of certain layers. The '941 Patent at issue today is a
8 little bit different than some of those other patents. The '941 Patent has to do
9 with programming a memory string, the voltages, et cetera, that are applied
10 to perform the programming as opposed to the structure and manufacturing
11 process of the NAND flash memory.

12 Slide 2 provides an overview of the topics I hope to address today.
13 I don't think in the time available we'll be able to cover all of them, and
14 there's a few that I'd like to focus on. But I'd be happy to answer questions
15 that the Board may have on any of the topics. I'd like to begin by spending
16 just a couple of minutes talking about the '941 Patent itself.

17 And turning to Slide 11, the one thing that I'd like to point out on
18 this slide is the priority date of the patent, which is in 2020. That's going to
19 become important later when we get into the Dong prior art reference. And
20 I'll note that this is a relatively late priority date for NAND flash memory.
21 It's just five years ago, and that the technology was fairly well developed at
22 that point.

23 The '941 Patent is concerned with reducing what's called program
24 disturb and pass disturb, and this is on Slide 12. The patent is sparse on
25 details. There is a passage in Column 6, Lines, 39 to 43 that references
26 some simulations and experiments that allegedly were done that would

1 explain that -- how the program disturb and pass voltage disturbed is
2 reduced. None of those simulations or experiments or any of the how is
3 explained in the '941 Patent. It doesn't give any concrete examples. There's
4 no specific voltages that are identified.

5 If we look at Slide 13, this is an annotated version of Figure 1 from
6 the patent, and the figures are quite similar in the patent in terms of what
7 they depict. And you can see here that there are a number -- of the red
8 annotations are added, but everything in black is in the original figure.
9 There's a number of voltages labeled V1, V2, et cetera, that the claims refer
10 to as first, second, third voltage. And on the left-hand side, you can see
11 there's a number of variables or indices, WL is word line, WLM is simply a
12 random variable.

13 Again, there are no examples given in the patent of what those
14 variables might be, the actual numbers of the length of the word line, et
15 cetera. It's all just relative, plus one minus one, et cetera. And the word
16 lines are grouped into what are called portions. Again, this is a very generic
17 term. There's no magic to it. I would submit it's not really even a term of
18 art. It's just a arbitrary grouping of word lines.

19 And the claims, if we turn to Slide 14, map to -- it happens to be
20 Claim 5. It's an independent claim. Slide 15 shows a similar mapping for
21 Claim 1 that indicates how the claims of the patent, the first voltage, second
22 voltage, the first portion, the second portion, et cetera, would apply to the
23 preferred embodiments illustrated in the figures of the patent. The key
24 takeaway from these mappings and figures is that -- what the '941 Patent is
25 all about is providing these voltage mappings.

26 And the voltages have to be applied to specific groupings of word

1 lines. But again, those groupings are arbitrary. They're all relative using
2 variables, and no examples are given in the patent of what those variables
3 might be or, for that matter, what any of the voltages might be, I'll say with
4 one exception that has to do with one of the voltages has to do with the
5 -- you know, lower than one of the other voltages.

6 And that is not really an issue here, that point is not disputed in the
7 proceeding. But for the most part, they're -- the voltages could be anything.
8 They just have to be applied to specific groupings of word lines.

9 So with that, let me turn to Slide 4, which provides an overview of
10 the four grounds that are at issue here. And I apologize there's a typo on
11 Ground 3. This is a carryover from a prior proceeding of references, saying
12 -- that should be Dong. All of the foregrounds rely on the Dong reference.
13 Grounds 1 and 2 rely exclusively on Dong. Ground 1 is anticipation.
14 Ground 2 is single reference obviousness. Grounds 3 and 4 combine the
15 Costa and Shirai references respectively for certain dependent claims.

16 So let's talk a little bit about the Dong reference, turning to Slide
17 16. The one thing that I'll point out on this slide is that the Dong reference
18 published in 2008, some 12 years or more than a decade before the priority
19 date of the '941 Patent. It was originally filed, I think, a year earlier in 2007.
20 There's no dispute that this reference or any others qualify as prior art.

21 There are two figures in Dong that we rely on, depending on the
22 claim. These are Figure 5A and 5G in the Dong reference. This is on Slide
23 17. And each of these figures provides a -- basically a voltage mapping to a
24 memory string of word lines in a NAND flash memory structure. If we look
25 at that Slide 6, we can see -- there we go. Slide 6, we provide an annotated
26 version of Figure 5A, which maps to Claims 5 through 10 where we identify

1 the claimed first and second portion and the various first, second, third
2 voltages, et cetera.

3 In this respect, I think it's important to point out that the Patent
4 Owner doesn't really challenge any of the voltage mappings. What is -- the
5 third voltage, for example, is V pass, and then it's applied to the W word
6 line, X plus 1 and so forth. And again, that's what the '941 Patent is really
7 all about is what are these voltages and what are the word lines that they are
8 being applied to. So we can see in Figure 5A the mapping. There's a typo at
9 the bottom. Let's just say Claim 5, the title is correct. This applies to
10 Claims 5 through 10.

11 And on Slide 7, we have the mapping for Dong Figure 5G to
12 independent Claim 1, independent Claim 11, and various dependent claims
13 as well. And again, there's no dispute here, at least for the independent
14 claims with respect to the voltage mappings, the V1 through V5 and the
15 portions which is really the heart of what the '941 Patent is all about.

16 So if we turn to Slide 18, this is paragraph 95 from the Dong
17 reference. And we've highlighted a passage in there that I think is important
18 and is very much disputed in this proceeding. And this is the passage that
19 says, in some embodiments, the array of storage elements can be three-
20 dimensional. So there's no dispute that a, quote, "three-dimensional array of
21 storage elements is disclosed in Dong.

22 JUDGE CYGAN: Counsel, can you explain the relevance of the
23 three-dimensional discussion to the limitations of Claims 1 and 5?

24 MR. JENSEN: Yes, and that's exactly where I was going next. So
25 all of the assorted claims include a limitation that resides -- I forget if it's
26 bottom to top or top to bottom. But either way, it includes that limitation.

1 And there's a dispute -- a claim construction dispute between the parties as
2 to what that means. I don't want to spend a lot of time on the claim
3 construction issue today, given the limited time. And the reason for that is
4 because it doesn't matter, Petitioner prevails under either party's
5 construction.

6 So very briefly, with respect to Petitioner's construction, we
7 propose that that term would be understood by a person of ordinary skill in
8 the art to mean source to drain. So from bottom to top would be source to
9 drain, such that the claim would apply to not only I'll say vertical memory
10 strings in a three-dimensional memory array, but also conventional or
11 traditional two-dimensional memory strings.

12 If we look at Slide 25, there really is no dispute between the parties
13 that if Petitioner's construction is correct, that the claims are anticipated.

14 JUDGE CYGAN: Counsel, just to clarify, for example, Claim 1,
15 does Claim 1 require a two-dimensional organization or does it require a
16 three-dimensional organization?

17 MR. JENSEN: Petitioner submits that it reads on both. If you
18 look at Claim 1 -- and let me go to slide, I think, 15 that has that. The claim
19 language you can see in the preamble. The preamble recites a memory
20 comprising. It doesn't recite either a two-dimensional memory or a three-
21 dimensional memory. It doesn't use the word vertical. That's nowhere to be
22 found in the claims. And I think that if the applicant or the claim drafter
23 wanted to restrict their claim or limit it to a three-dimensional or a vertical
24 memory string, that that would be apparent in the claim language itself.

25 The only hook that the Patent Owner has for its vertical argument
26 is that language bottom -- from bottom to top. And for the reason we

1 discuss in our papers, a person who has skill in the art would understand that
2 especially given the historical development of NAND flash memory from
3 two-dimensional to three-dimensional, that the claim broadly covers both,
4 especially given that the programming techniques translate readily from one
5 to the other.

6 And in fact, we'll talk about this a little bit later. In relevant part,
7 they are the same. They are literally identical, as taught in textbooks.

8 JUDGE CYGAN: And Claim 1 is not limited to a single memory
9 string correct?

10 MR. JENSEN: Yes, that is correct. Typically, when you program
11 a memory structure, you're programming word lines, which are connected to
12 a number of different memory cells. So I don't see any restriction in that
13 regard.

14 If we turn to Slide -- give one moment to find the slide number
15 here, 27, I do want to talk about why Dong first anticipates the claims under
16 the Patent Owner's construction, which restricts -- did we lose Judge
17 Kokoski? I see her monitor went off continuous.

18 JUDGE CYGAN: Right. Let's pause for a second until we get her
19 back up.

20 JUDGE KOKOSKI: We lost Judge McGraw.

21 MR. JENSEN: Oh, it switched monitors. I apologize.

22 JUDGE KOKOSKI: Yes, they moved me over. It's okay.

23 MR. JENSEN: No proceeding is complete without at least one
24 technical difficulty, and we've had our first. So welcome back, Judge
25 McGraw.

26 Let me pick up where I left off with talking about anticipation by

1 Dong under the Patent Owner's narrow construction of bottom to top, which
2 would require a vertical memory string structure. In this regard, we come
3 back to the disclosure in Dong, paragraph 95, that the array of storage
4 elements can be three-dimensional. And we'll talk about what that three-
5 dimensional disclosure means.

6 But Petitioner submits that that plainly includes and means a
7 vertical memory strain. So if we look at -- this on Slide 29, a comparison of
8 a representative figure in the '941 Patent on the left-hand side, that's Figure
9 8. But it could be any other figure as well. And Dong Figure 5A on the
10 right hand side, the - I'll say vertically oriented nature of the figures is
11 immediately apparent in both images.

12 And the Patent Owner talks a lot about Dong Figure 4, which we
13 do not rely on because it doesn't have the correct voltage mappings. But
14 they point to that figure and say, oh, that that figure is a two-dimensional
15 memory string, and therefore Dong Figures 5A and 5G must also necessarily
16 be and are limited to horizontal or 2D memory strings. We submit that that
17 would present a double standard at a minimum, given that the similarity
18 between the figures, their vertical orientation, but especially when you take
19 into account Dong's expressed disclosure in paragraph 95 that its memory
20 arrays can be three-dimensional.

21 Patent Owner contends that the term three-dimensional in Dong
22 includes a stack of 2D memory structures. I think that argument fails for a
23 couple of reasons. First, the parties have a dispute over -- and this is on
24 Slide 30. The parties have a dispute over what is the relevant date for
25 assessing the knowledge of a POSITA and for assessing the scope and
26 content of the prior art. Petitioner says the correct date to use is the priority

1 date in 2020 of the '941 Patent, and Patent Owner contends that the Dong
2 filing date of 2007 should be used.

3 Slide 31 we quote the anticipation and obviousness statutes, which
4 both confirm that the correct date to use for an invalidity analysis, including
5 what is a POSITA's knowledge, how would they understand the reference
6 and the term --

7 JUDGE MCGRAW: Excuse me, I do have a question.

8 MR. JENSEN: Yes.

9 JUDGE MCGRAW: I agree that the time frame for determining
10 obviousness is the effective date of the challenged pad. But the issue is what
11 would Dong have taught to someone as of that date. How are we to
12 understand that a person skilled in the art reading Dong in 2020 would
13 understand that its disclosures apply to a 3D-NAND vertical device?

14 For example, if somebody had a patent related to flying blimps that
15 was filed right after Kitty Hawk, and then there was a patent at issue in
16 2020, would somebody was looking back at the early Kitty Hawk-time
17 patent, would they understand that all of those disclosures in that patent
18 which they related to a flying machine would necessarily apply to the type of
19 flying machines that existed in 2020?

20 MR. JENSEN: I think there's two answers to that question, Judge
21 McGraw. The first one has to do with the knowledge of a POSITA, right?
22 Anytime a person of ordinary skill in the art read a prior art reference, they
23 bring with them -- and we cite a bunch of cases. I won't go through all of
24 them. But they necessarily carry with them the knowledge of a POSITA as
25 of the effective filing date of the claim being challenged. In this case, that is
26 in 2020.

1 By that point in time, the state of the art -- the development of 3D
2 NAND flash memory had become such that vertical memory strings were
3 ubiquitous in the art. And we submitted copious evidence of this. I'll point
4 you to example -- for example, to Slide 40, which is a press release from
5 Samsung who's a well-known NAND flash manufacturer. And they're --

6 JUDGE MCGRAW: I don't think there's a dispute that 3D NAND
7 technology was known. I think the issue is what would one of skill in the art
8 looking at Dong have understood Dong to teach. Where is the evidence in
9 the record that a person skilled in the art would have understood Dong
10 disclosures would relate to 3D vertical NAND technology, particularly
11 given Patent Owner's arguments that there is a difference between the
12 program modes for 2D and 3D NAND devices?

13 MR. JENSEN: So I think there's copious evidence in the record. I
14 can point you to our expert declarations where they discuss this, and even
15 the testimony of Patent Owner's own expert, Dr. Khatri, who conceded that
16 vertical memory strings were definitely known in the art as of 2020. And I
17 would submit to Your Honor that in view of the state of the art, again, the
18 POSITA carries with them that knowledge, and when they read the term 3D
19 NAND flash memory, the thing that comes to mind is a vertical memory
20 string.

21 And we know that as well from Patent Owner's own filings in
22 many related IPRs here where they repeatedly and consistently discussed 3D
23 NAND flash memory exclusively as referring to vertical memory strings.
24 And we cite a number of examples of that on Slide 37. So I don't think that
25 there can be any legitimate dispute that in 2020, vertical NAND flash
26 memory strings were synonymous with three-dimensional memory. And

1 then when a person of skill in the art in 2020, having that knowledge reads
2 the disclosure in Dong of three-dimensional memory, that that is
3 immediately what they envision, what they see, what they understand that
4 term to me.

5 But even if -- and I would submit that it would be improper to -- I'd
6 say try to do it through the back door what's prohibited through the front
7 door. And by that, I mean to say that a person of ordinary skill in the art,
8 even though they're reading the Dong reference in 2020, they have to time
9 warp their understanding and their state of mind back to 2007 when Dong
10 was filed. I think that's foreclosed by the statutes and the case law that it
11 expressly says you do not do that.

12 But I want to say even if you were to rewind in time and look at
13 Dong as of its 2007 filing date, that a person of ordinary skill in the art
14 would understand that the disclosure of three-dimensional included vertical
15 memory strings. And I'm on Slide 42 in the deck here. And this shows a
16 couple of images, excerpts from what we call the endo-1 reference. That's
17 Exhibit 1101.

18 And this reference is from 2003. And it's showing a three-
19 dimensional memory string. And you can see that in I'll say sort of physical
20 form. Illustrated on the left, there's multiple memory cells stacked
21 vertically. That's referred to as 3D memory. And the schematic diagram on
22 the right is identical to the memory strings, albeit shorter, it doesn't have as
23 many as many memory cells. But that's irrelevant.

24 That even in 2003, so four years before Dong was filed, three-
25 dimensional memory was known to be vertical memory strings. The endo-1
26 reference, I don't have a slide -- or the endo-2 reference, excuse me, goes

1 back even earlier in time to 2001 and has similar disclosure.

2 If we look at Slide 43, this is the Kito reference, Exhibit 1087, and
3 we show Figures 2 and 17. And this is a reference -- it's a patent
4 publication. It was filed in, I think -- believe January of 2007. So well
5 before the filing date of the Dong reference and the --

6 JUDGE MCGRAW: If I could interrupt again. So even if we
7 agree that three-dimensional NAND flash technology was known in 2007,
8 could you make the connection that one of skilled in the art would have
9 understood that Dong's program mode disclosures would apply to that 3D
10 vertical NAND technology?

11 MR. JENSEN: Absolutely, Your Honor. And we talked about that
12 in our petition, that the programming techniques that are applicable to 2D
13 memory and 3D memory in relevant part are the same. So the programming
14 techniques to reduce program disturb, which is what Dong is all about. And
15 we know that, for example, by looking at the -- we can look at the Aritome
16 reference, that's a textbook. Let me see if I can find the slide number for
17 that.

18 So that would be Slide 56. And the Aritome textbook talks about
19 and does and express, let's say, comparison and contrast between
20 programming 2D and 3D memory. So what's shown on Slide 56 is Figure
21 8.11 from Aritome. And he expressly identifies two program disturb modes.
22 He labels them one and two, and he calls those conventional modes. And
23 we'll see on the next slide that that is in -- conventional modes is in reference
24 to 2D memory streams.

25 And then he says there are two additional modes in 3D memory,
26 what he calls Modes 3 and 4. And Aritome illustrates those on Slide 57. So

1 it provides kind of a schematic diagram of a 3D memory. And there are
2 kind of four groupings of memory strings. The first one, number one, is the
3 string being programmed. That's STR in PGM. PGM is program mode.
4 Number two is the string or string --

5 JUDGE MCGRAW: Sir, excuse me, how would you respond to
6 Patent Owner's argument that because Modes 3 and 4 are only in 3D NAND
7 technology, not in 2D NAND technology, that one of skilled in the art would
8 not have understood Dong disclosure to apply to 3D vertical NAND
9 technology?

10 MR. JENSEN: So Dong's disclosure like -- just like the disclosure
11 in the '941 Patent focuses on the program disturb Modes 1 and 2 in the string
12 being programmed, and another string in the X mode. Sometimes that's
13 referred to as pass voltage disturbed. And Aritome expressly says that those
14 disturbed modes, this is on Slide 58, this is a quote from Aritome,
15 "Disturbed X mode is the same as a conventional program disturb mode in a
16 2D NAND cell."

17 So the disturbed modes are the same. And the solution for
18 reducing program disturb is also the same. And Aritome talks extensively
19 about that. The fact that there are additional program modes, 3 and 4 in 3D
20 NAND memory is irrelevant. The '941 Patent says nothing about those. It
21 says nothing about solving program modes 3 and -- program disturb modes 3
22 and 4. It doesn't even acknowledge that they exist. It's like if you have a
23 hamburger and you add a slice of cheese to it, it becomes a cheeseburger.
24 That's all fine and good. You still have a hamburger patty, and that is the
25 same.

26 In other words, program modes -- program disturb modes 1 and 2

1 and the proposed programming voltages that reduce or solve those problems
2 are identical. They're the same between 2D and 3D. We can see this, for
3 example, in Slide 60. This is another image from Aritome. On the left-hand
4 side, you have the conventional 2D program modes, X mode and PGM.
5 And you can see those illustrated on the bottom. And on the right-hand side,
6 you have 3D program modes. And you can see that the x mode and PGM
7 mode, those are modes 1 and 2, are identical in 2D and 3D. And the
8 solutions to them are also identical.

9 The fact that you have additional program modes 3 and 4 in three-
10 dimensional memory is beside the point. And we know this, additionally,
11 because if we turn to Slide 61, Aritome explains how it is that you would
12 address or solve program modes 3 and 4, right? And the solution to those
13 -- it's not highlighted. It's in the top part of the image. And it's a quote from
14 Aritome. So for solving the new program disturb modes, there's three things
15 you can do.

16 Number one is you can set a high threshold voltage of the drain
17 select line, which is the transistor on the top of the memory string that is not
18 being used to store a data bit; you can apply a bias to that transistor; or you
19 can insert dummy word lines. That's how you solve program modes 3 and 4.
20 Neither Don nor the asserted patent, frankly, talk about inserting dummy
21 word lines as a method of solving program disturb. And neither of them say
22 anything at all about programming the -- or not programming but making
23 changes to the drain select line transistor.

24 And in fact, we asked Patent Owner's expert about this at his
25 deposition, whether the '941 Patent had anything to do with the drain select
26 line at all. And his answer was it's not talking about the additional

1 transistors, the select transistors like DSL, for example, because that's not
2 the focus of the '941 Patent. The focus of the '941 Patent, just like Dong, is
3 on solving program disturb modes 1 and 2.

4 And in this regard, it's notable that -- because it's undisputed that
5 the voltage mappings in Dong read on the claims of the '941 Patent, that
6 those programming voltages were ineffective or did not solve the program
7 disturb problems, that those same programming voltages in the '941 Patent
8 would not solve those problems either. So there's a complete double
9 standard there. If Dong is somehow ineffective at solving program disturb
10 in 3D NAND flash memory, so is the '941 Patent. It does nothing to address
11 the problem.

12 JUDGE MCGRAW: Now these arguments that you're pointing to
13 now were all in the reply brief. Is there anything that was discussed in the
14 petition that would address what you're discussing now?

15 MR. JENSEN: Absolutely, Your Honor. If we looked at -- let me
16 see if I can find a cite for you. I think it starts in the technology background
17 section of the petition. And I know we have a slide on this, give me just a
18 moment. Let's turn to Slide 51. Slide 51 for example here, so this is from
19 petition at Page 13. And we have a quote here from it, that -- and this is a
20 quote from a reference itself, but it's included in a petition.

21 JUDGE MCGRAW: Okay.

22 MR. JENSEN: "Conceptually, a modern 3D structure could be
23 conceived by starting from the 2D NAND stream building block, turning it
24 on its side, resulting in a 3D --"

25 JUDGE MCGRAW: I don't want to hold you up. I know that you
26 have a lot of other issues to cover. So thank you for answering my question,

1 but feel free to move on if you like.

2 MR. JENSEN: The last thing I'll point out on this, because I think
3 it's an important point, is on Slide 52. This is a quote from our petition at
4 14, where we specifically discuss not just sort of the I'll say overall structure
5 or the conversion from 2D to -- the development from 2D to 3D NAND.
6 But we specifically say that the algorithms used to read, erase, and program
7 memory cells and memory strings are similar between 2D and 3D. And yes,
8 we did elaborate on that in our reply in response to arguments that the Patent
9 Owner had made in their Patent Owner response, but it was definitely teed
10 up in our petition.

11 Let me go back for just a moment to finish up a discussion on
12 -- this is at Slide 43, this is the 2007 Kito reference and -- which plainly
13 discloses a vertically oriented three-dimensional memory structure, memory
14 strings. When we asked the Patent Owner's expert about this at his
15 deposition, Dr. Khatri, he was like a deer in the headlights. He could not
16 answer a question. He could not tell whether these figures represented a
17 vertical memory string or a stack of -- a two-dimensional stack of -- excuse
18 me, a stack of two-dimensional memory arrays.

19 And I would submit to Your Honors that that is simply not credible
20 for someone who has purported expertise in this area. I think that anybody
21 with even a modicum of knowledge -- and certainly a POSITA would be
22 able to look at these structures and in an instant immediately recognize them
23 as vertically oriented memory strings. Dr. Khatri talked for pages and pages
24 and pages about why he would not be able to make such a determination.
25 And I submit that that is simply not credible.

26 There are a number of other examples. I won't belabor these here.

1 This is on Slide 44. The only thing that I want to point out at this point
2 -- and this is another 2007 reference, in response to their argument that there
3 was a lack of enablement in the prior art or that a person of ordinary skill in
4 the art wouldn't know how to do a vertical memory string. On the right-
5 hand side, in Figure 7A, is actually a cross section of an actual manufactured
6 vertical memory stream.

7 So these weren't just research, theses, or a dissertation somewhere,
8 research, hope in a backwater university or something. People were actually
9 manufacturing and fabricating these structures in 2007. And the Kito
10 reference on Slide 43 has over 100 figures showing the complete
11 manufacturing flow for manufacturing in 2007 a vertical 3D memory string
12 and device.

13 JUDGE CYGAN: Counselor, has there been any other claim
14 construction on this in any of the proceedings?

15 MR. JENSEN: There is a counterpart District Court proceeding, I
16 believe, in the Northern District of California where the construction of the
17 term bottom to top is at issue. I can double check on reply to confirm. But I
18 believe that no hearing has been held. That case has stayed. There was
19 claimed construction proceedings or briefing -- oh, no.

20 Okay. I stand corrected, no briefing was actually submitted. There
21 were expert declarations submitted in advance of claim construction
22 briefing, and the case was state at that point. The answer is yes and no. But
23 certainly no ruling, no briefing, no Markman hearing, but similar issue is
24 before that court.

25 JUDGE CYGAN: Thank you. Counsel, can you go back one
26 slide? I'm sorry, the slide with the three-dimensional figure on it. If you

1 took that figure and you're saying that figure on the right would show

2 -- which are the word lines in a bottom to top position, correct?

3 MR. JENSEN: Oh, yes, absolutely. Even under Patent Owner's

4 -- what we submit is a narrow construction that requires a vertically oriented
5 memory string, there can be no doubt that Kito discloses that.

6 JUDGE CYGAN: What if you took that memory structure

7 -- where in Claim 1 we're talking about a memory structure. What if you

8 took that and you knocked it on its side, would that now be in the bottom to
9 top?

10 MR. JENSEN: I would submit that under Petitioner's construction
11 it certainly would, where bottom to top means source to drain. I don't think
12 that there's been any proposal in this proceeding that you take a -- I'll say a
13 vertically-oriented 3D memory structure and rotate it 90 degrees. I would
14 submit that it would still maintain its character as a 3D memory structure. It
15 would not be somehow converted into a -- like a two-dimensional horizontal
16 array.

17 And I think this issue is -- or the disclosures in the Kito, the
18 Tanaka, and the endo references are relevant to Judge McGraw's earlier
19 question about how a person ordinary skill in the art would understand the
20 term three-dimensional in the Dong reference. Even if you got in your Back
21 to the Future machine and went back to 2007, that there is ample evidence
22 that three-dimensional would be understood at a minimum to include the
23 vertical memory strings in all the references that that we have discussed.

24 JUDGE CYGAN: And if I understand your answer from earlier,
25 there is -- there's no three-dimensional requirement in the claims?

26 MR. JENSEN: That is correct. They don't say three-dimensional.

1 And I think it's notable because in the specification of the asserted patent
2 there is some discussion in the background section, not in the actual
3 disclosure section of applying the voltages to the memory -- or to the word
4 line groupings. But in the background section there is some discussion of
5 vertical three-dimensional memory.

6 And so the Patentee was certainly aware of what that term was. If
7 they wanted to claim three-dimensional memory or vertical memory, they
8 certainly knew how to do it because they use those words in the background
9 section, albeit not in the actual substantive disclosure section of the patent.

10 In the few minutes that I have left, I'd like to turn briefly to Ground
11 3, and that is at Slide 63. And there's another claim construction issue that
12 comes into play here. Ground 3 three is obviousness over Dong in view of
13 Costa. And this applies to Claims 8 and 9. And these claims on Slide 64,
14 Claim 9 is representative. It talks about the first voltage in various -- what
15 they call levels. The first voltage has a first level.

16 If the X word line -- and that's the word line being programmed
17 -- is in a first portion, that voltage has a second level or a second value. If
18 the word line being programmed is in a second portion and -- basically it's
19 talking about as you program a memory string, as you move, whether it's up
20 or down, however you want to characterize that, but as you move from one
21 word line to the next in a memory string, that the claimed first voltage takes
22 on a different value.

23 And you can see that illustrated in -- on Slide 65, showing Figures
24 1 and 2 from the patent, where the word line being programmed, WL X, is in
25 a different location. And this is plainly disclosed in the Costa reference,
26 where they say that the pass voltage that is applied is dependent upon the

1 position of the selected memory cell in the group. The pass voltage for at
2 least a subset of the unselected memory cells that have already been
3 subjected to programming may be increased. This is the exact concept that
4 is being claimed in Claims 8 and 9.

5 Patent Owner makes an argument that the Petitioner did not make
6 a showing or did not somehow disclose that this claim limitation was met
7 because our petition was somehow limited to disclosing programming a
8 single word line in in a memory string. That I submit fails the red face test.
9 Both of the references that is Costa and Dong expressly disclosed that
10 programming proceeds through the entire memory string. You don't just
11 program a random cell in the middle of the memory string. You typically
12 start at the source end and work your way up the string toward the drain end,
13 and you program the memory cells one at a time or one word line at a time.

14 And that is, I'll say, part and parcel, that sort of table stakes for
15 how you perform memory string programming. The idea that that was
16 somehow not disclosed or we were limited -- our disclosure in the petition
17 was limited to a particular example that was given where the word line X
18 being programmed had a specific value like 4, is simply not credible. No
19 POSITA would believe that. If that was how they propose to program a
20 memory string, they wouldn't be employed for very long. It's super well-
21 known that programming proceeds across the entire memory string. And we
22 talk about that in multiple places in the petition.

23 JUDGE CYGAN: So, Counsel, under your understanding, the
24 programming involved programming a cell and then performing a verify
25 function, then moving on a programming a second one, all that would be
26 considered the programming?

1 MR. JENSEN: Yes, that goes to the claim construction of the term
2 program operation. So let me just touch on that briefly. And I know I'm
3 eating in my rebuttal time. I'll be brief. There's a dispute between the
4 parties with respect to the scope of the term program operation. Petitioner
5 submits that a POSITA would understand the term program operation to
6 include both the charge injection phase and the verification phase of
7 programming and that both of those are integral. They're essential to
8 performing a program operation, which is to say writing a bit of data to a
9 memory cell.

10 If you simply perform a charge injection and put some relatively
11 small amount of charge onto the cell that is insufficient to represent a data
12 value, Petitioner submits that you have not programmed -- you have not
13 performed the program operation to program that memory cell, that the
14 program operation requires the completion of both aspects. And they're
15 iterative, you keep adding charge until you get enough on the cell that you
16 can then confirm that you've written a bit of data and you move to the next
17 line.

18 JUDGE CYGAN: And Counsel, has this term been construed in
19 other proceedings?

20 MR. JENSEN: Not to my knowledge, Your Honor, no. And I
21 don't think it's even been proposed for construction in the District Court
22 since it wasn't an issue there.

23 JUDGE CYGAN: So no other IPR proceeding, for example, has
24 addressed this meaning?

25 MR. JENSEN: Not to my knowledge. I can double check with
26 lead counsel who is more familiar with some of the other proceedings. But

1 to my knowledge, this term has not been construed. I believe it may have
2 come up. You could probably do a control F search and find the term
3 program operation in some other proceeding. But it wasn't the subject of a
4 claim construction dispute.

5 The last thing that I'll note here on the program operation term if
6 we look at Slide 79. And this is from the Dong reference itself. And it
7 shows in Figure 20 a series of pulses. Dong itself characterizes this as
8 quote, "programming." Dong says, "During programming, you have charge
9 injection pulses, 2005, 2007, et cetera." Those are the ones in blue. And in
10 between those, you have a pulse sequence of verify pulses, 2006.

11 And so it's the combination of those program pulses or charge
12 injection pulses and verification pulses that collectively constitute a program
13 operation. And Dong Figure 20 is a singular program operation. That is the
14 sequence of pulses that would be applied to program one memory cell before
15 then moving on to a program operation for a subsequent or adjacent memory
16 cell.

17 Unless the Board has any further questions, I'll reserve the balance
18 of my time for rebuttal.

19 JUDGE CYGAN: Thank you, Counsel. I have you at three
20 minutes over into your rebuttal time. So that would give you 17 minutes for
21 your rebuttal.

22 Patent Owner, how much would you like -- time would you like to
23 reserve for surrebuttal?

24 MR. LOWRY: Good morning, Judge Cygan. I'd like to reserve 15
25 minutes for rebuttal, please.

26 JUDGE CYGAN: Okay. So that will be 60 minutes for your main

1 case, 15 for rebuttal. We'll go off the record while we resolve the second
2 technical issues here.

3 (Whereupon, the above-entitled matter went off the record at 11:06
4 a.m. and resumed at 11:08 a.m.)

5 MR. LOWRY: I'm going to start with Slide 2, Petitioner has not
6 carried its burden for any of the foregrounds. The case turns on a
7 straightforward mismatch between the claims and the prior art. The
8 challenged independent claims require vertically arranged word lines in 3D
9 architecture. But Petitioner's lead reference Dong discloses something
10 different, horizontal arranged word lines in a 2D arrangement. Ground 1
11 fails for this reason alone. Dong does not anticipate the claims because
12 Dong does not expressly disclose the claim vertically arranged word lines.

13 Ground 2 fails for a separate but equally fundamental reason. The
14 petition never presented a limitation specific theory for modifying Dong's
15 horizontal word lines into vertical ones. Now Grounds 1 and 2 are the only
16 grounds directed to the independent claim. So if the Board agrees with
17 Patent Owner on those two grounds, the case is over. Petitioner's challenge
18 to the dependent claims for Ground 3 and 4 necessarily fall with it.

19 Ground 3 addresses Claim 8 and 9 also fails on the merits.
20 Petitioner turns to Costa for this ground, but Costa addresses applying a
21 repass voltage during a verify phase after a cell has already been
22 programmed. Costa is therefore addressing a different operation at a
23 different time.

24 And Petitioner didn't address Ground 4. So I won't address round
25 four, unless when I get there the -- Your Honors has any questions.

26 JUDGE CYGAN: you're making a distinction between the verify

1 stage and the programming stage?

2 MR. LOWRY: Yes, Your Honor.

3 JUDGE CYGAN: I would like to ask Counsel for Patent Owner
4 and also clarify my earlier question for Petitioner about claim constructions
5 and other proceedings. I would like to, at some point, either in this
6 proceeding or following it, to have the parties clarify that nothing in
7 IPR2024-00792, where there was some dispute about applying voltages in
8 the verify stage, and also IPR2024-00795 where there was a discussion,
9 certainly by Patent Owner, about a pulse signal pair lines for a programming
10 step.

11 Was anything that was said in those proceedings which we need to
12 take into account in this one so that we have a constant construction for
13 program operation? It may be that the answer is this program operation
14 wasn't mentioned and it's a different term. If that's the case, I'd also just like
15 that to be clarified. Thank you.

16 MR. LOWRY: Yes, Your Honor. I can address that right now. If
17 we go to Slide 85, please. So Your Honor should take into account the other
18 proceeding, the IPR proceeding ending in 792, because it directly goes to the
19 credibility of Petitioner's expert. Because in the prior -- in his prior
20 testimony where he didn't have an incentive to say that program operation
21 includes these two operations, the charge injection and verify, he said the
22 opposite.

23 We see here at the top, he said that the program operation is a
24 pulse that creates charge in the storage region and then continuing. And the
25 non-highlighted part, and the verify operation determines whether the pulse
26 was sufficient to properly program the cell. Two different phases. He

1 doesn't describe the program operation as including the verify phase.

2 In another paragraph, he said -- regarding Costa, which is the same
3 prior art reference in this proceeding, he said, the read verify occurs after the
4 program operation. And on the bottom left, he repeats it again, a verify
5 operation is a read operation executed after a program operation. Now this
6 is relevant because he's saying the exact opposite here on the right. In the
7 orange box, you can see he now says a program operation includes
8 iteratively performing two steps, a charge injection phase and a verify phase.
9 And he goes on and says that and repeats it over and over again.

10 JUDGE CYGAN: And Counsel, just to clarify, in the other
11 proceeding, this is the '792 proceeding, correct?

12 MR. LOWRY: Yes.

13 JUDGE CYGAN: And that addressed a different patent?

14 MR. LOWRY: That's correct, Your Honor.

15 JUDGE CYGAN: Were those patents related to the patent -- was
16 that patent in '792 related to the patent here?

17 MR. LOWRY: I am unaware of -- if it was related. I can check on
18 -- and get back to you on surrebuttal. But neither party has alleged that it
19 was related. But I will say that, Your Honor, if program operation is clearly
20 known to a POSITA, as Petitioner proposes, then you would expect it to
21 have the same meaning in each setting, especially when you're talking about
22 the same prior art reference which is Costa.

23 In that prior testimony, Petitioner's expert characterized Costa as
24 having a program operation that occurs before the verify phase. And now
25 he's interpreting Costa in a different manner to say that a program operation
26 includes both charge injection and verify phase. And I think that goes

1 straight to the credibility of that testimony, Your Honor.

2 If I could jump to Slide 6, please. I'm just going to jump real back
3 -- right back to the '941 Patent for a minute. Your Honors, it begins with a
4 distinctly 3D NAND problem. As the number of layers increase and cells
5 are packed closer together in the vertical direction, two programming phase
6 problems become more severe, program disturb and pass voltage disturb.
7 The claims address this problem in context of a three-dimensional structure.

8 If we look at Slide 7, the '941 Patent solution, as described in the
9 specification, addresses those three-dimensional problems, the program
10 disturb and pass voltage disturbance. If we go to Claim 8 -- or Slide 8, this
11 solution is claimed. There is specific structure here and specific voltages.
12 Starting with the structure, the claim requires a first portion comprising the
13 word lines from bottom to top. Second portion, below the first portion,
14 comprising word lines from bottom to top. And then on Slide 9, we see the
15 voltages applied to which word lines all these are required by the claims.

16 Turning to Slide 10, Petitioner's Ground 1 has a core defect, which
17 I alluded to earlier. Dong does not expressly disclose the claimed vertical
18 word line arrangement. First, the claimed phrase from bottom to top should
19 be interpreted according to the plain ordinary meaning, such that it means
20 from lowest to highest. Second, Dong's Figure 5A and 5G are voltage
21 diagrams. They depict voltage schemes, not physical structure. When Dong
22 discloses structure, it does so in Figure 4. And Figure 4 shows a 2D array,
23 not the claimed vertical 3D arrangement.

24 Third, Dong's passing reference to three-dimensional does not
25 supply what the claims require. It does not expressly disclose where lines
26 arrange from bottom to top, as the claims recite, in order to anticipate. And

1 fourth, Your Honors, Petitioner invokes an at once envisaged theory for the
2 first time on reply to use POSITA knowledge to supply structure Dong itself
3 never discloses.

4 But anticipation doesn't work that way. The Nidec case makes
5 clear that a reference cannot anticipate by relying on what a POSA would
6 immediately envision to supply a limitation the reference itself does not
7 disclose. So however Petitioner repackages Dong on reply, the problem
8 remains the same, Dong never expressly discloses the claim vertical word
9 line arrangement and thus fails to anticipate.

10 Turning to Slide 11, I'll address the claim construction briefly,
11 Your Honors. I know Petitioner glossed over this, but this is a key issue in
12 this case. If we go to Slide 12, the patent uses bottom top in their ordinary
13 vertical sense; bottom means lowest, top means highest. That is how the
14 claims use those words, and that is how the figures depict them.

15 If we go to Slide 13, other claim --

16 JUDGE CYGAN: Counsel?

17 MR. LOWRY: Yes.

18 JUDGE CYGAN: When we're saying lowest to highest, what do
19 we -- what are we relating that to?

20 MR. LOWRY: We're relating it to a substrate, Your Honor.

21 JUDGE CYGAN: Okay. Is there a substrate discussed in the '941
22 Patent?

23 MR. LOWRY: No, the '941 Patent doesn't discuss substrate, but
24 there's unrebutted expert testimony from Patent Owner's expert, Dr. Khatri,
25 that Figure 8, for example, has -- a POSA that would read Figure 8 and
26 understand that in a three-dimensional sense there would be a substrate at

1 the bottom to provide a reference point. Those sites are Exhibit 2028,
2 paragraphs 85, 107, and 113. And again, they're unrebutted and not
3 contested by Petitioner.

4 JUDGE CYGAN: Figure 8 is, for example, shown horizontally,
5 right? I am simply wondering about how you're bringing in sort of the prior
6 art understanding. Because there's nothing of a substrate in the patent, and
7 certainly the patent states that the disclosure is limited only by the claims.
8 How should we understand your reference to the prior art to understand to
9 bring in all this the substrate has to be at the bottom and then everything is
10 over the substrate, and the substrate has to sit horizontally and everything
11 has to sit above it?

12 How do we understand your reference to the prior art and not have
13 the same understanding for the art that Petitioner is presenting? Is it simply
14 based upon the fact that your disclosure mentions 3D NAND and there are
15 references you're considering to not have the same type of 3D NAND? Is
16 that the difference that you're pointing to here?

17 MR. LOWRY: I want to make sure I understand your question.
18 Are you asking why -- well, let me say one thing real quick. It's that we
19 don't point to any prior art to say there's a substrate in the '941 Patent. That
20 is a POSITA understanding that's unrebutted in this proceeding, right? So
21 Dr. Khatri, Patent Owner's expert, said a POSA would understand there's a
22 substrate at the bottom of Figure 8, that would be the reference point, so that
23 the from bottom to top has a reference point when it's construed. We don't
24 point to any prior art -- unless I'm overlooking something, I'm happy to
25 address.

26 JUDGE CYGAN: So are you saying you have unsubstantiated

1 testimony?

2 MR. LOWRY: No, the testimony is not unsubstantiated, it's
3 un rebutted. I see what you're saying. So you're saying if the expert
4 testimony has to rely on something, and we're assuming that it would be
5 prior art. Is that the premise?

6 JUDGE CYGAN: So your expert testimony is based solely on the
7 reading of this patent, but it's also based upon the knowledge of how a
8 person of ordinary skill in the art would read it. Dr. Khatri made this the
9 statement; is that correct?

10 MR. LOWRY: Yes.

11 JUDGE CYGAN: And his statement is based upon reading this in
12 view of the ordinary skill in the art at the time -- at the appropriate time,
13 correct?

14 MR. LOWRY: Yes, that's correct.

15 JUDGE CYGAN: So it would be understood -- is this statement
16 that in general it's understood that 3D NAND would have a substrate at the
17 bottom and the strings going or is this -- because I seem to understand that
18 you're -- part of the dispute is that you could have 3D NAND -- instead of
19 the strings going straight up, they could be stacked in the other direction, and
20 that wouldn't meet your claims, correct?

21 MR. LOWRY: That's correct. That's one example, Your Honor.

22 JUDGE CYGAN: Okay. We have Dr. Khatri's evidence to say
23 that based upon -- what is Dr. Khatri making his distinction, about why these
24 have to be vertical stacks as opposed to horizontal stacks?

25 MR. LOWRY: Your Honor, I think it goes to the context of the
26 special -- specification, for example, which I was going through, which is

1 that the '941 Patent is directed expressly to three-dimensional problems. It
2 talks about the stacking of the cell and program and pass voltage
3 disturbance. Whereas another reference for example, Dong, doesn't have
4 those kinds of disclosures. And his disclosure is actually focused on a 2D
5 the horizontal style program disturb issues.

6 JUDGE CYGAN: One of the things which I'd like to understand
7 better is how that relates to the claims, which don't -- do any of the claims
8 mention program disturbance in them?

9 MR. LOWRY: No, Your Honor.

10 JUDGE CYGAN: So none of the claims mention a substrate or
11 program disturbance or 3D NAND or vertical NAND. They just mention
12 bottom to top. So I just want to make sure that we're basing essentially all
13 the dispute between Dong and the claims to Dr. Khatri's characterization that
14 these claims have to represent vertically-oriented strings of a 3D NAND.
15 And it's also his -- is it also his testimony that we're basing the fact that
16 Dong necessarily or would not obviously operate in that same manner, or are
17 we basing all this on Dr. Khatri statements?

18 MR. LOWRY: No, I don't think we're basing it all on Dr. Khatri's
19 statements. The context of the '941 -- not only from bottom to top, but
20 there's other claim language in there that has above and below in other
21 vertical references. That pushed the claims into a vertical structure. That, I
22 think, is undisputed under Patent Owner's construction from bottom to top.
23 And that matters here in the context of the '941 which is directed directly
24 right to three-dimensional vertical NAND issues and program disturb and
25 pass voltage disturbance.

26 And it goes on to say that I think in -- it's one of the last paragraphs

1 of the '941, which I can find for Your Honor. But it directly relates this
2 -- the claims to solving these issues. It is column 6 lines, 39 to 43, for
3 example. It says, "By using a memory section to have a plurality of portions
4 and applying voltages to the word lines of the memory according to the
5 portions, program disturbance and pass voltage disturbance may be reduced
6 according to simulations and experiments."

7 And that's referring right back to its discussion earlier about
8 addressing these three-dimensional issues, program disturbance and pass
9 voltage disturbance. Whereas if you look at the Dong reference, there's no
10 such disclosure like that. The only thing Petitioner can point to is a vague
11 three-dimensional statement, which I can address separately.

12 JUDGE CYGAN: I want to repeat my question I asked your
13 friends on the other side, which is that if you took the structure of Claim 1
14 and you tipped it on the side, it wouldn't -- those word lines would no longer
15 be in the bottom to top configuration. They'd be in a left to right
16 configuration. But wouldn't they still perform the program disturb
17 functions?

18 MR. LOWRY: Your Honor, are you referring to taking a -- like a
19 3D NAND structure and turning the whole thing on its side?

20 JUDGE CYGAN: Correct.

21 MR. LOWRY: That's one reason that the reference point's
22 important, as we talked about the substrate, is to understand that this
23 structure is not floating in the ether. There is a substrate there. A POSA
24 would have known there's substrate. There's unrebutted testimony to that.
25 But if it's on its side, it would no longer be from bottom to top. You
26 wouldn't have the vertical arrangement that's recited in the claims.

1 JUDGE CYGAN: Again, you're depending upon the testimony
2 from Dr. Khatri as to these things being relative to the substrate, correct?

3 MR. LOWRY: That's a portion, Your Honor. I'm happy to find
4 cites in Aritome or Micheloni, the bigger references, Exhibits 1009 and
5 1010, I believe, that repeatedly show the same thing. The substrates at the
6 bottom, 3D NAND goes up. If you look at the Petitioner's own examples of
7 this that they pointed to for the first time in reply, it shows the same thing,
8 substrate at the bottom. I think that it's very fair to say that a POSA would
9 have interpreted the claims in that context, rather than on the side which is
10 -- I haven't seen that in the record anywhere, Your Honor

11 JUDGE CYGAN: Is there anything that we should take from the
12 fact that the figures are all sort of described in sort of a vertical orientation,
13 and that the description of the figures is what -- is where we're getting the
14 bottom to top and the above and below? Can you explain why that language
15 in the claim isn't sort of a -- being brought down from the description of the
16 figures in this -- with the figures being more of a schematic view of it?

17 MR. LOWRY: I'm not sure I follow, Your Honor. Are you asking
18 that the figures themselves -- we should read the claims that the figures
19 provide some support as to the vertical nature of the claims?

20 JUDGE CYGAN: When we're looking at this patent, just to
21 clarify, since there's no structure that's given in it, there is an arrangement of
22 word lines, correct? But there's no discussion of drain lines or of substrates,
23 and so we have to understand that from the prior art. We have to understand
24 that this above and below is relative to the substrate. The question that I had
25 when I was looking through the claims is they seem to mirror the language
26 in the description of the figures. And the description of the figures doesn't

1 appear to be structural. I just want to see if you had a response to that.

2 MR. LOWRY: Yes, Your Honor. The specification itself is
3 -- addresses most of the figures. I'd say all the figures in there, right? So,
4 yes, there are -- there is mirrored language between the claims which have
5 support in the specification for specific figures. And you're right, there is no
6 mention of a source or a drain. There's no mention of every single structure
7 element in three-dimensional memory, but there is adequate support for what
8 the claims require, which is the top to bottom, from bottom to top
9 architecture.

10 And on Slide 15, you can see this. It's not just in one in one figure.
11 It's in all the figures. And it's not just when it's interpreting from bottom to
12 top. There's also above and below. On the right, you can see in red how it's
13 describing a -- how it's located in portion 910 above the lower most portion.
14 So this vertical nature of the claims is that's what the specification is driven
15 at, and that's what the claims are driven at as well. Does that answer your
16 question, Your Honor? I'm happy to elaborate if not.

17 JUDGE CYGAN: It does. And I think in your discussion, when I
18 let you proceed with it, you'll be discussing some of the technical reasons
19 why that makes a distinction, correct?

20 MR. LOWRY: Yes, Your Honor.

21 JUDGE CYGAN: Okay. Thank you.

22 MR. LOWRY: Circling back to from bottom to top, I'll just briefly
23 point out that other intrinsic evidence supported -- recited in the '941 Patent
24 itself support that bottom means lowest and top means highest. You can see
25 this in Dong 3, which is not the same prior art on reference that Petitioner
26 relies on. This further support that top and bottom being exactly what they

1 ordinarily mean, Your Honors. Slide 17 shows additional intrinsic evidence
2 that shows the same -- that makes the same point.

3 Now I just want to touch briefly on Slide 20 about Petitioner's
4 construction. In the petition, the construction was the source end of the
5 NAND string at the bottom and then drain end of NAND string at the top.
6 And then in reply, the construction shifted to indexed and programmed from
7 the source to drain. And now today, I heard Petitioners say that the
8 construction is just source to drain.

9 So I just like to level set and say this, none of those theories have
10 any support in the '941 path. Claims don't recite a source or drain. Figures
11 do not show a source or drain in the specification, never once used those
12 elements to define bottom and top. The Federal Circuit routinely rejects
13 such constructions, recognizing that broadening the terms of ordinary
14 meaning without supporting the intrinsic record violates principles
15 articulated in Phillips. Courts also do not to depart from the natural reading
16 of a phrase, absent clear lexicography or prosecution disclaimer, which the
17 Petitioner identifies neither here.

18 Now if we jump to Slide 22, Petitioner's new construction, this
19 indexing or programming from source to drain completely derives bottom
20 and top from any meaning. Under Petitioner's approach, from bottom to top
21 no longer refers to physical location at all. This is confirmed by Petitioner's
22 expert at the bottom. In deposition, he said it has nothing to do with the
23 physical level. Petitioner interprets bottom to top to mean source of drain
24 programming wherever the source and the drain happen to be.

25 So this sweeps in U-shaped NAND on the left where the source
26 and the drain are both at the top. It sweeps in the reverse arrangement, as

1 seen in the drain to source configuration in the middle, and it even sweeps in
2 two demand where the source is on the left and the drain is on the right.
3 Petitioner's construction doesn't give meaning different bottom to top. It
4 simply just deletes them from the claims.

5 I'll jump to Slide 27. Now I'd like to talk about Dong's figures,
6 which Patent Owner submits do not expressly disclose vertically arranged
7 word lines as recited. Now let's start with the standard here, because I think
8 there was some blending of anticipation obviousness during my friend's
9 presentation. Now anticipation is a high bar. One reference must disclose
10 either expressly or inherently every claim element arranged as the claim
11 requires. Petitioner has told the Board it's not relying on inherency. This is
12 in their reply.

13 So to anticipate here, Dong must expressly disclose the claimed
14 vertical architecture, reciting with word lines arranged from bottom to top.
15 But Dong does not. Dong's Figure 5A and 5G don't disclose the claimed
16 architecture, as the Board noted at institution, and Dong's single passing
17 statement that array can be three-dimensional is not an expressed disclosure
18 of every claimed element arranged as claimed required.

19 Let's look at the figures briefly. I'm on Slide 29. Dong's only
20 structural disclosure is Figure 4. And Figure 4's 2D with word lines ranged
21 horizontally, not vertically. Now Dong describes that a revised erase area
22 self-boosting mode, or REASB, like the one depicted in Figure 5C, is used
23 in the 2D architecture shown Figure 4. And as shown, you can see that the
24 voltages correspond here between Figure 4 and Figure 5C.

25 Now if we go to Slide 30, Dong says also what Figure 5A and 5G
26 are. They are different examples of self-boosting modes; modes, not

1 structures. Those figures describe voltage conditions. They do not redraw
2 the memory architecture. The fact that voltages are stacked vertically in
3 Figure 5A and 5G does not turn Dong's horizontal word lines into vertical
4 ones. When Dong discloses structure, it does so in Figure 4, as we saw and
5 is on the screen, which shows a 2D array with horizontal word lines.

6 Now Dong's own specification confirms that reading. You don't
7 have to take my word for it. If we go to Slide 31, Dong repeatedly ties
8 Figure 5A and 5G to the 2D physical structure shown in Figure 4. Paragraph
9 5 here is a good example. There Dong explains that EASB and REASB
10 boosting mode shown in Figure 5A, Figure 5G apply an isolation voltage, V
11 ISO in orange, to source side neighbors of the selected word line. And in
12 explaining that operation, Dong points directly to Figure 4 structure, says the
13 channel area of substrate 490 on a source side of the isolation word line, 412
14 in red, seen in Figure 4 is isolated from the drain to side channel area.

15 Now that matters, right? Because when Dong discusses these
16 figures, Figure 5A and 5G which Petitioner relies on, it expressly refers back
17 to Figure 4 structure. And it's also important to take away here, Your
18 Honors, that Petitioner never disputed this connection. They also never
19 disputed on Slide 32 the connection in Dong's paragraph 67, which confirms
20 the same point. When Dong discusses the EASB and REASB modes shown
21 in Figure 5A and 5G, it explains them by reference to Figure 4 structure,
22 again.

23 In this paragraph, Dong describes a hot carrier injection
24 phenomenon. Dong says that with EASB and REASB, as discussed, the
25 memory string is separated through source and drain sides by applying an
26 isolation voltage, V ISO shown in orange. And in that context, Dong

1 describes that if the boosting potential differs significantly between the
2 source and the drain sides, a hot carrier injection can cause program disturb.

3 Now in that same paragraph, Dong depicts this hot carrier injection
4 issue in Figure 4 structure with the electrons in purple moving across the
5 isolation storage Element 412 in red and into the floating gate of storage
6 Element 410 in blue. So again, Dong's specification ties Figure 5A and 5G
7 back to Figure 4's 2D structure. And again, Petitioner does not dispute that
8 connection.

9 If we go to Slide 34, Your Honors, we heard a lot about how these
10 pictures look similar. What we didn't hear a lot about was the description of
11 those figures. And when you look at those descriptions, they tell a clear
12 story, the figure -- '941 figure is structure, it shows a memory 700 that
13 depicts the physical memory with vertically arranged word lines. Dong's
14 Figure 5A, for example, is not structural. It depicts a self-boosting mode, as
15 Dong says itself. That's a voltage scheme. And again, Dong ties that
16 voltage scheme back to Figure 4 structure.

17 If we go to Slide 33, Petitioner mistakes a vertical drawing for a
18 vertical device, Your Honors. Dong's Figures 5A and 5G do not disclose
19 vertical word lines any more than a vertically drawn two median schematic
20 on the left in green. In both cases, the circuit schematic on the left in green
21 and Dong's voltage charts are illustrated vertically, but the disclosed
22 structure is not.

23 Sorry, that was 33, Your Honor. Turning to Slide 35, turning to
24 Dong's three-dimensional language, Petitioner's argument fails as a matter of
25 law. Dong's statement that the array of storage elements can be three-
26 dimensional does not anticipate claims requiring vertically arranged word

1 lines. First, there's no -- it's not an express disclosure of vertically arranged
2 word lines. And second, A POSA would not interpret Dong's three-
3 dimensional language as referring to 3D architectures with word lines
4 arranged vertically. A POSA would interpret it as referring to word lines
5 arranged horizontally.

6 If we go to Slide 36, now Dong's mere of statement three-
7 dimensional does not expressly disclose the claims, which require the
8 memory portions arranged from bottom to top. As a result, the recited
9 vertical arrangement is missing from Dong. It is not in the Figures 5A or 5G
10 nor is expressly disclosed by this language. On 37, Petitioners theory
11 depends on adding words to Dong, such that Dong discloses expressly that
12 the storage elements can be three-dimensional with vertical word lines.

13 But Your Honors, Dong does not say that, and there's a good
14 reason why. As Patent Owner's expert testified, a POSA would have
15 interpreted Dong's three-dimensional language as referring to 3D
16 architectures with word lines arranged horizontally. On Slide 38, these
17 horizontal-based 3D memory arrays, such as stacked NAND and multilayer
18 TFT architectures, were made up of stacked layers of horizontal 2D NAND
19 arrays. So they're like pancakes stacked on top of each other.

20 Now those structures were unquestionably three-dimensional, but
21 their word lines were still horizontal, not arranged vertically from bottom to
22 top as the claims required. That is also consistent with Dong's actual
23 disclosure, which is directed to 2D-based program disturb techniques.

24 Now if we go to Slide 39, Your Honors, at bottom, even giving
25 Petitioner the benefit of the doubt, Petitioner's theory still fails. In *Wasica*,
26 the Federal Circuit held that a disclosure of a broad genus, "any modulation

1 scheme," quote, unquote, which includes a constant frequency does not
2 anticipate the claimed species constant frequency.

3 The same is true here. Even taking Petitioner's argument at its
4 highest, Dong's generic reference three-dimensional memory does not
5 expressly disclose the species of vertically arranged word lines as recited
6 under -- as recited to meet an anticipation standard. And Petitioner never
7 built the factual record required to make a genus species theory in the first
8 place, never identify the relevant genus to find any species within it, or show
9 disclosure of that species with the required specificity. If we go to Slide 40.

10 JUDGE CYGAN: Counsel, is there any evidence on the record of
11 how many species there are of 3D NAND?

12 MR. LOWRY: Yes, Your Honor. Now again, I just want to point
13 out that Petitioner never made this argument. But there is evidence in the
14 record supporting that there's numerous species. Now neither party has gone
15 out and said, here's the defined set of species. But the record does show
16 multiple, which I'll give you some examples.

17 JUDGE CYGAN: Thank you.

18 MR. LOWRY: So the record shows many different 3D NAND
19 configurations exist, many of which do not disclose a vertical arrangement
20 of 32 cells in a 3D NAND context. And I just want to make clear why I said
21 32 cells. Because that's what Petitioners position is, right? If you look at
22 their petition, they say we would have had Dong at 32 cells, 32 cells tall
23 -- sorry, 32 cells in horizontal, and then we would have turned that to
24 vertical.

25 Now there are other configurations, for example, the -- we talked
26 about the stacked NAND and multi-TFT NAND. Petitioner raised straight

1 vertical channel NAND cells with four memory cells. That's not 32
2 NANDs. That's not 32 memory cells such that it anticipates U-shaped
3 NAND, including a snaking vertical, as well as one with of the transistor at
4 the bottom. That's shown in Exhibit 2012 and Exhibit 2016 -- at Figure 3
5 and 2016. There's also a different kind of gate, the vertical gate, lateral
6 channel NAND. That's Exhibit 1009, at Page 32.2.

7 The SGT cell has a diagonal structure with the word lines moving
8 side -- from left to right. That's Exhibit 1009, at Page 294. And then
9 Exhibit 1009, at 293, it shows many different kinds of 3D NAND cells, and
10 it shows a snapshot from 2006 to 2012.

11 JUDGE CYGAN: Can you point me to the evidence that links the
12 disclosure in the '941 Patent to simply one type of that, the vertical only, as
13 opposed to any of the -- as opposed to including any of the other types?

14 MR. LOWRY: Yes, Your Honor. I would first point to column 1
15 at lines 26 through 41, which describe the stated aim of the patent to address
16 specific three-dimensional issues. And it says here that -- in line 30, a three-
17 dimensional structure of memory can include a polarity of layers so as to
18 store more data on the same area. But as those number of layers increase,
19 program disturbance becomes -- or program disturbance comes an issue, and
20 so does pass for voltage disturbance. So solution for reducing those two
21 things is a need in the field.

22 And then it goes on to describe throughout the specification this
23 vertical arrangement from bottom to top. As I showed on the previous slide,
24 many portions of the specification use terms like above and below,
25 lowermost, uppermost to describe relationships between different portions.

26 JUDGE CYGAN: Let me make sure I understand this --

1 MR. LOWRY: Yes.

2 JUDGE CYGAN: -- correct, so the fact that this is a 3D vertical
3 stack is based upon the testimony of Dr. Khatri. We have a number of 3D
4 stacks which are present in the art, which might be covered by the prior art,
5 covered by Dong and -- instead of the vertical type. Because when we're
6 looking at Dong, we're looking at a 3D one. But your argument is that Dong
7 doesn't have the particular one.

8 But the reason why we would know that your patent has the
9 vertical stack is because it mentions above and below. But we know above
10 and below refers to the substrate because it's a vertical stack? I'm trying to
11 understand why at some level this isn't sort of a circular argument here.

12 MR. LOWRY: Yes, Your Honor. So I think one piece that may
13 have been missing there was that the claims directly recite these portions in
14 relation to each other. So it says a memory, for example -- and I'm
15 paraphrasing here, a memory with a portion, a first portion above or below a
16 second portion. And then it recites those specific word lines in those
17 portions and voltages applied to those word lines. So you have already some
18 structure there that requires the verticality.

19 Now the specification has additional evidence that not only
20 supports that, but it also describes portions in lowermost locations,
21 uppermost locations. It says this portion can be above that portion or below
22 another portion. So you have repeatedly this vertical arrangement recited
23 throughout. Now you add to that the stated aim of the patent to address
24 these characteristically three-dimensional issues. The patent expressly says
25 these are issues that come up when you start stacking layers too high in
26 three-dimensional -- in the three-dimensional direction. And that clearly

1 paints a picture in Patent Owner's mind of this vertical structure.

2 And then you have unrebutted testimony from Dr. Khatri, who
3 says a POSA would have looked at Figure 8, for example, and recognize that
4 there's a substrate at the bottom. I haven't seen an opposite -- any sort of
5 reference to the contrary, Your Honor. And it's shown again in references
6 like Aritome and Exhibit 1010, Micheloni, which I can I'm happy to pull for
7 you for surrebuttal.

8 JUDGE CYGAN: Thank you.

9 MR. LOWRY: So we're just discussing that Petitioner had not
10 made any sort of genus species theory. But there's another reason why the
11 three-dimensional language doesn't work here. It doesn't expressly disclose
12 vertical word lines as recited. On Slide 40, at minimum, Dong's three-
13 dimensional language is ambiguous. In the Federal Circuit's Hill, that
14 ambiguous references do not anticipate a claim.

15 Remember that we are under an anticipation standard here. We
16 need expressed disclosure. You can't have an extra step from the disclosure
17 within the four corners of the reference to something else to bring in other
18 disclosures using either prior art or a POSITA's knowledge.

19 In *Wasica*, the Federal Circuit recognized that a prior reference
20 disclosed signals that could be either constant or non-constant frequency. It
21 could be one or the other. But the Federal Circuit affirmed the Board's
22 finding that this ambiguous disclosure did not anticipate a claim reciting
23 constant frequency.

24 So just to recap, the reference said it disclosed signals with
25 constant or non-constant frequency, and still that was ambiguous enough to
26 not anticipate a recitation of constant frequency. So here, even giving

1 Petitioner the benefit of the doubt, Dong's use the three-dimensional could
2 refer to more than one type of architecture, including the 2B -- 2D based 3D
3 arrangement with horizontally ranged word lines.

4 Now I want to turn to Petitioner's new envisage theory. On Slide
5 42, for its new theory, Petitioner turned to *Kennametal* and said a POSA
6 would have once envisage the claimed invention. But that narrow line of
7 cases does not do the work Petitioner needs it to do here. It was also never
8 in the petition, Your Honors. This is a new argument we see for the first
9 time on the fly.

10 If we go to Slide 43, now *Kennametal* was a closed list case.
11 There the reference actually disclosed five binders and three coatings, and it
12 taught that any disclosed binder could be used with any disclosed coating.
13 This is really important, Your Honors, this highlighted section says because
14 all the limitations of *Kennametal*'s claim were specifically disclosed in the
15 prior reference, the Court found that a POSA would at once envisage the
16 recited combination used one of five disclosed binders.

17 So it was all there already in the reference. But Dong is the
18 opposite. Dong's passing reference to three-dimensional is not a closed list.
19 It's open ended, undefined. And Petitioner never laid the groundwork of the
20 record to say otherwise.

21 If we go to Slide 44, *Nidec* is also key here, Your Honors. It
22 squarely rejects Petitioner's new theory. The Federal Circuit drew a clear
23 line there, and it recognized *Kennametal* involved a limited set of disclosed
24 combinations. It does not let a Petitioner take a reference that is missing the
25 claim limitation and salvage anticipation by saying a skilled artisan would at
26 once envisage it.

1 As made it clear in *Nidec*, where the specific claim feature is not
2 expressly disclosed, it cannot be filled in for anticipation purposes even if a
3 POSITA could at once envisage it. That's exactly what Petitioner is trying to
4 do here. Dong's Figure 5A and 5G do not expressly disclose the recited
5 vertical word lines and neither does the three-dimensional language.

6 Now, one other issue, Your Honors, that Petitioner's problem is not
7 just legal; it's evidentiary. Petitioner's expert did not apply the *Kennametal*
8 standard. He applied a different one. What he says, A POSA would right
9 away visualize in 2020. But that's not the test. *Kennametal* requires
10 disclosure of the limitations at issue. And that analysis is missing here
11 because that expert applied the wrong standards. Testimonies apply is
12 -- should be given a little weight here.

13 On Slide 46, Petitioner can also not patch Dong with separate
14 references or background materials. Anticipation must come from a single
15 reference. Now Petitioner is asking the Board to supply through POSA the
16 knowledge a vertical architecture Dong never discloses. That's obviousness.
17 That's not anticipation. And even those outside materials do not get
18 Petitioner there because they at most a short silicon pillar structure, which is
19 a far cry from Dong expressly disclosing 32-word lines vertically arranged.

20 And on Slide 47, the Federal Circuit rejected the same move in
21 *Galderma* and refused to turn a second -- turn to a second reference for a
22 very specific teaching to use it to incorporate specific disclosure not found in
23 the primary reference. Your Honors, Patent Owner submits that's exactly
24 what's happening here.

25 Now if we go to Slide 49, I want to turn to why Ground 2 fails as
26 well, the obviousness position. On Slide 51, Petitioner never argued in its

1 petition that it would have been obvious to apply Dong's voltage schemes of
2 Figure 5A and 5G in a 3D NAND context with word lines arranged from
3 bottom to top as the claim requires. It said the opposite. It said Dong
4 discloses it, relying on Dong's Figure 5A and Dong's three-dimensional
5 language. That's a disclosure theory. It's not an obviousness theory.

6 And on Slide 52, the only Ground 2 obviousness modification the
7 petition identified was using a 32-cell memory string in Dong's horizontal
8 structure. That's a different point entirely and is completely unrelated to the
9 limitation from bottom to top. Petitioner's generic obviousness theory for
10 Ground 2 just saying that these claims are obvious cannot provide carte
11 blanche to raise obviousness for any limitation.

12 Now the petition referenced Shirai and Righetti to support
13 obviousness regarding this 32-cell memory string, not for a vertical word
14 line arrangement. And that was confirmed, we can see on Slide 53, by
15 Petitioner's expert who admitted that Shirai and Righetti were cited for a
16 narrow purpose, to support the use of the 32-cell memory string.

17 Now on slide, 54 Petitioner also points to the petition's generic
18 background section, not part of the argument section at all. He's saying this
19 supports obviousness. But that too fails scrutiny. That background section
20 never provides a claim's specific reason to modify Dong's to the architecture
21 into the claimed vertical architecture. In fact, it never mentions Dong or the
22 relevant limitation at all. The petition needed a specific reason a POSA
23 would modify Dong's 2D disturb to apply in the vertical word line
24 architecture, but that's missing here.

25 On Slide 55, you can see that it's generic because it's in five other
26 IPRs, Your Honor. It's stock language repeated across other of my

1 competitions. It's not a motivation to combine specific to the from bottom to
2 top limitation. Petitioner also leans on in Slide 56 conclusory expert
3 testimony, which cannot provide the requisite motivation.

4 If we go to Slide 58, I want to jump forward and talk about even if
5 the Board does not agree with me that Patent Owner never -- or Petitioner
6 never raises obviousness theory, that it still fails for two main reasons. First,
7 Dong only solves part of the problem. Dong addresses only two
8 conventional program disturb modes. The 3D NAND with vertically
9 arranged word lines presents four. Even on Petitioner's own theory, Dong
10 does not solve the full program disturb problem a POSA would face in 3D
11 NAND.

12 Second, vertical 3D NAND has a natural local sub boosting effect.
13 And that inherent behavior already provides sufficient boosting to avoid
14 program disturb without conventional 2D local sub-boosting techniques like
15 those in Dong.

16 JUDGE CYGAN: Counsel, how much program disturbance does
17 the claim require to be reduced?

18 MR. LOWRY: The claim itself doesn't have a specific
19 requirement for the reduction of -- a specific amount of reduction of
20 program disturbance or pass voltage disturbance.

21 JUDGE CYGAN: Thank you.

22 MR. LOWRY: Petitioner's theory runs into a technical problem,
23 though. Now the program disturb mechanisms of 3D NAND cells are much
24 different from that of 2D NAND cells because the cell structure and array
25 architecture are totally changed. Now this is from Petitioner's own evidence,
26 and there's a reason why this is here. This is right before discussing program

1 disturb. When you get into program disturb, you understand that 3D NAND
2 introduces program disturb modes that are not present in 2D NAND.

3 During program in 3D NAND, the program X, Y in X, Y disturbed
4 modes all occur simultaneously. That's a key point. They're happening at
5 the same time. Petitioner's own expert admitted that all four must be
6 addressed for 3D NAND to reliably operate during programming. So you
7 could stop there. Because Dong only addresses two of the four, a POSA
8 would not be motivated to use it in 3D NAND because it would be able to
9 reliably operate programming therein.

10 On Slide 661, Dong's 2D methods address only two conventional
11 program disturb modes, shown in green. Vertical 3D NAND, as mentioned,
12 provide four relevant disturbed modes: the two in green, plus the two in red.
13 So even on Petitioner's own theory, Dong does not solve the program
14 disturbs presented by vertical 3D NAND. It leaves red nodes unaddressed.

15 And I want to address something briefly, Your Honor, that -- I
16 think based on your question earlier, Judge Cygan, about whether a single
17 string would satisfy the claims. Now when you put a 2D NAND string into
18 3D NAND, I understand what you're saying as far as Dong would go that
19 you can just focus in -- hyperfocus on that one string and do the analysis
20 there. But what's important to note here is that you see this dotted line here
21 that stretches between strings one, two, three, and four, that dotted line is the
22 voltage that you must apply to all the strings at once.

23 So you can't pluck out one string and say, okay, we're going to do
24 the analysis here, Dong satisfies it, that's it. Because in 3D NAND, you
25 have to address all the strings at once with the voltages. And now this is
26 supported in Exhibit 2028, paragraph 76, which is Patent Owner's expert

1 saying the same thing.

2 If we go to Slide --

3 JUDGE CYGAN: Counsel, how many of those strings are
4 represented and required by Claim 1?

5 MR. LOWRY: I would say Claim 1, Your Honor, requires -- it
6 requires a memory with at least one string.

7 JUDGE CYGAN: So how does Claim 1 require the different type
8 of program disturb then would be represented by a single string in Dong?

9 MR. LOWRY: So Your Honor, I think these are two separate
10 issues as far as -- what Petitioner is trying to do here to meet their burden is
11 to take Dong and turn it vertically and use it in a 3D NAND sort of
12 environment, right? This vertical 3D NAND you hear him say over and
13 over again, three-dimensional is well-known. that's -- this vertical was
14 ubiquitous in 2020. So that's what we're doing here for Dong. And what
15 Patent Owner's position is that Petitioner never meets their burden here.
16 Because when you're looking at Dong, you wouldn't take that structure and
17 that program disturb mitigation method and put it in 3D NAND. That's the
18 main point.

19 Now I recognize what you're saying about the '941 claims. But I
20 think in order -- the real issue here is for Petitioner to meet their burden.
21 They have to show that a POSA would have been motivated to do that. And
22 on the record, I haven't seen -- I'm obviously biased, Your Honor, but I
23 haven't seen anything that rebuts these positions in a material way.

24 JUDGE CYGAN: So your arguments about Dong only meeting
25 two of the four program disturb modes, first, that's based on them meeting
26 them in a horizontal structure, correct? They would meet two of the four

1 program disturb modes not in a vertical structure, but when it's laid down, as
2 -- which you're contending the Dong reference is, which is a horizontal one,
3 correct?

4 MR. LOWRY: That's correct, Your Honor.

5 JUDGE CYGAN: Okay. So even in Dong's 2D methods, they do
6 address two program disturb modes. And your argument, if I understand it
7 correctly, is that you would never put them into a vertical form because you
8 wouldn't be addressing any additional program disturb modes. And
9 Petitioner's argument for why you move it from a horizontal to a vertical is
10 that you are addressing disturbed modes -- additional disturbed modes.
11 Because that wasn't what I was understanding Petitioner's argument to be
12 about why they would move Dong's into a vertical orientation.

13 MR. LOWRY: Right. And my understanding is they're saying,
14 look, there's four disturbed modes here; Dong covers two, that's all you need
15 to know, case closed. But the reality is all these four disturbed remotes, they
16 happen at the same time. So you can't just ignore and say, okay, for strings
17 three and four, I'm just going to go ahead and apply Dong and just have
18 program disturb there. You're basically deciding to do that. A POSA there
19 wouldn't be motivated to do that. They'd be motivated to address all this at
20 once. There's no dispute that all these modes happen simultaneously, and
21 they all have to be addressed at the same time.

22 JUDGE CYGAN: And your argument is that -- is not that Claim 1
23 requires four program disturb modes. Your argument is that any -- a person
24 of ordinary skill looking to Dong would not make that orientation change,
25 correct, regardless of what the claim requires?

26 MR. LOWRY: That's correct, Your Honor. It's Petitioners burden

1 to show that a POSA would have been motivated to turn Dong's horizontal
2 32-word lines into a vertical architecture. And there's a huge gap there. And
3 a POSA would not do that. And so Petitioner never meets their burden,
4 that's our position.

5 JUDGE CYGAN: Thank you.

6 MR. LOWRY: Briefly on Slide 62, there's another independent
7 reason why a POSITA would not be motivated to apply Dong's 2D program
8 to certain methods in vertical 3D NAND. It's because the structure is
9 different. 3D NAND on the right has this ultra bit thin body structure. And
10 the 2D NAND structure on the left, all the word lines are connected to the
11 substrate. And there's a practical effect from that. In 3D NAND you have
12 this natural, local self-boosting mode.

13 And if we go to Slide 63, we can see why that matters. And I'm
14 going to read from these because these are important. It says, "The NLSB
15 effect does not require the local boosting scheme used in conventional 2D
16 NAND like Dong." In Kang, in the bottom left, it says, "The NLSB effect
17 allows a sufficiently highly boosted potential of an inhibit string to be
18 achieved without a local sub-boosting program inhibit scheme like Dong."
19 So to put differently, the 3D NAND vertical architecture already has local
20 sub-boosting naturally built in. Dong's 2D sub-boosting methods are
21 designed to create that same boosting, and you don't need them when it's
22 already there.

23 I just want to touch briefly on Slide 66, Your Honor. There was
24 no reasonable expectation of success in the petition. It was just missing.
25 Patent Owner pointed that out on response. And in reply, now we have new,
26 reasonable expectation of success positions. But even on reply these

1 positions also fail. Petitioner never addresses why a POSITA would have
2 had a reasonable expectation of success in applying Dong's 2D NAND
3 program disturb methods in a vertical 3D NAND context.

4 I'd like to touch on Ground 3 briefly, Your Honor. I think I only
5 have time to maybe address the program operation, or I can address the
6 merits, Your Honor. Do you have a preference?

7 JUDGE MCGRAW: I think we can give you a few more minutes
8 to address both.

9 MR. LOWRY: Okay. So I'd like to turn to Claims 8 and 9 in
10 Ground 3. For Claims 8 and 9 in Ground 3, Petitioner relies on the Dong
11 and Costa references. Now Claims 8, 9 start from the same framework.
12 Independent Claims 5 define the first portion shown in blue as the word lines
13 from the first word lines of the CapWords line. Claim 5 then requires
14 applying a first voltage to the first word line, to the X minus two-word line.
15 Now Claims 8 and 9 further require the first voltage has a first level if the X,
16 Y line is in the first portion. That's required by both those claims.

17 Claim 8 adds that the first voltage has a third level if the X word
18 line is in the third portion shown in pink. Now why does this matter? If you
19 go to Slide 70, Ground 3 fails at the outset because Petitioner's own mapping
20 does not work. As seen on the left, Petitioner defined X as four, placing the
21 X word line on WL3 in the second portion. At the same time, Petitioner
22 defined the first portion as the first two-word lines, but Petitioner never
23 mapped the X portion in the first -- sorry, the X word line in the first portion.

24 And to be in the first portion, as Petitioner defined it, the X word
25 line would need to be one of those first two-word lines. But that would
26 violate the claims because Claim 5 requires that X is greater than or equal to

1 three. So, the first portion limitation is just -- it's not just missing from the
2 Petition. It's impossible under Petitioner's on mapping. So Ground 3 fails
3 for both Claims 8 and 9 cleanly for that reason.

4 I want to point out one thing, Your Honors. We saw very briefly
5 on Slide 6 and 7 Petitioner pointed to the original mapping, and then we
6 never saw it again. We never saw it again. I think that tells a story, right?
7 They have moved on from their original mappings because they're deficient.
8 If we go to Slide 71, Claim 8 fails for another reason independently. The
9 petition never mapped the requirement that the X word line is in the third
10 portion. It's just not in the petition.

11 If we go to a program operation --

12 JUDGE MCGRAW: Before you move on to that, what about
13 Petitioner's argument that they did provide mapping for Claim 8 when they
14 said that the first and second portions each have 16-word lines and they
15 stated that in their petition?

16 MR. LOWRY: I'm not aware of that in their petition, Your Honor,
17 where they said the first and second portion have 16-word lines. I recall
18 their --

19 JUDGE MCGRAW: They said the NAND string would be
20 divided into two equal zones. And since it's a 32-word line, half of 32
21 would be 16. So each section -- or each portion is 16-word lines.

22 MR. LOWRY: Are you are you referencing for Claims 8 and 9,
23 this combination for --

24 JUDGE MCGRAW: Yes.

25 MR. LOWRY: Okay.

26 JUDGE MCGRAW: It's their reply, Page 27.

1 MR. LOWRY: Okay. Your Honor, I will take a look at that and
2 be back on surrebuttal for that point. What I will say, Your Honor, is that
3 for that specific -- where they address Claims 8 and Claim 9, they're using
4 -- I'm just going to jump to Slide 96. They're using Dong and Costa in a way
5 that doesn't match their motivation to combine. Their motivation to combine
6 is we're going to take Dong to address the program charge version, the
7 section of that, of what they call the program operation, and we're going to
8 use Costa to address the verify operation.

9 But then when you look at how they're applying it, they're saying
10 that if you take each claimed portion in Dong as one of Costa's zones, the
11 claimed voltage, Dong's V pass, can change as it goes up the portions.
12 There's no motivation to combine to change Dong's V pass, according to
13 Costa's teachings. Again, their motivation to combine was using the two
14 separate teachings, one for program as in charge injection and one for verify,
15 not using Costa to modify Dong. And that's clear on the left, you can see the
16 highlighted language supports that. So let's go to

17 Let's go to Slide 79, please. I'm just going to touch briefly on the
18 intrinsic evidence supporting that a program operation does not include
19 verify. And here's what Petitioner didn't show you, which is the intrinsic
20 evidence. They pointed to Costa. They pointed to Dong. They never
21 pointed to the intrinsic evidence of the '941 Patent to try to construe a
22 program operation. If they did, they would see that the '941 Patent never
23 mentions a verify phase at all.

24 The '941 Patent describes a program operation as an operation for
25 programming a memory cell, then explains what that means. When the X
26 word line is used to perform a program operation, a program voltage,

1 VPGM, is applied to the X word line, then goes on to explain how other
2 voltages are applied.

3 Now if we go to Slide 80, you'll see this reflected in the claims
4 which recite applying voltages when an X word line is used to perform a
5 program operation. Now Slide 81 is an interesting point here, Your Honors,
6 that the context is important when we look at the stated aim of the '941
7 Patent. The aim is to reduce program disturb and pass voltage disturb on the
8 unselected word lines when a program voltage is applied.

9 Now as Patent Owner's expert testified on the right, the program
10 disturb and pass voltage disturb issues only occur during the actual
11 programming step. So not the verify step. And Petitioner does not dispute
12 that both program disturb and pass voltage disturb only occur during the
13 charge injection phase.

14 Now if we go to Slide 83, on the left you can see that the petition
15 also supports Patent Owner's interpretation to program. They say that to
16 program a particular NAND memory cell in the memory string, a high-
17 voltage Vpgm is applied to the word line connected to the cell, known as the
18 selected word line. This reflects what Aritome, their own reference, says
19 about the program operation. It's performed by applying a high voltage
20 Vpgm, just like the '941 Patent, Your Honor.

21 And I just want to make one more brief point, Your Honors, before
22 I sit down. On Slide 95 there was some discussion about Costa disclosing
23 this pass voltage. But the word admitted, that's really key here, is it's
24 actually a read pass voltage occurring during a verify phase. This is
25 confirmed by what Costa says in Petitioner's own expert. Costa is directed
26 to verify, not programming.

1 Petitioner's own expert admitted that point in the middle box here
2 on the right. Costa teaches adjusting voltages for verify operations alone.
3 Costa's text confirms it, saying that during sensing -- and I'm in the abstract
4 -- a selected memory cell receives a reference voltage while the remaining
5 memory cells receive a read or verify pass voltage. Unless there are any
6 questions, I'll reserve the remaining of my time for rebuttal.

7 JUDGE CYGAN: I have you at five minutes into your surrebuttal,
8 which was originally for 15 minutes.

9 And Petitioner, I have you at 17 minutes for your rebuttal. And
10 you may begin when ready.

11 MR. JENSEN: Thank you, Your Honor. I'd like to begin with the
12 program operation issue. And let me direct Your Honors to the '941 Patent
13 itself. This is at column 3, lines 6 to 8. And I need to, sorry, drag that onto
14 the screen here so we can see that. The '941 Patent itself says a program
15 operation set in the text may be an operation for programming a memory cell
16 form using, for example, a set of transistors. Petitioner submits that to
17 program a memory cell plainly means to store a bit of data on the memory
18 cell. That's what the memory cell does. That's what it's for. That's what it
19 means to program a memory cell through a program operation.

20 The fact that Dr. Liu in other proceedings use the terms -- first off,
21 Dr. Liu did -- first off, the term program operation has not been construed, to
22 my knowledge, in any of the other IPR proceedings. It is not a limitation in
23 a claim that has been in dispute. There has been some discussion of
24 programming, program operation, et cetera, in the other proceedings. Every
25 time that Dr. Liu testified about that, he discussed both a charge injection
26 and a verification phase or operation.

1 On occasion, he used the term operation. He could have said the
2 -- programming and memory cell or a program operation has two parts, two
3 phases, two aspects. On occasion, he said it has two operations. And I
4 would submit to Your Honors that where the term -- the specific term
5 program operation was not in dispute. It was a different patent, all of that
6 stuff. That the occasional use of the term operation instead of phase, part, or
7 aspect is a distinction without a difference. And there is no inconsistency,
8 Dr. Liu testified in every instance that there are two aspects, two parts, two
9 phases, two programming and memory cell, charge, injection, and
10 verification.

11 Let me direct Your Honors to -- on the issue of program operation
12 to our reply brief. This is at Page 26. And this has to do with programming
13 a word line in different portions of a memory string. And we quote both
14 Dong and Costa here that disclose -- you program all the cells in a memory
15 stream. And it would be not only manifestly unjust but incredibly incorrect
16 to say that Petitioner's theory was limited to programming only one cell in
17 the memory stream. Dong says, programming continues sequentially until
18 all memory cells are programmed. Costa in its abstract states, programming
19 progresses through all memory string cells.

20 Petitioner's theory was never restricted to programming only the
21 -- whether you call it the X equals 4 or the X equals 12, or the X equals 17th
22 word line. Rather, our theory encompassed programming a memory string.
23 And that's not only in our reply brief, but I would direct Your Honors to the
24 petition at Page 31, for example, where we say, as disclosed by Dong Figure
25 10, we point to the particular steps, programming continues sequentially
26 until all memory cells in a string are programmed.

1 There is no way that Petitioner's invalidity theories for Claims 8
2 and 9 were somehow limited to programming only one memory cell. And
3 that's just an artificial construct that the Patent Owner proposes to try and get
4 itself out of a box, knowing full well that all the cells in memory string are
5 programmed.

6 Let me turn to one of petitions -- changing topics now, I want to
7 talk about the bottom to top issues and the vertical memory strings. If we go
8 to Petitioners -- excuse me, Patent Owner's slides, let me see if I can pull
9 that up, Slide 37. Okay. Here we go. So this is Patent Owner's Slide 37.
10 And paragraph 95 is Dong's on the left where it has the three-dimensional
11 memory disclosure. And they say, oh, you're -- Petitioner is trying to
12 somehow add the words or read in this concept of with vertical word lines.

13 To begin, the claim doesn't say with vertical word lines. The claim
14 doesn't say anything at all about three-dimensional memory, let alone three-
15 dimensional memory with vertical word lines.

16 JUDGE MCGRAW: What about Claims 5's language regarding
17 above and below in other claims?

18 MR. JENSEN: So with respect to the above and below language,
19 that language is derivative of the bottom to top language. So the bottom to
20 top language is introduced first to provide a relative reference for where
21 these word line groupings are. And once you have established bottom to
22 top, which we submitted source to drain, of course it makes sense to refer to
23 word lines as being either below, i.e., the bottom or above; i.e., toward the
24 top. So it's simply an extension of the same argument. And it conflates to
25 the same thing, whether bottom to top means source to drain or whether it
26 requires a vertical orientation.

1 Let me expand on that a little bit by going to Slide 100 -- or let me
2 say Slide 99 addresses the above and below. We say the above and below
3 language simply reflects relative locations in a memory stream already
4 indexed from bottom to top, which we submit means source to drain. And in
5 this respect, I think it's significant that Dr. Khatri at his deposition agreed
6 that the purpose of the figures in the '941 Patent was to simply show -- as he
7 said they're variable names and they're relative orientations.

8 That's the purpose of this figure, right? The patent is interested in
9 the voltages you would apply to those word lines. The figures were not in
10 any way, shape, or form intended to restrict the patent, let alone the claims to
11 any particular memory -- physical memory structure, whether that's
12 horizontal or vertical memory lines.

13 JUDGE CYGAN: Counsel, to the extent that that accounts for the
14 language in Claim 5 about the word lines being order from bottom to top,
15 what accounts for the recitation that the second portion is above the first
16 portion?

17 MR. JENSEN: I'd submit that that falls into the same bucket, Your
18 Honor, that you have to be able to define those relative to one another. And
19 the way to do that is by knowing what is considered to be the bottom and top
20 of a memory string.

21 JUDGE CYGAN: Why isn't it a reasonable interpretation to say
22 that, as in Claim 5, the memory comprises the first portion and the second
23 portion and that the memory being a physical thing, the two portions of it are
24 physical things?

25 MR. JENSEN: Yes, and that's absolutely true. And the same
26 applies to horizontal 2D memory as well. There are physical memory cells.

1 They are oriented relative to one another. And once you've established the
2 framework, the indexing framework from bottom to top, it follows I'll say a
3 natural sequence to refer to things being above or below, et cetera.

4 JUDGE CYGAN: But in a horizontal configuration, you wouldn't
5 describe the first portion as being above the second portion, correct?

6 MR. JENSEN: Your Honor, I respectfully disagree with that. And
7 I can give you an example from Patent Owner's own dictionary that they
8 submitted in this case. This is on Slide 102. So this is the plain and
9 ordinary meaning right of bottom to top, putting aside any sort of POSITA
10 knowledge which we think is essential.

11 JUDGE CYGAN: Can we focus on above and below?

12 MR. JENSEN: I don't think they submitted any dictionary
13 definitions for above and below. But I would submit that they fall in into the
14 same category as the bottom to top discussion, which is the disputed claim
15 language. That's what the -- where the claim construction dispute centers.
16 And in this regard, the plain and ordinary meaning, Petitioner's construction
17 is consistent with the plain and ordinary meaning as highlighted here on
18 Slide 102, where bottom is the part -- closest to a reference point was
19 positioned.

20 And they give an example, it was positioned at the bottom of the
21 key for a rebound, talking about a basketball court which is plainly a
22 horizontal 2D structure. And the top says the same thing. It's the part
23 furthest from a given reference point, he took a jump shot from the top of the
24 key, or he took a shot from above the foul line. So the plain and ordinary
25 meaning of the phrase bottom to top is not restricted in any way, shape, or
26 form to a vertical orientation. And we submit that patent -- or Petitioner's

1 construction is consistent with the plain and ordinary mean.

2 There were some questions earlier about a substrate in the claim.

3 So Patent Owner's argument is, well, that Petitioner's source to drain
4 construction cannot be correct because the patent doesn't use the word
5 source or drain. Well, number one, there's no dispute that a memory string
6 has a source and drain. But neither does the specification contain any
7 reference whatsoever to a substrate. It's not in the figures. It's not in the
8 text. It's nowhere to be found.

9 And so by their own logic, their construction cannot be correct.

10 Because the same argument that they use to try to defeat the source to drain
11 construction applies with equal force to their construction, which also uses a
12 relative reference point. It just happens to be a different reference point.

13 But I don't want to lose sight of the forest for the trees here on the
14 bottom to top construction. The Petitioner believes we were correct. We
15 have the better of this. And I would direct Your Honors to look at Exhibit
16 1089, paragraphs 5 to 26 for additional details on the bottom to top issue.
17 But the more important point, in my view, is the Court doesn't need to get
18 wound up on construing bottom to top because Petitioner prevails under
19 either party's construction.

20 The Patent Owner talked about a *Wasica* case and a *Kennametal*
21 case. So on Slide 111 we have -- cite from the *Kennametal* case. It says, a
22 reference can anticipate a claim, even if it does not expressly spell out all the
23 limitations arranged or combined as in the claim if a person of ordinary skill
24 in the art reading the reference would at once envisage the claimed
25 arrangement or combination. We submit that's exactly the situation here.
26 That is true regardless of whether you read Dong in 2007, which we submit

1 is the incorrect date.

2 But it is certainly and absolutely the case in 2020 that a person of
3 ordinary skill in the art reading the Dong reference, knowing what three-
4 dimensional 3D NAND flash memory is, that it has vertical memory strings.
5 At that point, an argument to the contrary, that somebody -- a POSITA in
6 2020 would not understand three-dimensional memory to refer to vertical
7 memory strings passes the red face test.

8 We submitted copious evidence, market evidence, products on the
9 market. It was like 99.9 percent vertical memory string products in 2020.
10 Any POSITA reading Dong in 2020 would immediately know what a three-
11 dimensional NAND flash memory cell is and that it has vertical memory
12 strings. But even if you go back in time to that 2007 time point, we didn't
13 hear any counters. We didn't hear anything saying, oh, all those other
14 references that we cited, endo-1, endo-2, Kito, Tanaka, we didn't hear any
15 disagreement that all of those disclose vertical memory strings.

16 Their argument is somehow that they're -- with respect to the
17 Dong's disclosure of three-dimensional that, well, that might also include a
18 stacked two-dimensional memory. And this goes to their genus species
19 point. In *Kennametal*, one of the issues was, okay there's a very large
20 number of permutations, like a genus has a species of 100 things or
21 something. And the question is, well, would a person of ordinary skill in the
22 art reading a broad genus be able to understand a narrow disclosure of a
23 species? That is not the situation we have here.

24 The only two flavors, if you want to call it, in 2007 of three-
25 dimensional memory were vertical memory strains and stack 2D. Counsel
26 for YMTC talked about, well, there was a lot of different flavors because

1 some of the memory strings could be more than 32 bits or less than 32 bits.
2 That has nothing to do at all whatsoever with the categories of three-
3 dimensional memory that may have existed in 2007. It doesn't matter how
4 long the memory string is. That's not that doesn't change whether it's stack
5 2D or vertical. So the distinction that they're trying to draw is a false one.

6 They may have a point if the only thing that Dong disclosed was a
7 in memory. But Dong goes much further than disclosing just the memory.
8 If that was the entirety of Dong disclosures, you can apply these
9 programming voltages in a memory, I could see an argument that, well, how
10 do you know that -- a person of ordinary skill in the art necessarily
11 understand that to include vertical memory or three-dimensional memory.
12 But Dong goes further, it expressly discloses three-dimensional memory.
13 It's giving the more particular eyes the narrower more specific disclosure.

14 And that distinguishes the *Wasica* case and the *Nidec* case. And
15 we heard this from YMTC's counsel, well, there were -- if you look at that
16 case, it was talking about modulation schemes. And there were a number of
17 different modulation schemes. You could have phase modulation, frequency
18 modulation, AM, FM, QSK, PSK, all sorts of different modulation schemes.
19 And even if the -- that decision only talked about two of those, that decision
20 is in the context of a different patent with different technology.

21 Here in the context of three-dimensional NAND flash memory,
22 we've heard that there are only two flavors of it, the stacked 2D or vertical.
23 If you want to slice the tomato more finely, you can say, well, there's a U-
24 shaped memory string which is a form of vertical memory string as well that
25 you know has a U-shape, but it's still a vertical memory. And so regardless
26 of whether you look at the relevant date for evaluating both anticipation and

1 obviousness in 2007 or 2020, Petitioner prevails.

2 And that's the case -- moreover, even if Dong were restricted -- and
3 it's not. But even if it were restricted to 2D memory, we presented the
4 copious evidence that the program disturb and pass voltage disturb
5 techniques disclosed in Dong apply identically in the three-dimensional
6 memory context.

7 I see my time's up. And with that, I will close. Thank you.

8 JUDGE CYGAN: Thank you, Petitioner.

9 Patent Owner, you have 10 minutes for surrebuttal.

10 MR. LOWRY: Thank you, Your Honor. Okay. I'd like to start
11 first with Judge McGraw's question. And I want to apologize, I thought I
12 heard petition at 27 not reply at 27, which I think you're referring to these
13 new mappings in the reply. If I could jump to Slide 88, please. Now the
14 petition had specific mappings on the left. They also had this reservation of
15 rights, which seems contrary to the Board's rules and the statute that says
16 that these are just example, and other mappings could satisfy the claims.

17 So when I asked Petitioner's expert, are you aware of any other
18 mappings? He said, not at the moment, no. But then on reply, on Slide 89,
19 we see these new mappings. And you can see directly that the mappings
20 -- the variables for each mappings are different. The K value for the petition
21 and reply are different as are the M values. And you might be wondering,
22 why does that matter? Because by providing these new variables, Petitioner
23 provides a completely new obvious theory by redefining the first portion and
24 the second portion. Which is what those variables are relevant to, they
25 define the uppers and lower bounds of those portions.

26 And those types of shifting arguments are foreclosed by statute,

1 Federal Circuit precedent, Board guidelines. And it's clear why they did
2 this. Because their petition, which I pointed out earlier, had a first portion
3 that was only two-word lines on the left right. They had an issue with Claim
4 5, which required X to be greater than or equal to three. They couldn't get
5 the X word line in the first portion because they didn't map the first portion
6 big enough. That's their own problem they had in the petition. Now they're
7 trying to fix that on reply in a way that doesn't have anything to do with the
8 claim construction, Your Honors.

9 Now Petitioner pointed to petition 31 saying that, oh, well, look,
10 we said that Dong says you program all the word lines. Okay. I understand
11 that Dong says that. We don't contest that Dong says that. But if you look
12 at Petitioner's mapping on the left, you can program all the word lines from
13 bottom to top, left to right, however you want to program. You're never
14 going to get the X word line in the first portion. You still fail Claims 8 and
15 9 for that reason.

16 We heard some discussion about from bottom to top, and Judge
17 McGraw properly pointed out -- or sorry, Judge Cygan properly pointed out
18 that Claim 5 has this above language that requires this vertical arrangement.
19 And I would also like to point out that Claim 10 has similar language. It
20 recites a lower dummy word line formed above the first portion and an upper
21 dummy word line formed below the second portion. So again, in the claims
22 you have this repeated vertical architecture.

23 If we go to Slide 22, please. And I'd also --

24 JUDGE CYGAN: Counsel, is that also represented in Claim 1
25 which talks about a second portion formed below the first portion?

26 MR. LOWRY: Yes, Your Honor. Let me check Claim 11, but I

1 believe it's in all the independent claims. It is. Claim 11 cites -- recites a
2 first portion a second portion formed below the first portion.

3 Now on Slide 22, I'd just like to remind Your Honors that under
4 Petitioner's construction, the source of drain construction -- which my head's
5 spinning a little bit, Your Honor, because the construction has changed two
6 or three times now. Under their construction, they admit it has nothing to do
7 with the physical level. So they're trying to read out all this vertical
8 architecture that's in the claims, it's in the patent, in the specification.

9 And they're trying to say all these other vertical -- all these other
10 3D architectures or 2D architectures read on the claims, they're saying it's
11 nothing to do with the physical level at all, such that the source and drain,
12 what they call the top and bottom, can both be at the top. They can both be
13 -- the top can be at the bottom and the bottom can be at the top, as seen in
14 the sort -- the drain to source configuration in the middle.

15 Now we also heard some discussion about *Kennametal*. And I just
16 want to reorient the Board a little bit about that reference in *Kennametal*
17 actually disclosed the recited combination with the binders. It said, we have
18 a limited amount, a limited subset of these two components, and we're going
19 to pluck from those two and say a POSA would have once envisaged that
20 combination because it was already there. We don't have that kind of
21 disclosure in Dong.

22 Dong doesn't say the memory can be three-dimensional with
23 vertical word lines, horizontal word lines. It doesn't say anything about that.
24 So we don't have a disclosure that rises to the level of the anticipation
25 standard. And Nidec forecloses taking a POSA to knowledge, whether it's
26 from prior 2007 or 2020, and inserting that disclosure into Dong just because

1 a POSA would have once envisage it. I recommend the case -- of course the
2 vertical reading cases. But look at the cases that is not supported there.

3 I'd also like to make the point that there's almost this hammer and
4 nail theory, Your Honors, where, if POSA in this case would have seen
5 three-dimensional, boom, it's vertical word lines anywhere. That's the
6 impression I get. And that's just not the case. A POSA first is not an
7 automaton. It has an ordinary level of creativity. And the POSA's
8 knowledge is not limited to vertical word lines. A POSA would have been
9 generally knowledgeable about man, memory, structure, and fabrication
10 throughout the years. This is from the level of ordinary skill in the art.

11 And it's undisputed that three-dimensional NAND memory, Dong's
12 own disclosure of three-dimensional, includes 3D NAND with horizontal
13 word lines. That's undisputed. And in this context, a POSA would not look
14 back at every reference over last 20 years or 30 years and assume every
15 disclosure of three-dimensional means vertical wording.

16 JUDGE CYGAN: But if this three-dimensional means either
17 vertical or horizontal, why would a POSITA not immediately envision both
18 of those options? It's only two options.

19 MR. LOWRY: Right. So Your Honor, so I would submit that it's
20 not only two options. I think that's a framing provided by Petitioner. That's
21 somewhat of an oversimplification. What Petitioner is offering is that you
22 have 32-word lines in a horizontal arrangement, and you're going to take
23 those 32-word lines and turn them vertical.

24 Petitioner, first, never presented an argument that Dong's three-
25 dimensional language is sort of this genus and species such that you only
26 have two. That you would need to do in order to meet your burden. Here

1 you can look at the *Wasica* case where they -- at Pages 1285 to 86 where
2 they pointed that exact thing out. There was never a expressed definition for
3 the genus or what species are in there. And therefore, a Petitioner didn't
4 meet its burden in that case.

5 JUDGE MCGRAW: Is there a reason why a POSITA would not
6 envision a 32-word line vertical configuration? Are there limits to the
7 number of word lines that can be stacked vertically?

8 MR. LOWRY: I'll do my best to answer this, Your Honor. I think
9 that whether there's a limit to how many word lines can be stacked vertically
10 somewhat depends on what your timing or reference is. But I will say that
11 the *Nidec* case forecloses bringing in this word line envisaging into Dong
12 which doesn't actually have that disclosure.

13 That was the big line drawn by *Nidec* compared to *Kennametal*.
14 *Kennametal* had the disclosure. In *Nidec* case, it didn't have it. The prior
15 didn't have it. And so they drew a bright line saying you can't bring in a
16 POSITA knowledge to insert this disclosure for anticipation purposes.
17 Remember, we're in anticipation, not obviousness.

18 I'll also say that Petitioner's anticipation theory improperly
19 converts Dong's generic reference to 3D -- three-dimensional to the specific
20 expressed disclosure of vertical word lines with 32-word cells -- 32 cells.
21 But anticipation has to stand or fall on Dong's and on disclosure. To find
22 otherwise would let Dong preempt later developed vertical 3D NAND
23 structures applying the recited voltages, including structures Dong never
24 actually disclosed. And Judge McGraw touched on this earlier.

25 But this is like interpreting a disclosure of a wireless
26 communication device in 1990s and saying it anticipates the iPhone. This is

1 exactly what the *Galderma* case rejected, where the Federal Circuit refused
2 to turn a second -- to a second reference for a very specific teaching or use it
3 to incorporate a specific disclosure not found in the primary reference. And
4 unless there are further questions, Your Honors, I'll concede the rest of my
5 time.

6 JUDGE CYGAN: Thank you, Counsel. I'd like to thank counsel
7 for both parties for their attendance and presentations today. I appreciate the
8 level of preparedness of the counsel today and your excellent command of
9 the record on both sides, which was very helpful for the Board. I'd also like
10 to commend your colleagues who did a fine job of preparing the
11 demonstrative exhibits, which were also useful for us in following along
12 with the arguments you gave today. A final written decision will be issued
13 in due course. And this hearing is now adjourned.

14 (Whereupon, the above-entitled matter went off the record at 12:43
15 p.m.)

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