

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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MICRON TECHNOLOGY, INC.,  
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,  
Patent Owner

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Case No.: IPR2025-00191  
U.S. Patent No. 11,581,322  
Issue Date: February 14, 2023

Title: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH  
ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

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**PETITION FOR *INTER PARTES* REVIEW  
OF U.S. PATENT NO. 11,581,322  
PURSUANT TO 35 U.S.C. §§311-319 and 37 C.F.R. §42**

|                                                                                   | <b><u>Page</u></b> |
|-----------------------------------------------------------------------------------|--------------------|
| I. INTRODUCTION .....                                                             | 1                  |
| II. MANDATORY NOTICES .....                                                       | 6                  |
| A. Real Party-in-Interest .....                                                   | 6                  |
| B. Related Matters.....                                                           | 6                  |
| C. Counsel, Service, and Fee Information .....                                    | 8                  |
| III. REQUIREMENTS FOR <i>INTER PARTES</i> REVIEW.....                             | 10                 |
| A. Grounds for Standing .....                                                     | 10                 |
| B. Identification of Challenge and Statement of Precise Relief<br>Requested ..... | 10                 |
| IV. INSTITUTION SHOULD BE GRANTED.....                                            | 11                 |
| A. There are No Grounds for a § 314 Discretionary Denial in this<br>Case .....    | 11                 |
| 1. Possibility of a Stay .....                                                    | 11                 |
| 2. Proximity of the Court’s Trial Date.....                                       | 11                 |
| 3. Investment in the Parallel Proceeding .....                                    | 12                 |
| 4. Issue Overlap.....                                                             | 12                 |
| 5. Party Overlap .....                                                            | 13                 |
| 6. Other Circumstances .....                                                      | 13                 |
| B. Denial Under §325(d) Would Be Inappropriate.....                               | 13                 |
| V. TECHNOLOGY BACKGROUND.....                                                     | 14                 |
| VI. THE ’322 PATENT AND ITS PROSECUTION HISTORY .....                             | 21                 |
| VII. CLAIM CONSTRUCTION .....                                                     | 27                 |
| VIII. LEVEL OF ORDINARY SKILL IN THE ART.....                                     | 27                 |
| IX. DESCRIPTION OF THE PRIOR ART .....                                            | 27                 |
| A. Nishikawa.....                                                                 | 27                 |
| B. Nishikawa2.....                                                                | 31                 |
| C. Lu.....                                                                        | 32                 |

|    |                                                                                                                                                                                                                   |    |
|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| X. | GROUND 1: NISHIKAWA IN VIEW OF THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 1-3, 6-10, 13-16, AND 19-20 .....                                                                                                 | 34 |
| A. | Claim 1: .....                                                                                                                                                                                                    | 34 |
| 1. | [1.PRE] “A three-dimensional (3D) memory device, comprising:” .....                                                                                                                                               | 34 |
| 2. | [1.A] “a substrate;” .....                                                                                                                                                                                        | 34 |
| 3. | [1.B] “a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;” .....                                                                                                     | 35 |
| 4. | [1.C] “a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;” .....                                                                                          | 36 |
| 5. | [1.D] “a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate; and” ...                                                | 39 |
| 6. | [1.E] “a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones.” .....                | 53 |
| B. | Claim 2: .....                                                                                                                                                                                                    | 57 |
| 1. | [2] “The 3D memory device of claim 1, further comprising: a peripheral device on the substrate, a peripheral contact being arranged outside of the memory stack and in contact with the peripheral device.” ..... | 57 |
| C. | Claim 3: .....                                                                                                                                                                                                    | 59 |
| 1. | [3.PRE] “The 3D memory device of claim 2, further comprising:” .....                                                                                                                                              | 59 |
| 2. | [3.A] “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,” .                                                     | 59 |
| 3. | [3.B] “wherein each of the dielectric layer in the dummy channel structure, a spacer in the TAC, and a spacer in the peripheral contact comprises silicon oxide.” .....                                           | 65 |
| D. | Claim 6: .....                                                                                                                                                                                                    | 66 |

|    |                                                                                                                                                                                                                                                                                                               |    |
|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 1. | [6.PRE] “The 3D memory device of claim 1, further comprising:” .....                                                                                                                                                                                                                                          | 66 |
| 2. | [6.A] “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; and” .....                                                                                                                                         | 66 |
| 3. | [6.B] “a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate,” .....                                                                                                                                                                                | 67 |
| 4. | [6.C] “wherein: a diameter of the TAC is at least equal to a diameter of the peripheral contact; and” .....                                                                                                                                                                                                   | 67 |
| 5. | [6.D] “a diameter of the dummy channel structure is smaller than each of a diameter of the TAC and a diameter of the peripheral contact.” .....                                                                                                                                                               | 70 |
| E. | Claim 7: .....                                                                                                                                                                                                                                                                                                | 73 |
| 1. | [7] “The 3D memory device of claim 1, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.” ..... | 73 |
| F. | Claim 8: .....                                                                                                                                                                                                                                                                                                | 77 |
| 1. | [8] “A three-dimensional (3D) memory device, comprising:” .....                                                                                                                                                                                                                                               | 77 |
| 2. | [8.A] “a substrate;” .....                                                                                                                                                                                                                                                                                    | 77 |
| 3. | [8.B] “a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;” .....                                                                                                                                                                                                 | 78 |
| 4. | [8.C] “a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack; and” .....                                                                                                                                                                                  | 78 |

|    |                                                                                                                                                                                                                                                                                                                                                         |    |
|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 5. | [8.D] “a through array contact (TAC) comprising a substantially circular section and extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate.” ..... | 78 |
| G. | Claim 9: .....                                                                                                                                                                                                                                                                                                                                          | 79 |
| 1. | [9.PRE] “The 3D memory device of claim 8, further comprising:” .....                                                                                                                                                                                                                                                                                    | 79 |
| 2. | [9.A] “a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate;” .....                                                                                                                                                                                                                          | 79 |
| 3. | [9.B] “wherein a thickness of the spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact.” .....                                                                                                                                                                                                                 | 79 |
| H. | Claim 10: .....                                                                                                                                                                                                                                                                                                                                         | 81 |
| 1. | [10] “The 3D memory device of claim 9, wherein the spacer of the TAC and the spacer of the peripheral contact comprise a same material.” .....                                                                                                                                                                                                          | 81 |
| I. | Claim 13: .....                                                                                                                                                                                                                                                                                                                                         | 81 |
| 1. | [13] “The 3D memory device of claim 8, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.” .....                                          | 81 |
| J. | Claim 14: .....                                                                                                                                                                                                                                                                                                                                         | 81 |
| 1. | [14.PRE] “A three-dimensional (3D) memory device, comprising:” .....                                                                                                                                                                                                                                                                                    | 81 |
| 2. | [14.A] “a substrate;” .....                                                                                                                                                                                                                                                                                                                             | 81 |
| 3. | [14.B] “a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;” .....                                                                                                                                                                                                                                          | 82 |

|    |                                                                                                                                                                                                                                                                    |    |
|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 4. | [14.C] “a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;”<br>.....                                                                                                                                       | 82 |
| 5. | [14.D] “a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a substantially circular section; and” .....                                         | 82 |
| 6. | [14.E] “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,” .                                                                                                     | 82 |
| 7. | [14.F] “wherein: a first diameter of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs; and” ..... | 82 |
| 8. | [14.G] “a peripheral contact is arranged outside the memory stack and in contact with a peripheral device on the substrate.” .....                                                                                                                                 | 82 |
| K. | Claim 15: .....                                                                                                                                                                                                                                                    | 83 |
| 1. | [15.PRE] “The 3D memory device of claim 14, wherein:” .....                                                                                                                                                                                                        | 83 |
| 2. | [15.A] “a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact; and” .....                                                                                                                                 | 83 |
| 3. | [15.B] “a diameter of the TAC is at least equal to a diameter of the peripheral contact.” .....                                                                                                                                                                    | 83 |
| L. | Claim 16: .....                                                                                                                                                                                                                                                    | 83 |
| 1. | [16] “The 3D memory device of claim 15, wherein: a diameter of the dummy channel structure is smaller than each of the diameter of the TAC and the diameter of the peripheral contact.” .....                                                                      | 83 |
| M. | Claim 19: .....                                                                                                                                                                                                                                                    | 83 |

|     |                                                                                                                                                                                                                     |    |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 1.  | [19] “The 3D memory device of claim 1, wherein: the TAC has a substantially circular section and comprises a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC.” ..... | 83 |
| N.  | Claim 20: .....                                                                                                                                                                                                     | 84 |
| 1.  | [20] “The 3D memory device of claim 14, wherein: the TAC comprises a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC.” .....                                         | 84 |
| XI. | GROUND 2: NISHIKAWA IN VIEW OF LU AND THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 4-5, 11-12, AND 17-18 .....                                                                                                  | 84 |
| A.  | Motivation to Combine .....                                                                                                                                                                                         | 84 |
| B.  | Claim 4: .....                                                                                                                                                                                                      | 89 |
| 1.  | [4.PRE] “The 3D memory device of claim 1, wherein the memory stack comprises:” .....                                                                                                                                | 89 |
| 2.  | [4.A] “a lower memory deck on the substrate; and” .....                                                                                                                                                             | 89 |
| 3.  | [4.B] “an upper memory deck above the lower memory deck.” .....                                                                                                                                                     | 90 |
| C.  | Claim 5: .....                                                                                                                                                                                                      | 91 |
| 1.  | [5.PRE] “The 3D memory device of claim 4, wherein the channel structure comprises:” .....                                                                                                                           | 91 |
| 2.  | [5.A] “a lower channel structure extending vertically through the lower memory deck;” .....                                                                                                                         | 91 |
| 3.  | [5.B] “an upper channel structure extending vertically through the upper memory deck; and” .....                                                                                                                    | 93 |
| 4.  | [5.C] “an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.” .....                                                                       | 94 |
| D.  | Claim 11: .....                                                                                                                                                                                                     | 96 |
| 1.  | [11.PRE] “The 3D memory device of claim 8, wherein the memory stack comprises:” .....                                                                                                                               | 96 |
| 2.  | [11.A] “a lower memory deck on the substrate; and” ...                                                                                                                                                              | 96 |

|      |                                                                                                                                                |    |
|------|------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 3.   | [11.B] “an upper memory deck above the lower memory deck.” .....                                                                               | 96 |
| E.   | Claim 12: .....                                                                                                                                | 96 |
| 1.   | [12.PRE] “The 3D memory device of claim 11, wherein the channel structure comprises:” .....                                                    | 96 |
| 2.   | [12.A] “a lower channel structure extending vertically through the lower memory deck;” .....                                                   | 97 |
| 3.   | [12.B] “an upper channel structure extending vertically through the upper memory deck; and” .....                                              | 97 |
| 4.   | [12.C] “an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.” ..... | 97 |
| F.   | Claim 17: .....                                                                                                                                | 97 |
| 1.   | [17.PRE] “The 3D memory device of claim 14, wherein the memory stack comprises:” .....                                                         | 97 |
| 2.   | [17.A] “a lower memory deck on the substrate; and” ...                                                                                         | 97 |
| 3.   | [17.B] “an upper memory deck above the lower memory deck.” .....                                                                               | 97 |
| G.   | Claim 18: .....                                                                                                                                | 97 |
| 1.   | [18.PRE] “The 3D memory device of claim 17, wherein the channel structure comprises:” .....                                                    | 97 |
| 2.   | [18.A] “a lower channel structure extending vertically through the lower memory deck;” .....                                                   | 98 |
| 3.   | [18.B] “an upper channel structure extending vertically through the upper memory deck; and” .....                                              | 98 |
| 4.   | [18.C] “an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.” ..... | 98 |
| XII. | GROUND 3: NISHIKAWA IN VIEW OF NISHIKAWA2 AND THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 1-3, 6-10, 13-16, AND 19-20.....                | 98 |
| A.   | Motivation to Combine .....                                                                                                                    | 98 |

XIII. GROUND 4: NISHIKAWA IN VIEW OF NISHIKAWA2 AND LU  
AND THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS  
CLAIMS 4-5, 11-12, AND 17-18 ..... 100

XIV. SECONDARY CONSIDERATIONS ..... 100

XV. CONCLUSION..... 101

## **TABLE OF AUTHORITIES**

|                                                                                                                                                                                                  | <b>Page(s)</b> |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| <br><b>Cases</b>                                                                                                                                                                                 |                |
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| <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology,<br/>Inc. and Micron Consumer Products Group, LLC</i> ,<br>Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023)..... | 6, 7, 12       |
| <br><b>Statutes</b>                                                                                                                                                                              |                |
| 35 U.S.C. § 102(a)(1).....                                                                                                                                                                       | 27, 31, 32     |
| 35 U.S.C. §314(a) .....                                                                                                                                                                          | 8              |
| 35 U.S.C. §325(d) .....                                                                                                                                                                          | 8, 13          |
| <br><b>Other Authorities</b>                                                                                                                                                                     |                |
| 37 C.F.R. §42.10(b) .....                                                                                                                                                                        | 9              |
| 37 C.F.R. §42.15(a).....                                                                                                                                                                         | 9              |
| 37 C.F.R. §42.108(a).....                                                                                                                                                                        | 8              |

### LISTING OF EXHIBITS

| EXHIBIT NO. | DESCRIPTION                                                                      |
|-------------|----------------------------------------------------------------------------------|
| 1001        | U.S. Patent No. 11,581,322 to Guo et al. (“the ’322 Patent”)                     |
| 1002        | File History of U.S. Patent No. 11,581,322 (“the ’322 FH”)                       |
| 1003        | Declaration of Dr. Jack C. Lee (“Lee”)                                           |
| 1004        | <i>Curriculum Vitae</i> of Dr. Jack C. Lee                                       |
| 1005        | U.S. Patent No. 9,837,431 to Nishikawa et al. (“Nishikawa”)                      |
| 1006        | U.S. Patent No. 9,853,046 to Lu et al. (“Lu”)                                    |
| 1007        | U.S. Patent No. 10,658,378 to Tao et al.                                         |
| 1008        | U.S. Patent Publication No. 2019/0229125A1 to Zhou et al.                        |
| 1009        | U.S. Patent No. 10,777,501 to Nakajima et al. (“Nakajima”)                       |
| 1010        | Micheloni, “3D Flash Memories” (2016)                                            |
| 1011        | U.S. Patent Publication No. 2017/0179026 A1 to Toyama et al.                     |
| 1012        | U.S. Patent No. 10,354,980 to Mushiga et al. (“Mushiga”)                         |
| 1013        | PCT Publication No. WO 2019/042103A1 to Dai et al.                               |
| 1014        | U.S. Patent No.10,679,721 to Kim et al.                                          |
| 1015        | Aritome, “NAND Flash Memory Technologies” (“Aritome”)                            |
| 1016        | File History for U.S. Patent Application No. 16/745,342                          |
| 1017        | U.S. Patent Publication No. 2012/0280304A1 to Lee et al. (“Lee 304”)             |
| 1018        | U.S. Patent Publication No. 2017/0125430A1 to Nishikawa et al. (“Nishikawa 430”) |

Petition for *Inter Partes* Review of U.S. Patent No. 11,581,322

| EXHIBIT<br>NO. | DESCRIPTION                                                                                                     |
|----------------|-----------------------------------------------------------------------------------------------------------------|
| 1019           | U.S. Patent Publication No. 2015/0348987A1 to Lee et al. (“Lee 987”)                                            |
| 1020           | U.S. Patent Publication No. 2018/0301374A1 to Masamori et al. (“Masamori”)                                      |
| 1021           | U.S. Patent No. 8,107,292 to Maejima                                                                            |
| 1022           | U.S. Patent No. 10,347,654 to Iwai et al. (“Iwai”)                                                              |
| 1023           | U.S. Patent No. 10,559,583 to Park et al.                                                                       |
| 1024           | U.S. Patent No. 5,945,717 to Chevallier                                                                         |
| 1025           | U.S. Patent No. 10,347,487 to Lee et al.                                                                        |
| 1026           | Ronse, “Optical lithography—a historical perspective,” C. R. Physique 7 (2006) (“Ronse”)                        |
| 1027           | U.S. Patent No. 10,290,643 to Kai et al.                                                                        |
| 1028           | U.S. Patent No. 9,859,297 to Park et al.                                                                        |
| 1029           | U.S. Patent Publication No. 2018/0308559 to Kim et al. (“Kim 559”)                                              |
| 1030           | U.S. Patent No. 8,945,996 to Tang et al.                                                                        |
| 1031           | U.S. Patent No. 10,115,632 to Masamori <sup>632</sup> et al.                                                    |
| 1032           | U.S. Patent No. 10,879,254 to Guo et al.                                                                        |
| 1033           | U.S. Patent No. 9,793,139 to Sharangpani et al.                                                                 |
| 1034           | Wolf, “Silicon Processing for the VLSI Era, Volume 1-Process Technology,” Lattice Press (1986) (“Wolf Vol. 1”)  |
| 1035           | Wolf, “Silicon Processing for the VLSI Era, Volume 1-Process Integration,” Lattice Press (1990) (“Wolf Vol. 2”) |

Petition for *Inter Partes* Review of U.S. Patent No. 11,581,322

| EXHIBIT NO. | DESCRIPTION                                                                                                                                                                                                                                                                                                                    |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1036        | U.S. Patent Publ. No. 2019/0081061 to Tessariol et al.                                                                                                                                                                                                                                                                         |
| 1037        | U.S. Patent No. 10,304,852 to Cui et al. (“Cui”)                                                                                                                                                                                                                                                                               |
| 1038        | Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,879,254 (Ex. B-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) (“Ex. B-1, YMTC’s Contentions”) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]                                                    |
| 1039        | U.S. Patent No. 11,075,084 to Shen et al.                                                                                                                                                                                                                                                                                      |
| 1040        | U.S. Patent No. 10,504,596 to Goda et al.                                                                                                                                                                                                                                                                                      |
| 1041        | U.S. Patent No. 10,381,369 to Kim et al. (“Kim 369”)                                                                                                                                                                                                                                                                           |
| 1042        | Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL                                                                                                       |
| 1043        | Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at <a href="https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf">https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf</a>                      |
| 1044        | Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.’s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL |
| 1045        | Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL                                                                                                       |

Petition for *Inter Partes* Review of U.S. Patent No. 11,581,322

| <b>EXHIBIT<br/>NO.</b> | <b>DESCRIPTION</b>                                                                                                                                      |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1046                   | U.S. Patent No. 9,935,123 to Nishikawa (“Nishikawa2”)                                                                                                   |
| 1047                   | Printout, 11/26/2024, Britannica<br>( <a href="https://www.britannica.com/science/geometry">https://www.britannica.com/science/geometry</a> ) (ellipse) |

**LISTING OF CHALLENGED CLAIMS**

| Ref. #          | Listing of Challenged Claims                                                                                                                                                                          |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Claim 1:</b> |                                                                                                                                                                                                       |
| [1.PRE]         | A three-dimensional (3D) memory device, comprising:                                                                                                                                                   |
| [1.A]           | a substrate;                                                                                                                                                                                          |
| [1.B]           | a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;                                                                                                       |
| [1.C]           | a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;                                                                                            |
| [1.D]           | a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate; and                                                |
| [1.E]           | a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones.                  |
| <b>Claim 2:</b> |                                                                                                                                                                                                       |
| [2]             | The 3D memory device of claim 1, further comprising: a peripheral device on the substrate, a peripheral contact being arranged outside of the memory stack and in contact with the peripheral device. |
| <b>Claim 3:</b> |                                                                                                                                                                                                       |
| [3.PRE]         | The 3D memory device of claim 2, further comprising:                                                                                                                                                  |
| [3.A]           | a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,                                                   |

| Ref. #          | Listing of Challenged Claims                                                                                                                              |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3.B]           | wherein each of the dielectric layer in the dummy channel structure, a spacer in the TAC, and a spacer in the peripheral contact comprises silicon oxide. |
| <b>Claim 4:</b> |                                                                                                                                                           |
| [4.PRE]         | The 3D memory device of claim 1, wherein the memory stack comprises:                                                                                      |
| [4.A]           | a lower memory deck on the substrate; and                                                                                                                 |
| [4.B]           | an upper memory deck above the lower memory deck.                                                                                                         |
| <b>Claim 5:</b> |                                                                                                                                                           |
| [5.PRE]         | The 3D memory device of claim 4, wherein the channel structure comprises:                                                                                 |
| [5.A]           | a lower channel structure extending vertically through the lower memory deck;                                                                             |
| [5.B]           | an upper channel structure extending vertically through the upper memory deck; and                                                                        |
| [5.C]           | an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.                           |
| <b>Claim 6:</b> |                                                                                                                                                           |
| [6.PRE]         | The 3D memory device of claim 1, further comprising:                                                                                                      |
| [6.A]           | a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; and   |
| [6.B]           | a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate,                                          |
| [6.C]           | wherein: a diameter of the TAC is at least equal to a diameter of the peripheral contact; and                                                             |

| Ref. #          | Listing of Challenged Claims                                                                                                                                                                                                                                                                                                              |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [6.D]           | a diameter of the dummy channel structure is smaller than each of a diameter of the TAC and a diameter of the peripheral contact.                                                                                                                                                                                                         |
| <b>Claim 7:</b> |                                                                                                                                                                                                                                                                                                                                           |
| [7]             | The 3D memory device of claim 1, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.                                         |
| <b>Claim 8:</b> |                                                                                                                                                                                                                                                                                                                                           |
| [8.PRE]         | A three-dimensional (3D) memory device, comprising:                                                                                                                                                                                                                                                                                       |
| [8.A]           | a substrate;                                                                                                                                                                                                                                                                                                                              |
| [8.B]           | a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;                                                                                                                                                                                                                                           |
| [8.C]           | a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack; and                                                                                                                                                                                                                            |
| [8.D]           | a through array contact (TAC) comprising a substantially circular section and extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate. |
| <b>Claim 9:</b> |                                                                                                                                                                                                                                                                                                                                           |
| [9.PRE]         | The 3D memory device of claim 8, further comprising:                                                                                                                                                                                                                                                                                      |
| [9.A]           | a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate;                                                                                                                                                                                                                          |
| [9.B]           | wherein a thickness of the spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact.                                                                                                                                                                                                                 |

| Ref. #           | Listing of Challenged Claims                                                                                                                                                                                                                                                                      |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Claim 10:</b> |                                                                                                                                                                                                                                                                                                   |
| [10]             | The 3D memory device of claim 9, wherein the spacer of the TAC and the spacer of the peripheral contact comprise a same material.                                                                                                                                                                 |
| <b>Claim 11:</b> |                                                                                                                                                                                                                                                                                                   |
| [11.PRE]         | The 3D memory device of claim 8, wherein the memory stack comprises:                                                                                                                                                                                                                              |
| [11.A]           | a lower memory deck on the substrate; and                                                                                                                                                                                                                                                         |
| [11.B]           | an upper memory deck above the lower memory deck.                                                                                                                                                                                                                                                 |
| <b>Claim 12:</b> |                                                                                                                                                                                                                                                                                                   |
| [12.PRE]         | The 3D memory device of claim 11, wherein the channel structure comprises:                                                                                                                                                                                                                        |
| [12.A]           | a lower channel structure extending vertically through the lower memory deck;                                                                                                                                                                                                                     |
| [12.B]           | an upper channel structure extending vertically through the upper memory deck; and                                                                                                                                                                                                                |
| [12.C]           | an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.                                                                                                                                                                   |
| <b>Claim 13:</b> |                                                                                                                                                                                                                                                                                                   |
| [13]             | The 3D memory device of claim 8, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs. |
| <b>Claim 14:</b> |                                                                                                                                                                                                                                                                                                   |
| [14.PRE]         | A three-dimensional (3D) memory device, comprising:                                                                                                                                                                                                                                               |
| [14.A]           | a substrate;                                                                                                                                                                                                                                                                                      |

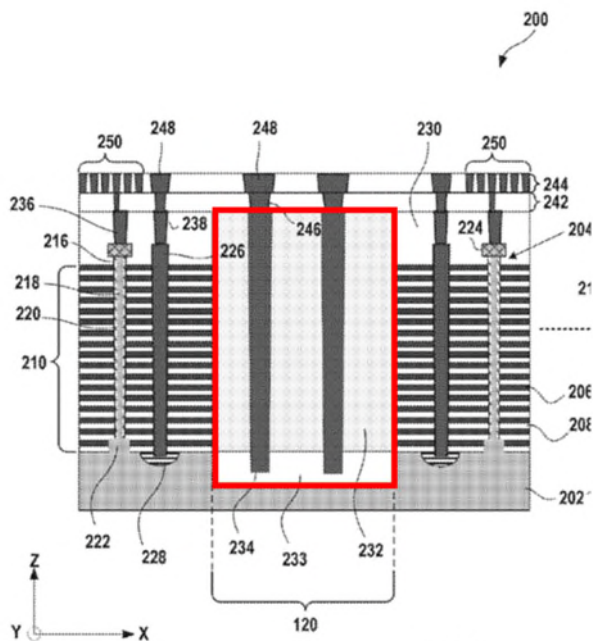
| Ref. #           | Listing of Challenged Claims                                                                                                                                                                                                                        |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [14.B]           | a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;                                                                                                                                                     |
| [14.C]           | a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;                                                                                                                                          |
| [14.D]           | a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a substantially circular section; and                                         |
| [14.E]           | a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,                                                                                                 |
| [14.F]           | wherein: a first diameter of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs; and |
| [14.G]           | a peripheral contact is arranged outside the memory stack and in contact with a peripheral device on the substrate.                                                                                                                                 |
| <b>Claim 15:</b> |                                                                                                                                                                                                                                                     |
| [15.PRE]         | The 3D memory device of claim 14, wherein:                                                                                                                                                                                                          |
| [15.A]           | a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact; and                                                                                                                                 |
| [15.B]           | a diameter of the TAC is at least equal to a diameter of the peripheral contact.                                                                                                                                                                    |
| <b>Claim 16:</b> |                                                                                                                                                                                                                                                     |
| [16]             | The 3D memory device of claim 15, wherein: a diameter of the dummy channel structure is smaller than each of the diameter of the TAC and the diameter of the peripheral contact.                                                                    |

| Ref. #           | Listing of Challenged Claims                                                                                                                                                                           |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Claim 17:</b> |                                                                                                                                                                                                        |
| [17.PRE]         | The 3D memory device of claim 14, wherein the memory stack comprises:                                                                                                                                  |
| [17.A]           | a lower memory deck on the substrate; and                                                                                                                                                              |
| [17.B]           | an upper memory deck above the lower memory deck.                                                                                                                                                      |
| <b>Claim 18:</b> |                                                                                                                                                                                                        |
| [18]             | The 3D memory device of claim 17, wherein the channel structure comprises:                                                                                                                             |
| [18.A]           | a lower channel structure extending vertically through the lower memory deck;                                                                                                                          |
| [18.B]           | an upper channel structure extending vertically through the upper memory deck; and                                                                                                                     |
| [18.C]           | an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.                                                                        |
| <b>Claim 19:</b> |                                                                                                                                                                                                        |
| [19]             | The 3D memory device of claim 1, wherein: the TAC has a substantially circular section and comprises a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC. |
| <b>Claim 20</b>  |                                                                                                                                                                                                        |
| [20]             | The 3D memory device of claim 14, wherein: the TAC comprises a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC.                                         |

## I. INTRODUCTION

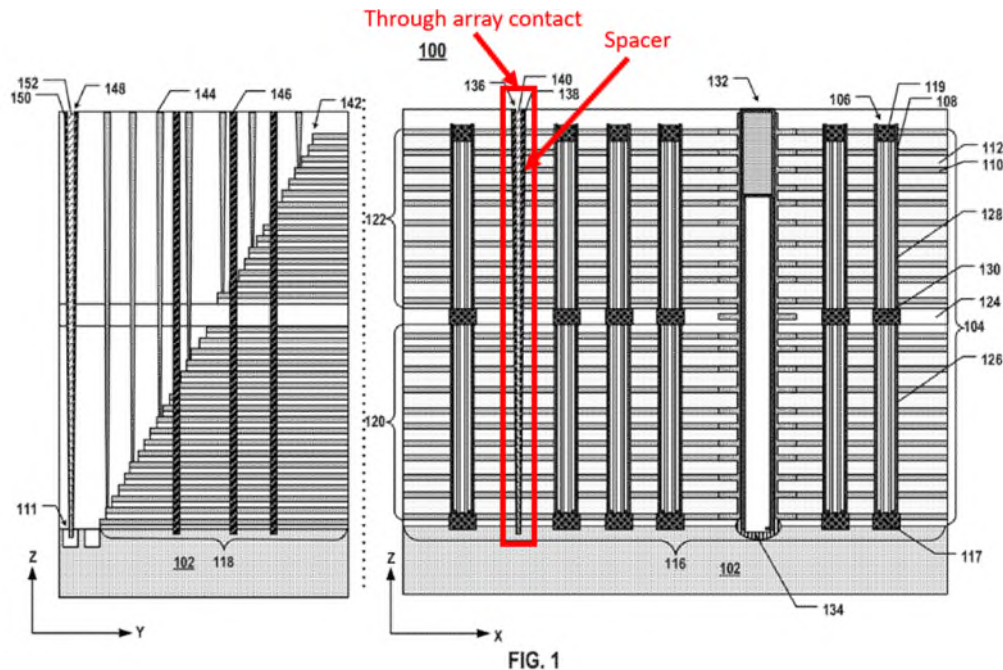
Petitioner Micron Technology, Inc. (“Petitioner”) respectfully requests *inter partes* review of claims 1-20 (the “Challenged Claims”) of U.S. Patent No. 11,581,322 (the “’322 Patent”) assigned to Yangtze Memory Technologies Co., Ltd (“Patent Owner” or “PO”).

The ’322 Patent relates to three-dimensional (3D) memory devices and specifically to 3D memory devices with “through array contacts” (TACs). Ex. 1001, 1:26-28. The ’322 Patent identifies a single alleged problem with the prior art—that TACs formed in barrier structures in a memory stack take up too much space. *Id.*, 4:55-5:22. The figure below depicts a barrier structure, i.e., a large oxide rectangular block:



Ex. 1007 (U.S. Pat. 10,658,378), Fig. 2 (annotated).

Instead of a barrier structure to isolate the TACs, the '322 Patent teaches employing a thin spacer (138) for each TAC.



Ex. 1001, Fig. 1 (annotated). The '322 Patent alleges that forming the TACs in the spacer would “simplify the fabrication flow” and “reduce process cost.” *Id.*, 4:55-5:22.

Claim 1 is illustrative. In addition to the above TAC, it covers the most basic 3D memory structures: a “substrate,” “a memory stack,” “a channel structure,” a TAC that is “buried into the substrate,” and “a slit structure” that “separate[s] the memory stack into a plurality of memory zones.”

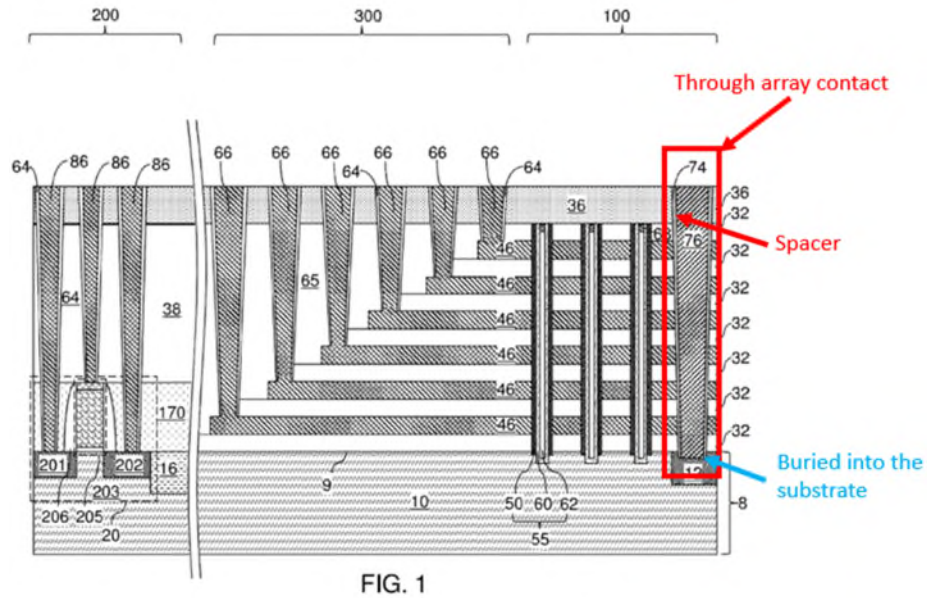
The alleged point of novelty, however, was not the reason for allowance. Instead, Applicant had to amend claim 1 to require that the TAC is “buried into the substrate” **and** further that the memory device includes “a slit structure” that

“separate[s] the memory stack into a plurality of memory zones.” See §VI. In fact, the file history makes clear that TACs that are buried into the substrate were already known in the art, and for claim 1, it was the combination of the TAC and the slit that led to allowance. In other words, the alleged distinguishing feature was simply the addition of a slit that divides the array. For other independent claims, e.g., claim 8, Applicant added that the TAC was “circular.” These alleged, minor distinctions in no way distinguish the prior art.

For example, the Examiner was unaware of Nishikawa (Ex. 1005, “Nishikawa”).<sup>1</sup> Nishikawa, in fact, discloses the same type of buried TAC that the Examiner found to disclose the buried TAC limitation during prosecution (leading the Applicant to amend the claims to further require, e.g., the slit limitation):

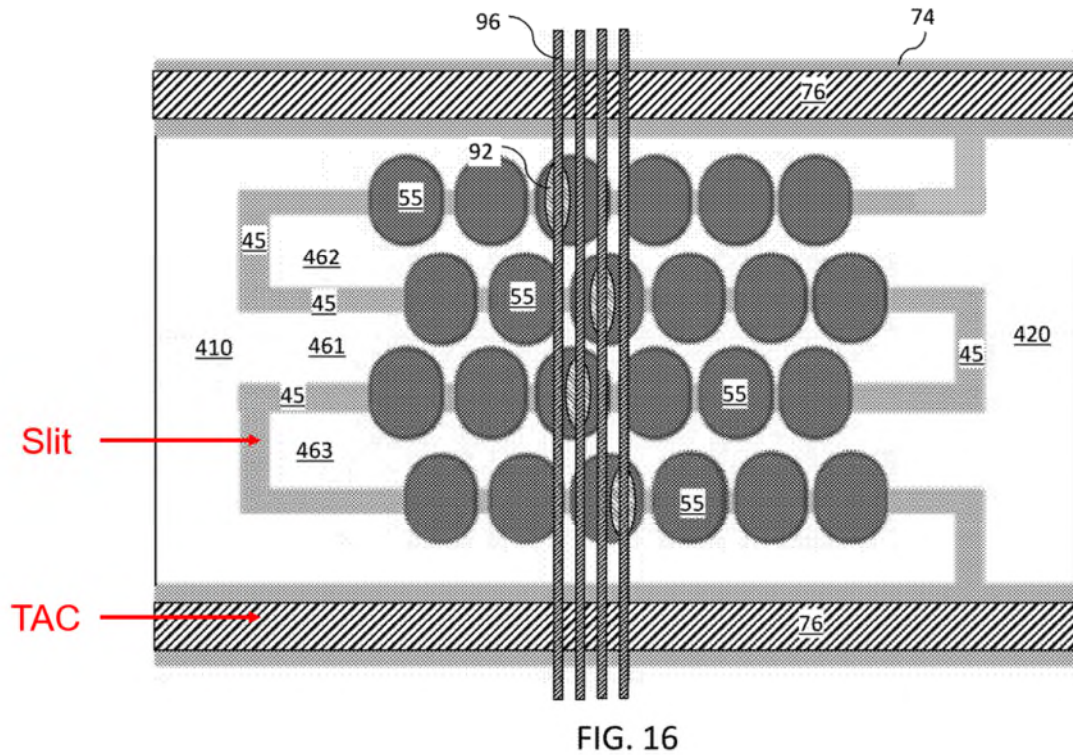
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<sup>1</sup> The Examiner cited two, unrelated patents to the same inventor. Ex. 1001, Cover.



Nishikawa, Fig. 1 (annotated); 6:45-62 (describing a TAC (“backside contact via structure 76”) having a thin “dielectric spacer 74”).

Critically, unlike the file history references that disclose a buried TAC, Nishikawa also discloses a distinct dividing slit, namely, “separator trenches 47” that become “separator dielectric structures 45”:



Nishikawa, Fig. 1. “The separator trenches 47 can laterally divide the alternating stack (32, 42) into a plurality of portions.” *Id.*, 8:16-16. Unlike the embodiment above in which the trenches include memory cells, Nishikawa also discloses that “[e]ach memory opening 49 can be located between a pair of separator dielectric structures 45.” *Id.*, 8:57-60.

What’s more, the Examiner also was unaware of another Nishikawa patent. Ex. 1046 (“Nishikawa2”). Nishikawa and Nishikawa2 describe the same memory architecture and are based on provisional applications that were filed only 5 days apart. Ex. 1005, Cover; Nishikawa2, Cover. Notably, Nishikawa2 states that the buried TAC—a source line contact—can be circular: “The openings 79 [which form

structures 76] can have any suitable shape, such as circular, rectangular or elongated trench shape.” Nishikawa2, 22:38-41. Indeed, circular TACs were widespread in the prior art. Thus, the other alleged distinctions over the prior art fare no better.

The dependent claims simply recite additional basic, well-known 3D NAND structures, e.g., dummy channels, multi-tier 3D NAND structures, etc. Some of these features are taught by Nishikawa, while the rest were well within the knowledge of a POSITA.

Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable under §103.

## **II. MANDATORY NOTICES**

### **A. Real Party-in-Interest**

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

### **B. Related Matters**

According to USPTO assignment records, the '322 Patent is currently assigned to Yangtze Memory Technologies, Co., Ltd. (“YMTC” or “PO”). On July 12, 2024, YMTC asserted the '322 Patent and U.S. Patent Nos. 10,672,711, 10,879,164, 10,879,254, 10,886,291, 11,101,276, 11,145,666, 11,450,604, 11,482,532, 11,568,941, and 12,010,838 against Micron (the “YMTC2 case”). On August 21, 2024, the YMTC2 case was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer*

Petition for *Inter Partes* Review of U.S. Patent No. 11,581,322

*Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”).

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

| Patent                               | PTAB Proceeding | Wave             |
|--------------------------------------|-----------------|------------------|
| T10,658,378 (claims 15-17 and 19-20) | IPR2024-00788   | Wave 1 Petitions |
| 10,861,872 (claims 1-6 and 11-13)    | IPR2024-00789   |                  |
| 10,868,031                           | IPR2024-00790   |                  |
| 10,937,806 (claims 8-9 and 11-12)    | IPR2024-00791   |                  |
| 10,950,623                           | IPR2024-00794   |                  |
| 11,468,957                           | IPR2024-00792   |                  |
| 11,501,822                           | IPR2024-00795   |                  |
| 11,600,342 (claims 1-6 and 8-20)     | IPR2024-00793   |                  |
| 10,658,378 (claims 1-7 & 18)         | IPR2024-00909   | Wave 2 Petitions |
| 10,861,872 (claims 7-10)             | IPR2024-00910   |                  |
| 10,937,806 (claim 10)                | IPR2024-00911   |                  |
| 11,600,342 (claim 7)                 | IPR2024-00912   |                  |
| 10,672,711                           | IPR2025-00117   | Wave 3 Petitions |
| 10,879,164                           | IPR2025-00118   |                  |
| 10,879,254                           | IPR2025-00034   |                  |
| 10,879,254                           | IPR2025-00119   |                  |

Petition for *Inter Partes* Review of U.S. Patent No. 11,581,322

| Patent     | PTAB Proceeding | Wave |
|------------|-----------------|------|
| 10,886,291 | IPR2025-TBD     |      |
| 11,101,276 | IPR2025-00228   |      |
| 11,145,666 | IPR2025-00189   |      |
| 11,450,604 | IPR2025-00035   |      |
| 11,482,532 | IPR2025-TBD     |      |
| 11,568,941 | IPR2025-00190   |      |
| 12,010,838 | IPR2025-00229   |      |

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a).

**C. Counsel, Service, and Fee Information**

Petitioner designates the following counsel:

| Lead Counsel                                                                                                                                                                                                                                             | Back-Up Counsel                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>Jeremy Jason Lang<br/>Registration No. 73,604<br/>(jlang@orrick.com)</p> <p>Postal &amp; Hand-Delivery Address:<br/>Orrick, Herrington &amp; Sutcliffe LLP<br/>1000 Marsh Road<br/>Menlo Park, CA 94025-1015<br/>T: 650-614-7400; F: 650-614-7401</p> | <p>Thomas James<br/>Registration No. 74,109<br/>(tjames@orrick.com)</p> <p>Postal &amp; Hand-Delivery Address:<br/>Orrick, Herrington &amp; Sutcliffe LLP<br/>353 N Clark Street<br/>Suite 3600<br/>Chicago, IL 60654<br/>T: 312-924-9800 F: 312-924-9899</p> <p>Jared Bobrow<br/><i>Pro Hac Vice</i> to be submitted<br/>(jbobrow@orrick.com)</p> <p>Postal &amp; Hand-Delivery Address:<br/>Orrick, Herrington &amp; Sutcliffe LLP<br/>1000 Marsh Road<br/>Menlo Park, CA 94025-1015<br/>T: 650-614-7400; F: 650-614-7401</p> |

Petitioner consents to service by electronic mail at the following addresses:  
PTABDocketJJL2@orrick.com, PTABDocketT6J1@orrick.com,  
PTABDocketJ3B3@orrick.com, and Micron-YMTC\_ohs@orrick.com. Pursuant to  
37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

The USPTO is authorized to charge the fee specified by 37 C.F.R. §42.15(a),  
and any other required fees, to Deposit Account No. 15-0665.

### III. REQUIREMENTS FOR *INTER PARTES* REVIEW

#### A. Grounds for Standing

Petitioner certifies that the '322 Patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Petitioner was served with a complaint alleging infringement of the '322 Patent on July 12, 2024.

#### B. Identification of Challenge and Statement of Precise Relief Requested

Petitioner requests *inter partes* review of claims 1-20.

This Petition assumes that the '322 Patent is entitled to its earliest-listed priority date: August 21, 2018. Ex. 1001, Cover, p. 2.

Petitioner relies on the following references: (1) Nishikawa (Ex. 1005), (2) Lu (Ex. 1006), and (3) Nishikawa2 (Ex. 1046). These references are prior art. See Section IX.

Petitioner challenges the claims on the following grounds:

**Ground 1:** Claims 1-3, 6, 7-10, 13-16, and 19-20 are obvious over Nishikawa.

**Ground 2:** Claims 4-5, 11-12, and 17-18 are obvious over Nishikawa in view of Lu.

**Ground 3:** Claims 1-3, 6, 7-10, 13-16, and 19-20 are obvious over Nishikawa in view of Nishikawa2.

**Ground 4:** Claims 4-5, 11-12, and 17-18 are obvious over Nishikawa in view of Nishikawa2 and Lu.

#### **IV. INSTITUTION SHOULD BE GRANTED**

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

##### **A. There are No Grounds for a § 314 Discretionary Denial in this Case**

Petitioner submits that it presents a “compelling” case and thus the Board should not discretionary deny. 6/21/22 Interim Procedure, 2, 4-5.

Petitioner also notes that the discretionary denial factors collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential).

##### **1. Possibility of a Stay**

Petitioner intends to seek a stay if the Board institutes IPR. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Grp. – Trucking LLC*, IPR2019-01393, Paper 24, 7 (PTAB June 16, 2020) (informative); *Fintiv*, 6-9, 12 (similar).

##### **2. Proximity of the Court’s Trial Date**

On September 18, 2024, the district court entered a scheduling order which set a trial date of June 15, 2026. *See* Ex. 1042. As a result, if IPR proceedings are instituted, they should be completed before the scheduled trial date. *See also* Ex. 1043 (statistics indicating that it takes on average 48.9 months to reach trial in district court). This weighs strongly in favor of institution.

### **3. Investment in the Parallel Proceeding**

Regarding the Co-Pending Litigation, to date, the parties and the district court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. *See* §II.B. Virtually no progress has been on the Wave 3 patents (which includes the '322 Patent). The parties just completed the exchange of contentions for the Wave 3 patents (from the YMTC2 case) but have not taken any depositions in the entire Co-Pending Litigation. Fact discovery is in its infancy. No claim construction positions have been exchanged for the Wave 3 patents, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution*, 10-11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv*, 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner, and subsequently asserted 149 claims across those patents. Ex. 1044. Petitioner proceeded with diligence, starting the filing of eleven petitions approximately three months after being served with the YMTC2 complaint. Ex. 1045. This also weighs strongly in favor of institution.

### **4. Issue Overlap**

Should the Board institute, Micron stipulates that it will not advance in

District Court any ground asserted in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution*, 11-12.

**5. Party Overlap**

As is normal, both Petitioner and Patent Owner are parties in the parallel proceeding.

**6. Other Circumstances**

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

**B. Denial Under §325(d) Would Be Inappropriate**

The Examiner did not consider Nishikawa, Nishikawa2, or Lu, and thus denial under §325(d) would be inappropriate. Moreover, the apparent point of novelty of, e.g., claim 1 of the '322 Patent, is burying a TAC in a substrate and providing slit structures to sub-divide the memory. See §VI. Nishikawa discloses exactly that. See §IX.A. And Nishikawa2 states that the TAC may be “circular.” See §§IX.A, X.A.5.

Further, as demonstrated in §VI although the Examiner analyzed a similar TAC in a different, unrelated Nishikawa patent, the Examiner did not analyze any reference that discloses such a TAC along with a slit. The Nishikawa reference of

Grounds 1-2 discloses the combination of a TAC and a slit. See §IX.A. The Examiner also was not aware of prior art which teaches that common source connections need not be in the form of trenches. See §X.A.5. Thus, Nishikawa and the supporting references herein cannot be cumulative to any prior art of record because Nishikawa and the supporting references teach the exact features that were used to distinguish the '322 Patent from the prior art during prosecution.

## V. TECHNOLOGY BACKGROUND

In a 3D NAND flash memory, memory cells exist in vertical, cylindrical NAND flash “strings”:

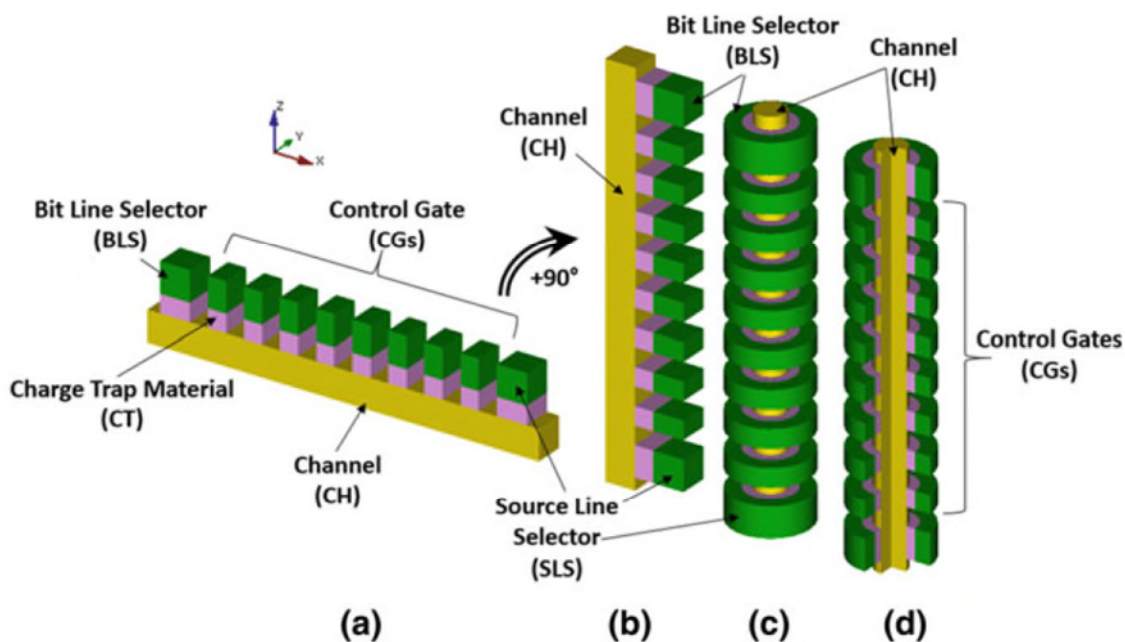


**Fig. 4.1** NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

Ex. 1010, 102. As labeled in Figure 4.1, above, each NAND string includes a “cylindrical channel.” *Id.*; Lee, ¶¶ 45-48.

A number of 3D architectures were well known, e.g., in the BiCS (Bit Cost Scalable) architecture, various “contacts,” that is, electrical connections, are on top of the memory array. These include source line contacts (for providing a ground connection to the memory cells):

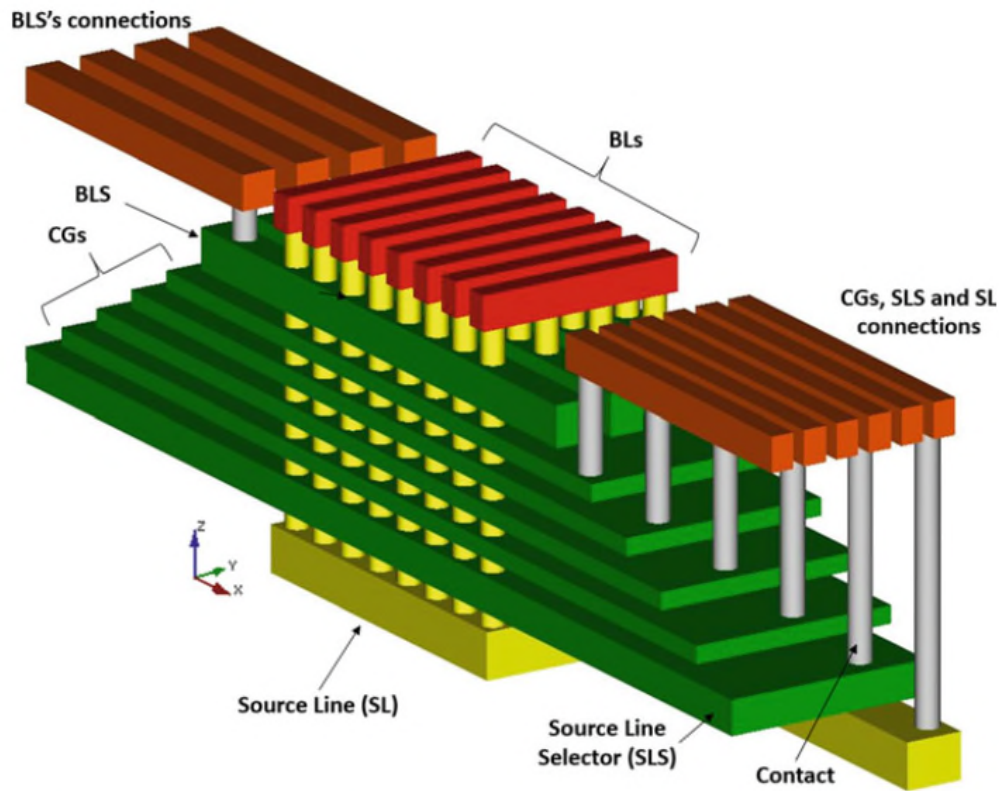


**Fig. 4.13** Top bird's eye view of BiCS with gate connections

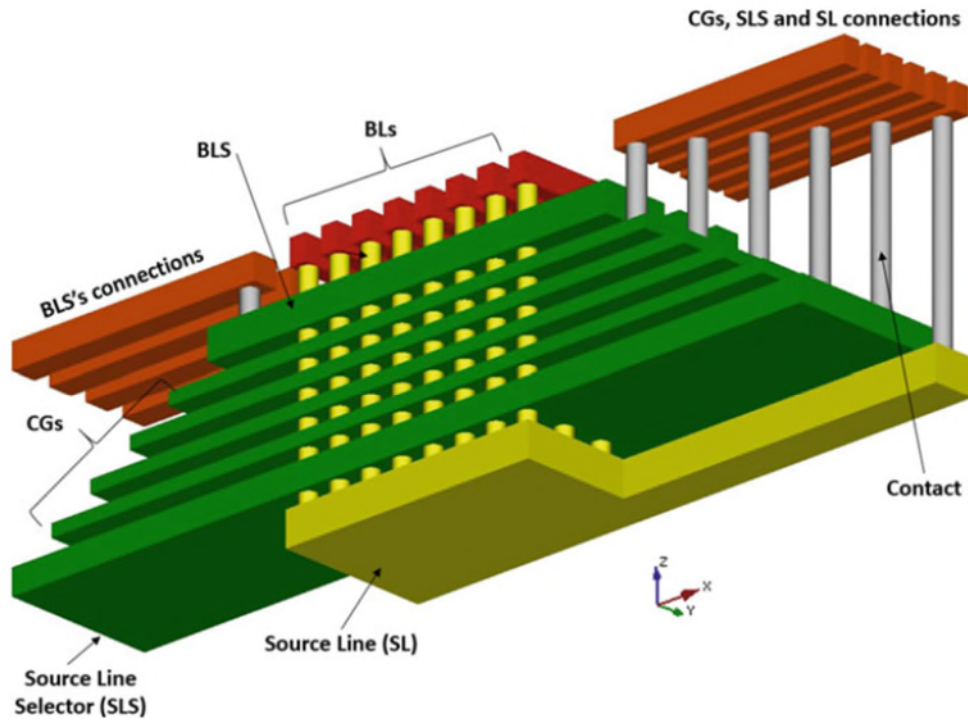


**Fig. 4.14** Bottom bird's-eye view of BiCS with gate connections

Ex. 1010, 109-110; Lee, ¶ 49. The above illustrates source line contacts that extend from the top of the device to the bottom, but do not travel through the stack. It was well known, however, to form contacts (which are typically cylindrical in shape) directly through the memory stack. The below provides several examples:

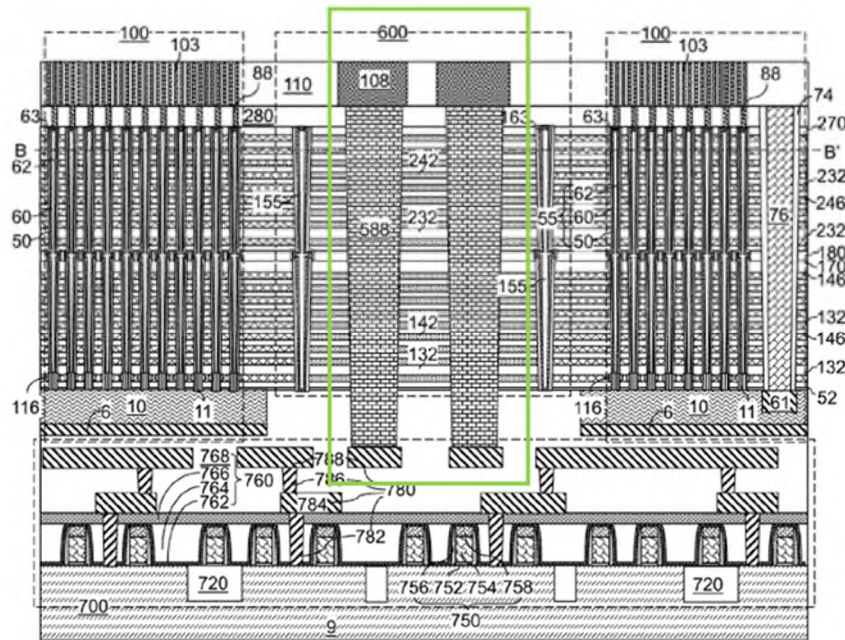


FIG. 69A

Ex. 1011 (U.S. Pat. Pub. 2017/0179026, Toyama), Title (“Through-Memory-Level Via Structures”), [0367], Fig. 69A (588).

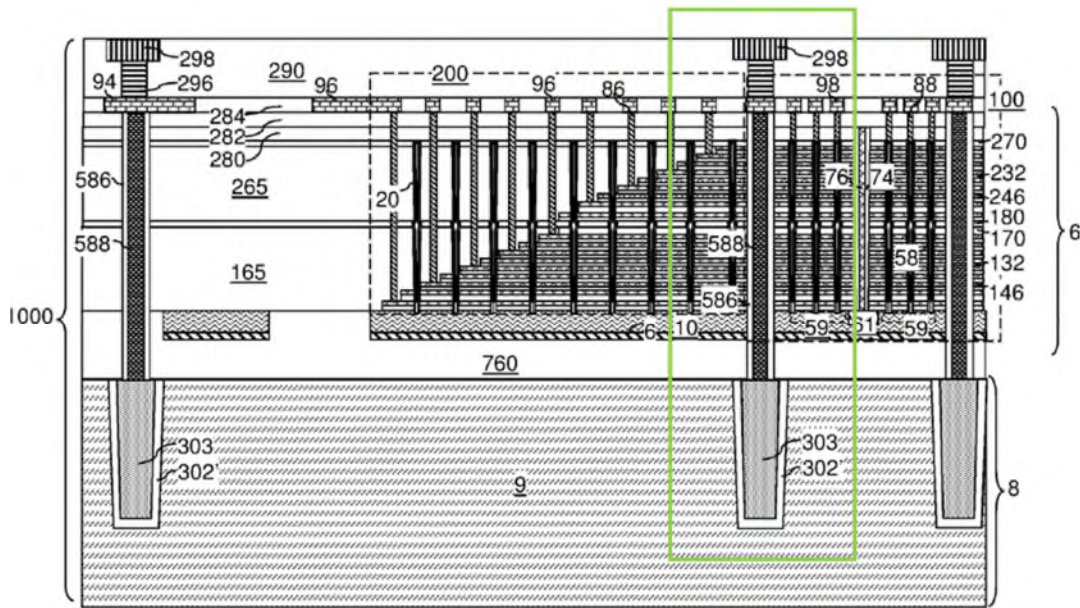
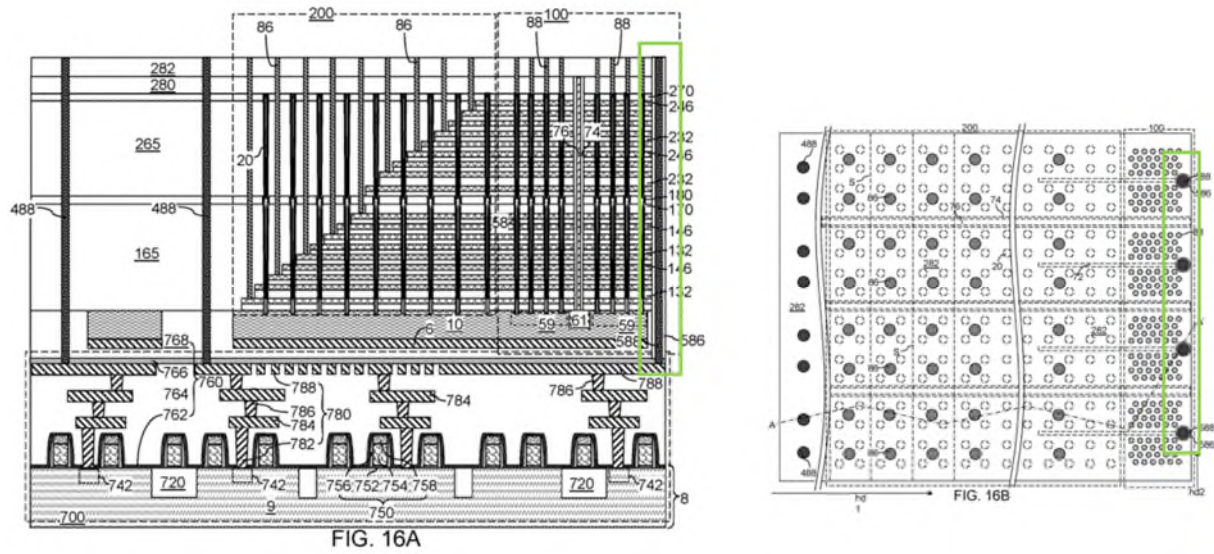
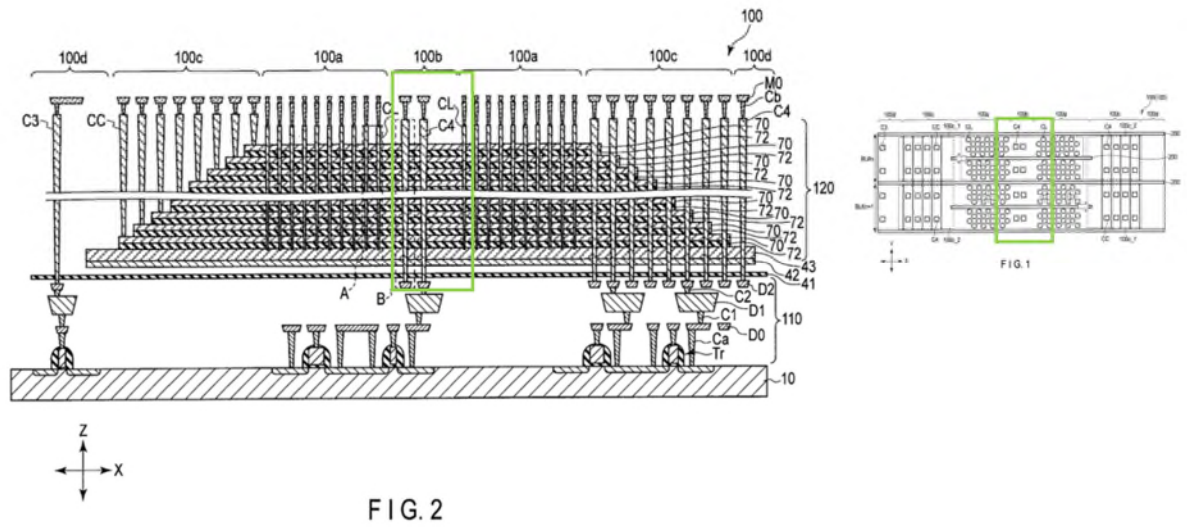


FIG. 5

Ex. 1012 (U.S. Pat. 10,354,980, Mushiga), 10:31-58, Fig. 5 (588).



Ex. 1008 (U.S. Pat. Pub. 2019/0229125), [0189], Figs. 16A, 16B (588).



Nakajima, Figs. 1-2, 6:45-52; Lee, ¶¶ 50-51.

The memory cells' control gates form a staircase structure as shown below:

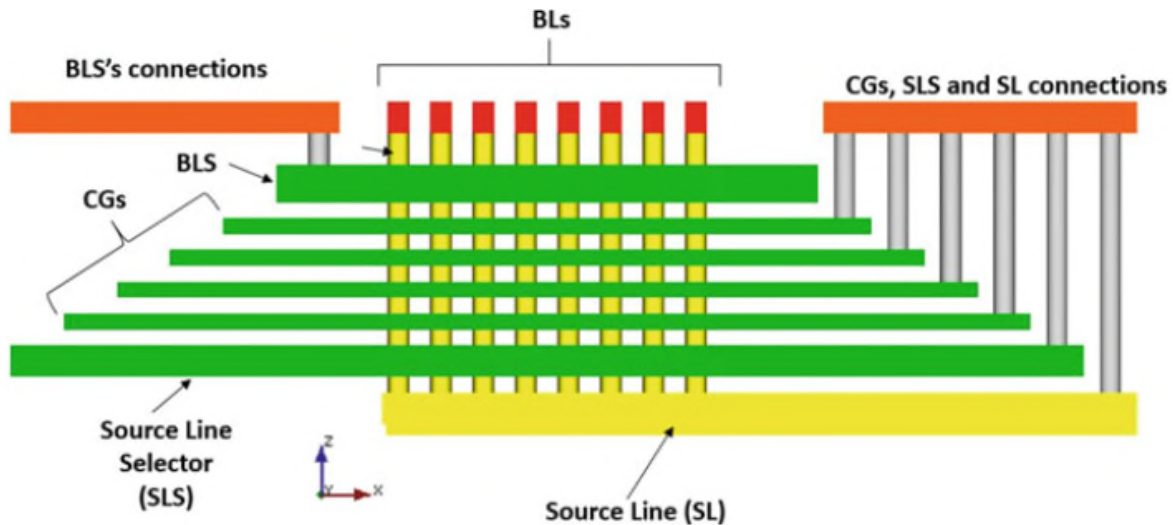


**Fig. 4.12** Vertical cross section of BiCS with gate connections

Ex. 1010, 109 (green control gates forming a staircase). Each control gate delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device. The memory cells that a single control gate controls are together a “word,” and the control gate is a “word line.” Ex. 1015 (Aritome), 38-40. Reflecting this, the grey columns contacting the top surface of the control gates (shown above in green) are “word line contacts.” Lee, ¶ 52.

Various modifications to the BiCS structure were known, including the use of slit structures, which extend vertically through the memory stack and extend laterally through the device, to serve as source line contacts for the NAND strings. As can be seen, these slits also segment the array into blocks:

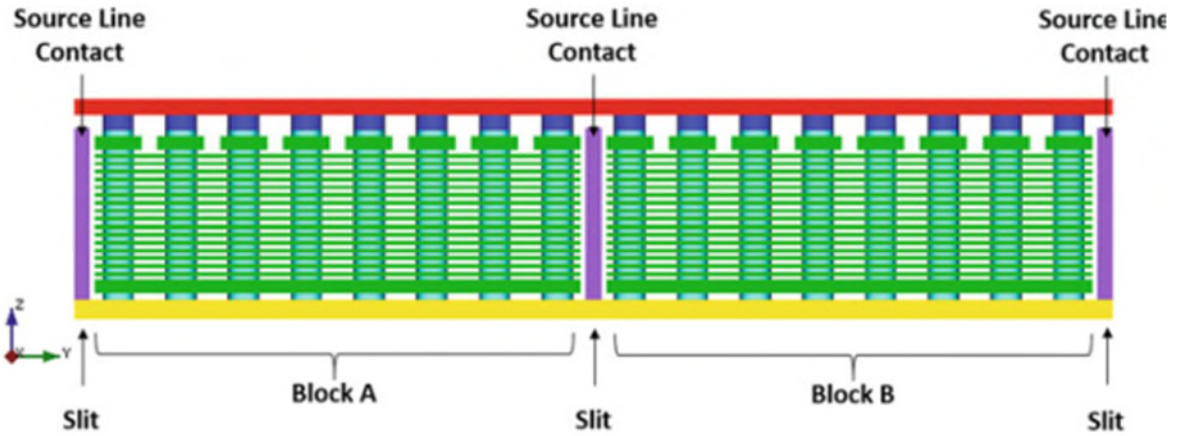


**Fig. 6.8** Side view of Fig. 6.7

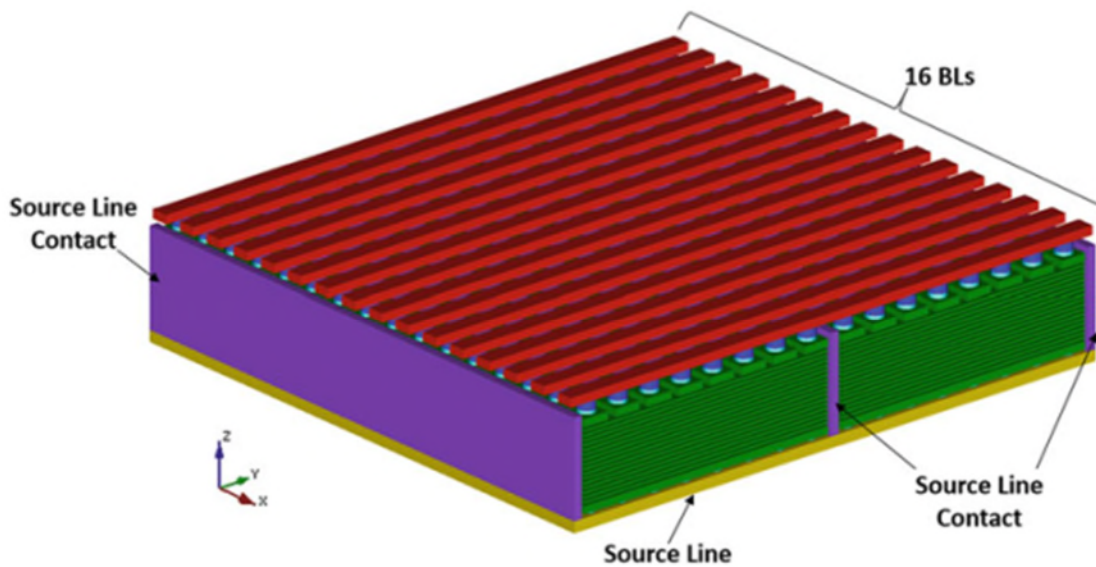


**Fig. 6.7** Array slits

Ex. 1010, 185.

In each of the above figures, there are various gaps between the depicted structures. These gaps are actually filled with an insulating material (a dielectric). The stack of alternating gate layers (wordlines) and insulating layers is known as the memory stack. Lee, ¶¶ 53-57.

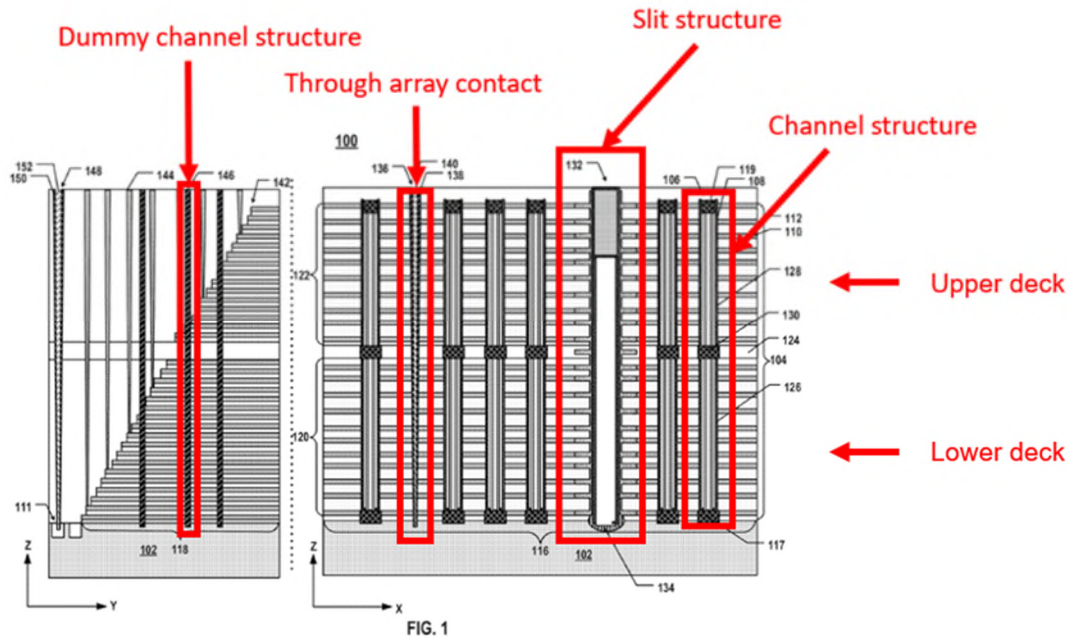
In sum, techniques for manufacturing 3D NAND memory stacks, TACs, and slits were well-known in the art before the '322 Patent's priority date. Lee, ¶ 58.

## **VI. THE '322 PATENT AND ITS PROSECUTION HISTORY**

The '322 Patent primarily relates to contacts that extend through the memory stack, i.e., “through array contacts” (“TACs”). TACs were known. *See* §V. Indeed, as the below file history summary demonstrates, the Applicant made minor distinctions to distinguish the art. For claim 1, the Applicant argued that claimed memory includes a dividing slit, and for other independent claims, it argued that the claims require a circular TAC.

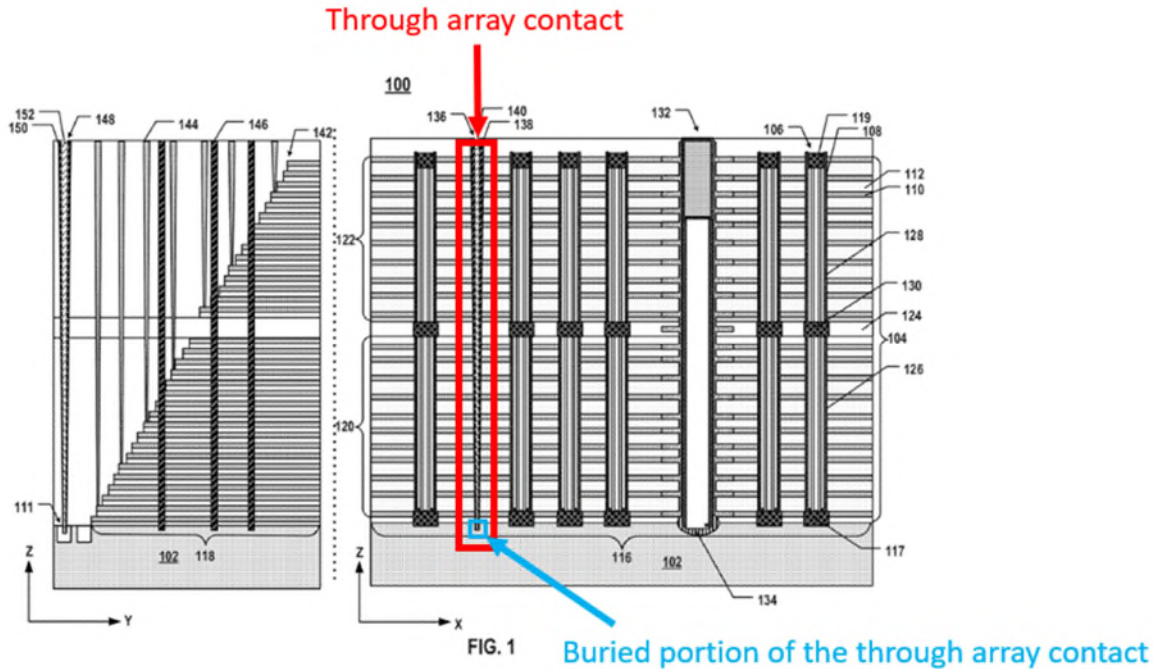
The specification of the '322 Patent generally describes well-known monolithic 3D memory structures that are formed along with the TACs: channel structures, dummy channel structures, peripheral contacts, slits (e.g., which may be used during the gate replacement process), and multi-deck memory stacks. Ex 1001, 6:49-61-7:4 (channels), 7:42-60 (multi-deck memory stack), 9:29-51 (dummy channels), 8:3-18 (slit structures), 9:52-10:8 (peripheral contacts).

Fig. 1 of the '322 Patent depicts the 3D memory structure with these basic elements. For example, Fig. 1 of the '322 Patent illustrates channel structures 106, a slit structure 132, a through array contact 146, and a dummy channel structure 146 in a 3D multi-deck memory stack.



Ex. 1001, Fig. 1 (annotated); Lee, ¶¶ 60-62.

The specification describes that “[i]n some embodiments, TAC 136 further extends through at least part of substrate 102.” Ex. 1001, 8:37-38. For example, a portion of the TAC depicted below extends below the surface of a substrate and terminates in the substrate:



*Id.*, Fig. 1 (annotated).

Certain claims require a slit structure that divides the array. The '322 Patent discloses that “[i]n some embodiments, 3D memory device 100 further includes slit structures 132. Each slit structure 132 can extend vertically through the conductor/dielectric layer pairs in memory stack 104. Slit structure 132 can also extend laterally (e.g., in the y-direction) to separate memory stack 104 into multiple blocks.” Ex. 1001, 8:3-8. The claims, however, do not require that the slit perform any type of function or comprise any particular material. The '322 Patent states only that in some embodiments, the slit structure may function as a source contact. *Id.*, 8:8-29; Lee, ¶¶ 63-65.

The file history is particularly instructive about the alleged point of novelty. The 322 Patent is a divisional of App. No. 16/745,342. Ex. 1001, Cover. There, the

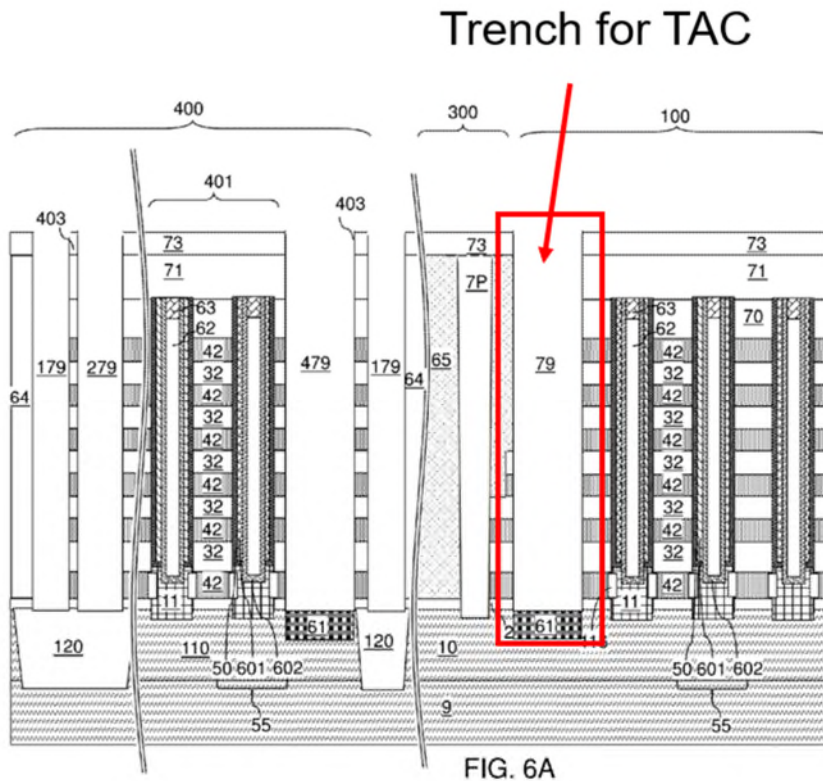
pending claims, which included the TAC limitation (but without the TAC being buried), were rejected over U.S. Publ. 2012/0280304 (“Lee 304”). Ex. 1016, 114-15. Of note, Lee 304 disclosed a TAC that was a common source line (trench), i.e., not a circular TAC. *Id.*; Ex. 1017 (Lee 304), Fig. 23, [0051], [0058]-[0059], [0095]. To obtain allowance, Applicant amended the claims to require that each conductive layer of the memory stack have a “shallow recess.” Ex. 1016, 148, 153, 157, 166.

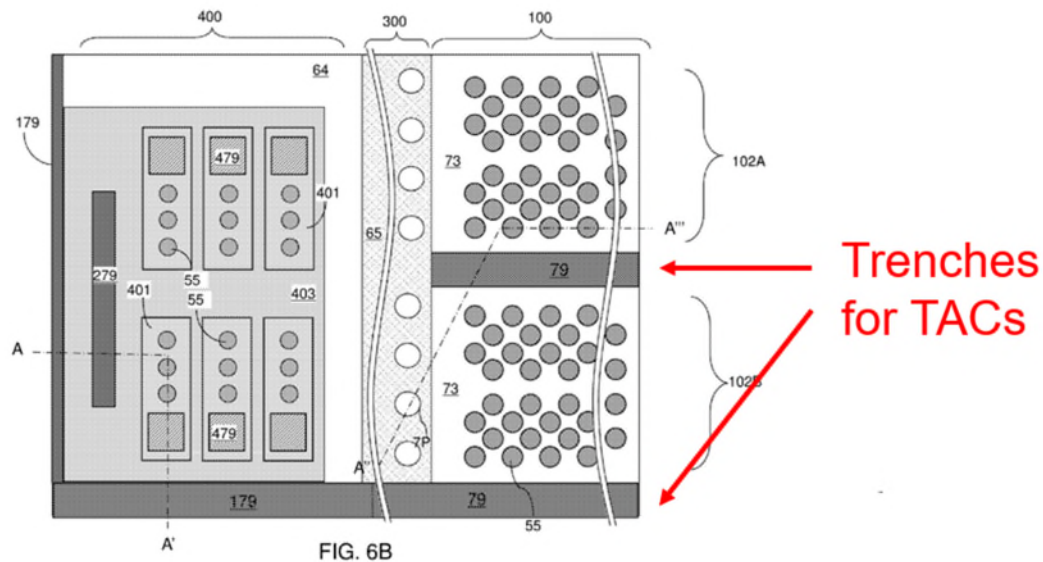
The original claims of the ’322 Patent did not include the “buried” TAC or “slit” limitations. Ex. 1002, 20. The claims were rejected over Lee 304 again, but this time in view of U.S. 2017/0125430 (Ex. 1018, “Nishikawa 430”). *Id.*, 100-01.

After an Examiner Interview, claim 1 was amended to also require a peripheral contact and that the thickness of the spacers for the peripheral contact and TAC be the same. Ex. 1002, 145-46, 149-152. Applicant attempted to distinguish the claims over Lee 304 and Nishikawa 430 based on the spacer limitation. *Id.*, 155. The Examiner rejected the claims again, this time based on Lee 304, Nishikawa 430, and U.S. 2015/0348987 (Ex. 1019, “Lee 987”). Ex. 1002, 162-163. The Examiner relied on Lee 987 for a peripheral contact and assigned no patentable weight to the spacer limitation. *Id.*, 164.

After an Examiner Interview, claim 1 was amended by deleting the dummy channel, peripheral contact, and spacers’ thickness limitations, and by adding the “buried” TAC and “slit” limitations. Ex. 1002, 210, 216. Claim 10 was amended to

require a circular TAC, and claim 17 was amended to require a TAC with a diameter. *Id.*, 217, 219. Applicant noted that the Examiner agreed that Lee 304 did not disclose a TAC buried in the substrate. *Id.*, 223. This appears to be in error. Lee 304, [0058]; Lee, ¶¶ 69-70. More importantly, Applicant noted that during the Interview, the Examiner cited Nishikawa 430's opening 79 as the TAC buried in the substrate. Ex. 1002, 223. Nishikawa 430's opening 79 is a trench that, ultimately, functions as a common source:





Nishikawa 430, Fig. 6A, [0084], [0086]. [0113]-[0115] (79 becoming “contact structures 76”); Lee, ¶ 71.

Faced with Nishikawa 430’s disclosures of a buried TAC, for claim 1, Applicant argued that the prior did not disclose the combination of a TAC buried in the substrate **and** a slit that separates the array. Ex. 1002, 222-23. As shown above, with Nishikawa 430’s 79 becoming a TAC, namely, “active region contract structure 76” (which itself is the form a slit that divides the array), there is no additional slit structure. For the two remaining independent claims, Applicant argued that the circular TAC requirement distinguishes Nishikawa 430’s TAC and the other prior art TACs. *Id.*, 223-24; Lee, ¶¶ 72-73.

The claims were allowed, and the Examiner noted the alleged distinguishing requirements of claim 1: the buried TAC **and** slit limitations. Ex. 1002, 249. For

claims 10 and 17, the Examiner noted that the circular requirements led to allowance. *Id.*, 250. The Examiner noted that nothing in the prior art of record suggested using a circular TAC. *Id.*; Lee, ¶ 74.

## **VII. CLAIM CONSTRUCTION**

For purposes of this Petition, Petitioner submits that no terms of the '322 Patent require construction, and the terms should receive their plain and ordinary meaning. Lee, ¶¶ 77-80.

## **VIII. LEVEL OF ORDINARY SKILL IN THE ART**

A POSITA in the field of the '322 Patent would have had a Bachelor of Science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts. See Lee, ¶¶ 34-38.

## **IX. DESCRIPTION OF THE PRIOR ART**

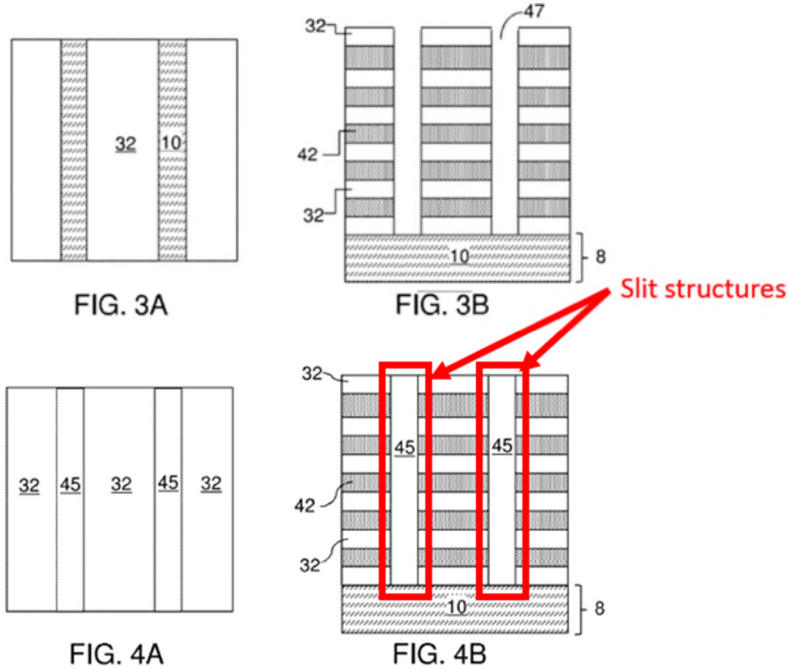
### **A. Nishikawa**

U.S. Patent No. 9,837,431 to Nishikawa et al. was filed on January 28, 2016, was issued on December 5, 2017, claims priority to a provisional application filed on November 20, 2015, and is prior art under 35 U.S.C. § 102(a)(1).



FIG. 1

Nishikawa further includes slit structures such as “separator dielectric structures 45”:



Nishikawa, Figs. 3A-B, 4A-B (annotated).

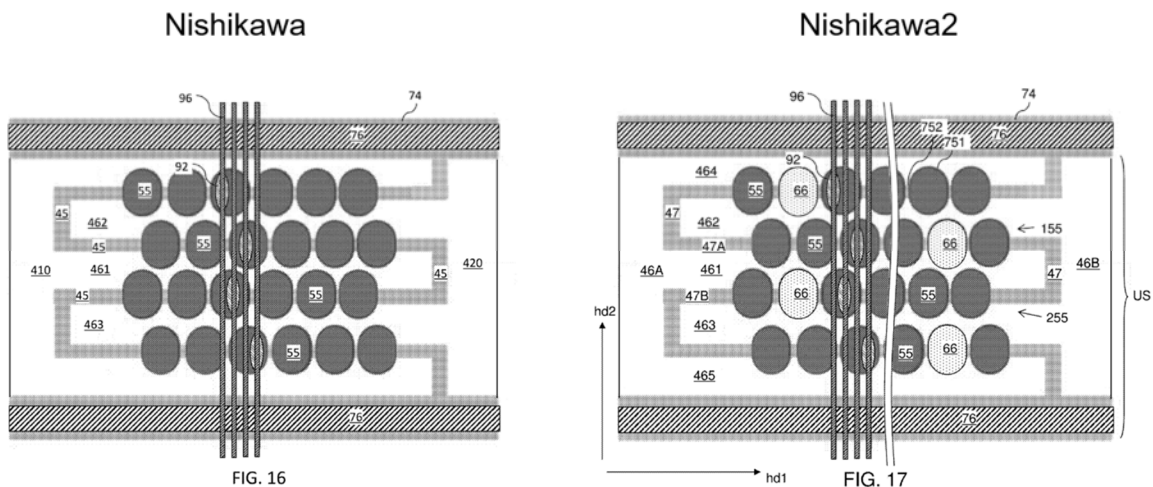
Nishikawa explains that the separator dielectric structures 45 divide the memory into multiple memory zones: “Each separator dielectric structure 45 can extend through the alternating stack (32, 42), i.e., from the top surface of the substrate 8 to the top surface of the alternating stack (32, 42). Thus, the alternating stack (32, 42) as formed at the processing steps of FIGS. 2A and 2B is divided into multiple laterally disjointed portions by the separator dielectric structures 45, each of which comprises discrete portions of the alternating stack (32, 42).” Nishikawa, 8:36-43; *see also id.*, 8:57-60, 9:1-24, 13:18-22, 14:52-15:3, 17:24-27; Lee, ¶¶ 86-87.

While Nishikawa does not expressly disclose circular TACs, Nishikawa2 states that the TACs may be “circular.” This Petition also demonstrates that circular TACs, as well as circular TACs that serve the same function as Nishikawa’s TACs, were widespread well before the effective filing of the ’322 Patent. *E.g.*, §V.

## B. Nishikawa2

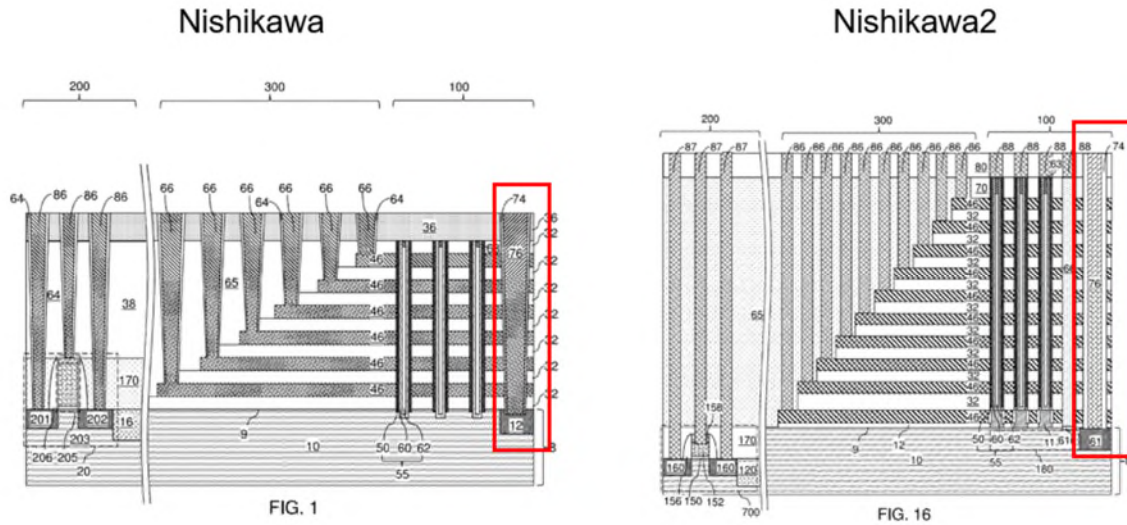
U.S. Patent No. 9,935,123 to Nishikawa et al. was filed on July 26, 2016, was issued on April 3, 2018, claims priority to a provisional application filed on November 25, 2015, and is prior art under 35 U.S.C. § 102(a)(1).

Nishikawa2 relates to the same memory architecture of Nishikawa:



Nishikawa, Fig. 16; Nishikawa2, Fig. 17; Lee, ¶¶ 88-90.

Nishikawa and Nishikawa2 disclose the same TAC that serves as a source line connection:



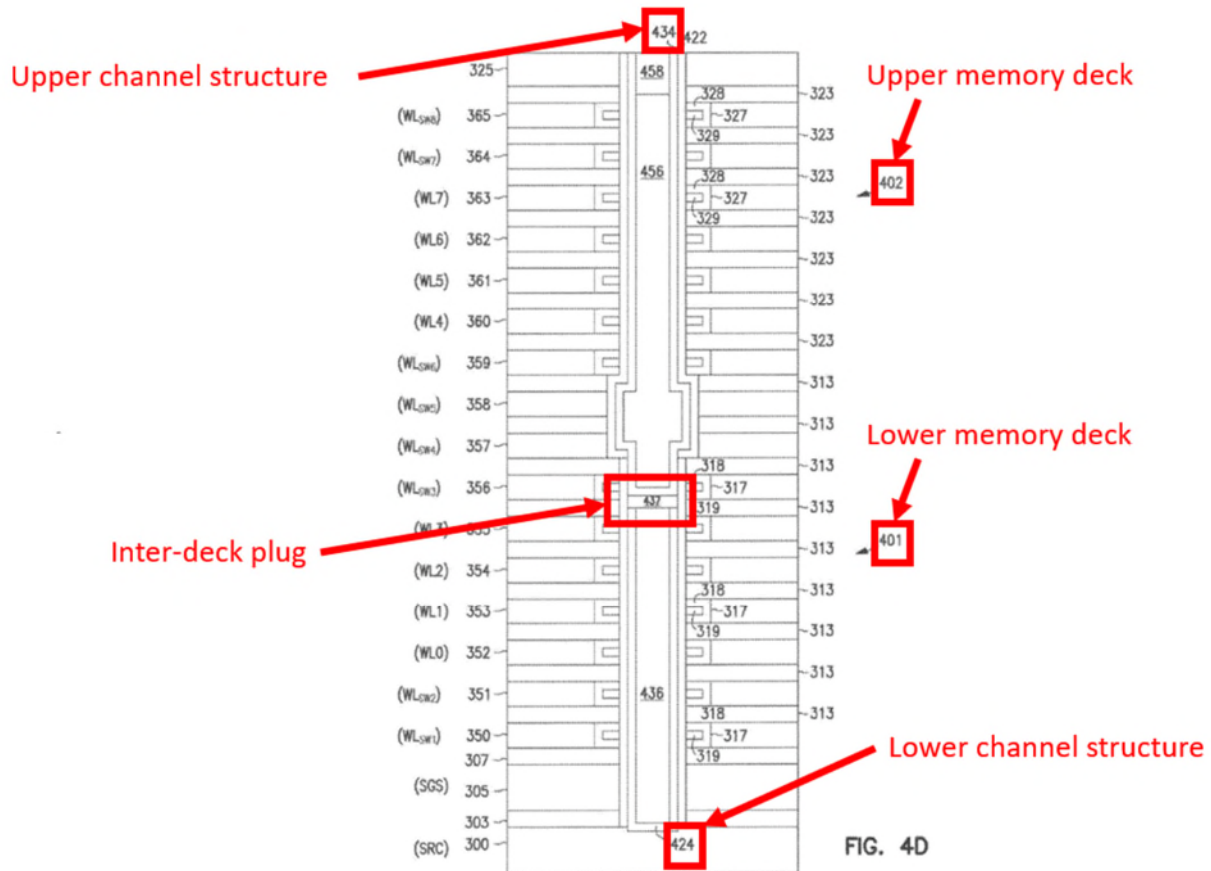
Nishikawa, Fig. 1; Nishikawa2, Fig. 16, 22:34-38 (source line connection), 23:59-67 (insulating spacer 74), 24:24-39 (forming “backside contact via structure 76” in “backside trench 79”).

Notably, Nishikawa2 states that this source line structure may be circular: “The openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape.” Nishikawa2, 22:38-41; Lee, ¶ 91.

### C. Lu

U.S. Patent No. 9,853,046 to Lu et al. is titled “Apparatuses and Methods for Forming Multiple Decks of Memory Cells,” was filed on June 6, 2016, issued on December 26, 2017, is a division of U.S. Application No. 14/509,621 filed on October 8, 2014, and is prior art under 35 U.S.C. § 102(a)(1). Like the ’322 Patent, Lu is directed to forming three-dimensional memory devices. Lu, 7:42-46.

Lu discloses a memory stack where channel regions are formed to include an upper and lower channel structures and where an inter-deck plug is formed therebetween. Lu, 14:13-61.



Lu, Fig. 4D (annotated); Lee, ¶¶ 92-94.

**X. GROUND 1: NISHIKAWA IN VIEW OF THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 1-3, 6-10, 13-16, AND 19-20**

**A. Claim 1:**

**1. [1.PRE] “A three-dimensional (3D) memory device, comprising:”**

Nishikawa discloses a three-dimensional (3D) memory device. *E.g.*, Nishikawa, 2:3-3:41 (“3D NAND stacked memory device”); 1:15-19 (“vertical NAND strings”), 4:22-24 (“3D NAND stacked memory device[s]”); Lee, ¶ 95.

**2. [1.A] “a substrate;”**

Nishikawa discloses a substrate (“substrate 8”).

Nishikawa discloses that the “substrate 8” includes a “substrate semiconductor layer 10” (Nishikawa, 4:43-56) and a “source region 12” (*id.*, 5:16-18).

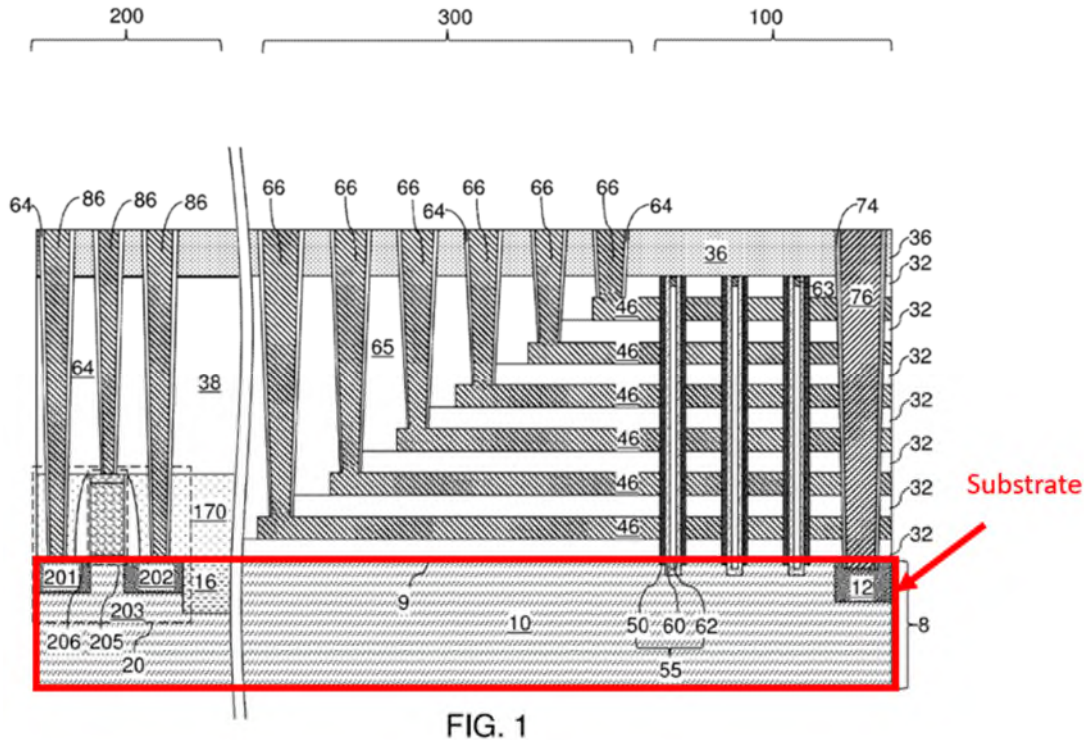


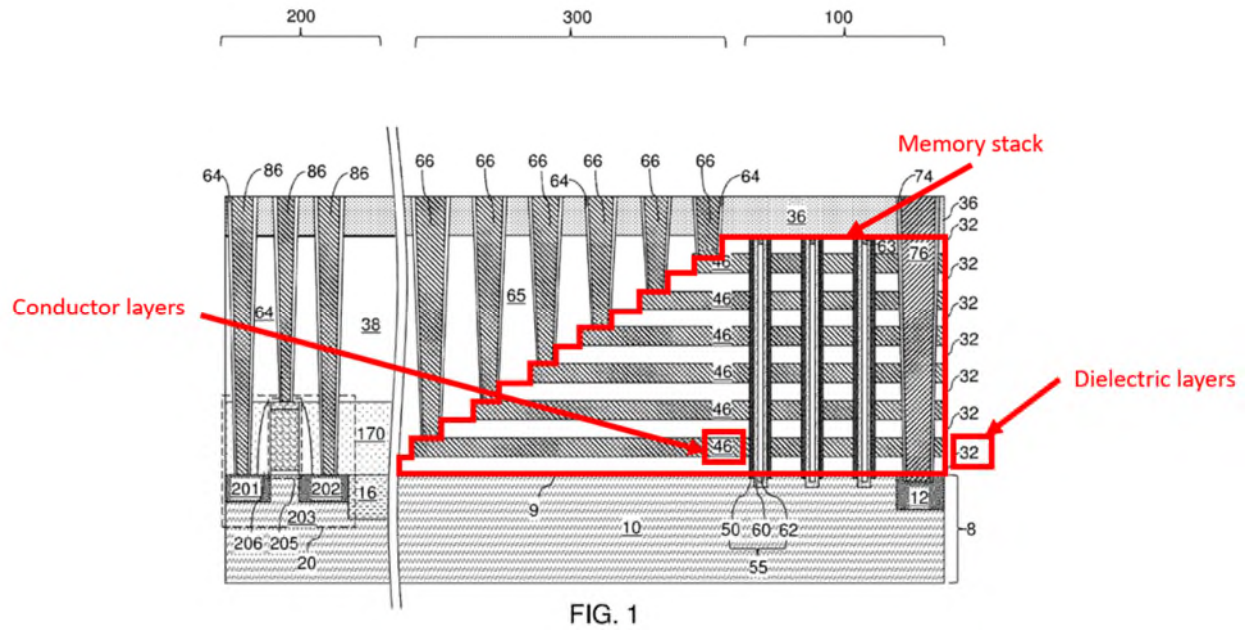
FIG. 1

*Id.*, Fig. 1 (annotated); Lee, ¶¶ 96-97.

**3. [1.B] “a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;”**

Nishikawa discloses a memory stack (“alternating stack”) on the substrate (“substrate 8”) and comprising a plurality of conductor (“electrically conductive layers 46”)/dielectric layer (“insulating layers 32,” e.g., silicon oxide) pairs.

Specifically, Nishikawa discloses an “alternating stack (32, 46) of the insulating layers 32 and the electrically conductive layers 46.” Nishikawa, 6:4-5.



*Id.*, Fig. 1 (annotated). The insulating (dielectric) layers 32 and the conductor layers 46 are formed alternatively on the top surface of the substrate 8, i.e., form pairs (32/46). Nishikawa, 5:50-6:2; Lee, ¶¶ 98-99.

Nishikawa discloses that the insulating layer 32 can be formed using, e.g., “silicon oxide,” i.e., dielectric layers. Nishikawa, 7:3-16; Lee, ¶ 100.

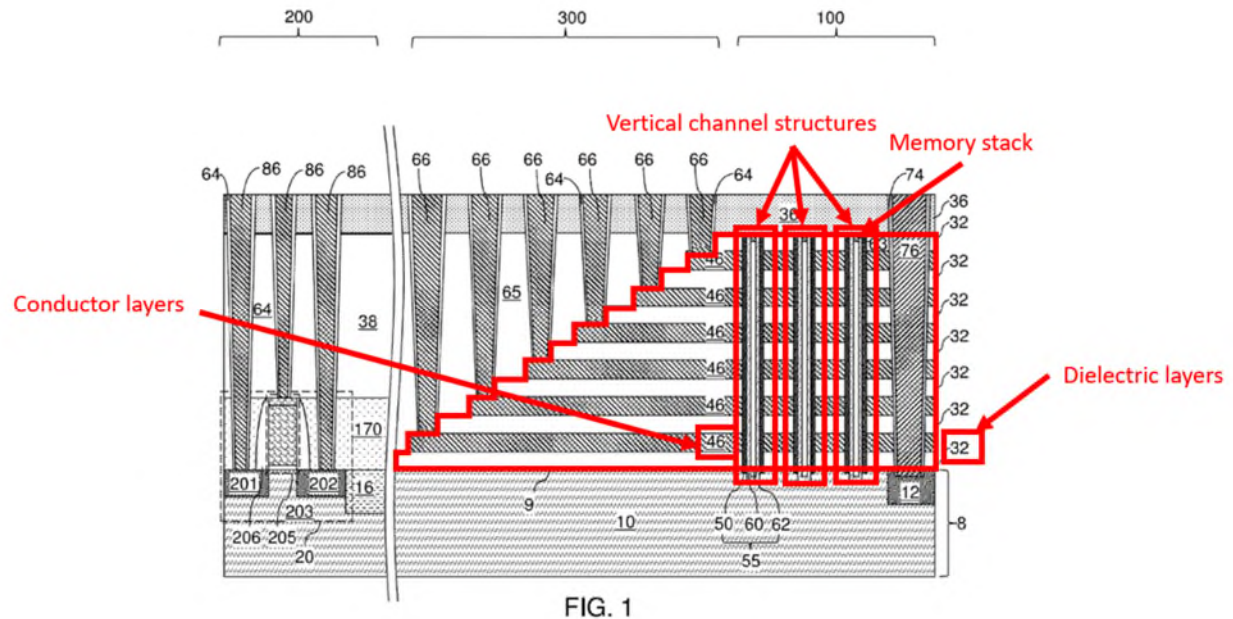
Nishikawa further discloses that “memory stack structures 55” are formed through the memory stack (32/46 pairs). Nishikawa, 6:3-8. Nishikawa’s memory stack is coextensive with the alternating stack of insulating layers 32 and electrically conductive layers 46. Lee, ¶ 101.

**4. [1.C] “a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;”**

Nishikawa discloses a channel structure (“memory stack structure 55”) extending vertically through the conductor (“electrically conductive layers

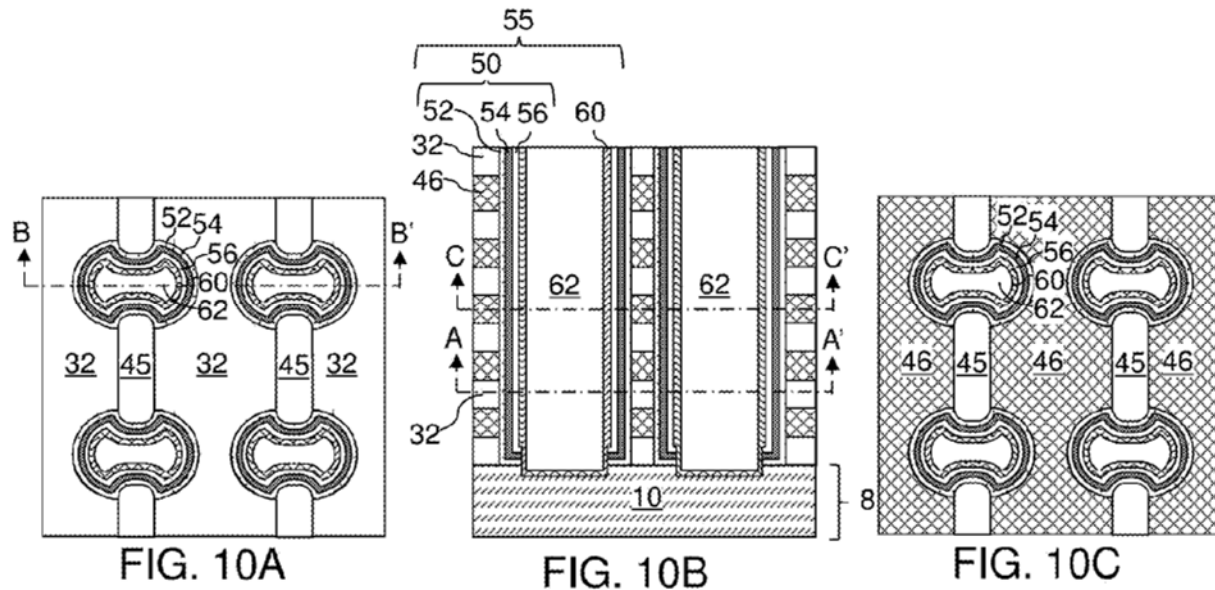
46”)/dielectric (“insulating layers 32”) layer pairs in the memory stack (“alternating stack”).

First, as illustrated in annotated Fig. 1, below, the memory stack structure[s] 55 of Nishikawa are channel structures:



Nishikawa, Fig. 1 (annotated). Memory stack structures 55 are channel structures because they contain a vertical semiconductor channel 60. Nishikawa discloses, “[r]eferring to FIGS. 10A-10C, a memory stack structure 55 (i.e., structure having layers (52, 54, 56, 60)) including a memory film 50 (i.e., film having layers (52, 54, 56)) and a vertical semiconductor channel 60 can be formed in each of the memory openings 49. Each memory film (52, 54, 56) can include, from outside to inside, a blocking dielectric layer 52, charge storage regions 54, and a tunneling dielectric

46.” Nishikawa, 11:33-39. In other words, the channel structure is a string of memory cells in which a channel forms. Lee, ¶¶ 102-04.



Nishikawa, Figs. 10A-C.

Second, as illustrated in annotated Fig. 1, below, the channel structures of Nishikawa (“memory stack structure[s] 55”) extend vertically through the conductor /dielectric layer pairs in the memory stack. Nishikawa, 6:3-5 (“The memory stack structures 55 can be formed through the alternating stack (32, 46) of the insulating layers 32 and the electrically conductive layers 46”); Lee, ¶ 106.

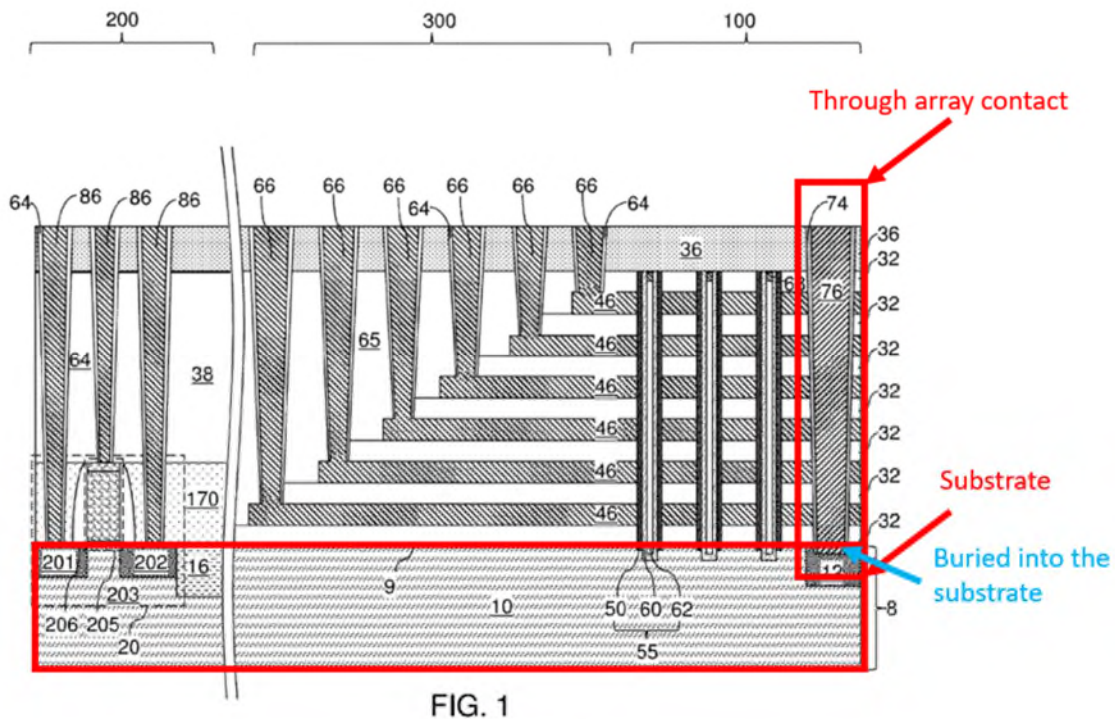
Nishikawa, Fig. 1 (annotated). Note that the channel structure extends from the top of the stack and into a source region the substrate. Nishikawa, 5:16-25; Lee, ¶ 107.

Nishikawa discloses a through array contact (TAC) (“backside contact via structure 76” and “dielectric spacer 74”) extending vertically through the conductor (“electrically conductive layers 46”)/dielectric (“insulating layers 32”) layer pairs in the memory stack (“alternating stack”) and buried into the substrate (“substrate 8”).

1001, 8:47-51. In other words, a TAC extends through the stack and includes a spacer and filling material, thereby providing a contact through the memory array. Nishikawa discloses exactly that. Lee, ¶¶ 108-109.

First, Nishikawa discloses that “[a] backside contact via structure 76 (e.g., source electrode/source local interconnect) can be formed through the alternating stack (32, 46) to provide electrical contact to the source region 12. A dielectric spacer 74 can be employed to provide electrical isolation for the backside contact via structure 76.” Nishikawa, 6:54-61. Note that “source electrode/source local interconnect” refers to the contact via structure 76 providing a connection to a source voltage above the substrate, through the stack, and down to the substrate (a common source region). *Id.*, 16:6-13 (providing source voltage to common source region of substrate); *see also* Ex. 1010, 109-110 (illustrating a common source contact). Contact via structure 76 would have been understood to include a conductive fill, e.g., tungsten, because Nishikawa describes providing an insulating liner for the contact, refers to it as a “contact,” and its function is to provide a source voltage to the substrate. Nishikawa, 6:54-61, 16:33-35, 16:6-13. Thus, the backside contact via structure 76 is a TAC because it includes a spacer and conductive filling material, and extends through each layer of the alternating stack; moreover, it is a functioning contact that provides a source voltage to the substrate. Lee, ¶¶ 110-11.

Second, as shown below, the TAC of Nishikawa (74, 76) extends vertically through the pairs of electrically conductive layers 46 and insulating layers 32 and is buried into the substrate 8 (it extends below the surface of the substrate 8 and terminates therein to provide the source connection to the substrate). Nishikawa, 6:54-61, 16:6-13. Again, the TAC extends through the memory stack because it forms a connection from above the stack down into the substrate (source region 12 in substrate 8). *Id.*, Lee, ¶ 112.



Nishikawa, Fig. 1 (annotated). As shown above, and in Figure 16, these TACs are proximate to the channel structures, which also travel through the full stack.

To the extent that PO argues that the backside contact is not a TAC because it is formed in a trench (i.e., is not circular) or because of its location (i.e., is not in the

middle of the stack), *see* Nishikawa, Fig. 16 (illustrating the backside contact via structure 76 as a trench towards the sides of the stack), PO would be incorrect.

To start, as demonstrated above, the '322 Patent defines a TAC without reference to its shape, that is, a TAC need only extend through the stack, have a spacer, and have a filling material. Nishikawa, 8:47-51. Nor does the specification require the TAC to be in any particular location (other than that it extends through the memory stack where channels are located, hence, reference to the “memory stack” in the limitation). *Id.* Further, the specification states that “[i]n some embodiments, TAC 136 has a substantially circular shape in the plan view, and conductor layer 140 and spacer 138 are disposed radially from the center of TAC 136 in this order.” In other words, only in some embodiments does a TAC have a circular shape. In fact, dependent claim 6 requires that the TAC have “a diameter” and claim 19 requires that TAC “has a substantially circular section” meaning that broader claim 1 requires no circular diameter (and thus no circular TAC). And the other independent claims (8 and 14) specifically recite a “circular” limitation, which would be redundant if a TAC inherently required a circular shape. Finally, the '322 file history demonstrates that Nishikawa’s contact via structure 76 is a TAC. PO had to amend the claims to add limitations, e.g., the “slit” and “circular” limitations, in view of a TAC in the form of a trench shape that provides a source connection. *See* §VI; Lee, ¶ 113.

Regardless, as explained below, employing a circular TAC, including in the middle of the stack, would have been obvious.

In Nishikawa, (1) the trench for the backside contact via structure 76 *may* serve as the opening for the gate replacement process and (2) the backside contact via structure 76 itself functions as a source line contact. Nishikawa, 5:50-61 (operational gate replacement process), 6:29-44 (gate replacement through trench), 9:58-10:7 (gate replacement through memory openings), 16:6-12 (source contact). Even if one were to employ Nishikawa's gate replacement process, replacing the backside contact via with a cylindrical TAC was a "known technique" that was at least "a suitable option" for Nishikawa's backside contact. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023); Lee, ¶ 114.

To start, Nishikawa2 demonstrates the knowledge of a POSITA. Nishikawa2 states that this same backside contact structure may be circular: "The openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape." Nishikawa2, 22:38-41; *see also id.*, 22:34-38 (source line connection), 23:59-67 (insulating spacer 74), 24:24-39 (forming "backside contact via structure 76" in "backside trench 79"). As illustrated below, Nishikawa's TACs are the same structure in the same memory architecture as Nishikawa2:



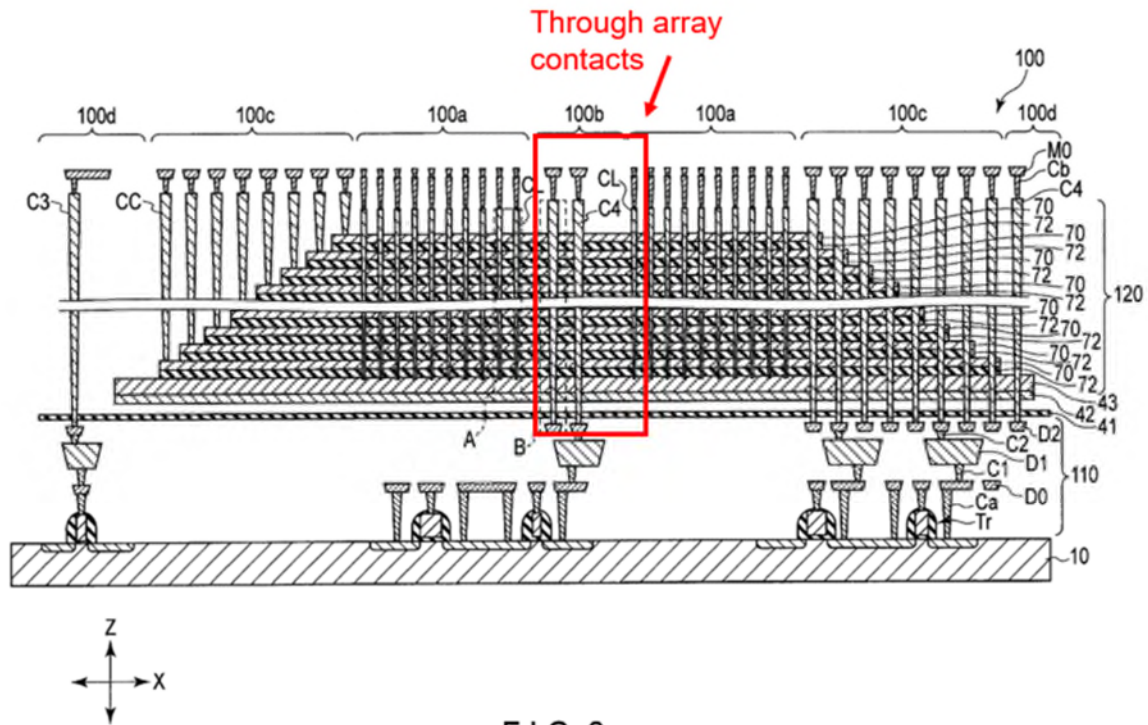
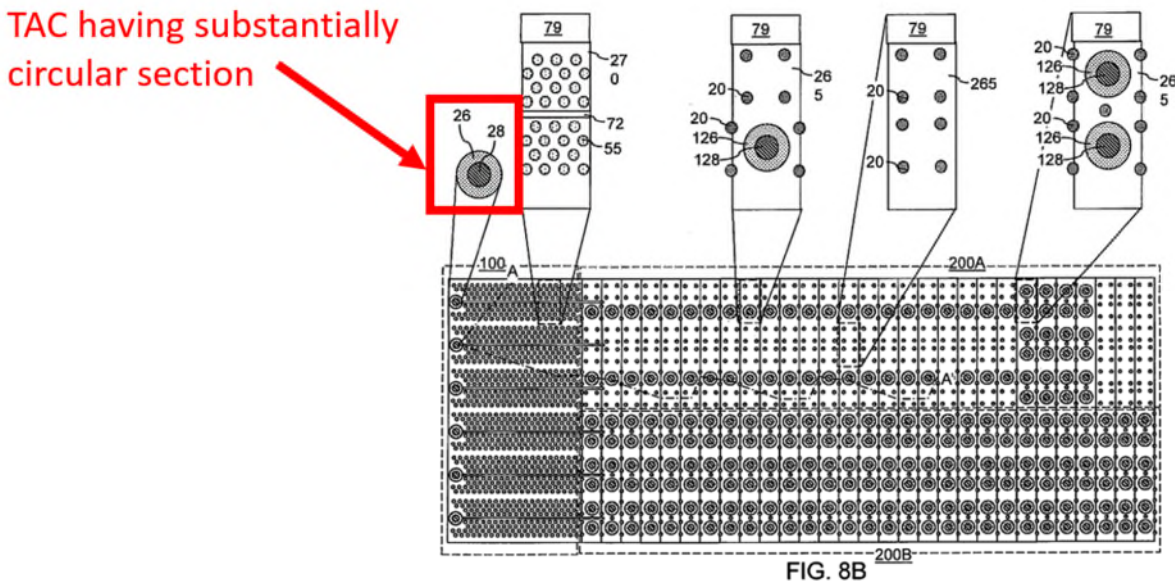


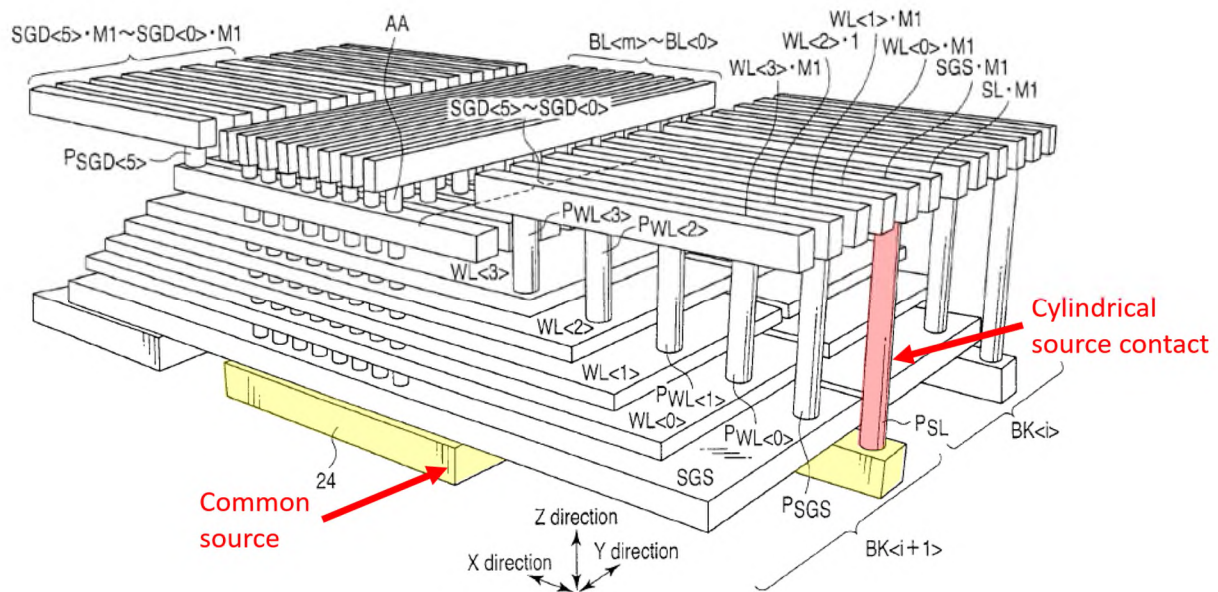
FIG. 2

Ex. [1009] (“Nakajima”), Fig. 2 (annotated), 3:64-67 (“The shape of the contacts CC, C3, and C4 . . . may be a substantially circular shape.”). Masamori likewise discloses through-array contacts (e.g., laterally-insulated conductive via structures (26, 28)) that have a cylindrical shape and extend through the stack:

FIG. 8A



Second, implementing source line contacts as cylindrical structures was well known. For example, Maejima discloses a cylindrical source contact extending from above a memory stack down to a common source below the memory stack as illustrated below:



Ex. 1021, Fig. 1 (annotated), 4:59-62 (“A source diffusion layer 24 formed in a semiconductor substrate is shared by, for example, all the blocks. The source diffusion layer 24 is connected to a source line SL·M1 through a contact plug P<sub>SL</sub>.”); *see also* §V (describing source line connections). Indeed, cylindrical source contacts were textbook material before the filing of the ’322 Patent:

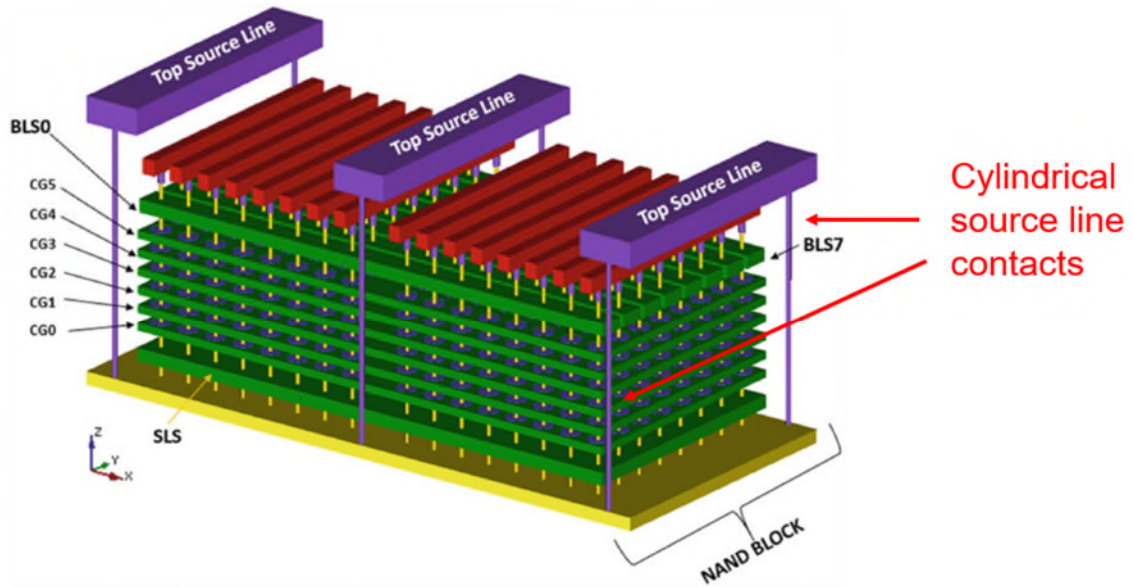


Fig. 5.17 C-FG array with top source line

Ex. 1010, 155.

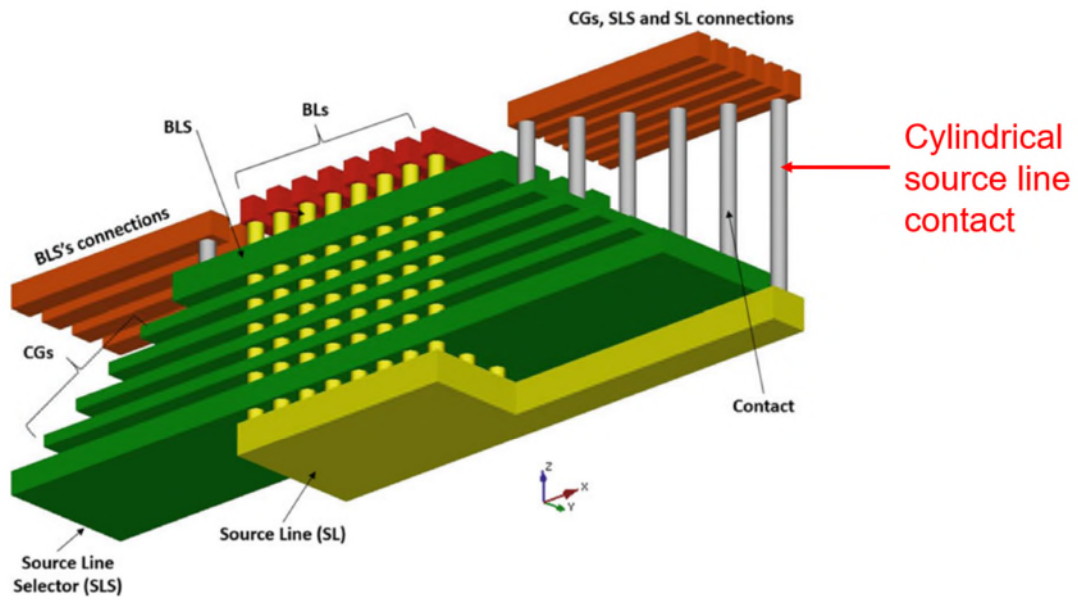
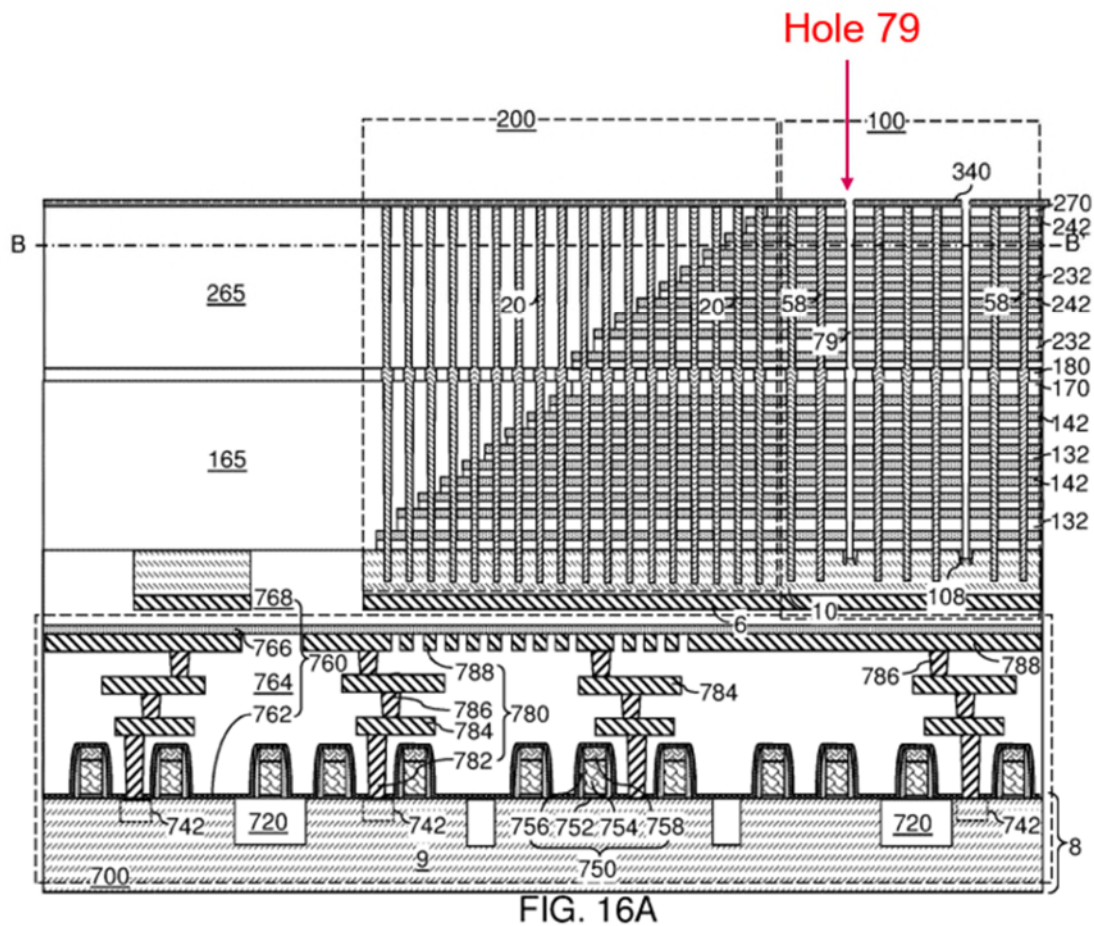
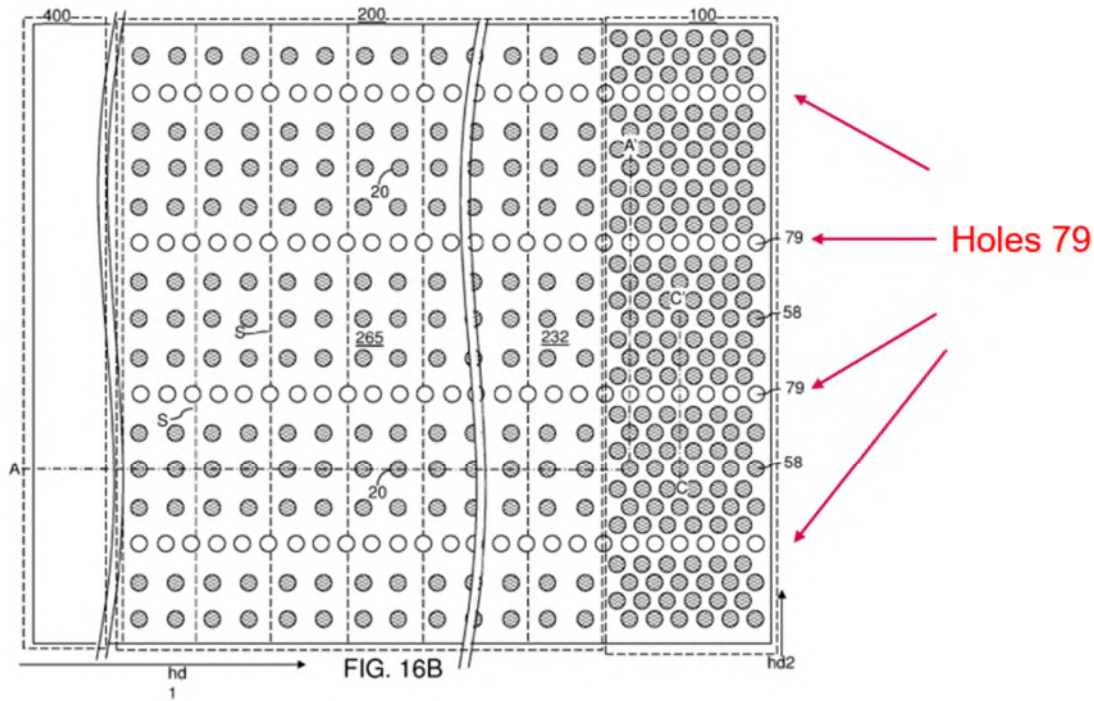


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

*Id.*, 110; Lee, ¶¶ 119-20.

Finally, even if one were to implement the gate replacement process in Nishikawa, and not implement it through the memory openings (an option in Nishikawa, *see* Nishikawa, 9:58-10:7), a POSITA understood that using circular holes for the TACs and using those holes for the gate replacement process was a suitable option (just like Nishikawa's memory holes). Iwai, for example, teaches using cylindrical voids (79) for the gate replacement process:





Ex. 1022, (U.S. Pat. 10,347,654, “Iwai”), Figs. 16A, B, 28:52-65 (extending through stack), 30:25-58 (using 79 voids for gate replacement process); *see also id.*, Fig. 25B, 33:18-21 (“Thus, each electrically conductive layer (146L, 246L) can be formed as a continuous material layer including multiple rows of holes, which are the multiple rows of backside openings 79.”), 37:47-51 (circular 79 arrangement). Iwai further discloses that the voids 79 may be converted to a trench if there is a desire to segment the array. *Id.*, 33:22-49, 34:18-33. In other words, Iwai expressly recognizes that a trench is not necessary for the gate replacement process. Lee, ¶ 121.

Accordingly, in addition to the below motivations, replacing the backside contact via with a cylindrical TAC was a “known technique” that was at least “a

suitable option” for Nishikawa’s trench and trench contact. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023); Lee, ¶ 122.

In addition, a POSITA would have been motivated, with a reasonable expectation of success, to modify the trench-shaped common source contact (74, 76) of Nishikawa to instead be a cylindrical source contact for several reasons.

First, if not employing the optional gate replacement process, there certainly is no need for the large trench (recall that source line contacts do not require a trench contact). The trench has a large footprint. Replacing the trench with smaller cylindrical source contact(s), in effect, recovers a large portion of that lost footprint, providing additional room for memory cells. In short, the modification increases the memory capacity. Indeed, Nishikawa2 discloses that eliminating the large trenches increases memory capacity. Nishikawa2, 27:55-28:3; Lee, ¶ 123. Moreover, the trench may require a long etching time due to the volume of material to etch. As a result, the smaller source line contact hole(s) save fabrication time. Lee, ¶ 124.

Second, if employing the optional gate replacement process, there is still no need for the large trench. Lee, ¶ 125. Nishikawa provides two options for the gate replacement process: either through the backside trenches or the memory hole openings. Nishikawa, 6:29-44, 9:58-10:8. Moreover, the prior art described above (*e.g.*, Iwai) demonstrates that the circular holes were known to be suitable for the gate replacement process as well. Iwai, Figs. 16A, B, 28:52-65, 30:25-58 (using 79

voids for gate replacement process). Importantly, Iwai improves on the gate replacement process by locating the voids for gate replacement throughout the array, like Nishikawa's teaching of employing the memory holes for the gate replacement process. This reduces the distance that the etchants and deposition material must flow to perform the gate replacement process. Lee, ¶ 126. A second benefit is that when implementing circular TAC as common source connections in Nishikawa, the common source connections can be spread throughout the array, providing closer contact points than Nishikawa's original source connection. Indeed, it was well known to advantageously spread source connection points throughout the array. Ex. 1010, 111 (showing 3 source connections), Ex. 1023 (Park 583) (U.S. Pat. 10,559,583), 6:8-12, Fig. 11 (showing first and second common source lines spread throughout memory array); Lee, ¶ 127.

A POSITA would have had a reasonable expectation of success in modifying Nishikawa's source contact lines to be cylindrical contacts. First, as illustrated above, cylindrical contacts, including those that extend through the memory stack, were well known. Second, as illustrated above, cylindrical contacts were known to be suitable for source connections and the holes therefor were known to be suitable for the gate replacement process. Third, processing techniques to implement these features were routine. Indeed, as the analysis under [6.C] demonstrates, Nishikawa

already discloses etching cylindrical holes and forming cylindrical contacts, e.g., the peripheral contacts. Lee, ¶ 128.

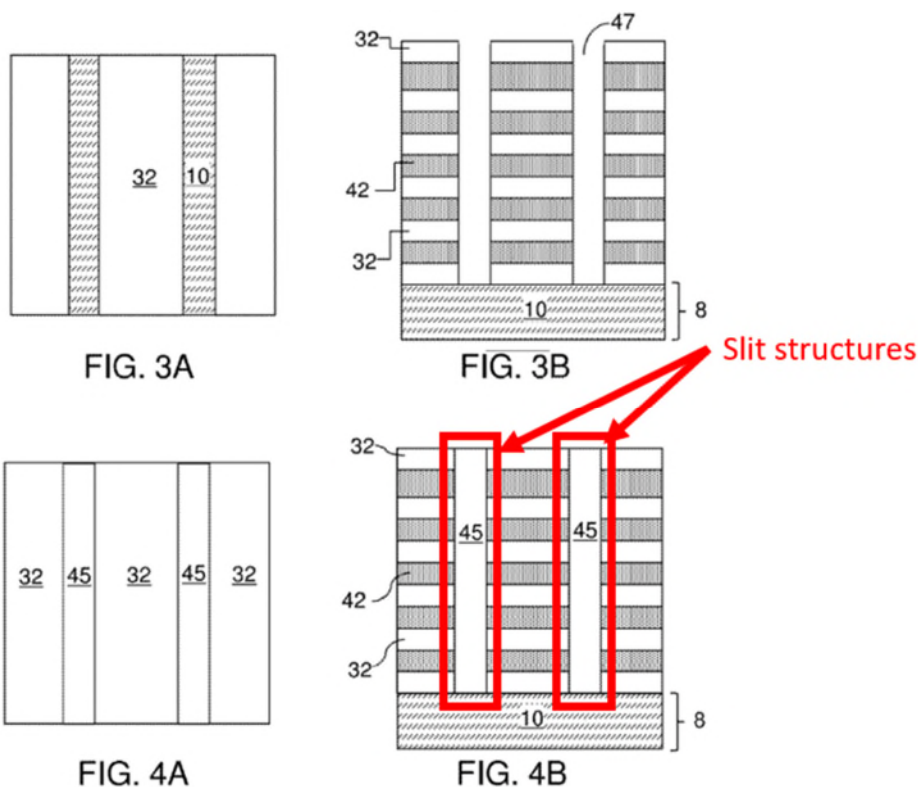
6. **[1.E] “a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones.”**

Nishikawa discloses a slit structure (“separator dielectric structure 45”) extending vertically through the conductor (“electrically conductive layers 46”)/dielectric (“insulating layers 32”) layer pairs in the memory stack (alternating stack) and configured to separate the memory stack into a plurality of memory zones (annotated on the figures below). Lee, ¶ 129.

As an initial matter, the ’322 Patent does not use the term “memory zones,” and instead states that “[s]lit structure 132 . . . can separate 3D memory device 100 into multiple memory blocks and/or memory fingers.” Ex. 1001, 8:16-18. Thus, “memory zones” would have been understood to refer to a block or group of memory cells, that is, areas of a memory array that are separated by the slits. Lee, ¶ 130.

The slit structure of Nishikawa is separator dielectric 45. The separator dielectric 45 is formed in a separator trench 47 “through the alternating stack (32, 42) to the top surface of the substrate 8 that is located at the bottom of the alternating stack (32, 42).” Nishikawa, 8:3-19. Nishikawa explains that the separator trench can be filled with a dielectric insulating material and that “the deposited separator insulating material constitutes separator dielectric structures 45.” *Id.*, 8:20-35.

Nishikawa further discloses that a “separator dielectric structure 45 can extend through the alternating stack (32, 42), i.e., from the top surface of the substrate 8 to the top surface of the alternating stack (32, 42).” Nishikawa, 8:36-43. The process of first forming the separator trench 47 (Figs. 3A-B) and then filling the separator trench with dielectric material to form the separator dielectric structures 45 (Figs. 4A-B) is shown below.



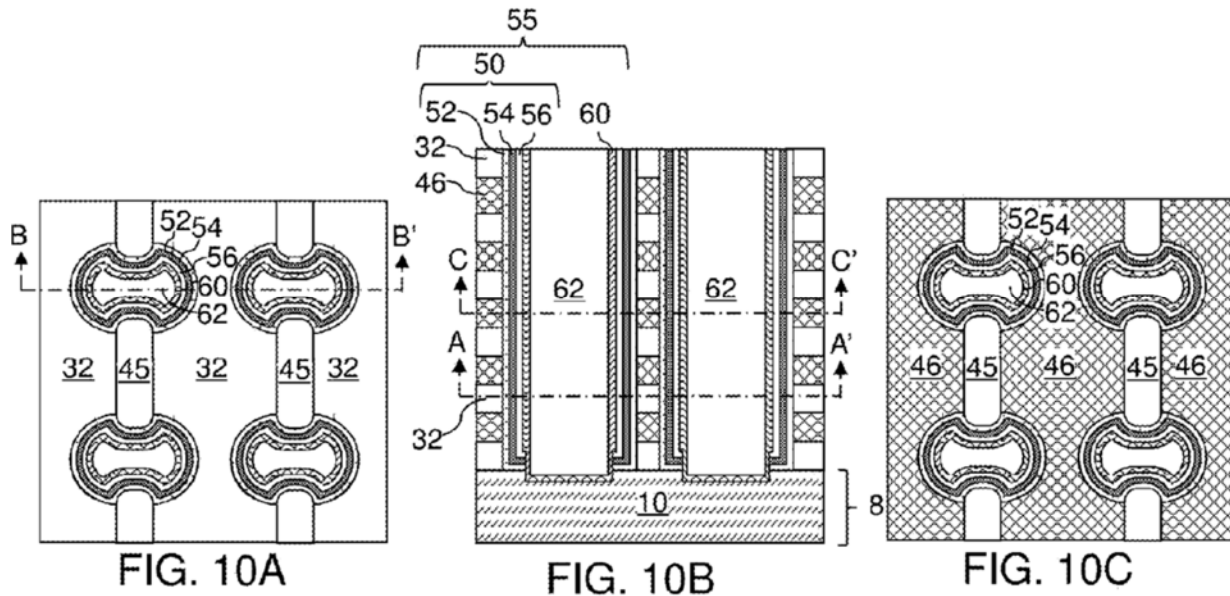
*Id.*, Figs. 3A-B, 4A-B (annotated); Lee, ¶¶ 131-32.

Nishikawa also discloses that “the alternating stack (32, 42) as formed at the processing steps of FIGS. 2A and 2B is divided into multiple laterally disjointed portions by the separator dielectric structures 45, each of which comprises discrete

portions of the alternating stack (32, 42).” Nishikawa, 8:36-43. These laterally disjoined portions are memory zones of memory cells that are formed within each region. Lee, ¶ 133.

Nishikawa discloses two types of slits. First, Nishikawa discloses that “[e]ach memory opening 49 can be located between a pair of separator dielectric structures 45.” Nishikawa, 8:57-59. In other words, the separator dielectric structures, by themselves, divide the array into groups of memory cells.

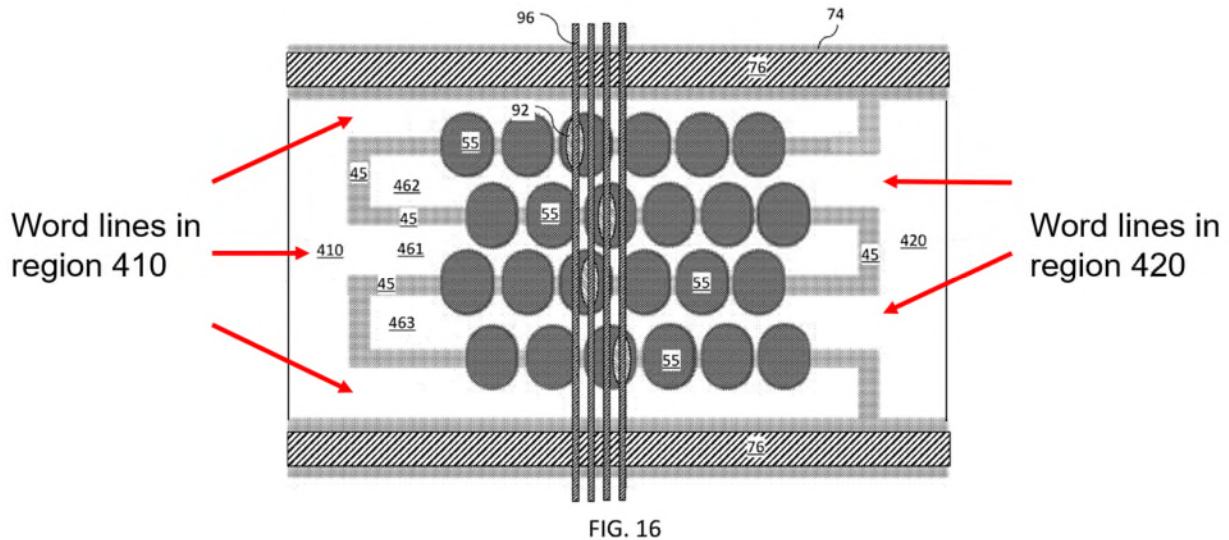
Second, Nishikawa discloses that “[i]n one embodiment, each memory opening 49 can divide a separator dielectric structure 45 into two physically disjoined portions. In this case, each memory opening 49 in the alternating stack (32, 42) can extend through the separator insulating material located in a respective separator dielectric structures 45, and can divide the separator dielectric structure 45 into two laterally disjoined portions.” Nishikawa, 8:59-67. Here, as shown below, while the memory channel structures are physically between portions of the slit structure, the slit still divides the array, because without it, there would be no separation.



*Id.*, Figs. 10A-C. Note that Nishikawa further discloses, in this embodiment, that independent memory cells are located on either side of the separator dielectric structure 45. For example, Nishikawa discloses “[e]ach memory cell in the NAND string comprises a portion of a first control gate electrode 461 (which is a first portion of an electrically conductive layer 46) located adjacent to a first portion 50A (**which is located on one side of a respective pair of separator dielectric structures 45**) of a memory film (52, 54, 56) and a portion of a second control gate electrode 462 which is located adjacent to a second portion 50B (**which is located on the other side of the respective pair of separator dielectric structures 45**) of the memory film (52, 54, 56).” *Id.*, 14:60-15:2. Nishikawa further explains that “[t]he second control gate electrode 462 is electrically insulated from the first control gate electrode 461.” *Id.*, 15:2-3. Even in this embodiment, the separator dielectric structures 45 divide

the memory stack into a plurality of memory cell groups (memory zones) because independent memory cells are formed on both sides of the separator dielectrics 45.

For example, in the embodiment below, the separator dielectrics 45 split the memory stacks into two regions (410 and 420):



*Id.*, 15:31-42 (“Each level of control gate electrodes can include a first word line and a second word line.”); Lee, ¶¶ 134-36.

**B. Claim 2:**

1. [2] “The 3D memory device of claim 1, further comprising: a peripheral device on the substrate, a peripheral contact being arranged outside of the memory stack and in contact with the peripheral device.”

Nishikawa discloses this limitation.

Nishikawa discloses a peripheral device (“peripheral device 20”) on the substrate (“substrate 8”), a peripheral contact (“peripheral contact via structures 86”)



**C. Claim 3:**

**1. [3.PRE] “The 3D memory device of claim 2, further comprising:”**

Nishikawa discloses or at least renders obvious the 3D memory device of claim 2. See [1]-[2], above.

**2. [3.A] “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,”**

As discussed in [1.C], Nishikawa discloses channel structures, i.e. memory stack structures 55. Nishikawa, 11:33-39. The channels include dielectric layers. See §X.A.4. As explained below, in view of the knowledge of a POSITA, a POSITA would have been motivated, with a reasonable expectation of success, to include dummy channels (of either the same materials or with a solid dielectric fill) in Nishikawa’s memory stack. As discussed in [1.D], Nishikawa discloses an optional gate replacement process. The motivations differ slightly depending on whether the gate replacement process is used or not.

To start, regardless of whether the gate replacement process is used, it was well known to include dummy channel structures in memory stacks for processing reasons. First, adding dummy channel structures was known to reduce the likelihood of defective bits on the edge of the memory cell region, because the additional rows of dummy channel structures extend the memory cell pattern to include the dummy region on the edges. Lee, ¶ 141. It was well known that when a pattern stops (instead

of extending into the dummy region), defects occur on the edge. *Id.* (citing Ex. 1024 (U.S. Pat. 5,945,717), 8:47-53 and Ex. 1025 (U.S. Pat. 10,347,487), 2:20-43 to explain the edge effect). Second, adding dummy structures would result in an overall more uniform feature pattern, which reduces processing issues. *Id.*, ¶ 142 (citing Ex. 1026 (Ronse), 11 to explain this processing issue). Thus, expanding the channel structure region (that is, in the cell region of the memory stack) to include dummy channels structures on all edges (that extend through the memory stack), thereby resulting in the dummy channel structures surrounding the active region, was a well-known technique to improve yield. *Id.*

Next, if employing the gate replacement process, it was well known to include dummy channel structures to provide structural support. Nishikawa<sup>2</sup> recognizes the need for support structures. Nishikawa<sup>2</sup>, 9:63-67. Lee, ¶ 143. By way of another example, Masamori discloses that as three-dimensional devices scale to smaller sizes, additional structural support is desired during the sacrificial gate replacement process. *See* Masamori, [0003]. Masamori discloses a dummy channel structure (“semiconductor-containing support structure 20”) that extend vertically through the conductor/dielectric layer pairs (second insulating layers 232, second conductive material layers 246 and first insulating layers 132, first conductive material layers 146) in the memory stack (annotated in Fig. 7A below). Although the layers of the semiconductor-containing support structure 20 are described in the context of the

memory opening fill structures 55, Masamori discloses that “the memory opening fill structures 55 and the semiconductor-containing support structures 20 can be formed simultaneously employing a same set of processing steps.” *Id.*, [0085]. Thus, a POSITA would have understood that the semiconductor-containing support structures 20 have the same layers as memory opening fill structures 55, as shown in Fig. 7A (including the dielectric layers, e.g., tunneling and blocking layers).

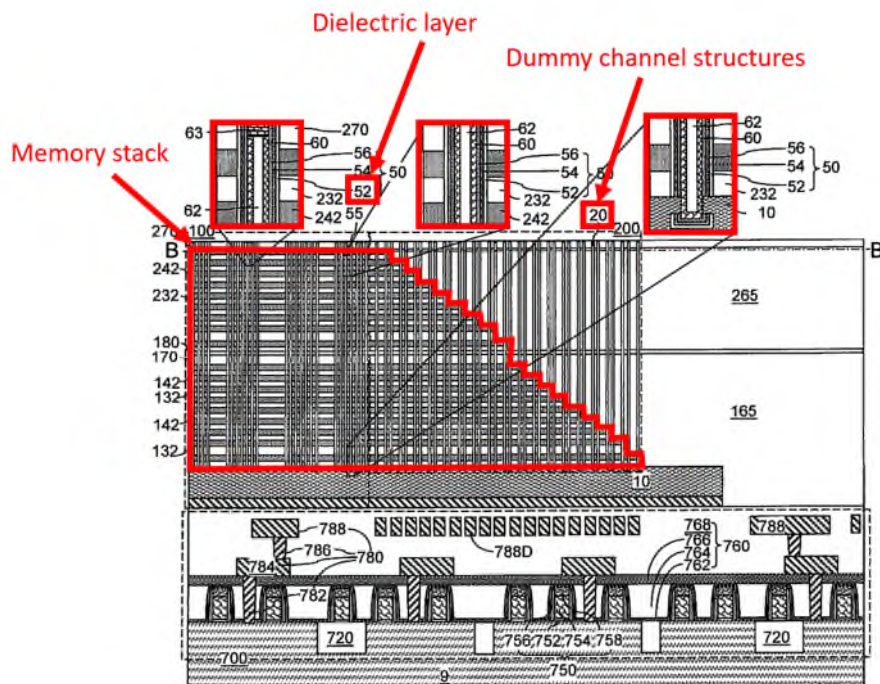


FIG. 7A

Masamori, Fig. 7A (annotated). Masamori discloses that “[t]he blocking dielectric layer 52 includes a blocking dielectric layer material such as silicon oxide, a dielectric metal oxide (such as aluminum oxide), or a combination thereof.” Masamori, [0086]. Silicon oxide layers are dielectric layers. Lee, ¶ 146. As illustrated, the semiconductor-containing support structures 20 extend through the

second insulating layers 232, second conductive material layers 246 and first insulating layers 132, first conductive material layers 146.

Kai further confirms the knowledge of a POSITA regarding dummy channel structures. Kai, for example, discloses forming active and dummy channels, which provide structural support. Ex. 1027 (U.S. Pat. 10,290,643, Kai), 9:23-26 (defining “support opening” as “a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed”), 9:45-48 (“support openings 19” extend through stack), 10:20-27 (forming channels in support openings). Kai refers to the dummy channels as “support pillar 20” and active channels as “memory stack structures.” *Id.*, 16:28-48, Figs. 6A, 15A, 25:58-63. Park 297, likewise, discloses active and dummy supporting channels. Ex. 1028 (U.S. Pat. 9,859,297, Park 297), 6:19-26, 7:45-51. Kim 559, too, forms active channels and dummy channels through the stack at the same time. Ex. 1029 (U.S. Pat. Pub. 2018/0308559, Kim 559) [0047] (“DS [Dummy Structure] may physically support,” and listing same materials as channels), [0071] (“The channel holes CH and the dummy holes DH may be formed at the same time.”), [0072] (same time), Fig. 13 (DH through stack on edge). It was known that to perform this gate replacement process, “support pillars” were necessary. Ex. 1030 (U.S. Pat. 8,945,996), 5:64-6:2, 7:19-23; Lee, ¶¶ 143-45.

Thus, additional motivation to use dummy channels when employing the gate replacement process includes, first, providing additional support during the gate replacement process. *E.g.*, Ex. 1027 (Kai), Fig. 6A (support members 20), 16:28-38. It was well known that adding additional dummy channels “provide[s] additional structural support during replacement of the [sacrificial gate layers].” Ex. 1031 (U.S. Pat. 10,115,632), 30:14-27; *see also id.*, 15:3-22 (structures 20 are dummy channel structures). Second, dummy channels can be made by the same process and at the same time as the active channels. Ex. 1027 (Kai), 10:20-27; Lee, ¶ 144. Third, dummy channels do not require connections to the upper-level devices, thereby not consuming space above the structures while also serving as support structures. Ex. 1028 (Park 297), 8:55-65; Lee, ¶ 147.

Adding dummy channel structures would have been routine and a POSITA would have had a high expectation of success. First, as discussed above, Nishikawa already discloses forming channel structures, and the same materials are used for dummy channels (including the dielectric layers). Second, for the reasons above, the additional dummy channel structures would actually reduce processing issues. Lee, ¶ 148. Third, as demonstrated above, dummy channels were commonplace. *Id.*

If PO argues that the claimed dummy channel structures must be fully filled with a dielectric material, PO would be incorrect.

To start, the '322 Patent discloses that “[d]ummy channel structure 146 can extend vertically through memory stack 104 and have a vertical opening filled with the same materials as those in channel structure 108.” Ex. 1001, 9:29-31. Then later, the '322 Patent discloses that “[i]n some embodiments, dummy channel structure 146 is **fully filled** with dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.” *Id.*, 9:35-39. If Applicant had intended the language “a dummy channel structure filled with a dielectric layer” to mean fully filled with a dielectric material, the claim would recite “fully filled.” For example, in claim 10 of related U.S. Patent No. 10,879,254, the Applicant did just that: “depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure.” Ex. 1032; Lee, ¶ 149.

Regardless, as the claim [3.A] analysis demonstrates, it would have been obvious in view of the knowledge of a POSITA to fully fill the dummy channel structures with dielectric material. One known beneficial use of dummy structures was as a support pillar. A common support pillar was a solid dielectric, e.g., silicon oxide, pillar. Ex. 1033 (U.S. Pat. 9,793,139), 15:21-39 (“dielectric support pillar 7P”). The known benefit of complete fill is that it provides more support relative to partial fill. *Id.*; Lee, ¶ 150.

**3. [3.B] “wherein each of the dielectric layer in the dummy channel structure, a spacer in the TAC, and a spacer in the peripheral contact comprises silicon oxide.”**

Nishikawa discloses, or in view of the knowledge of a POSITA renders obvious, this limitation.

As to the dummy channels, the analysis under claim [3.A] and [1.C] demonstrates that it would have been obvious to employ dummy channels with silicon oxide layers (partial or complete fill). *See also* Nishikawa, 12:11-27 (silicon oxide layers of channel structure, which [3.A] demonstrates would hence be present in the dummy channels).

As to the TAC spacer (spacer for backside contact 76), Nishikawa discloses a “dielectric spacer 74.” Nishikawa, 6:57-59. Likewise, as to the peripheral contact spacer (spacer for contact via structure 68), Nishikawa discloses a “dielectric liner 64.” *Id.*, 6:49-50, Fig. 1. Elsewhere, Nishikawa describes “dielectric material of insulating layers 32” as being “silicon oxide.” *Id.*, 6:2-8. Such dielectric spacers were typically silicon oxide. For example, Masamori discloses that the spacer of the laterally-insulated conductive via structure (26, 28), i.e. a TAC, can be silicon oxide. Masamori, [0099]; *see also* Ex. 1012 (Mushiga) 10:31-57 (disclosing a tubular spacer material 586 surrounding a through-memory-level-via structure 588). Thus, a POSITA would have understood, and at least found obvious, that Nishikawa discloses silicon oxide spacers for the TACs and peripheral contacts. Lee, ¶ 153.

At a minimum, a POSITA would have been motivated, with a reasonable expectation of success, to employ silicon oxide as the spacers and the dummy channel material layer for several reasons. First, Nishikawa already discloses using silicon oxide as a dielectric material to form other dielectric spacers such as the blocking dielectric layer 52. Nishikawa, 6:2-8. Second, silicon oxide was the typical dielectric material for spacers and channel structures, because of its relative ease of use in semiconductor fabrication. Ex. 1034 (Wolf Vol. 1), 48-49; Lee, ¶ 155. Third, silicon oxide was known to be an ideal insulator. Lee, ¶ 155. Finally, a POSITA would have had a reasonable expectation of success. Again, Nishikawa already employs silicon oxide in its process. And the deposition of silicon oxide to form spacers was routine, e.g., including the conformal deposition of silicon oxide spacers. Ex. 1034, 48-49; Nakajima, 7:44-49; Lee, ¶ 154.

**D. Claim 6:**

**1. [6.PRE] “The 3D memory device of claim 1, further comprising:”**

Nishikawa discloses or at least renders obvious the 3D memory device of claim 1. See [1.PRE]-[E], above.

**2. [6.A] “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; and”**

This limitation is identical to claim [3.A] and met for the same reasons.

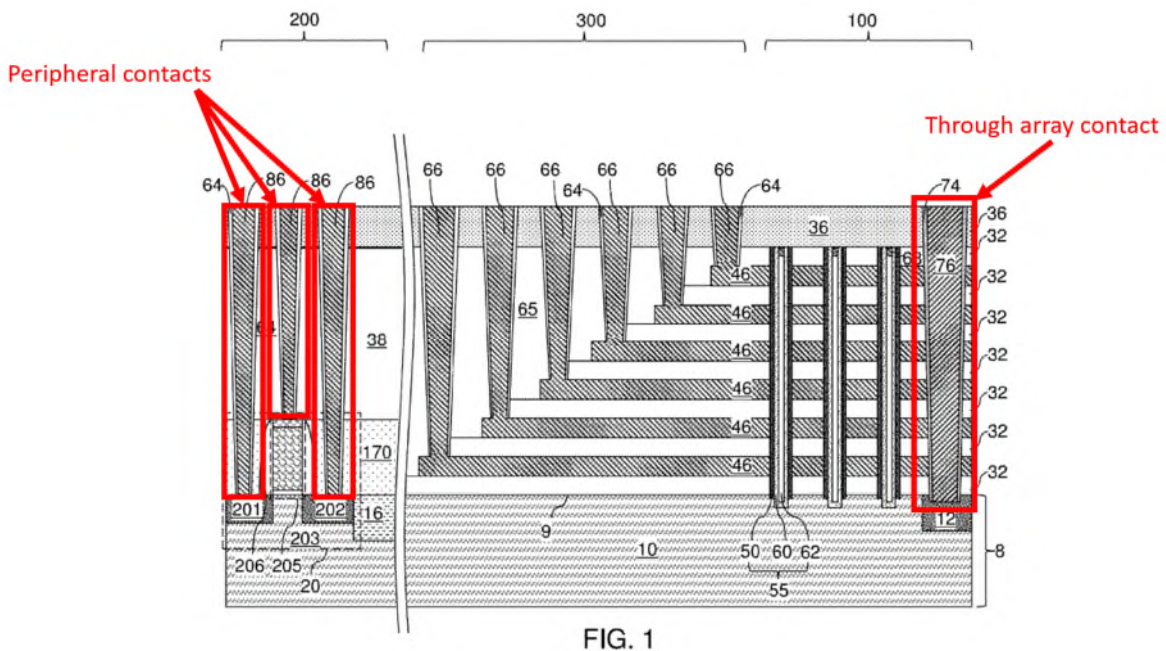
3. [6.B] “a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate,”

This limitation is substantively the same as claim [2] and met for the same reasons.

4. [6.C] “wherein: a diameter of the TAC is at least equal to a diameter of the peripheral contact; and”

Nishikawa in view the knowledge of a POSITA renders this limitation obvious.

As an initial matter, the analysis under claim [1.D] demonstrates that it would have been obvious to implement Nishikawa’s TAC as a cylindrical contact with a diameter. Nishikawa’s TACs and peripheral contacts are shown below:



Nishikawa, Fig. 1 (annotated). It would have been understood that Nishikawa’s peripheral contacts 86 are cylindrical with a diameter because these contacts extend

through the array and connect to devices, e.g., as shown above. Lee, ¶ 159. Moreover, such TACs were known to be cylindrical, as the analysis under claim [1.D] demonstrates.

One common textbook approach was to make contacts the same size. Ex. 1035 (Wolf Vol. 2), 33. Using the same contact size was known and standard specifically in the 3D memory space as well. For example, Mushiga discloses forming, at the same time, through-array contacts (588) having the same size and using the same processing steps:

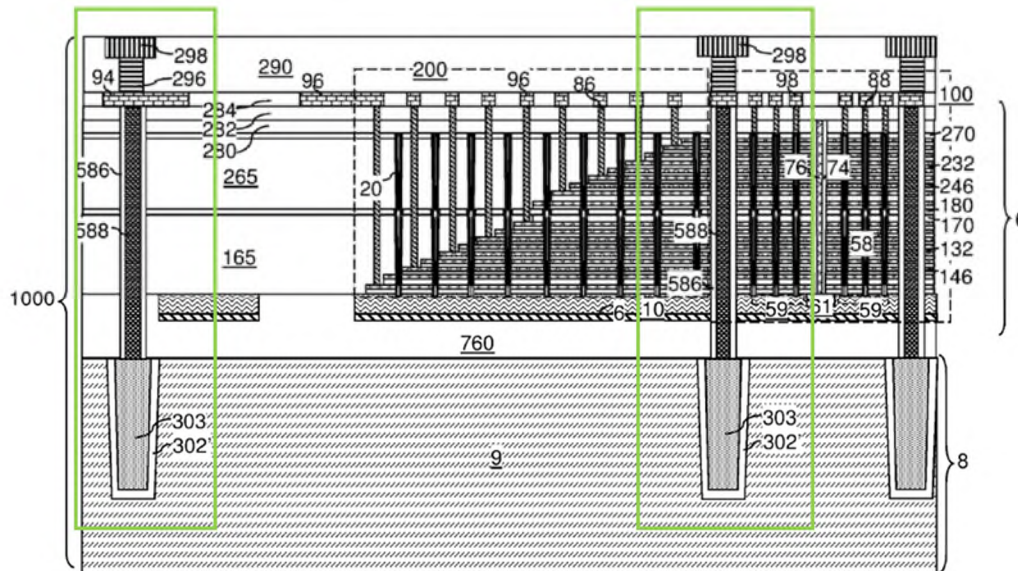


FIG. 5

Ex. 1012 (Mushiga), Fig. 5, 10:31-58; Lee, ¶¶ 160-61. As another example Nakajima discloses forming holes H1 through the stack for its TAVs (C4). One C4 structure is outside of the stack (on the right below):

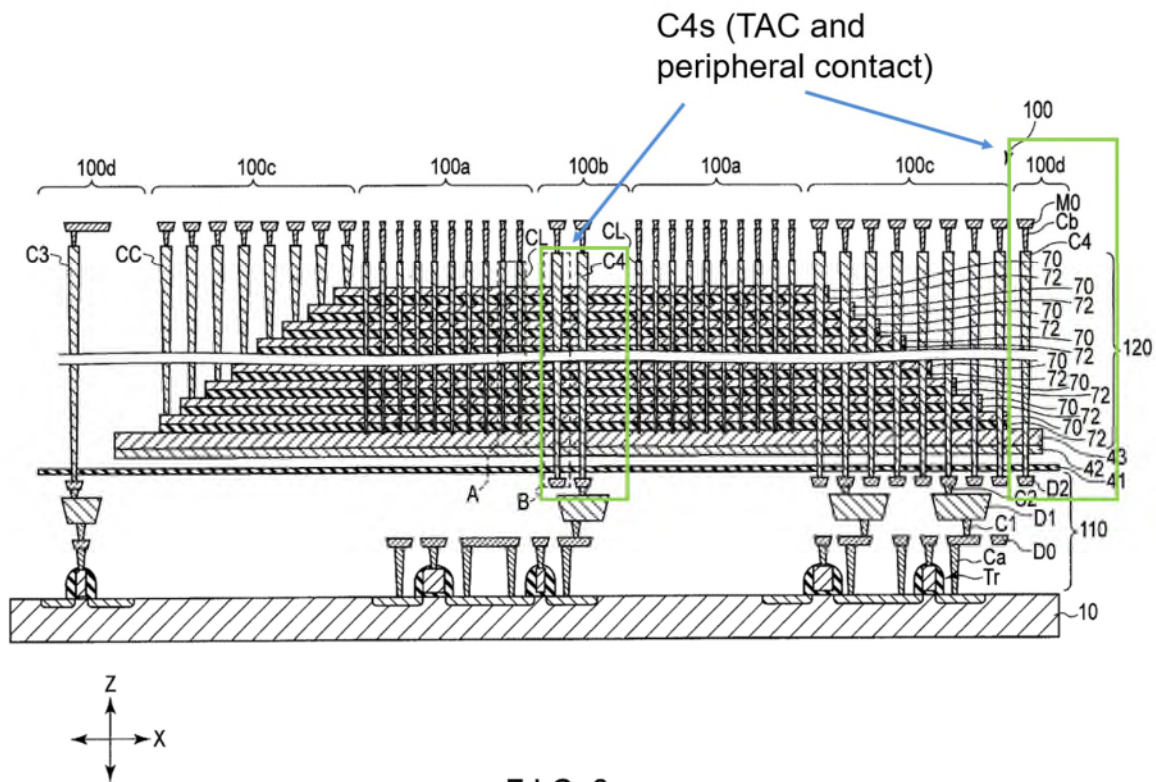


FIG. 2

Nakajima, Fig. 2. Nakajima only discloses one step for creating the H1 holes. *Id.*, 7:37-43. And Nakajima only discloses one set of steps for forming the C4 contacts. *Id.*, 7:5-8:11.

A POSITA would have been motivated to make the TAC and peripheral contacts the same size to employ a common process (including the hole size in masking steps) when forming the contacts. As can be seen above, this is precisely what Mushiga and Nakajima do for contacts in, and outside, the array. It saves considerable process time to use a common set of process steps to form multiple elements. Lee Decl., ¶ 162. That is why it was known to form openings for different structures at the same. *E.g.*, Ex. 1036 (U.S. Pat. Pub. 2019/0081061, Tessariol),

[0037] (“dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)”), Fig. 9. But if the holes sizes are different, then modifications to the etch chemistries are necessary. *E.g.*, Ex. 1035 (Wolf Vol. 2), 33; Lee, ¶ 162. Because of this well-known benefit, process technologies, e.g., etch chemistries, that achieve simultaneous etching of different holes had become textbook material before the ’322 Patent was filed. *Id.*

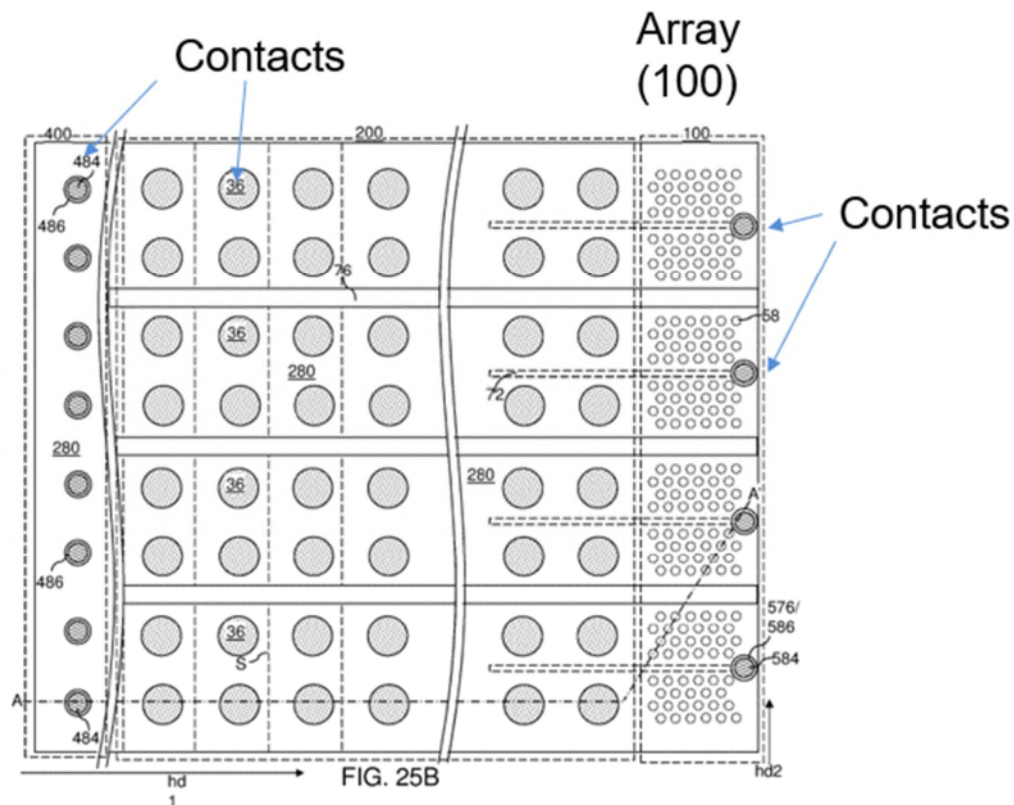
**5. [6.D] “a diameter of the dummy channel structure is smaller than each of a diameter of the TAC and a diameter of the peripheral contact.”**

Nishikawa in view of the knowledge of a POSITA renders this limitation obvious.

The analysis under claim [3.A] demonstrates that it would have been obvious to form dummy channel structures using the same process to form active channels. As explained below, the dummy channels have a much smaller diameter than the TACs and peripheral contacts and it would at least have been obvious to implement this arrangement.

Memory stacks contain millions or billions of channel structures, and these channel structures are smaller than contacts because the entire point of a memory is to have a very dense memory region. Lee, ¶ 165. Indeed, the fabrication process typically uses special processing to form a dense memory array region (e.g., as Ground 2 demonstrates, the desire for smaller channels led to multi-deck stacks).

Thus, it was textbook material to make the channel holes as small as possible, typically using memory-hole specific processing steps. Ex. 1010, 211-215. Dummy channel holes will generally have the same size as channel holes to maintain a uniform pattern and reduce the edge effect issues (that is, repeating the uniform pattern). Lee, ¶ 165. Recall the memory and dummy memory holes are made using the same process as well. See §X.C.2. For example, below is a top-down view showing channel structures in region 100 versus various contacts in regions 200 and 400:



Ex. 1037 (Cui), Fig. 25B. A POSITA would have understood the above figure to illustrate that features in the dense array are relatively smaller than features in the

This cross-sectional view shows a device with a central vertical structure 96. The structure 96 is composed of multiple parallel vertical elements. The device is bounded by a top layer 74 and a bottom layer 76, both with diagonal hatching. A grid of circular elements 55 is arranged in a 4x4 pattern. The elements 55 are connected to a network of horizontal and vertical lines 45. Specific labels include 410, 461, 462, 463, and 420, which likely represent different layers or components of the device. A red arrow points to one of the circular elements 55, with the word "Diameter" written next to it, indicating the measurement of the element's width.

Nishikawa, Fig. 16. The '322 Patent does not define “diameter” contrary to its plain and ordinary meaning, and an “ellipse” has both major and minor “diameter.” Ex. 1047; Lee, ¶ 167.

Regardless, Nishikawa discloses that the memory cells may be between separators 45. See §X.A.6. The conventional memory cell in this arrangement was circular. *E.g.*, Ex. 1037 (Cui), Fig. 25B (illustrate circular “memory opening fill structure 58”); Masamori, Fig. 8B (illustrating circular “memory stack structures 55”). Thus, a circular memory cell was not only a “known technique” that was “a suitable option” for Nishikawa’s memory, but the most conventional option. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023); Lee, ¶ 168.

**E. Claim 7:**

- 1. [7] “The 3D memory device of claim 1, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.”**

Nakajima renders this limitation obvious under PO’s incorrect interpretation and under the correct interpretation.

As an initial matter, the ’322 Patent makes clear that these limitations relate to an intentional etch that forms actual recesses in the sacrificial layers resulting in larger lateral dimensions of the TAC corresponding to conductive layers and smaller lateral dimensions of the TAC corresponding in dielectric layers. Ex. 1001, 13:52-65, Fig. 3D. For infringement, however, PO interprets this claim to cover largely undetectable and unintentional alleged recesses. Ex. 1038 (Ex. B-1, YMTC’s Contentions), 11, 28. As is well known, a typical etch through a stack of silicon

oxide and silicon nitride layers does not have the exact same selectivity towards each of silicon oxide and silicon nitride, and will result in uneven sidewalls, such that there are recesses in either the oxide layers or the sacrificial layers. Ex. 1039, (U.S. Pat. 11,075,084), 2:59-67 (In “3D NAND memory, it is important to have an etching gas which can etch both SiO<sub>2</sub> and SiN layers (or both SiO<sub>2</sub> and p-Si layers) without selectivity. In another words, ***it is a challenge to find an etch gas that has similar high etch rates of SiO<sub>2</sub> and SiN in terms of getting a smooth sidewall*** of high aspect ratio holes in 3D NAND memory.”); Lee, ¶ 170. Thus, under PO’s apparent interpretation, these various prior art etches that would form the holes for the backside contact via structure (74, 76) would also create these unintentional “shallow recesses,” which may be in the sacrificial silicon nitride, or dielectric, layers depending on the etch type. Ex. 1039, (U.S. Pat. 11,075,084), 2:59-67; Lee, ¶ 170.

### **PO’s Incorrect Claim Interpretation**

The alternating stack of Nishikawa includes “[e]lectrically insulating materials that can be employed for the insulating layers 32 includ[ing], but are not limited to . . . silicon oxide . . . [and] sacrificial material layers 42 compris[ing] sacrificial layers, such as silicon nitride . . . .” Nishikawa, 7:3-11. As discussed above, typical prior art etches that were both well-known and beneficial in that they create holes through the stack, e.g., for contacts, were also known to result in lateral

recesses in either the dielectric spacers or sacrificial layers. Ex. 1039, (U.S. Pat. 11,075,084), 2:59-67; Lee, ¶ 171. Thus, Nishikawa renders this limitation obvious under PO's incorrect claim interpretation because such unintentional recesses would naturally result, causing the claimed differences in width.

### **The Correct Claim Interpretation**

Nishikawa renders this limitation obvious in view of the knowledge of a POSITA. It was well known that an option for a TAC or other through-memory structures was to have a ribbed shape, that is, forming recesses in one of the stack layers. For example, Cui discloses contacts 183 that travel through the staircase and through the entire array. Ex. 1037 (Cui), Fig. 14A, 25:51-53 (e.g., 183 contact on right of region 200); *see also* Ex. 1027 (Kai), 11:9-34 (“laterally recessed”). Cui depicts an embodiment in which the sidewalls of this contact are straight (“cylindrical via cavity”). Ex. 1037 (Cui), Figs. 14B, 15A, 25:63-26:22. And it depicts alternative embodiments that intentionally creates large recesses in the insulating layers (“ribbed via cavity”) or sacrificial gates. *Id.*, Figs. 16A, 41A, 26:23-32, 44:65-45:25.

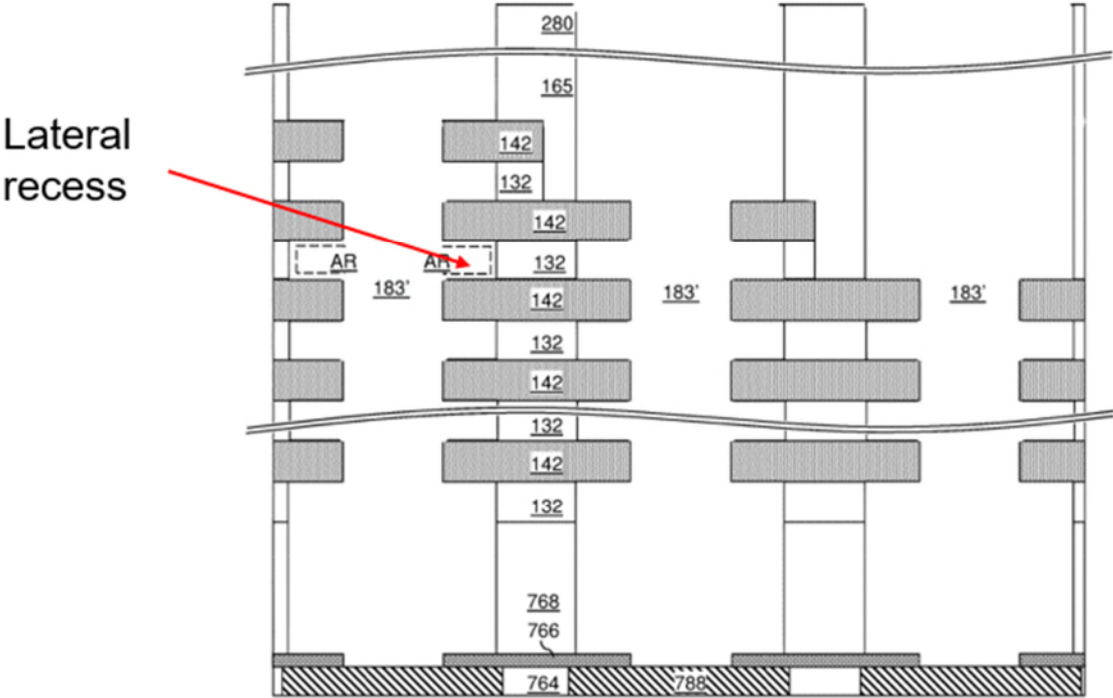


FIG. 16A

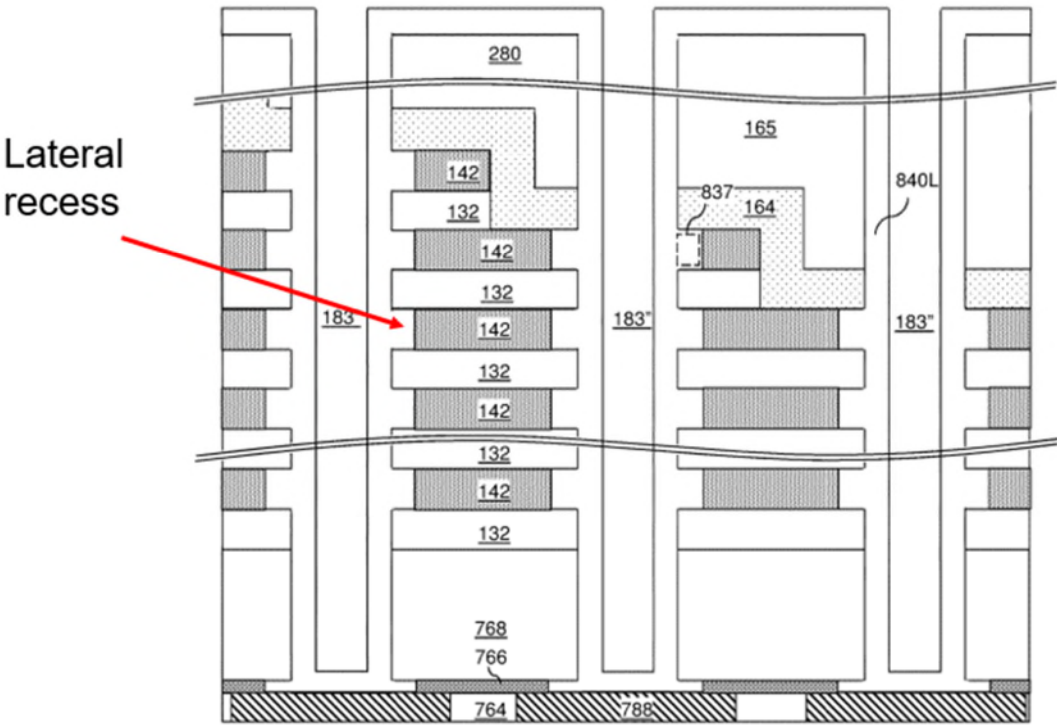


FIG. 41A

*Id.*, Figs. 16A, 41A; Lee, ¶ 172.

The ribbed via cavity serves the same purpose as the '322 Patent, namely, providing additional area for the dielectric liner. Ex. 1001, 13:38-51. In other words, there is additional space for the insulating spacer that surrounds the through-via. Ex. 1037 (Cui), 27:54-28:8. Accordingly, in view of the knowledge of a POSITA, it would have been obvious, and a POSITA would have been motivated, to create a ribbed via cavity in Nishikawa's through-array via holes. First, it was known to create lateral recesses to form "rib regions." *Id.*, 26:23-32. This advantageously creates additional area for the insulating spacer. Lee, ¶ 173. Second, there are only two options for creating such rib regions: in the sacrificial (or conductive) gates or in the dielectric layers. Both were known and result in a common benefit (see above). Lee, ¶ 174. A POSITA would have had a high expectation of success in forming the rib regions because the isotropic and selective etches were well known, as well as oxidation processes. *E.g.*, Ex. 1037 (Cui), 26:33-45, 44:65-45:25; Ex. 1027 (Kai), 11:9-34; Lee Decl., ¶ 175. Indeed, the '322 Patent provides virtually no explanation on creating these known rib regions. Ex. 1001, 17:51-61.

**F. Claim 8:**

**1. [8] "A three-dimensional (3D) memory device, comprising:"**

This limitation is identical to [1.PRE] and met for the same reasons.

**2. [8.A] "a substrate;"**

This limitation is identical to [1.A] and met for the same reasons.

3. **[8.B] “a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;”**

This limitation is identical to [1.B] and met for the same reasons.

4. **[8.C] “a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack; and”**

This limitation is identical to [1.C] and met for the same reasons.

5. **[8.D] “a through array contact (TAC) comprising a substantially circular section and extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate.”**

The analysis under identical to [1.D] demonstrates that Nishikawa in view of the knowledge of a POSITA render this limitation obvious. Specifically, as that analysis demonstrates, it would have been obvious to implement Nishikawa’s TAC 76 as a circular TAC (including its spacer and conductive fill therein that fills and contacts the spacer). Specifically, Nishikawa discloses dielectric spacer 74 for the backside contract trench 76. Nishikawa, 6:54-63. As the spacer must insulate the conductive core of Nishikawa’s TAC 76, the spacer extends fully through the stack, down to the substrate. Lee, ¶ 180. Further, the TAC would have been understood to contact the conductive layer, as the deposition process deposits the spacer (which will contact the hole side walls) and then deposits conductive core (which thus will contact the spacer).

**G. Claim 9:**

1. **[9.PRE] “The 3D memory device of claim 8, further comprising:”**

Nishikawa renders obvious the 3D memory device of claim 8. See [8.A]-[D], above.

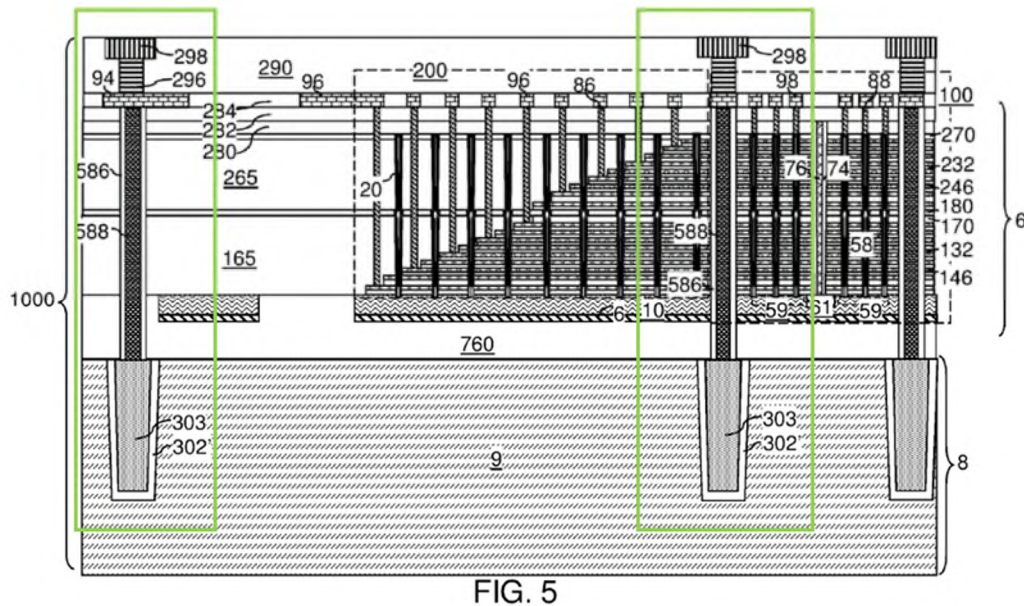
2. **[9.A] “a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate;”**

This limitation is identical to [2] and met for the same reasons.

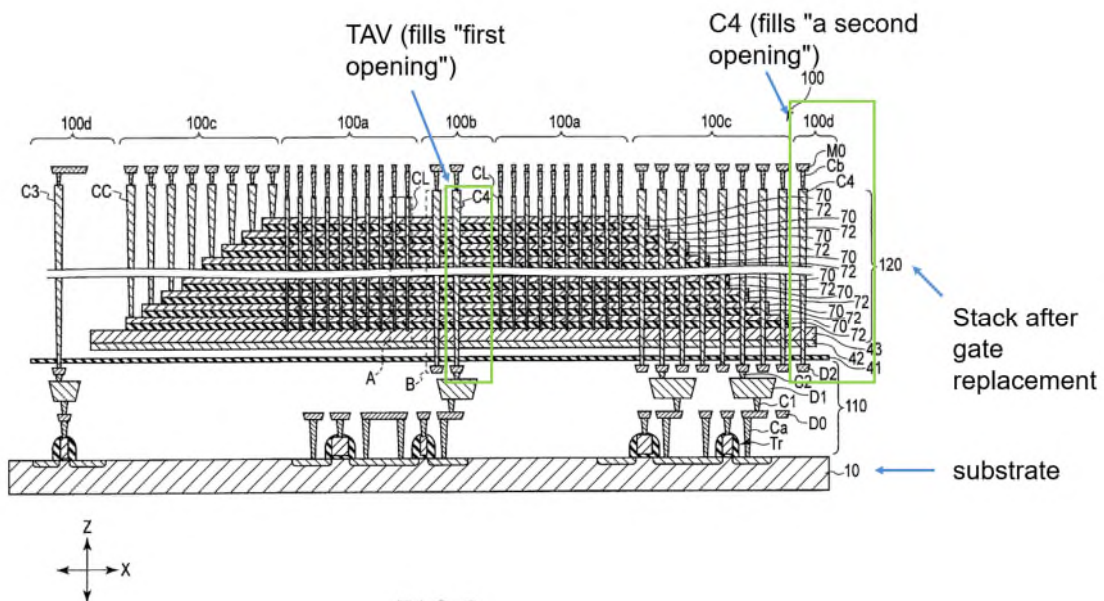
3. **[9.B] “wherein a thickness of the spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact.”**

The analysis under claim [6.C] demonstrates that it would have been obvious to simultaneously form the TACs and peripheral contacts and to form them with the same diameter (and save considerable process time). From this, it would have been obvious for the spacers to have a nominally identical thickness, because the holes will be the same size and thus the spacer deposition will form spacers of nominally identical thicknesses. Lee, ¶ 183. Again, forming the contacts at the same time, including the spacer deposition step, saves processing time. Also note that in Nishikawa, the holes would be the same height, and thus the spacer deposition will fill the same hole dimensions. Nishikawa, Fig. 1.

Mushiga conceptually illustrates that this simultaneous formation of spacers in forming through-array contacts (588) results in the same spacer thickness:



Ex. 1012, 10:31-58. This can also be seen in Nakajima, as Nakajima discloses forming one type of contact (C4) in various parts of the array, and only discloses a single spacer type:



Nakajima, Fig. 2; Lee, ¶¶ 184-85.

**H. Claim 10:**

1. **[10] “The 3D memory device of claim 9, wherein the spacer of the TAC and the spacer of the peripheral contact comprise a same material.”**

Nishikawa discloses, or at least renders obvious in view of the knowledge of a POSITA, this limitation.

Nishikawa discloses that its backside contact via structure 76 and peripheral contacts include dielectric spacers. Nishikawa, 6:40-59. To the extent that Patent Owner argues that the a “dielectric material” is too broad of a genus to constitute a “same material,” the claim [3.B] analysis demonstrates that it would have been obvious that each spacer is silicon oxide. Lee, ¶ 187.

**I. Claim 13:**

1. **[13] “The 3D memory device of claim 8, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.”**

This limitation is identical to claim [7] and met for the same reasons.

**J. Claim 14:**

1. **[14.PRE] “A three-dimensional (3D) memory device, comprising:”**

This limitation is identical to [1.PRE] and is met for the same reasons.

2. **[14.A] “a substrate;”**

This limitation is identical to [1.A] and is met for the same reasons.

3. **[14.B] “a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;”**

This limitation is identical to [1.B] and is met for the same reasons.

4. **[14.C] “a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;”**

This limitation is identical to [1.C] and is met for the same reasons.

5. **[14.D] “a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a substantially circular section; and”**

This limitation is substantively the same as [8.D] (but does not recite a spacer) and is met for the same reasons. *See also* [1.D].

6. **[14.E] “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,”**

This limitation is identical to a limitation in [3.A] and is met for the same reasons.

7. **[14.F] “wherein: a first diameter of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs; and”**

This limitation is identical to [7] and is met for the same reasons.

8. **[14.G] “a peripheral contact is arranged outside the memory stack and in contact with a peripheral device on the substrate.”**

This limitation is substantively the same as [2] and is met for the same reasons.

**K. Claim 15:**

**1. [15.PRE] “The 3D memory device of claim 14, wherein:”**

Nishikawa in view of the knowledge of a POSITA renders obvious the 3D memory device of claim 14. *See* [14.PRE]-[G], above.

**2. [15.A] “a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact; and”**

This limitation is substantively the same as [9.B] and is met for the same reasons.

**3. [15.B] “a diameter of the TAC is at least equal to a diameter of the peripheral contact.”**

This limitation is substantively the same as [6.C] and is met for the same reasons.

**L. Claim 16:**

**1. [16] “The 3D memory device of claim 15, wherein: a diameter of the dummy channel structure is smaller than each of the diameter of the TAC and the diameter of the peripheral contact.”**

This limitation is identical to [6.D] and is met for the same reasons.

**M. Claim 19:**

**1. [19] “The 3D memory device of claim 1, wherein: the TAC has a substantially circular section and comprises a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC.”**

This limitation is substantively the same as [8.D] and is met for the same reasons. *See also* [1.D].

**N. Claim 20:**

- 1. [20] “The 3D memory device of claim 14, wherein: the TAC comprises a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC.”**

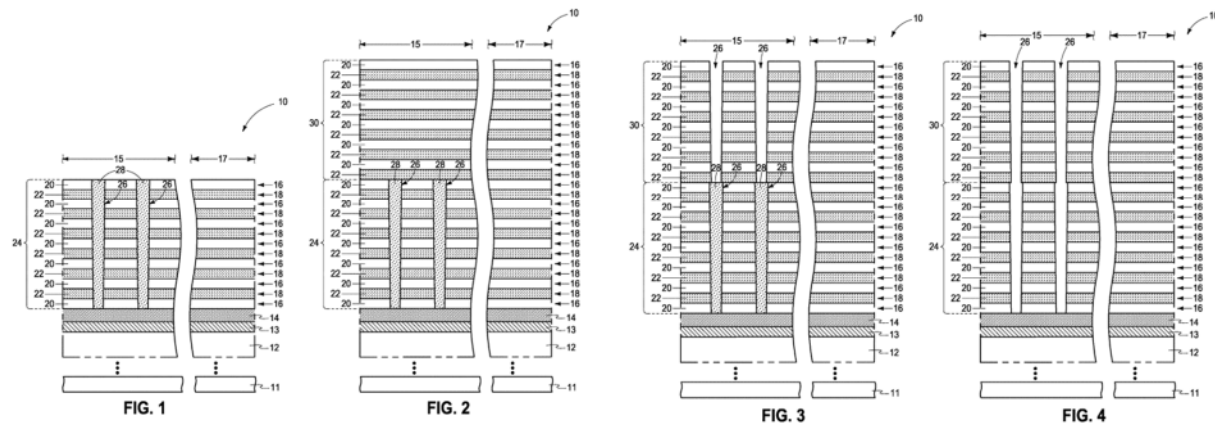
This limitation is substantively the same as [8.D] and is met for the same reasons.

**XI. GROUND 2: NISHIKAWA IN VIEW OF LU AND THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 4-5, 11-12, AND 17-18**

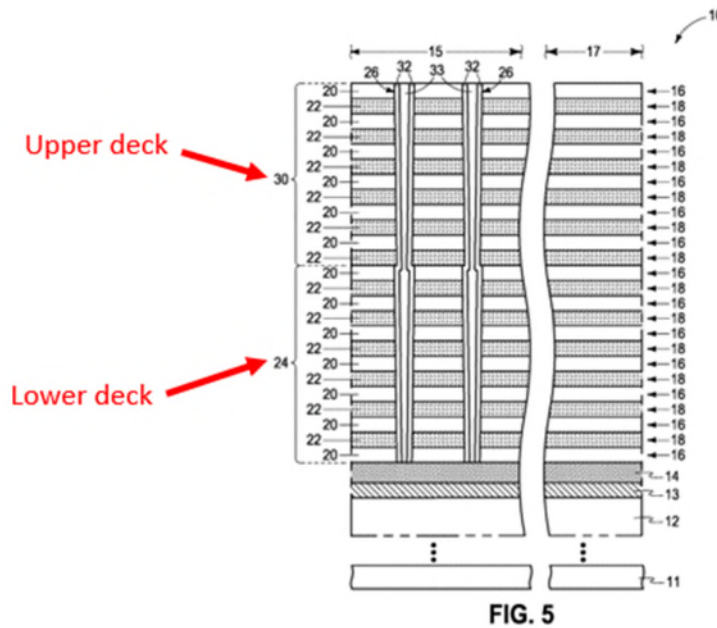
**A. Motivation to Combine**

A POSITA would have been motivated to combine Nishikawa with Lu’s teachings of multi-deck 3D memory stacks with a reasonable expectation of success for several reasons.

To start, a multi-deck memory stack refers to forming a first stack and then forming a second stack on top of the first. Lee Decl., ¶ 204. The driving motivation for multi-deck structures is the difficulty in etching high aspect ratio channel holes. This challenge became a limiting factor to memory density. Ex. 1010, 211-215. A multi-deck structure, however, enables the formation of high aspect ratio channel holes by forming the first deck, etching a hole through the first deck, forming the second deck, and then etching another hole through the top deck. This is shown below:



Ex. 1036, Fig. 1-4. The final channel structure is shown below:

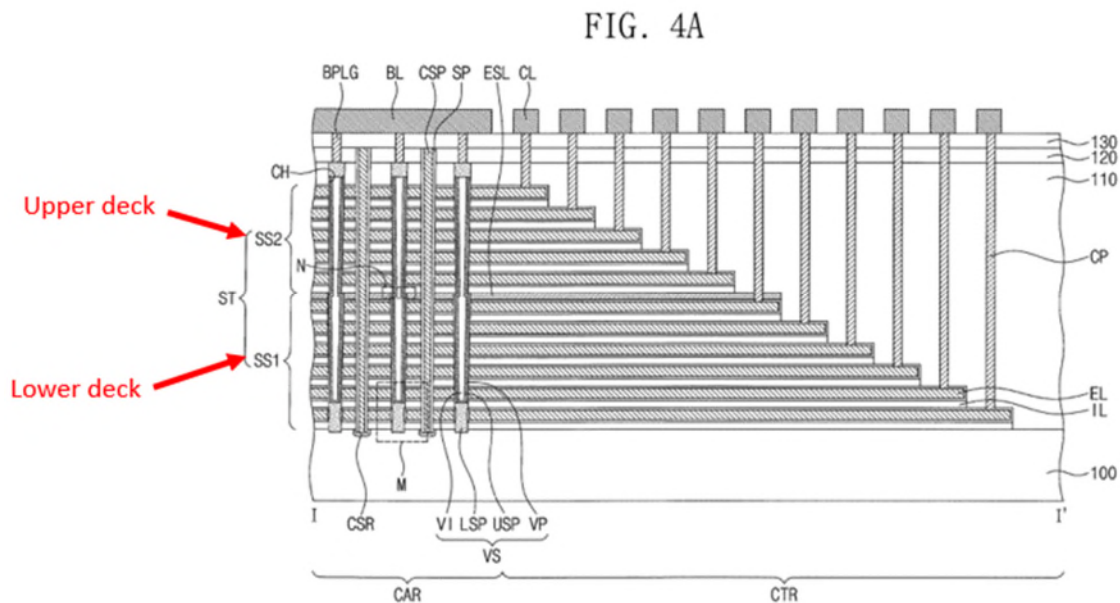


*Id.*, Fig. 5 (annotated). As can be seen above, each hole tapers due to natural etch processes. If there was only a single etch through a single stack with the same number of layers as both decks, the taper would be so large that the hole's diameter on the top would be too large, requiring too much surface area for a single channel.

Lee, ¶¶ 205-07. In effect, the taper would be twice as much, and the channel footprint on the surface of the top stack layer would be double in size. *Id.*

The benefits of multi-deck structures thus became well known. Indeed, by 2012, Micron was improving the process of multi-decks, recognizing this benefit of separately etching through each stack: “A deck-by-deck process flow has an advantage of a lower etching aspect ratio.” Ex. 1040, 1:28-29; Lee, ¶ 208.

As such, multi-deck 3D memories became the norm. For example, U.S. Patent No. 10,381,369 (“Kim 369”) discloses a multi-deck 3D NAND stack structure:



Ex. 1041, Fig. 4A (annotated). Kim 369 discloses that “[e]ach of the stack structures ST may include a lower structure SS1 and an upper structure SS2. The upper structure SS2 may be disposed on the lower structure SS1.” *Id.*, 5:60-6:1.

As yet another example, U.S. Patent Publication No. 2018/0301374

(“Masamori”) discloses a multi-deck 3D NAND stack structure:

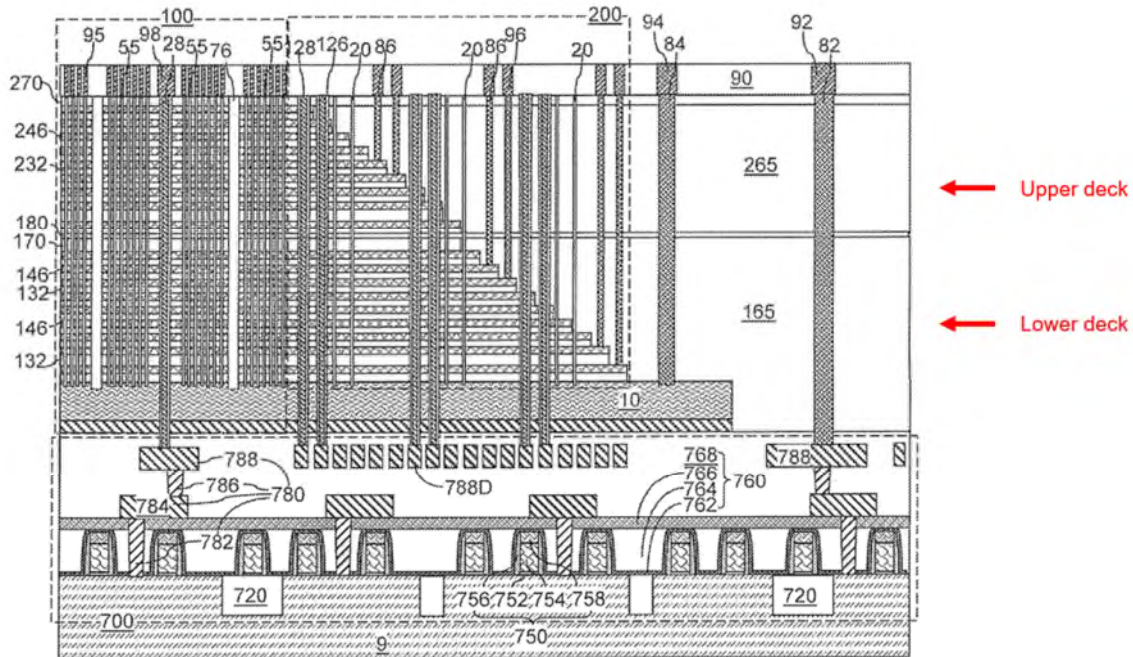


FIG. 14

Masamori, Fig. 14 (annotated). Masamori discloses that “[a] second tier structure can be formed over the first tier structure (132, 142, 170, 131). The second tier structure can include an additional alternating stack of insulating layers and spacer material layers, which can be sacrificial material layers.” *Id.*, [0073]; Lee, ¶¶ 209-211.

Turning to Lu, Lu is entitled “Apparatuses and methods for forming multiple decks of memory cells.” Lu, 1. Lu itself recognizes that “[a]s demand for storage capacity increases, the number of memory cell levels in some memory devices may be increased to accommodate the increased storage capacity. In some cases, forming

such memory devices using conventional techniques may pose a challenge.” *Id.*, 1:13-22. That is, forming the dense array via high-aspect ratios poses a challenge. Lee Decl., ¶ 212. Thus, Lu discloses techniques to form a first deck, etch the channel sub-hole, form a deck on top of that, and then etch another channel sub-hole. *E.g.*, Lu, Fig. 3. Thus, a POSITA would have been highly motivated to employ Lu’s teachings, and multi-deck teachings in general, to at least reduce the widths of the channel holes in Nishikawa’s memory and increase memory density. Lee Decl., ¶ 212.

A POSITA would have had a reasonable expectation of success in adapting Nishikawa to include a multi-deck structure. As the above multi-deck structures illustrate, multi-deck structures were the norm, including in devices that employ TACs and the other conventional Nishikawa features. Typically, the process first creates the multi-deck structure and channels, and then creates the TACs and slits. *E.g.*, Ex. 1036, [0029]-[0033] (forming decks and channels), [0034]-[0037] (forming staircase), [0038]-[0040] (forming TACs and dummy structures), [0041]-[0044] (forming trenches and performing gate replacement process). That is, the multi-deck structure is fully compatible with Nishikawa’s other 3D structures. Thus, a POSITA would have had a reasonable expectation of success in implementing the alternating stack (32, 46) of Nishikawa as a multi-deck structure. Lee, ¶ 213.

**B. Claim 4:**

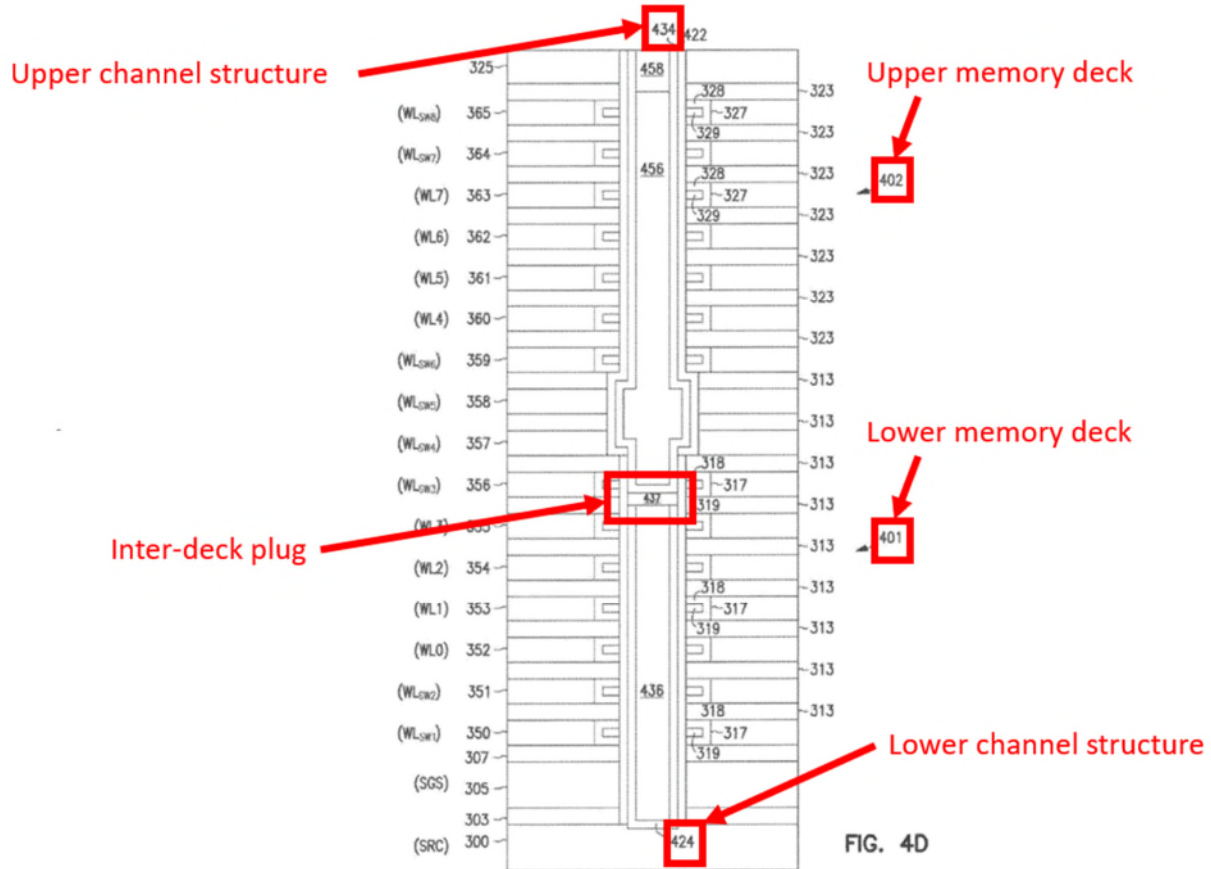
**1. [4.PRE] “The 3D memory device of claim 1, wherein the memory stack comprises:”**

Nishikawa discloses or renders obvious in view of the knowledge of a POSITA the 3D memory device of claim 1. *See* [1.PRE]-[E], above.

As discussed in [1PRE]-[E], Nishikawa discloses a memory stack having alternating dielectric and conductor layers. As the below demonstrates, it would have been obvious to implement this memory stack as a multi-deck structure to include lower and upper decks in view of Lu’s teachings. *See* §XI.A.

**2. [4.A] “a lower memory deck on the substrate; and”**

Lu discloses a lower memory deck (“deck 401”) and a substrate (“source material 300”). Lu discloses, for example, “source material 300 can include a conductively doped region of a semiconductor substrate.” Lu, 8:25-26.

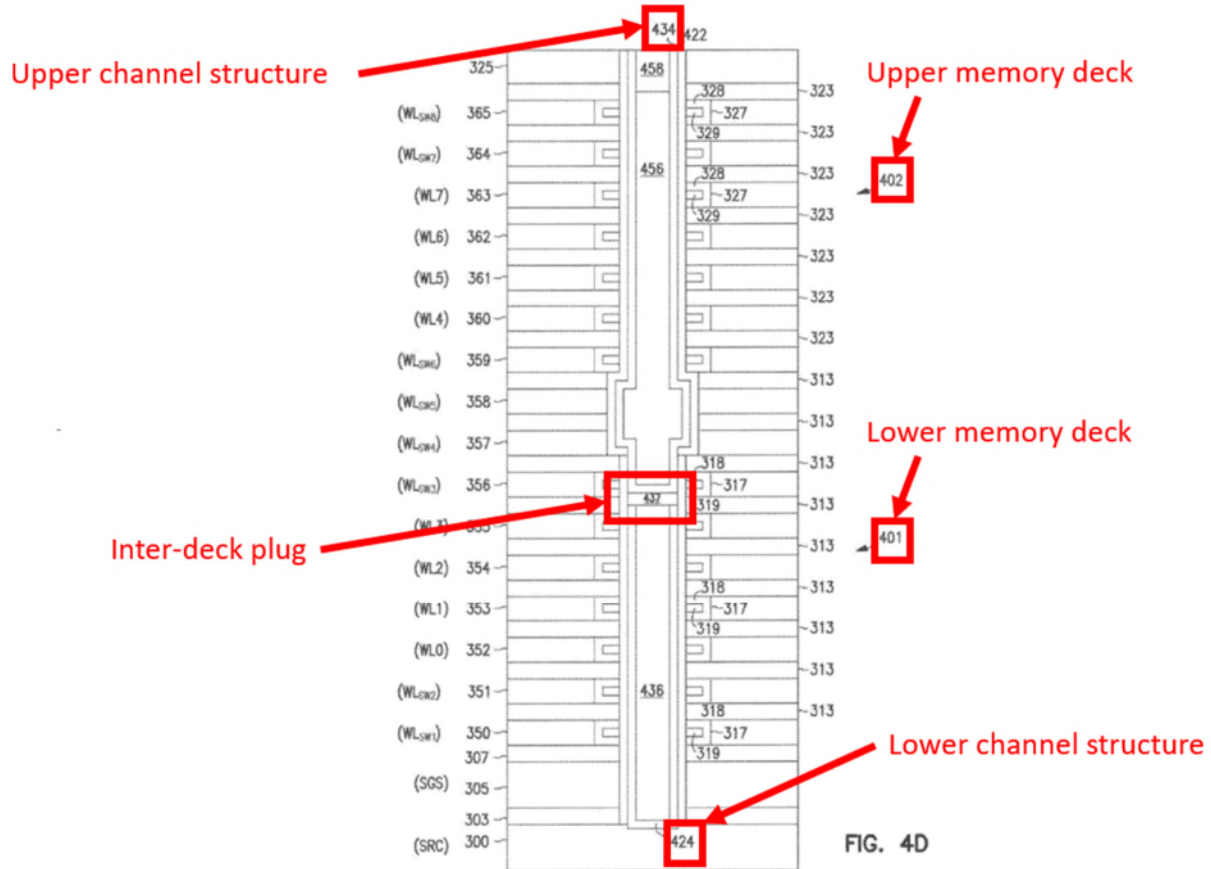


Lu, Fig. 4D (annotated), 14:29-44 (lower deck 401), 14:59-61 (decks 401 and 402);

Lee, ¶ 216.

**3. [4.B] “an upper memory deck above the lower memory deck.”**

Lu discloses an upper memory deck (“deck 402”) above the lower memory deck (“deck 401”), as illustrated below.



Lu, Fig. 4D (annotated) 14:59-61 (deck 402); Lee, ¶ 217.

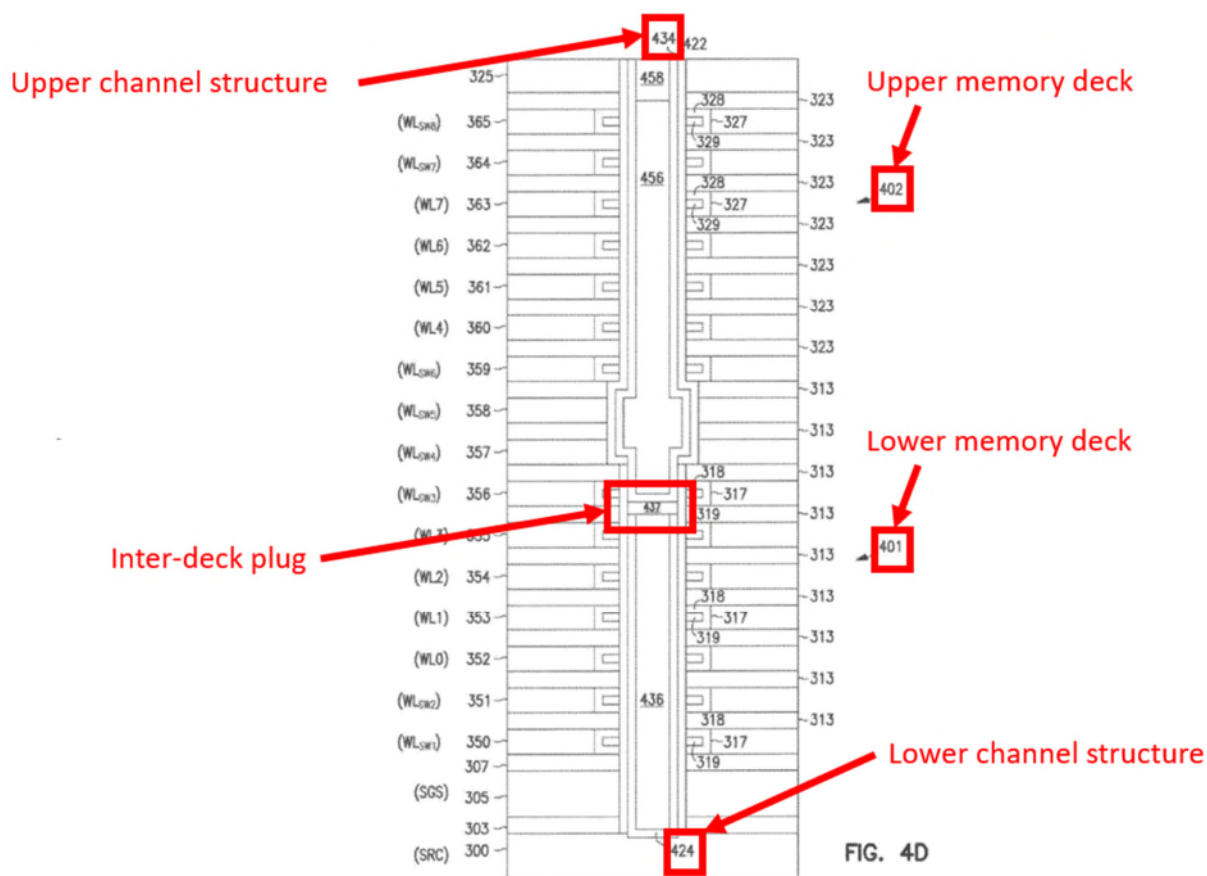
### C. Claim 5:

1. [5.PRE] “The 3D memory device of claim 4, wherein the channel structure comprises:”

Nishikawa in view of Lu and the knowledge of a POSITA renders obvious the 3D memory device of claim 4. See [4PRE]-[B], above.

2. [5.A] “a lower channel structure extending vertically through the lower memory deck;”

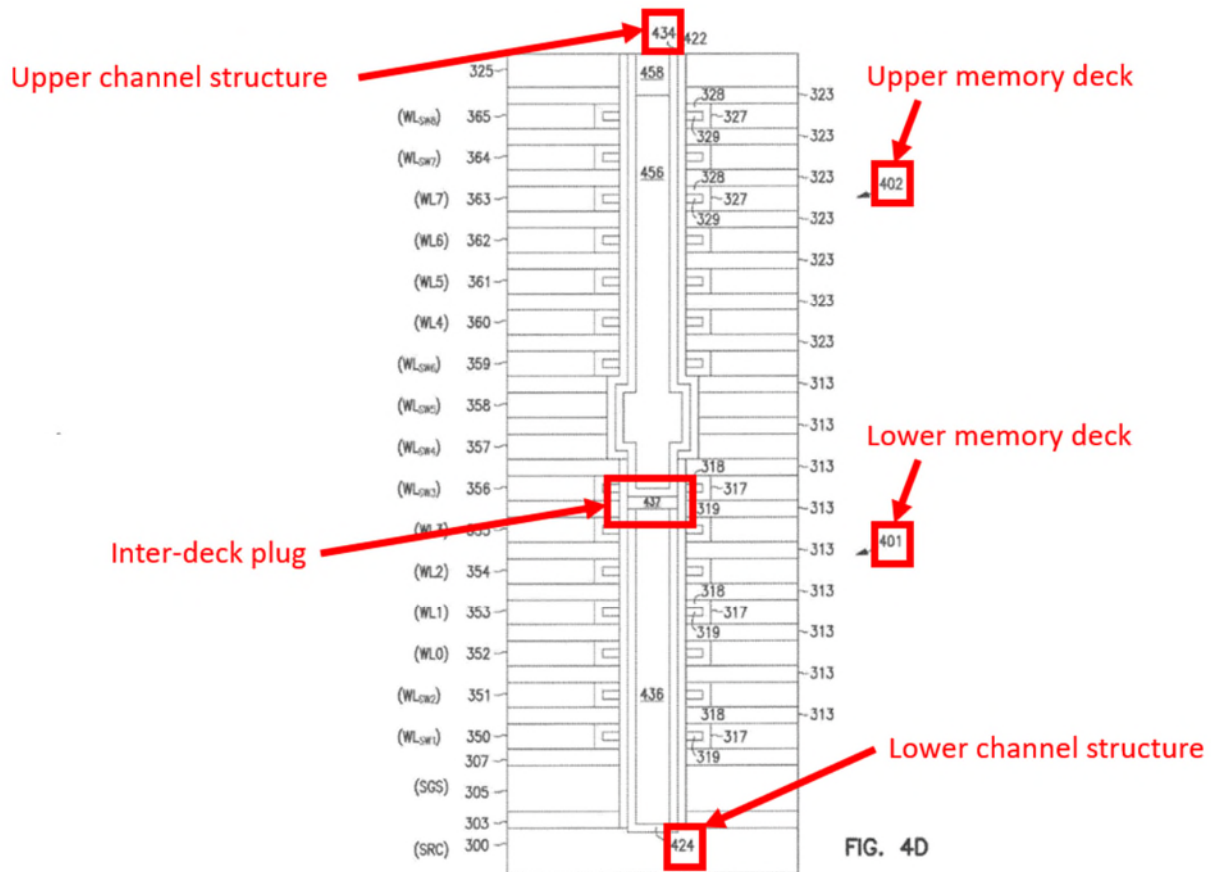
Lu discloses a lower channel structure (channel material 424) extending vertically through the lower memory deck (“deck 401”).



Lu, Fig. 4D (annotated). Lu discloses that “deck 401 can include a hole 410 extending through materials that include conductor materials 350 through 358, dielectric materials 313, and capping material 315. Hole 410 can contain tunneling material 312 on its sidewalls. At a portion of hole 410 (e.g., portion from source material 300 to approximately dielectric material 313 between conductor materials 355 and 356), **a channel material 424 is formed adjacent tunneling material 312 and source material 300.** A dielectric material 436 is also formed in hole 410 and is surrounded by channel material 424.” *Id.*, 14:29-38; Lee, ¶ 219.

3. **[5.B] “an upper channel structure extending vertically through the upper memory deck; and”**

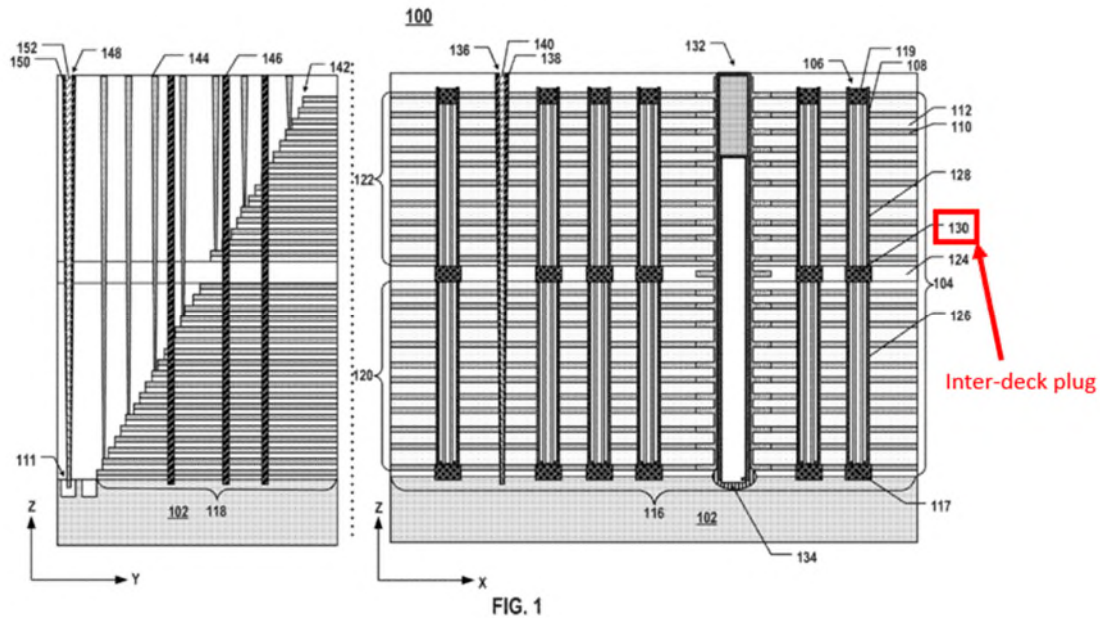
Lu discloses an upper channel structure (“channel material 434”) extending vertically through the upper memory deck (“deck 402”).



Lu, Fig. 4D (annotated), 14:57-62 (channel material 434); Lee, ¶ 220.

4. [5.C] “an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.”

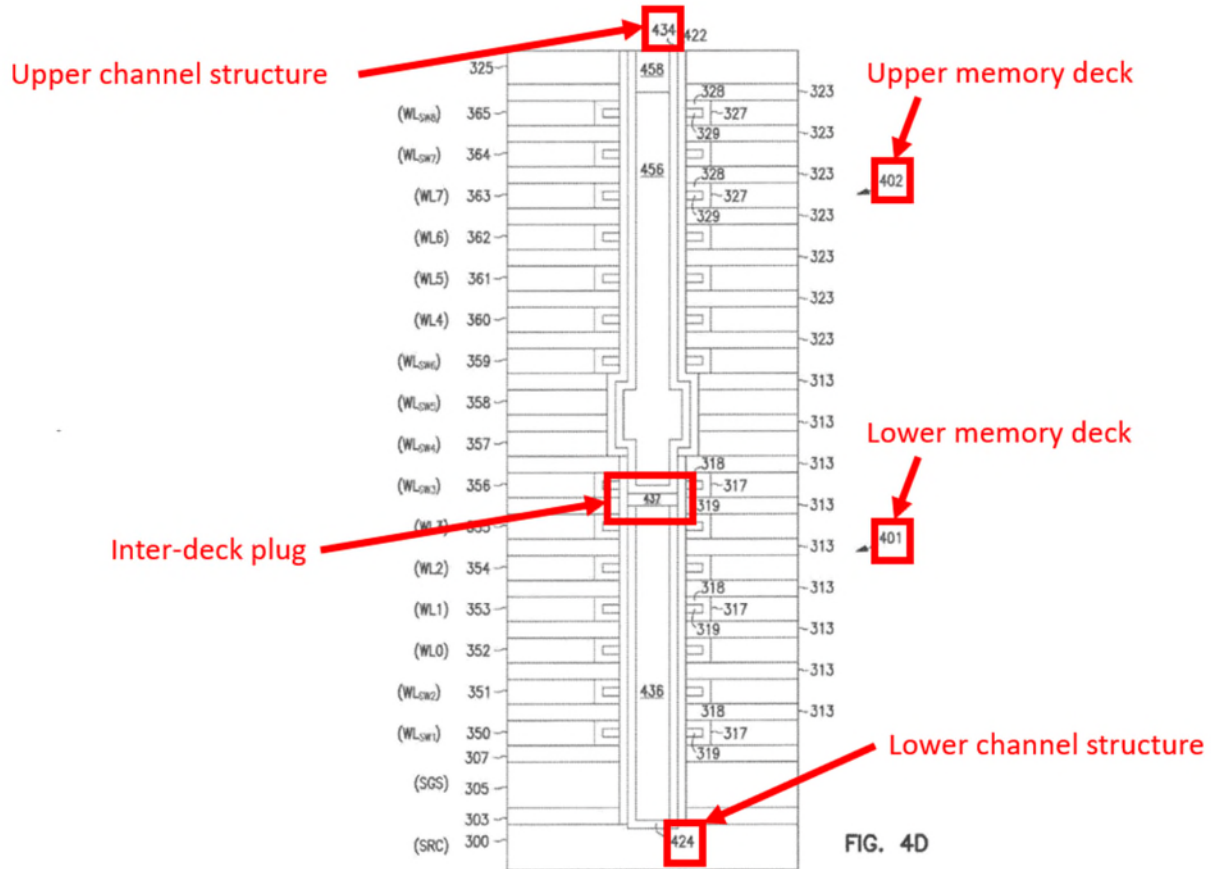
As an initial matter, the '322 Patent depicts “inter-deck plug” 130 as follows:



Ex. 1001, Fig. 1 (annotated); Lee, ¶ 221. The '332 Patent discloses that “an inter-deck plug 130 is disposed vertically between and in contact with lower channel structure 126 and upper channel structure 128. Inter-deck plug 130 can include semiconductor materials, such as polysilicon, and joint (e.g., electrically connect) lower and upper channel structures 126 and 128 to form channel structure 108.” Ex. 1001, 7:60-66.

Lu discloses exactly the same structure between the lower and upper decks. Specifically, Lu discloses an inter-deck plug (“material 437”) disposed vertically

between and in contact with the lower channel structure (“channel material 424”) and the upper channel structure (“channel material 434”):



Lu, Fig. 4D (annotated); Lee, ¶ 222.

Lu discloses “with reference to FIG. 4A through FIG. 4D may be used to form a . . . channel with solid conductive plug (e.g., polysilicon plug) between the . . . channel.” Lu, 14:26-28. Lu further discloses that “[a] material 437 can be formed adjacent tunneling material 312 . . . . Material 437 can include polysilicon (e.g., conductively doped polysilicon).” As illustrated, conductive polysilicon material 437 is formed between and in contact with the lower channel material 424 and upper

channel material 434, and thus a POSITA would understand the material 437 to be an inter-deck plug as claimed. Lee, ¶ 223.

Notably, the inter-deck plug provides a larger interface between the sub-channels, i.e., the lower and upper deck channel structures. This beneficially ensures electrical coupling between the sub-channel plugs to ensure the sub-channels collectively operate as a single channel structure. Lee, ¶ 222.

**D. Claim 11:**

1. **[11.PRE] “The 3D memory device of claim 8, wherein the memory stack comprises:”**

Nishikawa in view of the knowledge of a POSITA renders obvious the 3D memory device of claim 8. *See* [8.A]-[D], above.

2. **[11.A] “a lower memory deck on the substrate; and”**

This limitation is identical to [4.A] and is met for the same reasons.

3. **[11.B] “an upper memory deck above the lower memory deck.”**

This limitation is identical to [4.B] and is met for the same reasons.

**E. Claim 12:**

1. **[12.PRE] “The 3D memory device of claim 11, wherein the channel structure comprises:”**

Nishikawa in view of Lu and the knowledge of a POSITA renders obvious the 3D memory device of claim 11. *See* [11.PRE]-[B], above.

2. **[12.A] “a lower channel structure extending vertically through the lower memory deck;”**

This limitation is identical to [5.A] and is met for the same reasons.

3. **[12.B] “an upper channel structure extending vertically through the upper memory deck; and”**

This limitation is identical to [5.B] and is met for the same reasons.

4. **[12.C] “an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.”**

This limitation is identical to [5.C] and is met for the same reasons.

**F. Claim 17:**

1. **[17.PRE] “The 3D memory device of claim 14, wherein the memory stack comprises:”**

Nishikawa in view of the knowledge of a POSITA renders the 3D memory device of claim 14 obvious. *See* [14.PRE]-[G], above.

2. **[17.A] “a lower memory deck on the substrate; and”**

This limitation is identical to [4.A] and is met for the same reasons.

3. **[17.B] “an upper memory deck above the lower memory deck.”**

This limitation is identical to [4.B] and is met for the same reasons.

**G. Claim 18:**

1. **[18.PRE] “The 3D memory device of claim 17, wherein the channel structure comprises:”**

Nishikawa in view of Lu and the knowledge of a POSITA renders obvious the 3D memory device of claim 17. *See* [17.PRE]-[B], above.

2. **[18.A] “a lower channel structure extending vertically through the lower memory deck;”**

This limitation is identical to [5.A] and is met for the same reasons.

3. **[18.B] “an upper channel structure extending vertically through the upper memory deck; and”**

This limitation is identical to [5.B] and is met for the same reasons.

4. **[18.C] “an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.”**

This limitation is identical to [5.C] and is met for the same reasons.

**XII. GROUND 3: NISHIKAWA IN VIEW OF NISHIKAWA2 AND THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 1-3, 6-10, 13-16, AND 19-20**

Ground 3 applies the same claim mapping and arguments as Ground 1. Ground 3 simply expressly combines Nishikawa2’s express teaching of a circular TAC (along with the knowledge of a POSITA) with Nishikawa should PO argue that an express combination is necessary. The analysis below, therefore, does not repeat the claim mapping and only addresses the motivation to combine the Nishikawa references.

**A. Motivation to Combine**

A POSITA would have been motivated to combine Nishikawa with Nishikawa2, and specifically, to employ Nishkawa2’s teaching of circular TACs for several reasons.

To start, as §IX.A-B demonstrate, these references present the same memory architecture and key components—indeed, the provisional applications, filed by the same inventor, leading to these patents were filed only 5 days apart. Nishikawa, Cover; Nishikawa2, Cover. A POSITA would have considered potential improvements in Nishikawa2 given that its provisional was filed 5 days later. Lee Decl., ¶ 239.

Next, Nishikawa2 expressly recognizes that the source line connection can be circular, and as §X.A.5 demonstrates, expressly recognizes that this can increase memory capacity by removing the trench structure. Nishikawa2, 22:38-41, 27:55-28:3; Lee Decl., ¶ 240. §X.A.5 demonstrates other benefits, namely, spreading the source contacts throughout the array.

§X.A.5 demonstrates that a POSITA would have had a reasonable expectation of success in employing a circular TAC like the one in Nishikawa2 in Nishikawa. Lee Decl., ¶ 241.

**XIII. GROUND 4: NISHIKAWA IN VIEW OF NISHIKAWA2 AND LU AND THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 4-5, 11-12, AND 17-18**

Ground 4 applies the same claim mapping and arguments as Ground 3. Ground 4 simply expressly combines Lu's teaching of multiple stacks (along with the knowledge of a POSITA) to the combination of Nishikawa and Nishikawa2 should PO argue that an express combination is necessary. The analysis, therefore, does not repeat the claim mapping. Further, the motivations to combine Nishikawa and Nishikawa2 are set forth in XII. The motivations to include Lu's multi-deck structure are set forth in XI.A. The addition of Nishikawa2 to this ground has no impact on the benefits of including multi-deck structures, because increasing memory density provides the same benefit when considering Nishikawa and Nishikawa2 together. Nor is there any impact on the reasonable expectation of success, as circular TAC through multi-deck structures were a typical prior art feature. Lee Decl., ¶ 242.

**XIV. SECONDARY CONSIDERATIONS**

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See generally* Ex. 1002. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

**XV. CONCLUSION**

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

Dated: December 2, 2024

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**CERTIFICATE OF COMPLIANCE**

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,809 words.

Dated: December 2, 2024

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**CERTIFICATE OF SERVICE**

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated documents and exhibits were caused to be served on December 2, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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Copies of this Petition and accompanying documents and exhibits were also served via electronic mail on Patent Owner's counsel of record for related PTAB proceedings and in the related district court litigation – ROPES & GRAY LLP and LATHAW & WATKINS LLP:

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