

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT6413769

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
MEI LAN GUO	09/05/2018
YUSHI HU	08/22/2018
JI XIA	08/22/2018
HONGBIN ZHU	08/29/2018
RECEIVING PARTY DATA	
Name:	YANGTZE MEMORY TECHNOLOGIES CO., LTD.
Street Address:	18 GAOXIN 4TH ROAD
Internal Address:	EAST LAKE HIGH-TECH DEVELOPMENT ZONE
City:	WUHAN, HUBEI
State/Country:	CHINA
PROPERTY NUMBERS Total: 1	
Property Type	Number
Application Number:	17100847
CORRESPONDENCE DATA	
Fax Number:	(703)821-8128
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
Phone:	703-995-9887
Email:	uspto@bayes.law
Correspondent Name:	BAYES PLLC
Address Line 1:	1765 GREENSBORO STATION PLACE
Address Line 2:	SUITE 900
Address Line 4:	MCLEAN, VIRGINIA 22102
ATTORNEY DOCKET NUMBER:	10018-01-0015-US-DIV2
NAME OF SUBMITTER:	ZHIWEI ZOU
SIGNATURE:	/Zhiwei Zou/
DATE SIGNED:	11/21/2020
This document serves as an Oath/Declaration (37 CFR 1.63).	
Total Attachments: 3	

source=10018-01-0015-US_Declaration-Assign#page1.tif

source=10018-01-0015-US_Declaration-Assign#page2.tif

source=10018-01-0015-US_Declaration-Assign#page3.tif

COMBINED DECLARATION AND ASSIGNMENT**DECLARATION**

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☒ The attached application, or
- ☐ United States application or PCT international application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

Appl. No. *To Be Assigned*
Atty. Docket No. 10018-01-0015-PCT

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

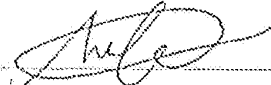
The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 153988** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

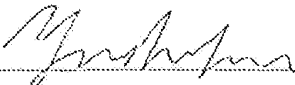
IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Mei Lan Guo Date: 2018.9.5

Signature of Inventor: 

Inventor: Yushi Hu Date: 2018.08.22

Signature of Inventor: 

Inventor: Ji Xia Date: 2018/8/22

Signature of Inventor: Ji Xia

Inventor: Hongbin Zhu Date: 2018/8/29

Signature of Inventor: 

SCORE Placeholder Sheet for IFW Content

Application Number: 17100847

Document Date: 11/21/2020

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

- Drawing

At the time of document entry (noted above):

- USPTO employees may access SCORE content via DAV or via the SCORE web page.
- External customers may access SCORE content via PAIR using the Supplemental Content tab.

Form Revision Date: March 1, 2019

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>	Attorney Docket No.	10018-01-0015-US-DIV2
	First Named Inventor	Mei Lan GUO
	Title	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
	Priority Mail Express® Label No.	

APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents.</i>	Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
1. ☒ Fee Transmittal Form (PTO/SB/17 or equivalent)	ACCOMPANYING APPLICATION PAPERS
2. ☐ Applicant asserts small entity status. See 37 CFR 1.27	10. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee <u>Yangtze Memory Technologies Co., Ltd.</u>
3. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.	11. ☐ 37 CFR 3.73(c) Statement ☒ Power of Attorney (when there is an assignee)
4. ☒ Specification [Total Pages <u>31</u>] Both the claims and abstract must start on a new page. (See MPEP § 608.01(a) for information on the preferred arrangement)	12. ☐ English Translation Document (if applicable)
5. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>20</u>]	13. ☒ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached
6. ☐ Inventor's Oath or Declaration [Total Pages <u>3</u>] (including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))	14. ☐ Preliminary Amendment
a. ☐ Newly executed (original or copy)	15. ☐ Return Receipt Postcard (MPEP § 503) (Should be specifically itemized)
b. ☒ A copy from a prior application (37 CFR 1.63(d))	16. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
7. ☒ Application Data Sheet * See note below. See 37 CFR 1.76 (PTO/AIA/14 or equivalent)	17. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
8. ☐ CD-ROM or CD-R in duplicate, large table, or Computer Program (Appendix) ☐ Landscape Table on CD	18. ☐ Other: _____ _____ _____ _____
9. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. – c. are required)	
a. ☐ Computer Readable Form (CRF)	
b. ☐ Specification Sequence Listing on:	
i. ☐ CD-ROM or CD-R (2 copies); or	
ii. ☐ Paper	
c. ☐ Statements verifying identity of above copies	

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
 (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS					
☒ The address associated with Customer Number: <u>153988</u> OR ☐ Correspondence address below					
Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	
Signature	/Zhiwei Zou/			Date	11/21/2020
Name (Print/Type)	Zhiwei Zou			Registration No. (Attorney/Agent)	66,041

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

FEE TRANSMITTAL		Complete if known	
		Application Number	
		Filing Date	Herewith
☐ Applicant asserts small entity status. See 37 CFR 1.27.		First Named Inventor	Mei Lan GUO
☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.		Examiner Name	To Be Determined
		Art Unit	To Be Determined
TOTAL AMOUNT OF PAYMENT	(\$)	Practitioner Docket No.	10018-01-0015-US-DIV2

METHOD OF PAYMENT (check all that apply)
☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 60-2227 Deposit Account Name: BAYES DEPOSIT ACCOUNT

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**
☒ Charge any additional fee(s) or underpayment of fee(s) ☐ Credit any overpayment of fee(s) under 37 CFR 1.16 and 1.17

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION**1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)**

Application Type	FILING FEES			SEARCH FEES			EXAMINATION FEES			Fees Paid (\$)
	U (\$)	S (\$)	M (\$)	U (\$)	S (\$)	M (\$)	U (\$)	S (\$)	M (\$)	
Utility	320	160*	80	700	350	175	800	400	200	1820
Design	220	110	55	160	80	40	640	320	160	
Plant	220	110	55	440	220	110	660	330	165	
Reissue	320	160	80	700	350	175	2,320	1,160	580	
Provisional	300	150	75	0	0	0		0	0	

* The \$150 small entity status filing fee for a utility application is further reduced to \$75 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	Undiscounted Fee (\$)	Small Entity Fee (\$)	Micro Entity Fee (\$)
Each claim over 20 (including Reissues)	100	50	25
Each independent claim over 3 (including Reissues)	480	240	120
Multiple dependent claims	860	430	215

Total Claims	Extra Claims	Fee (\$)	Fee Paid (\$)
6	0	0.00	

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee (\$)	Fee Paid (\$)	Multiple Dependent Claims	Fee (\$)	Fee Paid (\$)
2	0	0.00				

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$420 (\$210 for small entity) (\$105 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
20				

4. OTHER FEE(S)

Non-English specification, \$140 fee (\$70 for small entity) (\$35 for micro entity)

Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, \$400 fee (\$200 small or micro entity)

Other (e.g., late filing surcharge): _____

SUBMITTED BY

Signature	/Zhiwei Zou/	Registration No. (Attorney/Agent)	66,041	Telephone	
Name (Print/Type)	Zhiwei Zou			Date	11/21/2020

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	10018-01-0015-US-DIV2
		Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1					Remove						
Legal Name											
Prefix	Given Name			Middle Name			Family Name			Suffix	
	Mei Lan						Guo				
Residence Information (Select One)					US Residency					• Non US Residency	Active US Military Service
City	Wuhan			Country of Residence ⁱ			CN				
Mailing Address of Inventor:											
Address 1		18 Gaoxin 4th Road									
Address 2		East Lake High-Tech Development Zone									
City	Wuhan			State/Province							
Postal Code					Country ⁱ		CN				
Inventor 2					Remove						
Legal Name											
Prefix	Given Name			Middle Name			Family Name			Suffix	
	Yushi						Hu				
Residence Information (Select One)					US Residency					● Non US Residency	Active US Military Service
City	Wuhan			Country of Residence ⁱ			CN				
Mailing Address of Inventor:											
Address 1		18 Gaoxin 4th Road									
Address 2		East Lake High-Tech Development Zone									
City	Wuhan			State/Province							
Postal Code					Country ⁱ		CN				
Inventor 3					Remove						
Legal Name											

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	10018-01-0015-US-DIV2
		Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ji		Xia	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				

City	Wuhan	Country of Residence ⁱ	CN
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Mailing Address of Inventor:

Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan	State/Province	
Postal Code		Country ⁱ	CN
Inventor	4	Remove	

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hongbin		Zhu	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				

City	Wuhan	Country of Residence ⁱ	CN
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Mailing Address of Inventor:

Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan	State/Province	
Postal Code		Country ⁱ	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence Information of this application.

Customer Number	153988		
Email Address	uspto@bayes.law	Add Email	Remove Email

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	10018-01-0015-US-DIV2
		Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		

Application Information:

Title of the Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		
Attorney Docket Number	10018-01-0015-US-DIV2	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	20	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	153988		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	10018-01-0015-US-DIV2
		Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Division of	16745342	2020-01-17
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16745342	Division of	16149103	2018-10-01
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16149103	Continuation of	PCT/CN2018/101482	2018-08-21
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)	Remove
Additional Foreign Priority Data may be generated within this form by selecting the Add button.				Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	10018-01-0015-US-DIV2
		Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.



NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	10018-01-0015-US-DIV2
		Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	10018-01-0015-US-DIV2
		Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	10018-01-0015-US-DIV2
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Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	10018-01-0015-US-DIV2
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Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		

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ABSTRACT

Embodiments of three-dimensional (3D) memory devices having through array contacts (TACs) and methods for forming the same are disclosed. In an example, a 3D memory device includes a substrate, a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs, a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack, a TAC extending vertically through the conductor/dielectric layer pairs in the memory stack, and a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.

WHAT IS CLAIMED IS:

1. A three-dimensional (3D) memory device, comprising:
 - a substrate;
 - a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs;
 - a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;
 - a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack; and
 - a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.
2. The 3D memory device of claim 1, further comprising:
 - a peripheral device on the substrate; and
 - a peripheral contact outside of the memory stack and in contact with the peripheral device.
3. The 3D memory device of claim 2, wherein each of the TAC and peripheral contact comprises a spacer with a nominally same thickness.
4. The 3D memory device of claim 3, wherein the dielectric layer in the dummy channel structure and the spacers in the TAC and peripheral contact comprise silicon oxide.
5. The 3D memory device of claim 1, wherein the memory stack comprises:
 - a lower memory deck on the substrate; and
 - an upper memory deck above the lower memory deck.
6. The 3D memory device of claim 5, wherein the channel structure comprises:
 - a lower channel structure extending vertically through the lower memory deck;
 - an upper channel structure extending vertically through the upper memory deck; and
 - an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.

Atty. Dkt. No. 10018-01-0015-US-DIV2

THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is divisional of U.S. Application No. 16/745,342, filed on January 17, 2020, entitled “THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME,” which is divisional of U.S. Application No. 16/149,103, filed on October 1, 2018, entitled “THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME,” which is continuation of International Application No. PCT/CN2018/101482, filed on August 21, 2018, entitled “THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME,” all of which are hereby incorporated by reference in their entireties.

BACKGROUND

[0002] Embodiments of the present disclosure relate to three-dimensional (3D) memory devices and fabrication methods thereof.

[0003] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As a result, memory density for planar memory cells approaches an upper limit.

[0004] A 3D memory architecture can address the density limitation in planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array.

SUMMARY

[0005] Embodiments of 3D memory devices and fabrication methods thereof are disclosed herein.

Atty. Dkt. No. 10018-01-0015-US-DIV2

[0006] In one example, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A first opening extending vertically through the dielectric stack is formed. A spacer is formed on a sidewall of the first opening. A through array contact (TAC) extending vertically through the dielectric stack is formed by depositing a conductor layer in contact with the spacer in the first opening. A slit extending vertically through the dielectric stack is formed after forming the TAC. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0007] In another example, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A dummy channel structure extending vertically through the dielectric stack is formed. A first opening through the dielectric stack and a second opening outside of the dielectric stack are simultaneously etched. A first spacer on a sidewall of the first opening and a second spacer on a sidewall of the second opening are simultaneously formed. A conductor layer is deposited (i) filling in the first opening to form a TAC and (ii) filling in the second opening to form a peripheral contact. A slit extending vertically through the dielectric stack is formed after forming the TAC and peripheral device. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0008] In still another example, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A first opening through the dielectric stack, a second opening outside of the dielectric stack, and a third opening through the dielectric stack are simultaneously etched. A lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings. A dielectric layer is deposited (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the

second opening. Parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening are removed. A conductor layer is deposited (i) filling in the first opening to form a TAC and (ii) filling in the second opening to form a peripheral contact. A slit extending vertically through the dielectric stack is formed after forming the TAC and peripheral device. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0009] In a different example, a 3D memory device includes a substrate, a memory stack on the substrate including a plurality of conductor/dielectric layer pairs, a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack, a TAC extending vertically through the conductor/dielectric layer pairs in the memory stack, and a dummy channel structure fully filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0011] FIG. 1 illustrates a cross-section of an exemplary 3D memory device, according to some embodiments of the present disclosure.

[0012] FIGs. 2A–2E illustrate an exemplary fabrication process for forming channel structures of a 3D memory device, according to some embodiments of the present disclosure.

[0013] FIGs. 3A–3F illustrate exemplary fabrication processes for forming TACs, peripheral contacts, and dummy channel structures of a 3D memory device, according to various embodiments of the present disclosure.

[0014] FIGs. 4A–4C illustrate another exemplary fabrication process for forming TACs, peripheral contacts, and dummy channel structures of a 3D memory device, according to some embodiments of the present disclosure.

Atty. Dkt. No. 10018-01-0015-US-DIV2

- [0015] FIGs. 5A–5B illustrate an exemplary fabrication process for forming a slit structure and word line contacts of a 3D memory device, according to some embodiments of the present disclosure.
- [0016] FIG. 6 is a flowchart of an exemplary method for forming a 3D memory device, according to some embodiments.
- [0017] FIG. 7A is a flowchart of an exemplary method for forming a spacer on a sidewall of an opening, according to some embodiments of the present disclosure.
- [0018] FIG. 7B is a flowchart of another exemplary method for forming a spacer on a sidewall of an opening, according to some embodiments of the present disclosure.
- [0019] FIG. 8 is a flowchart of another exemplary method for forming a 3D memory device, according to some embodiments of the present disclosure.
- [0020] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

- [0021] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.
- [0022] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.
- [0023] In general, terminology may be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon

context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” may be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0024] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something but also includes the meaning of “on” something with an intermediate feature or a layer therebetween, and that “above” or “over” not only means the meaning of “above” or “over” something but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

[0025] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0026] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0027] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous

structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend laterally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which interconnect lines and/or via contacts are formed) and one or more dielectric layers.

[0028] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0029] As used herein, the term “3D memory device” refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND memory strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

[0030] In some 3D memory devices, interconnects can include through array contacts (TACs) for providing vertical interconnects between the stacked memory array device and peripheral device (e.g., for power bus and metal routing), thereby reducing metal levels and shrinking die size. TACs can be formed within barrier structures, which preserves a dielectric stack region within a memory stack for ease of etching the openings of the TACs. However, the regions enclosed by the barrier structures take up large area in the core array region where memory strings can be formed and also have a negative impact on the resistance of word lines. Moreover, the existing fabrication processes for forming the barrier structures become more challenging for the next-generation 3D memory devices (e.g., having 128 levels or more), which have less process margin.

Atty. Dkt. No. 10018-01-0015-US-DIV2

[0031] Various embodiments in accordance with the present disclosure provide a 3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures. For example, by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost. More process margin can also be obtained due to the elimination of etching and alignment steps for making the barrier structures, which enables high process extendibility for both current and future generations of 3D memory devices. Moreover, various embodiments of methods for forming the 3D memory device disclosed herein can allow TACs to be formed in the same fabrication process(es) for making other structures (e.g., peripheral contacts and/or dummy channel structures) and thus, further simplify the fabrication flow and reduce process cost.

[0032] FIG. 1 illustrates a cross-section of an exemplary 3D memory device 100, according to some embodiments of the present disclosure. 3D memory device 100 can include a substrate 102, which can include silicon (e.g., single crystalline silicon), silicon germanium (SiGe), gallium arsenide (GaAs), germanium (Ge), silicon on insulator (SOI), or any other suitable materials. In some embodiments, substrate 102 is a thinned substrate (e.g., a semiconductor layer), which was thinned from a normal thickness by grinding, wet/dry etching, chemical mechanical polishing (CMP), or any combination thereof.

[0033] 3D memory device 100 can include a memory stack 104 above substrate 102. Memory stack 104 can be a stacked storage structure through which memory strings (e.g., NAND memory strings 106) are formed. In some embodiments, memory stack 104 includes a plurality of conductor/dielectric layer pairs stacked vertically above substrate 102. Each conductor/dielectric layer pair can include a conductor layer 110 and a dielectric layer 112. That is, memory stack 104 can include interleaved conductor layers 110 and dielectric layers 112 stacked vertically. As shown in FIG. 1, each NAND memory string 106 extends vertically through interleaved conductor layers 110 and dielectric layers 112 in memory stack 104. In some embodiments, 3D memory device 100 is a NAND Flash memory device in which memory cells are provided at intersections of NAND memory strings 106 and conductor layers 110 (functioning as word lines) of 3D memory device 100. The number of conductor/dielectric layer pairs in memory stack

104 (e.g., 32, 64, 96, or 128) can set the number of memory cells in 3D memory device 100.

[0034] Conductor layers 110 can each have the same thickness or have different thicknesses. Similarly, dielectric layers 112 can each have the same thickness or have different thicknesses. Conductor layers 110 can include conductive materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), polycrystalline silicon (polysilicon), doped silicon, silicides, or any combination thereof. Dielectric layers 112 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In some embodiments, conductor layers 110 include metals, such as W, and dielectric layers 112 include silicon oxide. It is understood that a silicon oxide film (not shown), such as an in-situ steam generation (ISSG) silicon oxide, is formed between substrate 102 (e.g., a silicon substrate) and memory stack 104, according to some embodiments.

[0035] It is noted that x , y , and z axes are added to FIG. 1 to further illustrate the spatial relationship of the components in 3D memory device 100. The x -, y -, and z -directions are perpendicular to one another. Substrate 102 includes two lateral surfaces (e.g., a top surface and a bottom surface) extending laterally in the x -direction and y -direction (the lateral direction) in the x - y plane. As used herein, whether one component (e.g., a layer or a device) is “on,” “above,” or “below” another component (e.g., a layer or a device) of a semiconductor device (e.g., 3D memory device 100) is determined relative to the substrate (e.g., substrate 102) of the semiconductor device in the z -direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z -direction. The same notion for describing spatial relationship is applied throughout the present disclosure.

[0036] In some embodiments, 3D memory device 100 is part of a monolithic 3D memory device, in which the components of the monolithic 3D memory device (e.g., memory cells and peripheral devices) are formed on a single substrate (e.g., substrate 102). Peripheral devices 111, such as any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 100, can be formed on substrate 102 as well, outside of memory stack 104. Peripheral device 111 can be formed “on” substrate 102, where the entirety or part of peripheral device 111 is formed in substrate 102 (e.g., below the top surface of substrate 102) and/or directly on

substrate 102. Peripheral device 111 can include one or more of a page buffer, a decoder (e.g., a row decoder and a column decoder), a sense amplifier, a driver, a charge pump, a current or voltage reference, or any active or passive components of the circuits (e.g., transistors, diodes, resistors, or capacitors). Isolation regions (e.g., shallow trench isolations (STIs)) and doped regions (e.g., source regions and drain regions of the transistors) can be formed in substrate 102 as well, outside of memory stack 104.

[0037] As shown in FIG. 1, memory stack 104 can include an inner region 116 (also known as a “core array region”) and an outer region 118 (also known as a “staircase region”). In some embodiments, inner region 116 is the center region of memory stack 104 where an array of NAND memory strings 106 are formed through the conductor/dielectric layer pairs, and outer region 118 is the remaining region of memory stack 104 surrounding inner region 116 (including the sides and edges) without NAND memory strings 106.

[0038] As shown in FIG. 1, each NAND memory string 106 can include a channel structure 108 extending vertically through the conductor/dielectric layer pairs in inner region 116 of memory stack 104. Channel structure 108 can include a channel hole filled with semiconductor materials (e.g., forming a semiconductor channel) and dielectric materials (e.g., forming a memory film). In some embodiments, the semiconductor channel includes silicon, such as amorphous silicon, polysilicon, or single crystalline silicon. In some embodiments, the memory film is a composite layer including a tunneling layer, a storage layer (also known as a “charge trap/storage layer”), and a blocking layer. Each NAND memory string 106 can have a cylinder shape (e.g., a pillar shape). The semiconductor channel, tunneling layer, storage layer, and blocking layer are arranged along a direction from the center toward the outer surface of the pillar in this order, according to some embodiments. The tunneling layer can include silicon oxide, silicon oxynitride, or any combination thereof. The storage layer can include silicon nitride, silicon oxynitride, silicon, or any combination thereof. The blocking layer can include silicon oxide, silicon oxynitride, high dielectric constant (high-k) dielectrics, or any combination thereof.

[0039] In some embodiments, NAND memory strings 106 include a plurality of control gates (each being part of a word line/conductor layer 110) for NAND memory strings 106. Conductor layer 110 in each conductor/dielectric layer pair can function as a control

gate for memory cells of NAND memory string 106. Conductor layer 110 can include multiple control gates for multiple NAND memory strings 106 and can extend laterally as a word line ending in outer region 118 of memory stack 104.

[0040] In some embodiments, NAND memory string 106 includes two plugs 117 and 119 at a respective end in the vertical direction. Each plug 117 or 119 can be in contact with a respective end of channel structure 108. Plug 117 can include a semiconductor material, such as silicon, that is epitaxially grown from substrate 102. Plug 117 can function as the channel controlled by a source select gate of NAND memory string 106. Plug 117 can be at the lower end of NAND memory string 106 and in contact with channel structure 108 (e.g., on the upper end of channel structure 108). As used herein, the “upper end” of a component (e.g., NAND memory string 106) is the end farther away from substrate 102 in the *z*-direction, and the “lower end” of the component (e.g., NAND memory string 106) is the end closer to substrate 102 in the *z*-direction when substrate 102 is positioned in the lowest plane of 3D memory device 100.

[0041] Plug 119 can include semiconductor materials (e.g., polysilicon) or conductor materials (e.g., metals). In some embodiments, plug 119 includes an opening filled with titanium/titanium nitride (Ti/TiN as a barrier layer) and tungsten (as a conductor). By covering the upper end of channel structure 108 during the fabrication of 3D memory device 100, plug 119 can function as an etch stop layer to prevent etching of dielectrics filled in channel structure 108, such as silicon oxide and silicon nitride. In some embodiments, plug 119 functions as the drain of NAND memory string 106.

[0042] In some embodiments, memory stack 104 includes a lower memory deck 120 disposed on substrate 102 and an upper memory deck 122 disposed above lower memory deck 120. A joint layer 124 can be disposed vertically between and electrically isolate lower memory deck 120 and upper memory deck 122. Each of lower and upper memory deck 120 and 122 can have the same or different number of conductor/dielectric layer pairs. Joint layer 124 can include dielectrics, such as silicon oxide. By separating memory stack 104 into lower and upper memory decks 120 and 122, or even more memory decks in some embodiments, channel structure 108 of NAND memory string 106 can be jointed by multiple channel structures, each of which is separately formed through a respective memory deck, to increase process yield. As shown in FIG. 1, channel structure 108 of NAND memory string 106 includes a lower channel structure 126

extending vertically through lower memory deck 120 and an upper channel structure 128 extending vertically through upper memory deck. In some embodiments, an inter-deck plug 130 is disposed vertically between and in contact with lower channel structure 126 and upper channel structure 128. Inter-deck plug 130 can include semiconductor materials, such as polysilicon, and joint (e.g., electrically connect) lower and upper channel structures 126 and 128 to form channel structure 108. That is, NAND memory string 106 can include plug 117, lower channel structure 126, inter-deck plug 130, upper channel structure 128, and plug 119 from bottom to top in this order.

[0043] In some embodiments, 3D memory device 100 further includes slit structures 132. Each slit structure 132 can extend vertically through the conductor/dielectric layer pairs in memory stack 104. Slit structure 132 can also extend laterally (e.g., in the y-direction) to separate memory stack 104 into multiple blocks. Slit structure 132 can include an opening (slit) filled with conductive materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), silicides, or any combination thereof. Slit structure 132 can further include a spacer having dielectric materials, such as silicon oxide, laterally between the filled conductive materials and memory stack 104 to electrically insulate the filled conductive materials from surrounding conductor layers 110 in memory stack 104. As a result, slit structures 132 can separate 3D memory device 100 into multiple memory blocks and/or memory fingers.

[0044] In some embodiments, slit structure 132 functions as the source contact for NAND memory strings 106 in the same memory block or the same memory finger that share the same array common source. Slit structure 132 can thus be referred to as a “common source contact” of multiple NAND memory strings 106. In some embodiments, substrate 102 includes a doped region 134 (including p-type or n-type dopants at a desired doping level), and the lower end of slit structure 132 is in contact with doped region 134 of substrate 102. Slit structure 132 thus can electrically connect to NAND memory strings 106 by doped region 134.

[0045] As shown in FIG. 1, 3D memory device 100 further includes TACs 136 each extending vertically through the conductor/dielectric layer pairs in memory stack 104. Each TAC 136 can extend vertically through interleaved conductor layers 110 and dielectric layers 112. In some embodiments, TAC 136 can extend through the entire thickness of memory stack 104, (e.g., all the conductor/dielectric layer pairs in the

vertical direction). In some embodiments, TAC 136 further extends through at least part of substrate 102. TAC 136 can carry electrical signals from and/or to 3D memory device 100, such as part of the power bus, with shorten interconnect routing. In some embodiments, TAC 136 can provide electrical connections between 3D memory device 100 and peripheral device 111 and/or between back-end-of-line (BEOL) interconnects (not shown) and peripheral device 111. TAC 136 can also provide mechanical support to memory stack 104.

[0046] TAC 136 can include a vertical opening through memory stack 104 and that is filled with filling materials. In some embodiments, TAC 136 includes a spacer 138 on a sidewall of the opening and a conductor layer 140 in contact with spacer 138 in the opening. Conductor layer 140 can include conductive materials, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Spacer 138 can electrically insulate conductor layer 140 of TAC 136 from surrounding conductor layers 110 in memory stack 104. In some embodiments, TAC 136 has a substantially circular shape in the plan view, and conductor layer 140 and spacer 138 are disposed radially from the center of TAC 136 in this order. Spacer 138 of TAC 136 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

[0047] As shown in FIG. 1, at least on one side in the lateral direction (e.g., in the y-direction), outer region 118 of memory stack 104 can include a staircase structure 142. In some embodiments, another staircase structure (not shown) is disposed on the opposite side of memory stack 104 in the y-direction. Each “level” of staircase structure 142 can include one or more conductor/dielectric layer pairs, each including conductor layer 110 and dielectric layer 112. The top layer in each level of staircase structure 142 can be conductor layer 110 for interconnection in the vertical direction. In some embodiments, each two adjacent levels of staircase structure 142 are offset by a nominally same distance in the vertical direction and a nominally same distance in the lateral direction. For each two adjacent levels of staircase structure 142, the first level (and conductor layer and dielectric layer therein) that is closer to substrate 102 can extend laterally further than the second level (and conductor layer and dielectric layer therein), thereby forming a “landing area” on the first level for interconnection in the vertical direction.

[0048] Staircase structure 142 can be used for landing word line contacts 144 and/or for balancing load in certain processes during fabrication (e.g., etching and chemical mechanical polishing (CMP)) by dummy channel structures 146 therethrough. The lower end of each word line contact 144 can be in contact with top conductor layer 110 (word line) in a respective level of staircase structure 142 to individually address a corresponding word line of 3D memory device 100. Word line contact 144 can include an opening (e.g., a via hole or a trench) extending vertical through one or more dielectric layers and filled with conductive materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof.

[0049] Dummy channel structure 146 can extend vertically through memory stack 104 and have a vertical opening filled with the same materials as those in channel structure 108. Different from channel structures 108, a contact is not formed on dummy channel structure 146 to provide electrical connections with other components of 3D memory device 100, according to some embodiments. In some embodiments, dummy channel structure 146 is fully filled with dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. Thus, dummy channel structures 146 cannot be used for forming memory cells in 3D memory device 100. Instead, dummy channel structures 146 can provide mechanical support to the memory array structures, e.g., memory stack 104. Although dummy channel structures 146 are disposed in outer region 118 of memory stack 104 as shown in FIG. 1, it is understood that dummy channel structures 146 can be formed in inner region 116 of memory stack 104 as well. In some embodiments, dummy channel structure 146 is fully filled with a dielectric layer, such as a silicon oxide layer, and extends vertically through the conductor/dielectric layer pairs in memory stack 104, either in inner region 116 or in outer region 118.

[0050] As shown in FIG. 1, 3D memory device 100 can further include peripheral contacts 148 extending vertically through one or more dielectric layers and in contact with peripheral devices 111 outside of memory stack 104. Peripheral contact 148 can provide electrical connections with peripheral devices 111. Peripheral contact 148 can include a vertical opening filled with filling materials. In some embodiments, similar to TAC 136, peripheral contact 148 includes a spacer 150 on a sidewall of the opening and a conductor layer 152 in contact with spacer 150 in the opening. Conductor layer 152 can

include conductive materials, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. In some embodiments, peripheral contact 148 has a substantially circular shape in the plan view, and conductor layer 152 and spacer 150 are disposed radially from the center of peripheral contact 148 in this order. Spacer 150 of peripheral contact 148 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In some embodiments, spacer 150 of peripheral contact 148 and spacer 138 of TAC 136 have nominally the same thickness in the lateral direction (e.g., radial direction). In some embodiments, both spacer 150 of peripheral contact 148 and spacer 138 of TAC 136 include silicon oxide.

[0051] It is understood that 3D memory device 100 can include additional components and structures not shown in FIG. 1 including, but not limited to, other local contacts and interconnects in one or more BEOL interconnect layers above memory stack 104 and/or below substrate 102.

[0052] FIGs. 2A–2E illustrate an exemplary fabrication process for forming channel structures of a 3D memory device, according to some embodiments of the present disclosure. FIGs. 3A–3F illustrate exemplary fabrication processes for forming TACs, peripheral contacts, and dummy channel structures of a 3D memory device, according to various embodiments of the present disclosure. FIGs. 4A–4C illustrate another exemplary fabrication process for forming TACs, peripheral contacts, and dummy channel structures of a 3D memory device, according to some embodiments of the present disclosure. FIGs. 5A–5B illustrate an exemplary fabrication process for forming a slit structure and word line contacts of a 3D memory device, according to some embodiments of the present disclosure. FIG. 6 is a flowchart of an exemplary method 600 for forming a 3D memory device, according to some embodiments. FIG. 8 is a flowchart of another exemplary method 800 for forming a 3D memory device, according to some embodiments of the present disclosure. Examples of the 3D memory device depicted in FIGs. 2-6 and 8 include 3D memory device 100 depicted in FIG. 1. FIGs. 2-6 and 8 will be described together. It is understood that the operations shown in methods 600 and 800 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. Further, some of the operations may be performed simultaneously, or in a different order than shown in FIGs. 6 and 8.

[0053] Referring to FIG. 6, method 600 starts at operation 602, in which a dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. The substrate can be a silicon substrate. In some embodiments, a lower dielectric deck is formed first, followed by the formation of a joint layer. An upper dielectric deck can then be formed on the joint layer to form the dielectric stack. Method 600 proceeds to operation 604, as illustrated in FIG. 6, in which a channel structure extending vertically through the dielectric stack is formed. In some embodiments, a lower channel structure extending vertically through the lower dielectric deck is formed. An inter-deck plug can then be formed on the lower channel structure in the joint layer. Once the upper dielectric deck is formed, an upper channel structure extending vertically through the upper dielectric deck can be formed and jointed with the lower channel structure by the inter-deck plug, thereby forming the channel structure. In some embodiments, a staircase structure is formed at one side of the dielectric stack.

[0054] As illustrated in FIG. 2A, a lower dielectric deck 204 including a plurality of dielectric/sacrificial layer pairs is formed on a silicon substrate 202. In some embodiments, sacrificial layers 206 and dielectric layers 208 are alternately deposited by one or more thin film deposition processes including, but not limited to, physical vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), or any combination thereof. In some embodiments, sacrificial layers 206 include silicon nitride, and dielectric layers 208 include silicon oxide. It is understood that the sequence of depositing sacrificial layers 206 and dielectric layers 208 is not limited. The deposition can start with sacrificial layer 206 or dielectric layer 208 and can end with sacrificial layer 206 or dielectric layer 208.

[0055] As illustrated in FIG. 2B, an array of lower channel structures 210 are formed, each of which extends vertically through interleaved sacrificial layers 206 and dielectric layers 208 in lower dielectric deck 204. In some embodiments, fabrication processes to form lower channel structure 210 include forming a channel hole through interleaved sacrificial layers 206 and dielectric layers 208 in lower dielectric deck 204 using dry etching/and or wet etching, such as deep reactive-ion etching (DRIE), followed by filling the channel hole with a plurality of layers, such as a dielectric layer and a semiconductor layer, using thin film deposition processes. In some embodiments, the dielectric layer is a composite dielectric layer, such as a combination of multiple dielectric layers including,

but not limited to, a tunneling layer, a storage layer, and a blocking layer. The tunneling layer can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. The storage layer can include materials for storing charge for memory operation. The storage layer materials can include, but not limited to, silicon nitride, silicon oxynitride, a combination of silicon oxide and silicon nitride, or any combination thereof. The blocking layer can include dielectric materials including, but not limited to, silicon oxide or a combination of silicon oxide/silicon oxynitride/silicon oxide (ONO). The blocking layer can further include a high-k dielectric layer, such as an aluminum oxide (Al_2O_3) layer. The semiconductor layer can include polysilicon, serving as a semiconductor channel. The semiconductor layer and dielectric layer can be formed by processes such as ALD, CVD, PVD, or any combination thereof.

[0056] As illustrated in FIG. 2B, a joint layer 212 is formed on lower dielectric deck 204 by depositing a dielectric layer, such as a silicon oxide layer, using thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof. An array of inter-deck plugs 214 are formed in joint layer 212 and in contact with array of lower channel structures 210, respectively. Inter-deck plugs 214 can be formed by patterning and etching openings through joint layer 212, followed by deposition of semiconductor materials, such as polysilicon, using thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof.

[0057] As illustrated in FIG. 2C, an upper dielectric deck 216 is formed on joint layer 212 and above lower dielectric deck 204. A dielectric stack 218 including lower dielectric deck 204 and upper dielectric deck 216 can thus be formed. The same fabrication processes for forming lower dielectric deck 204 can be used for forming upper dielectric deck 216 and thus, are not repeated again.

[0058] As illustrated in FIG. 2D, an array of upper channel structures 220 each extending vertically through upper dielectric deck 216 are formed and in contact with array of inter-deck plugs 214, respectively. An array of channel structures 222 each including lower channel structure 210 and upper channel structure 220 that are electrically connected by inter-deck plug 214 are thus formed. The same fabrication processes for forming lower channel structures 210 can be used for forming upper channel structures 220 and thus, are not repeated.

[0059] As illustrated in FIG. 2E, staircase structures 224 are formed on the sides of dielectric stack 218. Staircase structure 224 can be formed by the so-called “trim-etch” processes, which, in each cycle, trim (e.g., etching incrementally and inwardly, often from all directions) a patterned photoresist layer, followed by etching the exposed portions of the dielectric/sacrificial layer pair using the trimmed photoresist layer as an etch mask to form one step of staircase structure 224.

[0060] Method 600 proceeds to operation 606, as illustrated in FIG 6, in which a dummy channel structure extending vertically through the dielectric stack is formed. As illustrated in FIG. 3A, an array of dummy channel structures 302 are formed through dielectric layer 218. Dummy channel structure 302 can be formed by first etching an opening through dielectric stack 218 and/or one or more dielectric layers using wet etching and/or dry etching, such as DRIE. In some embodiments, the opening is then fully filled with a dielectric layer, such as a silicon oxide layer, using one or more thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof. In some embodiments, dummy channel structures 302 are formed simultaneously with channel structures 222 in the same fabrication steps, such that the opening of each dummy channel structure 302 is filled with at least some of the materials filling in channel structures 222.

[0061] Method 600 proceeds to operation 608, as illustrated in FIG 6, in which a first opening through the dielectric stack and a second opening outside of the dielectric stack are simultaneously etched. As illustrated in FIG. 3B, first openings (TAC holes) 304 each extending vertically through the dielectric/sacrificial layer pairs in dielectric stack 218 are formed by wet etching and/or drying etching of interleaved dielectric layers 208 and sacrificial layers 206 (e.g., silicon nitride and silicon oxide). In some embodiments, TAC holes 304 are etched using DRIE. Second openings (peripheral contact holes) 306 can be simultaneously formed by the same wet etching and/or drying etching process, such as DRIE, to etch through one or more dielectric layers (e.g., silicon oxide and/or silicon nitride) outside of dielectric stack 218. The depths of TAC hole 304 and peripheral contact hole 306 in the vertical direction can be nominally the same. The lateral dimensions of TAC hole 304 and peripheral contact hole 306, such as the diameters, can be nominally the same or different in various embodiments. For example,

the diameter of TAC hole 304 is greater than the diameter of peripheral contact hole 306, according to some embodiments.

[0062] As shown in FIG. 3B, TAC hole 304 and peripheral contact hole 306 can reach to silicon substrate 202, and the lower end of peripheral contact hole 306 can be in contact with a peripheral device 307 formed on silicon substrate 202. In some embodiments, peripheral device 307 includes transistors, which can be formed by a plurality of processes including, but not limited to, photolithography, dry/wet etch, thin film deposition, thermal growth, implantation, CMP, and any other suitable processes. In some embodiments, doped regions are formed in silicon substrate 202 by ion implantation and/or thermal diffusion, which function, for example, as source regions and/or drain regions of the transistors. In some embodiments, isolation regions (e.g., STIs) are also formed in silicon substrate 202 by wet etching and/or dry etching and thin film deposition processes. The fabrication process for forming peripheral device 307 can occur at any fabrication stage prior to the etching of peripheral contact hole 306.

[0063] Method 600 proceeds to operation 610, as illustrated in FIG 6, in which a first spacer and a second spacer are simultaneously formed on sidewalls of the first opening and the second opening, respectively. FIG. 7A is a flowchart of an exemplary method for forming a spacer on a sidewall of an opening, according to some embodiments. Referring to FIG. 7A, at operation 702, to form the first spacer, a dielectric layer is deposited on the sidewall and bottom surface of the first opening. At operation 704, part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The deposition of the dielectric layer can include ALD, and the removal of the part of the dielectric layer can include anisotropic etching on the bottom surface of the first opening.

[0064] As illustrated in FIG. 3C, a first spacer 308 is formed on the sidewall, but not the bottom surface, of TAC hole 304. A dielectric layer can be first deposited into TAC hole 304 using one or more thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof, which covers the sidewall and bottom surface of TAC hole 304. The part of the dielectric layer deposited on the bottom surface, but not on the sidewall, of TAC hole 304 can then be etched through using “bottom punch” processes. In some embodiments, a silicon oxide layer can be deposited on the sidewall and bottom surface of TAC hole 304 using ALD, and the part of the silicon oxide layer deposited on the bottom surface of TAC hole 304 can be removed using any suitable anisotropic etching

directed to the bottom surface of TAC hole 304. In one example, a bias with a sufficient voltage level may be added to DRIE to etch through the silicon oxide layer on the bottom surface, but not through the sidewall, of TAC hole 304. Second spacer 310 can be simultaneously formed on the sidewall, but not the bottom surface, of peripheral contact hole 306, using the same deposition and bottom punch processes. In some embodiments, the thicknesses of first spacer 308 and second spacer 310 are nominally the same in the lateral direction (e.g., radial direction).

[0065] FIG. 7B is a flowchart of another exemplary method for forming a spacer on a sidewall of an opening, according to some embodiments. Referring to FIG. 7B, at operation 706, to form the first spacer on the sidewall of the first opening, a plurality of shallow recesses are first formed by removing parts of the sacrificial layers abutting the sidewall of the first opening. At operation 708, a dielectric layer is deposited filling in the shallow recesses and on the sidewall and a bottom surface of the first opening. At operation 710, part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The removal of the part of the dielectric layer includes isotropic etching on the sidewall and the bottom surface of the first opening, according to some embodiments.

[0066] Different from the example illustrated in FIG. 3C in which first spacer 308 is formed by ALD deposition and bottom punch processes, FIGs. 3D-3E illustrate another example in which a first spacer 314 is formed by any deposition process, followed by an etch-back process. As illustrated in FIG. 3D, parts of sacrificial layers 206 in dielectric stack 218 that abut the sidewall of TAC hole 304 are removed by wet etching and/or dry etching, such as using a wet etchant for silicon nitride. A plurality of shallow recesses 312 can then be formed along the sidewall of TAC hole 304. The degree of the etching, i.e., the lateral dimension of shallow recess, can be controlled by the etching rate and/or etching time. The sacrificial layer partial removal process can provide space for a thicker dielectric layer deposition in the next step.

[0067] As illustrated in FIG. 3E, a first spacer 314 is formed on the sidewall, but not the bottom surface, of TAC hole 304. A dielectric layer can be first deposited into TAC hole 304 using one or more thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof, which fills in shallow recesses 312 (as shown in FIG. 3D) and covers the sidewall and bottom surface of TAC hole 304. The part of the dielectric layer

deposited on the bottom surface of TAC hole 304 can be then removed using etch-back processes. In some embodiments, isotropic etching can be applied to etch the dielectric layer deposited on both the sidewall and the bottom surface of TAC hole 304. Because the dielectric layer is substantially thicker along the sidewall (filling in shallow recesses 312) than on the bottom surface, when the part of the dielectric layer on the bottom surface has been etched through, the part of the dielectric layer on the sidewall can be partially etched, leaving first spacer 314 covering only the sidewall of TAC hole 304. In other words, the thickened dielectric layer along the sidewall is etched-back, leaving a thinner dielectric layer as first spacer 314, according to some embodiments. The etching rate and/or etching time of any suitable isotropic etching process can be controlled to fully etch through the dielectric layer on the bottom surface of TAC hole 304, but partially etch back the dielectric layer on the sidewall of TAC hole 304.

[0068] Method 600 proceeds to operation 612, as illustrated in FIG 6, in which a conductor layer is deposited in the first opening to form a TAC and in the second opening to form a peripheral contact. In some embodiments, the conductor layer is a composite layer including an adhesion/barrier layer and a conductor. As illustrated in FIG. 3F, a conductor layer 316 is deposited in TAC hole 304 (as shown in FIGs. 3C-3E) to fill the remaining space of TAC hole 304, thereby forming a TAC 318 extending vertically through dielectric stack 218. In some embodiments, an adhesion/barrier layer is first formed along first spacer 308/314 by depositing titanium/titanium nitride (Ti/TiN) or titanium/tantalum nitride (Ta/TaN) using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination thereof. A conductor can then be formed in the remaining space of TAC hole 304 by depositing metals, such as tungsten, using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination thereof. A conductor layer 320 can be simultaneously formed in peripheral contact hole 306 (as shown in FIGs. 3C-3E) to form a peripheral contact 322 in contact with peripheral device 307, using the same deposition processes. The excess conductor layer after deposition can be removed by CMP.

[0069] Method 600 proceeds to operation 614, as illustrated in FIG 6, in which a slit extending vertically through the dielectric stack is formed after the formation of the TAC. Method 600 proceeds to operation 616, as illustrated in FIG 6, in which a memory stack

including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers. In some embodiments, a slit structure is formed by depositing a conductor layer in the slit after the formation of the memory stack. In some embodiments, a plurality of word line contacts each in contact with a respective one of the conductor layers of the conductor/dielectric layer pairs in the staircase structure are formed.

[0070] As illustrated in FIG. 5A, an opening (slit) can be etched through the dielectric/sacrificial layer pairs in dielectric stack 218 (as shown in FIGs. 3-4). The slit can be formed by wet etching and/or dry etching of dielectrics (e.g., silicon oxide and silicon nitride). The opening can be used as the pathway for gate replacement processes that replace sacrificial layers 206 in dielectric stack 218 with conductor layers 502 to form a plurality of conductor/dielectric layer pairs. The replacement of sacrificial layers 206 with conductor layers 502 can be performed by wet etching sacrificial layers 206 (e.g., silicon nitride) selective to dielectric layers 208 (e.g., silicon oxide) and filling the structure with conductor layers 502 (e.g., W). Conductor layers 502 can be deposited by PVD, CVD, ALD, electrochemical depositions, or any combination thereof. Conductor layers 502 can include conductive materials including, but not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. As a result, after the gate replacement processes, dielectric stack 218 in FIGs. 3-4 becomes memory stack 504 including the conductor/dielectric layer pairs, i.e., interleaved conductor layers 502 and dielectric layers 208, on silicon substrate 202.

[0071] As illustrated in FIG. 5A, a slit structure 506 is formed by filling (e.g., depositing) conductive materials into the slit by PVD, CVD, ALD, electrochemical depositions, or any combination thereof. Slit structure 506 can include conductive materials including, but not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. In some embodiments, a dielectric layer (e.g., a silicon oxide layer) is formed first between the conductive materials of slit structure 506 and conductor layers 502 surrounding slit structure 506 as a spacer. The lower end of slit structure 506 can be in contact with a doped region 507, which can be formed in silicon substrate 202 using ion implantation and/or thermal diffusion.

[0072] As illustrated in FIG. 5B, each word line contact 508 is in contact with a respective one of conductor layers 502 of the conductor/dielectric layer pairs in staircase structure 224. Word line contacts 508 are formed through one or more dielectric layers by first etching vertical openings (e.g., by wet etching and/or dry etching), followed by filling the openings with conductive materials using ALD, CVD, PVD, electrochemical depositions, or any combination thereof. In some embodiments, other conductive materials are filled in the openings to function as an adhesion/barrier layer. Etching of dielectric layers to form the openings of word line contacts 508 can be controlled by etch stop at a different material. For example, etching of dielectric layers can be stopped when reaching to conductor layers 502 in staircase structure 224.

[0073] FIG. 8 is a flowchart of another exemplary method 800 for forming a 3D memory device, according to some embodiments of the present disclosure. Operations 802, 804, 814, and 816 are similar to operations 602, 604, 614, and 616, respectively, and thus are not repeated. Method 800 proceeds to operation 806, as illustrated in FIG 8, in which a first opening through the dielectric stack, a second opening outside of the dielectric stack, and a third opening through the dielectric stack are simultaneously etched. In some embodiments, the lateral dimension (e.g., diameter) of the third opening is smaller than lateral dimensions of the first and second openings. Each of the first, second, and third openings has a nominally circular shape in the plan view, according to some embodiments.

[0074] As illustrated in FIG. 4A, a first opening (TAC hole) 402, a second opening (peripheral contact hole) 404, and a third opening (dummy channel hole) 406 are simultaneously formed, each of which reaches to silicon substrate 202. The lower end of peripheral contact hole 404 can be in contact with a peripheral device 405 formed on silicon substrate 202. TAC hole 402 and dummy channel hole 406 can be etched through interleaved sacrificial layers 206 and dielectric layers 208 (e.g., silicon nitride and silicon oxide) in dielectric stack 218 using wet etching and/or dry etching, and peripheral contact hole 404 can be simultaneously etched through one or more dielectric layers (e.g., silicon oxide) using the same wet etching and/or dry etching process. In some embodiments, TAC hole 402, peripheral contact hole 404, and dummy channel hole 406 are etched using DRIE at the same time. The depths of TAC hole 402, peripheral contact hole 404, and dummy channel hole 406 in the vertical direction can be nominally the same. In

some embodiments, each of TAC hole 402, peripheral contact hole 404, and dummy channel hole 406 has a substantially circular shape in the plan view. The lateral dimensions (e.g., diameters) of TAC hole 402, peripheral contact hole 404, and dummy channel hole 406 can be controlled by patterning process and/or etching parameters, such as etching rate and etching time. In some embodiments, in the plan view, the diameter of dummy channel hole 406 is smaller than the diameter of TAC hole 402 and the diameter of peripheral contact hole 404. In some embodiments, the diameter of peripheral contact hole 404 is smaller than the diameter of TAC hole 402 in the plan view.

[0075] Method 800 proceeds to operation 808, as illustrated in FIG 8, in which a dielectric layer is deposited (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening. Method 800 proceeds to operation 810, as illustrated in FIG 8, in which parts of the dielectric layer deposited on the bottom surfaces of the first and second openings are removed.

[0076] As illustrated in FIG. 4B, a dielectric layer (e.g., silicon oxide) is deposited into TAC hole 402, peripheral contact hole 404, and dummy channel hole 406 using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination thereof. Due to the different lateral dimensions of TAC hole 402, peripheral contact hole 404, and dummy channel hole 406, by controlling the deposition parameters, such as the deposition rate and/or deposition time, the deposited dielectric layer can fully fill in dummy channel hole 406 to form a dummy channel structure 408, but only partially fill in TAC hole 402 and peripheral contact hole 404 to form a first spacer 410 and a second spacer 412, respectively, on the sidewalls of TAC hole 402 and peripheral contact hole 404. Dummy channel structure 408 is thus formed extending vertically through dielectric stack 218. As described above, parts of the dielectric layer deposited on the bottom surfaces of TAC hole 402 and peripheral contact hole 404 can be removed (i.e., etched through) using the bottom punch process, such as high bias DRIE. As a result, first and second spacers 410 and 412 are formed on the sidewalls, but not the bottom surfaces, of TAC hole 402 and peripheral contact hole 404, respectively. In some embodiments, the simultaneously formed first and second spacers 410 and 412 have nominally the same thickness in the radial direction in the plan view.

[0077] Method 800 proceeds to operation 812, as illustrated in FIG 8, in which a conductor layer is deposited (i) filling in the first opening to form a TAC and (ii) filling in

the second opening to form a peripheral contact. As illustrated in FIG. 4C, a conductor layer 414 is deposited in TAC hole 402 (as shown in FIG. 4B) to fill the remaining space of TAC hole 402, thereby forming a TAC 416 extending vertically through dielectric stack 218. In some embodiments, an adhesion/barrier layer is first formed along first spacer 410 by depositing Ti/TiN or Ta/TaN using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination thereof. A conductor can then be formed in the remaining space of TAC hole 402 by depositing metals, such as tungsten, using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination thereof. A conductor layer 418 can be simultaneously formed in peripheral contact hole 404 (as shown in FIG. 4B) to form a peripheral contact 420 in contact with peripheral device 405, using the same deposition processes. The excess conductor layer after deposition can be removed by CMP.

[0078] According to one aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A first opening extending vertically through the dielectric stack is formed. A spacer is formed on a sidewall of the first opening. A TAC extending vertically through the dielectric stack is formed by depositing a conductor layer in contact with the spacer in the first opening. A slit extending vertically through the dielectric stack is formed after forming the TAC. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0079] In some embodiments, a staircase structure is formed at one edge of the dielectric stack prior to forming the first opening. A plurality of word line contacts each in contact with a respective one of the conductor layers of the conductor/dielectric layer pairs in the staircase structure are formed, according to some embodiments.

[0080] In some embodiments, a slit structure is formed by depositing a conductor layer in the slit.

[0081] In some embodiments, a dummy channel structure extending vertically through the dielectric stack is formed prior to forming the first opening.

- [0082] In some embodiments, to form the first opening, the first opening through the dielectric stack and a second opening outside of the dielectric stack are simultaneously etched. In some embodiments, to form the TAC, the conductor layer is deposited in the first opening to form the TAC and in the second opening to form a peripheral contact.
- [0083] In some embodiments, to form the spacer on the sidewall of first opening, a dielectric layer is deposited on the sidewall and a bottom surface of the first opening, and part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The deposition of the dielectric layer includes ALD, and the removal of the part of the dielectric layer includes anisotropic etching on the bottom surface of the first opening, according to some embodiments.
- [0084] In some embodiments, to form the spacer on the sidewall of first opening, a plurality of shallow recesses are formed by removing parts of the sacrificial layers abut the sidewall of the first opening, a dielectric layer is deposited filling in the shallow recesses and on the sidewall and a bottom surface of the first opening, and part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The removal of the part of the dielectric layer includes isotropic etching on the sidewall and the bottom surface of the first opening, according to some embodiments.
- [0085] In some embodiments, to form the first opening, the first opening through the dielectric stack, a second opening outside of the dielectric stack, and a third opening through the dielectric stack are simultaneously etched. A lateral dimension of the third opening can be smaller than lateral dimensions of the first and second openings.
- [0086] In some embodiments, to form the spacer on the sidewall of the first opening, a dielectric layer is deposited (i) fully filling in the third opening to form a dummy channel structure and (2) partially filling in the first opening and the second opening, and parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening are removed. Each of the first, second, and third openings can have a nominally circular shape in the plan view.
- [0087] In some embodiments, the dielectric layers in the dielectric/sacrificial layer pairs include silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs include silicon nitride, and the spacer includes silicon oxide.
- [0088] According to another aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of

dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A dummy channel structure extending vertically through the dielectric stack is formed. A first opening through the dielectric stack and a second opening outside of the dielectric stack are simultaneously etched. A first spacer on a sidewall of the first opening and a second spacer on a sidewall of the second opening are simultaneously formed. A conductor layer is deposited (i) filling in the first opening to form a TAC and (ii) filling in the second opening to form a peripheral contact. A slit extending vertically through the dielectric stack is formed after forming the TAC and peripheral device. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0089] In some embodiments, a staircase structure is formed at one edge of the dielectric stack prior to forming the dummy channel structure. A plurality of word line contacts each in contact with a respective one of the conductor layers of the conductor/dielectric layer pairs in the staircase structure are formed, according to some embodiments.

[0090] In some embodiments, a slit structure is formed by depositing a conductor layer in the slit.

[0091] In some embodiments, to form the first spacer on the sidewall of the first opening, a dielectric layer is deposited on the sidewall and a bottom surface of the first opening, and part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The deposition of the dielectric layer includes ALD, and the removal of the part of the dielectric layer includes anisotropic etching on the bottom surface of the first opening, according to some embodiments.

[0092] In some embodiments, to form the spacer on the sidewall of first opening, a plurality of shallow recesses are formed by removing parts of the sacrificial layers abutting the sidewall of the first opening, a dielectric layer is deposited filling in the shallow recesses and on the sidewall and a bottom surface of the first opening, and part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The removal of the part of the dielectric layer includes isotropic etching on the sidewall and the bottom surface of the first opening, according to some embodiments.

- [0093] In some embodiments, the dielectric layers in the dielectric/sacrificial layer pairs include silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs include silicon nitride, and the first and second spacers include silicon oxide.
- [0094] According to still another aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A first opening through the dielectric stack, a second opening outside of the dielectric stack, and a third opening through the dielectric stack are simultaneously etched. A lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings. A dielectric layer is deposited (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening. Parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening are removed. A conductor layer is deposited (i) filling in the first opening to form a TAC and (ii) filling in the second opening to form a peripheral contact. A slit extending vertically through the dielectric stack is formed after forming the TAC and peripheral device. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.
- [0095] In some embodiments, a staircase structure is formed at one edge of the dielectric stack prior to etching the first, second, and third openings. A plurality of word line contacts each in contact with a respective one of the conductor layers of the conductor/dielectric layer pairs in the staircase structure are formed, according to some embodiments.
- [0096] In some embodiments, a slit structure is formed by depositing a conductor layer in the slit.
- [0097] In some embodiments, each of the first, second, and third openings has a nominally circular shape in the plan view.
- [0098] In some embodiments, the dielectric layers in the dielectric/sacrificial layer pairs includes silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs includes silicon nitride, and the dielectric layer filling the first, second, and third openings include silicon oxide.

[0099] According to yet another aspect of the present disclosure, a 3D memory device includes a substrate, a memory stack on the substrate including a plurality of conductor/dielectric layer pairs, a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack, a TAC extending vertically through the conductor/dielectric layer pairs in the memory stack, and a dummy channel structure fully filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.

[0100] In some embodiments, the 3D memory device further includes a peripheral device on the substrate, and a peripheral contact outside of the memory stack and in contact with the peripheral device.

[0101] In some embodiments, each of the TAC and peripheral contact includes a spacer with a nominally same thickness. The dielectric layer in the dummy channel structure and the spacers in the TAC and peripheral contact include silicon oxide, according to some embodiments.

[0102] In some embodiments, the 3D memory device further includes a lower memory deck on the substrate and an upper memory deck above the lower memory stack. In some embodiments, the channel structure includes a lower channel structure extending vertically through the lower memory deck, an upper channel structure extending vertically through the upper memory deck, and an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.

[0103] In some embodiments, the 3D memory device further includes a staircase structure at one edge of the memory stack, and a plurality of word line contacts each in contact with a respective one of the conductor layers of the conductor/dielectric layer pairs in the staircase structure.

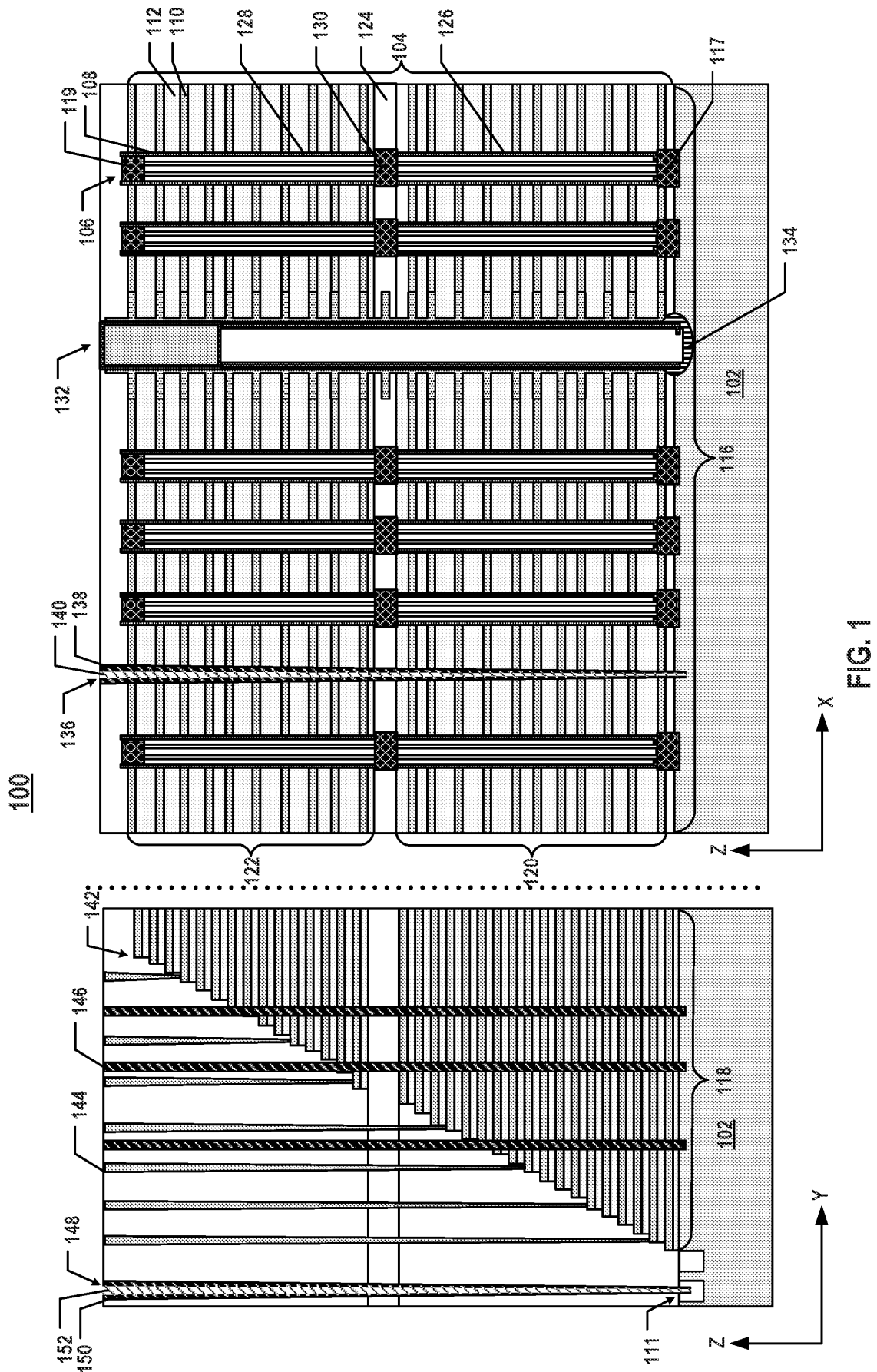
[0104] The foregoing description of the specific embodiments will so reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or

phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

[0105] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0106] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0107] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.



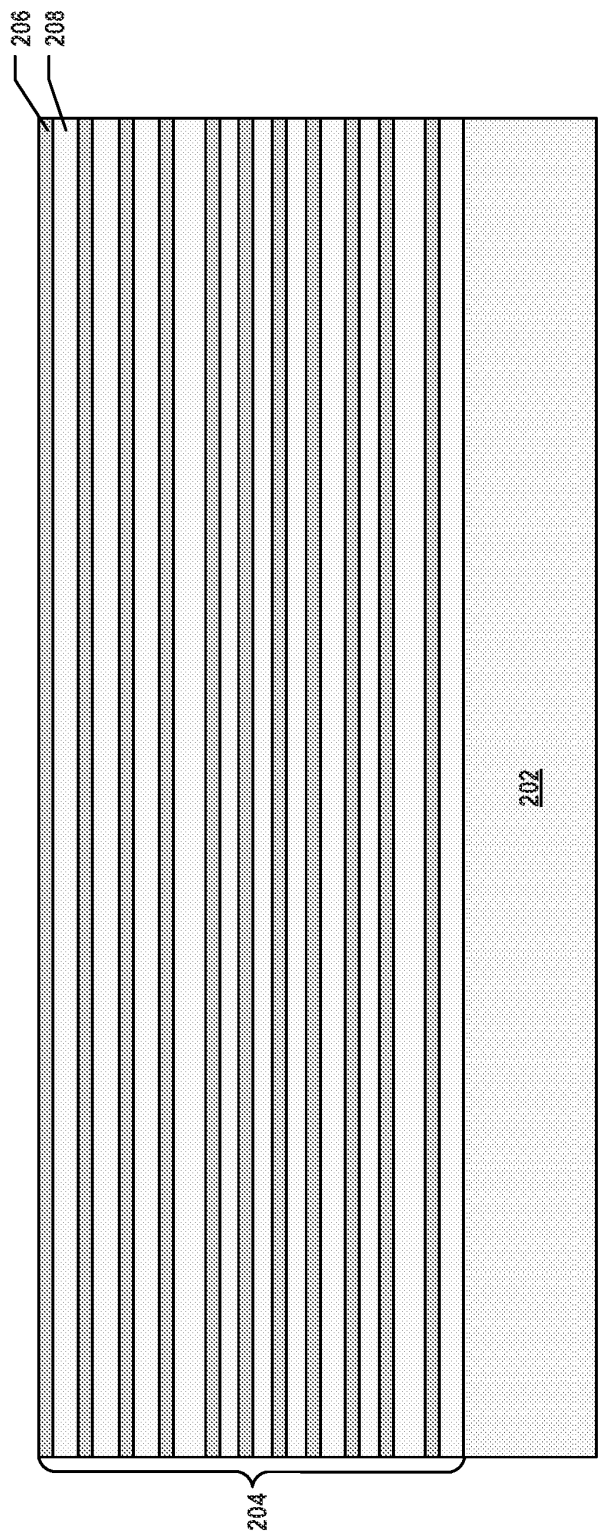


FIG. 2A

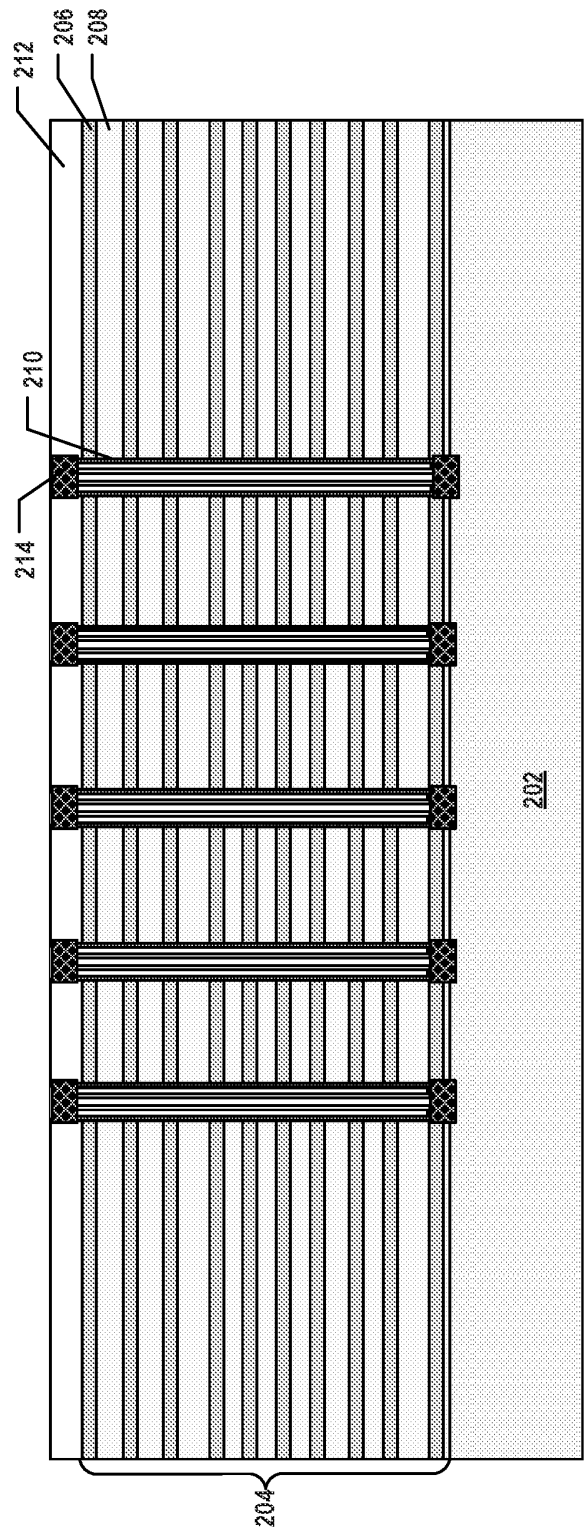


FIG. 2B

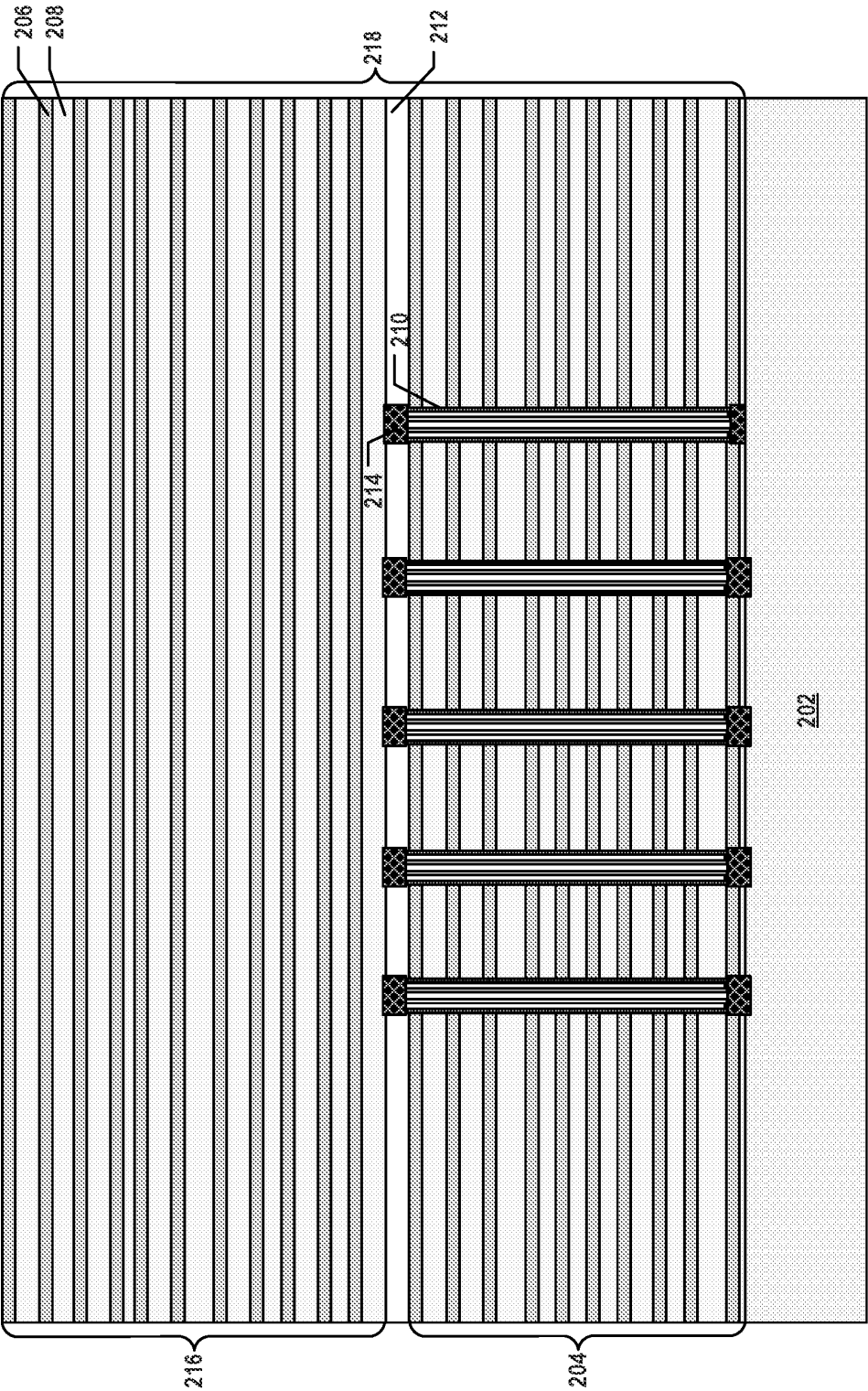


FIG.2C

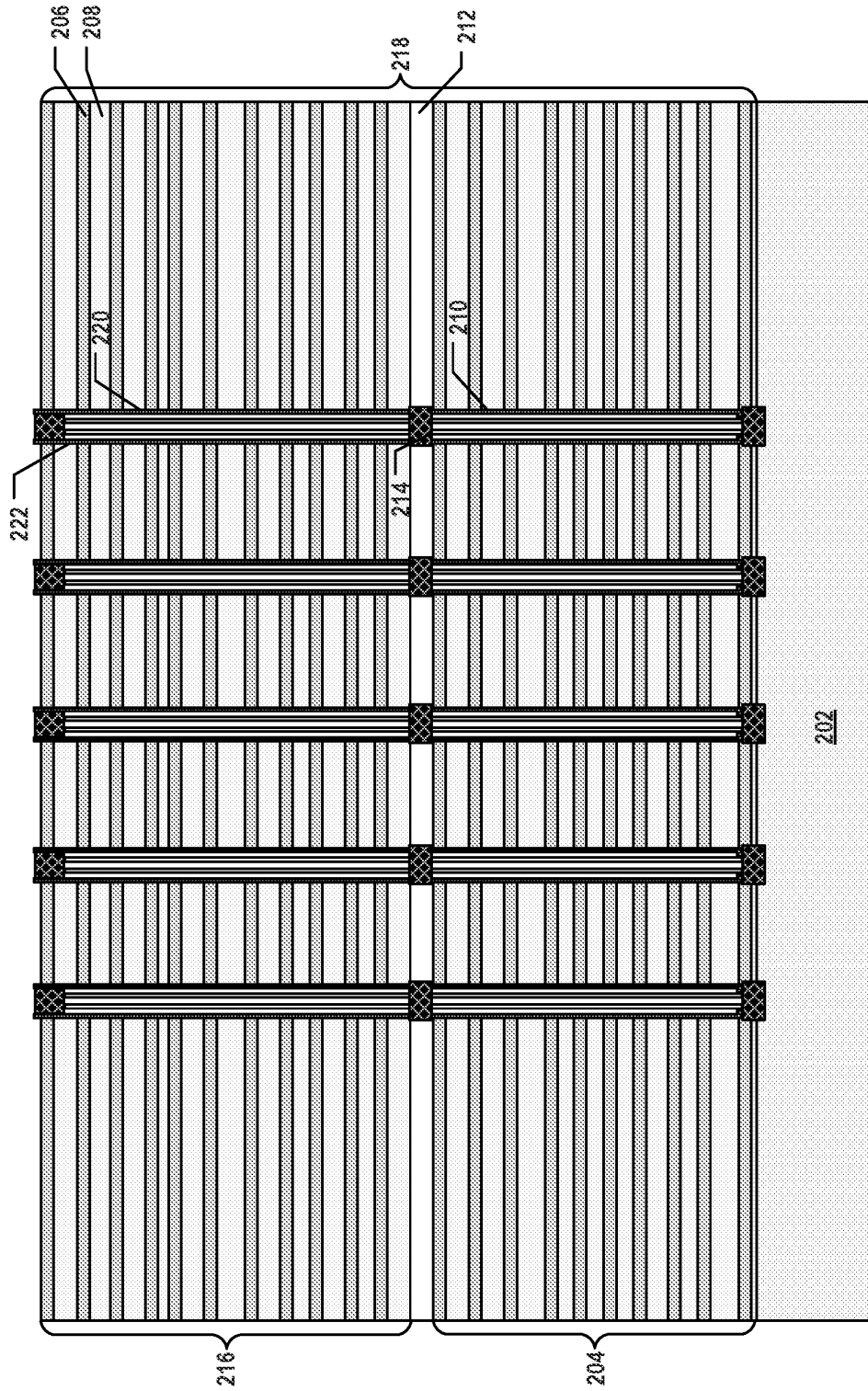


FIG. 2D

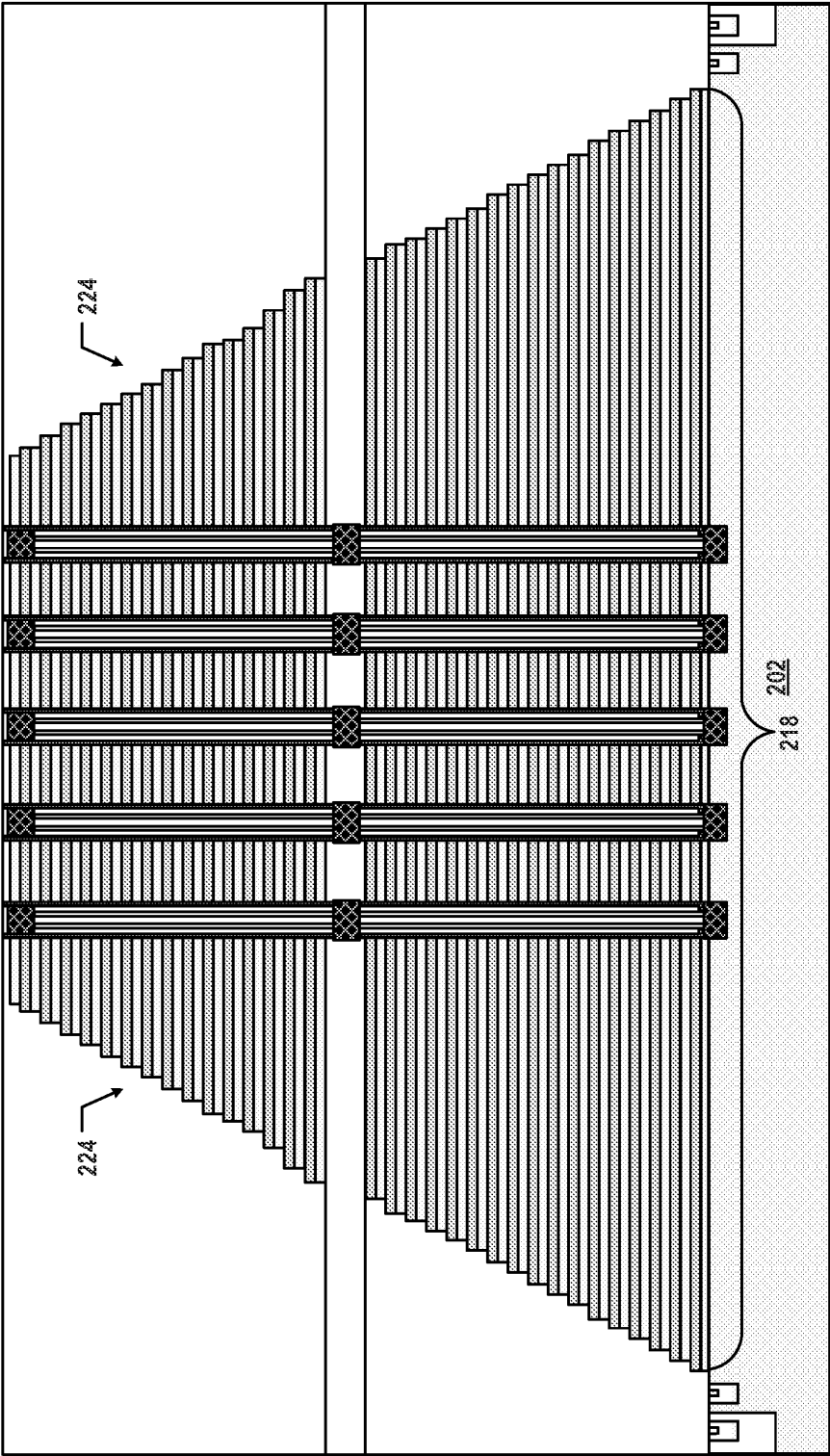


FIG. 2E

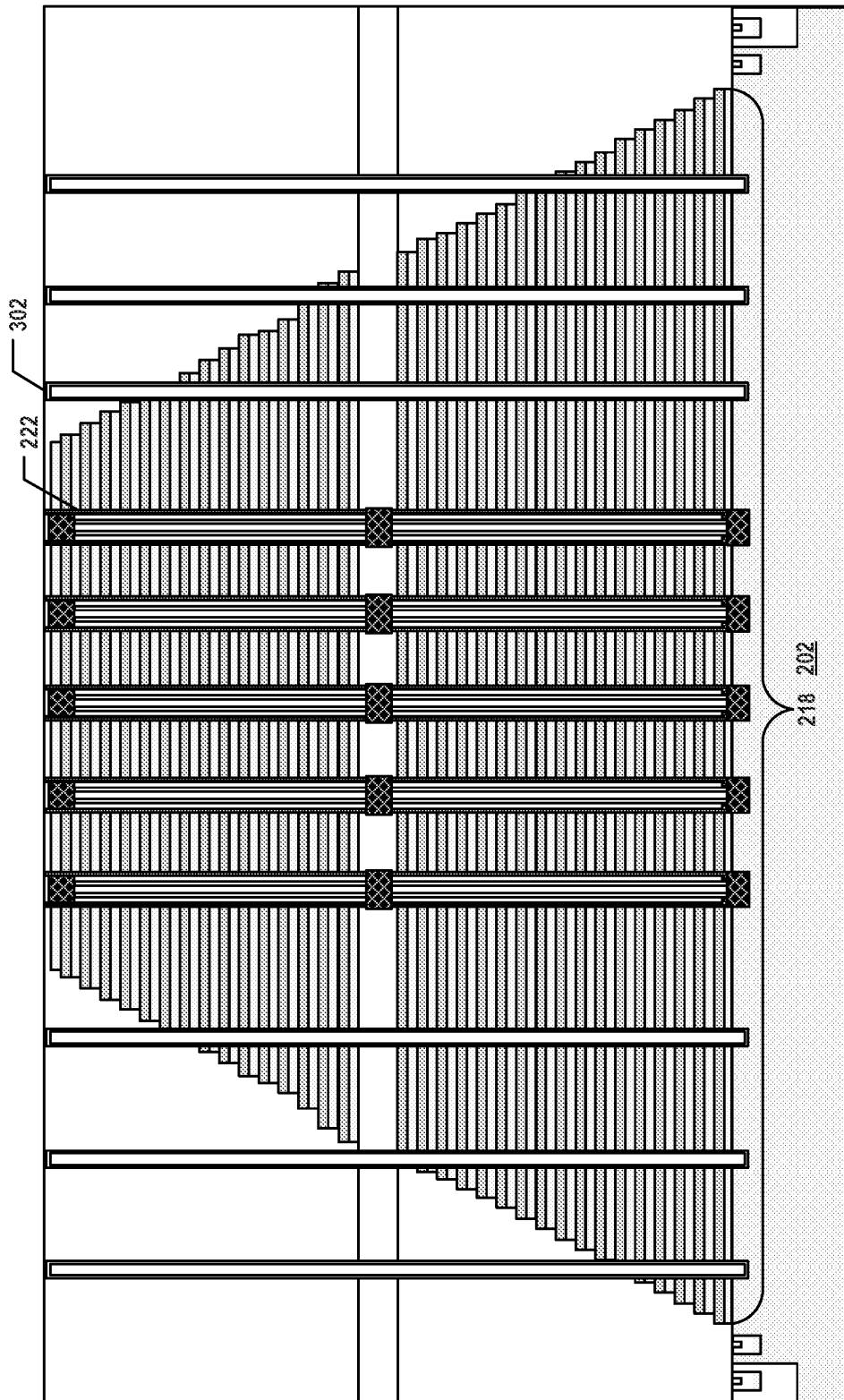


FIG. 3A

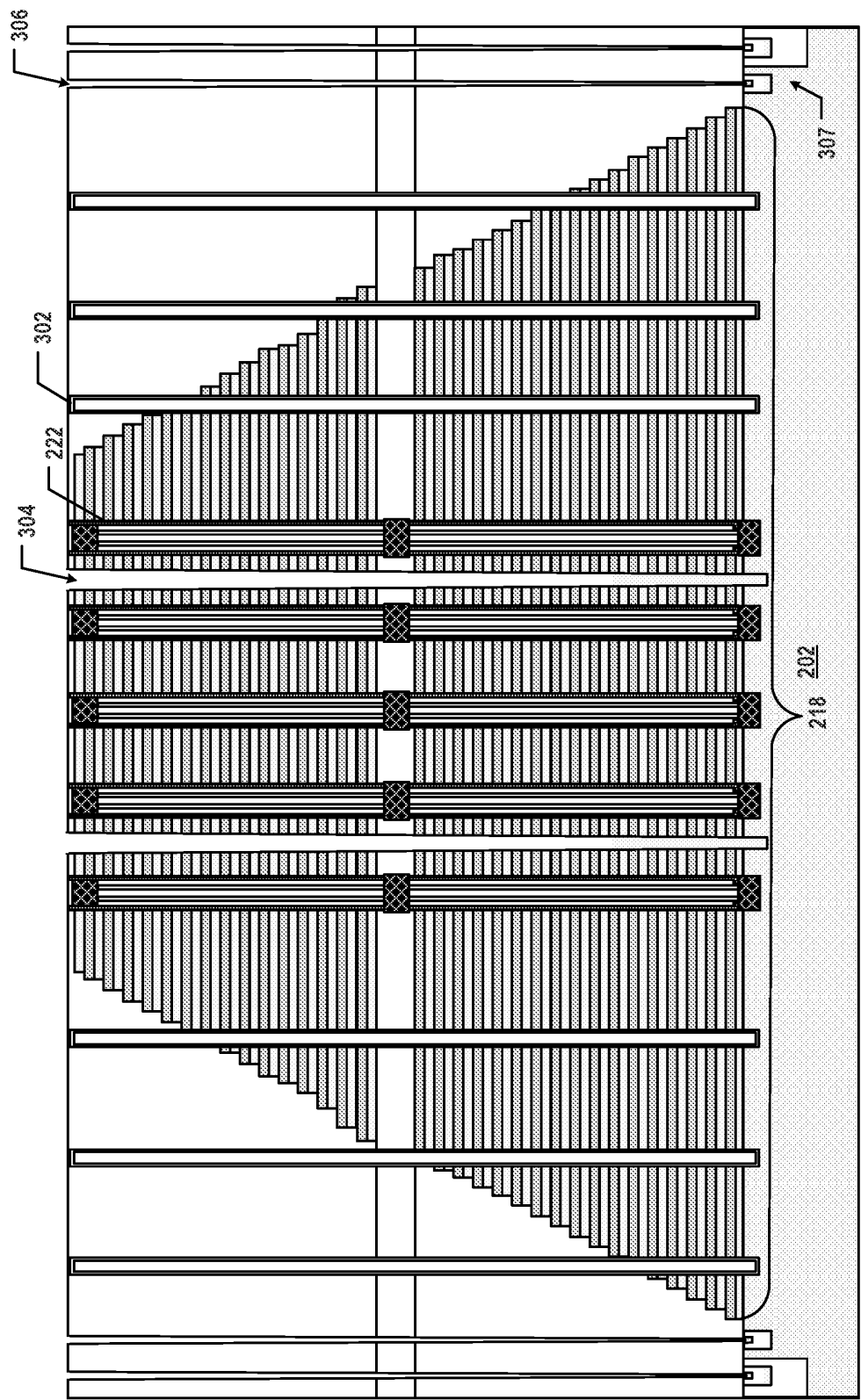


FIG. 3B

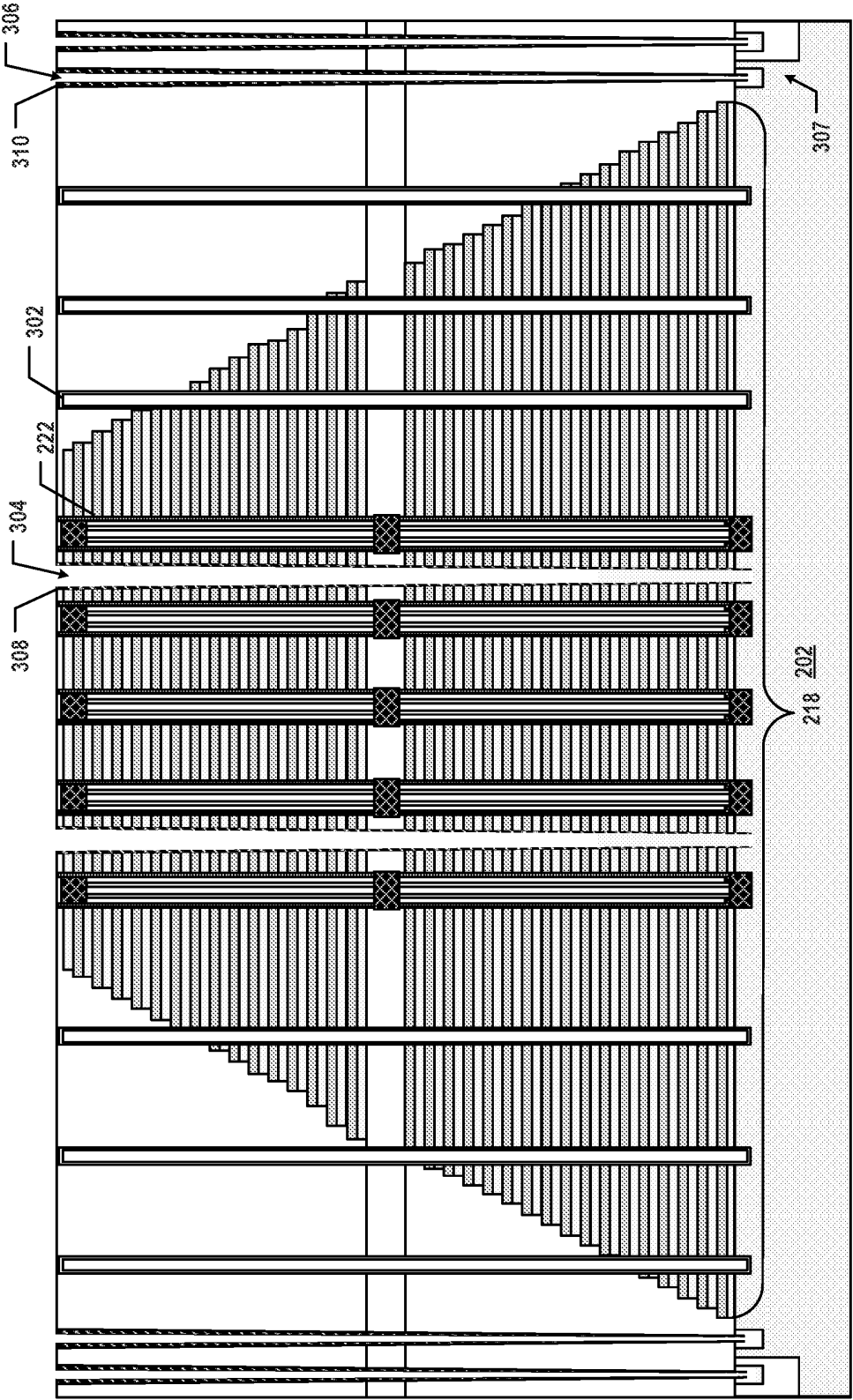


FIG. 3C

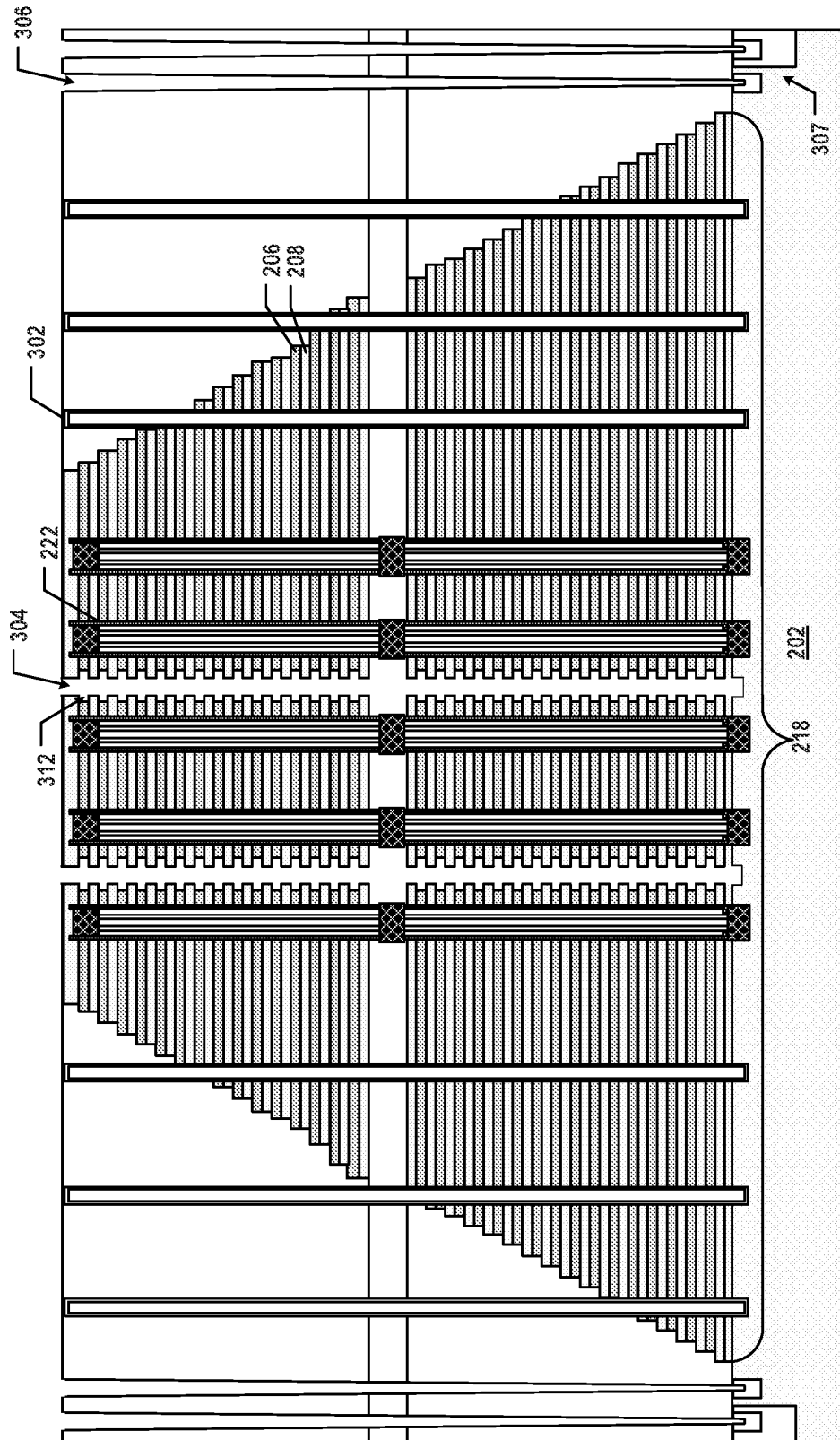


FIG. 3D

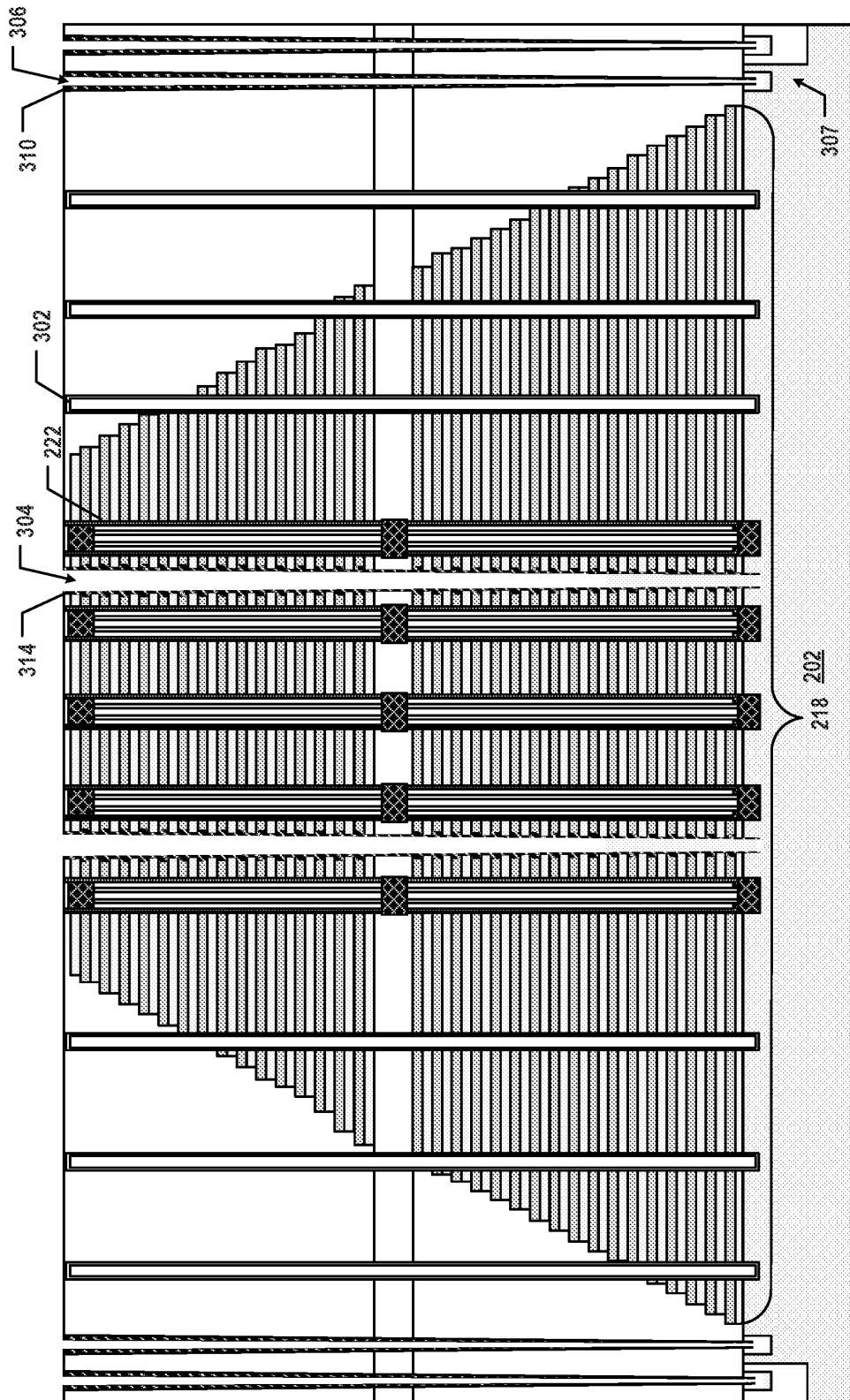


FIG. 3E

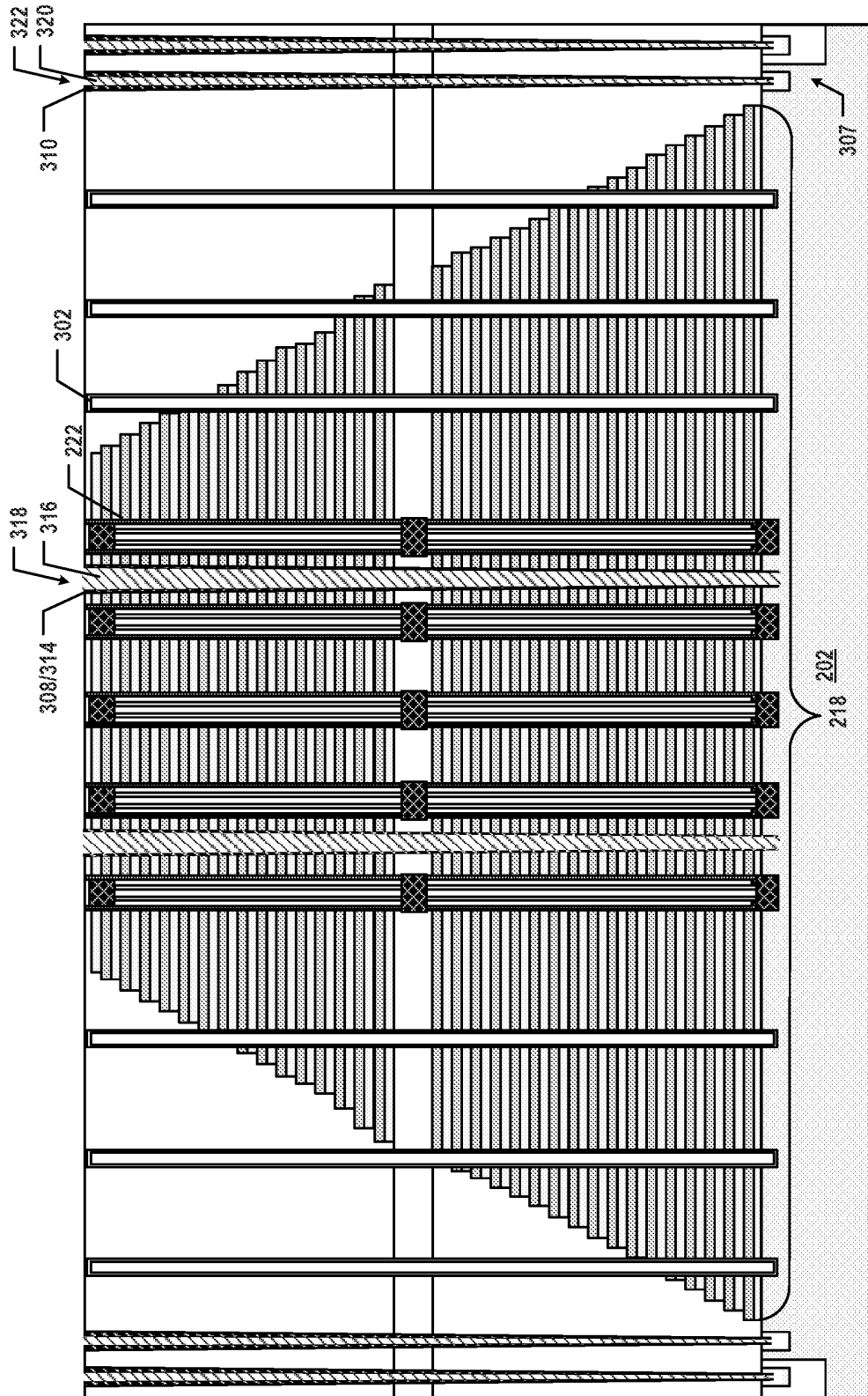


FIG. 3F

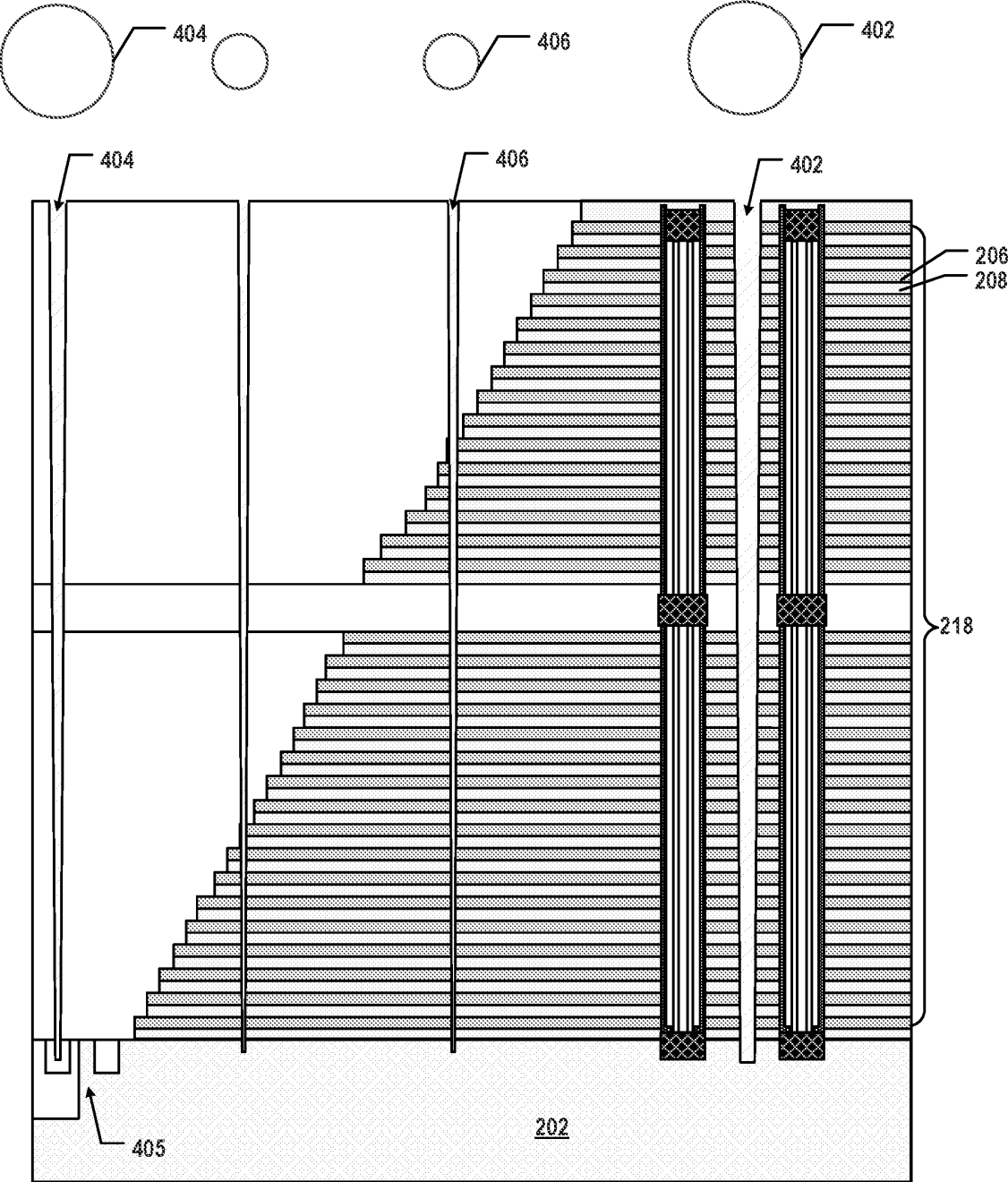


FIG. 4A

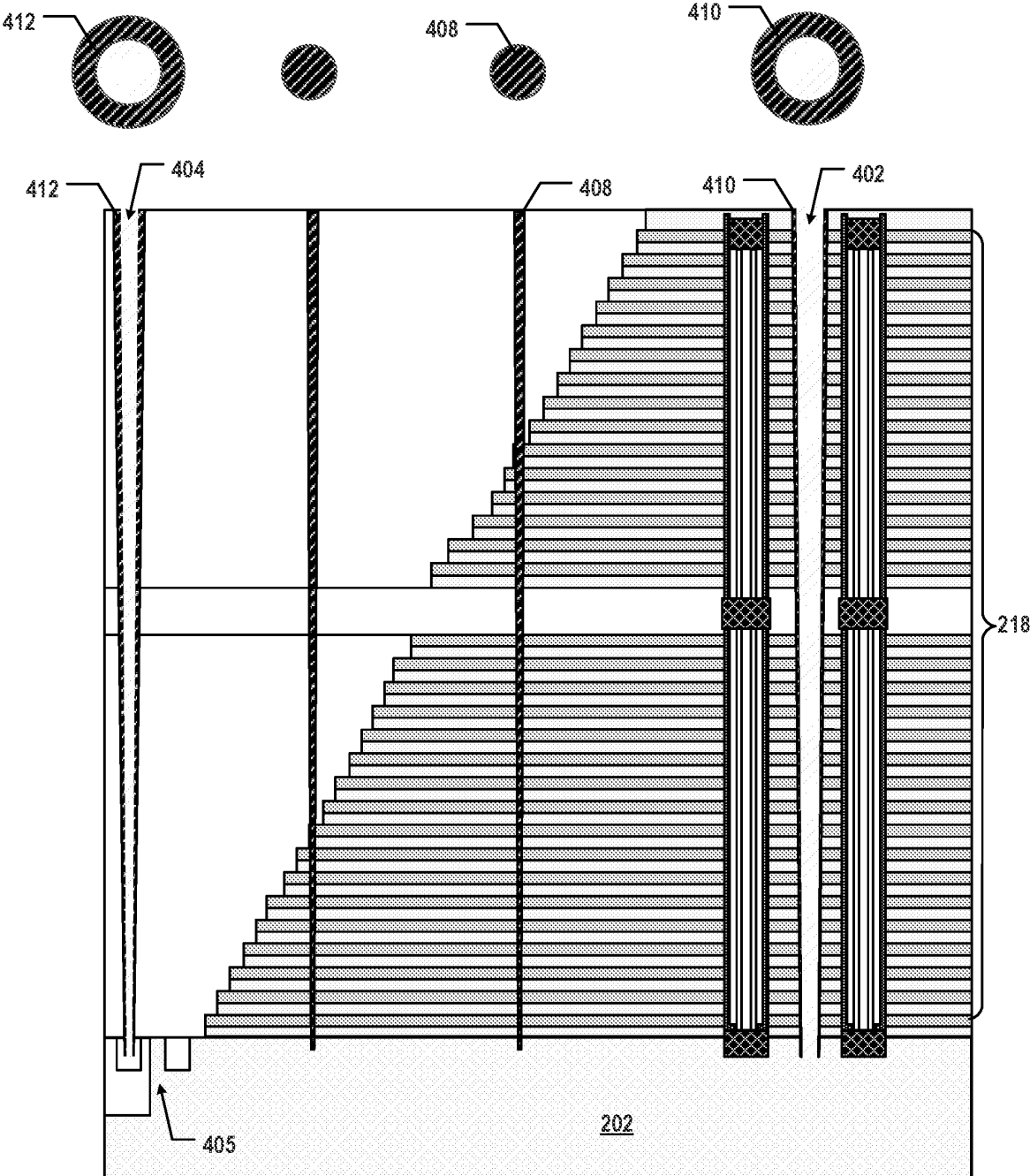


FIG. 4B

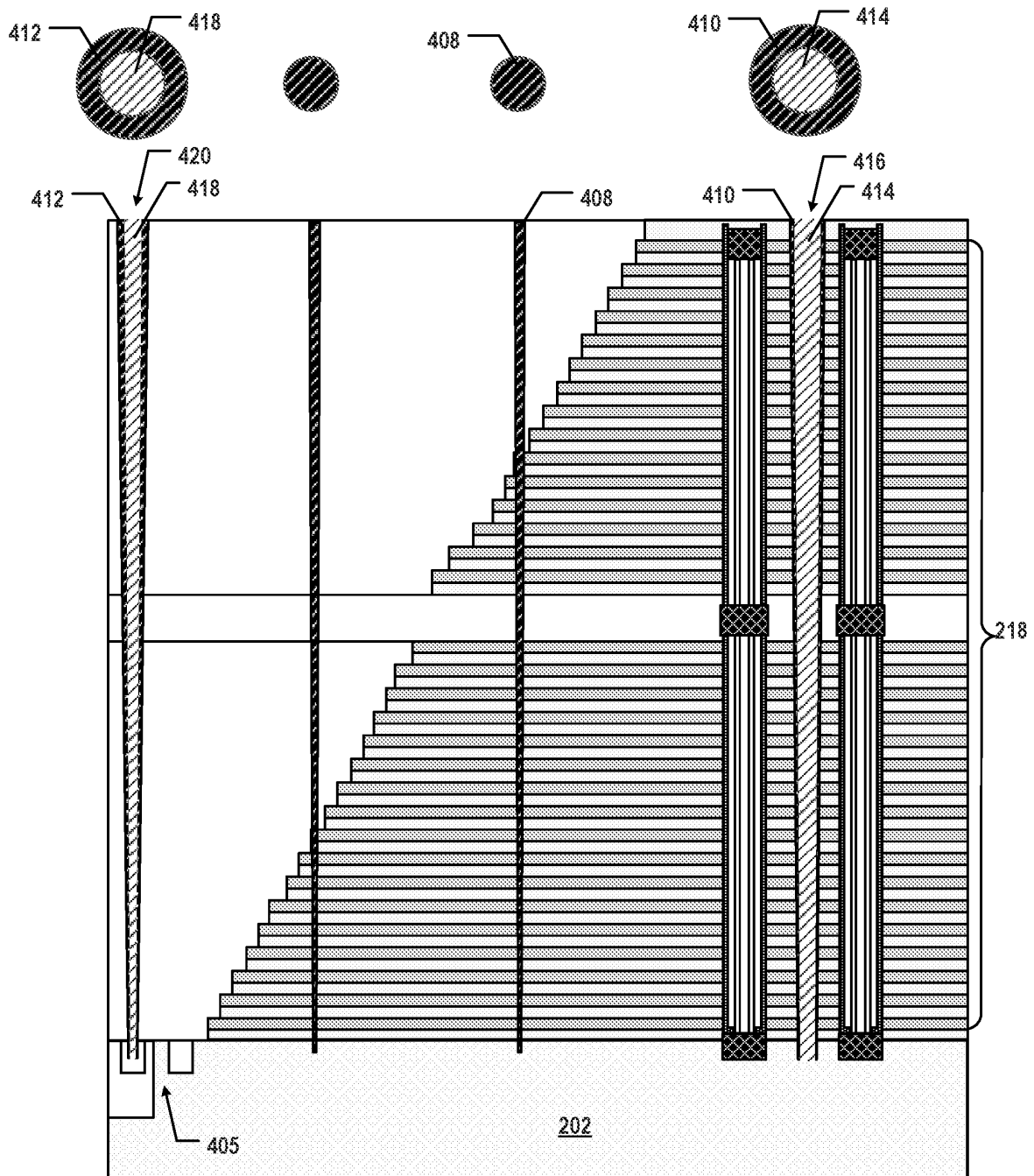


FIG. 4C

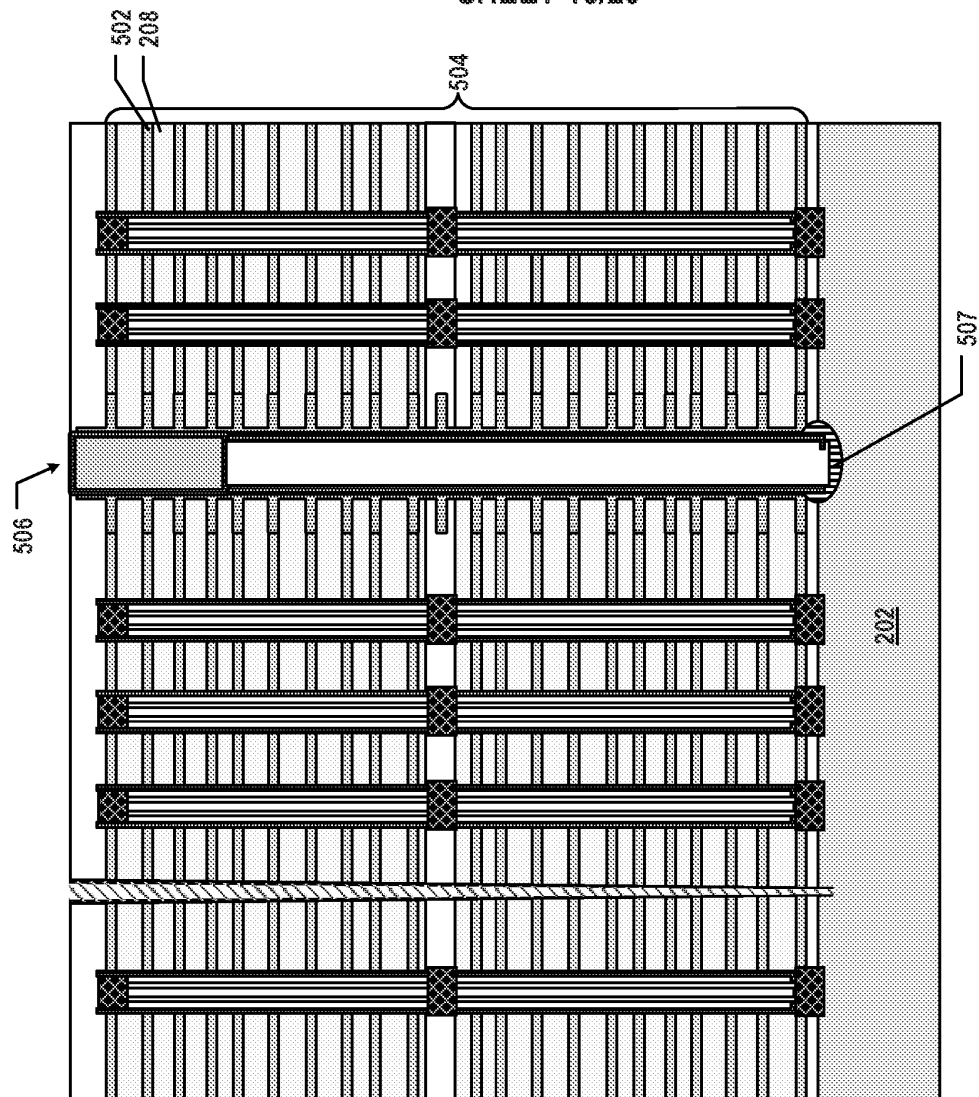
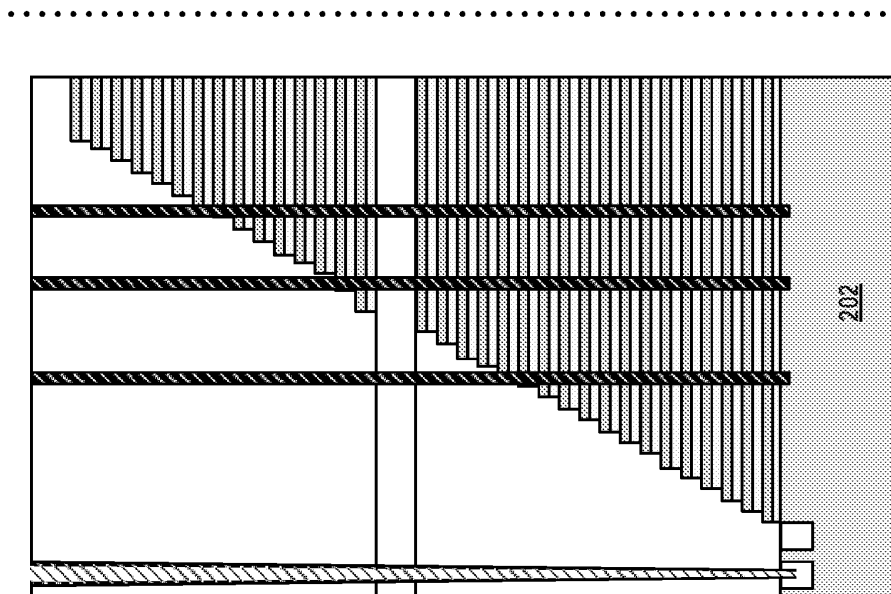


FIG. 5A



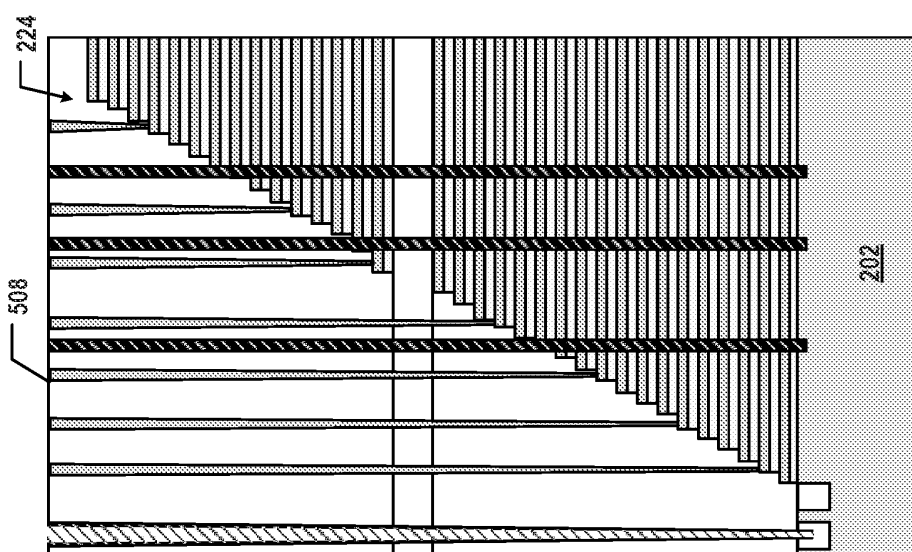
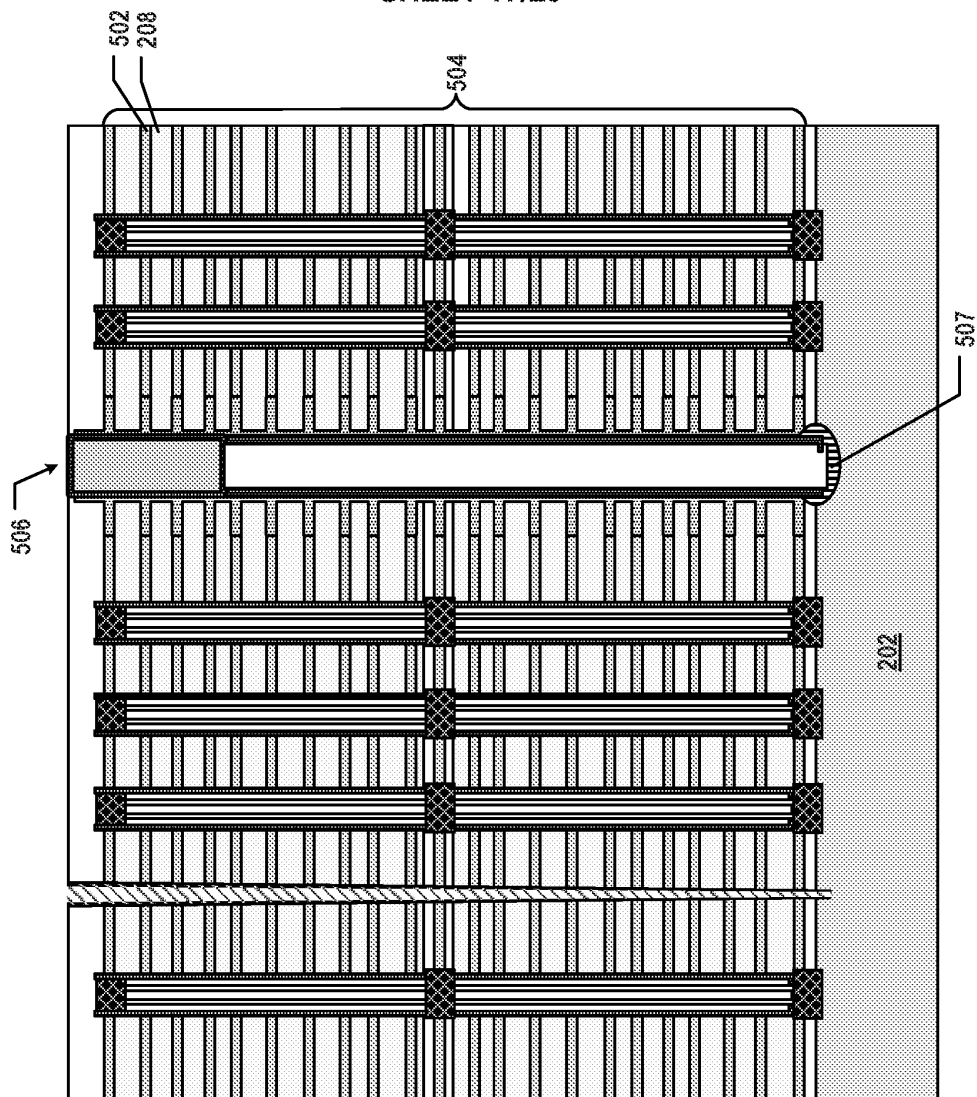


FIG. 5B

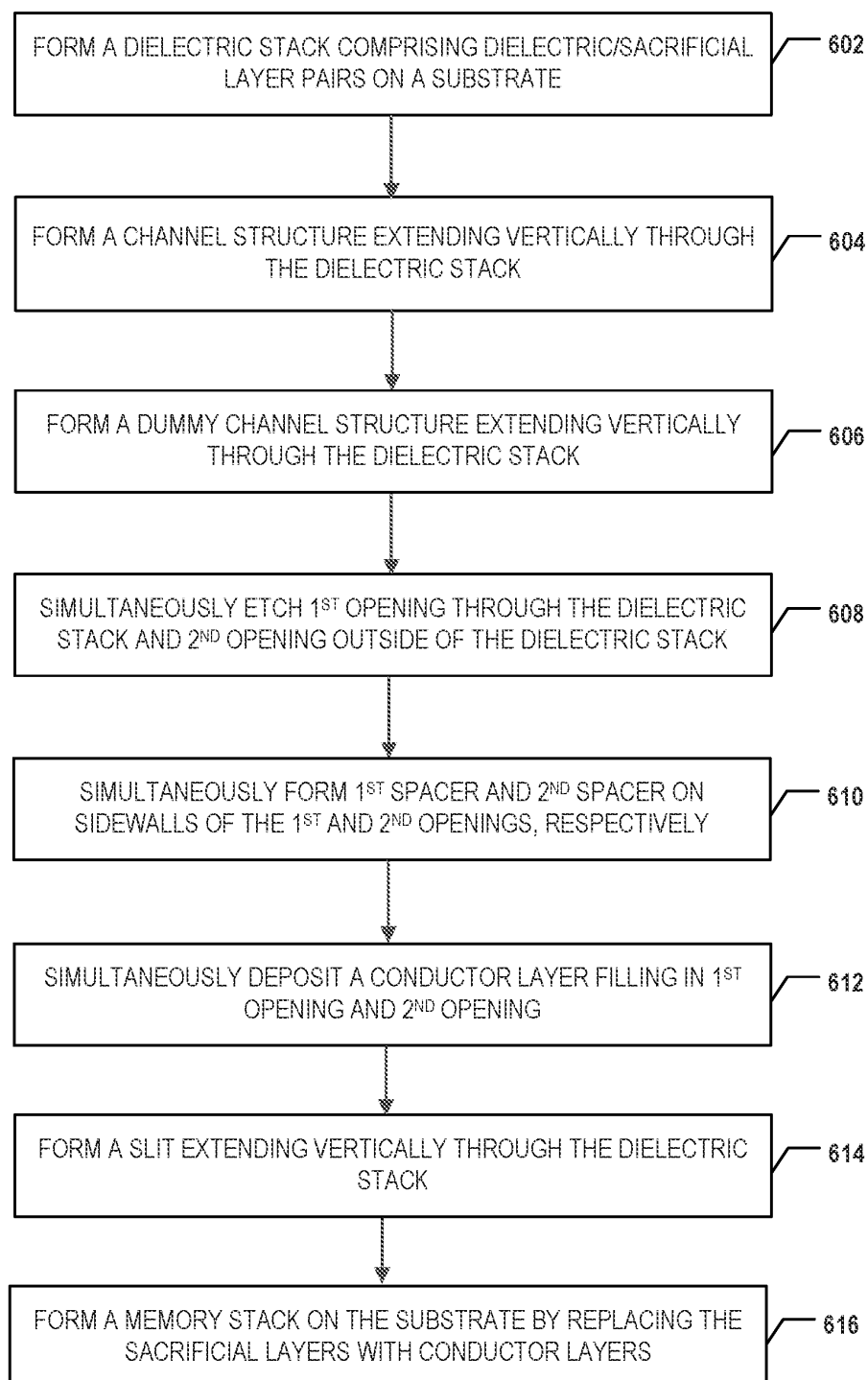
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FIG. 6

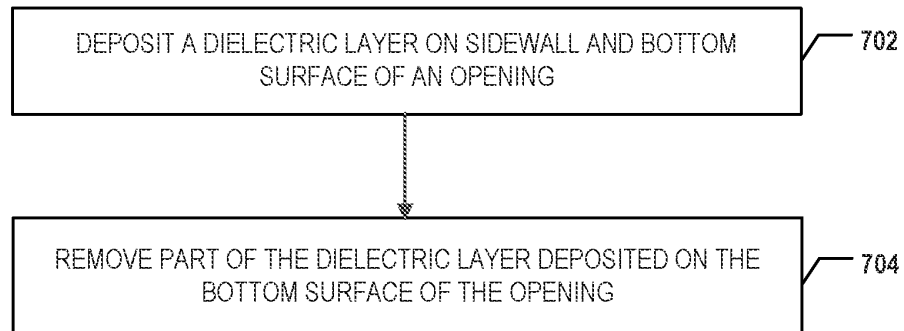


FIG. 7A

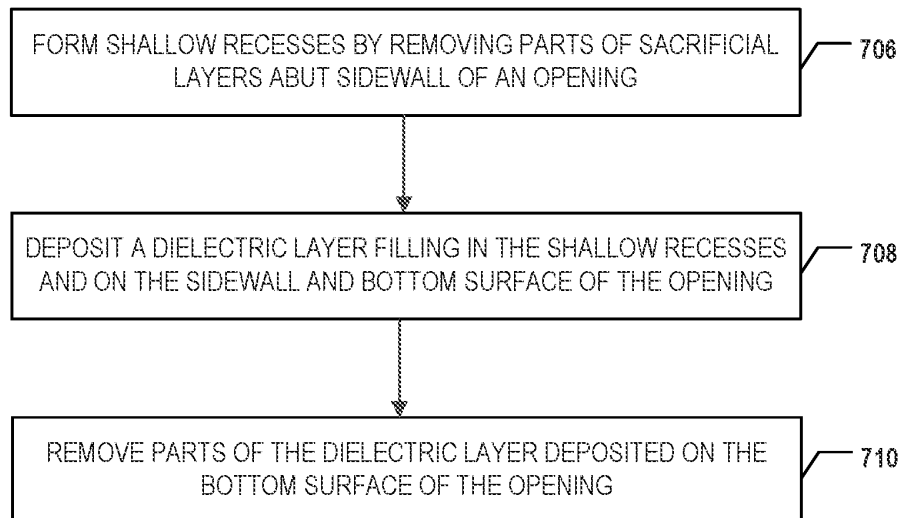


FIG. 7B

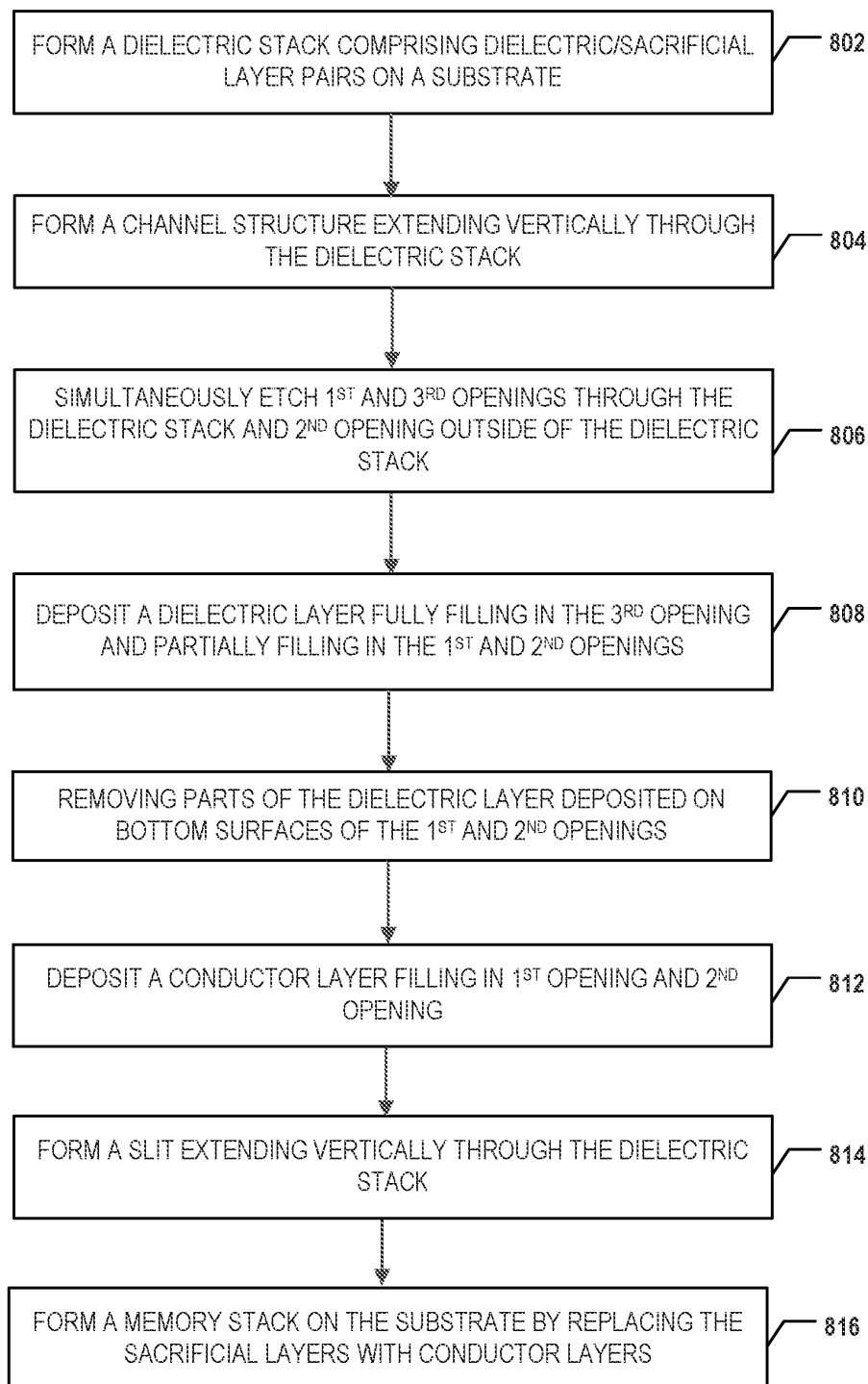
800

FIG. 8

COMBINED DECLARATION AND ASSIGNMENT**DECLARATION**

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☒ The attached application, or
- ☐ United States application or PCT international application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

Appl. No. *To Be Assigned*
Atty. Docket No. 10018-01-0015-PCT

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

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The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

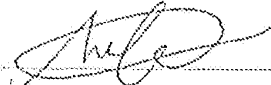
The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 153988** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

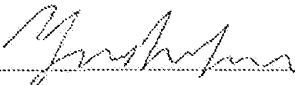
IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Mei Lau Guo Date: 2018.9.5

Signature of Inventor: 

Inventor: Yushi Hu Date: 2018.08.22

Signature of Inventor: 

Inventor: Ji Xia Date: 2018/8/22

Signature of Inventor: Ji Xia

Inventor: Hongbin Zhu Date: 2018/8/29

Signature of Inventor: 

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Application Number	
Filing Date	
First Named Inventor	Mei Lan GUO
Title	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	10018-01-0015-US-DIV2

SIGNATURE of Applicant or Patent Practitioner

Signature	/Zhiwei Zou/	Date (Optional)	11/21/2020
Name	Zhiwei Zou	Registration Number	66,041
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.



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153988

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I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

SIMON SHI-NING YANG

Title

CEO

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	Filing Date	
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV2

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	2	20140175532	A1	2014-06-26	Chen		
	3	20160099255	A1	2016-04-07	Lai		
	4	20150206895	A1	2015-07-23	OH et al.		
	5	20150179660	A1	2015-06-25	Yada et al.		

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	First Named Inventor	Mei Lan GUO	
	Art Unit	TBD	
	Examiner Name	TBD	
	Attorney Docket Number	10018-01-0015-US-DIV2	

6	20130264631	A1	2013-10-10	Alsmeier et al.
7	20120280304	A1	2012-11-08	LEE et al.
8	20120119287	A1	2012-05-17	PARK et al.

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	3	106920794	CN	A	2017-07-04	YANGTZE MEMORY TECH CO LTD		
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	5	106920796	CN	A	2017-07-04	YANGTZE MEMORY TECH CO LTD		
	6	106256005	CN	A	2016-12-21	SANDISK TECHNOLOGIES INC		

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	First Named Inventor	Mei Lan GUO	
	Art Unit	TBD	
	Examiner Name	TBD	
	Attorney Docket Number	10018-01-0015-US-DIV2	

	7	107771356	CN	A	2018-03-06	SANDISK TECHNOLOGIES INC	
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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	International Search Report issued in corresponding International Application No. PCT/CN2018/101482, mailed May 5, 2019, 5 pages	
	2	Written Opinion of the International Searching Authority issued in corresponding International Application No. PCT/CN2018/101482, mailed May 5, 2019, 4 pages	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		
	First Named Inventor	Mei Lan GUO	
	Art Unit	TBD	
	Examiner Name	TBD	
	Attorney Docket Number	10018-01-0015-US-DIV2	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2020-11-21
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		
First Named Inventor/Applicant Name:		Mei Lan Guo		
Filer:		Zhiwei Zou/Anna O'Connor		
Attorney Docket Number:		10018-01-0015-US-DIV2		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1820

Electronic Acknowledgement Receipt	
EFS ID:	41191365
Application Number:	17100847
International Application Number:	
Confirmation Number:	1008
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0015-US-DIV2
Receipt Date:	21-NOV-2020
Filing Date:	
Time Stamp:	17:32:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1820
RAM confirmation Number	E2020AKH33061040
Deposit Account	602227
Authorized User	Anna O'Connor
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	10018-01-0015-US-DIV2_UtilityPatentAppTransmittal.pdf	491713	no	2
			581d4e363d5c7ccd71257ba600e9bb2cb866f022		
Warnings:					
Information:					
2	Application Data Sheet	10018-01-0015-US-DIV2_ADS.pdf	1829303	no	10
			704d560451d4aa6033ad4cbc591631482b70e4f7		
Warnings:					
Information:					
3		10018-01-0015-US-DIV2_FINALApplication.pdf	180561	yes	31
			59768613fab7b44d0ae1c178a63a2b55f4a940bc		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Abstract		31	31	
	Claims		30	30	
	Specification		1	29	
Warnings:					
Information:					
4	Drawings-only black and white line drawings	10018-01-0015-US-DIV2_FINALFigures.pdf	149151	no	20
			46a10c850b91d6f8e81e6d097c7c35406d82b431		
Warnings:					
Information:					
5	Oath or Declaration filed	10018-01-0015-US_Declaration-Assign.pdf	4566449	no	3
			b2556008c56fba9052ebbeb08081adacacb941bb		

Warnings:					
Information:					
6	Power of Attorney	10018-01-0015-US-DIV2_GenPOA.pdf	344335	no	2
			b99eea0e2104d8618d11a951c2e37f1d7337e1d8		
Warnings:					
Information:					
7	Information Disclosure Statement (IDS) Form (SB08)	10018-01-0015-US-DIV2_IDS-SB08.pdf	612729	no	5
			e2a2b6709df783a1a00ac0bfacc4c2ec3d7ae6129		
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	34904	no	2
			f0c4dd13df0cb6a2c99599fc3646e0792c87a02d		
Warnings:					
Information:					
Total Files Size (in bytes):			8209145		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17100847
	Filing Date	2020-11-21
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV2

U.S.PATENTS							Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
	1						
If you wish to add additional U.S. Patent citation information please click the Add button.							Add
U.S.PATENT APPLICATION PUBLICATIONS							Remove
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
	1	20150236038	A1	2015-08-20	PACHAMUTHU et al.		
	2	20180331118	A1	2018-11-15	AMANO		
	3	20170062454	A1	2017-03-02	LU et al.		
	4	20170179152	A1	2017-06-22	TOYAMA et al.		
	5	20160322381	A1	2016-11-03	Liu et al.		
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add
FOREIGN PATENT DOCUMENTS							Remove

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17100847
	Filing Date		2020-11-21
	First Named Inventor	Mei Lan GUO	
	Art Unit	TBD	
	Examiner Name	TBD	
	Attorney Docket Number	10018-01-0015-US-DIV2	

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² i	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

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	Filing Date	2020-11-21
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV2

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2020-12-04
Name/Print	Zhiwei Zou	Registration Number	66,041

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	41303744
Application Number:	17100847
International Application Number:	
Confirmation Number:	1008
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0015-US-DIV2
Receipt Date:	04-DEC-2020
Filing Date:	
Time Stamp:	19:07:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	10018-01-0015-US-DIV2_IDS2-SB08.pdf	612169	no	4
			78ec512b743a54c3f386fe317661f7183a8e1092		
Warnings:					

Information:	
Total Files Size (in bytes):	612169
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 17/100,847	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	6	minus 20 = *				x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
17/100,847	11/21/2020	2812	1820	10018-01-0015-US-DIV2	6	1

CONFIRMATION NO. 1008

FILING RECEIPT



0000000122257911

153988
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

Date Mailed: 12/29/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

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Applicant(s)

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Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd.

Power of Attorney: The patent practitioners associated with Customer Number 153988

Domestic Priority data as claimed by applicant

This application is a DIV of 16/745,342 01/17/2020
which is a DIV of 16/149,103 10/01/2018 PAT 10566336
which is a CON of PCT/CN2018/101482 08/21/2018

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 12/23/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/100,847**

Projected Publication Date: 04/08/2021

Non-Publication Request: No

Early Publication Request: No

Title

THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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page 2 of 4

this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/100,847	11/21/2020	Mei Lan Guo	10018-01-0015-US-DIV2

CONFIRMATION NO. 1008

153988
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

PUBLICATION NOTICE



OC000000124731273

Title:THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

Publication No.US-2021-0104531-A1

Publication Date:04/08/2021

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/100,847	11/21/2020	Mei Lan Guo	10018-01-0015-US-DIV2	1008
153988	7590	04/08/2022	EXAMINER	
Bayes PLLC			TRAN, DZUNG	
8260 Greensboro Drive				
Suite 625				
McLean, VA 22102				
			ART UNIT	PAPER NUMBER
			2829	
			NOTIFICATION DATE	DELIVERY MODE
			04/08/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Status of the Claims

1. Claims 1-6 are pending.

Action on merits of claims 1-6 as follows.

Priority

2. Receipt is acknowledged of certified copies of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statements (IDSs) submitted on November 21st, 2020 and December 04th, 2020 have been considered by the examiner.

Drawings

4. The drawings filed on 11/21/2020 are acceptable.

Specification

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

7. Claims 1-6 are rejected under 35 U.S.C. 103 as being unpatentable over Lee (US 2012/0280304, hereinafter as Lee '304) in view of Nishikawa (US 2017/0125430, hereinafter as Nishi '430).

Regarding Claim 1, Lee '304 teaches a three-dimensional (3D) memory device, comprising:

a substrate (Fig. 23, (100); [0066]);

a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs

(Fig. 23, (140/110); [0076]-[0077]);

a channel structure (Fig. 23, (730); [0095]) extending vertically through the conductor/dielectric layer pairs in the memory stack; and

a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack.

Thus, Lee '304 is shown to teach all the features of the claim with the exception of explicitly the features: "a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack".

However, Nishi '430 teaches a dummy channel structure (Fig. 5, (7P); [0080]) filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs (32/46) in the memory stack. Examiner considers the dielectric support pillars (7P) is the dummy channel structure.

Thus, it would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Lee '304 by having a dummy channel structure for the purpose of providing structural support to the memory device structure (see para. [0095]) as suggested by Nishi '430.

Regarding Claim 2, Nishi '430 teaches a peripheral device (Fig. 11, (400); [0029]) on the substrate (Fig. 11, (9); [0029]); and a peripheral contact (Fig. 11, (476); [0115]) outside of the memory stack and in contact with the peripheral device (405; [0133]).

Regarding Claim 3, Nishi '430 teaches each of the TAC and peripheral contact comprises a spacer (Fig. 23, (160); [0095]) with a nominally same thickness.

Regarding Claim 4, Nishi '430 teaches the dielectric layer in the dummy channel structure and the spacer in the TAC comprise silicon oxide (see para. [0082]).

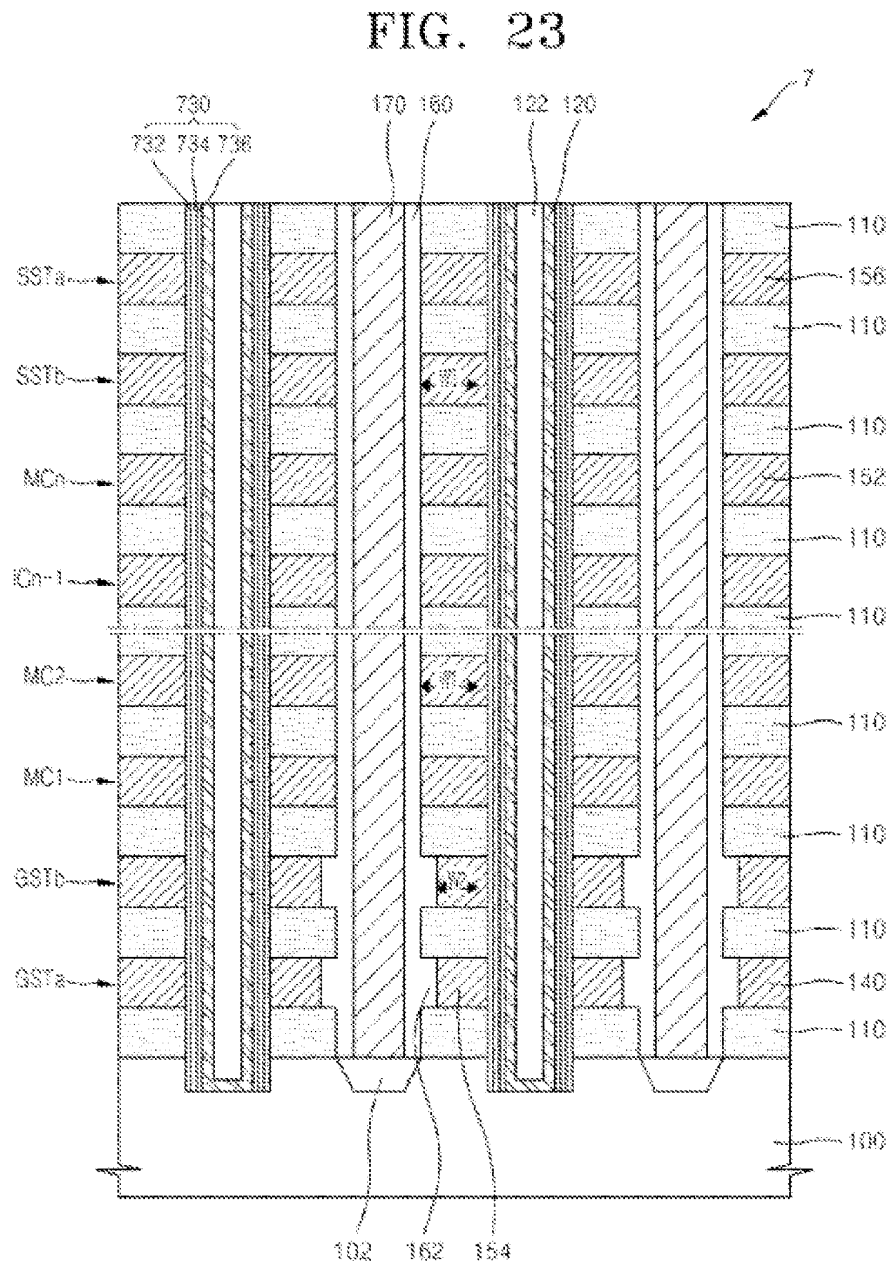


Fig. 23 (Lee '304)

8. Claims 5-6 are rejected under 35 U.S.C. 103 as being unpatentable over Lee '304 and Nishi '430 as applied to claim 1 above, and further in view of Pachamuthu (US 2015/0236038, hereinafter as Pacha '038).

Regarding Claim 8, Nishi '430 teaches a lower memory deck on the substrate (see Fig. 1).

Thus, Lee '304 and Nishi '430 are shown to teach all the features of the claim with the exception of explicitly the features: "an upper memory deck above the lower memory deck".

However, Pacha '038 teaches an upper memory deck (Fig. 15, (232/242); [0099]) above the lower memory deck (Fig. 15, (132/146); [0099]).

Thus, it would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Lee '304 and Nishi '430 by having an upper memory deck above the lower memory deck in order to form a vertical stack of multilevel memory arrays above a single substrate, with no intervening substrates (see para. [0001] and [0039]) as suggested by Pacha '038.

Regarding Claim 6, Nishi '430 teaches a lower channel structure (730) extending vertically through the lower memory deck (see Fig. 23).

Furthermore, Pacha '038 teaches an upper channel structure (Fig. 32, (260); [0141]) extending vertically through the upper memory deck; and an inter-deck plug (doped semiconductor regions 163; [0140]) disposed vertically between and in contact with the lower channel structure and the upper channel structure.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to semiconductor devices:

Kaminaga (US 2019/0115357 A1)

Cui et al. (US 10304852 B1)

Son et al. (US 2018/0151587 A1)

Yu et al. (US 2017/0358593 A1)

Hwang et al. (US 9812464 B1)

10. For applicant's benefit portions of the cited reference(s) have been cited to aid in the review of the rejection(s). While every attempt has been made to be thorough and consistent within the rejection it is noted that the *PRIOR ART MUST BE CONSIDERED IN ITS ENTIRETY, INCLUDING DISCLOSURES THAT TEACH AWAY FROM THE CLAIMS*. See MPEP 2141.02 VI.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DZUNG T TRAN whose telephone number is (571) 270-3911. The examiner can normally be reached on M-F 8 AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DZUNG TRAN/
Primary Examiner, Art Unit 2829

Notice of References Cited	Application/Control No. 17/100,847		Applicant(s)/Patent Under Reexamination Guo et al.	
	Examiner DZUNG T TRAN		Art Unit 2829	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20190115357-A1	04-2019	OH; Sung-Lae	H01L29/1037	1/1
*	B	US-10304852-B1	05-2019	Cui; Zhixin	H01L27/11565	1/1
*	C	US-20180151587-A1	05-2018	SON; Jaeick	H01L27/11573	1/1
*	D	US-20170358593-A1	12-2017	YU; Jixin	H01L27/1157	1/1
*	E	US-9812464-B1	11-2017	Hwang; Sung-Min	H01L27/1157	1/1
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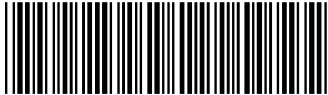
FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.
	Examiner DZUNG T TRAN	Art Unit 2829

CPC - Searched*		
Symbol	Date	Examiner
H01L 27/11531; 21/76816; 21/76877; 23/5226	04/04/2022	DT

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	314	04/04/2022	DT

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Conducted inventor name searching	04/04/2022	DT
Conducted assignee searching	04/04/2022	DT
Text searching	04/04/2022	DT

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	2319	((("LIU") near3 ("Jun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2019/11/19 02:24 PM
L2	4485	(257/315).CCLS.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2019/11/19 02:25 PM
L3	4485	(257/315).CCLS.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2019/11/19 02:30 PM
L4	4483	L3 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:30 PM
L5	4240	L4 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:31 PM
L6	2125	L5 and (bit near line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:31 PM
L7	2319	((("LIU") near3 ("Jun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2019/11/19 02:45 PM
L8	1023	L7 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:45 PM
L9	8	L8 and (memory near stack)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:46 PM
L10	1	(12/262223).APP.	(USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:47 PM
L11	56	("20070132049" "20070229166" "20080151611" "20080165567" "5559425" "5680038" "6128214" "6493258" "6504750" "6724654" "6870755" "7433226").PN. OR ("7835173").URPN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:47 PM
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L18	2355	L17 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 03:31 PM
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L28	2355	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 05:03 PM
L29	1788	L28 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 05:03 PM
L30	2355	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 05:06 PM
L31	1741	H01L27/11573.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 05:06 PM
L32	1105	H01L27/11575.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 05:51 PM
L33	1971	H01L27/11575.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 05:51 PM
L34	7516	H01L27/11582.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 06:20 PM
L35	4196	H01L27/11582.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 06:20 PM
L36	3296	L35 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 06:20 PM
L37	3260	L36 and (memory	(US-PGPUB; USPAT;	OR	OFF	OFF	2019/11/19

L38	2337	string) L37 and (bit near line)	USOCR) (US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	06:20 PM 2019/11/19 06:20 PM
L39	1159	L38 and stack	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 06:21 PM
L40	1324	(257/314).CCLS.	(US-PGPUB)	OR	ON	ON	2019/11/20 06:10 AM
L41	142	((("GUO") near3 ("Mei") near3 ("Lan")) OR (("HU") near3 ("Yushi")) OR (("XIA") near3 ("Ji")) OR (("ZHU") near3 ("Hongbin"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2019/11/20 06:10 AM
L42	2770	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/20 06:19 AM
L43	2391	L42 and @pd<"20180821"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/20 06:19 AM
L44	4923	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/20 07:00 AM
L45	4252	L44 and @pd<"20180821"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/20 07:00 AM
L46	1826	L45 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/20 07:00 AM
L47	5604	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/20 07:49 AM
L48	4538	L47 and @pd<"20180821"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/20 07:49 AM
L49	2126	L48 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/20 07:49 AM
L50	1937	H01L23/5283.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/20 07:49 AM
L51	3	("20140175532" "20160 099255" "20170125430 ").PN.	(US-PGPUB; USPAT)	OR	OFF	OFF	2019/11/20 08:10 AM
L52	2775	H01L27/11524.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/12/18 10:42 AM
L53	2477	L52 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 10:42 AM
L54	2464	L53 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 10:42 AM
L55	2358	L54 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 11:00 AM
L56	925	H01L27/11529.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/12/18 11:01 AM
L57	1715	H01L27/11529.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 11:02 AM
L58	4129	H01L27/11556.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 12:06 PM
L59	2225	H01L27/11556.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/12/18 12:06 PM

L60	2407	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/12/18 12:06 PM
L61	1800	L60 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 12:07 PM
L62	6	("20140175532" "20160 099255" "20170125430 ").PN.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2019/12/18 03:05 PM
L64	1	("9449987").PN.	(USPAT; USOCR)	OR	OFF	OFF	2019/12/18 05:54 PM
L65	0	(14/995017).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2019/12/18 05:54 PM
L66	2	"14832579"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 05:55 PM
L67	1	("20170052258").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2019/12/18 05:57 PM
L68	0	(14/995017).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2019/12/18 06:12 PM
L69	72	("20070210338" "20070252201" "20090230449" "20090242967" "20100044778" "20100112769" "20100120214" "20100155810" "20100155818" "20100181610" "20100207195" "20100320528" "20110076819" "20110133606" "20110266606" "20120001247" "20120001249" "20120001250" "20120012920" "20120119287" "20130264631" "20140061849" "20140199815" "20150076584" "20150179660" "5915167" "7005350" "7023739" "7177191" "7221588" "7233522" "7514321" "7575973" "7696559" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8394716" "9023719" "9305934").PN. OR ("9449987").URPN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 06:13 PM
L70	1	("9449987").PN.	(USPAT; USOCR)	OR	OFF	OFF	2019/12/18 06:13 PM

L71	179	((("GUO") near3 ("Mei") near3 ("Lan")) OR ((("HU") near3 ("Yushi")) OR ((("XIA") near3 ("Ji")) OR ((("ZHU") near3 ("Hongbin")))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2020/06/18 08:41 AM
L72	1326	(257/314).CCLS.	(US-PGPUB)	OR	ON	ON	2020/06/18 08:43 AM
L73	2120	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2020/06/18 08:47 AM
L74	3081	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 09:16 AM
L75	2449	L74 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:16 AM
L76	753089	"55" and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:16 AM
L77	1242	L75 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:16 AM
L78	1033	L75 and (bit data)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:18 AM
L79	1421	L77 L78	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:18 AM
L80	5390	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 09:58 AM
L81	4301	L80 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:59 AM
L82	1852	L81 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:59 AM
L83	6379	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 09:59 AM
L84	4603	L83 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 10:00 AM
L85	2159	L84 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 10:00 AM
L86	2210	H01L23/5283.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 10:51 AM
L87	2984	H01L27/11524.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 10:52 AM
L88	2481	L87 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 10:53 AM
L89	2468	L88 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 10:53 AM
L90	2270	L89 and (bit data)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 10:53 AM
L91	990	H01L27/11529.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 12:01 PM
L92	1832	H01L27/11529.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 12:01 PM
L93	4636	H01L27/11556.CPC.	(US-PGPUB; USPAT;	OR	OFF	OFF	2020/06/18

L94	2504	H01L27/11556.CPC.	USOCR) (US-PGPUB)	OR	OFF	OFF	12:01 PM 2020/06/18 12:02 PM
L95	1755	L94 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 12:02 PM
L96	0	H01L27/11557.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 12:53 PM
L97	2710	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 12:53 PM
L98	1803	L97 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 12:53 PM
L99	2006	H01L27/11573.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 12:54 PM
L100	5136	H01L27/11582.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/09/22 06:28 AM
L101	3325	L100 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/09/22 06:28 AM
L102	3285	L101 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/09/22 06:28 AM
L103	3067	L102 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/09/22 06:29 AM
L104	2215	L103 and (bit near line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/09/22 06:29 AM
L105	5	("20120119287" "20120 280304" "20130264631 " "20150179660" "2015 0206895").PN.	(US-PGPUB; USPAT)	OR	OFF	OFF	2020/11/28 11:07 AM
L106	2576	((("LIU") near3 ("Jun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2020/11/28 11:08 AM
L107	3495	(257/314).CCLS.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 11:08 AM
L108	3490	L107 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 11:09 AM
L109	3341	L108 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 11:09 AM
L110	2939	L109 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 11:09 AM
L111	1833537	6and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 11:09 AM
L112	1965	L110 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 11:09 AM
L113	2193	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2020/11/28 12:06 PM
L114	3229	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/11/28 12:09 PM
L115	2457	L114 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 12:09 PM

L116	1254	L115 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 12:09 PM
L117	2039	L115 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 12:09 PM
L118	2197	L116 L117	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 12:09 PM
L119	5627	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/11/28 01:07 PM
L120	4301	L119 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 01:07 PM
L121	1929	L120 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 01:07 PM
L122	8	("20130264631" "20160099255" "20120280304" "20150206895" "20140175532" "20150179660" "20170125430" "20120119287").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 01:30 PM
L123	1	("20200161321").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 01:31 PM
L124	3	L122 and dummy	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:19 PM
L125	6821	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/11/28 02:33 PM
L126	4604	L125 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:33 PM
L127	2431	L126 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:33 PM
L128	1975	L127 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:33 PM
L129	1	(14/133979).APP.	(USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:37 PM
L130	72	("20070210338" "20070252201" "20090230449" "20090230454" "20090242967" "20100044778" "20100112769" "20100120214" "20100155810" "20100155818" "20100181610" "20100207195" "20100320528" "20110076819" "20110133606" "20110266606" "20110303970" "20120001247" "20120001249" "20120001250" "20120012920"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:37 PM

L131	85	"20120032245" "20120208347" "20130089974" "20130264631" "7005350" "7023739" "7177191" "7221588" "7233522" "7514321" "7575973" "7696559" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8394716").PN. OR ("9449983").URPN. ("10008570" "10121794" "10553599" "10559588" "20030047755" "20030122204" "20030155582" "20030219933" "20040041192" "20040063286" "20040125629" "20040251488" "20050062098" "20080012065" "20090321855" "20100109071" "20110045657" "20110287612" "20120023894" "20120068247" "20120276702" "20130009236" "20130089974" "20130134492" "20140225160" "20140225181" "20140264525" "20150129954" "20150179660" "20160049421" "20160099250" "20160118391" "20160141294" "20160181264" "20160260733" "20160358933" "20170062454" "20170110464" "20170110470" "20170162591" "20170229472" "20170338243" "20170365613" "20180122906"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:47 PM
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L132	72	"20190252405" "20190326313" "5915167" "6274490" "6372569" "6677213" "6777274" "6833306" "6881994" "7005350" "7012299" "7202119" "8187936" "8829593" "8884357" "8946023" "9023719" "9136130" "9177966" "9230980" "9230987" "9305932" "9331093" "9356031" "9425299" "9449980" "9449983" "9460931" "9478495" "9502471" "9570463" "9576975" "9627395" "9627403" "9691884" "9698153" "9728551" "9780108" "9853043" "9876025" "9941295").PN. OR ("10797060").URPN. ("10115735" "10355017" "20060157797" "20070155074" "20070210338" "20070252201" "20080096328" "20080116583" "20090230449" "20090242967" "20100044778" "20100090286" "20100112769" "20100120214" "20100155810" "20100155818" "20100181610" "20100207195" "20100320528" "20110076819" "20110133606" "20110233688" "20110266606" "20120001247" "20120001249" "20120001250" "20120012920" "20120119287" "20120168877" "20120261756" "20120280290" "20130140669" "20130161746" "20130181264" "20130217190"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:47 PM
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		"20130264631" "20130320417" "20140117421" "20140154846" "20150008520" "20150206945" "20150214058" "20150364490" "20160163702" "20160260712" "20160351709" "20180331118" "5915167" "6319782" "6323525" "7005350" "7023739" "7177191" "7221588" "7233522" "7514321" "7575973" "7696559" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8394716" "9023719" "9305934" "9449983" "9460931" "9601503" "9859422").PN. OR ("10770459").URPN.					
L133	0	(15/873101).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 04:55 PM
L134	10	("6169019" "201701333 98" "5945350" "201603 51709" "20030190497" "5576579" "5942799" "6 229211" "20180040476 " "5847463" "6268299" " 20180245215" "200600 84247" "5874353" "201 50138862" "200300252 06" "20020140103" "20 030194859").PN.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 04:57 PM
L135	1	("20180331118").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 04:59 PM
L136	1	(15/080269).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 05:01 PM
L137	1	("20160204117").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 05:02 PM
L138	1	(14/862916).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 05:03 PM
L139	1	("20160322381").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 05:03 PM
L140	1	(14/611785).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 05:04 PM
L141	1	("20150236038").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 05:04 PM
L142	14	(US-20170125430-\$ or US-20150179660-\$ or	(US-PGPUB; USPAT)	OR	OFF	OFF	2020/11/30 10:31 AM

		US-20180122906-\$ or US-20120119287-\$ or US-20170062454-\$ or US-20180331118-\$ or US-20160204117-\$ or US-20160322381-\$ or US-20150236038-\$.did. or (US-8664761-\$ or US-9449987-\$ or US-10453798-\$ or US- 9806093-\$ or US- 10381322-\$).did.					
L143	2	((("20120280304") or ("20200161321")).PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2021/01/29 01:50 PM
L144	220	((("GUO") near3 ("Mei") near3 ("Lan")) OR (("HU") near3 ("Yushi")) OR (("XIA") near3 ("Ji")) OR (("ZHU") near3 ("Hongbin"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2021/03/04 10:34 AM
L145	1549	(257/315).CCLS.	(US-PGPUB)	OR	ON	ON	2021/03/04 10:34 AM
L146	1326	(257/314).CCLS.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 10:38 AM
L147	1027	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:25 AM
L148	1027	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:25 AM
L149	3337	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 11:32 AM
L150	2461	L149 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:32 AM
L151	1249	L150 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:32 AM
L152	5796	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 11:46 AM
L153	4304	L152 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:46 AM
L154	1932	L153 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:47 AM
L155	7132	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 01:26 PM
L156	4606	L155 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 01:26 PM
L157	2161	L156 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 01:26 PM
L158	0	H01L23/5283.CPC1	(US-PGPUB)	OR	OFF	OFF	2021/03/04 01:27 PM
L159	2521	H01L23/5283.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 01:27 PM
L160	1622	L159 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 01:29 PM

L161	3255	H01L27/11524.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 02:19 PM
L162	2481	L161 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:19 PM
L163	2468	L162 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:19 PM
L164	1852	L163 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:20 PM
L165	2019	H01L27/11529.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:20 PM
L166	5634	H01L27/11556.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:59 PM
L167	3084	H01L27/11556.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 02:59 PM
L168	1760	L167 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:00 PM
L169	3129	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 03:05 PM
L170	1803	L169 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:08 PM
L171	2336	H01L27/11573.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 03:45 PM
L172	1379	L171 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:45 PM
L173	5703	H01L27/11582.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 03:46 PM
L174	3326	L173 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L175	3286	L174 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L176	3067	L175 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L177	2423	L176 and (hole recess\$3)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L178	2354	L177 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:47 PM
L179	2251	L178 and (word data)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:47 PM
L180	1	("20120098048").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2021/03/04 04:48 PM
L181	303	((("GUO") near3 ("Mei") near3 ("Lan")) OR ("HU") near3 ("Yushi")) OR ("XIA") near3 ("Ji")) OR ("ZHU") near3 ("Hongbin"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/04/04 06:59 AM
L182	99	L181 AND ("YANGTZE MEMORY TECHNOLOGIES CO LTD.".ase. OR "MICRON	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/04/04 07:50 AM

		TECHNOLOGY, INC.".ase. OR "INTEL CORPORATION".ase. OR "WUXI PETABYTE TECHNOLOGIES CO LTD.".ase. OR "DELTA ELECTRONICS (SHANGHAI) CO LTD.".ase. OR "EMAGIN CORPORATION".ase. OR "AUBURN UNIVERSITY".ase. OR "INTEL CORPORATINO".ase. OR "SHENZHEN JIUHU TECHNOLOGY CO LIMITED".ase. OR "SHENZHEN JIUHU TECHNOLOGY CO LTD".ase.))					
L183	10019	257/314	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/04/04 07:51 AM
L184	8823	L183 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 07:52 AM
L185	919	L184 AND (bit nlearine)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 07:52 AM
L186	727	L184 AND (bit NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 07:52 AM
L187	569	H01L27/11531.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/04/04 08:25 AM
L188	1105	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:25 AM
L189	7192	H01L21/76816.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:40 AM
L190	4750	L189 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:40 AM
L191	472	L190 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 08:41 AM
L192	13	("20180331118" "20130264631" "20160099255" "20170062454" "20120280304" "20150179660" "20150206895" "20150236038" "20160322381" "20120119287" "20140175532" "20170125430" "20170179152").P N.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:54 AM
L193	1	"20210104531"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:59 AM
L194	2	"20120280304"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 09:03 AM
L195	12904	H01L21/76877.CPC.	(US-PGPUB; USPAT;	OR	OFF	OFF	2022/04/04

L196	8763	L195 AND @pd<"20180914"	USOCR) (US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	10:00 AM 2022/04/04 10:00 AM
L197	521	L196 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:00 AM
L198	361	H01L23/52.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:26 AM
L199	8494	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:26 AM
L200	8997	L199 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 10:26 AM
L201	601	L200 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:27 AM
L202	13	("20180331118" "20130 264631" "20160099255 " "20170062454" "2012 0280304" "2015017966 0" "20150206895" "201 50236038" "201603223 81" "20120119287" "20 140175532" "20170125 430" "20170179152").P N.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:18 AM
L203	1	(14/862916).APP.	(USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:20 AM
L204	135	("5387530" "5915167" "7177191" "7221588" "7233522" "7514321" "7575973" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8193054" "8198672" "8349681" "8394716" "8445347" "8450181" "8614126" "8658499" "8741761" "8828884" "8847302" "8878278" "8884357" "8928061" "8946023" "9023719" "9230979" "9437606" "20060003531" "20060258076" "20070210338" "20070252201" "20080067583" "20080169496" "20090026561" "20090121271" "20090242967" "20100044778" "20100059811" "20100112769" "20100120214" "20100133599"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:20 AM

		"20100155810" "20100155818" "20100171162" "20100181610" "20100207195" "20100213458" "20100320528" "20110065270" "20110076819" "20110133606" "20110151667" "20110266606" "20110287612" "20110312174" "20120001247" "20120001249" "20120003800" "20120003831" "20120052674" "20120061744" "20120068242" "20120074367" "20120119287" "20120140562" "20120153376" "20120208347" "20120256247" "20120261638" "20120261722" "20120276719" "20130248974" "20130264631" "20130313627" "20130313717" "20130322174" "20140225181" "20140264525" "20140264533" "20140264542" "20140273373" "20150076580" "20150179660" "20150348984" "20160049423" "20160163728" "20160276359").pn. OR ("9627403").urpn. AND (PGPB USPT USOC).dbnm.					
L205	23	"10304852"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:28 AM
L206	14	("9812464" "10304852" "10319635" "20160118399" "20170012052" "20170047343"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:29 AM

		"20170084696" "20170179154" "20170358593" "20180151587" "20190067316" "20190164991").pn. OR ("10573659").urpn. AND (PGPB USPT USOC).dbnm.					
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PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N63	1	(form\$3 near2 spacer near3 sidewall near3 first near open\$3) and (form\$3 near3 array ear contact near2 extend\$3 near vertically tnear3 dielectric near stack near3 conductor near layer near4 spacer near3 first near open\$3) and (after near form\$3 TAC near2 form\$3 near2 slit near extend\$3 near vertically near3 dielectric near stack).clm.	(USPAT)	OR	OFF	OFF	2019/12/18 03:52 PM
N181	0	(memory near stack\$3 near2 substrate near2 interleav\$3 near2 plurality near2 conduct\$3 near layers near2 dielectric near layers near4 plurality near2 conduct\$4 near layers near3 respect\$3 near shallow near recess) and (channel near structure near extend\$3 near vertically near2 memory near stack\$3).clm.	(USPAT)	OR	OFF	OFF	2021/03/04 03:21 PM

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

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	Filing Date	
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV2

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	1	20170125430	A1	2017-05-04	NISHIKAWA et al.		
	2	20140175532	A1	2014-06-26	Chen		
	3	20160099255	A1	2016-04-07	Lai		
	4	20150206895	A1	2015-07-23	OH et al.		
	5	20150179660	A1	2015-06-25	Yada et al.		

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Art Unit	TBD	
Examiner Name	TBD	
Attorney Docket Number	10018-01-0015-US-DIV2	

6	20130264631	A1	2013-10-10	Alsmeier et al.
7	20120280304	A1	2012-11-08	LEE et al.
8	20120119287	A1	2012-05-17	PARK et al.

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	1	108377660	CN	A	2018-08-07	SANDISK TECHNOLOGIES LLC		
	2	108140644	CN	A	2018-06-08	SANDISK TECHNOLOGIES LLC		
	3	106920794	CN	A	2017-07-04	YANGTZE MEMORY TECH CO LTD		
	4	106910746	CN	A	2017-06-30	YANGTZE MEMORY TECH CO LTD		
	5	106920796	CN	A	2017-07-04	YANGTZE MEMORY TECH CO LTD		
	6	106256005	CN	A	2016-12-21	SANDISK TECHNOLOGIES INC		

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Application Number		
Filing Date		
First Named Inventor	Mei Lan GUO	
Art Unit	TBD	
Examiner Name	TBD	
Attorney Docket Number	10018-01-0015-US-DIV2	

	7	107771356	CN	A	2018-03-06	SANDISK TECHNOLOGIES INC	
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	International Search Report issued in corresponding International Application No. PCT/CN2018/101482, mailed May 5, 2019, 5 pages	
	2	Written Opinion of the International Searching Authority issued in corresponding International Application No. PCT/CN2018/101482, mailed May 5, 2019, 4 pages	

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
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Application Number		
Filing Date		
First Named Inventor	Mei Lan GUO	
Art Unit	TBD	
Examiner Name	TBD	
Attorney Docket Number	10018-01-0015-US-DIV2	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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See attached certification statement.

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☒ A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2020-11-21
Name/Print	Zhiwei Zou	Registration Number	66,041

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17100847
	Filing Date	2020-11-21
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV2

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	1	20150236038	A1	2015-08-20	PACHAMUTHU et al.		
	2	20180331118	A1	2018-11-15	AMANO		
	3	20170062454	A1	2017-03-02	LU et al.		
	4	20170179152	A1	2017-06-22	TOYAMA et al.		
	5	20160322381	A1	2016-11-03	Liu et al.		
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Application Number	17100847
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First Named Inventor	Mei Lan GUO
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	10018-01-0015-US-DIV2

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See attached certification statement.

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☒ A certification statement is not submitted herewith.

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Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2020-12-04
Name/Print	Zhiwei Zou	Registration Number	66,041

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Bibliographic Data

Application No: 17/100,847

Foreign Priority claimed: ☒ Yes ☐ No

35 USC 119 (a-d) conditions met: ☒ Yes ☐ No ☐ Met After Allowance

Verified and Acknowledged: /DZUNG TRAN/

Examiner's Signature

Initials

Title:

THREE-DIMENSIONAL MEMORY DEVICES HAVING
THROUGH ARRAY CONTACTS AND METHODS FOR FORMING
THE SAME

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/21/2020	257	2829	10018-01-0015-US-DIV2
RULE			

APPLICANTS

YANGTZE MEMORY TECHNOLOGIES CO., LTD., Wuhan, CHINA

INVENTORS

Mei Lan Guo, Wuhan, CHINA

Yushi Hu, Wuhan, CHINA

Ji Xia, Wuhan, CHINA

Hongbin Zhu, Wuhan, CHINA

CONTINUING DATA

This application is a DIV of 16745342 01/17/2020 PAT 11049866

16745342 is a DIV of 16149103 10/01/2018 PAT 10566336

16149103 is a CON of PCT/CN2018/101482 08/21/2018

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

12/23/2020

STATE OR COUNTRY

CHINA

ADDRESS

Bayes PLLC

8260 Greensboro Drive

Suite 625

McLean, VA 22102

UNITED STATES

FILING FEE RECEIVED

\$1,820

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17100847
	Filing Date	2020-11-21
	First Named Inventor	Mei Lan GUO
	Art Unit	2829
	Examiner Name	TRAN, DZUNG
	Attorney Docket Number	10018-01-0015-US-DIV2

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
	1	20190355663	A1	2019-11-21	NISHIKAWA et al.		
	2	20190287982	A1	2019-09-19	HINOUE et al.		
	3	20170373079	A1	2017-12-28	SHARANGPANI et al.		
	4	20130164928	A1	2013-06-27	Lim et al.		
	5	20110049646	A1	2011-03-03	Lim et al.		
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add
FOREIGN PATENT DOCUMENTS							Remove

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17100847
	Filing Date		2020-11-21
	First Named Inventor	Mei Lan GUO	
	Art Unit	2829	
	Examiner Name	TRAN, DZUNG	
	Attorney Docket Number	10018-01-0015-US-DIV2	

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² i	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							

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NON-PATENT LITERATURE DOCUMENTS

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		

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Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17100847
	Filing Date	2020-11-21
	First Named Inventor	Mei Lan GUO
	Art Unit	2829
	Examiner Name	TRAN, DZUNG
	Attorney Docket Number	10018-01-0015-US-DIV2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2022-05-01
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		17100847		
Filing Date:		21-Nov-2020		
Title of Invention:		THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		
First Named Inventor/Applicant Name:		Mei Lan Guo		
Filer:		Zhiwei Zou/Anna O'Connor		
Attorney Docket Number:		10018-01-0015-US-DIV2		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description		Fee Code	Quantity	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
Total in USD (\$)				260

Electronic Acknowledgement Receipt	
EFS ID:	45605622
Application Number:	17100847
International Application Number:	
Confirmation Number:	1008
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0015-US-DIV2
Receipt Date:	01-MAY-2022
Filing Date:	21-NOV-2020
Time Stamp:	18:34:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 260
RAM confirmation Number	E202251134464889
Deposit Account	602227
Authorized User	Anna O'Connor
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	10018-01-0015-US-DIV2_IDS3-SB08.pdf	612173	no	4
			e7af847cf94b437fbc9d92a47cd4446d377161a		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37939	no	2
			eb7b8d9845db5e55f15a468a12cea45e9760705f		
Warnings:					
Information:					
Total Files Size (in bytes):			650112		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

USPTO Automated Interview Request (AIR)

Jun 7 2022

This paper requesting to schedule and/or conduct an interview is appropriate because:

This submission is requested to be accepted as an authorization for this interview to communicate via the internet. Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned concerning scheduling of the interview via video conference, instant messaging, or electronic mail, and to conduct the interview in accordance with office practice including video conferencing.

Name(s):
Ching-Ling Huang

S-signature:
/ChingLing Huang/

Registration Number:
62003

U.S. Application Number:
17100847

Confirmation Number:
1008

E-mail Address:
cheri.huang@bayes.law

Phone Number:
+1 5713152666

Proposed Time of Interview:
6-13-2022 11:00 AM ET

Alternative Proposed Time(s) of Interview:
6-14-2022 11:00 AM ET

Alternative Proposed Time(s) of Interview:
6-14-2022 1:00 PM ET

Preferred Interview Type:
Telephonic

I am the applicant or applicant's representative for this application.

Topic for Discussion:
Section 103 rejections



UNITED STATES
PATENT AND TRADEMARK OFFICE



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/100,847	11/21/2020	Mei Lan Guo	10018-01-0015-US-DIV2	1008
153988	7590	06/15/2022	EXAMINER	
Bayes PLLC			TRAN, DZUNG	
8260 Greensboro Drive				
Suite 625				
McLean, VA 22102				
			ART UNIT	PAPER NUMBER
			2829	
			NOTIFICATION DATE	DELIVERY MODE
			06/15/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

<i>Applicant-Initiated Interview Summary</i>	Application No. 17/100,847	Applicant(s) Guo et al.		
	Examiner DZUNG T TRAN	Art Unit 2829	AIA (First Inventor to File) Status Yes	Page 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	Title	Type
DZUNG T TRAN	Primary Examiner	Telephonic
CHERI HUANG	Attorney	

Date of Interview: 10 June 2022

Issues Discussed:

Proposed Amendment(s)

A proposed amendment to claim 1 was discussed. The examiner agreed that the proposed amendments would overcome the current arts (Lee and Nishikawa 's references). Examiner will do further search when the amended claims are filed. No agreement as to allowability was reached during the interview

/DZUNG TRAN/ Primary Examiner, Art Unit 2829	
Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04 Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing	

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD				Application or Docket Number 17/100,847		Filing Date 11/21/2020		☐ To be Mailed	
Substitute for Form PTO-875									
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED - PART I									
FOR		(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA			RATE (\$)		FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A			N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A			N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A			N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*			x \$100 =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*			x \$480 =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL			
APPLICATION AS AMENDED - PART II									
AMENDMENT	07/05/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	x \$480 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						SLIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/AMANDA CHRISTINE LEMUS/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".									
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Mei Lan GUO

Confirmation No.: 1008

Applicant: YANGTZE MEMORY
TECHNOLOGIES CO. LTD.

Art Unit: 2829

Application No.: 17/100,847

Examiner: Dzung TRAN

Filing Date: November 21, 2020

Atty. Docket: 10018-01-0015-US-DIV2

Title: **THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY
CONTACTS AND METHODS FOR FORMING THE SAME**

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop AMENDMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

In reply to the Office Action dated April 8, 2022, Applicant submits the following
Amendments and Remarks:

Amendments to the Claims are reflected in the listing of claims of this paper.

Remarks and Arguments follow the Amendment section of this paper.

be provided for in documents accompanying this paper. However, if additional extensions
of time are necessary to prevent abandonment of this application, then such extensions of time are
hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue
prosecution or appeal of this application (including issue fee, fees for a net addition of claims or
forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2227.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A three-dimensional (3D) memory device, comprising:
a substrate;
a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs;
a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;
a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack; ~~[[and]]~~
a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; and
a peripheral contact in contact with a peripheral device,
wherein a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact.

2. (Currently Amended) The 3D memory device of claim 1, further comprising:
~~[[a]] the peripheral device on the substrate; and a, the peripheral contact being arranged outside of the memory stack and in contact with the peripheral device.~~

3. (Canceled)

4. (Currently Amended) The 3D memory device of claim 2 [[3]], wherein each of the dielectric layer in the dummy channel structure, ~~[[and]] the spacers~~ spacer in the TAC, and the spacer in the peripheral contact comprises ~~comprise~~ silicon oxide.

5. (Original) The 3D memory device of claim 1, wherein the memory stack comprises:
a lower memory deck on the substrate; and
an upper memory deck above the lower memory deck.

6. (Original) The 3D memory device of claim 5, wherein the channel structure comprises:

- a lower channel structure extending vertically through the lower memory deck;
- an upper channel structure extending vertically through the upper memory deck; and
- an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.

7. (New) The 3D memory device of claim 1, wherein a diameter of the TAC is at least equal to a diameter of the peripheral contact.

8. (New) The 3D memory device of claim 1, wherein a diameter of the dummy channel structure is smaller than each of a diameter of the TAC and a diameter of the peripheral contact.

9. (New) The 3D memory device of claim 1, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.

10. (New) A three-dimensional (3D) memory device, comprising:

- a substrate;
- a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs;
- a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;
- a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack;
- a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; and
- a peripheral contact in contact with a peripheral device,

wherein:

a diameter of the TAC is at least equal to a diameter of the peripheral contact; and
a diameter of the dummy channel structure is smaller than each of the diameter of the TAC
and the diameter of the peripheral contact.

11. (New) The 3D memory device of claim 10, wherein a thickness of a spacer in the
TAC is nominally identical to a thickness of a spacer in the peripheral contact.

12. (New) The 3D memory device of claim 11, wherein the spacer of the TAC and the
spacer of the peripheral contact comprise a same material.

13. (New) The 3D memory device of claim 12, where the same material comprises
silicon oxide.

14. (New) The 3D memory device of claim 10, wherein the memory stack comprises:
a lower memory deck on the substrate; and
an upper memory deck above the lower memory deck.

15. (New) The 3D memory device of claim 14, wherein the channel structure comprises:
a lower channel structure extending vertically through the lower memory deck;
an upper channel structure extending vertically through the upper memory deck; and
an inter-deck plug disposed vertically between and in contact with the lower channel
structure and the upper channel structure.

16. (New) The 3D memory device of claim 10, wherein a first lateral dimension of the
TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a
second lateral dimension of the TAC corresponding to each dielectric layer of the
conductor/dielectric layer pairs.

17. (New) A three-dimensional (3D) memory device, comprising:
a substrate;

a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs;
a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;

a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack; and

a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,

wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.

18. (New) The 3D memory device of claim 17, further comprising:

a peripheral contact in contact with a peripheral device,

wherein:

a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact; and

a diameter of the TAC is at least equal to a diameter of the peripheral contact.

19. (New) The 3D memory device of claim 18, wherein:

a diameter of the dummy channel structure is smaller than each of the diameter of the TAC and the diameter of the peripheral contact.

20. (New) The 3D memory device of claim 17, wherein the memory stack comprises:

a lower memory deck on the substrate; and

an upper memory deck above the lower memory deck.

21. (New) The 3D memory device of claim 20, wherein the channel structure comprises:

a lower channel structure extending vertically through the lower memory deck;

an upper channel structure extending vertically through the upper memory deck; and

an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendments, claims 1, 2, and 4-21 are pending in the application, with claims 1, 10, and 17 being independent claims. Applicant hereby amends claims 1, 2, and 4; and adds new claims 7-21. These changes introduce no new matter, and their entry is respectfully requested. Support for the amendments and the new claims may be found throughout the application as filed, including the original claims and paragraphs [0062]-[0066] of the original specification.

Further, by this Amendment, claim 3 is canceled without prejudice to or disclaimer of the subject matter thereof.

Throughout the arguments, Applicant reminds the Examiner that the claims are given their broadest reasonable meaning in view of the specification, and any paraphrasing of the claim features is not to be interpreted as reading any features into, or characterizing of, the claims.

Based on the above amendments and the following remarks, Applicant respectfully requests that the Examiner reconsider and withdraw the outstanding rejections.

Examiner Interview

Applicant appreciates the courtesies extended to Applicant's representative, Ching-Ling Huang (Reg. No. 62,003), by the Examiner in the telephonic interview on June 10, 2022. During the interview, the parties discussed the rejections under 35 U.S.C. § 103, different manners of the proposed amendments to the independent claims, and the applied references. Applicant also thanks for the Examiner's agreement that the proposed amendments in the three different manners, as reflected in this Amendment and Reply, would all overcome the applied references.

Rejections under 35 U.S.C. § 103

Applicant respectfully traverses the rejection of claims 1-4 under 35 U.S.C. § 103 as allegedly being unpatentable over U.S. Patent Appl. Pub. No. 2012/0280304 ("*Lee*") in view of U.S. Patent Appl. Pub. No. 2017/0125430 ("*Nishikawa*"); and the rejection of claims 5 and 6 under 35 U.S.C. § 103 as allegedly being unpatentable over *Lee* in view of U.S. Patent Appl. Pub. No. 2015/0236038 ("*Pachamuthu*"). No *prima facie* case of obviousness has been established.

Atty. Dkt. No. 10018-01-0015-US-DIV2

By this Amendment, Applicant amends the pending claims to further distinguish them from the cited references. For example, independent claim 1 has been amended to incorporate original claim 3 and recites a three-dimensional (3D) memory device including, for example, “a peripheral contact in contact with a peripheral device,” where “a thickness of a spacer in [a] TAC is nominally identical to a thickness of a spacer in the peripheral contact.” *Lee*, *Nishikawa*, and *Pachamuthu*, whether taken alone or in combination, do not disclose at least these elements.

In particular, during the interview, the Examiner agreed that the proposed amendments would overcome the outstanding rejections. Amendments to claim 1 in the listing of claims of this paper are identical to those discussed in the interview. For at least this reason, amended independent claim 1 is allowable.

Specifically, in the rejection of claim 3, the Examiner alleged that *Nishikawa* teaches the claimed “each of the TAC and peripheral contact comprises a spacer with nominally same thickness,” referring to paragraph [0095] and FIG. 23 of *Nishikawa* for support. Office Action at 4. Applicant respectfully disagrees.

Nishikawa does not disclose FIG. 23. Therefore, Applicant submits that the Examiner may refer to *Lee* instead. In paragraph [0095], *Lee* discloses that “[] first control gate electrodes 152 may have a first width W1 between a sidewall insulation layer 160 and [a] channel regions 120..., and [] second control gate electrodes 154 may have a second width W2 that is narrower compared to the first width W1.... [T]hird control gate electrodes 156 may have... a third width W3 between the sidewall insulation layer 160 and the channel region 120, and the third width W3 may be the same as the first width W1.” As shown in FIG. 23 of *Lee*, none of W1, W2, and W3 can be equivalent from the claimed “thickness” of the “spacer,” as recited in claim 3.

That is, *Nishikawa* and *Lee*, whether taken alone or in combination, do not disclose or suggest “a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact,” as included in original claim 3 and recited in amended claim 1 (emphases added). *Pachamuthu* does not cure the deficiency. Therefore, amended independent claim 1 is allowable.

Dependent claims 2 and 4-6 are also allowable at least by virtue of their dependence upon claim 1. Claim 3 is canceled, rendering its rejection moot.

Accordingly, Applicant respectfully requests withdrawal of the rejections of claims 1-6 under 35 U.S.C. § 103.

New Claims

By this Amendment, Applicant adds new claims 7-21 to address other aspects of the instant application. New claims 7-9 depend upon claim 1. New claim 10 is an independent claim which new claims 11-16 depend upon. New 17 is an independent claim which new claims 18-21 depend upon.

Applicant discussed new claims 10 and 17 with the Examiner during the interview and thanks for the Examiner's agreement that new claims 10 and 17 are patentable in view of the currently applied references.

Dependent claims 7-9, 11-16, and 18-21 are also allowable at least by virtue of their dependence upon claim 1, 10, or 17.

Therefore, Applicant respectfully requests that the Examiner would allow new claims 7-21, together with the other pending claims, in the next official communication.

Conclusion

All of the stated grounds of the rejections in the Office Action have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw the presently outstanding rejections. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

BAYES PLLC

/Ching-Ling Huang/

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Date: July 5, 2022

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Electronic Acknowledgement Receipt

EFS ID:	46116673
Application Number:	17100847
International Application Number:	
Confirmation Number:	1008
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Ching-Ling Huang/Anna O'Connor
Filer Authorized By:	Ching-Ling Huang
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		10018-01-0015-US-DIV2_ResponseUnder111_signed.pdf	258408 ea8c81b6de49a43529dd46c7b6097a21ef4822e1	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Request for Reconsideration-After Non-Final Rejection	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	10
Warnings:			
Information:			
Total Files Size (in bytes):		258408	
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153988	7590	08/08/2022	EXAMINER	
Bayes PLLC			TRAN, DZUNG	
8260 Greensboro Drive				
Suite 625				
McLean, VA 22102				
			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
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Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Status of the Claims

1. Applicant's remarks/amendments of claims 1-6 in the reply filed on July 05th, 2022 are acknowledged. Claims 1-2 and 4 have been amended. Claims 7-21 have been added. Claim 3 has been cancelled. Claims 1-2 and 4-21 are pending.

Action on merits of claims 1-2 and 4-21 as follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

3. Claims 1-2, 4, 7-13 and 16-19 are rejected under 35 U.S.C. 103 as being unpatentable over Lee (US 2012/0280304, hereinafter as Lee '304) in view of Nishikawa

(US 2017/0125430, hereinafter as Nishi '430) and further in view of Lee (US 2015/0348987, hereinafter as Lee '987).

Regarding Claim 1, Lee '304 teaches a three-dimensional (3D) memory device, comprising:

a substrate (Fig. 23, (100); [0066]);

a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs (Fig. 23, (140/110); [0076]-[0077]);

a channel structure (Fig. 23, (730); [0095]) extending vertically through the conductor/dielectric layer pairs in the memory stack; and

a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack.

Thus, Lee '304 is shown to teach all the features of the claim with the exception of explicitly the features: "a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; a peripheral contact in contact with a peripheral device, wherein a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact".

However, Nishi '430 teaches a dummy channel structure (Fig. 5, (7P); [0080]) filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs (32/46) in the memory stack. Examiner considers the dielectric support pillars (7P) is the dummy channel structure; and a thickness of a spacer (Fig. 12, (74); [0113]) in the TAC is nominally identical to a thickness of a spacer (Fig. 12, (474); [0113]) in the peripheral contact.

Thus, it would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Lee '304 by having a dummy channel structure

for the purpose of providing structural support to the memory device structure (see para. [0095]) as suggested by Nishi '430.

Thus, Lee '304 and Nishi '430 are shown to teach all the features of the claim with the exception of explicitly the features: "a peripheral contact in contact with a peripheral device".

However, Lee '987 teaches a peripheral contact (Fig. 19, (248); [0167]) in contact with a peripheral device (CMOS transistor; [0158]).

It would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Lee '304 and Nishi '430 by having a peripheral contact in contact with a peripheral device in order to connect the memory cell structure and the peripheral circuit structure (see para. [0167]) as suggested by Lee '987.

Further, it has been held to be within the general skill of a worker in the art to select a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Regarding Claim 10, Lee '304 teaches a three-dimensional (3D) memory device, comprising:

a substrate (Fig. 23, (100); [0066]);

a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs (Fig. 23, (140/110); [0076]-[0077]);

a channel structure (Fig. 23, (730); [0095]) extending vertically through the conductor/dielectric layer pairs in the memory stack; and

a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack.

Thus, Lee '304 is shown to teach all the features of the claim with the exception of explicitly the features: "a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; a peripheral contact in contact with a peripheral device; and a diameter of the TAC is at least equal to a diameter of the peripheral contact; and a diameter of the dummy channel structure is smaller than each of the diameter of the TAC and the diameter of the peripheral contact".

However, Nishi '430 teaches a dummy channel structure (Fig. 5, (7P); [0080]) filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs (32/46) in the memory stack. Examiner considers the dielectric support pillars (7P) is the dummy channel structure; and a diameter of the TAC (79) is at least equal to a diameter of the peripheral contact (479) (see Fig. 9); and a diameter of the dummy channel structure (7P; [0080]) is smaller than each of the diameter of the TAC (79; [0086]) and the diameter of the peripheral contact (479; [0086]).

Thus, it would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Lee '304 by having a dummy channel structure for the purpose of providing structural support to the memory device structure (see para. [0095]) as suggested by Nishi '430.

Thus, Lee '304 and Nishi '430 are shown to teach all the features of the claim with the exception of explicitly the features: "a peripheral contact in contact with a peripheral device".

However, Lee '987 teaches a peripheral contact (Fig. 19, (248); [0167]) in contact with a peripheral device (CMOS transistor; [0158]).

It would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Lee '304 and Nishi '430 by having a peripheral contact in contact with a peripheral device in order to connect the memory cell structure and the peripheral circuit structure (see para. [0167]) as suggested by Lee '987.

Further, it has been held to be within the general skill of a worker in the art to select a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Regarding Claim 17, Lee '304 teaches a three-dimensional (3D) memory device, comprising:

a substrate (Fig. 23, (100); [0066]);

a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs (Fig. 23, (140/110); [0076]-[0077]);

a channel structure (Fig. 23, (730); [0095]) extending vertically through the conductor/dielectric layer pairs in the memory stack; and

a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack.

Thus, Lee '304 is shown to teach all the features of the claim with the exception of explicitly the features: "a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs".

However, Nishi '430 teaches a dummy channel structure (Fig. 5, (7P); [0080]) filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs (32/46) in the memory stack. Examiner considers the dielectric support pillars (7P) is the dummy channel structure.

Thus, it would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Lee '304 by having a dummy channel structure for the purpose of providing structural support to the memory device structure (see para. [0095]) as suggested by Nishi '430.

Thus, Lee '304 and Nishi '430 are shown to teach all the features of the claim with the exception of explicitly the features: "a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs".

However, it has been held to be within the general skill of a worker in the art to have a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

FIG. 23

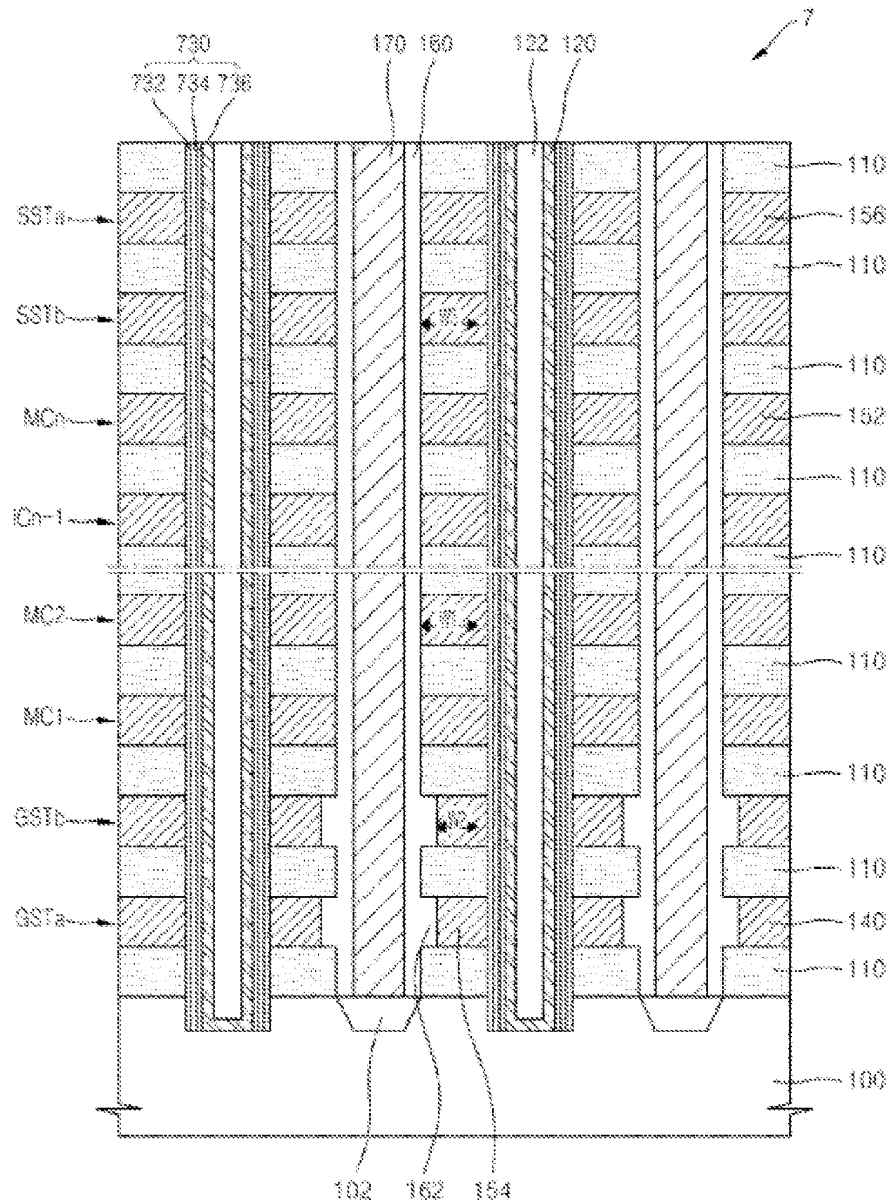


Fig. 23 (Lee '304)

Regarding Claim 7, Nishi '430 teaches a diameter of the TAC (Fig. 9, (79); [0086]) is at least equal to a diameter of the peripheral contact (479; [0086]).

Further, it has been held to be within the general skill of a worker in the art to select a diameter of the TAC is at least equal to a diameter of the peripheral contact on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Regarding Claims 8 and 19, Nishi '430 teaches a diameter of the dummy channel structure (7P; [0080]) is smaller than each of a diameter of the TAC (79) and a diameter of the peripheral contact (479) (see Fig. 9).

Further, it has been held to be within the general skill of a worker in the art to select a diameter of the dummy channel structure is smaller than each of a diameter of the TAC and a diameter of the peripheral contact on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Regarding Claims 9 and 16, Lee '304, Nishi '430 and Lee '987 are shown to teach all the features of the claim with the exception of explicitly the features: "a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs".

However, it has been held to be within the general skill of a worker in the art to have a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Regarding Claim 11, Nishi '430 teaches a thickness of a spacer (74; [0113]) in the TAC is nominally identical to a thickness of a spacer (474; [0113]) in the peripheral contact.

Furthermore, it has been held to be within the general skill of a worker in the art to have a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220

USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Regarding Claim 12, Nishi '430 teaches the spacer of the TAC (74) and the spacer of the peripheral contact (274) comprise a same material (see para. [0111]-[0113]; and Figs. 9 and 10).

Furthermore, it has been held to be within the general skill of a worker in the art to have the spacer of the TAC and the spacer of the peripheral contact comprise a same material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claim 13, Nishi '430 teaches the same material comprises silicon oxide (see para. [0111]).

Furthermore, it has been held to be within the general skill of a worker in the art to have the material (e.g. silicon oxide) for the spacer of the TAC/peripheral contact on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claim 18, Nishi '430 teaches a thickness of a spacer (74; [0113]) in the TAC is nominally identical to a thickness of a spacer (474; [0113]) in the peripheral contact; and a

diameter of the TAC (Fig. 9, (79); [0086]) is at least equal to a diameter of the peripheral contact (479; [0086]).

Furthermore, it has been held to be within the general skill of a worker in the art to have a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

4. Claims 5-6, 14-15 and 20-21 are rejected under 35 U.S.C. 103 as being unpatentable over Lee '304, Nishi '430 and Lee '987 as applied to claim 1 above, and further in view of Pachamuthu (US 2015/0236038, hereinafter as Pacha '038).

Regarding Claims 5, 14 and 20, Nishi '430 teaches a lower memory deck on the substrate (see Fig. 1).

Thus, Lee '304, Nishi '430 and Lee '987 are shown to teach all the features of the claim with the exception of explicitly the features: "an upper memory deck above the lower memory deck".

However, Pacha '038 teaches an upper memory deck (Fig. 15, (232/242); [0099]) above the lower memory deck (Fig. 15, (132/146); [0099]).

Thus, it would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Lee '304, Nishi '430 and Lee '987 by having an upper memory deck above the lower memory deck in order to form a vertical stack of multilevel memory arrays above a single substrate, with no intervening substrates (see para. [0001] and [0039]) as suggested by Pacha '038.

Regarding Claims 6, 15 and 21, Nishi '430 teaches a lower channel structure (730) extending vertically through the lower memory deck (see Fig. 23).

Furthermore, Pacha '038 teaches an upper channel structure (Fig. 32, (260); [0141]) extending vertically through the upper memory deck; and an inter-deck plug (doped semiconductor regions 163; [0140]) disposed vertically between and in contact with the lower channel structure and the upper channel structure.

Response to Arguments

5. Applicant's arguments with respect to claims 1-2 and 4-21, filed on 07/05/2022, have been considered but are moot in view of the new ground of rejection.

Interviews After Final

6. Applicants note that an interview after a final rejection is permitted in order to place the application in condition for allowance or to resolve issues prior to appeal. However, prior to the interview, the intended purpose and content of the interview should be presented briefly, preferably in writing. Upon review of the agenda, the Examiner may grant the interview if the examiner is convinced that disposal or clarification for appeal may be accomplished with only

nominal further consideration. Interviews merely to restate arguments of record or to discuss new limitations will be denied. See **MPEP § 714.13**

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

8. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Dzung Tran whose telephone number is (571) 270-3911. The examiner can normally be reached on M-F 8 AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Supervisor Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DZUNG TRAN/

Primary Examiner, Art Unit 2829

<i>Notice of References Cited</i>	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.	
	Examiner DZUNG T TRAN	Art Unit 2829	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20150348987-A1	12-2015	LEE; SUNG-HUN	H01L27/11582	257/326
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.
	Examiner DZUNG T TRAN	Art Unit 2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant					☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE								
Final	Original	04/04/2022	08/03/2022							
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	2	✓	✓							
	3	✓	-							
	4	✓	✓							
	5	✓	✓							
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<i>Search Notes</i> 	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.
	Examiner DZUNG T TRAN	Art Unit 2829

CPC - Searched*		
Symbol	Date	Examiner
H01L 27/11531; 21/76816; 21/76877; 23/5226	04/04/2022 (Updated on 08/01/2022)	DT

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

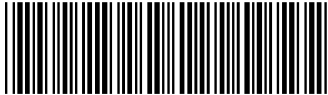
US Classification - Searched*			
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* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Conducted inventor name searching	04/04/2022 (Updated on 08/01/2022)	DT
Conducted assignee searching	04/04/2022 (Updated on 08/01/2022)	DT
Text searching	04/04/2022	DT
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Interference Search			
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<i>Search Notes</i> 	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.
	Examiner DZUNG T TRAN	Art Unit 2829

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PE2E SEARCH - Search History (Prior Art)

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Page 5 of 23

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L118	2197	L116 L117	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 12:09 PM
L119	5627	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/11/28 01:07 PM
L120	4301	L119 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 01:07 PM
L121	1929	L120 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 01:07 PM
L122	8	("20130264631" "20160099255" "20120280304" "20150206895" "20140175532" "20150179660" "20170125430" "20120119287").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 01:30 PM
L123	1	("20200161321").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 01:31 PM
L124	3	L122 and dummy	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:19 PM
L125	6821	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/11/28 02:33 PM
L126	4604	L125 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:33 PM
L127	2431	L126 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:33 PM
L128	1975	L127 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:33 PM
L129	1	(14/133979).APP.	(USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:37 PM
L130	72	("20070210338" "20070252201" "20090230449" "20090230454" "20090242967" "20100044778" "20100112769" "20100120214" "20100155810" "20100155818" "20100181610" "20100207195" "20100320528" "20110076819" "20110133606" "20110266606" "20110303970" "20120001247" "20120001249" "20120001250" "20120012920"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:37 PM

L131	85	"20120032245" "20120208347" "20130089974" "20130264631" "7005350" "7023739" "7177191" "7221588" "7233522" "7514321" "7575973" "7696559" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8394716").PN. OR ("9449983").URPN. ("10008570" "10121794" "10553599" "10559588" "20030047755" "20030122204" "20030155582" "20030219933" "20040041192" "20040063286" "20040125629" "20040251488" "20050062098" "20080012065" "20090321855" "20100109071" "20110045657" "20110287612" "20120023894" "20120068247" "20120276702" "20130009236" "20130089974" "20130134492" "20140225160" "20140225181" "20140264525" "20150129954" "20150179660" "20160049421" "20160099250" "20160118391" "20160141294" "20160181264" "20160260733" "20160358933" "20170062454" "20170110464" "20170110470" "20170162591" "20170229472" "20170338243" "20170365613" "20180122906"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:47 PM
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L132	72	"20190252405" "20190326313" "5915167" "6274490" "6372569" "6677213" "6777274" "6833306" "6881994" "7005350" "7012299" "7202119" "8187936" "8829593" "8884357" "8946023" "9023719" "9136130" "9177966" "9230980" "9230987" "9305932" "9331093" "9356031" "9425299" "9449980" "9449983" "9460931" "9478495" "9502471" "9570463" "9576975" "9627395" "9627403" "9691884" "9698153" "9728551" "9780108" "9853043" "9876025" "9941295").PN. OR ("10797060").URPN. ("10115735" "10355017" "20060157797" "20070155074" "20070210338" "20070252201" "20080096328" "20080116583" "20090230449" "20090242967" "20100044778" "20100090286" "20100112769" "20100120214" "20100155810" "20100155818" "20100181610" "20100207195" "20100320528" "20110076819" "20110133606" "20110233688" "20110266606" "20120001247" "20120001249" "20120001250" "20120012920" "20120119287" "20120168877" "20120261756" "20120280290" "20130140669" "20130161746" "20130181264" "20130217190"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:47 PM
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		"20130264631" "20130320417" "20140117421" "20140154846" "20150008520" "20150206945" "20150214058" "20150364490" "20160163702" "20160260712" "20160351709" "20180331118" "5915167" "6319782" "6323525" "7005350" "7023739" "7177191" "7221588" "7233522" "7514321" "7575973" "7696559" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8394716" "9023719" "9305934" "9449983" "9460931" "9601503" "9859422").PN. OR ("10770459").URPN.					
L133	0	(15/873101).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 04:55 PM
L134	10	("6169019" "201701333 98" "5945350" "201603 51709" "20030190497" "5576579" "5942799" "6 229211" "20180040476 " "5847463" "6268299" " 20180245215" "200600 84247" "5874353" "201 50138862" "200300252 06" "20020140103" "20 030194859").PN.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 04:57 PM
L135	1	("20180331118").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 04:59 PM
L136	1	(15/080269).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 05:01 PM
L137	1	("20160204117").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 05:02 PM
L138	1	(14/862916).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 05:03 PM
L139	1	("20160322381").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 05:03 PM
L140	1	(14/611785).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 05:04 PM
L141	1	("20150236038").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 05:04 PM
L142	14	(US-20170125430-\$ or US-20150179660-\$ or	(US-PGPUB; USPAT)	OR	OFF	OFF	2020/11/30 10:31 AM

		US-20180122906-\$ or US-20120119287-\$ or US-20170062454-\$ or US-20180331118-\$ or US-20160204117-\$ or US-20160322381-\$ or US-20150236038-\$.did. or (US-8664761-\$ or US-9449987-\$ or US-10453798-\$ or US- 9806093-\$ or US- 10381322-\$).did.					
L143	2	((("20120280304") or ("20200161321")).PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2021/01/29 01:50 PM
L144	220	((("GUO") near3 ("Mei") near3 ("Lan")) OR (("HU") near3 ("Yushi")) OR (("XIA") near3 ("Ji")) OR (("ZHU") near3 ("Hongbin"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2021/03/04 10:34 AM
L145	1549	(257/315).CCLS.	(US-PGPUB)	OR	ON	ON	2021/03/04 10:34 AM
L146	1326	(257/314).CCLS.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 10:38 AM
L147	1027	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:25 AM
L148	1027	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:25 AM
L149	3337	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 11:32 AM
L150	2461	L149 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:32 AM
L151	1249	L150 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:32 AM
L152	5796	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 11:46 AM
L153	4304	L152 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:46 AM
L154	1932	L153 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:47 AM
L155	7132	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 01:26 PM
L156	4606	L155 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 01:26 PM
L157	2161	L156 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 01:26 PM
L158	0	H01L23/5283.CPC1	(US-PGPUB)	OR	OFF	OFF	2021/03/04 01:27 PM
L159	2521	H01L23/5283.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 01:27 PM
L160	1622	L159 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 01:29 PM

L161	3255	H01L27/11524.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 02:19 PM
L162	2481	L161 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:19 PM
L163	2468	L162 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:19 PM
L164	1852	L163 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:20 PM
L165	2019	H01L27/11529.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:20 PM
L166	5634	H01L27/11556.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:59 PM
L167	3084	H01L27/11556.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 02:59 PM
L168	1760	L167 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:00 PM
L169	3129	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 03:05 PM
L170	1803	L169 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:08 PM
L171	2336	H01L27/11573.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 03:45 PM
L172	1379	L171 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:45 PM
L173	5703	H01L27/11582.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 03:46 PM
L174	3326	L173 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L175	3286	L174 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L176	3067	L175 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L177	2423	L176 and (hole recess\$3)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L178	2354	L177 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:47 PM
L179	2251	L178 and (word data)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:47 PM
L180	1	("20120098048").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2021/03/04 04:48 PM
L181	303	((("GUO") near3 ("Mei") near3 ("Lan")) OR ("HU") near3 ("Yushi")) OR ("XIA") near3 ("Ji")) OR ("ZHU") near3 ("Hongbin"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/04/04 06:59 AM
L182	99	L181 AND (("YANGTZE MEMORY TECHNOLOGIES CO LTD.".ase. OR "MICRON	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/04/04 07:50 AM

		TECHNOLOGY, INC.".ase. OR "INTEL CORPORATION".ase. OR "WUXI PETABYTE TECHNOLOGIES CO LTD.".ase. OR "DELTA ELECTRONICS (SHANGHAI) CO LTD.".ase. OR "EMAGIN CORPORATION".ase. OR "AUBURN UNIVERSITY".ase. OR "INTEL CORPORATINO".ase. OR "SHENZHEN JIUHU TECHNOLOGY CO LIMITED".ase. OR "SHENZHEN JIUHU TECHNOLOGY CO LTD".ase.))					
L183	10019	257/314	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/04/04 07:51 AM
L184	8823	L183 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 07:52 AM
L185	919	L184 AND (bit nlearine)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 07:52 AM
L186	727	L184 AND (bit NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 07:52 AM
L187	569	H01L27/11531.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/04/04 08:25 AM
L188	1105	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:25 AM
L189	7192	H01L21/76816.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:40 AM
L190	4750	L189 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:40 AM
L191	472	L190 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 08:41 AM
L192	13	("20180331118" "20130264631" "20160099255" "20170062454" "20120280304" "20150179660" "20150206895" "20150236038" "20160322381" "20120119287" "20140175532" "20170125430" "20170179152").P N.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:54 AM
L193	1	"20210104531"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:59 AM
L194	2	"20120280304"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 09:03 AM
L195	12904	H01L21/76877.CPC.	(US-PGPUB; USPAT;	OR	OFF	OFF	2022/04/04

L196	8763	L195 AND @pd<"20180914"	USOCR) (US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	10:00 AM 2022/04/04 10:00 AM
L197	521	L196 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:00 AM
L198	361	H01L23/52.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:26 AM
L199	8494	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:26 AM
L200	8997	L199 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 10:26 AM
L201	601	L200 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:27 AM
L202	13	("20180331118" "20130 264631" "20160099255 " "20170062454" "2012 0280304" "2015017966 0" "20150206895" "201 50236038" "201603223 81" "20120119287" "20 140175532" "20170125 430" "20170179152").P N.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:18 AM
L203	1	(14/862916).APP.	(USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:20 AM
L204	135	("5387530" "5915167" "7177191" "7221588" "7233522" "7514321" "7575973" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8193054" "8198672" "8349681" "8394716" "8445347" "8450181" "8614126" "8658499" "8741761" "8828884" "8847302" "8878278" "8884357" "8928061" "8946023" "9023719" "9230979" "9437606" "20060003531" "20060258076" "20070210338" "20070252201" "20080067583" "20080169496" "20090026561" "20090121271" "20090242967" "20100044778" "20100059811" "20100112769" "20100120214" "20100133599"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:20 AM

		"20100155810" "20100155818" "20100171162" "20100181610" "20100207195" "20100213458" "20100320528" "20110065270" "20110076819" "20110133606" "20110151667" "20110266606" "20110287612" "20110312174" "20120001247" "20120001249" "20120003800" "20120003831" "20120052674" "20120061744" "20120068242" "20120074367" "20120119287" "20120140562" "20120153376" "20120208347" "20120256247" "20120261638" "20120261722" "20120276719" "20130248974" "20130264631" "20130313627" "20130313717" "20130322174" "20140225181" "20140264525" "20140264533" "20140264542" "20140273373" "20150076580" "20150179660" "20150348984" "20160049423" "20160163728" "20160276359").pn. OR ("9627403").urpn. AND (PGPB USPT USOC).dbnm.					
L205	23	"10304852"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:28 AM
L206	14	("9812464" "10304852" "10319635" "20160118399" "20170012052" "20170047343"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:29 AM

		"20170084696" "20170179154" "20170358593" "20180151587" "20190067316" "20190164991").pn. OR ("10573659").urpn. AND (PGPB USPT USOC).dbnm.					
L207	312	((("GUO") near3 ("Mei") near3 ("Lan")) OR (("HU") near3 ("Yushi")) OR (("XIA") near3 ("Ji")) OR (("ZHU") near3 ("Hongbin"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/08/01 09:38 AM
L208	101	L207 AND (("YANGTZE MEMORY TECHNOLOGIES CO LTD.").ase. OR "MICRON TECHNOLOGY, INC.".ase. OR "INTEL CORPORATION".ase. OR "WUXI PETABYTE TECHNOLOGIES CO LTD.".ase. OR "DELTA ELECTRONICS (SHANGHAI) CO LTD.".ase. OR "EMAGIN CORPORATION".ase. OR "AUBURN UNIVERSITY".ase. OR "INTEL CORPORATINO".ase. OR "SHENZHEN JIUHU TECHNOLOGY CO LIMITED".ase. OR "SHENZHEN JIUHU TECHNOLOGY CO LTD".ase.))	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/08/01 09:43 AM
L209	1346	257/314	(US-PGPUB)	OR	ON	ON	2022/08/01 09:46 AM
L210	580	H01L27/11531.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 10:41 AM
L211	1126	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 10:41 AM
L212	6984	H01L27/11524.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 10:50 AM
L213	4633	L212 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 10:50 AM
L214	1812	L213 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 10:51 AM
L215	3900	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:22 AM

L216	2491	L215 AND @pd<"20180914"	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:22 AM
L217	473	L216 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:23 AM
L218	6635	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:31 AM
L219	8774	L218 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 11:31 AM
L220	521	L219 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:32 AM
L221	8876	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:54 AM
L222	9023	L221 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 11:54 AM
L223	602	L222 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:55 AM
L224	3387	H01L23/5283.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 12:33 PM
L225	3222	L224 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 12:34 PM
L226	196	L225 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 12:34 PM
L227	49	L225 AND (memory NEAR stack\$3)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 12:34 PM
L228	550	L225 AND (spacer dummy)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 12:35 PM
L229	663	L226 OR L227 OR L228	(US-PGPUB)	OR	OFF	OFF	2022/08/01 12:35 PM
L230	1383	H01L27/11529.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 01:11 PM
L231	1	"20210104531"	(US-PGPUB)	OR	OFF	OFF	2022/08/01 02:46 PM
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PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default	Plurals	British	Time Stamp
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08/01/2022 06:56:53 PM

Workspace: 17_100847_memory string

Page 22 of 23
DT

				Operator		Equivalents	
N63	1	(form\$3 near2 spacer near3 sidewall near3 first near open\$3) and (form\$3 near3 array ear contact near2 extend\$3 near vertically tnear3 dielectric near stack near3 conductor near layer near4 spacer near3 first near open\$3) and (after near form\$3 TAC near2 form\$3 near2 slit near extend\$3 near vertically near3 dielectric near stack).clm.	(USPAT)	OR	OFF	OFF	2019/12/18 03:52 PM
N181	0	(memory near stack\$3 near2 substrate near2 interleav\$3 near2 plurality near2 conduct\$3 near layers near2 dielectric near layers near4 plurality near2 conduct\$4 near layers near3 respect\$3 near shallow near recess) and (channel near structure near extend\$3 near vertically near2 memory near stack\$3).clm.	(USPAT)	OR	OFF	OFF	2021/03/04 03:21 PM

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17100847
	Filing Date	2020-11-21
	First Named Inventor	Mei Lan GUO
	Art Unit	2829
	Examiner Name	TRAN, DZUNG
	Attorney Docket Number	10018-01-0015-US-DIV2

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	1	20190355663	A1	2019-11-21	NISHIKAWA et al.		
	2	20190287982	A1	2019-09-19	HINOUE et al.		
	3	20170373079	A1	2017-12-28	SHARANGPANI et al.		
	4	20130164928	A1	2013-06-27	Lim et al.		
	5	20110049646	A1	2011-03-03	Lim et al.		
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17100847
Filing Date	2020-11-21
First Named Inventor	Mei Lan GUO
Art Unit	2829
Examiner Name	TRAN, DZUNG
Attorney Docket Number	10018-01-0015-US-DIV2

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		

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EXAMINER SIGNATURE

Examiner Signature	/DZUNG TRAN/	Date Considered	08/01/2022
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17100847
Filing Date	2020-11-21
First Named Inventor	Mei Lan GUO
Art Unit	2829
Examiner Name	TRAN, DZUNG
Attorney Docket Number	10018-01-0015-US-DIV2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2022-05-01
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/100,847	11/21/2020	Mei Lan Guo	10018-01-0015-US-DIV2	1008
153988	7590	09/06/2022	EXAMINER	
Bayes PLLC			TRAN, DZUNG	
8260 Greensboro Drive				
Suite 625				
McLean, VA 22102				
			ART UNIT	PAPER NUMBER
			2829	
			NOTIFICATION DATE	DELIVERY MODE
			09/06/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

<i>Applicant-Initiated Interview Summary</i>	Application No. 17/100,847	Applicant(s) Guo et al.		
	Examiner DZUNG T TRAN	Art Unit 2829	AIA (First Inventor to File) Status Yes	Page 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	Title	Type
DZUNG T TRAN	Primary Examiner	Telephonic
CHERY HUANG	Attorney	

Date of Interview: 29 August 2022

Issues Discussed:

Proposed Amendment(s)

A proposed amendment to claim 1 was discussed. The examiner agreed that the proposed amendments would overcome the current cited prior arts. Examiner will do further search when the amended claims are filed. No agreement as to allowability was reached during the interview

/DZUNG TRAN/ Primary Examiner, Art Unit 2829	
Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04 Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing	

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 17/100,847		Filing Date 11/21/2020		☐ To be Mailed			
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO											
APPLICATION AS FILED - PART I											
		(Column 1)		(Column 2)							
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		x \$100 =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		x \$480 =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL					
APPLICATION AS AMENDED - PART II											
		(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	09/22/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0			x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0			x \$480 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
								TOTAL ADD'L FEE		0	
		(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=			x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=			x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
								TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.								SLIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".								/APRIL L. WALKER/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".											
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Mei Lan GUO *et al.*

Confirmation No.: 1008

Applicant: YANGTZE MEMORY
TECHNOLOGIES CO. LTD.

Art Unit: 2829

Application No.: 17/100,847

Examiner: Dzung TRAN

Filing Date: November 21, 2020

Atty. Docket: 10018-01-0015-US-DIV2

Title: **THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY
CONTACTS AND METHODS FOR FORMING THE SAME**

Amendment and Reply Under 37 C.F.R. § 1.116

Mail Stop AF

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

In reply to the Final Office Action dated August 8, 2022, and in view of the attached Request for Consideration under After Final Consideration Pilot Program (AFCP) 2.0, Applicant proposes that the above-identified application be amended in light of Applicant's remarks as follows:

Amendments to the Claims are reflected in the listing of claims of this paper.

Remarks and Arguments follow the Amendment section of this paper.

Attachment to this paper includes **an AFCP 2.0 Request**.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2227.

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0		
Practitioner Docket No.: 10018-01-0015-US-DIV2	Application No.: 17/100,847	Filing Date: November 21, 2020
First Named Inventor: Mei Lan GUO	Title: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME	
APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116. 1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (e.g., a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c). 2. The above-identified application contains an outstanding final rejection. 3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect. 4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection. 5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response. 6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web). 7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, e.g., extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.] 8. By filing this certification and request, applicant acknowledges the following: • Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0. • The examiner will verify that the AFCP 2.0 submission is compliant, i.e., that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions: ○ The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, e.g., by mailing an advisory action. ○ If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview. ▪ The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate. ▪ If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.		
Signature /Ching-Ling Huang/	Date 2022/09/22	
Name (Print/Typed) Ching-Ling Huang	Practitioner Registration No. 62,003	
Note: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.		
☐ * Total of _____ forms are submitted.		

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Mei Lan GUO *et al.*

Confirmation No.: 1008

Applicant: YANGTZE MEMORY
TECHNOLOGIES CO. LTD.

Art Unit: 2829

Application No.: 17/100,847

Examiner: Dzung TRAN

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Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A three-dimensional (3D) memory device, comprising:
 - a substrate;
 - a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;
 - a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;
 - a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate; and
~~a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; and~~
a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones
~~a peripheral contact in contact with a peripheral device,~~
~~wherein a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact.~~
2. (Currently Amended) The 3D memory device of claim 1, further comprising:
[[the]] a peripheral device on the substrate, [[the]] a peripheral contact being arranged outside of the memory stack and in contact with the peripheral device.
3. (Canceled)
4. (Currently Amended) The 3D memory device of claim 2, further comprising:
a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack, wherein each of the dielectric layer in the dummy channel structure, [[the]] a spacer in the TAC, and [[the]] a spacer in the peripheral contact comprises silicon oxide.

5. (Original) The 3D memory device of claim 1, wherein the memory stack comprises:
a lower memory deck on the substrate; and
an upper memory deck above the lower memory deck.
6. (Original) The 3D memory device of claim 5, wherein the channel structure comprises:
a lower channel structure extending vertically through the lower memory deck;
an upper channel structure extending vertically through the upper memory deck; and
an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.
7. (Currently Amended) The 3D memory device of claim 1, further comprising:
a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; and
a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate,
wherein:
a diameter of the TAC is at least equal to a diameter of the peripheral contact; and
a diameter of the dummy channel structure is smaller than each of a diameter of the TAC and a diameter of the peripheral contact.
8. (Canceled)
9. (Previously Presented) The 3D memory device of claim 1, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.
10. (Currently Amended) A three-dimensional (3D) memory device, comprising:

a substrate;
a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;
a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack; and
a through array contact (TAC) comprising a substantially circular section and extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate[[;]]
~~a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; and~~
~~a peripheral contact in contact with a peripheral device;~~
~~wherein:~~
~~a diameter of the TAC is at least equal to a diameter of the peripheral contact; and~~
~~a diameter of the dummy channel structure is smaller than each of the diameter of the TAC and the diameter of the peripheral contact.~~

11. (Currently Amended) The 3D memory device of claim 10, further comprising:
a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate;

wherein a thickness of [[a]] the spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact.

12. (Previously Presented) The 3D memory device of claim 11, wherein the spacer of the TAC and the spacer of the peripheral contact comprise a same material.

13. (Canceled)

14. (Previously Presented) The 3D memory device of claim 10, wherein the memory stack comprises:

a lower memory deck on the substrate; and
an upper memory deck above the lower memory deck.

15. (Previously Presented) The 3D memory device of claim 14, wherein the channel structure comprises:

a lower channel structure extending vertically through the lower memory deck;
an upper channel structure extending vertically through the upper memory deck; and
an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.

16. (Previously Presented) The 3D memory device of claim 10, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.

17. (Currently Amended) A three-dimensional (3D) memory device, comprising:
a substrate;
a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;
a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;
a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a substantially circular section; and
a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,
wherein:
a first diameter lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs; and

a peripheral contact is arranged outside the memory stack and in contact with a peripheral device on the substrate.

18. (Currently Amended) The 3D memory device of claim 17, ~~further comprising: a peripheral contact in contact with a peripheral device~~, wherein:

a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact; and

a diameter of the TAC is at least equal to a diameter of the peripheral contact.

19. (Previously Presented) The 3D memory device of claim 18, wherein:

a diameter of the dummy channel structure is smaller than each of the diameter of the TAC and the diameter of the peripheral contact.

20. (Previously Presented) The 3D memory device of claim 17, wherein the memory stack comprises:

a lower memory deck on the substrate; and

an upper memory deck above the lower memory deck.

21. (Previously Presented) The 3D memory device of claim 20, wherein the channel structure comprises:

a lower channel structure extending vertically through the lower memory deck;

an upper channel structure extending vertically through the upper memory deck; and

an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.

22. (New) The 3D memory device of claim 1, wherein:

the TAC has a substantially circular section and comprises a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC.

23. (New) The 3D memory device of claim 17, wherein:

the TAC comprises a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendments, claims 1, 2, 4-7, 9-12, and 14-23 are pending in the application, with claims 1, 10, and 17 being independent claims. Applicant hereby proposes to amend claims 1, 2, 4, 7, 10-12, 17, and 18; and proposes to add new claims 22 and 23. These changes introduce no new matter, and their entry is respectfully requested. Support for the amendments and the new claims may be found throughout the application as filed, including the original claims and paragraphs [0043]-[0046] of the original specification.

Further, by this Amendment, claims 8 and 13 are canceled without prejudice to or disclaimer of the subject matter thereof.

Throughout the arguments, Applicant reminds the Examiner that the claims are given their broadest reasonable meaning in view of the specification, and any paraphrasing of the claim features is not to be interpreted as reading any features into, or characterizing of, the claims.

Based on the above amendments and the following remarks, Applicant respectfully requests that the Examiner reconsider and withdraw both outstanding rejections.

Examiner Interview

Applicant appreciates the courtesies extended to Applicant's representative, Ching-Ling Huang (Reg. No. 62,003), by the Examiner in the telephonic interview on August 29, 2022. During the interview, the parties discussed the rejections under 35 U.S.C. § 103, the independent claims, and the applied references. Applicant also thanks for the Examiner's agreement that the proposed amendments to claims 1 and 17, as reflected in this Amendment and Reply, would all overcome the applied references.

Rejections under 35 U.S.C. § 103

In the outstanding Final Office Action, claims 1, 2, 4, 7-13, and 16-19 were rejected under 35 U.S.C. § 103 as allegedly being unpatentable over U.S. Patent Appl. Pub. No. 2012/0280304 ("*Lee '304*") in view of U.S. Patent Appl. Pub. No. 2017/0125430 ("*Nishikawa*"), and further in view of U.S. Patent Appl. Pub. No. 2015/0348987 ("*Lee '987*"); and claims 5, 6, 14, 15, 20, and 21 were rejected under 35 U.S.C. § 103 as allegedly being unpatentable over *Lee '304* in view of

Atty. Dkt. No. 10018-01-0015-US-DIV2

Nishikawa and *Lee* '987, and further in view of U.S. Patent Appl. Pub. No. 2015/0236038 ("*Pachamuthu*").

Applicant respectfully traverses the rejections and submits that no *prima facie* case of obviousness has been established.

For example, independent claim 1, as proposed to be amended, recites a 3D memory device including, e.g., "a through array contact (TAC) extending vertically through [] conductor/dielectric layer pairs in [a] memory stack and buried into [a] substrate," and "a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones," (emphases added).

Lee '304, *Nishikawa*, *Lee* '987, and *Pachamuthu*, whether taken alone or in any combination, do not disclose or suggest at least the above-quoted elements. In particular, during the interview discussion, the Examiner agreed with this viewpoint. *See also* Applicant-Initiated Interview Summary dated September 6, 2022.

Further, independent claim 17, as proposed to be amended, recites a 3D memory device including, e.g., "a through array contact (TAC) extending vertically through [] conductor/dielectric layer pairs in [a] memory stack and buried into [a] substrate, the TAC comprising a substantially circular section," where: "a first diameter of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs," and "a peripheral contact is arranged outside the memory stack and in contact with a peripheral device on the substrate." The applied references, whether taken alone or in any combination, do not disclose or suggest at least these elements.

During the interview discussion, the Examiner also agreed with this viewpoint. *See also id.* *Lee* '304 at least does not disclose or suggest the claimed "TAC" that is buried into the substrate. As a result, the Examiner turned to *Nishikawa* for compensation and asserted that the opening 79 of *Nishikawa* corresponds to the claimed "TAC." Final Office Action at 2 and 7. However, FIG. 6 of *Nishikawa* shows that the opening 79 is a slit. That is, *Nishikawa* does not disclose or suggest "a through array contact (TAC) extending vertically through [] conductor/dielectric layer pairs in [a] memory stack and buried into [a] substrate, the TAC comprising a substantially circular section," as recited in amended independent 17 (emphases added) and thus fails to cure the deficiencies of *Lee* '304.

As to the element in claim 17 regarding “a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs,” the Examiner contended that “the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device, and thus “it has been held to be within the general skill of a worker in the art.” Final Office Action at 8. However, this is not correct, at least for the reason that the original specification clearly explains that “[a] plurality of shallow recesses 312 can then be formed along the sidewall of TAC hole 304... The sacrificial layer partial removal process can provide space for a thicker dielectric layer deposition in the next step.” Original specification, ¶[0066] (emphasis added). In view of the above, this claimed element in claim 17 should be properly considered for its patentable weight and thus the Examiner’s rejection is not proper. Therefore, amended independent claim 17 is allowable.

Further, by this Amendment, Applicant also proposes to amend independent claim 10 to recite, e.g., “a through array contact (TAC) comprising a substantially circular section and extending vertically through [] conductor/dielectric layer pairs in [a] memory stack and buried into [a] substrate,” where “the TAC compris[es] a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate.” *Lee ’304*, *Nishikawa*, *Lee ’987*, and *Pachamuthu* are also silent about these features.

In the rejection of independent claim 10, the Examiner appeared to assert that the common source line 170 of *Lee ’304* corresponds to the claimed “TAC.” Final Office Action at 5. However, as discussed above, the common source line 170 of *Lee ’304* does not show the features that “a through array contact (TAC) comprising a substantially circular section and extending vertically through [] conductor/dielectric layer pairs in [a] memory stack and buried into [a] substrate,” where “the TAC comprising a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate,” as recited in amended claim 10 (emphases added). That is, independent claim 10 is also allowable.

Dependent claims 2, 4-7, 9, 11, 12, 14-16, and 18-21 are also allowable at least by virtue of their dependence upon base claim 1, 10, or 17. Claims 8 and 13 are canceled, rendering their rejection moot.

Accordingly, Applicant respectfully requests withdrawal of the rejections of claims 1, 2, and 4-21 under 35 U.S.C. § 103.

New Claims

By this Amendment, Applicant proposes to add new claims 22 and 23 that depend upon claims 1 and 17, respectively, to address other aspects of the instant application.

New claims 22 and 23 are also allowable at least by virtue of their dependence upon claim 1 or 17.

Therefore, Applicant respectfully requests that the Examiner would allow new claims 22 and 23, together with the other pending claims, in the next official communication.

Conclusion

All of the stated grounds of the rejections in the Final Office Action have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw the presently outstanding rejections. Applicant believes that a full and complete reply has been made to the outstanding Final Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

BAYES PLLC

/Ching-Ling Huang/

Ching-Ling Huang
Agent for Applicant
Registration No. 62,003

Date: September 22, 2022

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McLean, VA 22102
(703) 995-9887

Electronic Acknowledgement Receipt	
EFS ID:	46673109
Application Number:	17100847
International Application Number:	
Confirmation Number:	1008
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Ching-Ling Huang/Anna O'Connor
Filer Authorized By:	Ching-Ling Huang
Attorney Docket Number:	10018-01-0015-US-DIV2
Receipt Date:	22-SEP-2022
Filing Date:	21-NOV-2020
Time Stamp:	15:03:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	After Final Consideration Program Request	10018-01-0015-US-DIV2_AFCP.pdf	226432	no	2
			00ea1b338e876ca400f94bcf9e36d826dd8807a4		
Warnings:					

Information:					
2		2018-00113-YMTC-PCT-US-DV1-DV1_AmendmentFOAofAugust 8_2022_10018-01-0015-US-DIV2_signed.pdf	296351 b894f7be1bede5e436edba280ae891cbf6c e8b74	yes	12
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Response After Final Action		1	1	
	Claims		2	7	
	Applicant Arguments/Remarks Made in an Amendment		8	12	
Warnings:					
Information:					
Total Files Size (in bytes):			522783		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/100,847	11/21/2020	Mei Lan Guo	10018-01-0015-US-DIV2	1008
153988	7590	09/30/2022	EXAMINER	
Bayes PLLC			TRAN, DZUNG	
8260 Greensboro Drive				
Suite 625				
McLean, VA 22102				
			ART UNIT	PAPER NUMBER
			2829	
			NOTIFICATION DATE	DELIVERY MODE
			09/30/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

Advisory Action Before the Filing of an Appeal Brief	Application No. 17/100,847	Applicant(s) Guo et al.	
	Examiner DZUNG T TRAN	Art Unit 2829	AIA (FITF) Status Yes

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 22 September 2022 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:

a) ☐ The period for reply expires ____ months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires ____ months from the mailing date of the prior Advisory Action or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANTS FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because

a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);

b) ☐ They raise the issue of new matter (see NOTE below);

c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See Continuation Sheet (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____

9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____

13. ☐ Note the attached Information *Disclosure Statement(s)*. (PTO/SB/08) Paper No(s). _____

14. ☒ Other: Form PTO-2323 is attached.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____

Claim(s) objected to: _____

Claim(s) rejected: 1-2 and 4-21

Claim(s) withdrawn from consideration: _____

/DZUNG TRAN/ Primary Examiner, Art Unit 2829	
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Continuation of 3: Applicant's request for entry into AFCP 2.0, filed on 09/22/2022, is acknowledged, but is denied because the response cannot be reviewed and a search conducted in the limited amount of time authorized for this pilot program. Therefore, the response is being reviewed under pre-pilot practice.

AFCP 2.0 Decision

Application No.

17/100,847

Applicant(s)

Guo et al.

Examiner

DZUNG T TRAN

Art Unit

2829

AIA (FITF) Status

Yes

This is in response to the After Final Consideration Pilot request filed 22 September 2022.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

- ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.
- ☐ A non-broadening amendment to at least one independent claim was not submitted.
- ☐ The request is not the first proper AFCP 2.0 request submitted in response to the most recent final rejection.
- ☐ Other: _____

2. Proper Request

- A. After final amendment submitted with the request will not be treated under AFCP 2.0.

The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

- ☒ The after final amendment will be treated under pre-pilot procedure.

- B. Updated search and/or completed additional consideration.

The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

- ☐ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.
- ☐ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action. See attached interview summary for further details.
- ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.
- ☐ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.
- ☐ 5. Other: _____

Examiner Note: Please attach an interview summary when necessary as described above.

DO NOT ENTER: /D.T/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Mei Lan GUO *et al.*

Confirmation No.: 1008

Applicant: YANGTZE MEMORY
TECHNOLOGIES CO. LTD.

Art Unit: 2829

Application No.: 17/100,847

Examiner: Dzung TRAN

Filing Date: November 21, 2020

Atty. Docket: 10018-01-0015-US-DIV2

Title: **THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY
CONTACTS AND METHODS FOR FORMING THE SAME**

Amendment and Reply Under 37 C.F.R. § 1.116

Mail Stop AF

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

In reply to the Final Office Action dated August 8, 2022, and in view of the attached Request for Consideration under After Final Consideration Pilot Program (AFCP) 2.0, Applicant proposes that the above-identified application be amended in light of Applicant's remarks as follows:

Amendments to the Claims are reflected in the listing of claims of this paper.

Remarks and Arguments follow the Amendment section of this paper.

Attachment to this paper includes **an AFCP 2.0 Request**.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2227.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 17/100,847		Filing Date 11/21/2020		☐ To be Mailed			
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO											
APPLICATION AS FILED - PART I											
		(Column 1)		(Column 2)							
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		x \$100 =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		x \$480 =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL					
APPLICATION AS AMENDED - PART II											
		(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	09/30/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0			x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0			x \$480 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
								TOTAL ADD'L FEE		0	
		(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=			x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=			x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
								TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.								LIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".								/AMANDA N FORD/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".											
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL **(Submitted Only via EFS-Web)**

Application Number	17/100,847	Filing Date	2020-11-21	Docket Number (if applicable)	10018-01-0015-US-DIV2	Art Unit	2829
First Named Inventor	Mei Lan Guo			Examiner Name	Dzung TRAN		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, to any international application that does not comply with the requirements of 35 U.S.C. 371, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV.

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☐ Enclosed

☐ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____.
 (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
 The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
 Deposit Account No 602227

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature
 Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-14)

Approved for use through 07/31/2016. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	CHING-LING HUANG/	Date (YYYY-MM-DD)	2022-09-30
Name	CHING-LING HUANG	Registration Number	62003

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		17100847		
Filing Date:		21-Nov-2020		
Title of Invention:		THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		
First Named Inventor/Applicant Name:		Mei Lan Guo		
Filer:		Ching-Ling Huang/Anna O'Connor		
Attorney Docket Number:		10018-01-0015-US-DIV2		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description		Fee Code	Quantity	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1360	1360
Total in USD (\$)				1360

Electronic Acknowledgement Receipt	
EFS ID:	46736170
Application Number:	17100847
International Application Number:	
Confirmation Number:	1008
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Ching-Ling Huang/Anna O'Connor
Filer Authorized By:	Ching-Ling Huang
Attorney Docket Number:	10018-01-0015-US-DIV2
Receipt Date:	30-SEP-2022
Filing Date:	21-NOV-2020
Time Stamp:	18:26:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1360
RAM confirmation Number	E20229TI26324793
Deposit Account	602227
Authorized User	Anna O'Connor
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	17100847_RCE_form10018-01-0015-US-DIV2_signed.pdf	1349914	no	3
			6a4c3f76ff725d97c6c15e601fbf858e9671568		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37792	no	2
			5684cac6a2459edd8b944167bb117aa549da1ea9		
Warnings:					
Information:					
Total Files Size (in bytes):			1387706		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

153988 7590 10/12/2022
Bayes PLLC
8260 Greensboro Drive
Suite 625
McLean, VA 22102

EXAMINER	
TRAN, DZUNG	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 10/12/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/100,847	11/21/2020	Mei Lan Guo	10018-01-0015-US-DIV2	1008

TITLE OF INVENTION: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	01/12/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

153988 7590 10/12/2022
Bayes PLLC
8260 Greensboro Drive
Suite 625
McLean, VA 22102

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/100,847	11/21/2020	Mei Lan Guo	10018-01-0015-US-DIV2	1008

TITLE OF INVENTION: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	01/12/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, DZUNG	2829	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/100,847	11/21/2020	Mei Lan Guo	10018-01-0015-US-DIV2	1008
153988	7590	10/12/2022	EXAMINER	
Bayes PLLC 8260 Greensboro Drive Suite 625 McLean, VA 22102			TRAN, DZUNG	
			ART UNIT	PAPER NUMBER
			2829	
DATE MAILED: 10/12/2022				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/100,847	Applicant(s) Guo et al.	
	Examiner DZUNG T TRAN	Art Unit 2829	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 09/22/2022.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are See Continuation Sheet. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☒ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☒ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	

/DZUNG TRAN/ Primary Examiner, Art Unit 2829	
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Continuation of 3. The allowed claim(s) is/are: 1-2,4-7,9-12 and 14-23

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Request for Continued Examination

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/30/2022 has been entered.

DETAILED ACTION

Response to Amendment

1. This office action is in response to Amendment filed on 09/22/2022.
Claims 1-2, 4, 7, 10-11, 17 and 18 have been amended.
Claims 3, 8 and 13 have been cancelled.
New Claims 22-23 have been added.

Response to Arguments/Reason

2. Applicant's arguments, with regards to claims 1-2, 4-7, 9-12, 14-21 and new claims 22-23, filed on 09/22/2022 have been fully considered and they are persuasive. Particularly, on pages 8-11 of the Applicant's Response, applicants argued that Lee '034, Nishi '430 and Lee '987 do not disclose the limitations of independent claim including: "a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and

buried into the substrate”; and “a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones”. The Examiner finds the arguments are persuasive. Therefore, the Examiner made decision to allow these limitations over the prior art of record.

Allowable Subject Matter

3. Claims 1-2, 4-7, 9-12, 14-22 and 23 are allowed.
4. The following is an examiner’s statement of reasons for allowance: the whole application meets all formal and substantive requirements and the language of the claims is enabled by, and finds adequate descriptive support in, the application disclosure as originally filed. Concerning 35 U.S.C. § 102 and § 103 requirements, the application meets all requirements.
5. Regarding claim 1, the known prior art does not teach the claim as a whole. In particular, the prior art does not disclose or fairly suggest the limitations: “a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate”; and “a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones” in combination with the remaining limitations called for in claim 1.
6. None of the prior art on record contains such a limitation, nor given the prior art on record is it obvious to one of ordinary skill in the art to add said limitations as called for in claim 1. Therefore, claim 1 is allowed as it is not anticipated by or obvious over the teachings of the prior art on record. Furthermore, claims 1-2, 4-7 and 9 are also allowed as they depend from an allowed base claim.

7. Regarding claims 10 and 17, the known prior art does not teach the claim as a whole. In particular, the prior art does not disclose or fairly suggest the limitations: “a through array contact (TAC) comprising a substantially circular section and extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate” in combination with the remaining limitations called for in claims 10 and 17.

8. None of the prior art on record contains such a limitation, nor given the prior art on record is it obvious to one of ordinary skill in the art to add said limitations as called for in claims 10 and 17. Therefore, claims 10 and 17 are allowed as it is not anticipated by or obvious over the teachings of the prior art on record. Furthermore, claims 11-12, 14-16 and 18-23 are also allowed as they depend from the allowed bases claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

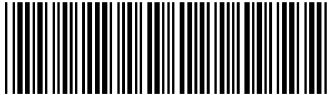
Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DZUNG T TRAN whose telephone number is (571) 270-3911. The examiner can normally be reached on M-F 8 AM-5PM.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DZUNG TRAN/
Primary Examiner, Art Unit 2829

<i>Search Notes</i> 	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.
	Examiner DZUNG T TRAN	Art Unit 2829

CPC - Searched*		
Symbol	Date	Examiner
H01L 27/11531; 21/76816; 21/76877; 23/5226	04/04/2022 (Updated on 10/05/2022)	DT

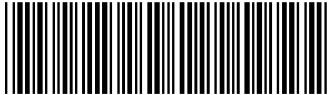
CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	314	04/04/2022 (Updated on 10/05/2022)	DT

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Conducted inventor name searching	04/04/2022 (Updated on 10/05/2022)	DT
Conducted assignee searching	04/04/2022 (Updated on 10/05/2022)	DT
Text searching	04/04/2022	DT
Text searching	08/01/2022	DT
Text searching	10/05/2022	DT

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<i>Search Notes</i> 	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.
	Examiner DZUNG T TRAN	Art Unit 2829

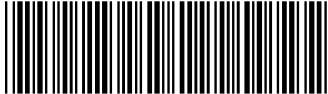
Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	Conducted interference key words searching	10/05/2022	DT

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<i>Index of Claims</i> 	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.
	Examiner DZUNG T TRAN	Art Unit 2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	04/04/2022	08/03/2022	10/05/2022						
1	1	✓	✓	=						
2	2	✓	✓	=						
	3	✓	-	-						
3	4	✓	✓	=						
4	5	✓	✓	=						
5	6	✓	✓	=						
6	7		✓	=						
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16	19		✓	=						
17	20		✓	=						
18	21		✓	=						
19	22			=						
20	23			=						

Issue Classification 	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.
	Examiner DZUNG T TRAN	Art Unit 2829

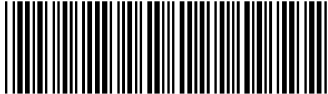
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H01L	/	23	/	5226	I	2013-01-01
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H01L	/	27	/	11573	I	2013-01-01
H01L	/	27	/	11582	I	2013-01-01

CPC Combination Sets					
Symbol				Type	Set
	/		/		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/DZUNG TRAN/ Primary Examiner, Art Unit 2829	05 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office

Part of Paper No.: 20221005

Issue Classification 	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.
	Examiner DZUNG T TRAN	Art Unit 2829

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L	/	27	/ 11524
NON-CLAIMED			
/		/	

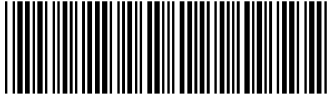
US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
257	314

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/DZUNG TRAN/ Primary Examiner, Art Unit 2829	05 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office

Part of Paper No.: 20221005

Issue Classification 	Application/Control No. 17/100,847	Applicant(s)/Patent Under Reexamination Guo et al.
	Examiner DZUNG T TRAN	Art Unit 2829

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	8	10	16	19										
2	2	9	11	17	20										
	3	10	12	18	21										
3	4		13	19	22										
4	5	11	14	20	23										
5	6	12	15												
6	7	13	16												
	8	14	17												
7	9	15	18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/DZUNG TRAN/ Primary Examiner, Art Unit 2829	05 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	2319	((("LIU") near3 ("Jun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2019/11/19 02:24 PM
L2	4485	(257/315).CCLS.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2019/11/19 02:25 PM
L3	4485	(257/315).CCLS.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2019/11/19 02:30 PM
L4	4483	L3 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:30 PM
L5	4240	L4 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:31 PM
L6	2125	L5 and (bit near line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:31 PM
L7	2319	((("LIU") near3 ("Jun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2019/11/19 02:45 PM
L8	1023	L7 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:45 PM
L9	8	L8 and (memory near stack)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:46 PM
L10	1	(12/262223).APP.	(USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:47 PM
L11	56	("20070132049" "20070229166" "20080151611" "20080165567" "5559425" "5680038" "6128214" "6493258" "6504750" "6724654" "6870755" "7433226").PN. OR ("7835173").URPN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 02:47 PM
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L13	4043	H01L27/11556.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 03:07 PM
L14	2171	H01L27/11556.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 03:07 PM
L15	2745	H01L27/11524.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 03:30 PM

L16	2472	L15 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 03:31 PM
L17	2461	L16 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 03:31 PM
L18	2355	L17 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 03:31 PM
L19	1775	L18 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 03:31 PM
L20	917	H01L27/11529.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 03:55 PM
L21	1694	H01L27/11529.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 03:55 PM
L22	931	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 04:21 PM
L23	1396	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR; JPO; DERWENT)	OR	OFF	OFF	2019/11/19 04:21 PM
L24	1396	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2019/11/19 04:21 PM
L25	1903	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2019/11/19 04:21 PM
L26	1759	H01L27/11548.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2019/11/19 04:22 PM
L27	8526	H01L27/1157.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2019/11/19 05:02 PM
L28	2355	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 05:03 PM
L29	1788	L28 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 05:03 PM
L30	2355	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 05:06 PM
L31	1741	H01L27/11573.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 05:06 PM
L32	1105	H01L27/11575.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 05:51 PM
L33	1971	H01L27/11575.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 05:51 PM
L34	7516	H01L27/11582.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 06:20 PM
L35	4196	H01L27/11582.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/19 06:20 PM
L36	3296	L35 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 06:20 PM
L37	3260	L36 and (memory	(US-PGPUB; USPAT;	OR	OFF	OFF	2019/11/19

L38	2337	string) L37 and (bit near line)	USOCR) (US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	06:20 PM 2019/11/19 06:20 PM
L39	1159	L38 and stack	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/19 06:21 PM
L40	1324	(257/314).CCLS.	(US-PGPUB)	OR	ON	ON	2019/11/20 06:10 AM
L41	142	((("GUO") near3 ("Mei") near3 ("Lan")) OR (("HU") near3 ("Yushi")) OR (("XIA") near3 ("Ji")) OR (("ZHU") near3 ("Hongbin"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2019/11/20 06:10 AM
L42	2770	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/20 06:19 AM
L43	2391	L42 and @pd<"20180821"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/20 06:19 AM
L44	4923	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/20 07:00 AM
L45	4252	L44 and @pd<"20180821"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/20 07:00 AM
L46	1826	L45 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/20 07:00 AM
L47	5604	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/20 07:49 AM
L48	4538	L47 and @pd<"20180821"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/20 07:49 AM
L49	2126	L48 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/11/20 07:49 AM
L50	1937	H01L23/5283.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/11/20 07:49 AM
L51	3	("20140175532" "20160 099255" "20170125430 ").PN.	(US-PGPUB; USPAT)	OR	OFF	OFF	2019/11/20 08:10 AM
L52	2775	H01L27/11524.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/12/18 10:42 AM
L53	2477	L52 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 10:42 AM
L54	2464	L53 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 10:42 AM
L55	2358	L54 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 11:00 AM
L56	925	H01L27/11529.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/12/18 11:01 AM
L57	1715	H01L27/11529.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 11:02 AM
L58	4129	H01L27/11556.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 12:06 PM
L59	2225	H01L27/11556.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/12/18 12:06 PM

L60	2407	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2019/12/18 12:06 PM
L61	1800	L60 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 12:07 PM
L62	6	("20140175532" "20160 099255" "20170125430 ").PN.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2019/12/18 03:05 PM
L64	1	("9449987").PN.	(USPAT; USOCR)	OR	OFF	OFF	2019/12/18 05:54 PM
L65	0	(14/995017).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2019/12/18 05:54 PM
L66	2	"14832579"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 05:55 PM
L67	1	("20170052258").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2019/12/18 05:57 PM
L68	0	(14/995017).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2019/12/18 06:12 PM
L69	72	("20070210338" "20070252201" "20090230449" "20090242967" "20100044778" "20100112769" "20100120214" "20100155810" "20100155818" "20100181610" "20100207195" "20100320528" "20110076819" "20110133606" "20110266606" "20120001247" "20120001249" "20120001250" "20120012920" "20120119287" "20130264631" "20140061849" "20140199815" "20150076584" "20150179660" "5915167" "7005350" "7023739" "7177191" "7221588" "7233522" "7514321" "7575973" "7696559" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8394716" "9023719" "9305934").PN. OR ("9449987").URPN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2019/12/18 06:13 PM
L70	1	("9449987").PN.	(USPAT; USOCR)	OR	OFF	OFF	2019/12/18 06:13 PM

L71	179	((("GUO") near3 ("Mei") near3 ("Lan")) OR ((("HU") near3 ("Yushi")) OR ((("XIA") near3 ("Ji")) OR ((("ZHU") near3 ("Hongbin")))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2020/06/18 08:41 AM
L72	1326	(257/314).CCLS.	(US-PGPUB)	OR	ON	ON	2020/06/18 08:43 AM
L73	2120	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2020/06/18 08:47 AM
L74	3081	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 09:16 AM
L75	2449	L74 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:16 AM
L76	753089	"55" and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:16 AM
L77	1242	L75 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:16 AM
L78	1033	L75 and (bit data)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:18 AM
L79	1421	L77 L78	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:18 AM
L80	5390	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 09:58 AM
L81	4301	L80 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:59 AM
L82	1852	L81 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 09:59 AM
L83	6379	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 09:59 AM
L84	4603	L83 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 10:00 AM
L85	2159	L84 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 10:00 AM
L86	2210	H01L23/5283.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 10:51 AM
L87	2984	H01L27/11524.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 10:52 AM
L88	2481	L87 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 10:53 AM
L89	2468	L88 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 10:53 AM
L90	2270	L89 and (bit data)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 10:53 AM
L91	990	H01L27/11529.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 12:01 PM
L92	1832	H01L27/11529.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 12:01 PM
L93	4636	H01L27/11556.CPC.	(US-PGPUB; USPAT;	OR	OFF	OFF	2020/06/18

10/05/2022 12:55:52 PM

Workspace: 17_100847_memory string

Page 5 of 30

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L94	2504	H01L27/11556.CPC.	USOCR) (US-PGPUB)	OR	OFF	OFF	12:01 PM 2020/06/18 12:02 PM
L95	1755	L94 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 12:02 PM
L96	0	H01L27/11557.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 12:53 PM
L97	2710	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 12:53 PM
L98	1803	L97 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/06/18 12:53 PM
L99	2006	H01L27/11573.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/06/18 12:54 PM
L100	5136	H01L27/11582.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/09/22 06:28 AM
L101	3325	L100 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/09/22 06:28 AM
L102	3285	L101 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/09/22 06:28 AM
L103	3067	L102 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/09/22 06:29 AM
L104	2215	L103 and (bit near line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/09/22 06:29 AM
L105	5	("20120119287" "20120 280304" "20130264631 " "20150179660" "2015 0206895").PN.	(US-PGPUB; USPAT)	OR	OFF	OFF	2020/11/28 11:07 AM
L106	2576	((("LIU") near3 ("Jun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2020/11/28 11:08 AM
L107	3495	(257/314).CCLS.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 11:08 AM
L108	3490	L107 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 11:09 AM
L109	3341	L108 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 11:09 AM
L110	2939	L109 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 11:09 AM
L111	1833537	6and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 11:09 AM
L112	1965	L110 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 11:09 AM
L113	2193	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2020/11/28 12:06 PM
L114	3229	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/11/28 12:09 PM
L115	2457	L114 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 12:09 PM

L116	1254	L115 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 12:09 PM
L117	2039	L115 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 12:09 PM
L118	2197	L116 L117	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 12:09 PM
L119	5627	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/11/28 01:07 PM
L120	4301	L119 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 01:07 PM
L121	1929	L120 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 01:07 PM
L122	8	("20130264631" "20160099255" "20120280304" "20150206895" "20140175532" "20150179660" "20170125430" "20120119287").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 01:30 PM
L123	1	("20200161321").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 01:31 PM
L124	3	L122 and dummy	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:19 PM
L125	6821	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2020/11/28 02:33 PM
L126	4604	L125 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:33 PM
L127	2431	L126 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:33 PM
L128	1975	L127 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 02:33 PM
L129	1	(14/133979).APP.	(USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:37 PM
L130	72	("20070210338" "20070252201" "20090230449" "20090230454" "20090242967" "20100044778" "20100112769" "20100120214" "20100155810" "20100155818" "20100181610" "20100207195" "20100320528" "20110076819" "20110133606" "20110266606" "20110303970" "20120001247" "20120001249" "20120001250" "20120012920"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:37 PM

L131	85	"20120032245" "20120208347" "20130089974" "20130264631" "7005350" "7023739" "7177191" "7221588" "7233522" "7514321" "7575973" "7696559" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8394716").PN. OR ("9449983").URPN. ("10008570" "10121794" "10553599" "10559588" "20030047755" "20030122204" "20030155582" "20030219933" "20040041192" "20040063286" "20040125629" "20040251488" "20050062098" "20080012065" "20090321855" "20100109071" "20110045657" "20110287612" "20120023894" "20120068247" "20120276702" "20130009236" "20130089974" "20130134492" "20140225160" "20140225181" "20140264525" "20150129954" "20150179660" "20160049421" "20160099250" "20160118391" "20160141294" "20160181264" "20160260733" "20160358933" "20170062454" "20170110464" "20170110470" "20170162591" "20170229472" "20170338243" "20170365613" "20180122906"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:47 PM
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L132	72	"20190252405" "20190326313" "5915167" "6274490" "6372569" "6677213" "6777274" "6833306" "6881994" "7005350" "7012299" "7202119" "8187936" "8829593" "8884357" "8946023" "9023719" "9136130" "9177966" "9230980" "9230987" "9305932" "9331093" "9356031" "9425299" "9449980" "9449983" "9460931" "9478495" "9502471" "9570463" "9576975" "9627395" "9627403" "9691884" "9698153" "9728551" "9780108" "9853043" "9876025" "9941295").PN. OR ("10797060").URPN. ("10115735" "10355017" "20060157797" "20070155074" "20070210338" "20070252201" "20080096328" "20080116583" "20090230449" "20090242967" "20100044778" "20100090286" "20100112769" "20100120214" "20100155810" "20100155818" "20100181610" "20100207195" "20100320528" "20110076819" "20110133606" "20110233688" "20110266606" "20120001247" "20120001249" "20120001250" "20120012920" "20120119287" "20120168877" "20120261756" "20120280290" "20130140669" "20130161746" "20130181264" "20130217190"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 04:47 PM
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		"20130264631" "20130320417" "20140117421" "20140154846" "20150008520" "20150206945" "20150214058" "20150364490" "20160163702" "20160260712" "20160351709" "20180331118" "5915167" "6319782" "6323525" "7005350" "7023739" "7177191" "7221588" "7233522" "7514321" "7575973" "7696559" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8394716" "9023719" "9305934" "9449983" "9460931" "9601503" "9859422").PN. OR ("10770459").URPN.					
L133	0	(15/873101).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 04:55 PM
L134	10	("6169019" "201701333 98" "5945350" "201603 51709" "20030190497" "5576579" "5942799" "6 229211" "20180040476 " "5847463" "6268299" " 20180245215" "200600 84247" "5874353" "201 50138862" "200300252 06" "20020140103" "20 030194859").PN.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 04:57 PM
L135	1	("20180331118").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 04:59 PM
L136	1	(15/080269).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 05:01 PM
L137	1	("20160204117").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 05:02 PM
L138	1	(14/862916).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 05:03 PM
L139	1	("20160322381").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/11/28 05:03 PM
L140	1	(14/611785).APP.	(US-PGPUB; USOCR)	OR	OFF	OFF	2020/11/28 05:04 PM
L141	1	("20150236038").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2020/11/28 05:04 PM
L142	14	(US-20170125430-\$ or US-20150179660-\$ or	(US-PGPUB; USPAT)	OR	OFF	OFF	2020/11/30 10:31 AM

		US-20180122906-\$ or US-20120119287-\$ or US-20170062454-\$ or US-20180331118-\$ or US-20160204117-\$ or US-20160322381-\$ or US-20150236038-\$.did. or (US-8664761-\$ or US-9449987-\$ or US-10453798-\$ or US- 9806093-\$ or US- 10381322-\$).did.					
L143	2	((("20120280304") or ("20200161321")).PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2021/01/29 01:50 PM
L144	220	((("GUO") near3 ("Mei") near3 ("Lan")) OR (("HU") near3 ("Yushi")) OR (("XIA") near3 ("Ji")) OR (("ZHU") near3 ("Hongbin"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	OFF	OFF	2021/03/04 10:34 AM
L145	1549	(257/315).CCLS.	(US-PGPUB)	OR	ON	ON	2021/03/04 10:34 AM
L146	1326	(257/314).CCLS.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 10:38 AM
L147	1027	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:25 AM
L148	1027	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:25 AM
L149	3337	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 11:32 AM
L150	2461	L149 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:32 AM
L151	1249	L150 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:32 AM
L152	5796	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 11:46 AM
L153	4304	L152 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:46 AM
L154	1932	L153 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 11:47 AM
L155	7132	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 01:26 PM
L156	4606	L155 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 01:26 PM
L157	2161	L156 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 01:26 PM
L158	0	H01L23/5283.CPC1	(US-PGPUB)	OR	OFF	OFF	2021/03/04 01:27 PM
L159	2521	H01L23/5283.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 01:27 PM
L160	1622	L159 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 01:29 PM

L161	3255	H01L27/11524.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 02:19 PM
L162	2481	L161 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:19 PM
L163	2468	L162 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:19 PM
L164	1852	L163 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:20 PM
L165	2019	H01L27/11529.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:20 PM
L166	5634	H01L27/11556.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 02:59 PM
L167	3084	H01L27/11556.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 02:59 PM
L168	1760	L167 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:00 PM
L169	3129	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 03:05 PM
L170	1803	L169 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:08 PM
L171	2336	H01L27/11573.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 03:45 PM
L172	1379	L171 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:45 PM
L173	5703	H01L27/11582.CPC.	(US-PGPUB)	OR	OFF	OFF	2021/03/04 03:46 PM
L174	3326	L173 and @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L175	3286	L174 and (memory string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L176	3067	L175 and stack\$3	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L177	2423	L176 and (hole recess\$3)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:46 PM
L178	2354	L177 and (bit line)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:47 PM
L179	2251	L178 and (word data)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2021/03/04 03:47 PM
L180	1	("20120098048").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2021/03/04 04:48 PM
L181	303	((("GUO") near3 ("Mei") near3 ("Lan")) OR ("HU") near3 ("Yushi")) OR ("XIA") near3 ("Ji")) OR ("ZHU") near3 ("Hongbin"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/04/04 06:59 AM
L182	99	L181 AND (("YANGTZE MEMORY TECHNOLOGIES CO LTD.".ase. OR "MICRON	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/04/04 07:50 AM

		TECHNOLOGY, INC.".ase. OR "INTEL CORPORATION".ase. OR "WUXI PETABYTE TECHNOLOGIES CO LTD.".ase. OR "DELTA ELECTRONICS (SHANGHAI) CO LTD.".ase. OR "EMAGIN CORPORATION".ase. OR "AUBURN UNIVERSITY".ase. OR "INTEL CORPORATINO".ase. OR "SHENZHEN JIUHU TECHNOLOGY CO LIMITED".ase. OR "SHENZHEN JIUHU TECHNOLOGY CO LTD".ase.))					
L183	10019	257/314	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/04/04 07:51 AM
L184	8823	L183 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 07:52 AM
L185	919	L184 AND (bit nlearine)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 07:52 AM
L186	727	L184 AND (bit NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 07:52 AM
L187	569	H01L27/11531.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/04/04 08:25 AM
L188	1105	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:25 AM
L189	7192	H01L21/76816.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:40 AM
L190	4750	L189 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:40 AM
L191	472	L190 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 08:41 AM
L192	13	("20180331118" "20130264631" "20160099255" "20170062454" "20120280304" "20150179660" "20150206895" "20150236038" "20160322381" "20120119287" "20140175532" "20170125430" "20170179152").P N.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:54 AM
L193	1	"20210104531"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 08:59 AM
L194	2	"20120280304"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 09:03 AM
L195	12904	H01L21/76877.CPC.	(US-PGPUB; USPAT;	OR	OFF	OFF	2022/04/04

L196	8763	L195 AND @pd<"20180914"	USOCR) (US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	10:00 AM 2022/04/04 10:00 AM
L197	521	L196 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:00 AM
L198	361	H01L23/52.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:26 AM
L199	8494	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:26 AM
L200	8997	L199 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 10:26 AM
L201	601	L200 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/04/04 10:27 AM
L202	13	("20180331118" "20130 264631" "20160099255 " "20170062454" "2012 0280304" "2015017966 0" "20150206895" "201 50236038" "201603223 81" "20120119287" "20 140175532" "20170125 430" "20170179152").P N.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:18 AM
L203	1	(14/862916).APP.	(USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:20 AM
L204	135	("5387530" "5915167" "7177191" "7221588" "7233522" "7514321" "7575973" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829" "8187936" "8193054" "8198672" "8349681" "8394716" "8445347" "8450181" "8614126" "8658499" "8741761" "8828884" "8847302" "8878278" "8884357" "8928061" "8946023" "9023719" "9230979" "9437606" "20060003531" "20060258076" "20070210338" "20070252201" "20080067583" "20080169496" "20090026561" "20090121271" "20090242967" "20100044778" "20100059811" "20100112769" "20100120214" "20100133599"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:20 AM

		"20100155810" "20100155818" "20100171162" "20100181610" "20100207195" "20100213458" "20100320528" "20110065270" "20110076819" "20110133606" "20110151667" "20110266606" "20110287612" "20110312174" "20120001247" "20120001249" "20120003800" "20120003831" "20120052674" "20120061744" "20120068242" "20120074367" "20120119287" "20120140562" "20120153376" "20120208347" "20120256247" "20120261638" "20120261722" "20120276719" "20130248974" "20130264631" "20130313627" "20130313717" "20130322174" "20140225181" "20140264525" "20140264533" "20140264542" "20140273373" "20150076580" "20150179660" "20150348984" "20160049423" "20160163728" "20160276359").pn. OR ("9627403").urpn. AND (PGPB USPT USOC).dbnm.					
L205	23	"10304852"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:28 AM
L206	14	("9812464" "10304852" "10319635" "20160118399" "20170012052" "20170047343"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/04/04 11:29 AM

		"20170084696" "20170179154" "20170358593" "20180151587" "20190067316" "20190164991").pn. OR ("10573659").urpn. AND (PGPB USPT USOC).dbnm.					
L207	312	((("GUO") near3 ("Mei") near3 ("Lan")) OR (("HU") near3 ("Yushi")) OR (("XIA") near3 ("Ji")) OR (("ZHU") near3 ("Hongbin"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/08/01 09:38 AM
L208	101	L207 AND (("YANGTZE MEMORY TECHNOLOGIES CO LTD.").ase. OR "MICRON TECHNOLOGY, INC.".ase. OR "INTEL CORPORATION".ase. OR "WUXI PETABYTE TECHNOLOGIES CO LTD.".ase. OR "DELTA ELECTRONICS (SHANGHAI) CO LTD.".ase. OR "EMAGIN CORPORATION".ase. OR "AUBURN UNIVERSITY".ase. OR "INTEL CORPORATINO".ase. OR "SHENZHEN JIUHU TECHNOLOGY CO LIMITED".ase. OR "SHENZHEN JIUHU TECHNOLOGY CO LTD".ase.))	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/08/01 09:43 AM
L209	1346	257/314	(US-PGPUB)	OR	ON	ON	2022/08/01 09:46 AM
L210	580	H01L27/11531.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 10:41 AM
L211	1126	H01L27/11531.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 10:41 AM
L212	6984	H01L27/11524.CPC.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 10:50 AM
L213	4633	L212 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 10:50 AM
L214	1812	L213 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 10:51 AM
L215	3900	H01L21/76816.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:22 AM

L216	2491	L215 AND @pd<"20180914"	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:22 AM
L217	473	L216 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:23 AM
L218	6635	H01L21/76877.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:31 AM
L219	8774	L218 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 11:31 AM
L220	521	L219 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:32 AM
L221	8876	H01L23/5226.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:54 AM
L222	9023	L221 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 11:54 AM
L223	602	L222 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 11:55 AM
L224	3387	H01L23/5283.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 12:33 PM
L225	3222	L224 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 12:34 PM
L226	196	L225 AND ((bit data) NEAR line)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 12:34 PM
L227	49	L225 AND (memory NEAR stack\$3)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 12:34 PM
L228	550	L225 AND (spacer dummy)	(US-PGPUB)	OR	OFF	OFF	2022/08/01 12:35 PM
L229	663	L226 OR L227 OR L228	(US-PGPUB)	OR	OFF	OFF	2022/08/01 12:35 PM
L230	1383	H01L27/11529.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/08/01 01:11 PM
L231	1	"20210104531"	(US-PGPUB)	OR	OFF	OFF	2022/08/01 02:46 PM
L232	24	(Artificial Intelligence) More like doc: US-20210104531-A1 Text: (US-20200066739-A1 OR US-11049866-B2 OR US-20200161321- A1 OR US- 20210296333-A1 OR US-10566336-B1 OR TW-202010109-A OR US-10879254-B2 OR US-20200161322-A1 OR TW-I683423-B OR US-20210082931-A1 OR CN-109314118-B OR CN-109314118-A OR US-10910397-B2 OR WO-2020037489- A1 OR CN-114551463-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/01 02:56 PM

L233	13	A OR US- 20210134826-A1 OR TW-201834221-A OR US-20210082953-A1 OR US-10847539-B2 OR US-20200212058- A1).did. (US-20200066739-A1 OR US-11049866-B2 OR US-20200161321- A1 OR US- 20210296333-A1 OR US-10566336-B1 OR TW-202010109-A OR US-10879254-B2 OR US-20200161322-A1 OR TW-I683423-B OR US-20210082931-A1 OR CN-109314118-B OR CN-109314118-A OR US-10910397-B2 OR WO-2020037489- A1 OR CN-114551463- A OR US- 20210134826-A1 OR TW-201834221-A OR US-20210082953-A1 OR US-10847539-B2 OR US-20200212058- A1).did.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 03:02 PM
L234	5	("20110049646" OR "20130164928" OR "20170373079" OR "20190287982" OR "20190355663").pn.	(US-PGPUB; USPAT)	OR	OFF	OFF	2022/08/01 03:06 PM
L235	1	(15/483862).APP.	(USPAT; USOCR)	OR	OFF	OFF	2022/08/01 03:10 PM
L236	118	("5084417" "5807788" "5915167" "5942799" "6001461" "6194310" "6404054" "6525364" "6958265" "7067871" "7071108" "7177191" "7221588" "7232764" "7233522" "7378353" "7485961" "7514321" "7531862" "7547951" "7575973" "7598557" "7608195" "7648872" "7745265" "7745312" "7808038" "7848145" "7851851" "7969008" "8008710" "8053829" "8093725" "8187936" "8193054" "8193074" "8198672" "8222160" "8283228" "8349681"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 03:10 PM

		"8446003" "8767439" "8828814" "8884357" "8987087" "8987089" "9023719" "9153486" "9230973" "9252151" "9397046" "9397093" "9406694" "9449983" "9460931" "9659998" "20020190379" "20030059632" "20030075802" "20030209746" "20040082156" "20040159874" "20040232467" "20060102586" "20060118954" "20070023917" "20070210338" "20070252201" "20090227105" "20090267132" "20100044778" "20100112769" "20100120214" "20100155810" "20100155818" "20100176432" "20100181610" "20100187584" "20100207195" "20100320528" "20110076819" "20110133606" "20110266606" "20120001247" "20120001249" "20120012921" "20120070944" "20120115300" "20120256247" "20130094109" "20130122712" "20130221445" "20130224960" "20130248974" "20130264631" "20130270631" "20130313627" "20140008714" "20140264471" "20140353738" "20150037912" "20150076585" "20150144481" "20150325473" "20150380419" "20160133512"				
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L237	1	"20160148945" "20160149002" "20160149049" "20160163870" "20160276158" "20170186752" "20170243873" "20180151474").pn. OR ("10361213").urpn. AND (PGPB USPT USOC).dbnm. (15/483862).APP.	(USPAT; USOCR)	OR	OFF	OFF	2022/08/01 03:20 PM
L238	118	("5084417" "5807788" "5915167" "5942799" "6001461" "6194310" "6404054" "6525364" "6958265" "7067871" "7071108" "7177191" "7221588" "7232764" "7233522" "7378353" "7485961" "7514321" "7531862" "7547951" "7575973" "7598557" "7608195" "7648872" "7745265" "7745312" "7808038" "7848145" "7851851" "7969008" "8008710" "8053829" "8093725" "8187936" "8193054" "8193074" "8198672" "8222160" "8283228" "8349681" "8446003" "8767439" "8828814" "8884357" "8987087" "8987089" "9023719" "9153486" "9230973" "9252151" "9397046" "9397093" "9406694" "9449983" "9460931" "9659998" "20020190379" "20030059632" "20030075802" "20030209746" "20040082156" "20040159874" "20040232467" "20060102586" "20060118954" "20070023917" "20070210338" "20070252201" "20090227105" "20090267132" "20100044778" "20100112769"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 03:20 PM

		"20100120214" "20100155810" "20100155818" "20100176432" "20100181610" "20100187584" "20100207195" "20100320528" "20110076819" "20110133606" "20110266606" "20120001247" "20120001249" "20120012921" "20120070944" "20120115300" "20120256247" "20130094109" "20130122712" "20130221445" "20130224960" "20130248974" "20130264631" "20130270631" "20130313627" "20140008714" "20140264471" "20140353738" "20150037912" "20150076585" "20150144481" "20150325473" "20150380419" "20160133512" "20160148945" "20160149002" "20160149049" "20160163870" "20160276158" "20170186752" "20170243873" "20180151474").pn. OR ("10361213").urpn. AND (PGPB USPT USOC).dbnm.					
L239	2	"15291640"	(US-PGPUB)	OR	OFF	OFF	2022/08/01 03:25 PM
L240	2	"20120280304" OR "20170125430"	(US-PGPUB)	OR	OFF	OFF	2022/08/01 03:35 PM
L241	1	(14/925224).APP.	(USPAT; USOCR)	OR	OFF	OFF	2022/08/01 03:45 PM
L242	72	("5915167" "7005350" "7023739" "7177191" "7221588" "7233522" "7514321" "7575973" "7696559" "7745265" "7808038" "7848145"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 03:45 PM

		"7851851" "8008710" "8053829" "8187936" "8394716" "8643142" "8878278" "9023719" "20070210338" "20070252201" "20090230449" "20090242967" "20100044778" "20100112769" "20100120214" "20100155810" "20100155818" "20100181610" "20100207195" "20100320528" "20110076819" "20110133606" "20110266606" "20120001247" "20120001249" "20120001250" "20120012920" "20120119287" "20120280304" "20130264631" "20150076584" "20150076586" "20150179660" "20150206895").pn. OR ("9620512").urpn. AND (PGPB USPT USOC).dbnm.					
L243	11	("9484354" "9536897" "9601577" "9620512" "9666281" "9728551" "9768193" "20120070944" "20150079748" "20160027796" "20170271354").pn. OR ("10937797").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 03:50 PM
L244	12	("6067249" "7772618" "8048798" "8378409" "20110049611" "20120168858").pn. OR ("9484354").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/01 04:01 PM
L245	1	"20150348987"	(US-PGPUB)	OR	OFF	OFF	2022/08/01 04:44 PM
L246	1	"20210104531"	(US-PGPUB)	OR	OFF	OFF	2022/08/03 08:40 AM
L247	23	("20110049646" "20180	(US-PGPUB; USPAT;	OR	OFF	OFF	2022/08/03

		331118" "20130164928 "20130264631" "2016 0099255" "2017006245 4" "20190115357" "201 90355663" "201202803 04" "20150179660" "20 150206895" "20150236 038" "20160322381" "2 0170358593" "2017037 3079" "20180151587" " 10304852" "201902879 82" "20120119287" "20 140175532" "9812464" "20170125430" "20170 179152").PN.	USOCR)				08:42 AM
L248	66	("5915167" "8193571" "8395190" "9412749" "9455267" "9570463" "9576967" "9659956" "9673213" "9754963" "9786681" "9853038" "9881929" "9991280" "20060110880" "20090230449" "20100133598" "20100213527" "20100254191" "20110031546" "20110065272" "20110198687" "20110248327" "20110266606" "20120098050" "20120181701" "20140042519" "20140092686" "20140192594" "20140231954" "20150055413" "20150076586" "20150115455" "20150155292" "20150179662" "20150187425" "20150236038" "20160049421" "20160086969" "20160329341" "20170110402" "20170287926" "20170358590" "20180182771").pn. OR ("10304852").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/03 08:45 AM
L249	2	"20150236038"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/08/03 09:07 AM

L250	85	L207 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 06:12 AM
L251	49	L250 AND (("MICRON TECHNOLOGY, INC.".ase. OR "INTEL CORPORATION".ase. OR "DELTA ELECTRONICS (SHANGHAI) CO., LTD.".ase. OR "EMAGIN CORPORATION".ase. OR "AUBURN UNIVERSITY".ase. OR "TELEFONAKTIEBOLA GET LM ERICSSON (PUBL)".ase.))	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 06:34 AM
L252	1346	257/314	(US-PGPUB)	OR	OFF	OFF	2022/10/05 06:35 AM
L253	8823	L252 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 06:35 AM
L254	1321	L252 AND @pd<"20180914"	(US-PGPUB)	OR	OFF	OFF	2022/10/05 06:36 AM
L255	4413116	storage OR buffer OR memory OR cache OR disk OR disc OR diskette OR RAM OR ROM OR SDRAM OR DRAM OR CD-ROM OR PROM OR EPROM OR EEPROM OR (readable near3 (storage OR memory OR media)) OR ((information OR data) near3 storage) OR NVRAM OR (nonvolatile adj3 memory) OR ((recordable OR writable) near3 media)	(US-PGPUB)	OR	OFF	OFF	2022/10/05 06:36 AM
L256	1284	L254 AND L255	(US-PGPUB)	OR	OFF	OFF	2022/10/05 06:37 AM
L257	581	H01L27/11531.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/10/05 08:07 AM
L258	872	L257 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 08:07 AM
L259	442	L258 AND L255	(US-PGPUB)	OR	OFF	OFF	2022/10/05 08:07 AM
L260	3861	H01L27/11524.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/10/05 08:19 AM
L261	4632	L260 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 08:19 AM
L262	2474	L261 AND L255	(US-PGPUB)	OR	OFF	OFF	2022/10/05

L263	5251397	(slit split open opening interleaving aperture gap hole interleav\$3 space spacing cutout notch\$2 hollow)	(US-PGPUB)	OR	OFF	OFF	08:20 AM 2022/10/05 08:21 AM
L264	2134	L262 AND L263	(US-PGPUB)	OR	OFF	OFF	2022/10/05 08:21 AM
L265	3272	L264 AND (stack\$3 OR string)	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 08:22 AM
L266	1777	L264 AND (stack\$3 OR string)	(US-PGPUB)	OR	OFF	OFF	2022/10/05 08:22 AM
L267	4600	H01L27/11556.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/10/05 08:50 AM
L268	3284	L267 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 08:51 AM
L269	1599	L268 AND L263	(US-PGPUB)	OR	OFF	OFF	2022/10/05 08:51 AM
L270	4039	H01L27/1157.CPC.	(US-PGPUB)	OR	OFF	OFF	2022/10/05 09:28 AM
L271	3217	L270 AND @pd<"20180914"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 09:28 AM
L272	1722	L271 AND (stack\$3 OR string)	(US-PGPUB)	OR	OFF	OFF	2022/10/05 09:28 AM
L273	1597	L272 AND (slit split open opening interleaving aperture gap hole interleav\$3 space spacing cutout notch\$2 hollow)	(US-PGPUB)	OR	OFF	OFF	2022/10/05 09:28 AM
L274	46	(Artificial Intelligence) Similar to: 17/100,847 with 0 CPC Selections and 0 Text Selections Text: (CN-111725231-A OR CN-112242396-A OR US-10734401-B1 OR KR-20210009146-A OR US-20220102369-A1 OR CN-114256264-A OR KR-20210095390-A OR KR-20220041982-A OR US-20200303401-A1 OR KR-20200111332-A OR DE-102021119273-A1 OR US-20210335819-A1 OR US-20190237477-A1 OR JP-2022054427-A OR US-10903229-B2 OR CN-113594168-A OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO))	OR	OFF	OFF	2022/10/05 10:10 AM

		US-20210343637-A1 OR CN-113161369-A OR US-20210233928-A1 OR KR-20190091109-A OR JP-2022520174-A OR EP-3891812-A1 OR WO-2020220268-A1 OR US-11430807-B2 OR CN-110085594-A OR US-20200357812-A1 OR US-10714490-B1 OR KR-20210102979-A OR CN-110235249-B OR US-20210074716-A1 OR TW-202107684-A OR CN-114664791-A OR US-10515973-B2 OR US-10763274-B2 OR CN-112106193-A OR CN-109859783-A OR US-20190043874-A1 OR US-10256247-B1 OR US-20200006370-A1 OR CN-110235249-A OR US-9520360-B2 OR US-20210143169-A1 OR WO-2022021022-A1 OR US-20220028440-A1 OR WO-2020000365-A1 OR CN-111403415-B OR CN-109314115-B OR CN-111403415-A OR US-10580787-B2 OR TW-202205518-A).did.					
L275	10	L274 AND (slit split open opening interleaving aperture gap hole interleav\$3 space spacing cutout notch\$2 hollow)	(US-PGPUB)	OR	OFF	OFF	2022/10/05 10:13 AM
L276	37	(Artificial Intelligence) More like doc: US-20210233928-A1 Text: (US-11430807-B2 OR CN-113161369-A OR KR-20210095390-A OR CN-113161368-A OR US-20200203366-A1 OR US-20210125928-A1 OR US-20210210505-A1 OR US-10854622-B2 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA,	OR	OFF	OFF	2022/10/05 10:18 AM

L277	11	KR-20210088836-A OR US-20200295023-A1 OR US-20200203370- A1 OR CN-113948515- A OR US- 20210225871-A1 OR EP-3557622-A2 OR US-10748923-B2 OR EP-3557622-B1 OR US-20170294388-A1 OR US-20210408037- A1 OR US-10515979- B2 OR US- 20180226424-A1).did. ("8304348" "8461566" "9029938" "9373540" "9620511" "10079203" "10192929" "10395982" "10916563" "20190326166" "20210125928").pn. OR ("11430807").urpn. AND (PGPB USPT USOC).dbnm.	VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 10:18 AM
L278	10	("8008722" "8163617" "8237218" "8324680" "8981458" "20110062510" "20110233648" "20110303969").pn. OR ("9620511").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 10:20 AM
L279	2	"20150008499"	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 10:21 AM
L280	1	"20170194347"	(US-PGPUB)	OR	OFF	OFF	2022/10/05 10:24 AM
L281	37	(Artificial Intelligence) More like doc: US-9899412-B2 Text: (US-20150008499-A1 OR US-20170194347- A1 OR US-9620511-B2 OR KR-20150006531-A OR KR-102114341-B1 OR US-20150060977- A1 OR US- 20180026050-A1 OR US-10263009-B2 OR US-10854630-B2 OR US-20120228697-A1 OR US-9082655-B2 OR US-8653585-B2 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/10/05 10:24 AM

L282	1	US-20140162419-A1 OR US-20160247813-A1 OR CN-109449162-A OR US-20160343730-A1 OR CN-105914184-B OR US-10199390-B2 OR CN-109449162-B OR KR-20130007703-A).did. (16/140422).APP.	(USPAT; USOCR)	OR	OFF	OFF	2022/10/05 10:31 AM
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L285	1	(13/848232).APP.	(USPAT; USOCR)	OR	OFF	OFF	2022/10/05 10:41 AM
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L287	29	(Artificial Intelligence) More like doc: US-20200006370-A1 Text: (US-10763274-B2 OR US-20200357812-A1 OR CN-111403415-A OR CN-109314115-B OR TW-202002177-A OR CN-111403415-B OR TW-I688046-B OR US-20200006371-A1 OR US-20210104534-A1 OR WO-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO;	OR	OFF	OFF	2022/10/05 10:43 AM

		2020000365-A1 OR US-20210272976-A1 OR US-11043506-B2 OR KR-102309462-B1 OR KR-20200127260-A OR WO-2020000318- A1 OR CN-109314115- A OR US- 20200091164-A1 OR US-10651187-B2 OR US-20200235115-A1 OR US-11037946- B2).did.	JPO; DERWENT; IBM_TDB)				
L288	12	"10763274"	(US-PGPUB; USPAT; USOCR; DERWENT)	OR	OFF	OFF	2022/10/05 10:45 AM
L289	1	"10763274"	(US-PGPUB)	OR	OFF	OFF	2022/10/05 10:46 AM
L290	0	(16/940393).APP.	(USPAT; USOCR)	OR	OFF	OFF	2022/10/05 10:46 AM
L291	0	(16/940393).APP.	(USPAT)	OR	OFF	OFF	2022/10/05 10:46 AM
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L293	14	("20110215394" "20120062777" "20140061751" "20140211566" "20140225235" "20140284713" "20150037200" "20150129878" "20150325588" "20150372005" "20160027504" "20160118128" "20170278806" "20170330887").pn. OR ("10763274").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2022/10/05 10:47 AM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N63	1	(form\$3 near2 spacer near3 sidewall near3 first near open\$3) and (form\$3 near3 array ear contact near2 extend\$3 near vertically tnear3 dielectric near stack near3 conductor near layer near4 spacer near3 first near open\$3)	(USPAT)	OR	OFF	OFF	2019/12/18 03:52 PM

N181	0	and (after near form\$3 TAC near2 form\$3 near2 slit near extend\$3 near vertically near3 dielectric near stack).clm. (memory near stack\$3 near2 substrate near2 interleav\$3 near2 plurality near2 conduct\$3 near layers near2 dielectric near layers near4 plurality near2 conduct\$4 near layers near3 respect\$3 near shallow near recess) and (channel near structure near extend\$3 near vertically near2 memory near stack\$3).clm.	(USPAT)	OR	OFF	OFF	2021/03/04 03:21 PM
N182	0	(through NEAR array NEAR contact NEAR extend\$3 NEAR vertically near3 conductor NEAR dielectric NEAR layer NEAR pairs near2 memory NEAR stack near2 bur\$3 near3 substrate) AND (slit NEAR structure NEAR extend\$3 vertically near3 conductor NEAR dielectric NEAR layer NEAR pairs near2 memory NEAR stack near3 separate near2 memory NEAR stack near3 plurality near2 memory NEAR zones).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/05 12:55 PM



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/100,847	11/21/2020	Mei Lan Guo	10018-01-0015-US-DIV2	1008
153988	7590	10/18/2022	EXAMINER	
Bayes PLLC			TRAN, DZUNG	
8260 Greensboro Drive				
Suite 625				
McLean, VA 22102				
			ART UNIT	PAPER NUMBER
			2829	
			NOTIFICATION DATE	DELIVERY MODE
			10/18/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

Corrected Notice of Allowability	Application No. 17/100,847	Applicant(s) Guo et al.	
	Examiner DZUNG T TRAN	Art Unit 2829	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 09/22/2022.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are See Continuation Sheet. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov**.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____. 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material ____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	5. ☐ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	---

/DZUNG TRAN/ Primary Examiner, Art Unit 2829	
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Continuation of 3. The allowed claim(s) is/are: 1-2,4-7,9-12 and 14-23

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

153988 7590 10/12/2022
Bayes PLLC
8260 Greensboro Drive
Suite 625
McLean, VA 22102

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Anna O'Connor	(Typed or printed name)
/Anna O'Connor/	(Signature)
January 9, 2023	E-FILED (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/100,847	11/21/2020	Mei Lan Guo	10018-01-0015-US-DIV2	1008

TITLE OF INVENTION: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	01/12/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, DZUNG	2829	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 BAYES PLLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

YANGTZE MEMORY TECHNOLOGIES CO., LTD.

WUHAN, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 60-2227

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

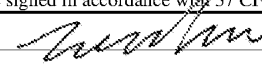
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature 

Date 1/9/2023

Typed or printed name Zhiwei Zou

Registration No. 66,041

Electronic Patent Application Fee Transmittal				
Application Number:		17100847		
Filing Date:		21-Nov-2020		
Title of Invention:		THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		
First Named Inventor/Applicant Name:		Mei Lan Guo		
Filer:		Zhiwei Zou/Anna O'Connor		
Attorney Docket Number:		10018-01-0015-US-DIV2		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	47339017
Application Number:	17100847
International Application Number:	
Confirmation Number:	1008
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0015-US-DIV2
Receipt Date:	09-JAN-2023
Filing Date:	21-NOV-2020
Time Stamp:	14:17:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	E202319E18161796
Deposit Account	602227
Authorized User	Anna O'Connor
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	10018-01-0015-US-DIV2_IFTransmittal.pdf	281353	no	1
			b1a0a6338aabf139dd4bce964e63a1fbb3bcbfd3		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37676	no	2
			19b79e88da56ba4ae9757b05052e23440f0ee4c4		
Warnings:					
Information:					
Total Files Size (in bytes):			319029		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/100,847	02/14/2023	11581322	10018-01-0015-US-DIV2	1008

153988 7590 01/25/2023
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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 77 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional inventors):

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IR103 (Rev. 10/09)

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Micron v. YMTC
IPR2025-00191