

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00191
U.S. Patent No. 11,581,322
Issue Date: February 14, 2023

Title: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH
ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

**DECLARATION OF DR. JACK C. LEE IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 11,581,322**

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I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in Claims 1-20 of U.S. Patent No. 11,581,322, which I refer to herein as the ’322 Patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of \$680 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My *curriculum vitae* (“CV”) is attached hereto as Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. This includes classes relating to, among other things, 3D NAND technology. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professorship in Engineering in the

Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

10. My current research and teaching interests include semiconductor devices, semiconductor memory applications (including non-volatile memory), fabrication processes, silicon-on-insulator technologies, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, and alternative channel materials. I routinely encounter and address topics relating to NAND flash memory, and more specifically 3D NAND flash memory, in my research. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

11. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. Many of these relate to the structure and operation of memory devices, including non-volatile memory such as NAND flash memory and 3D NAND flash memory. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

12. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

13. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. ASSIGNMENT AND MATERIALS CONSIDERED

14. I have been asked to provide analysis and explain the subject matter of the '322 Patent, including the state of the art when the application underlying the '322 Patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '322 Patent including how that art relates to Claims 1-20 (which I refer to as the “challenged claims”) of the '322 Patent and to provide my opinions regarding whether that art invalidates the challenged claims.

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15. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the challenged claims of the '322 Patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

16. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '322 Patent.

17. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the '322 Patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

EXHIBIT NO.	DESCRIPTION
1005	U.S. Patent No. 9,837,431 to Nishikawa et al. (“Nishikawa”)
1006	U.S. Patent No. 9,853,046 to Lu et al. (“Lu”)
1007	U.S. Patent No. 10,658,378 to Tao et al.
1008	U.S. Patent Publication No. 2019/0229125A1 to Zhou et al.
1009	U.S. Patent No. 10,777,501 to Nakajima et al. (“Nakajima”)

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EXHIBIT NO.	DESCRIPTION
1010	Micheloni, “3D Flash Memories” (2016)
1011	U.S. Patent Publication No. 2017/0179026 A1 to Toyama et al.
1012	U.S. Patent No. 10,354,980 to Mushiga et al.
1013	PCT Publication No. WO 2019/042103A1 to Dai et al.
1014	U.S. Patent No.10,679,721 to Kim et al.
1015	Aritome, “NAND Flash Memory Technologies”
1016	File History for U.S. Patent Application No. 16/745,342
1017	U.S. Patent Publication No. 2012/0280304A1 to Lee et al. (“Lee 304”)
1018	U.S. Patent Publication No. 2017/0125430A1 to Nishikawa et al. (“Nishikawa 430”)
1019	U.S. Patent Publication No. 2015/0348987A1 to Lee et al. (“Lee 987”)
1020	U.S. Patent Publication No. 2018/0301374A1 to Masamori et al. (“Masamori”)
1021	U.S. Patent No. 8,107,292 to Maejima
1022	U.S. Patent No. 10,347,654 to Iwai et al.
1023	U.S. Patent No. 10,559,583 to Park et al.
1024	U.S. Patent No. 5,945,717 to Chevallier
1025	U.S. Patent No. 10,347,487 to Lee et al.
1026	Ronse, “Optical lithography—a historical perspective,” C. R. Physique 7 (2006)

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EXHIBIT NO.	DESCRIPTION
1027	U.S. Patent No. 10,290,643 to Kai et al.
1028	U.S. Patent No. 9,859,297 to Park et al.
1029	U.S. Patent Publication No. 2018/0308559 to Kim et al.
1030	U.S. Patent No. 8,945,996 to Tang et al.
1031	U.S. Patent No. 10,115,632 to Masamori et al.
1032	U.S. Patent No. 10,879,254 to Guo et al.
1033	U.S. Patent No. 9,793,139 to Sharangpani et al.
1034	Excerpts from Wolf, “Silicon Processing for the VLSI Era, Volume 1-Process Technology,” Lattice Press (1986) (“Wolf Vol. 1”)
1035	Excerpts from Wolf, “Silicon Processing for the VLSI Era, Volume 1-Process Integration,” Lattice Press (1990) (“Wolf Vol. 2”)
1036	U.S. Patent Publication No. 2019/0081061 to Tessariol et al.
1037	U.S. Patent No. 10,304,852 to Cui et al.
1038	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,879,254 (Ex. B-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) (“Ex. B-1, YMTC’s Contentions”) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1039	U.S. Patent No. 11,075,084 to Shen et al.
1040	U.S. Patent No. 10,504,596 to Goda et al.
1041	U.S. Patent No. 10,381,369 to Kim et al.

EXHIBIT NO.	DESCRIPTION
1046	U.S. Patent No. 9,935,123 to Nishikawa (“Nishikawa2”)
1047	Printout, 11/26/2024, Britannica (https://www.britannica.com/science/geometry) (ellipse)

IV. UNDERSTANDING OF THE LAW

18. I am not an attorney, but have been instructed in and applied the law as described in this section.

19. I understand that the first step in comparing a challenged claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the challenged claims of the alleged invention in Section IX (where I discuss certain claim terms).

20. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

21. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

22. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

23. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

24. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that

it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

25. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

26. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

27. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one

field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

28. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

29. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

30. I have been informed and I understand that factors referred to as “objective indicia of non-obviousness” or “secondary considerations” are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

31. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a “nexus,” between any such secondary indicia and the claimed invention.

32. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

33. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

34. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

35. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

36. In my opinion, a POSITA in the field of the '322 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

37. In my opinion, this POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled.

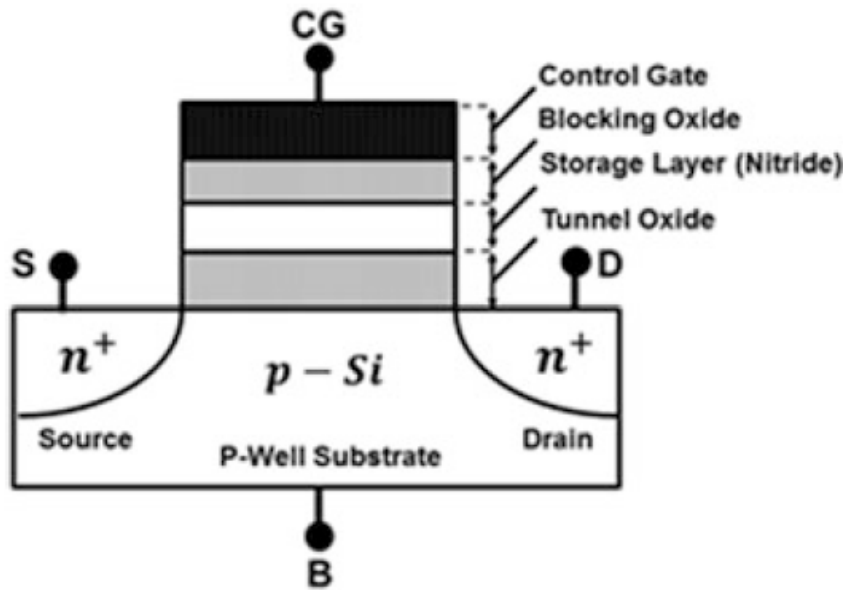
38. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile 3D NAND flash memory—I was a person of more than the ordinary level of skill in the art as of August 2018. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE ART

39. I have been asked to provide a brief overview of the technology relevant to the '322 Patent and the state of the art when the '322 priority application was filed.

40. The '322 Patent (and the prior art I discuss herein) relate to three-dimensional (3D) NAND flash memory. “Flash memory” has been known for many decades and is a type of memory that stores information even when power is removed (*viz.*, when the device is turned off).

41. At the heart of flash memory lies the “memory cell,” which stores information as electrical charge. An example memory cell is below:



Ex. 1010, 41. In a memory cell, current flows from the “drain” of the device to the “source” of the device, which is typically connected to a low voltage, such as ground. *Id.*, 150 (“[T]he Source Line ... plays the role of the ‘local ground’ for each memory cell.”).

42. The acronym “NAND” refers to a “not-AND” logic gate, and NAND flash memory is a particular type of flash memory where the memory cells form a structure similar to that of a NAND gate. Ex. 1010, 14. The other most common type of flash memory is NOR flash, but NAND offers a higher integration density and occupies a larger market than NOR flash.

43. A NAND flash memory device, like most flash memory devices, has an associated memory controller that controls the read, write, and erase operations

on a memory cell by applying a voltage to that cell's "control gate," labeled as "CG" in the above figures. Ex. 1010, 41.

44. For many years, a NAND flash memory was "planar," that is, two-dimensional (2D). In 2D NAND flash memory, all memory cells lie on a 2D plane (*i.e.*, the x-y plane) on the surface of a memory chip as shown below:

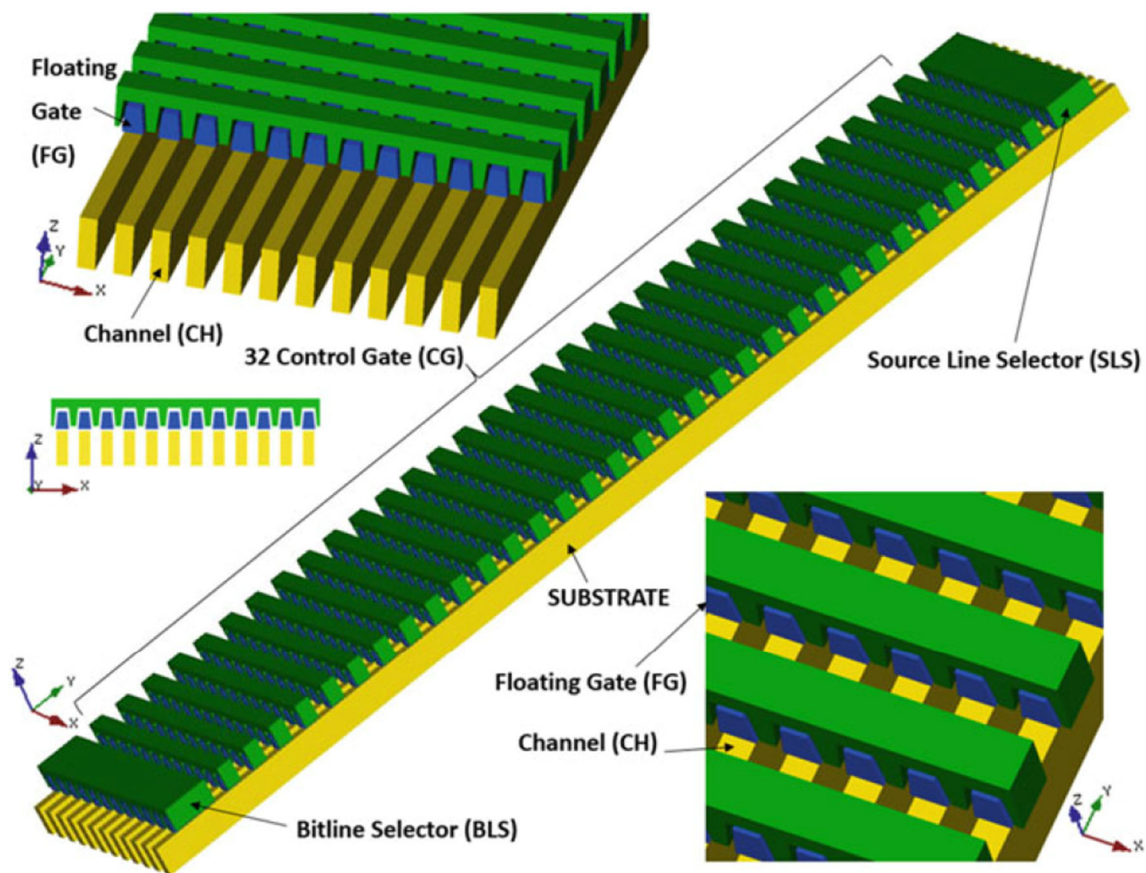


Fig. 3.9 Bird's-eye view of a planar NAND string

Ex. 1010, 86.

45. To boost data storage densities and reduce cost per gigabit, the art developed so-called "three-dimensional (3D) NAND flash cells" starting in about

2006. Ex. 1015, 292. Unlike planar 2D NAND flash memory, in 3D NAND flash memory the memory cells are arranged in vertical, cylindrical NAND flash columns, often referred to as “memory strings.” Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block and turning the 2D NAND string on its side, resulting in a 3D structure with a vertical channel. The following image provides an example:

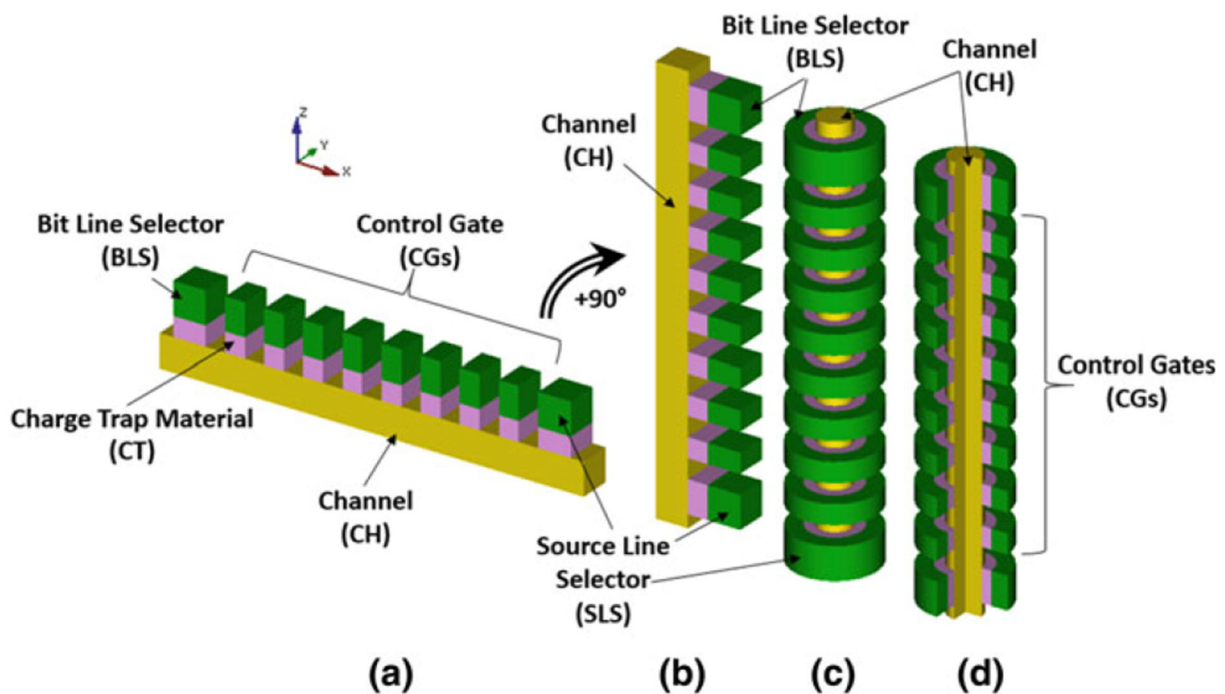


Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

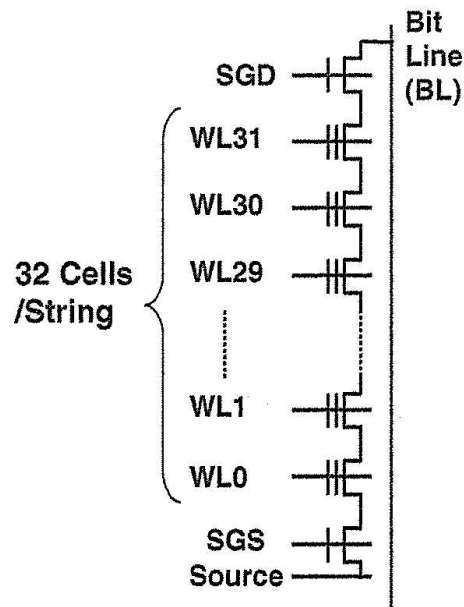
Ex. 1010, 102. As labeled in Figure 4.1, above, each NAND string includes a “cylindrical channel.” *Id.*, 58. The concept of a “channel” was well-known in semiconductor devices and refers to a thin and layer of charge that is formed between the source and drain of a transistor when a voltage is applied to the gate. The

“channel” is highly conductive and allows current to easily flow between the source and drain. The “cylindrical channel” in 3D NAND devices also provides the means for current to flow in a memory string.

46. Multiple of such vertical channels are then repeated in a three-dimensional array. Ex. 1015, 296.

47. As can be seen above, the NAND flash memory “strings” each contain multiple cells “connected in series.” Ex. 1015, 38. The source of one cell is connected to the drain of the next one. Depending on the technology, typically a string consists of 32 to 128 NAND cells.

48. Each end of a string is terminated with a “select transistor.” One is often called the “SGD” (drain-end select gate transistor) and the other one is often called “SGS” (source-end select gate transistor). The “SGD connects” at the string’s drain side “to isolate it from a bit line (BL).” Ex. 1015, 38. Hence, the SGD is also known as the “bit line select transistor” or the “upper select gate.” The SGS connects at the string’s source side “to isolate it from a source line (SL).” *Id.* Since the source line is commonly connected to the ground terminal, SGS is also known as the “ground select transistor” or the “lower select gate.” Word lines are connected to each memory cell control gate. *Id.*, 38-39. A schematic representation of a memory string is shown below:



Ex. 1015, 39.

49. Various architectures for constructing 3D NAND flash memory were known in the art. One such example is the well-known BiCS (Bit Cost Scalable) architecture, where various “contacts” (electrical connections) are formed on top of the memory array. Below are two illustrations of the BiCS architecture show top and bottom perspective views.

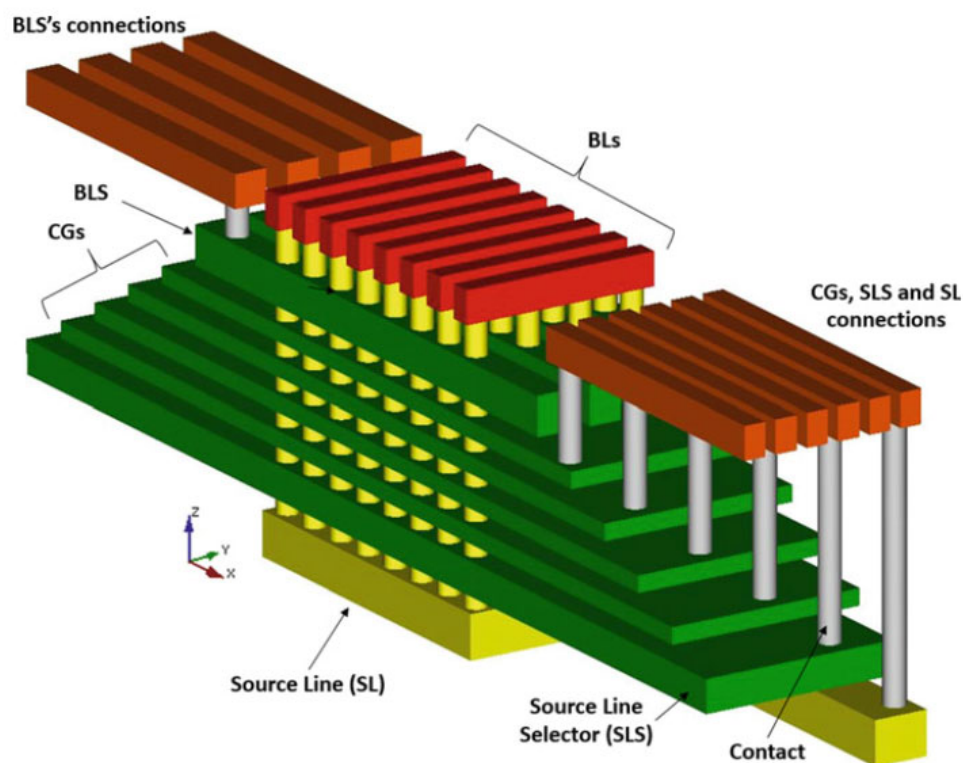


Fig. 4.13 Top bird's eye view of BiCS with gate connections

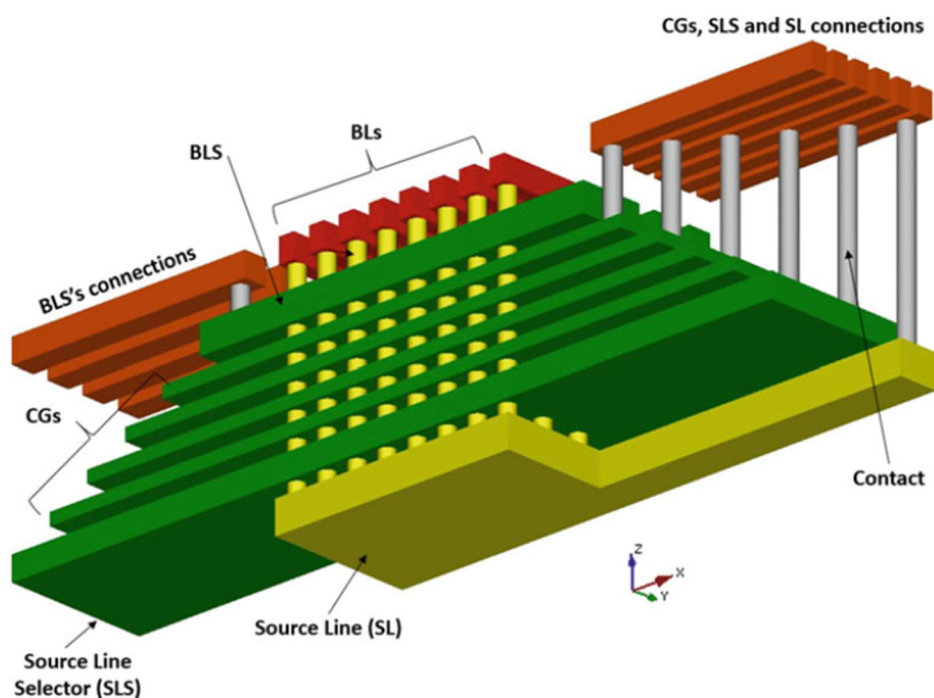


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1010, 109-110. As is traditional in MOSFET transistors, the “source” terminal connects to a low voltage, such as ground. The same holds true in 3D NAND design, and the BiCS architecture includes source line contacts for providing a low voltage (e.g., ground) connection to the memory strings. This is shown in yellow in the figures above.

50. As can be seen above, the source line contact does not travel directly through the memory stack. It was well known, however, to form contact directly through the memory stack by forming a hole in the stack, an insulating line in the hole, and filling the hole with a conductive material. I provide a several examples below:

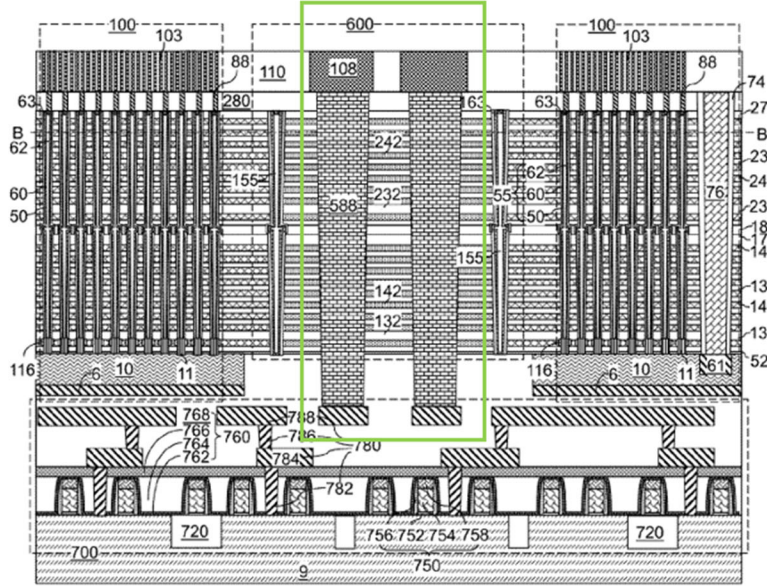


FIG. 69A

Ex. 1011 (Toyama), Title (“Through-Memory-Level Via Structures”), [0367], Fig.

69A (588) (annotated) ¹.

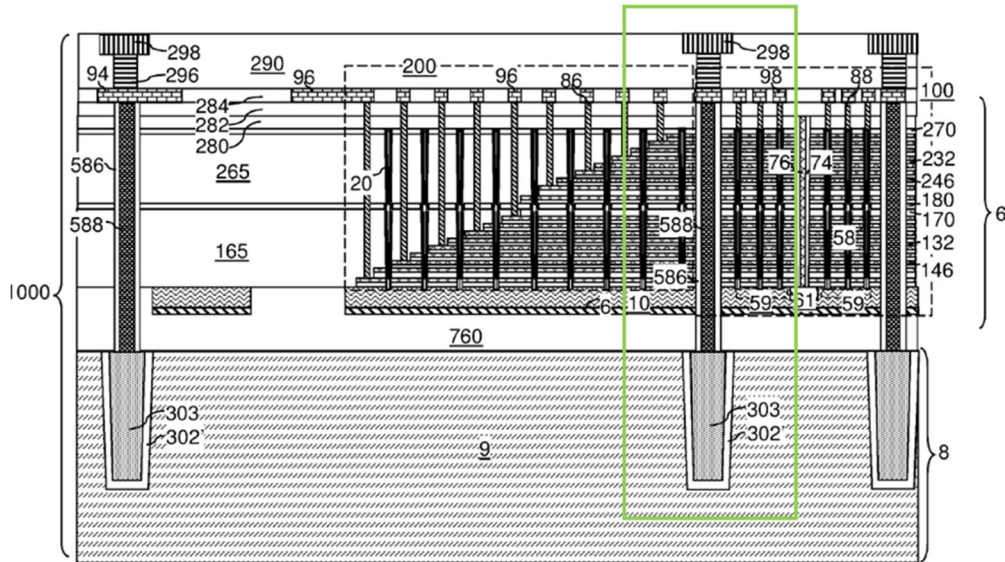
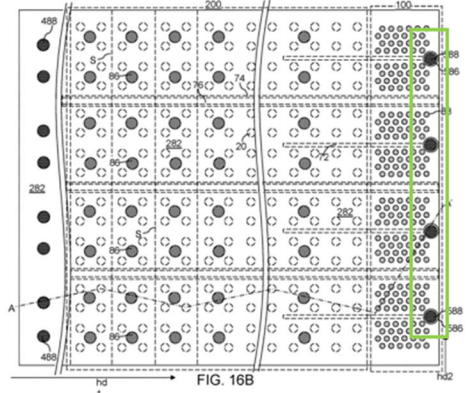


FIG. 5

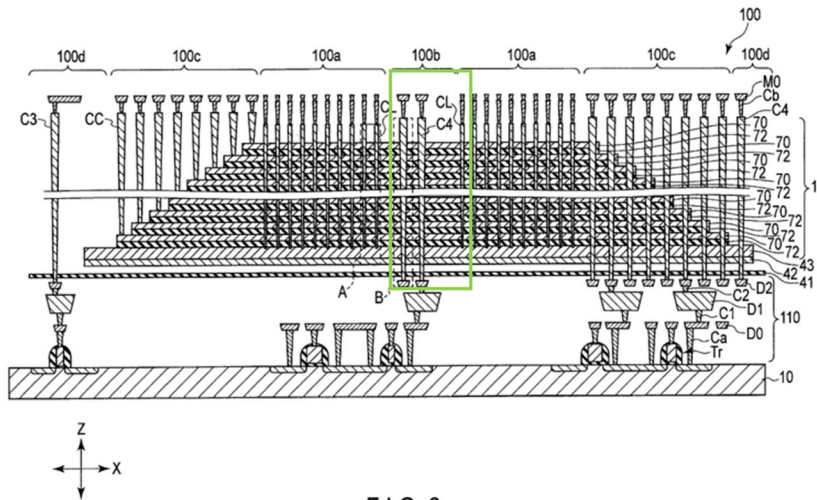
Ex. 1012 (Mushiga), 10:31-58, Fig. 5 (588).

¹ Annotations added throughout unless noted.

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Ex. 1008 (U.S. Pat. Pub. 2019/0229125), [0189], Figs. 16A, 16B (588).



Ex. 1009 (Nakajima), Figs. 1-2, 6:45-52.

51. The individual memory cells in a memory string are accessed by word lines that typically extend horizontally and connect to a control gate for a given cell on each memory string. On the periphery of the 3D NAND device, the word lines

form a staircase structure, where each subsequent word line protrudes a short distance beyond the word line above it, like a staircase, as shown below in green.

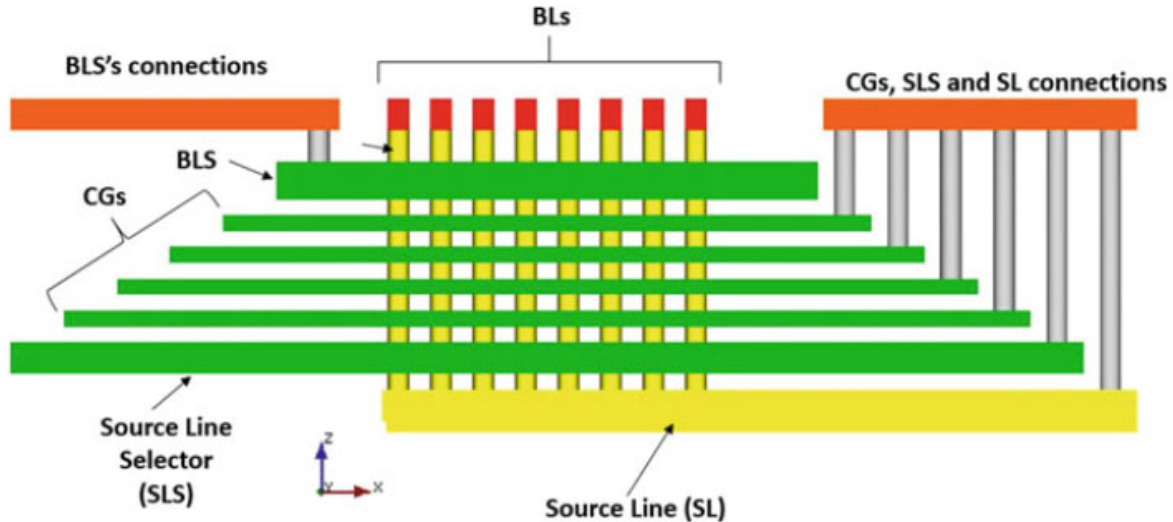


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1010, 109 (green control gates forming a staircase). As noted, each word line delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device.

52. The collection of memory cells controlled by a common signal together constitute a “word,” and the control gate is a “word line.” *Id.*; Ex. 1015, 38-40. The grey columns in the figure above, often referred to as “local contacts,” show how the word lines can be controlled by signals on the top surface of the 3D NAND device. In the context of 3D NAND chips, “local contacts” refer to the electrical connections made within the memory device to link various components such as the word lines and source lines. In facts, local contacts are also often referred to as “vias,” which

have been widely known and used in all sorts of semiconductor devices for many decades. These vias create vertical electrical connections between the different layers within the 3D NAND stack. They are integral to the architecture of semiconductor devices generally, including 3D NAND technology where they enable the functional linkage of stacked memory cells across multiple layers. Note that these local contacts can be of various lengths – some long and some very short. For example, the local contacts (the grey columns in the figure above) that connect to the word lines located near the top of the memory stack are very short while the grey column that connect to the source line is much longer. Where local contacts are connecting an existing vertical structure, such as a memory string or slit, the local contacts tend to be relative short.

53. A variety of modifications to the BiCS architecture were known, including the use of slit structures to serve as source line contacts for the NAND strings. Exemplary slit structures are shown in purple below. These particular slit structures function as contacts for connecting to the source (which may be shared by some, or all, memory strings) located on the bottom of the 3D NAND device. Because slits have an insulating liner, they can separate the array into blocks, which are units of the array.

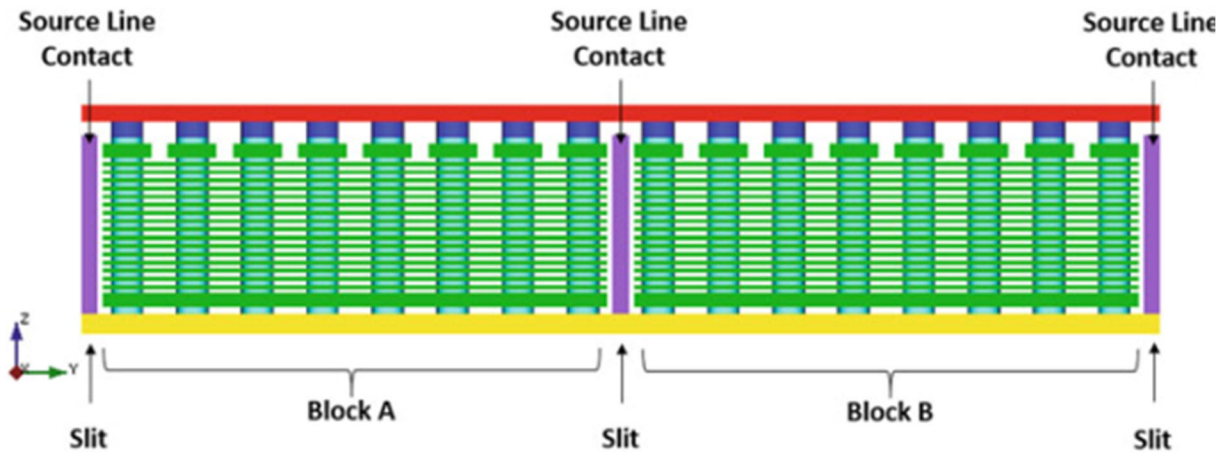


Fig. 6.8 Side view of Fig. 6.7

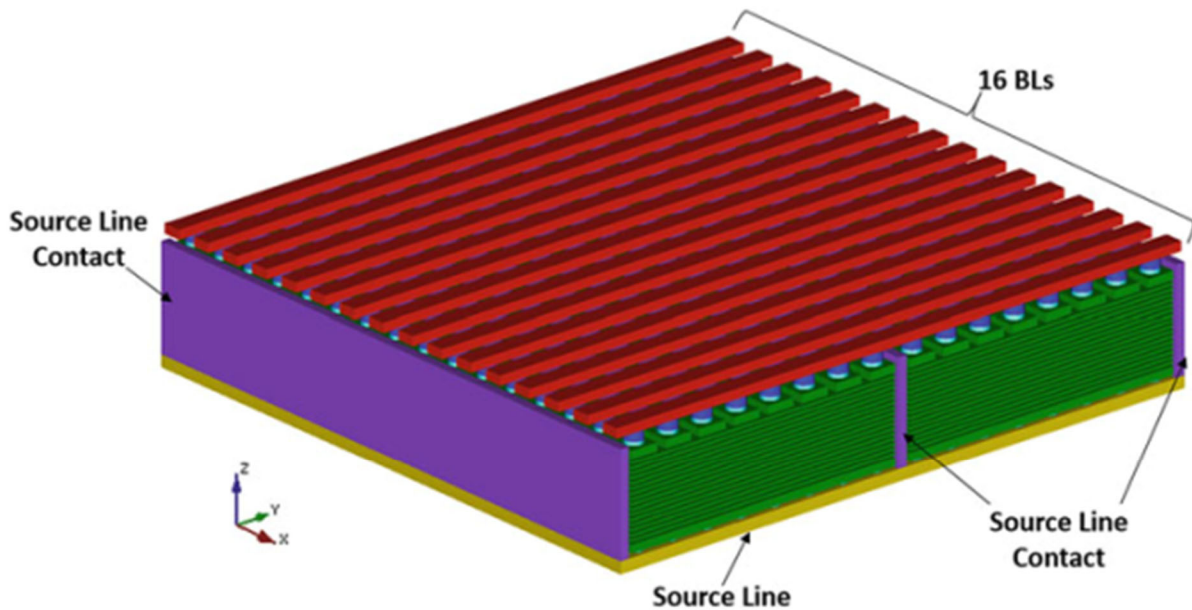


Fig. 6.7 Array slits

Ex. 1010, 185.

54. In both figures above, gaps are shown between the various structures. In actual 3D NAND memory devices, these “gaps” are not empty space; rather, they are filled with insulating material (known as “dielectric” material). Among other

things, dielectrics serve to isolate electrical signals and prevent one conductive structure from interfering with another other. Another function performed by the dielectric is mechanical support to prevent the other structures from collapsing.

55. Well before the effective filing date of the '254 Patent, companies (including Micron) had developed various techniques for manufacturing 3D NAND flash memory, many of which leveraged fabrication principles and materials that had been in use generally in the semiconductor manufacturing industry for decades.

56. The fabrication of 3D NAND memory chips involves etching techniques to construct vertical, high-density storage architectures. These etching processes, fundamental to semiconductor manufacturing, have been well established prior to 2018 but have been adapted for 3D NAND. Here are just a few examples of etching processes used for 3D NAND. Channel hole etching which typically makes use of a dry etching process, e.g., deep reactive ion etching (DRIE) to create vertical channels through the NAND stack. DRIE was developed in the mid-1990s, allows for etching with high aspect ratios, essential for the vertical structures in 3D NAND. Staircase etching involves sequential etching steps to create a staircase-like structure for accessing word lines across each memory layer. This process leverages standard lithographic and etching techniques known long before 2018, adapted to create the precise, repetitive structures needed for multi-layer access. Hard-mask etching process, well-known long before 2018, involves depositing a durable

material like nitrides which is then patterned using photolithography to serve as a mask. The hard mask protects underlying layers during subsequent etching. Selective etching is used to remove specific materials without damaging others by using different chemistries in plasma to target certain layers of materials, again was well-known long before 2018. Spacer etching which involves depositing and then partially removing the material developed to define narrow, uniform spacers (gaps) for cell isolation. Spacer etching processes was developed for lightly-doped drain (LDD) MOSFETs back in the 1980's and adapted for 3D NAND manufacturing process. Each of these processes originates from fundamental techniques known in semiconductor manufacturing well before 2018, adapted for the advanced architecture of 3D NAND.

57. Stacking multiple chips, also known as 3D integration, was just one of many advancements in semiconductor technology that have happened over the years. The concept of 3D integration should not be confused with 3D NAND. Although 3D integration has application to 3D NAND chips, the concept of vertically stacking multiple dies/chips predates 3D NAND by many years and has been used extensively in a variety of chip technologies. This method significantly enhances device performance and functionality while conserving space, addressing the limitations faced by traditional planar scaling methods. Naturally, when stacking multiple dies on top of one another, via structures (also called through-silicon vias

(TSVs) or through-array contacts (TACs)) were implemented to provide connections between different chips in the stack. I discuss and provide examples of TACs above.

58. In summary, techniques for manufacturing 3D NAND memory devices, including TACs and slits, were well-known in the art before the '254 Patent's effective filing date.

VII. THE '322 PATENT

A. Effective Filing Date

59. I have been instructed to assume the PCT application filing date, August 21, 2018, is the priority date of the '322 Patent.

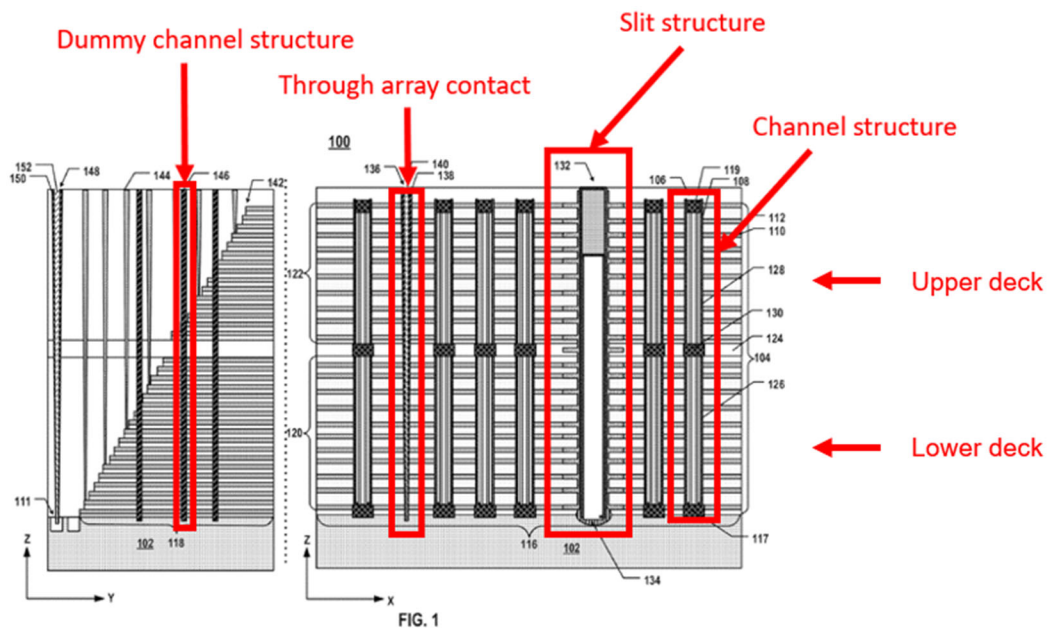
B. Overview

60. The '322 Patent highlights what the specification alleges is the point of novelty: “Three-dimensional memory devices having *through array contacts* and methods for forming the same” and primarily relates to “through array contact[s]” in a 3D memory device. The '322 Patent refers to contacts that extend through the memory stack as “through array contacts” (“TACs”). Such contacts, however, were well known. *See* §VI.

61. The specification of the '322 Patent describes conventional 3D memory structures in addition to the TACs: channel structures (memory strings), dummy channel structures (inactive memory strings), peripheral contacts (contacts outside of the array), slits (long lateral openings in the stack), and multi-deck memory stacks

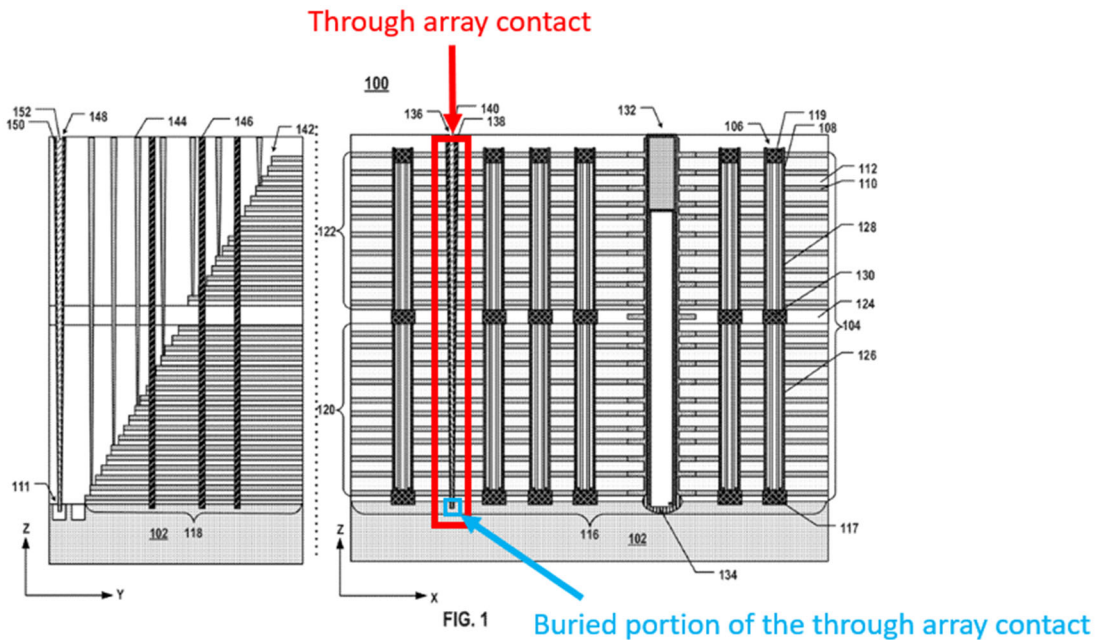
(effectively memory stacks on top of one another). Ex 1001, 6:49-61-7:4 (channels), 7:42-60 (multi-deck memory stack), 9:29-51 (dummy channels), 8:3-18 (slit structures), 9:52-10:8 (peripheral contacts).

62. Fig. 1 of the '322 Patent illustrates channel structures 106, a slit structure 132, a through array contact 146, and a dummy channel structure 146 in a 3D multi-deck memory stack.



Ex. 1001, Fig. 1 (annotated).

63. The specification describes that “[i]n some embodiments, TAC 136 further extends through at least part of substrate 102.” Ex. 1001, 8:37-38. This description corresponds to the “buried” claim limitation. As shown below, a portion of the TAC depicted below extends below the surface of a substrate and terminates in the substrate:



Id., Fig. 1 (annotated).

64. The '322 discloses that “[i]n some embodiments, 3D memory device 100 further includes slit structures 132. Each slit structure 132 can extend vertically through the conductor/dielectric layer pairs in memory stack 104. Slit structure 132 can also extend laterally (e.g., in the y-direction) to separate memory stack 104 into multiple blocks.” Ex. 1001, 8:3-8. In other word, the slit is a trench in the memory stack, and the slit structure fills that trench.

65. The claims do not recite any function of the slit structure or any specific material of the slit structure. The '322 Patent states that in some embodiments, the slit structure may function as a source contact, e.g., by comprising a conductive material that contacts the substrate. *Id.*, 8:8-29. A source contact electrically couples a source voltage to the substrate (to which the source side of the channel structures

connect). In some other embodiments, the slit structure separates the memory stack into multiple blocks or fingers, aiding in electrical isolation and enabling localized memory operations. *Id.*, 8:3-18.

C. Prosecution History

66. The 322 Patent is a divisional of App. No. 16/745,342. Ex. 1001, Cover. The pending claims in the divisional included the TAC limitation, but without the TAC being buried, and these claims were rejected over U.S. Publ. 2012/0280304 (“Lee 304”). Ex. 1016, 114-15. Lee 304 disclosed a TAC that was a common source line in a trench shape. Recall this TAC provides a source voltage to the substrate. This TAC not a circular TAC. *Id.*; Ex. 1017 (Lee 304), Fig. 23, [0051], [0058]-[0059], [0095]. Applicant amended the claims to require that each conductive layer of the memory stack have a “shallow recess,” and the claims were allowed. Ex. 1016, 148, 153, 157, 166.

67. I will now summarize the file history of the ’322 Patent. The original claims did not include the “buried” or “slit” limitations (but did include a dummy channel limitation). Ex. 1002, 20. The claims were rejected over Lee 304 in view of U.S. 2017/0125430 (Ex. 1018, “Nishikawa 430”). *Id.*, 100-01. The rejection asserts that Lee 304 discloses the TAC and Nishikawa 430 discloses a dummy channel structure. *Id.*, 101.

68. After an Examiner Interview, Claim 1 was amended to also require a peripheral contact and that the thickness of the spacers for the peripheral contact and TAC be the same. Ex. 1002, 145-46, 149-152. Similar additional claims were added. *Id.*, 149-52. Applicant attempted to distinguish the claims based on the spacer limitation. *Id.*, 155. The Examiner rejected the claims again in view of Lee, Nishikawa 430, and U.S. 2015/0348987 (Ex. 1019, “Lee 987”). Ex. 1002, 162-163.

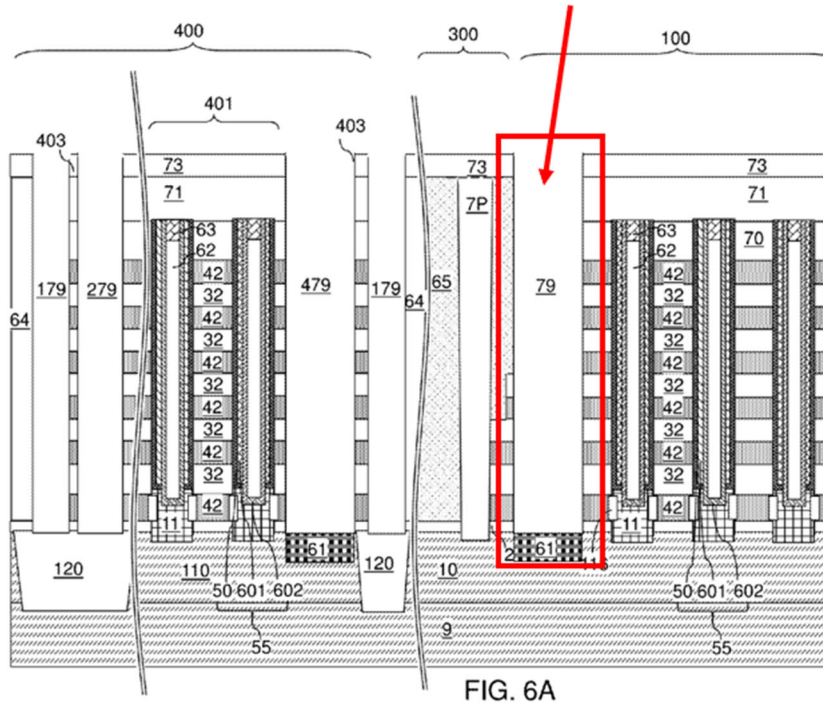
69. After an Examiner Interview, claim 1 was amended by deleting the dummy channel, peripheral contact, and spacers’ thickness limitations, and by adding the “buried” and “slit” limitations. Ex. 1002, 210, 216. Claim 10 was amended to require a circular TAC, and Claim 17 was amended to require a TAC with a diameter. *Id.*, 217, 219.

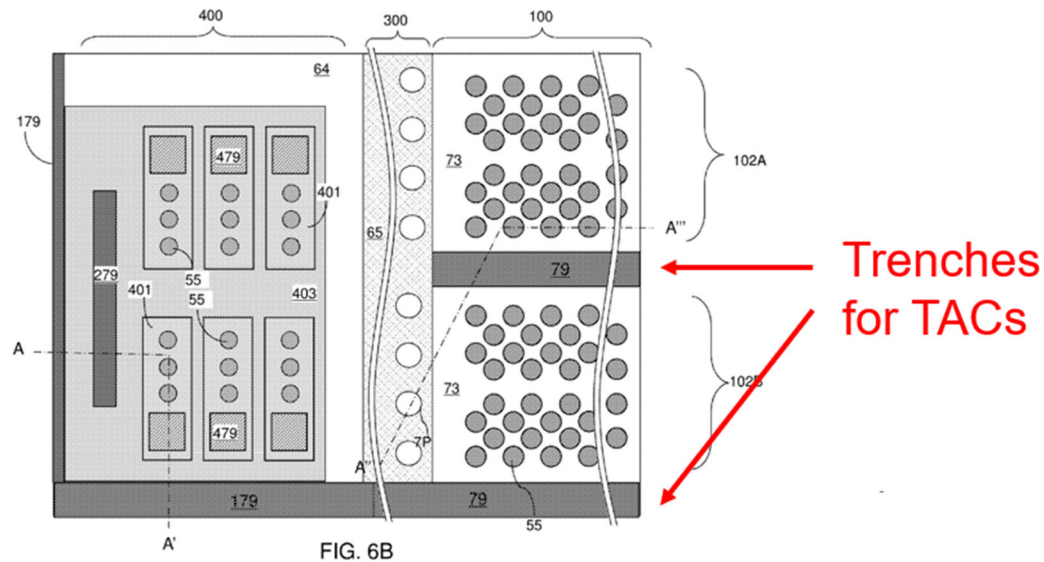
70. Applicant noted that the Examiner agreed that Lee 304 did not disclose a TAC buried in the substrate. *Id.*, 223. This appears to be in error. Lee 304, [0058] (describing that source line 170 may physically contact impurity region in “semiconductor layer 100”). Lee 304’s TAC was a source line contact that is buried into the substrate because it provides a source voltage to the substrate, and the source side of the channels connect to this source voltage (the substrate becomes a common source region).

71. Applicant noted that during the Interview, the Examiner cited Nishikawa 430’s opening 79 as the TAC buried in the substrate. Ex. 1002, 223.

Nishikawa 430's opening 79 is a trench and becomes a TAC (with an insulating spacer and conductive core). This TAC is buried into the substrate to function as a source line connection:

Trench for TAC





Nishikawa 430, Fig. 6A, [0084], [0086]. [0113]-[0115] (trench structure becoming “memory active region contact structures 76”).

72. Applicant argued that the prior did not disclose the combination of a TAC buried in the substrate *and* a slit that separates the array. Ex. 1002, 222-23. As shown above, there is no other slit in Nishikawa 430 except the TACs. Thus, the Examiner apparently found that Nishikawa was missing the combination of a TAC and slit.

73. For the two remaining independent claims (with the requirement that the TAC be circular), Applicant argued that the circular TAC requirement distinguishes Nishikawa 430’s TAC and the other prior art TACs. *Id.*, 223-24.

74. The claims were then allowed. The Examiner noted the alleged distinguishing requirements of Claim 1: the buried TAC *and* slit limitations. Ex. 1002, 249. For Claims 10 and 17, the Examiner noted that the circular requirements

led to allowance. *Id.*, 250. The Examiner noted that nothing in the prior art of record suggested using a circular TAC. *Id.* In my opinion, the Examiner clearly erred because circular TACs were well known.

D. Summary of Grounds for Invalidity: Nishikawa Grounds

75. Nishikawa, combined with the knowledge of a POSITA (and Lu for Claims 4-5, 12-12, and 17-18), renders Claims 1-20 of the '322 Patent obvious. Specifically, Nishikawa's teachings and the knowledge of POSITA would motivate a POSITA to apply known techniques to yield a predictable result, achieving the claimed invention with a reasonable expectation of success. The methods outlined herein leverage predictable, routine practices and widely adopted techniques in semiconductor fabrication, particularly for high-aspect-ratio structures. A POSITA would recognize these implementations as industry-standard approaches, derived directly from well-documented methods and widely recognized for their reliability and effectiveness in achieving the claimed outcomes.

76. Nishikawa2 confirms the knowledge of a POSITA.

VIII. CLAIM CONSTRUCTION

77. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand

that during an inter partes review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

78. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the “intrinsic evidence” or “intrinsic record”).

79. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the “extrinsic evidence” or the “extrinsic record”), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

80. In my opinion, the challenged claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

IX. UNPATENTABILITY ANALYSIS

81. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '322 Patent, Claims 1-20 of the '322 Patent are unpatentable as obvious over the prior art discussed in this declaration.

A. Overview of the Prior Art

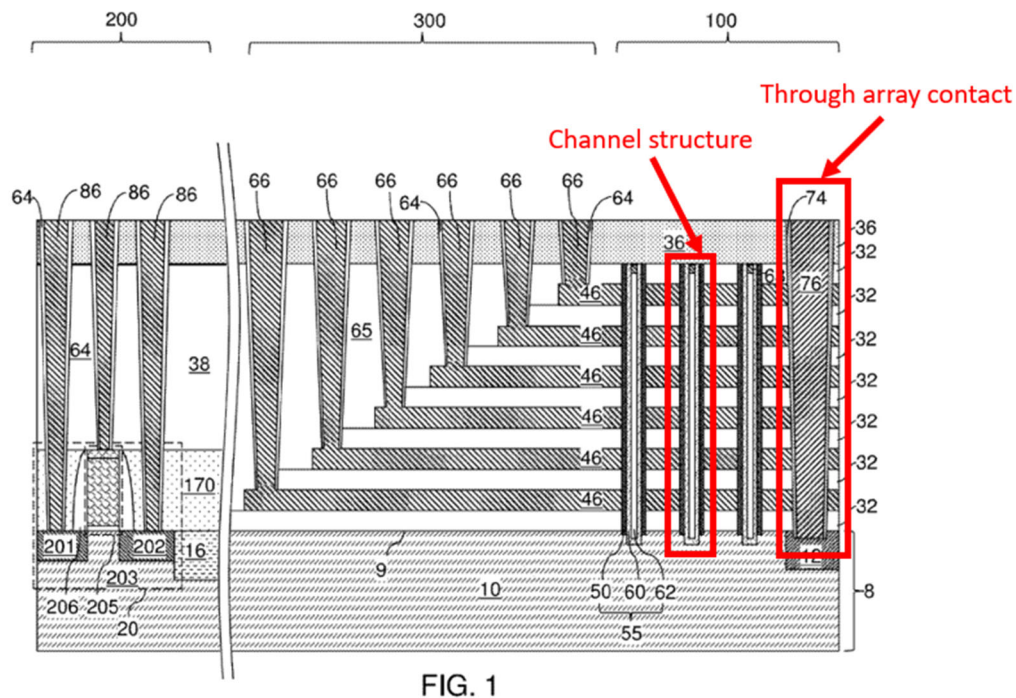
82. The following paragraphs provide an overview of the primary references that I discuss throughout this declaration.

1. Nishikawa

83. U.S. Patent No. 9,837,431 to Nishikawa et al. was filed on January 28, 2016, was issued on December 5, 2017, and claims priority to a provisional application filed on November 20, 2015. I understand that Nishikawa is prior art to the '322 Patent.

84. Nishikawa relates to 3D NAND. Nishikawa, 1:15-19. Like the '322 Patent, Nishikawa discloses that its 3D NAND device includes a TAC through the memory stack that is buried in the substrate (as I will describe, this structure provides a source connection to the substrate).

85. Nishikawa discloses TAC (“backside contact via structure 76”) and channel structures (“memory stack structures 55”):



Nishikawa, Fig. 1 (annotated), 6:3-6 (discussing memory stack structures 55), 6:54-59 (discussing the backside contact via structure 76). As I highlight below, the “backside contact via structure 76” is buried into the substrate:

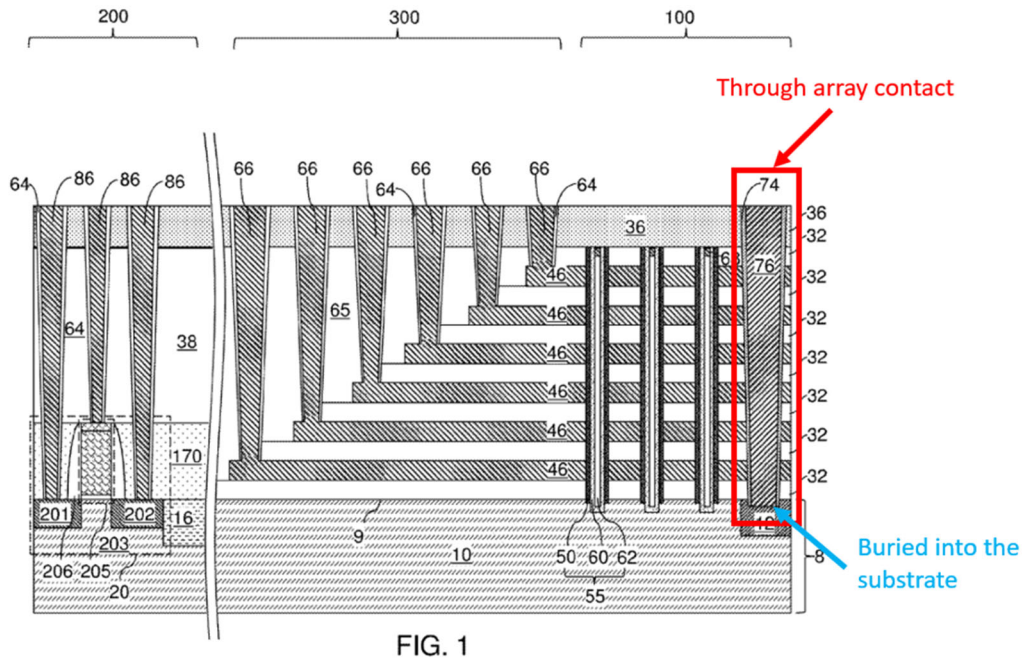
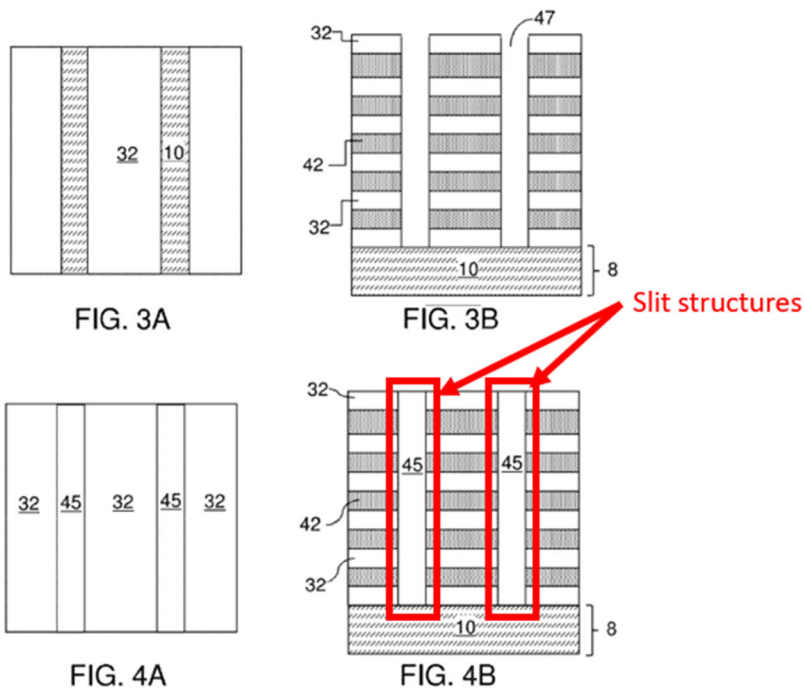


FIG. 1

Nishikawa, Fig. 1 (annotated). The TAC 76 extends into source region 12. As can be seen above, this provides a source connection to the substrate, which provides a common source for the channel structures. Nishikawa, 5:16-25. I describe these source connections in my overview of the background technology. Recall that memory strings typically connect to a drain voltage on top (e.g., via bit line) and source voltage on the bottom (e.g., via the substrate)

86. Nishikawa also discloses slit structures (“separator dielectric structures 45”):

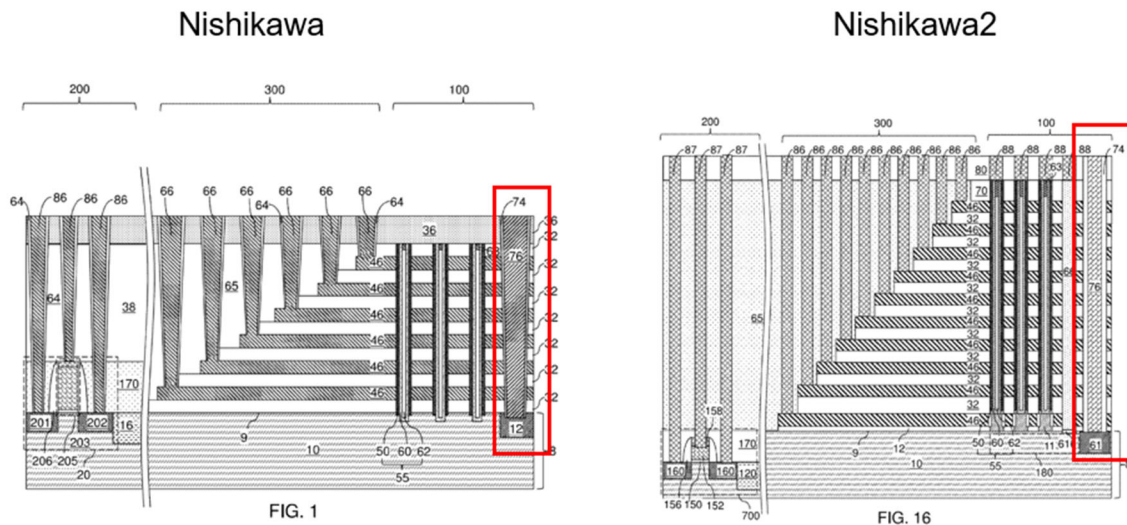


Nishikawa, Figs. 3A-B, 4A-B (annotated). Figure 4B shows the slits extending vertically through the stack, thereby separating the gate layers. Figures 4A shows a top-down view, illustrating that the slits extend laterally throughout the array.

87. Separator dielectric structures 45, as the name implies, divide the memory into multiple memory zones: “Each separator dielectric structure 45 can extend through the alternating stack (32, 42), i.e., from the top surface of the substrate 8 to the top surface of the alternating stack (32, 42). Thus, the alternating stack (32, 42) as formed at the processing steps of FIGS. 2A and 2B is divided into multiple laterally disjointed portions by the separator dielectric structures 45, each of which comprises discrete portions of the alternating stack (32, 42).” Nishikawa, 8:36-43; *see also id.*, 8:57-60, 9:1-24, 13:18-22, 14:52-15:3, 17:24-27. This was a

embodiments in which the channel structures do not extend through the separator 47 structures, but as can be seen above, both references disclose an embodiment where the channel structures are made partially within the separator 47 structures.

91. Both Nishikawa and Nishikawa2 also include common source lines 76, which as I discuss later, Nishikawa2 expressly states may be “circular.” This was, however, already well known in the prior art.



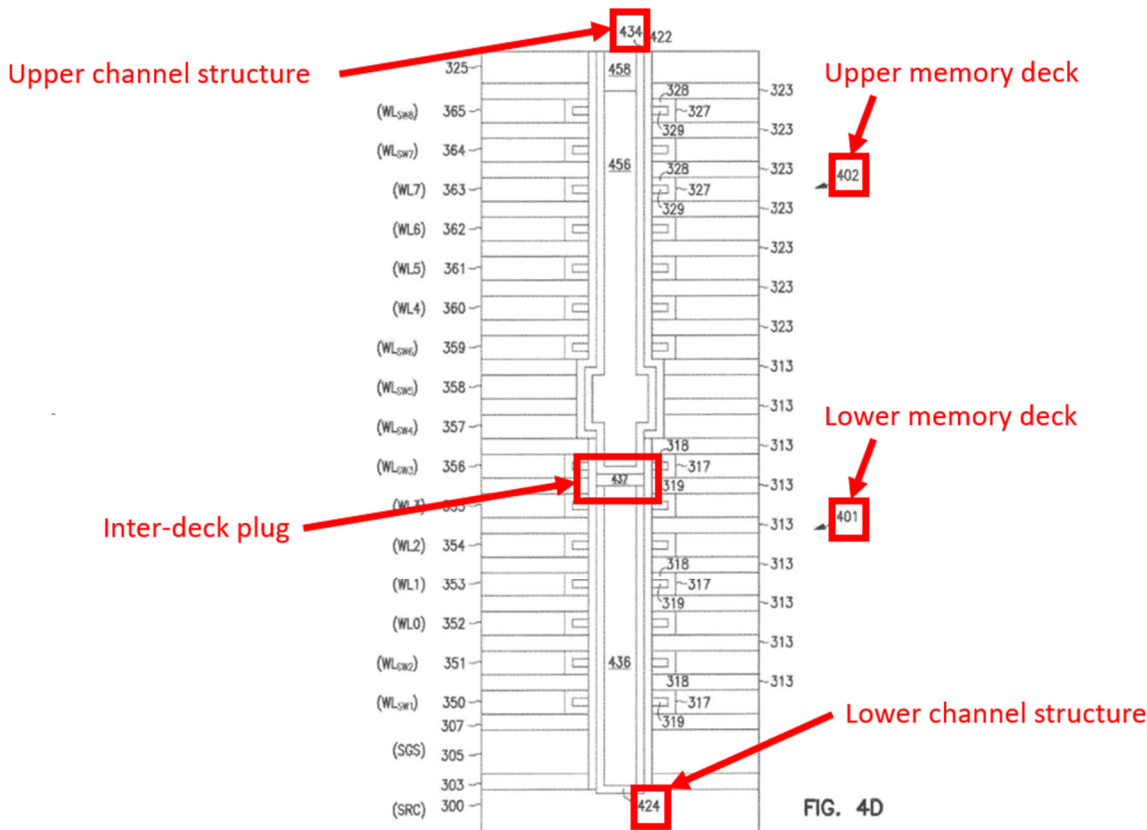
Nishikawa, Fig. 1; Nishikawa2, Fig. 16, 22:34-38 (source line connection), 23:59-67 (insulating spacer 74), 24:24-39 (forming “backside contact via structure 76” in “backside trench 79”). Specifically, Nishikawa2 discloses that “The openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape.” *Id.*, 22:38-41.

3. Lu

92. U.S. Patent No. 9,853,046 to Lu et al. is titled “Apparatuses and Methods for Forming Multiple Decks of Memory Cells” was filed on June 6, 2016, issued on December 26, 2017, and is a division of U.S. Application No. 14/509,621 filed on October 8, 2014. I understand that Lu is prior art to the ’322 Patent.

93. Lu relates to 3D memory and, specifically, multi-deck memory stacks (see below discussion). Lu, 7:42-46

94. Lu discloses a memory stack where each channel structure includes an upper channel structure and a lower channel structure (with an inter-deck plug between the upper and lower structures). Lu, 14:13-61.



Lu, Fig. 4D (annotated). I discuss in detail the motivations for employing multi-deck structures. But in short, a multi-deck structure can increase memory density by enabling the formation of high-aspect ratio channel holes through a memory stack with a large number of layers.

B. Ground 1: Nishikawa in View of the Knowledge of a POSITA
Render Obvious Claims 1-3, 6-10, 13-16, and 19-20

1. Claim 1:

[1.PRE] “A three-dimensional (3D) memory device, comprising:”

95. While not offering an opinion on whether the preamble is limiting, Nishikawa discloses it. Nishikawa describes in figures 1-17 and the accompanying

text “an exemplary device structure containing a 3D NAND stacked memory device.” *E.g.*, Nishikawa, 2:3-3:41; *see also id.*, 1:15-19 (“three-dimensional non-volatile memory devices, such as vertical NAND strings and other three-dimensional devices, and methods of making the same”), 4:22-24 (“3D NAND stacked memory device[s]”).

[1.A] “a substrate;”

96. As I describe below, Nishikawa discloses a substrate (“substrate 8”).

97. Nishikawa discloses that the “substrate 8” includes a “substrate semiconductor layer 10” (Nishikawa, 4:43-56) and a “source region 12” (*id.*, 5:16-18). The source region 12, as shown below, provide an area for the source line connection (TAC 76) to connect to the substrate.

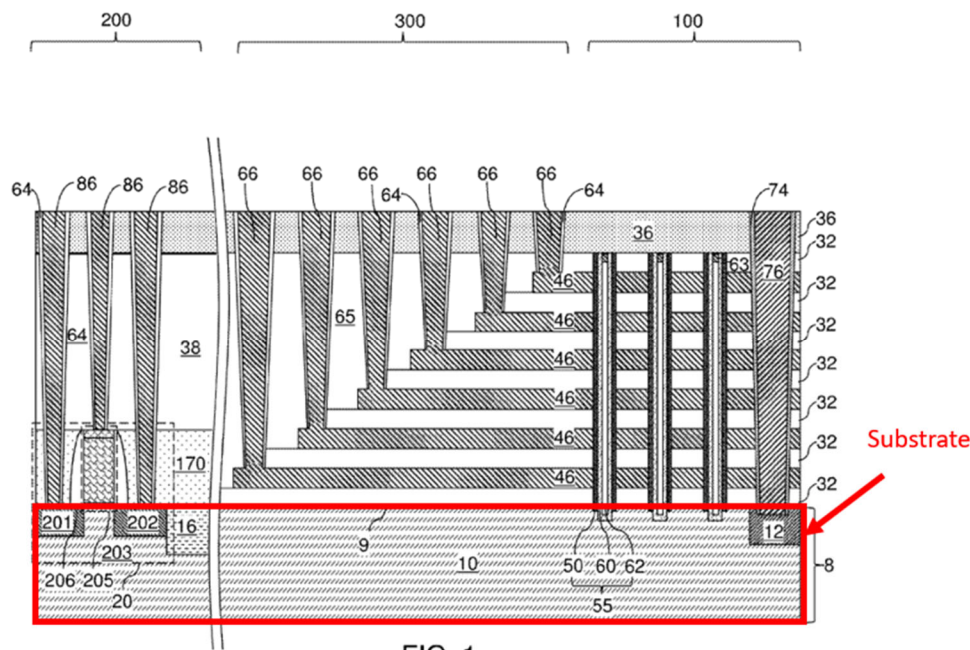


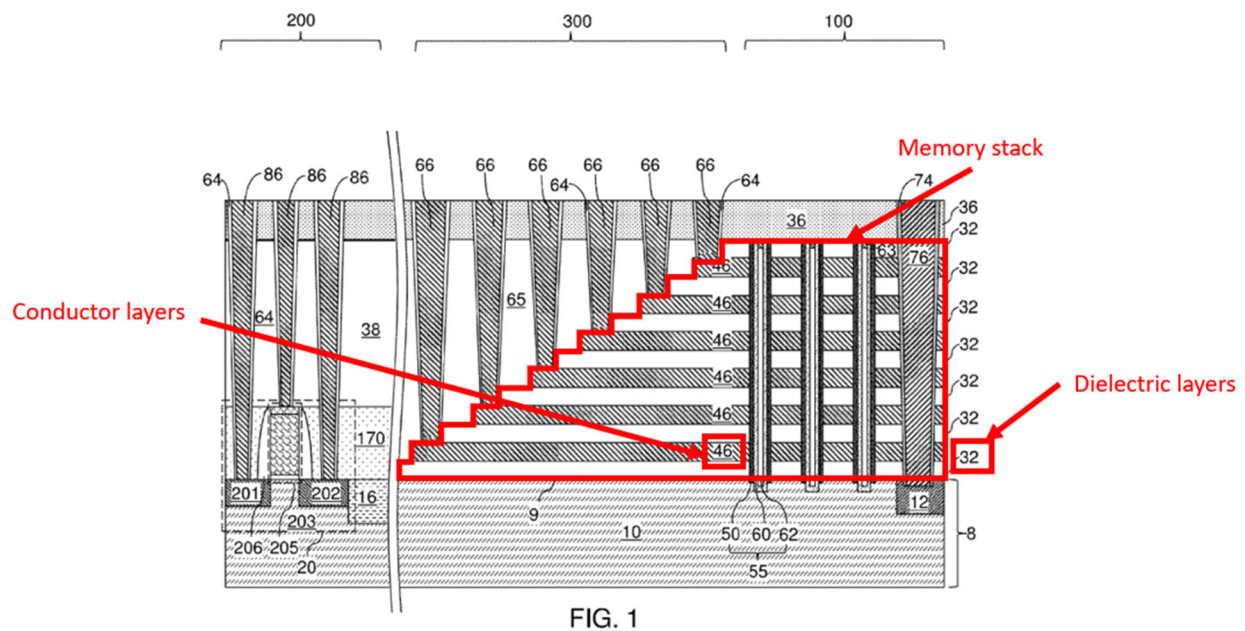
FIG. 1

Id., Fig. 1 (annotated).

[1.B] “a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;”

98. As I describe below, Nishikawa discloses a memory stack (“alternating stack”) on the substrate (“substrate 8”) and comprising a plurality of conductor (“electrically conductive layers 46”)/dielectric layer (“insulating layers 32,” e.g., silicon oxide) pairs

99. Nishikawa discloses the conventional memory stack for a 3D NAND of alternating conductor and dielectric layers. Specifically, Nishikawa discloses an “alternating stack (32, 46) of the insulating layers 32 and the electrically conductive layers 46.” Nishikawa, 6:4-5.



Id., Fig. 1 (annotated). The insulating (dielectric) layers 32 and the conductor layers 46 are formed alternatively on the top surface of the substrate 8. Nishikawa, 5:50-6:2. The alternating insulating (dielectric) layers 32 and conductor layers 46 form

pairs in the alternating stack. Each conductor layer is a gate layer, i.e., word line. The word line interface with the channel structures at memory cells. The dielectric layers isolate the gate layers.

100. Nishikawa discloses that the dielectric insulating layer 32 can be formed using, e.g., “silicon oxide.” Nishikawa, 7:3-16. The typical material for these dielectric layers in a 3D NAND were silicon dioxide.

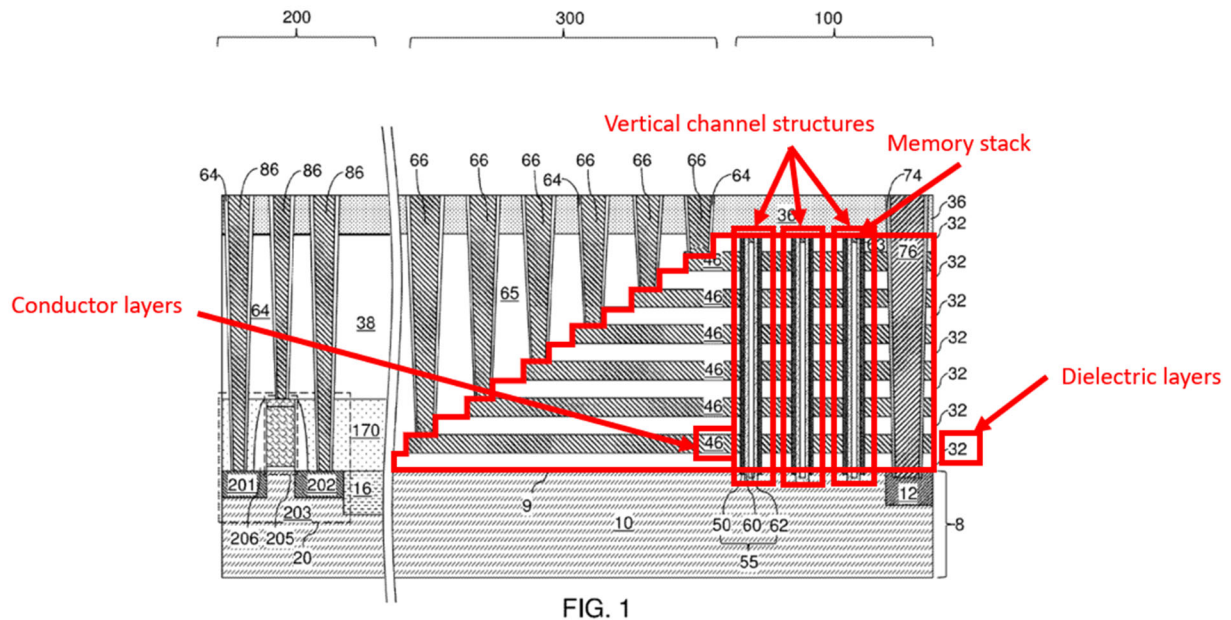
101. Nishikawa further discloses that “memory stack structures 55 can be formed through the alternating stack (32, 46) of the insulating layers 32 and the electrically conductive layers 46[.]” Nishikawa, 6:3-8. As illustrated in annotated Fig. 1, above, the memory stack of Nishikawa is coextensive with the alternating stack of insulating layers 32 and electrically conductive layers 46. In other words, the memory stack is the alternating conductive layers (gate layers) and dielectric layers after fabrication, e.g., after forming the staircase which removes portions of the initial memory stack. Again, the memory stack structures (memory strings) are strings of memory cells, with memory cells being at the intersection of gate layers and the channel structures.

[1.C] “a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;”

102. As I describe below, Nishikawa discloses a channel structure (“memory stack structure 55”) extending vertically through the conductor (“electrically

conductive layers 46”)/dielectric (“insulating layers 32”) layer pairs in the memory stack (“alternating stack”).

103. The memory stack structure[s] 55 of Nishikawa are channel structures:

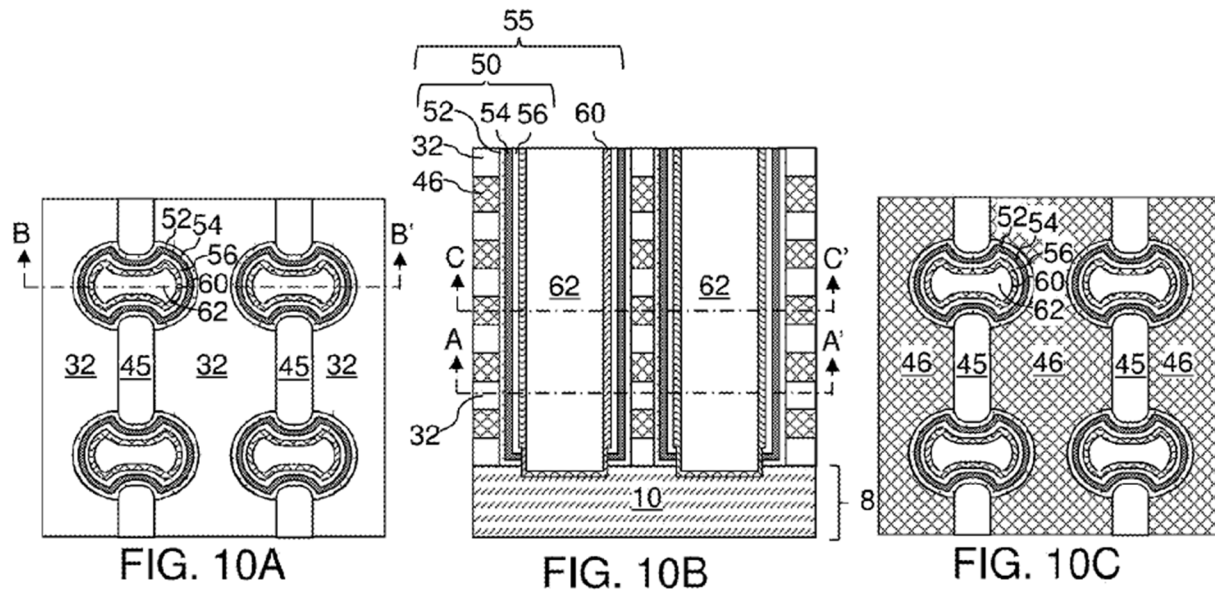


Nishikawa, Fig. 1 (annotated).

104. Each memory stack structures 55 includes a vertical semiconductor channel 60. Nishikawa discloses the layers of the memory stack structures: “[r]eferring to FIGS. 10A-10C, a memory stack structure 55 (i.e., structure having layers (52, 54, 56, 60)) including a memory film 50 (i.e., film having layers (52, 54, 56)) and a vertical semiconductor channel 60 can be formed in each of the memory openings 49. Each memory film (52, 54, 56) can include, from outside to inside, a blocking dielectric layer 52, charge storage regions 54, and a tunneling dielectric 46.” Nishikawa, 11:33-39. These various layers for the memory channel structure

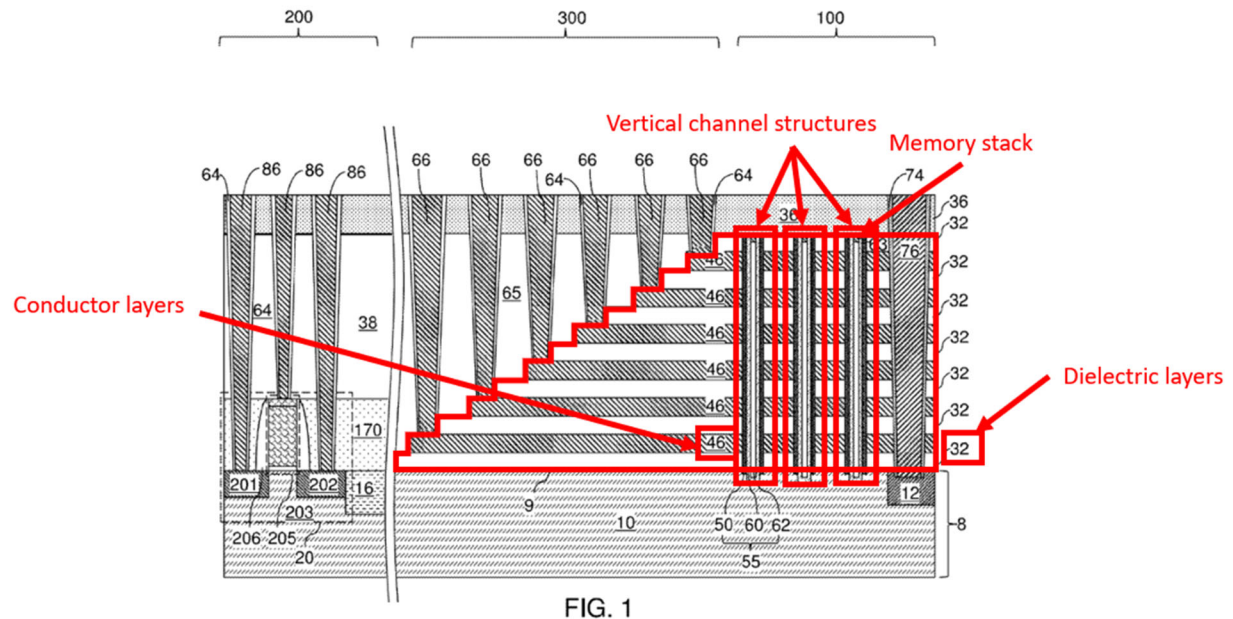
enable the memory channel structure to store information. The charge storage region stores charge. The blocking and tunneling layers function to inject and remove charge from the charge storage region

105. Figures 10A-C depict the layers of the channel structures:



Nishikawa, Figs. 10A-C.

106. Second, the channel structures of Nishikawa (“memory stack structure[s] 55”) extend vertically through the conductor /dielectric layer pairs in the memory stack. Nishikawa, 6:3-5 (“The memory stack structures 55 can be formed through the alternating stack (32, 46) of the insulating layers 32 and the electrically conductive layers 46”). This is because the gate layers interface to the channel structures and operate as word lines to effectuate access operations on the memory cells of the memory strings:



Nishikawa, Fig. 1 (annotated).

107. The channel structures extend from the top of the stack and into a source region the substrate. Nishikawa, 5:16-25. The top of the memory structure will connect to a drain voltage (e.g., via bit line) and the bottom of the memory structure connects to the source voltage in the substrate (e.g., in the common source region of the substrate).

[1.D] “a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate; and”

108. As I describe below, Nishikawa discloses a through array contact (TAC) (“backside contact via structure 76” and “dielectric spacer 74”) extending vertically through the conductor (“electrically conductive layers 46”)/dielectric

(“insulating layers 32”) layer pairs in the memory stack (“alternating stack”) and buried into the substrate (“substrate 8”).

109. I will first address how the specification of the ’322 Patent describes a TAC. The ’322 Patent states that a TAC “can include a vertical opening through memory stack 104 and that is filled with filling materials,” and further explains that “TAC 136 includes a spacer 138 on a sidewall of the opening and a conductor layer 140 in contact with spacer 138 in the opening.” Ex. 1001, 8:47-51 and Fig. 1. In other words, as the name TAC implies, a TAC extends through the stack and includes a spacer and filling material. That is, it is a contact through the array. The insulating spacer insulates the conductive core from, e.g., the gate layers.

110. First, Nishikawa discloses “[a] backside contact via structure 76 (e.g., source electrode/source local interconnect) can be formed through the alternating stack (32, 46) to provide electrical contact to the source region 12. A dielectric spacer 74 can be employed to provide electrical isolation for the backside contact via structure 76.” Nishikawa, 6:54-62 and Fig. 1. Nishikawa refers to “source electrode/source local interconnect” to mean that contact via structure 76 provides a connection to a source voltage above the substrate, through the stack, and down to the substrate (a common source region). *Id.*, 16:6-13 (providing source voltage to common source region of substrate); *see also* Ex. 1010, 109-110 (illustrating a common source contact). I discuss this extensively in the background technology

section. This TAC provides a source voltage to the substrate, and the channel structures connection to this source voltage in the substrate.

111. Contact via structure 76 would have been understood to include a conductive fill, e.g., tungsten. This is because the contact via structure electrical couples the source voltage to the substrate. Also, Nishikawa describes providing an insulating liner for the contact because it is conductive, thereby preventing inadvertent coupling to the gate layers. That Nishikawa describes contact via structure 76 as a “contact” is also consistent with it including a conductive core. Nishikawa, 6:54-61, 16:6-13. In summary, the backside contact via structure 76 is a TAC because it includes a spacer and conductive filling material, and extends through each layer of the alternating stack. It also functions to electrically couple a source voltage to the substrate (and in turn, to the bottom of the channel structures).

112. Second, as shown below, the TAC of Nishikawa (74, 76) extends vertically through the pairs of electrically conductive layers 46 and insulating layers 32 and is buried into the substrate 8 (it extends below the surface of the substrate 8 and terminates therein to provide the source connection to the substrate). Nishikawa, 6:54-61, 16:6-13. Again, it is buried into the substrate because it electrically couples the source voltage from above the memory stack to the substrate (and in turn, to the bottom of the channel structures). *Id.* Recall that the top of the channel structures receive a drain voltage.



Nishikawa, Fig. 1 (annotated).

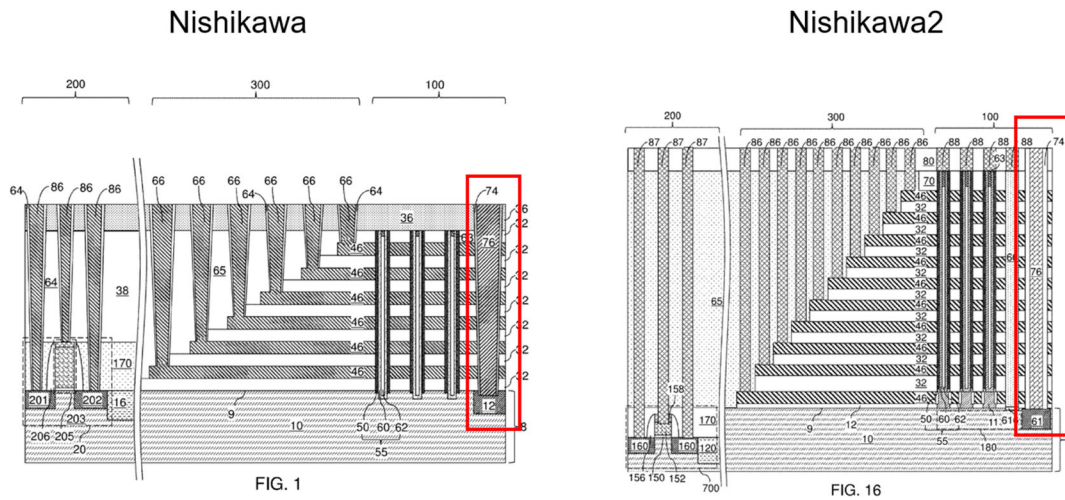
113. In my opinion, a POSITA would not have understood Claim 1 to require a circular TAC or require the TAC to be in any particular location through the stack (other than it being through the memory stack where the channel structures are located). Nishikawa's contact via structure 76 is in the shape of a long trench. Nishikawa, Fig. 16 (illustrating the backside contact via structure 76 as a trench towards the sides of the stack). First, as I discuss above, the '322 Patent describes a TAC without reference to its shape. Instead, it describes that a TAC extends through the stack, has a spacer, and has a filling material. Ex. 1001, 8:47-51. The specification is also silent as to what portion of the stack that TAC extends through. *Id.* In fact, the specification makes clear that the TAC ***only could be*** circular. The

specification states that “[i]n some embodiments, TAC 136 has a substantially circular shape in the plan view, and conductor layer 140 and spacer 138 are disposed radially from the center of TAC 136 in this order.” *Id.*, 8:56-59. A POSITA would have understood, therefore, that in other embodiments, the TAC may assume non-circular shapes. Consistent with this, dependent Claim 6 and Claim 19 require that the TAC have “a diameter” and a “substantially circular section,” respectively. I understand that dependent claims add additional limitations to the independent claim. Thus, a POSITA would have understood that Claim 1 does not require the TAC to have a circular diameter, that is, be circular in shape. Similar to this, other independent Claims (8 and 14) recite a “circular” limitation, but Claim 1 does not. A POSITA would have thus understood that “circular” was not a requirement of a TAC without additional limiting claim language. I also note that in the file history, the Applicant had to amend the claims to add limitations, e.g., the “slit” and “circular” limitations, in view of a TAC that was in the form of a trench shape that provides a source connection. *See* §VII.C. In other words, the Applicant did not argue that Claim 1’s recitation of “TAC” alone was sufficient to distinguish a contact in the shape of a trench. Second, it is also my opinion that it would have been obvious to form Nishikawa’s backside contact via as a circular TAC in the middle of the stack for several reasons.

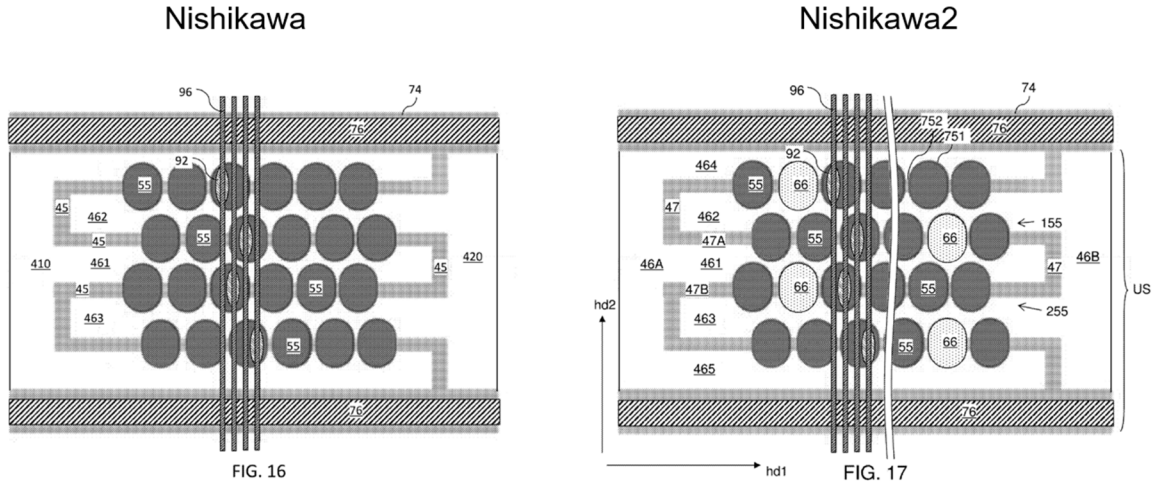
114. It is first important to consider the purpose of Nishikawa's backside contact trench. It *may* serve as the opening for the gate replacement process (to etch out the sacrificial gates and deposit replacement gates), and it functions as a source line contact (providing a source voltage to the substrate). Nishikawa discloses that its invention may or may not use a gate replacement process. Nishikawa, 5:50-61. If employing the gate replacement process, the process may use the trench or the memory openings for the etch of sacrificial gates and deposition of replacement gates. *Id.*, 6:29-44 (gate replacement through trench), 9:58-10:7 (gate replacement through memory openings). Regardless, after any potential gate replacement process, the contact via serves as a common source line. *Id.*, 16:6-12 (source contact). As I describe below, regardless of whether or not using the gate replacement process, replacing the backside contact via with a cylindrical TAC was both known and suitable (in fact, advantageous) in Nishikawa 3D NAND.

115. Nishikawa2 demonstrates the knowledge of a POSITA. Nishikawa2 states that this same TAC (for a common source line connection) may be circular: "The openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape." Nishikawa2, 22:38-41; *see also id.*, 22:34-38 (source line connection), 23:59-67 (insulating spacer 74), 24:24-39 (forming "backside contact via structure 76" in "backside trench 79"). As I describe in §IX.A.1-2, Nishikawa's

and Nishikawa2's TACs are the same structure in the same memory architecture (e.g., peripheral region, staircase, channel region, and separator structures 47):



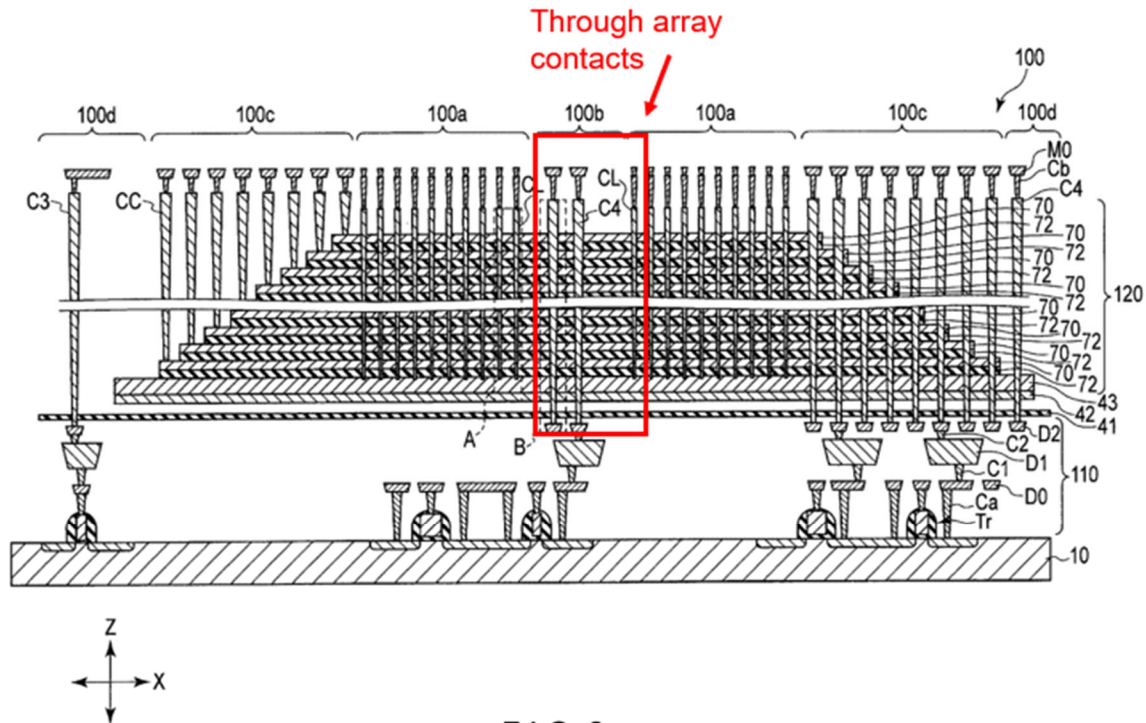
Nishikawa, Fig. 1; Nishikawa2, Fig. 16.



Nishikawa, Fig. 16; Nishikawa2, Fig. 17.

116. It is important to note that circular (or cylindrical) TACs that extend through the stack were widely known in the prior art. Below I provide several examples.

117. Nakajima discloses circular TACs C4 extending through the middle of the memory stack (as well as through other portions):



Nakajima, Fig. 2 (annotated), 3:64-67 (“The shape of the contacts CC, C3, and C4 is a rectangular shape in FIG. 1, as viewed in the Z-direction. However, the shape of the contacts CC, C3, and C4 is not limited thereto, but may be a substantially circular shape.”).

118. Masamori (Ex. 1020, “Masamori”) likewise discloses through-array contacts (e.g., laterally-insulated conductive via structures (26, 28)) that have a cylindrical shape and extend through the stack:

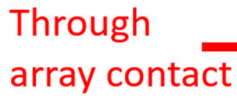
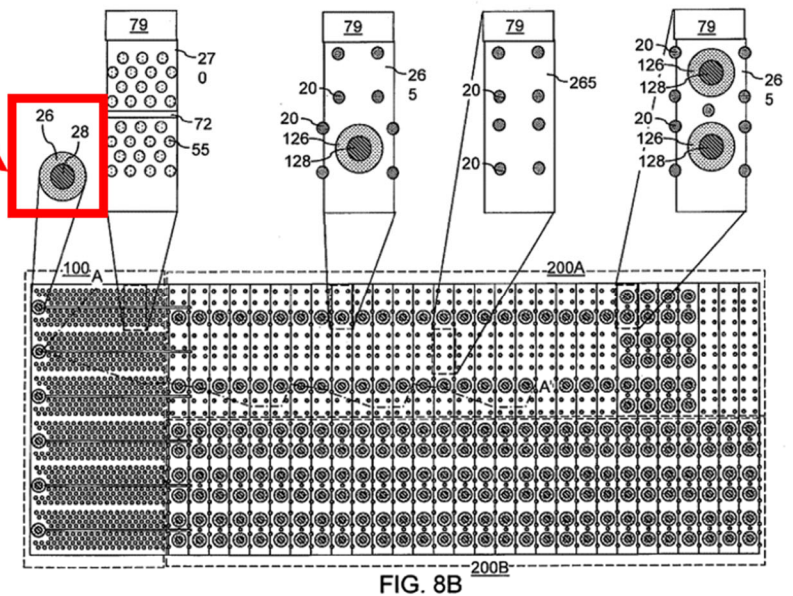


FIG. 8A

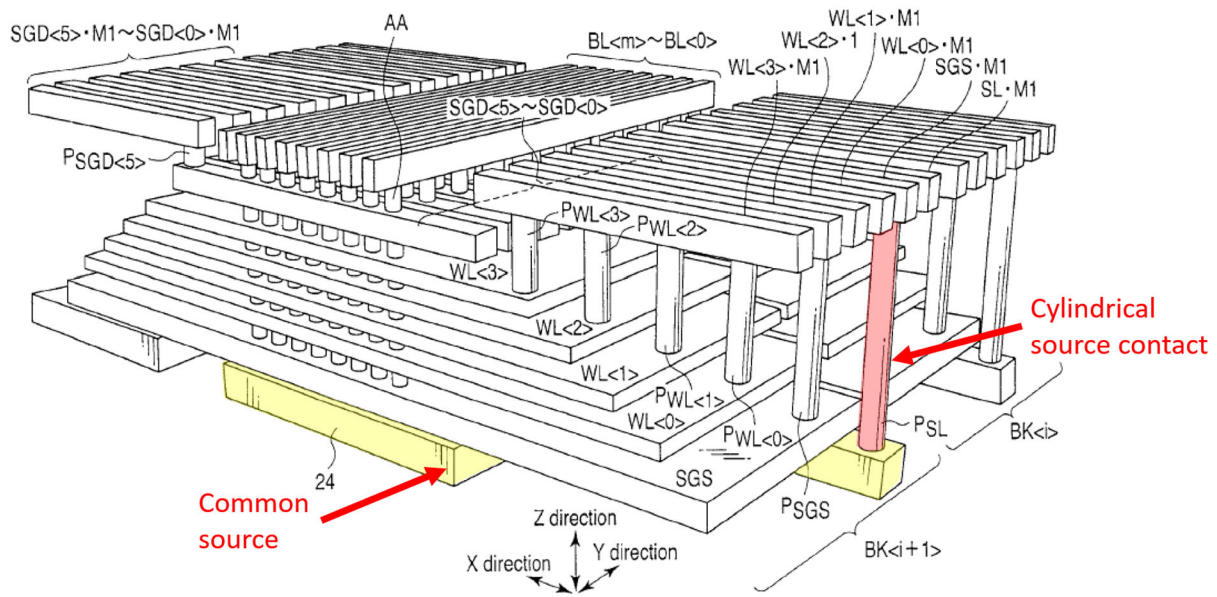
Ex. 1020, Fig. 8A (annotated), [0096] (“Referring to FIGS. 8A and 8B, laterally-insulated conductive via structures (26, 28) and laterally-insulated support structures (126, 128) can be formed through each layer in the alternating stacks $\{(132, 142), (232, 242)\}$ ”).

TAC having substantially
circular section



Ex. 1020, Fig. 8B (annotated). I provide other examples in the technology background section. In short, the techniques for etching through the stack, forming an insulating liner, and filling the remaining void with a conductive core were well known and routine to implement.

119. It is also important to note that employing source line contacts as cylindrical structures was also textbook material. For example, Maejima discloses a cylindrical source contact extending from above a memory stack down to a common source below the memory stack:



Ex. 1021, Fig. 1 (annotated), 4:59-62 (“A source diffusion layer 24 formed in a semiconductor substrate is shared by, for example, all the blocks. The source diffusion layer 24 is connected to a source line $SL \cdot M1$ through a contact plug P_{SL} .”); *see also* §VI (describing source line connections). As the above shows, the source line couples a voltage above the stack to below the substrate, ultimately to the common source region of the substrate to which the channel structures connect.

120. These types of cylindrical source contacts were textbook material:

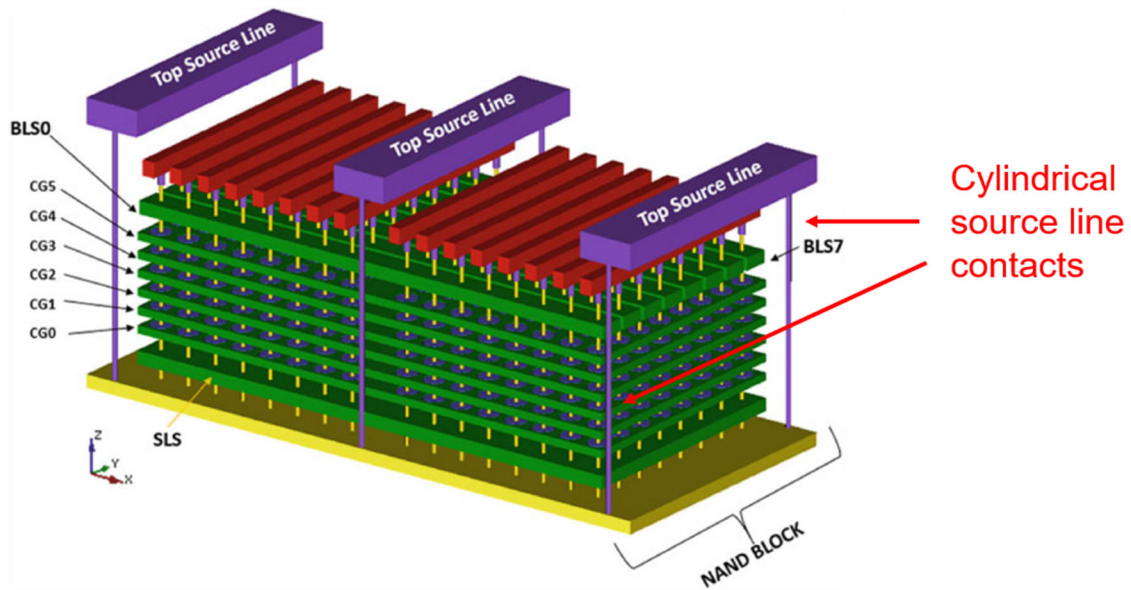


Fig. 5.17 C-FG array with top source line

Ex. 1010, 155.

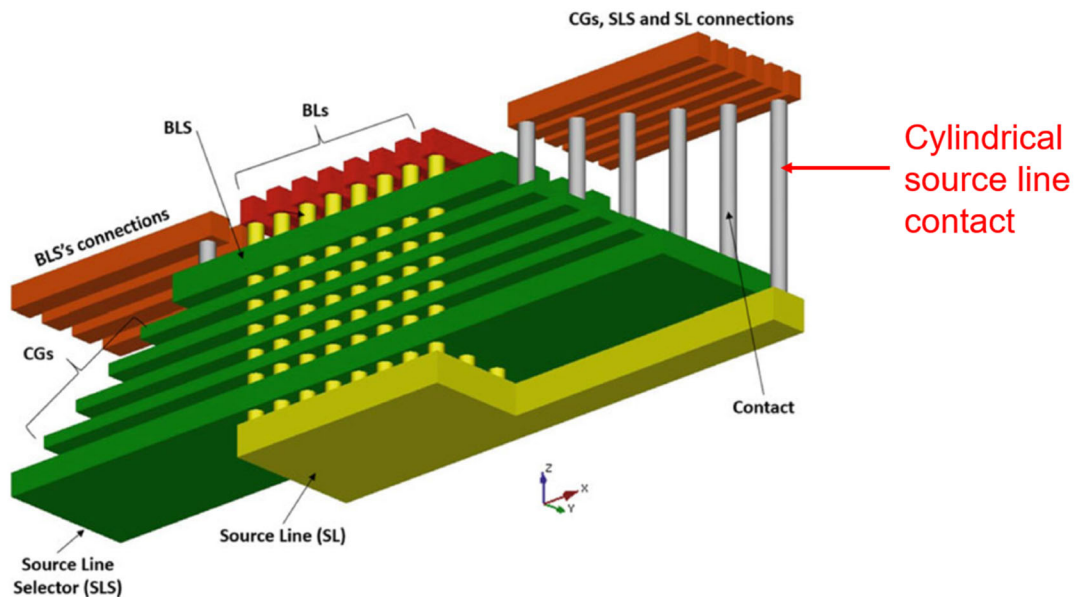
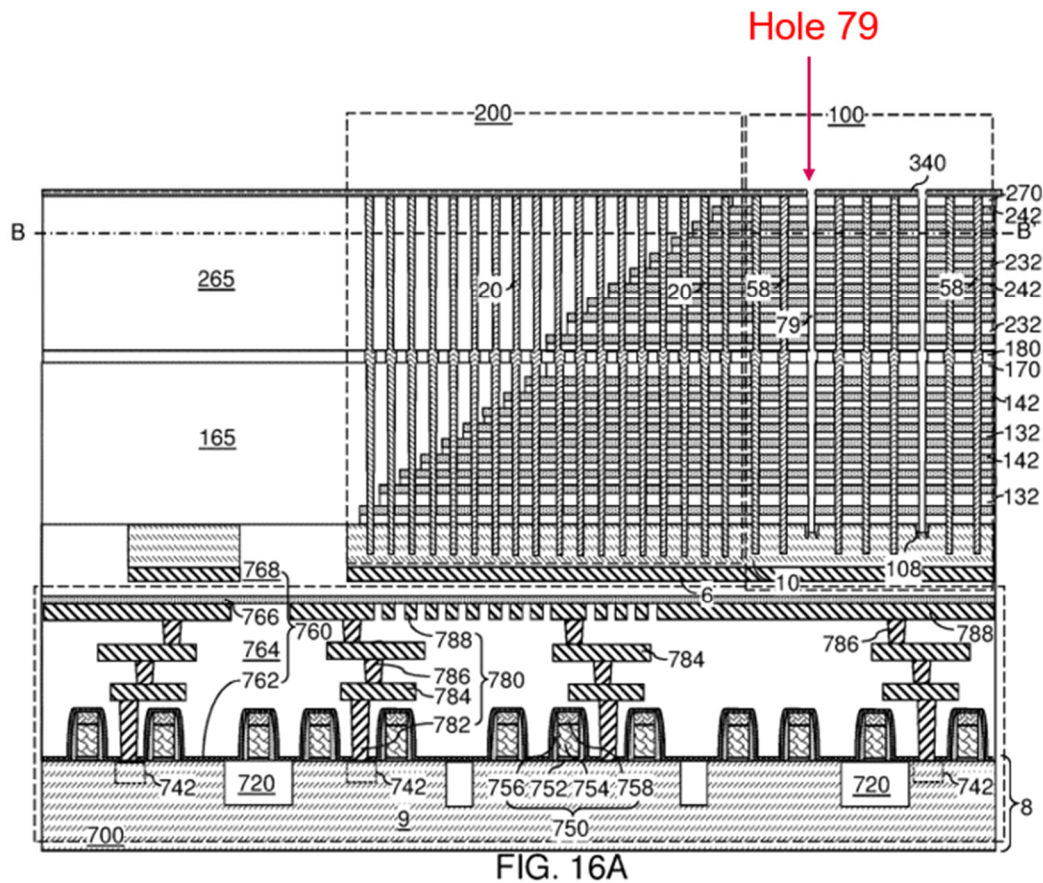
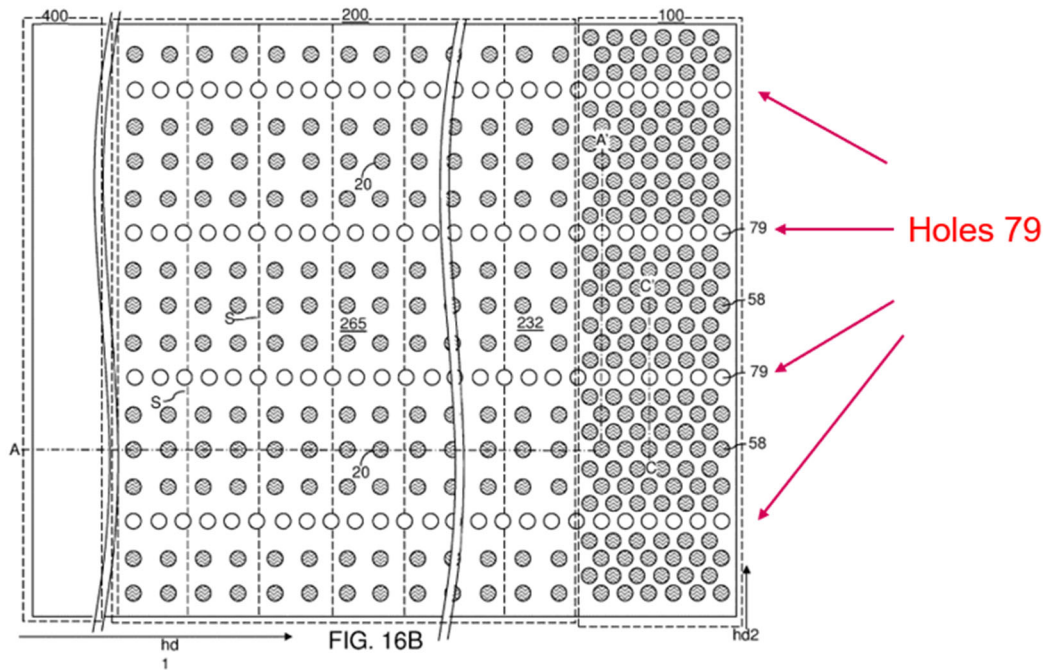


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Id., 110. As can be seen, these cylindrical source lines electrical couple the source voltage to the common source region of a substrate, which again, the bottom portions of the channels connect thereto.

121. It is also important to note that it was known to implement the gate replacement process through circular voids (instead of a trench). Indeed, Nishikawa itself discloses this (through the memory openings). Nishikawa, 9:58-10:7). By way of another example, Iwai teaches using cylindrical voids (79) for the gate replacement process:





Ex. 1022, Figs. 16A, 16B, 28:52-65 (extending through stack), 30:25-58 (using 79 voids for gate replacement process); *see also id.*, Fig. 25B, 33:18-21 (“Thus, each electrically conductive layer (146L, 246L) can be formed as a continuous material layer including multiple rows of holes, which are the multiple rows of backside openings 79.”), 37:47-51 (circular 79 arrangement). I note that Iwai discloses that the voids 79 may be converted to a continuous trench if there is a desire to segment the array. *Id.*, 33:22-49, 34:18-33 (“In contrast, as shown in FIG. 19C, the backside openings 79 are not significantly expanded and are not merged into continuous trenches at the levels of the insulating layers (132, 232).”). But in other embodiments, Iwai does not create these trenches, demonstrating that either type of void shapes was suitable for the gate replacement process.

122. The above demonstrates that implementing Nishikawa's backside contact via as cylindrical TACs was both known and a suitable option. In addition, as I describe below, there were advantages to doing so, and thus a POSITA would have been motivated, with a reasonable expectation of success, to do so.

123. First, the trench has a large footprint, and thus it would increase memory capacity to replace the trench with smaller footprint circular contacts. Nishikawa discloses that the gate replacement process is optional. And source line contacts do not require a trench contact (see above). Thus, replacing the trench with smaller circular contacts recovers footprint for memory cells, increasing memory capacity. Nishikawa2 recognizes this. Nishikawa2, 27:55-28:3 ("If the backside trenches are present, then the size and lateral extent of backside trenches can be reduced to a level sufficient to accommodate only backside contact via structures."). In other words, Nishikawa2 is stating that one could use the memory openings, or other circular openings for the gate line replacement, and thus one could reduce the footprint of the source line contacts to be only for the source line connection function.

124. Similarly, the trench requires etching a significant amount of material (namely, the memory stack) to form the voids. The smaller, circular TACs, however, would require etching a relatively less amount of material. Thus, a POSITA would

have expected to save process time by replacing the large trenches with smaller circular TACs.

125. Second, even if employing the optional gate replacement process, the benefits regarding saving footprint remains true. Recall that Nishikawa provides two options for the gate replacement process: either through the backside trenches or the memory hole openings. Nishikawa, 6:29-44, 9:58-10:8. Thus, using the trench for the gate replacement process is not necessary. And as I describe above, the voids for the circular TACs were suitable for the gate replacement process as well. Ex. 1022, Figs. 16A, 16B, 28:52-65, 30:25-58 (using 79 voids for gate replacement process). Nishikawa2 accomplishes this by spreading the access holes through the array. Nishikawa2, 27:59-63 (“In another embodiment, by distributing the access openings across the entirety of the openings, eliminates the need to employ the optional backside trenches for replacement of the sacrificial material layers.”).

126. In addition, Iwai demonstrates a benefit of using the circular voids for the gate replacement process. As shown above, Iwai spaces the circular voids 79 through the array. In other words, Iwai teaches spreading out the voids for the replacement process. The gate replacement process involves introducing etchants into these voids to first etch the sacrificial gate then depositing the replacement gates. For both of these processes, the materials must flow to first etch out the entire

sacrificial gates and then flow to fully fill the voids. Taking the etching of the sacrificial gates, for example, those etchants must travel through the void and then etch horizontally to entirely etch out the sacrificial gates. The longer the distance that these materials must flow scales the processing time to effectuate the etch (and the same is true with replacing the gates). Thus, spacing these voids throughout the array beneficially shortens the distance that the etchants (and deposition of replacement gate material, e.g., tungsten) must travel.

127. Another benefit of employing circular TACs as common source connections in Nishikawa is the ability to easily spread out the common source connections to the substrate. This enables multiple connections to the substrate to ensure the source voltage properly electrical couples to the common source region. Because of this, it was known to include multiple of these connections in this art. Ex. 1010, 111 (showing 3 source connections), Ex. 1023, 6:8-12, Fig. 11 (showing first and second common source lines spread throughout memory array). All that is necessary is forming multiple of the source connections spread through the array, which as I describe in the technology background, was well known.

128. Finally, a POSITA would have had a reasonable expectation of success in modifying Nishikawa's source contact lines to be cylindrical contacts. First, the processes for forming cylindrical contacts that extend through the array well known. This typically involves an anisotropic (directional) etch. Also, a POSITA would

recognize that implementing TACs with a substantially circular cross-section would improve manufacturing yield by reducing the risk of etch irregularities and enhancing process control during spacer and conductor deposition. Circular geometries are inherently simpler to pattern lithographically and more robust to misalignment compared to trench-shaped contacts. These benefits align with well-documented practices in the semiconductor industry to optimize process reliability and scalability. Second, as I describe above, a POSITA understood that cylindrical contacts were suitable for source connections. Similarly, the circular holes (before forming the insulating liner and conductive core) were suitable for the gate replacement process. I also note that Nishikawa already discloses etching cylindrical holes (see Claim 6 analysis) and forming cylindrical contacts, e.g., the peripheral contacts. Again, the process typically simply involves an anisotropic etch, forming an insulating liner (e.g., by well-known conformal liner deposition), and filling the remaining void with a conductive material, e.g., tungsten.

[1.E] “a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones.”

129. As I describe below, Nishikawa discloses a slit structure (“separator dielectric structure 45”) extending vertically through the conductor (“electrically conductive layers 46”)/dielectric (“insulating layers 32”) layer pairs in the memory stack (alternating stack) and configured to separate the memory stack into a plurality

of memory zones (annotated on the figures below). The slit structures disclosed by Nishikawa serve to segment the memory array into independent zones, preventing electrical interference between adjacent zones and enabling precise control over gate voltages in respective memory blocks. This segmentation improves device reliability and scalability, which are critical considerations for high-density 3D NAND designs. As such, a POSITA would readily recognize that Nishikawa's separator dielectric structures meet the functional requirements of the claimed slit structures.

130. I first note that specification of the '322 Patent does not use the term "memory zones." The specification does describe that "[s]lit structure 132 . . . can separate 3D memory device 100 into multiple memory blocks and/or memory fingers." Ex. 1001, 8:16-18. In other words, the slits separate the memory array into portions by effectively cutting the stack (with voids for the slits) to create separate portions of the stack, i.e., the gate layers are not continuous, but are in segments. Thus, "memory zones" would have been understood to refer to a block or group of memory cells. The block or group of memory cells share common gate layers, and the slits segment the array such that respective blocks or groups of memory cells have common gate layers.

131. The slit structure of Nishikawa is separator dielectric 45. The separator dielectric 45 is formed in a separator trench 47 "through the alternating stack (32, 42) to the top surface of the substrate 8 that is located at the bottom of the alternating

stack (32, 42).” Nishikawa, 8:3-19. Nishikawa explains that the separator trench can be filled with a dielectric insulating material and that “the deposited separator insulating material constitutes separator dielectric structures 45.” *Id.*, 8:20-35. The voids for the separator dielectric 45 segments the array stack into separate portions, and the insulating fill isolates those segments. In short, there are separate areas of the memory stack, such that a gate layer does not extend through the entire memory array (but only its respective memory zone).

132. Nishikawa discloses that a “separator dielectric structure 45 can extend through the alternating stack (32, 42), i.e., from the top surface of the substrate 8 to the top surface of the alternating stack (32, 42).” Nishikawa, 8:36-43. This is because it segments the memory stack. This is shown below:

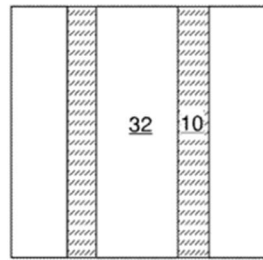


FIG. 3A

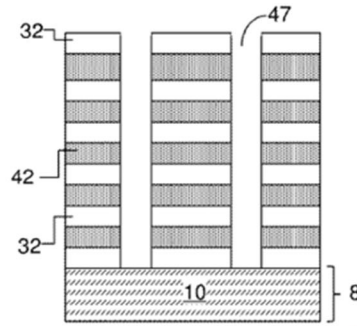


FIG. 3B

Slit structures

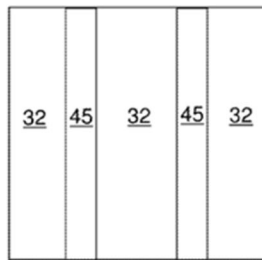


FIG. 4A

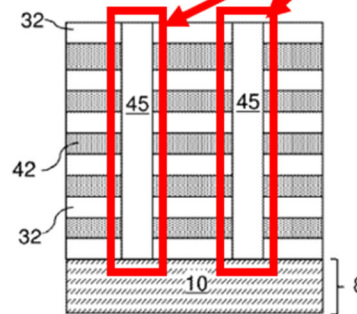


FIG. 4B

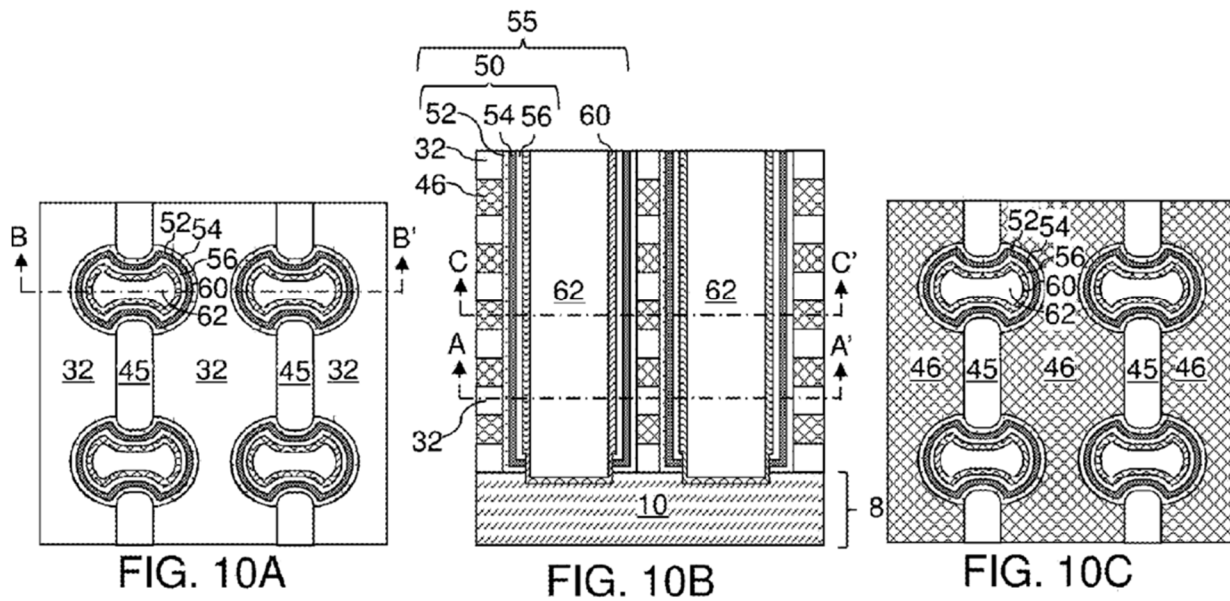
Id., Figs. 3A-B, 4A-B (annotated).

133. Nishikawa also discloses that “the alternating stack (32, 42) as formed at the processing steps of FIGS. 2A and 2B is divided into multiple laterally disjointed portions by the separator dielectric structures 45, each of which comprises discrete portions of the alternating stack (32, 42).” Nishikawa, 8:36-43. These laterally disjointed portions are memory zones of memory cells that are formed within each region. Again, these slits segment the memory stack (and importantly, the gate layers) into respective portions.

134. Nishikawa discloses two types of slits. First, Nishikawa discloses that “[e]ach memory opening 49 can be located between a pair of separator dielectric

structures 45.” Nishikawa, 8:57-59. In other words, the separator dielectric structures, by themselves, divide the array into groups of memory cells. This was the conventional type of slit (as I discuss in the background technology section).

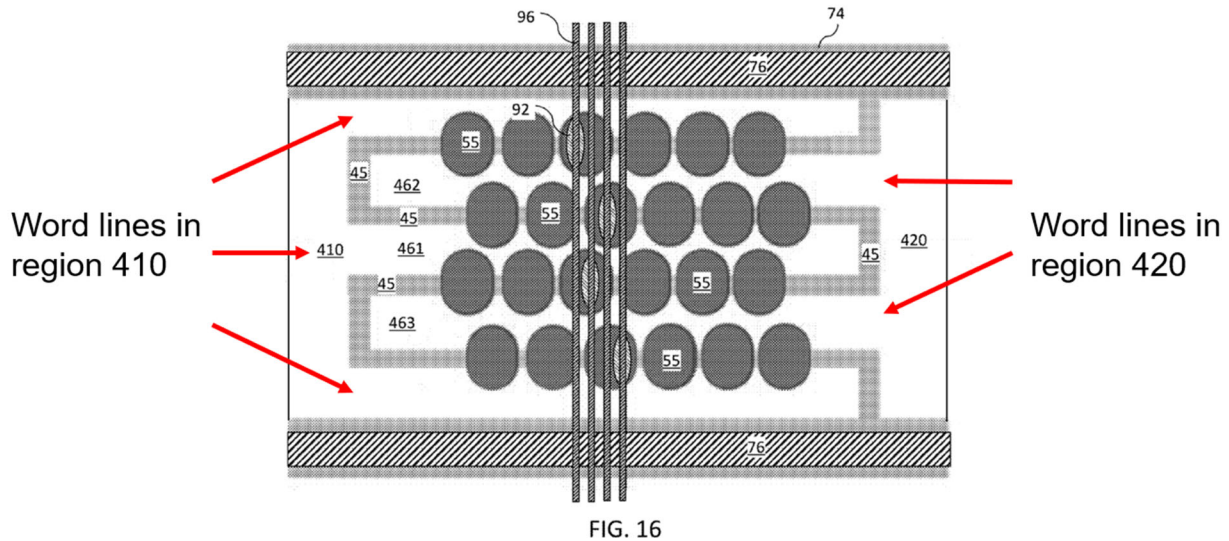
135. Second, Nishikawa discloses that “[i]n one embodiment, each memory opening 49 can divide a separator dielectric structure 45 into two physically disjointed portions. In this case, each memory opening 49 in the alternating stack (32, 42) can extend through the separator insulating material located in a respective separator dielectric structures 45, and can divide the separator dielectric structure 45 into two laterally disjointed portions.” Nishikawa, 8:59-67. As shown below, while the memory channel structures are physically between portions of the slit structure, the slit still divides the array, because without it, there would be no separation. In other words, if there were not the slits, there would not be portions of the gate layers and memory zones. Applying a voltage to any portion of a gate layer would result in that voltage developing on the entire gate layer, rather to a respective portion of the gate layer corresponding a subset of the memory strings.



Id., Figs. 10A-C.

136. In this second form of slits, Nishikawa discloses “[e]ach memory cell in the NAND string comprises a portion of a first control gate electrode 461 (which is a first portion of an electrically conductive layer 46) located adjacent to a first portion 50A (*which is located on one side of a respective pair of separator dielectric structures 45*) of a memory film (52, 54, 56) and a portion of a second control gate electrode 462 which is located adjacent to a second portion 50B (*which is located on the other side of the respective pair of separator dielectric structures 45*) of the memory film (52, 54, 56).” *Id.*, 14:60-15:2. Nishikawa further explains that “[t]he second control gate electrode 462 is electrically insulated from the first control gate electrode 461.” *Id.*, 15:2-3. In other words, independent memory cells are formed

on both sides of the separator dielectrics 45. Thus, these independent memory cells are in respective memory zones. This is shown below:



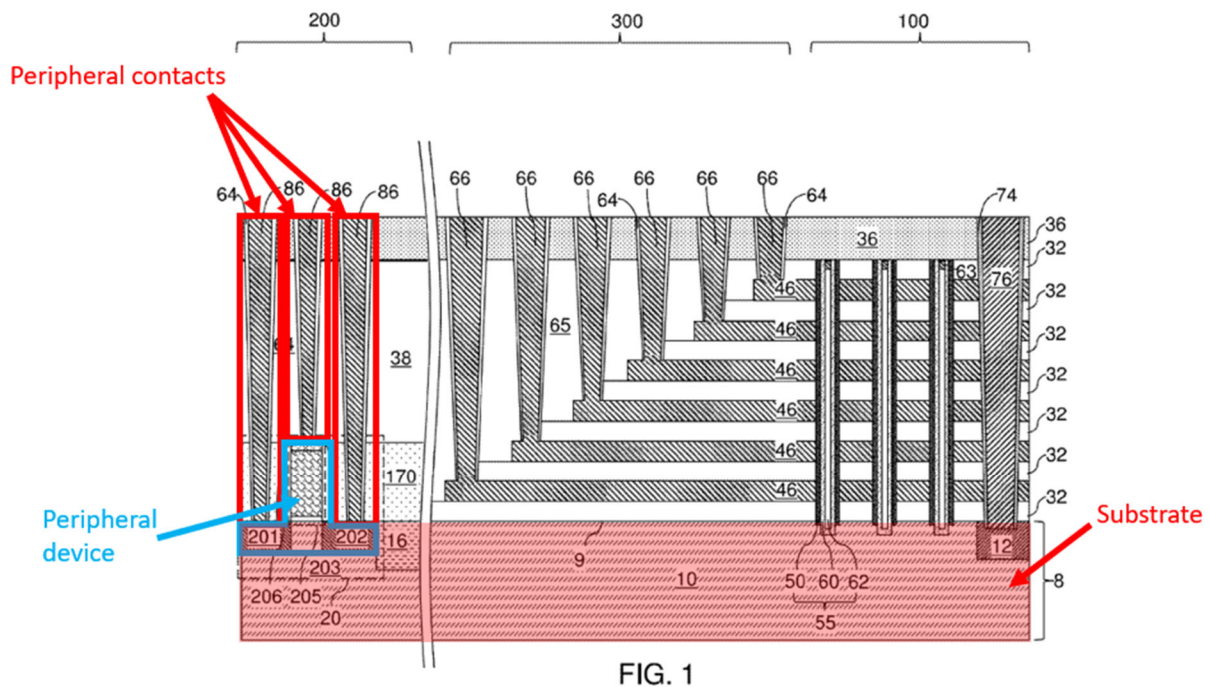
Id., 15:31-42 (“Each level of control gate electrodes can include a first word line and a second word line. The first word line can comprise a comb shaped word line WLL/410 . . . The second word line can comprise a comb shaped word line WLR/420”).

2. Claim 2:

[2] “The 3D memory device of claim 1, further comprising: a peripheral device on the substrate, a peripheral contact being arranged outside of the memory stack and in contact with the peripheral device.”

137. As I describe below, Nishikawa discloses a peripheral device (“peripheral device 20”) on the substrate (“substrate 8”), a peripheral contact (“peripheral contact via structures 86”) being arranged outside of the memory stack (in “peripheral device region 200”) and in contact with the peripheral device.

138. The peripheral device 20 is arranged outside the memory stack in the peripheral device region 200, i.e., it does not extend through the memory stack (alternating stack of dielectric and oxide layers) and is in contact with the peripheral contact via structures 86. Nishikawa, 4:36-39 (“an array of memory devices can be formed in a device region 100, and at least one peripheral device 20 can be formed in a peripheral device region 200.”), 5:30-45 (describing types of peripheral devices), 6:52-54 (describing formation of peripheral contact structure 86). The peripheral device shown below is exemplary. That is, while it depicts a transistor (with its gate, drain, and source), this obviously exemplary as Nishikawa more generally describes circuitry such as driver circuits. *Id.*, 6:3-28.



Nishikawa, Fig. 1 (annotated).

3. Claim 3:

[3.PRE] “The 3D memory device of claim 2, further comprising:”

139. Nishikawa discloses or at least renders obvious the 3D memory device of Claim 2. *See* §§IX.B.1-2, above.

[3.A] “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,”

140. As discussed in §IX.B.1[1.C], Nishikawa discloses channel structures, i.e. memory stack structures 55. Nishikawa, 11:33-39. The channels include dielectric layers, e.g., blocking and tunneling layers. *See* §IX.B.1[1.C]. A POSITA would have been motivated, with a reasonable expectation of success, to include dummy channels (of either the same materials or with a solid dielectric fill) in Nishikawa’s memory stack for several reasons. Recall that Nishikawa discloses an optional gate replacement process. *See* §IX.B.1[1.D]. I address the motivations under both scenarios.

141. Whether using a gate replacement process or not, it has been well known for decades to include dummy structures for two well-known process reasons. First, it has been known that elements, such as channel structures, at the end of an array are subject to process variations. Ex. 1024 (U.S. Pat. 5,945,717 - Chevallier), 8:47-53 (“In a typical flash cell array, cells located at the edge of the array are much more subject to processing variations than the cells not located at the edge. Because of this, it is common to refrain from using the cells at the array edge.

Such cells, which extend around the perimeter of the array, are sometimes referred to as dummy cells.”). For modern processes, this has become even a greater issue. Ex. 1025 (U.S. Pat. 10,347,487 - Lee), 2:20-43 (“Edge of array issues may typically occur at the boundary between a chop mask and pitch double patterning. An abnormality at the edge of an array pattern can cause blowout or shorting issues, depending on the integration process. Conventionally, an abnormal edge pattern at the edge of array may be controlled by adding a dummy pattern region, which is later sacrificed in processing.”). Thus, one normally employs dummy channel structures at the edge of the array. Otherwise, these channel structures may be defective, and not properly store data.

142. Second, adding dummy channels such that the overall pattern is more consistent was well known for decades, too. Ex. 1026 (Ronse), 11 (“As a result, this technique is particularly useful in regular patterns like memories, and much less in random logic designs where features can be completely irregular.”) Semiconductor fabrication involves patterning, and patterning periodic structures is much more difficult than a consistent pattern due to, for example, pattern distortion. Thus, again, the use of dummy structures was the norm to reduce fabrication issues.

143. If using the gate replacement process with Nishikawa, additional motivations exist. Dummy channels provide structure support, which is important during the gate line replacement process. The gate replacement process etches out

the sacrificial gates and leaves voids where those sacrificial gates were in the stack. As a result, “support pillars” are necessary to support the stack during this process. Ex. 1030 (U.S. Pat. 8,945,996 - Tang), 5:64-6:2, 7:19-23. Nishikawa2 recognizes this known need. Nishikawa2, 9:63-67. While Nishikawa2 does not expressly say these would be dummy channels, a POSITA would recognize that as consistent with Nishikawa2’s “dielectric pillar structure” statement. *Id.* A common support structure was a dummy channel. Ex. 1031 (U.S. Pat. 10,115,632), 30:14-27; *see also id.*, 15:3-22 (structures 20 are dummy channel structures). I note that it was well known to include dummy support members that extend through the entire stack or partially through the stack. Ex. 1027 (Kai), Fig. 6A (support members 20), 16:28-38. For example, the dummy channels may be on the edge of the array or in the staircase region.

144. Prior art references such as Kai (Ex. 2017) confirm that adding active and dummy channels for structural support was a recognized technique, as dummy channels provide reinforcement without requiring upper-level connections, a key feature for achieving structural integrity in high-aspect-ratio stacks. Ex. 1027 (Kai), 10:20-27. A POSITA would apply this approach as a routine measure to bolster stack stability, particularly during gate replacement processes. This predictable implementation leverages standard support techniques recognized as necessary for maintaining high-aspect-ratio structures. *E.g., id.*, 9:23-26 (defining “support

opening” as “a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed”), 9:45-48 (“support openings 19” extend through stack), 10:20-27 (forming channels in support openings).

145. By way of example, Kai refers to the dummy channels as “support pillar structure 20” and active channels as “memory stack structures.” Ex. 1027 (Kai), 16:28-38; Fig. 15A, 25:58-63 (dummy support channels (20) have no connection to the upper level, whereas the active channel structures (55) include contacts (88)). By way of another example, Park discloses forming active and dummy, supporting channels. Ex. 1028 (Park), 6:19-26, 7:45-51. Kim (Ex. 1029, ’599 Patent) provides another similar example of forming active and dummy, supporting channels. Note that dummy channel structures can be made at the same time as active channels, and if the dummy channels have all the same materials as the active channels, this saves processing time. Ex. 1029 (U.S. Pat. Pub. 2018/0308559) [0047] (“The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region CTR,” “DS may physically support,” and listing same materials as channels), [0071] (“The channel holes CH and the dummy holes DH may be formed at the same time.”), [0072] (same time), Fig. 13 (DH through stack on edge).

146. Masamori details forming the dummy and active channels at the same time, noting that as three-dimensional devices scale to smaller sizes, additional

structural support is desired during the sacrificial gate replacement process. *See* Ex. 1020, [0003]. Masamori discloses a dummy channel structures (“semiconductor-containing support structure 20”) that extend vertically through the conductor/dielectric layer pairs, as shown below. The layers of the semiconductor-containing support structure 20 are described in the context of the memory opening fill structures 55, and Masamori discloses that “[t]he memory opening fill structures 55 and the semiconductor-containing support structures 20 can be formed simultaneously employing a same set of processing steps.” *Id.*, [0085]. Thus, the semiconductor-containing support structures 20 have the same layers as memory opening fill structures 55:

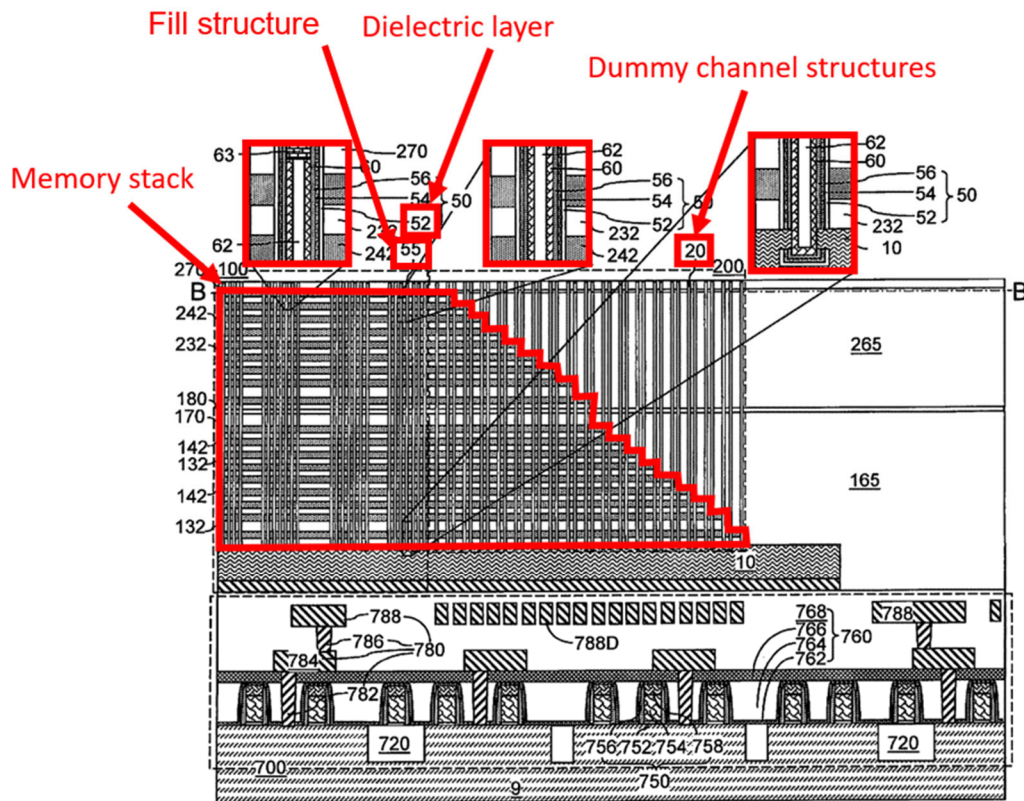


FIG. 7A

Ex. 1020, Fig. 7A (annotated). “The blocking dielectric layer 52 includes a blocking dielectric layer material such as silicon oxide, a dielectric metal oxide (such as aluminum oxide), or a combination thereof.” Ex. 1020, [0086]. Silicon oxide layers are dielectric layers. The tunneling layer is typically silicon oxide as well.

147. And dummy channels can be made by the same process and at the same time as the active channels. Ex. 1027 (Kai), 10:20-27. The dummy channels, however, typically will not include interconnects to upper-level elements, because the structures do not store data. Thus, dummy channels do not consume space above

the structures, but still function as support members (and have the processing benefits that I describe above).

148. Finally, employing dummy structures would have been routine and a POSITA would have had a high expectation of success in doing so. First, Nishikawa already discloses forming channel structures. Simply not connecting a channel structure to upper-level interconnects, such that it is an active channel, forms a dummy channel. The materials in the active and the dummy channels can be exactly the same. Also, I describe above that the addition of dummy channel structures actually reduces processing issues, such as defective bits and simplifies patterning. And again, these were commonplace and textbook material for decades.

149. A POSITA would not understand this limitation to require that the claimed dummy channel structures must be fully filled with a dielectric material. The '322 Patent discloses that “[d]ummy channel structure 146 can extend vertically through memory stack 104 and have a vertical opening filled with the same materials as those in channel structure 108.” Ex. 1001, 9:29-31. The '322 Patent further discloses that “[i]n some embodiments, dummy channel structure 146 is **fully filled** with dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.” *Id.*, 9:35-39. Thus, a POSITA would have understood that “filled” does not require “fully filled,” as those terms are used differently in the context of the '322 Patent. In other words, if Applicant

had intended the language “a dummy channel structure filled with a dielectric layer” to mean fully filled with a dielectric material, a POSITA would have expected the claim to expressly recite “fully filled.” This is consistent with Claim 10 of related U.S. Patent No. 10,879,254, where Applicant claimed “depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure.” Ex. 1032 (Guo).

150. Even if this claim did require “fully filled,” that would have been obvious, because as I describe above, one known beneficial use of dummy structures was as a support pillar. A common support pillar was a solid dielectric, e.g., silicon oxide, pillar. Ex. 1033 (Sharangpani), 15:21-39 (“dielectric support pillar 7P”). Here, the support pillar is one solid, dielectric fill, which can provide more relative support than various layers of a semiconductor memory string (particularly if voids are left in the memory string core).

[3.B] “wherein each of the dielectric layer in the dummy channel structure, a spacer in the TAC, and a spacer in the peripheral contact comprises silicon oxide.”

151. As I describe below, Nishikawa discloses, or in view of the knowledge of a POSITA renders obvious, this limitation. As discussed in detail below, silicon oxide was a preferred material for spacers in 3D NAND devices due to its high thermal stability, excellent insulating properties, and compatibility with common deposition techniques such as low-pressure chemical vapor deposition (LPCVD) or

atomic layer deposition (ALD). These properties made it an industry-standard choice for forming spacers that effectively isolate conductive structures while maintaining structural integrity during high-temperature annealing steps. A POSITA would therefore have readily understood Nishikawa's dielectric spacers to include silicon oxide as the material of choice.

152. With respect to the dummy channels, my analysis under claim [3.A] and [1.C] demonstrates that it would have been obvious to include dummy channels in Nishikawa's memory, which include silicon oxide layers, e.g., blocking and tunneling layers. Further, it would have been obvious to completely fill the dummy holes with silicon oxide, thereby forming a dielectric support pillar. A common support pillar was a solid dielectric, e.g., silicon oxide, pillar. Ex. 1033 (Sharangpani), 15:21-39 ("dielectric support pillar 7P"). Here, the support pillar is one solid, dielectric fill, which can provide more relative support than various layers of a semiconductor memory string (particularly if voids are left in the memory string core).

153. With respect to the TAC spacer, Nishikawa discloses a "dielectric spacer 74." Nishikawa, 6:57-59. With respect to the peripheral contact spacer, Nishikawa discloses a "dielectric liner 64." *Id.*, 6:49-50, Fig. 1. It would have been understood, or at least obvious, that these spacers would be silicon oxide. Nishikawa describes dielectric elements as silicon oxide. For example, Nishikawa describes

“dielectric material of insulating layers 32” as being “silicon oxide.” *Id.*,7:17-33; *see also id.*, 11:52-57 (similar). Importantly, dielectric spacers for contacts were typically silicon oxide, because of the advantages that I describe below. As an example, Masamori discloses that the spacer of the laterally-insulated conductive via structure (26, 28), i.e. a TAC, can be silicon oxide. Ex. 1020 (Masamori), [0099]; *see also* Ex. 1012 (Mushiga), 10:31-57 (disclosing a tubular spacer material 586 surrounding a through-memory-level-via structure 588). Thus, a POSITA would have understood Nishikawa to disclose the TAC and peripheral contacts to include silicon dioxide spacers, because a POSITA would have at once thought of silicon dioxide spacers in view of Nishikawa above disclosures.

154. In addition, a POSITA would have been motivated with a reasonable expectation of success to employ silicon oxide as the dielectric material to fill the dummy holes and to form the spacers. First, as I describe above, Nishikawa already discloses using silicon oxide as a dielectric material to form similar structures. Nishikawa,7:17-33, 11:52-57. Thus, a POSITA would have understood that Nishikawa is employing a typical dielectric material for structures and would consistently use that same material for similar structures. Second, again, silicon oxide was the typical dielectric material for spacers and channel structures. For these structures, the spacer and channel layers (blocking and tunneling layers) requires a conformal deposition. Processes using silicon oxide to implement these layers were

well understood and, in fact, textbook material. Ex. 1034 (Wolf Vol. 1), 48-49.

Third, silicon oxide is an ideal insulator in the semiconductor context. To begin, from a material perspective, it properly isolates metal structures, thereby preventing inadvertent electrical coupling. From a deposition perspective, because of being able to conformally deposit silicon oxide, it is very conducive to forming spacers that properly encase structures, thereby fully insulating the element. Finally, a POSITA would have had a reasonable expectation of success. Not surprisingly, Nishikawa already employs silicon oxide in its process, because again, processes for depositing and forming silicon oxide elements such as spacers were well known. These processes were textbook material for many decades before the filing of the '322 Patent. Ex. 1034, 48-49; Ex. 1009, 7:44-49.

4. Claim 6:

[6.PRE] “The 3D memory device of claim 1, further comprising:”

155. Nishikawa discloses or at least renders obvious the 3D memory device of Claim 1.

[6.A] “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack; and”

156. This limitation is identical to Claim [3.A] and met for the same reasons.

[6.B] “a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate,”

157. This limitation is substantively the same as Claim [2] and met for the same reasons.

[6.C] “wherein: a diameter of the TAC is at least equal to a diameter of the peripheral contact; and”

158. As I describe below, Nishikawa in view the knowledge of a POSITA renders this limitation obvious.

159. As an initial matter, my analysis under Claim [1.D] demonstrates that it would have been obvious to implement Nishikawa’s TAC as a cylindrical contact with a diameter. Nishikawa’s TACs and peripheral contacts (again, the ’322 Patent uses “peripheral” to refer to outside of the array, which is common usage in the memory context) are shown below:

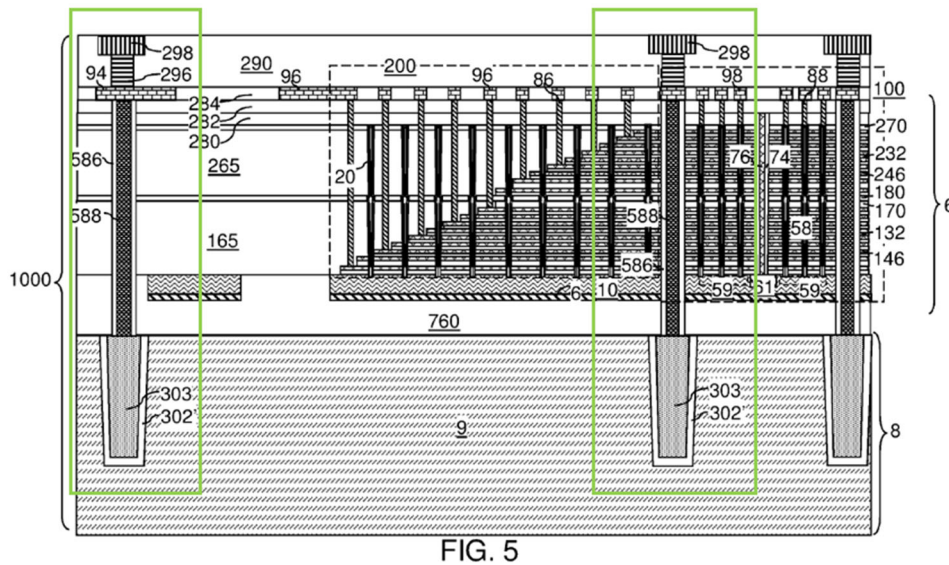


FIG. 1

Nishikawa, Fig. 1 (annotated). It would have been understood that Nishikawa's peripheral contacts 86 are cylindrical with a diameter because these contacts extend through the array and connect to devices. For example, as shown above, the three contacts connect to a drain, source, and gate of a transistor. These elements of a transistor are not in a trench shape, but would require a cylindrical contact to contact to the respective elements. As I explain in my analysis under Claim [1.D], these cylindrical contacts were very well known.

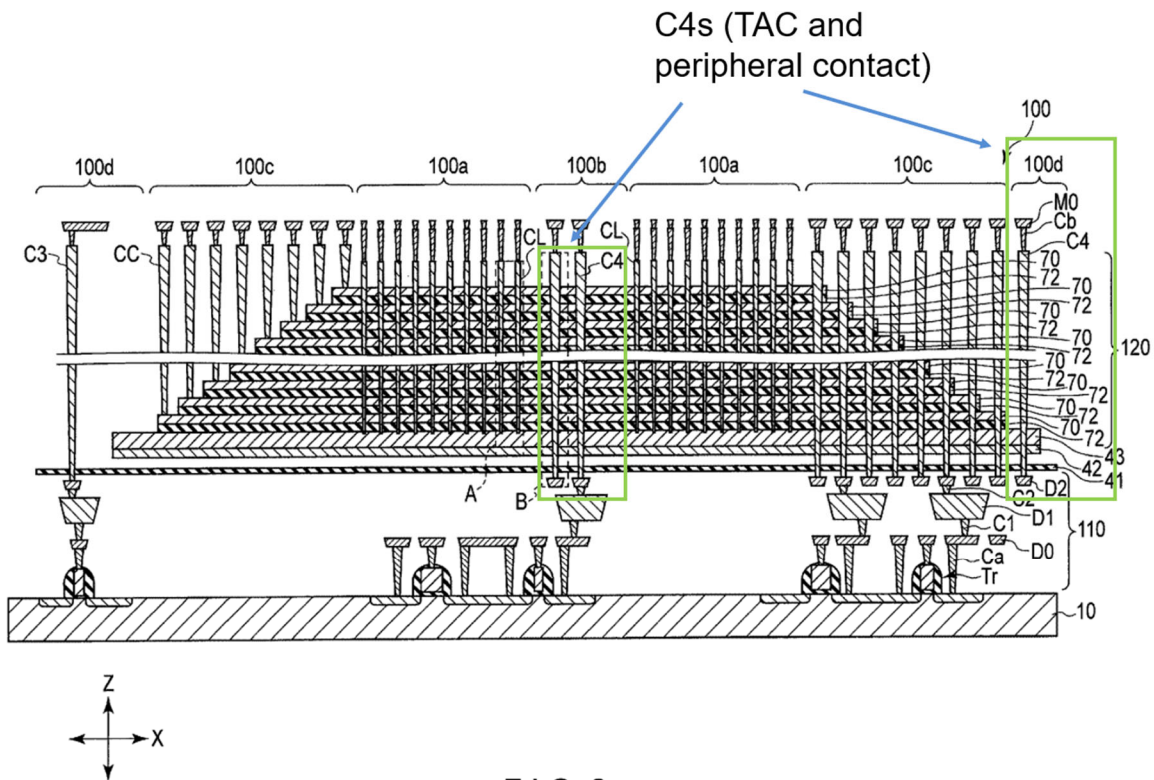
160. One common that dates back many decades is to form all contacts the same size. This was a standard, textbook approach. *E.g.*, Ex. 1035 (Wolf Vol. 2), 33. There are various advantages to this approach, including using the same pattern on masking layers to form the contact holes and simpler etching chemistries (which

I discuss more below). This conventional approach was known in the specific 3D NAND context as well. For example, Mushiga discloses forming, at the same time, through-array contacts (588), having the same size and using the same processing steps:



Ex. 1012, Fig. 5 (annotated), 10:31-58.

161. While the above figure is not drawn to scale, a POSITA would have understood the same relative sizes of these contacts to represent that the contacts are made with the same process and made to be the same size. This can be seen with respect to Nakajima as well. Nakajima discloses forming holes H1 through the stack for its TACs (C4). One C4 structure is outside of the stack (on the right below) and others are through the array:



Ex. 1009, Fig. 2 (annotated). Nakajima only discloses one step for creating the H1 holes and C4 contacts. *Id.*, 7:37-8:11. Accordingly, Nakajima depicts these contacts being the same size.

162. A POSITA would have been motivated to make the TAC and peripheral contacts the same size to employ a common process (including the hole size in masking steps) when forming the contacts, e.g., as Mushiga and Nakajima (*see* above) teach. This can save considerable process time because it involves simply employ a common size for the holes in a pattern, e.g., in forming the masks for an anisotropic etch. Using this technique, even if the holes were for different structures,

e.g., dummy and active vias, was well known. *E.g.*, Ex. 1036 (Tessariol), [0037] (“dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)”), Fig. 9. Implementing different hole sizes requires using specific etch chemistries to account for the different sizes. *E.g.*, Ex. 1035 (Wolf Vol. 2), 33. In short, creating the contacts of the same size, using the same process steps, simplifies the process and shortens fabrication time.

[6.D] “a diameter of the dummy channel structure is smaller than each of a diameter of the TAC and a diameter of the peripheral contact.”

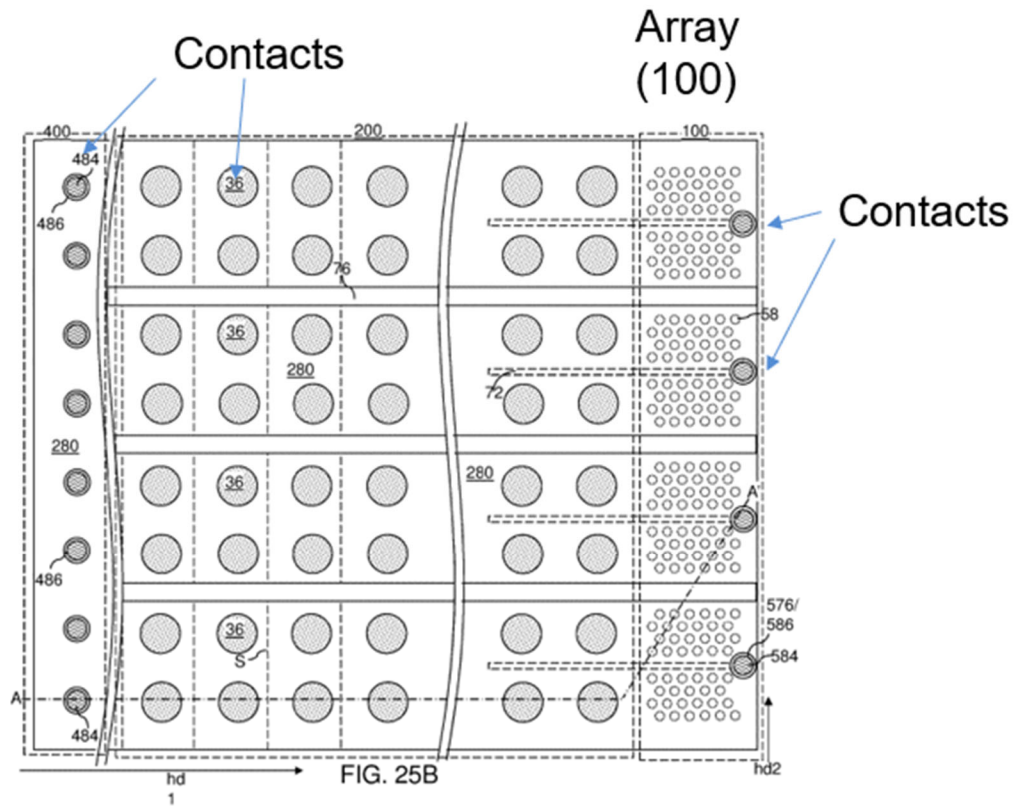
163. As I describe below, Nishikawa in view of the knowledge of a POSITA renders this limitation obvious.

164. My analysis under Claim [3.A] demonstrates that it would have been obvious to form dummy channel structures using the same process to form active channels. As the below explains, the dummy channels have a much smaller diameter than the TACs and peripheral contacts.

165. The array contains millions or billions of channel structures and is the densest area. The driving force in manufacturing memory is to create as dense as an array as possible for two reasons. First, memory capacity is obviously a key element of a memory. Second, the denser the array, the less silicon is necessary to create a given memory size. As density increases, the memory design becomes more cost effective. Thus, a large focus of design efforts for memory revolves around

fabricating a dense array. As Ground 2 demonstrates, for example, the desire for a dense array with high-aspect ratio memory holes led to the multi-deck design. This desire for a dense array was textbook material well before the filing of the '322 Patent. *E.g.*, Ex. 1010 (Micheloni), 211-215. The dummy channel holes will generally have the same size as active channel holes to maintain a uniform pattern and reduce the edge effect issues. I discuss this in greater detail in my analysis under Claim 3. One point of employing dummy channels is to produce a repeating, uniform pattern, where the array edges include the dummy channels. The premise of these benefits is using the same size of dummy and active channels. Further, as I describe under Claim 3, the dummy and active memory holes are made using the same process. Thus, a single process makes a uniform, repeating pattern of these dummy and active holes, all of which will be the same size.

166. The below figure illustrates a top-down view representing contacts and channels:



Ex. 1037 (Cui), Fig. 25B (annotated). A POSITA would have understood from this figure that the intent is to show a relative size difference between the contacts and denser array with smaller channel structures (in array portion 100). In short, it would have been understood, or at least obvious, that the dummy channels have a diameter that is smaller than the diameters of the TACs and peripheral contacts.

167. I also note that while the channel structures of Nishikawa are semi-circular, in my opinion, these structures would have been understood to include a diameter. Below, I annotate a diameter:

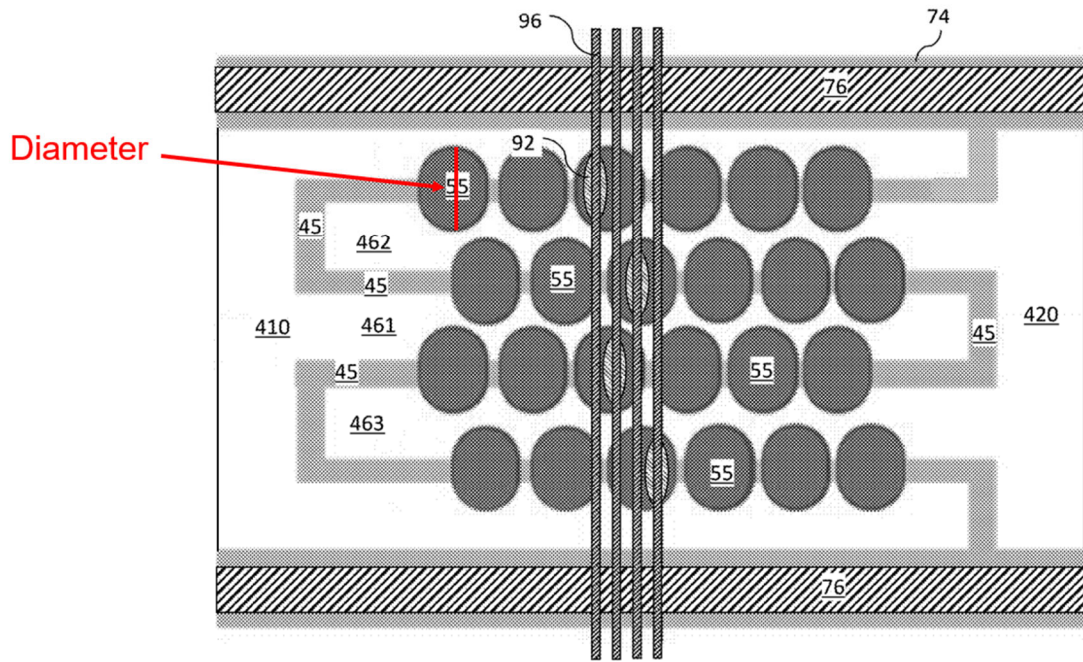


FIG. 16

Nishikawa, Fig. 16 (annotated). Specifically, ellipses have two diameters, a major and minor axis. The longer diameter is the major axis. I do not observe any definitional language in the '322 specification that runs counter to this plain and ordinary understanding of “diameter.” Mathematical descriptions of an ellipse are consistent with this understanding of ellipses having diameters. *E.g.*, Ex. 1047.

168. I also note that Nishikawa discloses that the memory cells may be between separators 45. *See* §IX.B.1[1.E]. In the above figure, however, Nishikawa employs a semi-circular channel structure where the channel structures extend in part through the separator. But in the embodiment in which the channel structures are not partly within the separators 45, it would have been obvious to form the channel structures purely circular (that is, cylindrical structures), because this was

the conventional approach. *E.g.*, Ex. 1037 (Cui), Fig. 25B (illustrate circular “memory opening fill structure 58”); Ex. 1020 (Masamori), Fig. 8B (illustrating circular “memory stack structures 55”). In other words, the most conventional and obvious approach in view of Nishikawa’s embodiment wherein the channel structures do not partially reside in separator 45 elements, is to employ conventional cylindrical channel structures.

5. Claim 7:

[7] “The 3D memory device of claim 1, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.”

169. As I describe below, Nakajima renders this limitation obvious under PO’s incorrect interpretation and under the correct interpretation. I address this limitation under what appears to be PO’s incorrect interpretation of the limitation and the correct interpretation.

170. The ’322 Patent discloses an etch that intentionally forms recesses in the sacrificial layers. Ex. 1001, 13:52-65, Fig. 3D. It appears in alleging infringement in the district court case, however, PO interprets this claim to include largely undetectable and unintentional alleged recesses. Ex. 1038 (Ex. B-1, YMTC’s Contentions), 11, 28. In typical etches through a stack with silicon oxide and silicon nitride layers (usually the composition of the sacrificial gates), the result will be recesses in either the silicon oxide or silicon nitride layers due to what is

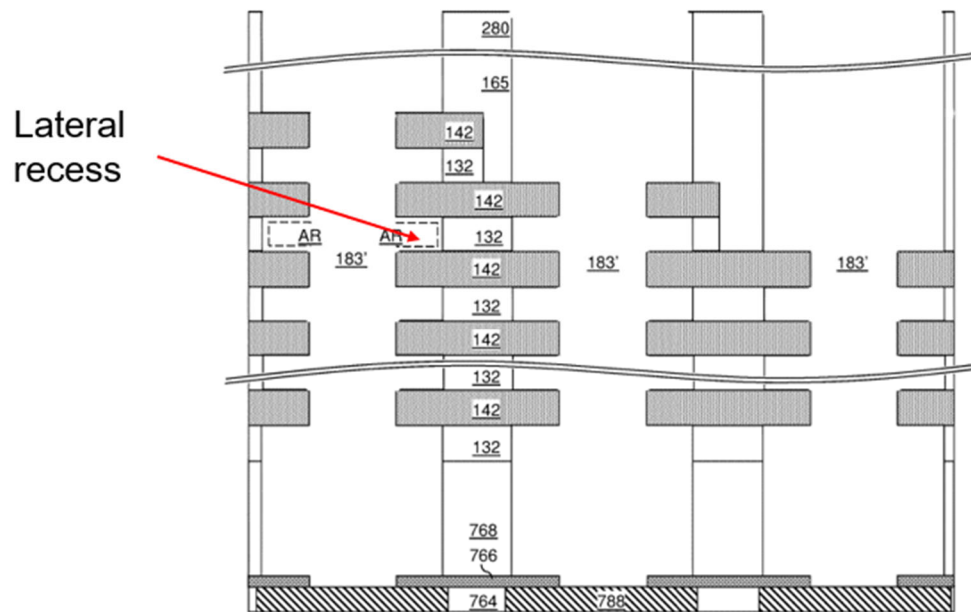
known as etch selectivity. In simple terms, an etch involves using a chemical, which may in a wet or dry form, to remove material. That chemical, however, can favor a particular type of material, and more aggressively remove that material. For a stack of silicon oxide and silicon nitride layers, prior art etches would typically favor one of these material types. Ex. 1039 (U.S. Pat. 11,075,084), 2:59-67 (In “3D NAND memory, it is important to have an etching gas which can etch both SiO₂ and SiN layers (or both SiO₂ and p-Si layers) without selectivity. In another words, it is a challenge to find an etch gas that has similar high etch rates of SiO₂ and SiN in terms of getting a smooth sidewall of high aspect ratio holes in 3D NAND memory.”). Thus, prior art etches would naturally create very small lateral recesses, which may be in the silicon nitride sacrificial layers depending on the etch type. *Id.*, 2:59-67.

PO’s Incorrect Claim Interpretation

171. Nishikawa discloses the typical alternating stack of silicon oxide dielectric layers and silicon nitride sacrificial gate layers. Nishikawa, 7:3-11. And recall that typical prior art etches that effectively create a hole through that stack result in very small lateral recesses in either the dielectric spacers or sacrificial layers. Ex. 1039 (U.S. Pat. 11,075,084), 2:59-67. Thus, it would have been obvious that small unintentional recesses would naturally result, because this was known as a natural result of these prior art etches.

The Correct Claim Interpretation

172. Creating intentional lateral recesses in a hole for a contact, however, was also known. For example, Cui (U.S. Pat. 10,304,852) discloses contacts 183 that travel through the staircase and through the entire array. Ex. 1037 (Cui), Fig. 14A, 25:51-53 (e.g., 183 contact on right of region 200); see also Ex. 1027 (Kai), 11:9-34 (“laterally recessed”). Cui discloses two types of these holes. First, Cui depicts an embodiment in which the sidewalls of this contact are straight (“cylindrical via cavity”). Ex. 1037 (Cui), Fig. 15A, 25:63-26:22. Second, Cui depicts an alternative embodiment with large recesses in the conductor layers or sacrificial gates (“ribbed via cavity”). *Id.*, Fig. 16A, 26:23-32, Fig. 41A, 44:65-45:25. In other words, both alternative options were known.



Id., Fig. 16A.

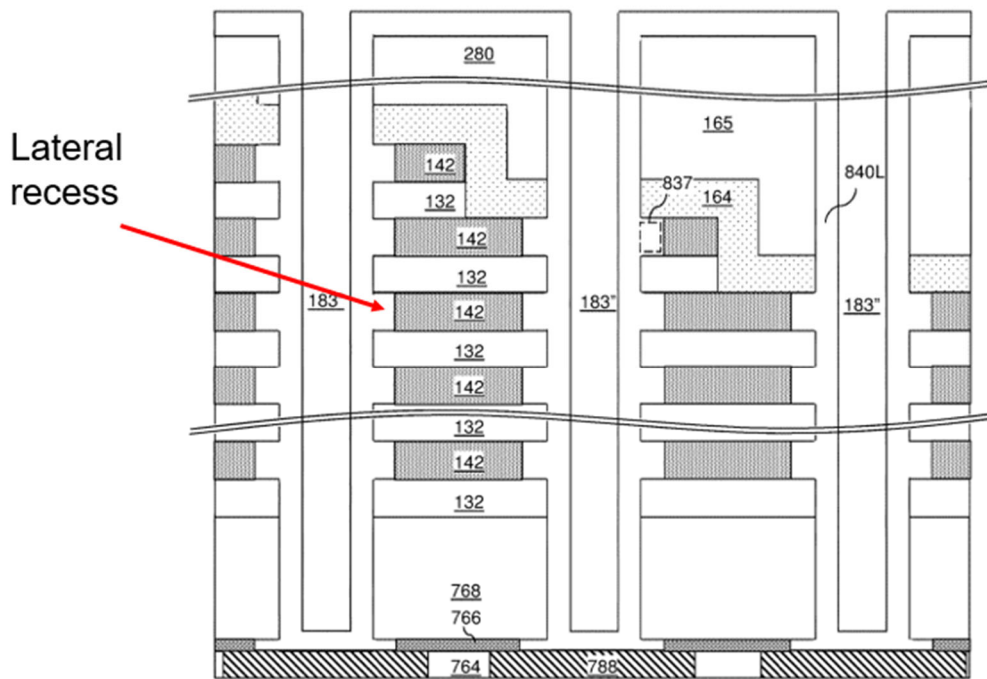


FIG. 41A

Id., Figs. 16A, 41A.

173. The ribbed via cavity in Cui creates additional space. In effect, the spacer, or liner, is longer now, because it travels into and out of the lateral recesses. The '322 Patent describes this same purpose of the lateral recesses. Ex. 1001, 13:38-51. Cui refers to these additional regions as “rib regions.” Ex. 1037 (Cui), 26:23-32. The dielectric material, i.e., the spacer, will additionally fill these rib regions

174. Implementing the rib regions provide two fundamental options. First, the rib regions can be made in the sacrificial or conductive gates. Second, the rib regions can be made in the dielectric layers. Both result in the same additional space. It is only a matter of selecting one of two options. Etching these regions in each

layer type was known. Ex. 1037 (Cui), Fig. 16A, 26:23-32 (recesses in dielectric layers), 44:65-45:25 (recesses in sacrificial layers); Ex. 1027 (Kai), 11:9-34 (recesses in sacrificial gates).

175. A POSITA would have had a high expectation of success in forming the rib regions. Again, etch chemistries that naturally create small lateral recesses were known. Further, isotropic and selective etches were well known, and selecting an etch chemistry to a certain selectivity was well known. E.g., Ex. 1037 (Cui), 26:33-45; Ex. 1027 (Kai), 11:9-34 (recesses in sacrificial gates).

6. Claim 8:

[8.PRE] “A three-dimensional (3D) memory device, comprising:”

176. This limitation is identical to [1.PRE] and met for the same reasons.

[8.A] “a substrate;”

177. This limitation is identical to [1.A] and met for the same reasons.

[8.B] “a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;”

178. This limitation is identical to [1.B] and met for the same reasons.

[8.C] “a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack; and”

179. This limitation is identical to [1.C] and met for the same reasons.

[8.D] “a through array contact (TAC) comprising a substantially circular section and extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate.”

180. My analysis under identical to [1.D] demonstrates that Nishikawa in view of the knowledge of a POSITA renders this limitation obvious. Specifically, it would have been obvious to implement Nishikawa’s TAC 76 as circular TAC, wherein a conformal spacer and conductive also assume circular shapes. The spacer insulates the conductive core of Nishikawa’s TAC 76 and thus extend through the entire stack. The conductive core contacts the spacer because the deposition of the conductive core fills the remaining void after forming the spacer.

7. Claim 9:

[9.PRE] “The 3D memory device of claim 8, further comprising:”

181. Nishikawa renders obvious the 3D memory device of Claim 8. *See* §IX.B.6, above.

[9.A] “a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate;”

182. This limitation is identical to [2] and met for the same reasons.

[9.B] “wherein a thickness of the spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact.”

183. My analysis under Claim [6.C] demonstrates that it would have been obvious to simultaneously form the TACs and peripheral contacts and to form them with the same diameter, thereby saving significant process time and simplifying the

185. As another example, Nakajima discloses forming one type of contact (C4) in various parts of the array, and depicts the same structure size:

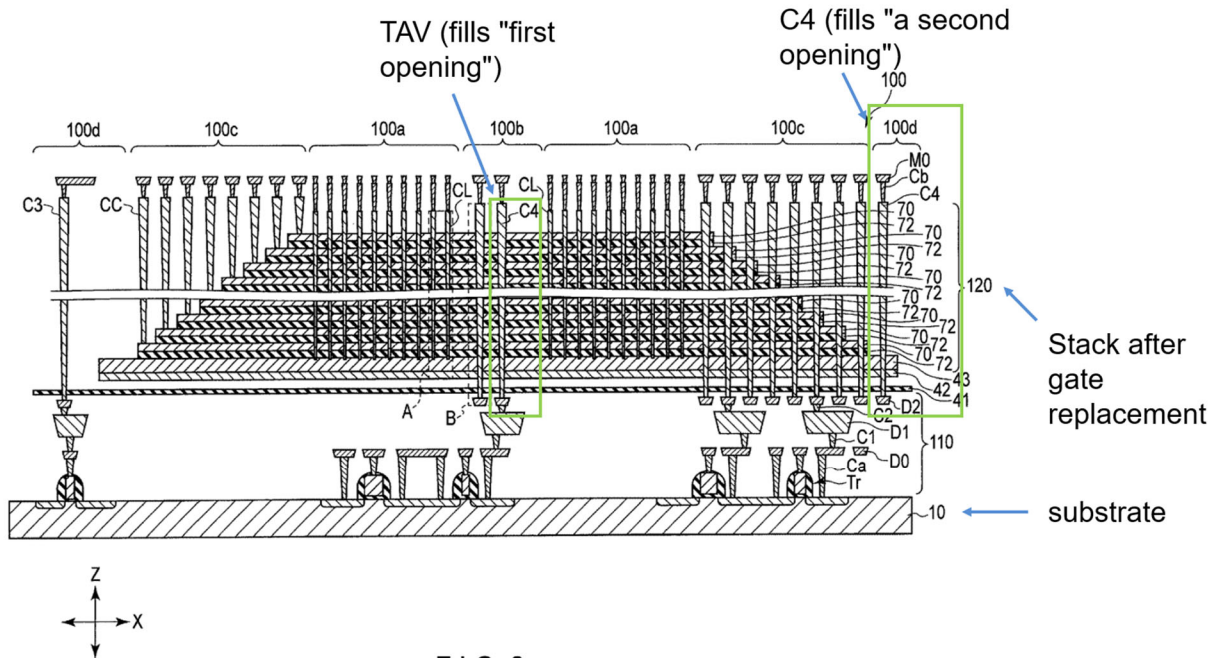


FIG. 2

Ex. 1009 (Nakajima), Fig. 2 (annotated). Accordingly, it would have been understood, or at least obvious, that forming the contacts with the same process and of the same size, results in spacers of nominally identical thickness.

8. Claim 10:

[10] “The 3D memory device of claim 9, wherein the spacer of the TAC and the spacer of the peripheral contact comprise a same material.”

186. As I describe below, Nishikawa discloses, or at least renders obvious in view of the knowledge of a POSITA, this limitation.

187. Nishikawa discloses that its backside contact via structure 76 and peripheral contacts include dielectric spacers. Nishikawa, 6:39-59. First, a POSITA

would have understood Nishikawa to disclose these spacers comprising the same material, i.e., a select dielectric material. Second, a POSITA would have understood, or at least found obvious, such a select dielectric material to be silicon oxide, as I explain in my analysis for Claim [3.B] (e.g., because Nishikawa describes similar structures to be silicon oxide).

9. Claim 13:

[13] “The 3D memory device of claim 8, wherein a first lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.”

188. This limitation is identical to Claim 7 and met for the same reasons.

10. Claim 14:

[14.PRE] “A three-dimensional (3D) memory device, comprising:”

189. This limitation is identical to [1.PRE] and is met for the same reasons.

[14.A] “a substrate;”

190. This limitation is identical to [1.A] and is met for the same reasons.

[14.B] “a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;”

191. This limitation is identical to [1.B] and is met for the same reasons.

[14.C] “a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;”

192. This limitation is identical to [1.C] and is met for the same reasons.

[14.D] “a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a substantially circular section; and”

193. This limitation is substantively the same as [8.D] (but does not recite a spacer) and is met for the same reasons.

[14.E] “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,”

194. This limitation is identical to a limitation in [3.A] and is met for the same reasons.

[14.F] “wherein: a first diameter of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs; and”

195. This limitation is identical to [7] and is met for the same reasons.

[14.G] “a peripheral contact is arranged outside the memory stack and in contact with a peripheral device on the substrate.”

196. This limitation is substantively the same as [2] and is met for the same reasons.

11. Claim 15:

[15.PRE] “The 3D memory device of claim 14, wherein:”

197. Nishikawa in view of the knowledge of a POSITA renders obvious the 3D memory device of Claim 14. *See* §IX.B.10.

[15.A] “a thickness of a spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact; and”

198. This limitation is substantively the same as [9.B] and is met for the same reasons.

[15.B] “a diameter of the TAC is at least equal to a diameter of the peripheral contact.”

199. This limitation is substantively the same as [6.C] and is met for the same reasons.

12. Claim 16:

[16] “The 3D memory device of claim 15, wherein: a diameter of the dummy channel structure is smaller than each of the diameter of the TAC and the diameter of the peripheral contact.”

200. This limitation is identical to [6.D] and is met for the same reasons.

13. Claim 19:

[19] “The 3D memory device of claim 1, wherein: the TAC has a substantially circular section and comprises a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC.”

201. This limitation is substantively the same as [8.D] and is met for the same reasons.

14. Claim 20:

[20] “The 3D memory device of claim 14, wherein: the TAC comprises a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC.”

202. This limitation is substantively the same as [8.D] and is met for the same reasons.

C. Ground 2: Nishikawa in View of Lu and the Knowledge of a POSITA Render Obvious Claims 4-5, 11-12, and 17-18

1. Motivation to Combine

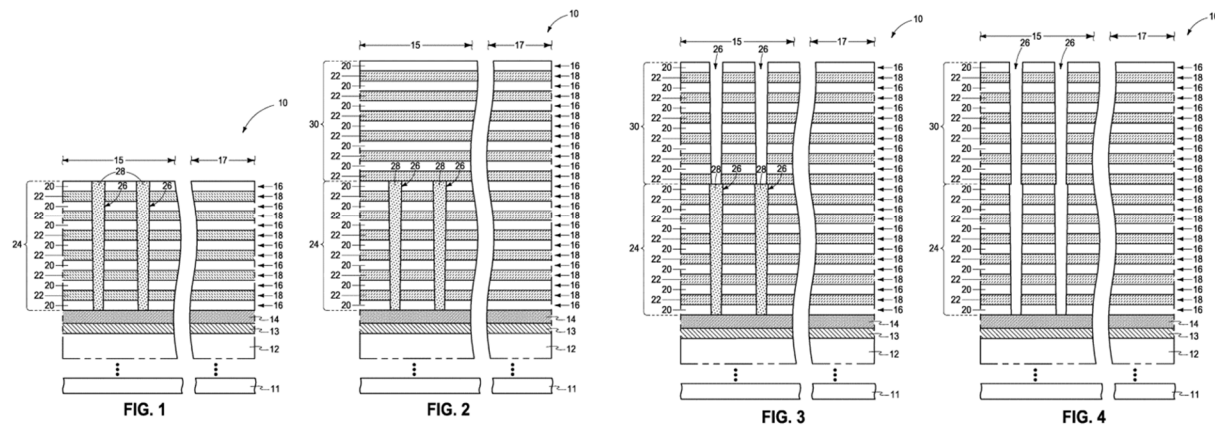
203. As I explain in detail below, a POSITA would have been motivated to combine Nishikawa with Lu's teachings of multi-deck 3D memory stacks with a reasonable expectation of success for several reasons.

204. A multi-deck memory stack refers to forming a first stack of alternating dielectric layers and conductive (or sacrificial) layers, then forming a second stack of the same layers thereon, and potentially forming additional stacks thereon. Typically, as I describe below, additional processing is done on a stack before forming another stack thereon. In short, a deck can be thought of a conventional memory stack.

205. The design of multi-deck structures was the result of challenges in etching high aspect ratio channel holes. Recall that memory designs typically attempt to achieve a very dense memory array. In 3D NAND, this requires a memory with many layers and forming high-aspect ratio holes through that stack. These high-aspect holes became a limiting factor to memory density. Ex. 1010 (Micheloni), 211-215.

206. A multi-deck structure significantly aids in forming high-aspect ratio holes. As I explain below, in simple terms, a two-deck stack reduces the taper of the etch by a factor of two, effectively narrowing the width of the top of the memory

hole by a factor of two. The typical process involves forming the first deck and etching a hole through the first deck. Then, the process forms the second deck and etches a hole through that deck, and that hole will intersect with an underlying hole (of course, this is done for a larger pattern of holes). An exemplary two-deck etch process is shown below:



Ex. 1036 (Tessariol), Figs. 1-4. Note, as shown above, a sacrificial fill in the first deck hole may be formed, and later etched. After forming the holes through the decks, the channel structure may be formed (though a first channel structure can be formed before forming the second deck):



FIG. 5

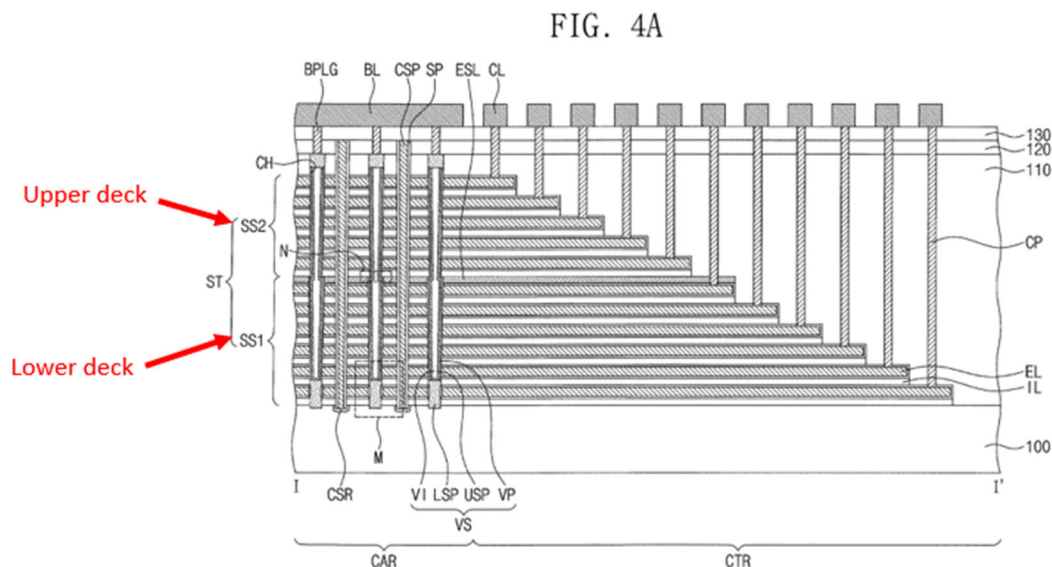
Id., Fig. 5 (annotated).

207. Importantly, as shown above, each hole tapers as the hole gets deeper. The top of each hole (for the top and bottom decks) is the same diameter, tapering to the bottom of each hole, wherein the top hole diameter is the same size for both holes. The taper is a result of the etchants being in contact with the top portion of each hole (for each deck) longer. If there was a single etch through both decks, the amount of taper would significantly increase, because the time in which the etchants were in contact with the top of the top hole would increase because of the long etch time to etch through the entire stack. In simple terms, the taper would be twice as much when comparing an X-layer single deck design versus X-layer two-deck

design. This reduces the density of the channels in a given area by approximately two.

208. Because of this intuitive footprint saving from a multi-deck design, multi-deck designs became well known well before the filing of the '322 Patent, and efforts began to focus on the details of the multi-deck designs. For example, Micron was improving the process of multi-decks, recognizing this benefit of separately etching through each stack: "A deck-by-deck process flow has an advantage of a lower etching aspect ratio." Ex. 1040, 1:28-29. This refers to forming the sub-holes in each deck does not require etching a single, very high-aspect ratio hole.

209. For all these reasons, multi-deck 3D memories became conventional before the '322 Patent. For example, U.S. Patent No. 10,381,369 (Ex. 1041) discloses a multi-deck 3D NAND stack structure:



Ex. 1041, Fig. 4A (annotated).

210. Kim 369 discloses that “[a] cell array block BLK may be disposed on the substrate 100. The cell array block BLK may include stack structures ST, each of which includes insulating layers IL and electrodes layers EL which are vertically alternately stacked (sometimes referred to as alternating electrode layers and insulating layers). Each of the stack structures ST may include a lower structure SS1 and an upper structure SS2. The upper structure SS2 may be disposed on the lower structure SS1.” Ex. 1041, 5:60-6:1.

211. Masamori discloses a multi-deck 3D NAND stack structure:

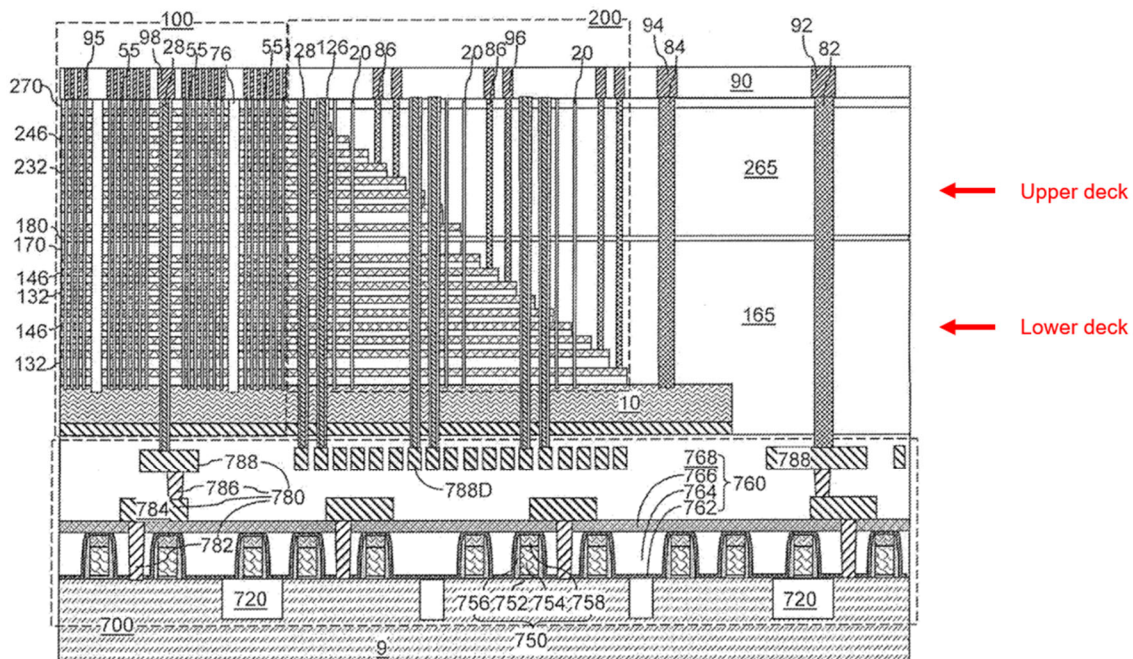


FIG. 14

Ex. 1020, Fig. 14 (annotated). Masamori discloses that “[a] second tier structure can be formed over the first tier structure (132, 142, 170, 131). The second tier structure can include an additional alternating stack of insulating layers and spacer material

layers, which can be sacrificial material layers. For example, a second alternating stack (232, 242) of material layers can be subsequently formed on the top surface of the first alternating stack (132, 142).” *Id.*, [0073].

212. Lu is entitled “Apparatuses and methods for forming multiple decks of memory cells.” Lu, Cover. Lu discloses that “[a]s demand for storage capacity increases, the number of memory cell levels in some memory devices may be increased to accommodate the increased storage capacity. In some cases, forming such memory devices using conventional techniques may pose a challenge.” *Id.*, 1:13-22. Lu would have been understood to be referring to the difficulties of forming high-aspect ratio holes in the memory stack that I describe above. Accordingly, Lu discloses techniques to form a first deck, etch the channel sub-hole, form a deck on top of that, and then etch another channel sub-hole. *E.g., id.*, Fig. 3A-L. Again, as I describe above, the major benefit from this is reducing the taper of the holes because of forming two separate holes (each half in height when comparing the two holes to a single hole through the entire stack height) that intersect. Thus, a POSITA would have been highly motivated to employ Lu’s teachings, and multi-deck teachings in general, to at least reduce the widths of the channel holes in Nishikawa’s memory and increase memory density.

213. A POSITA would have had a reasonable expectation of success in adapting Nishikawa to include a multi-deck structure. First, multi-deck structures

were the norm, including multi-deck designs that employ TACs. Typically, the process first creates the multi-deck structure and channels, then the TACs and slits. *E.g.*, Ex. 1036 (Tessariol), [0029]-[0033] (forming decks and channels), [0034]-[0037] (forming staircase), [0038]-[0040] (forming TACs and dummy structures), [0041]-[0044] (forming trenches and performing gate replacement process). Forming the TACs and slits often occurs after formation of all the decks, because the TACs do not require such high-aspect ratio holes in a dense array. In short, all of Nishikawa's other 3D structures are compatible with a multi-deck design. Thus, a POSITA would have had a reasonable expectation of success in implementing the alternating stack (32, 46) of Nishikawa as a multi-deck structure.

2. Claim 4:

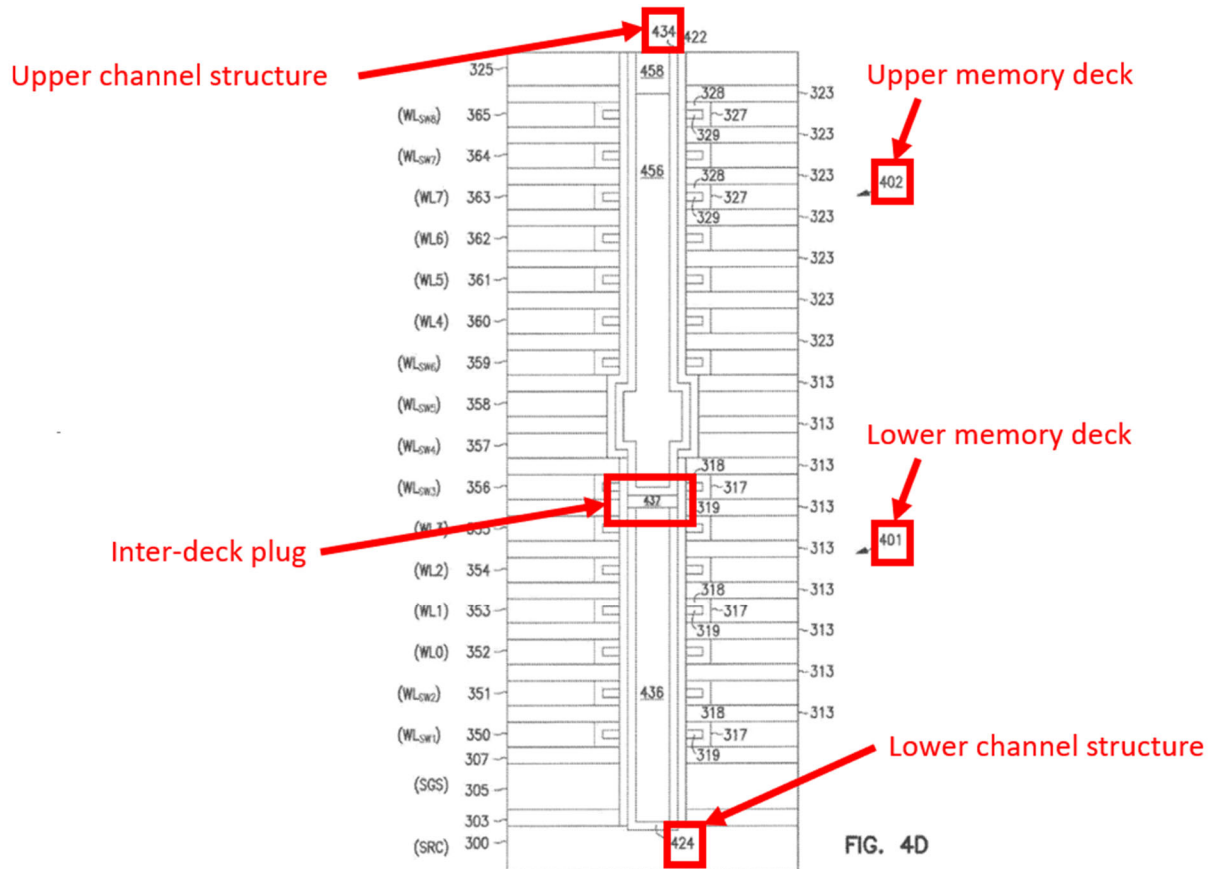
[4.PRE] "The 3D memory device of claim 1, wherein the memory stack comprises:"

214. Nishikawa discloses or renders obvious in view of the knowledge of a POSITA the 3D memory device of Claim 1. *See* §IX.B.1.

215. As discussed in §IX.B.1[1.B], Nishikawa discloses a memory stack having alternating dielectric and conductor layers. As the below demonstrates, it would have been obvious to implement this memory stack as a multi-deck structure to include lower and upper decks in view of Lu's teachings.

[4.A] “a lower memory deck on the substrate; and”

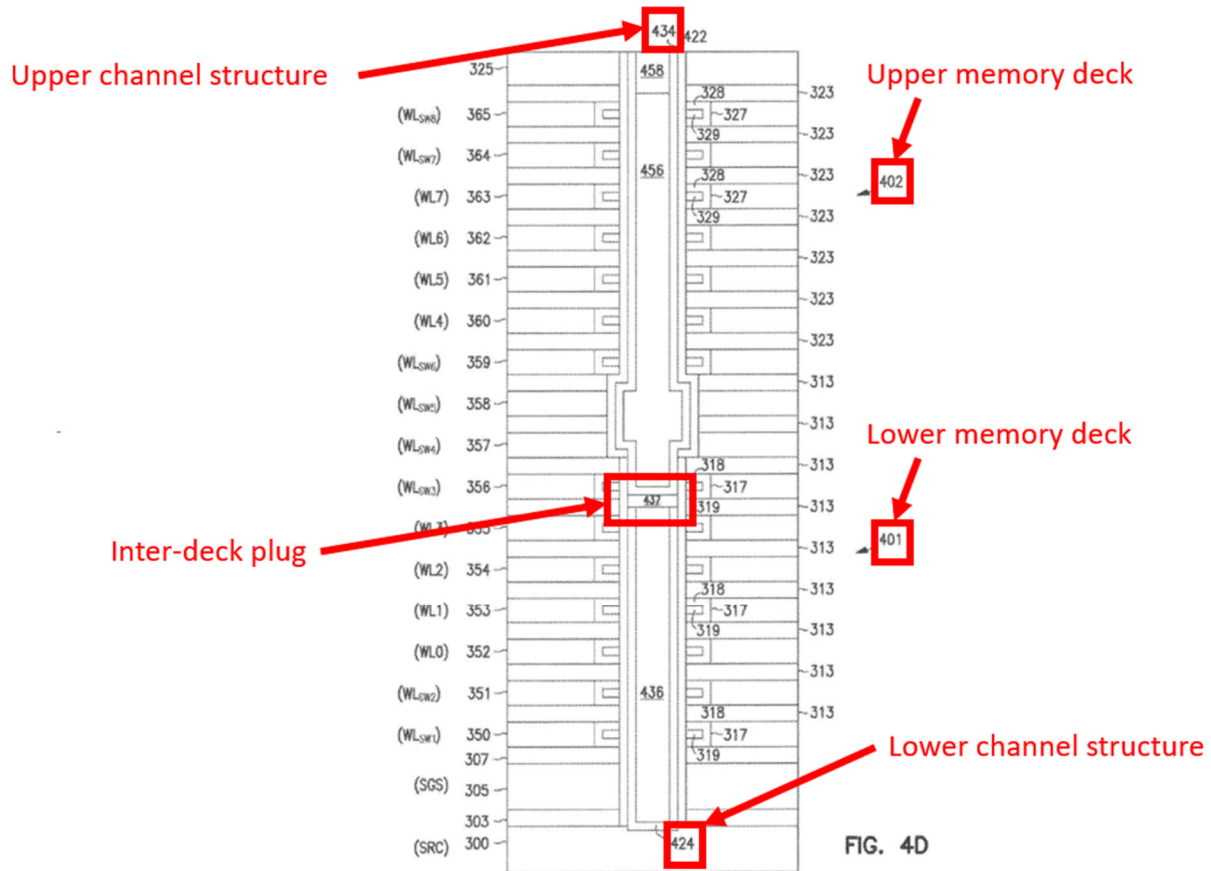
216. Lu discloses a lower memory deck (“deck 401”) and a substrate (“source material 300”). Lu discloses, for example, “source material 300 can include a conductively doped region of a semiconductor substrate.” Lu, 8:25-26. Recall that the bottom of the channels connect to a common source region in the substrate.



Lu, Fig. 4D (annotated), 14:29-44 (lower deck 401), 14:59-61 (decks 401 and 402).

[4.B] “an upper memory deck above the lower memory deck.”

217. Lu discloses an upper memory deck (“deck 402”) above the lower memory deck (“deck 401”).



Lu, Fig. 4D (annotated) 14:59-61 (deck 402).

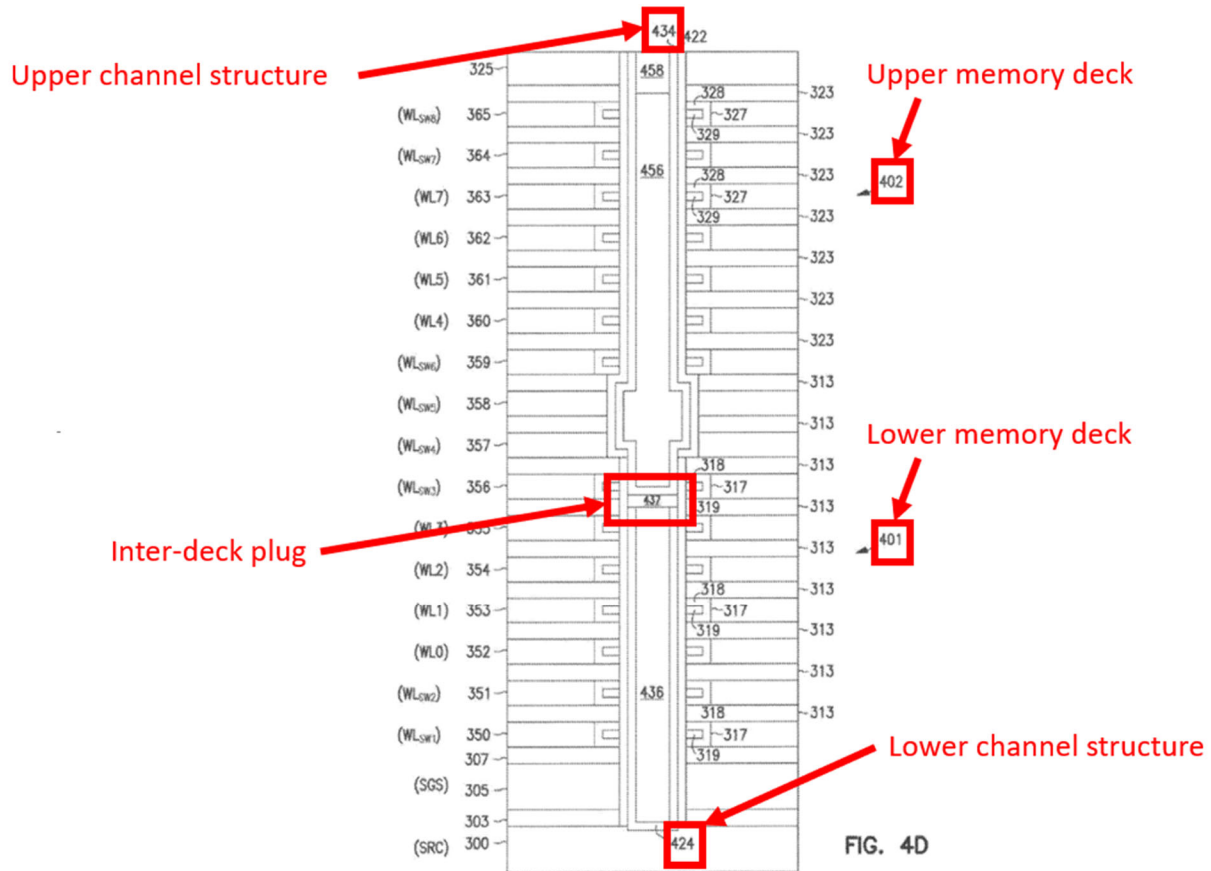
3. Claim 5:

[5.PRE] “The 3D memory device of claim 4, wherein the channel structure comprises:”

218. Nishikawa in view of Lu and the knowledge of a POSITA renders obvious the 3D memory device of Claim 4. See §IX.C.2.

[5.A] “a lower channel structure extending vertically through the lower memory deck;”

219. Lu discloses a lower channel structure (a channel material 424) extending vertically through the lower memory deck (“deck 401”).

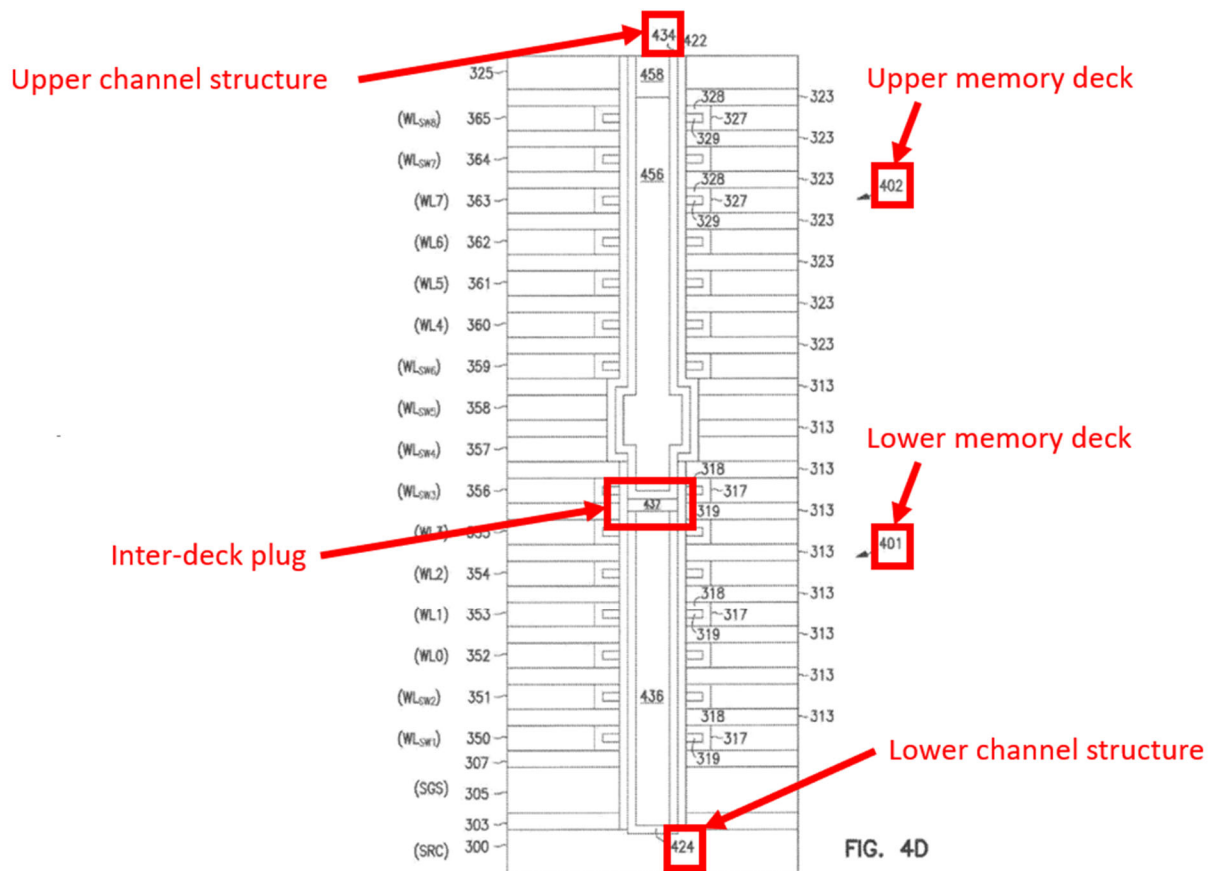


Lu, Fig. 4D (annotated). Lu discloses “deck 401 can include a hole 410 extending through materials that include conductor materials 350 through 358, dielectric materials 313, and capping material 315. Hole 410 can contain tunneling material 312 on its sidewalls. At a portion of hole 410 (e.g., portion from source material 300 to approximately dielectric material 313 between conductor materials 355 and 356), *a channel material 424 is formed adjacent tunneling material 312 and source material 300*. A dielectric material 436 is also formed in hole 410 and is surrounded by channel material 424.” *Id.*, 14:29-38. The channel material 424 is the channels

of the memory cells of the memory string. It is a continuous layer of the memory string.

**[5.B] “an upper channel structure extending vertically through the upper memory deck;
and”**

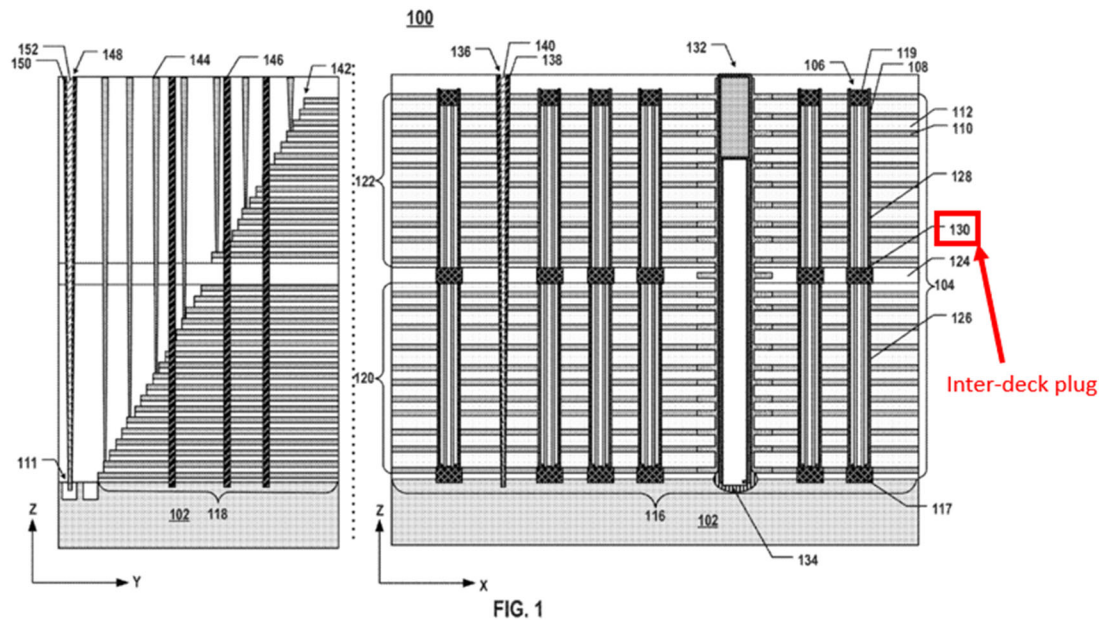
220. Lu discloses an upper channel structure (“channel material 434”) extending vertically through the upper memory deck (“deck 402”). This structure, in effect, is the companion to the lower channel structure 424. It forms the top channel layer of the memory string.



Lu, Fig. 4D (annotated), 14:59-62 (channel material 434).

[5.C] “an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.”

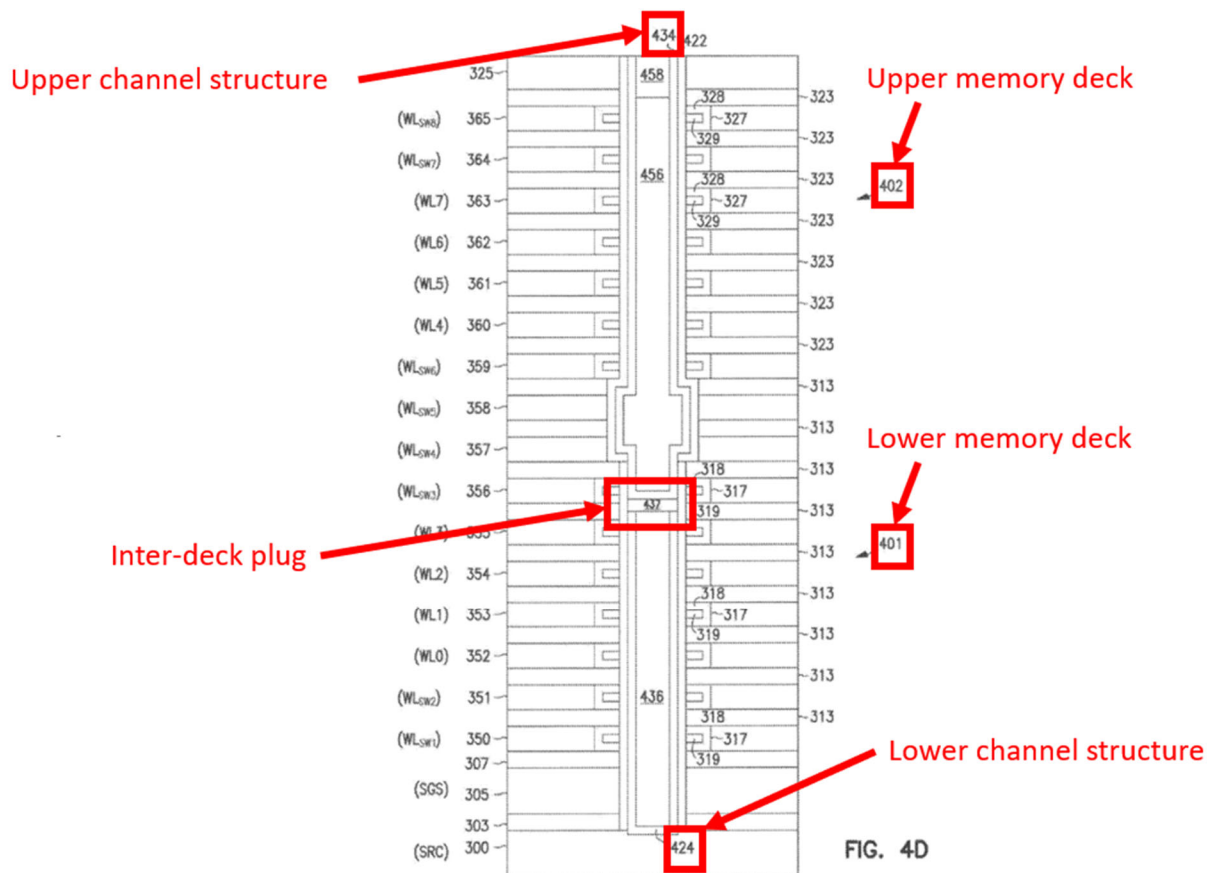
221. The '322 Patent depicts “inter-deck plug” 130 as follows:



Ex. 1001, Fig. 1 (annotated). The '332 Patent discloses that “an inter-deck plug 130 is disposed vertically between and in contact with lower channel structure 126 and upper channel structure 128. Inter-deck plug 130 can include semiconductor materials, such as polysilicon, and joint (e.g., electrically connect) lower and upper channel structures 126 and 128 to form channel structure 108.” Ex. 1001, 7:60-66. In short, this “plug” electrically couples the lower and upper channel structures.

222. Lu discloses exactly the same plug structure between the lower and upper decks. Specifically, Lu discloses an inter-deck plug (“material 437”) disposed

vertically between and in contact with the lower channel structure (“channel material 424”) and the upper channel structure (“channel material 434”):



Lu, Fig. 4D (annotated). As can be seen, because the plug is wider in diameter than the lower and upper channel structures, the lower and upper channel structure need not align perfectly, because the plug will ensure electrical coupling.

223. Lu discloses “with reference to FIG. 4A through FIG. 4D may be used to form a . . . channel with solid conductive plug (e.g., polysilicon plug) between the . . . channel.” Lu, 14:25-28. Lu further discloses that “[a] material 437 can be formed adjacent tunneling material 312 Material 437 can include polysilicon

(e.g., conductively doped polysilicon).” *Id.* 14:38-43. Conductive polysilicon material 437 is formed between and in contact with the lower channel material 424 and upper channel material 434. Again, this structure electrically couples the lower and upper channel structure, accounting for potential misalignment between these structures. It interfaces the lower and upper channel structures.

4. Claim 11:

[11.PRE] “The 3D memory device of claim 8, wherein the memory stack comprises:”

224. Nishikawa in view of the knowledge of a POSITA renders obvious the 3D memory device of Claim 8. *See* §IX.B.6.

[11.A] “a lower memory deck on the substrate; and”

225. This limitation is identical to [4.A] and is met for the same reasons.

[11.B] “an upper memory deck above the lower memory deck.”

226. This limitation is identical to [4.B] and is met for the same reasons.

5. Claim 12:

[12.PRE] “The 3D memory device of claim 11, wherein the channel structure comprises:”

227. Nishikawa in view of Lu and the knowledge of a POSITA renders obvious the 3D memory device of Claim 11. *See* §IX.C.4.

[12.A] “a lower channel structure extending vertically through the lower memory deck;”

228. This limitation is identical to [5.A] and is met for the same reasons.

[12.B] “an upper channel structure extending vertically through the upper memory deck; and”

229. This limitation is identical to [5.B] and is met for the same reasons.

[12.C] “an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.”

230. This limitation is identical to [5.C] and is met for the same reasons.

6. Claim 17:

[17.PRE] “The 3D memory device of claim 14, wherein the memory stack comprises:”

231. Nishikawa in view of the knowledge of a POSITA renders the 3D memory device of Claim 14 obvious. *See* §IX.B.10.

[17.A] “a lower memory deck on the substrate; and”

232. This limitation is identical to [4.A] and is met for the same reasons.

[17.B] “an upper memory deck above the lower memory deck.”

233. This limitation is identical to [4.B] and is met for the same reasons.

7. Claim 18:

[18.PRE] “The 3D memory device of claim 17, wherein the channel structure comprises:”

234. Nishikawa in view of Lu and the knowledge of a POSITA renders obvious the 3D memory device of Claim 17. *See* §IX.C.6.

[18.A] “a lower channel structure extending vertically through the lower memory deck;”

235. This limitation is identical to [5.A] and is met for the same reasons.

[18.B] “an upper channel structure extending vertically through the upper memory deck; and”

236. This limitation is identical to [5.B] and is met for the same reasons.

[18.C] “an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.”

237. This limitation is identical to [5.C] and is met for the same reasons. In summary, a POSITA would have had a reasonable expectation of success in combining the teachings of Nishikawa and Lu to implement the claimed 3D memory device due to the compatibility of their disclosed structures and the routine nature of the underlying fabrication processes. Nishikawa’s 3D NAND architecture provides a foundational memory stack with alternating dielectric and conductive layers, while Lu’s multi-deck structure directly addresses known challenges of high-aspect-ratio etching and enhances memory density by dividing the memory stack into manageable layers. These techniques were widely adopted in the industry and relied on standard processes such as forming sub-holes in individual decks, conformal deposition of silicon oxide spacers, and integration of inter-deck plugs to electrically couple stacked decks. The predictable results of these combined teachings align with conventional practices, minimizing the need for undue experimentation. As both references describe complementary aspects of 3D NAND fabrication, a POSITA would have readily recognized that integrating Lu’s multi-deck strategy into Nishikawa’s architecture would be a routine and reliable enhancement.

**D. GROUND 3: NISHIKAWA IN VIEW OF NISHIKAWA2 AND
THE KNOWLEDGE OF A POSITA RENDER OBVIOUS
CLAIMS 1-3, 6-10, 13-16, AND 19-20**

238. My analysis for Ground 3 applies the same claim mapping as Ground 1 and I do not repeat it here. I have been asked, however, to consider specific motivations for combining Nishikawa and Nishikawa2. In my opinion, a POSITA would have been motivated to combine Nishikawa with Nishikawa2, and specifically, Nishikawa2's express reference to a circular TAC for the source line connections for several reasons.

239. As I describe in IX.A.1-2, Nishikawa and Nishikawa2 disclose the same memory architecture. Both are SanDisk patents to the same inventor and clearly relate to the same design work. This is also apparent from the provisional applications leading to these patents being filed only 5 days apart. Nishikawa, Cover; Nishikawa2, Cover. Given this, a POSITA would have been strongly inclined to consider these related disclosures, particularly because one may include more detail to disclose additional options or features. It is normal practice for POSITAs to consider a set of material when considering a memory design or general approach to a problem.

240. Nishikawa2 expressly recognizes that the source line connection can be circular. Under my analysis of [1.D], I discuss that Nishikawa2 recognizes that this can increase memory capacity and explain that by removing the large trench, more

room is available for channel structures. Nishikawa2, 22:38-41, 27:55-28:3. There, I also describe that spreading the source line connections throughout the array also provides additional contact points for these connections, effectively weaving them throughout the array while not requiring large trench structures. I demonstrate that this approach was textbook material. Thus, a POSITA would have recognized the specific benefits that Nishikawa2 teaches with respect to its circular TAC.

241. I explain in my analysis of [1.D] that a POSITA would have had a reasonable expectation of success in implementing a circular TAC in Nishikawa and do not repeat it here. I also note, however, that a POSITA would have expected the features within the Nishikawa references to be compatible given the same memory architecture and same inventor for the same company.

E. GROUND 4: NISHIKAWA IN VIEW OF NISHIKAWA2 AND LU AND THE KNOWLEDGE OF A POSITA RENDER OBVIOUS CLAIMS 4-5, 11-12, AND 17-18

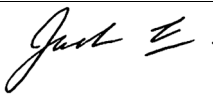
242. My analysis for Ground 4 applies the same claim mapping as Ground 3 and I do not repeat it here. Similar to Ground 3, I was asked whether a POSITA would be motivated to likewise combine Nishikawa with Nishikawa2 and Lu. A POSITA would have been motivated to combine Nishikawa and Nishikawa2 for the same reasons set forth in Ground 3. Likewise, a POSITA would have been motivated include a multi-deck structure for the same reasons in Ground 4. Finally,

that the TAC is circular has no impact on the expectation of success, because circular TACs through multi-deck structures were commonplace. *See* §VI.

F. Secondary Considerations of Non-Obviousness

243. Based on my review of the '322 Patent's file history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims. Nor am I otherwise aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like relating to the '322 Patent. Instead, as discussed above, it is my opinion that the subject matter embraced by the challenged claims was known in and obvious over the prior art.

244. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: December 2, 2024
Location: Austin TX
Signature: 
DR. JACK C. LEE