Jack C. Lee
Professor Emeritus
Electrical and Computer Engineering Department
The University of Texas at Austin

Current Status
Professor Emeritus
Department of Electrical and Computer Engineering
The University of Texas at Austin

Research / teaching experience and expertise:

- Integrated circuits manufacturing
- Photovoltaic/solar cell technologies
- Alternative channel devices
- Dielectric and passivation processes
- Display technologies
- Semiconductor memory devices

Education

9/84 – 8/88	Ph.D., Electrical Engineering, University of California at Berkeley
9/80 – 12/81	M.S., Electrical Engineering, University of California at Los Angeles
9/76 – 6/80	B.S., Electrical Engineering (with highest honors), University of California at Los Angeles

Professional Career

9/23 – present	Professor Emeritus Department of Electrical and Computer Engineering The University of Texas at Austin
9/00 – 8/23	Cullen Trust for Higher Education Endowed Professorship in Engineering #4 Department of Electrical and Computer Engineering The University of Texas at Austin
9/96 – 8/23	Professor, Department of Electrical and Computer Engineering The University of Texas at Austin
9/92 – 8/96	Associate Professor, Department of Electrical and Computer Engineering The University of Texas at Austin
9/88 – 8/92	Assistant Professor, Department of Electrical and Computer Engineering The University of Texas at Austin
1/88 – 6/88	Lecturer, Electrical Engineering and Computer Science Department University of California at Berkeley
6/79 – 8/84	Member of Technical Staff, High-Speed Bipolar Device Program TRW Microelectronics Center, Redondo Beach, CA

Honors and Awards

IEEE Electron Devices Society Distinguished Lecturer, 2004 - 2016.

Fellow, The Institute of Electrical and Electronic Engineers (IEEE), 2002 "For contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices"

Gordon Lepley IV Endowed Memorial Teaching Award, ECE Department, The University of Texas at Austin, 2004

Cullen Trust For Higher Education Endowed Professorship in Engineering, 2000-present
Dean's Fellow, College of Engineering, The University of Texas at Austin, 1999, 2003
Lockheed Fort-Worth Division Award for Excellence in Engineering Teaching, College of Engineering, The University of Texas at Austin, 1996
Award of Excellence, Halliburton Foundation, 1993
Departmental Teaching Award, College of Engineering, The University of Texas at Austin, 1993
SRC Inventor Recognition Award, Semiconductor Research Corporation, 1991
Hughes Aircraft Company Endowed Faculty Fellowship in Engineering, The University of Texas at Austin, 1991- 2000
Outstanding Engineering Teaching by an Assistant Professor, College of Engineering, The University of Texas at Austin, 1991
Best Paper Award, SEMATECH Centers of Excellence Coordination Meeting, 1990.
Dow Outstanding Young Faculty Award, American Society for Engineering Education, 1990
Engineering Research Initiation Award, Engineering Foundation of the United Engineering Trustees, 1989
Best Paper Award, IEEE International Reliability Physics Symposium, 1988

Litigation Experience as Testifying Experts
The following is a list of cases in which I have provided expert testimony, including through a declaration, report or testimony at deposition or trial since 2016

- Yangtze Memory Technologies v. Micron
  January 2024 –
  Case No. 3:23-cv-05792-RFL (Northern District of California)
  (Representing defendant, Micron)

- BeSang v. Micron
  March 2023 –
  Case No. 2:23-cv-00028 (Eastern District of Texas)
  Case No. IPR2023-00900
  (Representing defendant, Micron)

- The Trustees of Purdue University v. Wolfspeed, Inc.
  February 2022 -
  Case No. 1:21-cv-840 (Middle District of North California)
  (Representing defendant, Wolfspeed)

- GlobalFoundries - IPR
  March 2021 –
  Case No. IPR2022-00xx
  (Representing defendant and filed an IPR declaration)

- HD Silicon Solutions LLC v. Microchip Technology Inc.
  January 2021 –

Case No. 6:20-cv-1092 Western District of Texas, Waco Division
Case No. IPR2021-00752
(Representing defendant, Microchip Technology Inc.)

- Longitude Licensing Limited vs Western Digital
  March 2023 – January 2024
  Case No. IPR2023-00xx
  (Representing defendant, Western Digital)

- Impinj, Inc. v. NXP USA, Inc.
  September 2019 – July 2023
  Case No. 19-cv-03l61 (Northern District of California)
  Case No. 2:20-cv-01503-RSM-MAT (Western District of Washington, Seattle)
  (Representing defendant, NXP USA, Inc.)

- Monterey Research, LLC v. Qualcomm Inc.
  February 2020 – May 2022
  Case No. 1:19-cv-2083 (District of Delaware)
  (Representing defendant, Qualcomm)

- Bell Semiconductor, LLC v. Texas Instruments Incorporated
  July 2020 – March 2021
  Case No. 2:20-cv-00048 (Eastern District of TX, Marshall Division)
  (Representing defendant, Texas Instruments)

- Greenthread LLC v. Samsung
  February 2020 – July 2020
  Case No. 2:19-CV-00147-JRG Eastern District of Texas, Marshall
  (Representing plaintiff, Greenthread LLC)

- MLC Intellectual Property LLC vs. Micron Technology, Inc.,
  June 2016 –
  Case No. 3:14-cv-03657-SI, Northern District of California
  (Representing plaintiff, MLC Intellectual Property LLC)

- Hanwha v. LONGi Solar Technology
  April 2019 – June 2020
  ITC Investigation no. 337-TA-1151
  (Representing defendant LONGi Solar Technology)

- Vista Peak Ventures, LLC v. Innolux Corp.
  January 2019 – March 2019
  Case No. 2:18-cv-280 Eastern District of Texas, Marshall
  Case No. IPR2019-00xx
  (Representing IPR Petitioner, Innolux Corp.)

- Home Semiconductor Corp. v. Samsung
  August 2018 – June 2020
  Case No. 13-2033-RGA, The District of Delaware
  (Representing plaintiff, Home Semiconductor Corp.)

- Mariner IC Inc. v. Asustek Computer Inc. and Tivo Corp.
  May 2018 – Aug. 2019
  Case No. 2:18-cv-00069-JRG (Eastern District of Texas, Marshall Division)
  Case No. 2:18-cv-00166-JRG (Eastern District of Texas, Marshall Division)
  (Representing plaintiff, Mariner IC Inc.)

- Godo Kaisha IP Bridge 1 v. OmniVision Technologies, Inc.
  January 2018 – December 2018
  C.A. No. 16-290-JFB-SRF, The District of Delaware
  (Representing defendant, OmniVision Technologies, Inc.)

- Macronix v. Toshiba
  May 2017 – February 2018
  ITC Investigation No. 337-TA-1046
  (Representing defendant, Toshiba)

- University of Illinois v. Micron Technology
  September 2009 – November 2017
  Case No. 2:11-cv-02288, 7/23/2012, Central District of Illinois, Urbana Division
  (Representing plaintiff, Univ. of Illinois)

- Silicon Genesis v. Soitec
  October 2016 – March 2017
  ITC Investigation No. 337-TA-1025
  (Representing plaintiff, Silicon Genesis)

Non-Litigation Consulting

- Applied Materials, Inc.
  Teaching short courses on semiconductor physics, devices, design/layout, and fabrication technologies (2-3 courses per year).

Jack C. Lee is a Professor Emeritus of the Electrical and Computer Engineering Department. He held the Cullen Trust for Higher Education Endowed Professorship in Engineering # 4 at The University of Texas at Austin from 2000-2023. He received the B.S. and M.S. degrees in electrical engineering from University of California, Los Angeles, in 1980 and 1981, respectively; and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1988. From 1979 to 1984, he was a Member of Technical Staff at the TRW Microelectronics Center, CA, in the High-Speed Bipolar Device Program. He worked on bipolar device and circuit design, fabrication and testing. In 1988, he joined the faculty of The University of Texas at Austin. His current research interests include semiconductor devices including 3D structures such as FinFETs, fabrication processes, characterization and modeling, dielectric process, characterization and reliability, high-K gate dielectrics and electrode, semiconductor memory applications, alternative channel materials, display technologies and photovoltaic/solar cell technologies. Dr. Lee has over 40 years of experience in semiconductor technology and dielectric processing. He has published over 600 journal publications and conference proceedings and 9 patents; and co-authored 8 book and book chapters. He has also been recognized with many teaching and research awards. Dr. Lee is a Fellow of IEEE and had been a Distinguished Lecturer for the IEEE Electron Devices Society.

Publications
Jack C. Lee
Refereed Journal Publications

1. J. Lee, K. Mayaram and C. Hu, "A Theoretical Study of Gate/Drain Offset in LDD MOSFET's," IEEE Electron Device Letters, vol. EDL-7, no. 3, p. 152 - 154, March 1986.

2. J. Lee, I-C Chen and C. Hu, "Comparison Between CVD and Thermal Oxide Dielectric Integrity," IEEE Electron Device Letters, vol. EDL-7, no. 9, p. 506 - 509, September 1986.

3. K. Mayaram, J. Lee and C. Hu, "A Model for the Electric Field in Lightly Doped Drain Structures," IEEE Transactions on Electron Devices, vol. ED-34, no.7, p. 1509 - 1518, July 1987.

4. J. Lee and C. Hu, "Polarity Asymmetry of Oxides Grown on Polycrystalline Silicon," IEEE Transactions on Electron Devices, vol. ED-35, no. 7, p. 1063 - 1070, July 1988.

5. J. Lee, C. Hegarty and C. Hu, "Electrical Characteristics of MOSFET's Using Low-Pressure Chemical Vapor Deposited Oxide," IEEE Electron Device Letters, vol. EDL-9, no. 7, p. 324 - 327, July 1988.

6. J. Lee, I-C Chen and C. Hu, "Modeling and Characterization of Gate Oxide Reliability," Special Issue of IEEE Transactions on Electron Devices on Reliability, Vol. ED-35, no. 12, p. 2268 - 2278, December 1988.

7. H. Hwang, W. Ting, D. L. Kwong, J. Lee, L. Buhrow and R. Bowling, "Electrical Characteristics of Reoxidized-nitrided CVD Oxide," Applied Physics Letters, 55(8), p. 755 - 756, 21 August, 1989.

8. R. Moazzami, J. Lee and C. Hu, "Temperature Acceleration of Time-Dependent Dielectric Breakdown," Special issue of IEEE Transactions on Electron Devices on Vacuum Microelectronic Devices, vol. ED-36, no. 11, p. 2462 - 2465, November 1989.

9. H. Hwang, W. Ting, D.L. Kwong, J. Lee, L. Buhrow and R.A. Bowling, "Effects of Dynamic Stressing on Nitrided and Reoxidized-Nitrided Chemical Vapor Deposited Gate Oxides," IEEE Electron Device Letters, vol. EDL-10, no. 12, p. 568 - 570, December 1989.

10. J. Lin, S. Banerjee, J. Lee, and C. Teng, "Soft Breakdown in Titanium-Silicided Shallow Source/Drain Junction," IEEE Electron Device Letters, vol. EDL-11, no. 5, p. 191 - 193, May 1990.

11. K. Park, S. Batra, J. Lin, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain, and G. Lux, "Anomalous Capacitance-Voltage Behavior Due to Dopant Segregation and

Carrier Trapping in Arsenic-Implanted Polysilicon and Polycide Gates," Applied Physics Letters, vol. 56, no. 23, p.2325 - 2327, June 4, 1990.

12. J. Lin, S. Banerjee, J. Lee, and C. Teng, "Anomalous Current-Voltage Behavior in Titanium-Silicided Source/Drain Junctions," Journal of Applied Physics, vol. 68, no. 3, p. 1082 - 1087, August 1, 1990.

13. H. Hwang, W. Ting, B. Maiti, D.L. Kwong and J. Lee, "Electrical Characteristics of Ultrathin Gate Dielectrics Prepared by Rapid Thermal Oxidation of Si in N_2O," Applied Physics Letters, vol. 57, no. 10, p. 1010 - 1011, Sept. 3, 1990.

14. S. Batra, K. Park, J. Lin, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain and G. Lux "Effects of Dopant Redistribution, Segregation and Carrier Trapping in As-Implanted MOS Gates," IEEE Transactions on Electron Devices, vol. 37, no. 11, p. 2322 - 2330, October, 1990.

15. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "The Impact of Trench Isolation on Latch-up Immunity in Bulk, Non-epitaxial CMOS," IEEE Electron Device Letters, vol. EDL-12, no. 2, p. 77 - 79, February, 1991.

16. W. Ting, H. Hwang, J. Lee and D. L. Kwong, "Composition and Growth Kinetics of Ultrathin SiO_2 Films Formed by Oxidizing Si Substrate in N_2O," Applied Physics Letters, vol. 57, p. 2808 - 2810, 1990.

17. W. Ting, P.C. Li, G. Q. Lo, J. Lee and D.L. Kwong, "Metal-Oxide Semiconductor Characteristics of Rapid Thermal Processed Chemical Vapor Deposited SiO_2 Gate Dielectrics," Solid State Electronics, vol. 34, no. 4, p 385 - 388, 1991.

18. W. Ting, H. Hwang, J. Lee and D.L. Kwong, "Growth Kinetics of Ultrathin SiO_2 Films Prepared by Rapid Thermal Oxidation of Si Substrates in N_2O," Journal of Applied Physics, vol. 70, no. 2, p. 1072 - 1074, July 15, 1991.

19. J. Lin, K. Park, S. Batra, S. Banerjee, J. Lee and G. Lux, "Enhancement of Boron Diffusion Through Gate Oxides in MOS Devices During Rapid Thermal Silicidation," Applied Physics Letters, vol. 58, no. 19, p. 2123 - 2125, May 1991.

20. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "A Physical Model for Boron Penetration Through Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N_2O," Applied Physics Letters, vol. 59, no. 13, p. 1581 - 1582, September 23, 1991.

21. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "Improved Reliability Characteristics of Submicron nMOSFET's with Oxynitride Gate Dielectrics Prepared by Rapid Thermal Oxidation in N_2O," IEEE Electron Device Letters, vol. 12, no.9, p.495-497, September 1991.

22. J. Carrano, C. Sudhama, V. Chikarmane, J. Lee, A. Tasch, W. Shepherd and N. Abt, "Electrical and Reliability Properties of PZT Thin Films for ULSI DRAM Applications," IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, vol. 38, no. 6, p. 690 - 703, November 1991.

23. V. Chikarmane, C. Sudhama, J. Kim, J. Lee, A. Tasch and S. Novak, "Comparative Study of The Perovskite Phase Microstructure Evolution and Electrial Properties of PZT Thin Film Capacitors Annealed in Oxygen and Nitrogen Ambients," Applied Physics Letters, vol. 59, no. 22, p. 2850 - 2852, Nov. 25, 1991.

24. M. Hao and J. Lee, "Electrical Characteristics of Oxynitrides Grown on Textured Single-Crystal Silicon," Applied Physics Letters, vol. 60, no. 4, p. 445 - 447, January 27, 1992 .

25. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "Parametric Study of Latchup-Immunity of Deep Trench-Isolated, Bulk, Non-epitaxial CMOS," IEEE Trans. Elec. Dev., vol. 39, no. 4, p. 921 - 931, April 1992.

26. V. Chikarmane, J. Kim, C. Sudhama, J. Lee and A. Tasch, "Annealing of Lead Zirconate Titanate (65/35) Thin Films for Storage Dielectric Applications: Phase Transformations and Electrical Characteristics," Journal of Electronic Materials, vol. 21, no. 5, p. 503 - 512, May 1992.

27. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "Effects of Post-Deposition Annealing Ambient on the Electrical Characteristics and Phase Transformation Kinetics of Sputtered Lead Zirconate titanate (65/35) Thin Film Capacitors," Journal of Vacuum Science and Technology, vol. 10, no. 4, p. 1562 - 1568, July 1992.

28. V.K. Mathews, R. L. Maddox, P.C. Fazan, J. Rosato, H. Hwang and J. Lee, "Degradation of Junction Leakage in Devices Subjected to Gate Oxidation in Nitrous Oxide," IEEE Electron Device Letters, vol. 13, no. 12, p. 648 - 650, Dec. 1992.

29. B. Maiti, M. Hao, I. Lee and J. Lee,"Improved Ultrathin Oxynitride Formed by Thermal Nitridation and Low Pressure Chemical Vapor Deposition Process," Applied Physics Letters, vol. 61, p. 1790 - 1792, 1992.

30. B. Maiti and J. Lee, "Low-Pressure Chemical Vapor Deposited Silicon-Rich Oxides for Non-volatile Memory Applications," IEEE Electron Device Letters, vol. 13, no. 12, p. 624 - 626, Dec. 1992.

31. H. Hwang, M. Y. Hao, J. Lee, V. Mathews, P. Fazan and C. Dennison, "Furnace N_2O Oxidation Process for Submicron MOSFET Device Applications," Solid-State Electronics, vol. 36, p. 749 - 751, 1993.

32. H. Hwang, J. Lee, P. Fazan and C. Dennison, "Hot-Carrier Reliability Characteristics of Narrow Width MOSFETs," Solid-State Electronics, Vol. 36, No. 4, p. 665 - 666, 1993.

33. B. Maiti and J. Lee, "A New Low-Thermal Budget Process for Ultrathin Oxynitride Dielectrics," Journal of Electronic Materials, 1992.

34. J. Lin, W. Chen, S. Banerjee and J. Lee, "Cobalt Disilicide as a Dopant Diffusion Source for Polysilicon Gates in MOS Devices," Journal of Electronic Materials, vol. 22, p. 667 - 673, 1993.

35. W. Chen, J. Lin, S. Banerjee and J. Lee, "Thermal Stability and Dopant Drive-Out Characteristics of $CoSi_2$ Polycide Gates," Journal of Applied Physics, vol. 73, p. 4712 - 4714, May 1993.

36. J. Lee, V. Chikarmane, C. Sudhama, and J. Kim, "Sputtered PZT Thin Films for Memory Applications," Journal of Integrated Ferroelectrics, vol. 3, 1993.

37. C. Sudhama, J. Kim, J. Lee, W. Shepherd and E. Meyer, "The Effects of Lanthanum Doping on the Electrical Properties of Sol-Gel Derived Ferroelectric Lead Zirconate Titanate (PZT) for ULSI DRAM Applications," Journal of Vacuum Science and Technology, p. 1302 - 1309, July / Aug 1993.

38. M. Y. Hao, H. Hwang and J. Lee, "Silicon-Implanted SiO2 for Non-volatile Memory Applications," Solid-State Electronics, vol. 36, p. 1321 - 1324, 1993.

39. M. Y. Hao, H. Hwang and J. Lee, "Memory Effects of Silicon-Implanted Oxides for EEPROM Applications," Applied Physics Letters, vol. 62, No. 13, p. 1530 - 1532, March 1993.

40. S. Batra, K. Picone, K. Park, S. Bhattacharya, S. Banerjee, J. Lee, M. Manning and C. Dennison, "Study of Lateral Non-Uniformity as a Function of Junction Depth in Ultra-Shallow Junctions and Its Effects on Leakage Behavior in As-Deposited Polycrystalline Si and Amorphous Si Diodes," Solid-State Electronics vol. 36, no. 7, p. 955 - 960, 1993.

41. J. Lee, C. Sudhama, J. Kim and R. Khamankar, (Invited Paper) "High Dielectric Constant Ferroelectric Thin Films for DRAM Applications", Extended Abstracts of International Conf. on Solid State Devices and Materials, p. 850 - 852, 1993.

42. W. M. Chen, S. K. Banerjee, and J. C. Lee," Degradation mechanism and improvement of thermal stability of $CoSi_2$/polycrystalline Si layers," Applied Physics Letters, vol. 64, no. 12, p. 1505 - 1507, 1994.

43. W. M. Chen, J. Lin, S. K. Banerjee, and J. C. Lee," Simultaneous Shallow-Junction Formation and Gate Doping p-channel Metal-Semiconductor-Oxide Field-Effect

Transistor Process Using Cobalt Silicide as a Diffusion/Doping Source," Applied Physics Letters, vol. 64, no. 3, p. 345 - 347, 1994.

44. M. Y. Hao, B. Maiti, and J. Lee," Novel Process for Reliable Ultrathin Tunnel Dielectrics," Appl. Phys. Lett., vol.. 64, p. 2102 - 2104, April 1994.

45. B. Jiang, C. Sudhama, R. Khamankar, J. Kim and J. Lee, "Effects of Nonlinear Storage Capacitor on DRAM READ/WRITE," IEEE Electron Device Letters, vol. 15, no. 4, p.126 - 128, April 1994.

46. J. Kim, C. Sudhama, R. Khamankar, B. Jiang, J. Lee, P. Maniar, R. Moazzami, R. Jones and C. J. Mogab, "La Doped PZT Thin Films for Gigabit DRAM Technology," 1994 Symposium on VLSI Tech. Digest, p. 151 - 152, 1994.

47. M. Y. Hao, K. Lai, W. M. Chen, and J. Lee, " Surface Cleaning Effect on Dielectric Integrity for Ultrathin Oxynitrides Grown in N_2O," Applied Physics Letters, vol. 65, no. 9, p. 1133 - 1135, August 1994.

48. K. Lai, M. Y. Hao, C. Y. Hu, W. M. Chen, and J. Lee, " Effects of Surface Preparation on the Electrical and Reliability Properties of Ultrathin Thermal Oxide," IEEE Electron Device Letters, vol. ED-15, no. 11, p. 446 - 448, November, 1994.

49. M. Y. Hao, W. M. Chen, K. Lai, M. Gardner, J. Fulford, and J. Lee, "Correlation of Dielectric Breakdown with Hole Transport for Ultrathin Thermal Oxides and N_2O Oxynitrides," Applied Physics Letters, vol. 66, no. 9, p. 1126 - 1128, February 27, 1995.

50. R. Khamankar, J. Kim, C. Sudhama, B. Jiang, and J. Lee, "Effects of Electrical Stress Parameters on Polarization Loss in Ferroelectric PZT Thin Film Capacitors," Electron Device Letter, p. 130 - 132, April 1995.

51. J. Lee, B. Jiang, R. Khamankar, and J. Kim, "Nonlinearity of Ferroelectric Capacitors on DRAM R/W Operations," Integrated Ferroelectrics, p. 319 - 328, 1995.

52. W. M. Chen, M. Y. Hao, K. Lai, M. Gardner, J. Fulford, and J. Lee, " 'Turn-around' Effects of Stress-Induced Leakage Current of Ultrathin N_2O-Annealed Oxides," Applied Physics Letters, vol. 67, No. 5, p. 1 - 3, July 1995.

53. Kafai Lai, Wei-Ming Chen, Ming-Yin Hao, Mark Gardner, Jim Fulford, Jack C. Lee, "'Turn-around' effects of stress-induced leakage current of ultrathin N_2O-annealed oxides", Applied Physics Letters, vol. 67, no. 5, p. 673-5, Jul. 31, 1995.

54. Kafai Lai, Kiran Kumar, Anthony I. Chou, and Jack C. Lee, "Plasma damage and photo-annealing effects of thin gate oxides and oxynitrides during O_2 plasma exposure", IEEE Elec. Dev. Lett., vol. 17, no. 3, p. 82, Mar. 1996.

55. Anthony I. Chou, Kafai Lai, Kiran Kumar, Mark Gardner, Jim Fulford, and Jack C. Lee, "Optimization of gate dopant concentration and microstructure for improved electrical and reliability characteristics of ultrathin oxides and N_2O-oxynitrides", Applied Physics Letters, vol. 69, no. 7, p. 934, Aug. 12, 1996.

56 C. Lin, A. Chou, K. Kumar, P. Chowdhury, and J. C. Lee, "Effect of BF_2 implantation on ultra-thin gate oxide reliability" Appl. Phys. Lett., vol. 69, no. 11, p1591, Sep. 1996.

57. C. Lin, A. Chou, K. Kumar, P. Chowdhury, and J. C. Lee, "Reliability of gate oxide grown on nitrogen-implanted Si substrate" Appl. Phys. Lett. Vol. 69, No. 24, 9 Dec. 1996.

58. K. Kumar, A. Chou, C. Lin, P. Choudhury, and J. C. Lee, "Optimization of sub 3 nm gate dielectrics grown by rapid thermal oxidation in a nitric oxide ambient", Appl. Phys. Lett. 70 (3), 20 January 1997.

59. Prasenjit Chowdhury, Anthony I. Chou, Kiran Kumar, Chuan Lin and Jack C. Lee, "Improvement of Ultra-Thin Gate Oxide and Oxynitirde Integrity Using Fluorine Implantation Techniques," Applied Physics Letters 70 (1), January 6, 1997.

60. A. Chou, K. Lai, K. Kumar, P. Chowdhury and J. Lee, "Modeling of Stress-Induced Leakage Current in Ultra-Thin Oxide with the Trap Assisted Tunneling Mechanism," Applied Physics Lettes, vol. 70, no. 25, Pg. 3407, June 23, 1997.

61. Byoung Hun Lee, Yongjoo Jeon,Keith Zawadzki, Wen-Jie Qi and Jack C. Lee, "Effect of interfacial layer growth on the electrical characteristics of thin titanium oxide films on silicon", Appl. Phys. Lett. Vol. 74, p. 3143, 1999.

62. Tung-Sheng Chen, Venkatasubramani Balu, Shylaja Katakam, Jian-Hung Lee and Jack C. Lee, “Effects of Ir Electrodes on BST Thin Film Capacitors for High-Density Memory Application” IEEE Transactions on Electron Devices vol. 46, no. 12, p. 2304, Dec. 1999.

63. Jian-Hung Lee, Razak Mohammedali, Venkatasubramani Balu, Jeong Hee Han, Sundar Gopalan, Chun-Hui Wong and Jack C. Lee “The Niobium Doping Effects on Resistance Degradation of Strontium Titanate Thin Film Capacitors”, Applied Physics Letters, vol. 75, no. 10, p. 1455, September 6, 1999.

64. Sundar Gopalan, Chun-Hui Wong, Venkatasubramani Balu, Jian-Hung Lee, Jeong Hee Han, Razak Mohammedali, and Jack C. Lee, “Effects of Nb Doping on the Microstructure and Electrical Properties of Strontium Titanates Thin Films for Semiconductor Memory Applications”, Applied Physics Letters, vol. 75, no. 14, p. 2123, October 4, 1999.

65. T. Ngai, W. Qi, R. Sharma, J. Fretwell, X. Chen, J. Lee and S. Banerjee, “Electrical Properties of ZrO_2 Gate Dielectric on SiGe,” Applied Physics Letters, vol. 76, no. 4, p. 502, January 24, 2000.

66. Laegu Kang, Byoung Hun Lee, Wen-Jie Qi, Yongjoo Jeon, Renee Nieh, Sundar Gopalan, Katsunori Onishi, and Jack C. Lee,” Electrical Characteristics of Highly Reliable Ultra-Thin Hafnium Oxide Gate Dielectric,” IEEE Electron Dev. Lett., vol. 21, 4, p.181, 2000.

67. Byoung Hun Lee, Laegu Kang, Renee Nieh, Wen-Jie Qi, and Jack C. Lee, "Thermal stability and electrical characteristics of Hafnium oxide gate dielectric reoxidized with rapid thermal annealing", Appl. Phys. Lett., 76, p.1926, 2000.

68. A. Lucas, S. Gopalan, J. Lee, S. Kaushal, R. Niino and Y. Tada, “Ultrathin Gate Oxynitrides Grown Using Fast Ramp Vertical Furnace for Sub-130 Nanometer Technology,” Electrochemical and Solid-State Letters, vol. 3, no. 8, p. 389-391, August 2000.

69. Wen-Jie Qi, Renee Nieh, Easwar Dharmarajan, Byoung Hun Lee, Yongjoo Jeon, Laegu Kang, Katsunori Onishi, and Jack C. Lee, “Ultrathin zirconium silicate film with good thermal stability for alternative gate dielectric applications”, Appl. Phys. Lett., vol. 77, no.11, p. 1704-1706, Sept. 2000.

70. Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Laegu Kang, Yongjoo Jeon, Aaron Lucas, and Jack C. Lee, "Electrical and reliability characteristics of ZrO_2 deposited directly on Si for gate dielectric application", Appl. Phys. Lett., vol. 77, no. 20, p.3269, 2000.

71. T. Ngai, W.J. Qi, R. Sharma, J.L. Fretwell, X. Chen, J.C. Lee, and S.K. Banerjee, “Transconductance Improvement in Surface-Channel SiGe pMOSFETs using ZrO_2 Gate Dielectric,” Applied Physics Letters, May 14, 2001.

72. P.D. Kirsch, C. S. Kang, J. Lozano, J. C. Lee, J. G. Eckerdt, “Electrical and spectroscopic comparison of HfO2/Si interfaces on nitrided and un-nitrided Si (100),” Journal of Applied Physics, Volume 91, Number 7, pp. 1 – 11, 1 April 2002.

73. H. Cho, C. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, S. Krishnan and Jack Lee, “Structural and Electrical Properties of HfO_2 with Top Nitrogen Incorporated Layer,” IEEE Electron Device Letters, vol. 23, no. 5, p. 249, May 2002.

74. S. Gopalan, K. Onishi, R. Nieh, C. Kang, R. Choi, J. Cho, S. Krishnan, and J. Lee, “Electrical and Physical Characteristics of Ultrathin Hafnium Silicate Films with Polycrystalline Silicon and TaN Gates,” Applied Physics Letters, vol. 80, no. 23, p. 4416, June 10, 2002.

75. R. Nieh, R. Choi, S. Gopalan, K. Onishi, C. Kang, H. Cho, S. Krishnan and J. Lee, "Evaluation of Silicon Surface Nitridation Effects on Ultra-thin ZrO2 Gate Dielectrics," Applied Physics Letters, vol. 81, no. 9, p. 1663, August 26, 2002.

76. Chang Seok Kang, Hag-Ju Cho, Katsunori Onishi, Renee Nieh, Rino Choi, Sundar Gopalan, Sid Krishnan, Jeong H. Han, and Jack C. Lee, "Bonding states and electrical properties of ultrathin HfOxNy gate dielectrics", Appl. Phys. Lett. 81, p2593, September 30, 2002.

77. Chang Seok Kang, Katsunori Onishi, Laegu Kang, and Jack C. Lee, "Effects of Hf contamination on the properties of silicon oxide metal--oxide--semiconductor devices", Appl. Phys. Lett. 81, p5018, December 23, 2002.

78. Y. Kim, K. Onishi, C. Kang, H. Cho, R. Nieh, S. Gopalan, R. Choi, J. Han, S. Krishnan, and J. Lee, "Area Dependence of TDDB Characteristics for HfO_2 Gate Dielectrics," IEEE Electron Devices Letters, vol. 23, no. 10, p. 594, October 2002.

79. Y. Fan, R. Nieh, J. Lee, G. Lucovsky, G. Brown, F. Register and S. Banerjee, "Voltage and Temperature Dependent Gate Capacitance and Current Model: Application to ZrO2 n-channel MOS Capacitor," IEEE Tran. Electron Devices, vol. 49, no. 11, p. 1969, November 2002.

80. S. Mudanai, F. Li, S. Samavedam, R. Tobin, C. Kang, R. Nieh, L. Register, J. Lee, and S. Banerjee, "Interfacial Defect States in HfO2 and ZrO2 nMOS Capacitor," IEEE Electron Devices Letters, vol. 23, no. 12, p. 728, December 2002.

81. Y.H. Kim, K. Onishi, C. Kang, H. Cho, R. Choi, S. Krishnan, M. Akbar and J. Lee, "Thickness Dependence of Weibull Slopes of HfO_2 Gate Dielectrics," IEEE Electron Devices Letters, vol. 24, no. 1, p. 40, January 2003.

82. Z. Shi, D. Onsongo, K. Onishi, J. Lee, and S. Banerjee, "Mobility Enhancement in Surface Channel SiGe PMOSFETs With HfO_2 Gate Dielectrics," IEEE Electron Device Letter, vol. 24, no. 1, p. 34, January 2003.

83. K. Onishi, C. Kang, R. Choi, H. Cho, S. Gopalan, R. Nieh, S. Krishnan and J. Lee, "Improvement of Surface Carrier Mobility of HfO_2 MOSFET's by High-Temperature Forming Gas Annealing," IEEE Trans. On Electron Devices, vol. 50, no. 2, p. 384 – 390, February 2003.

84. R. Nieh, C. Kang, H. Cho, K. Onishi, R. Choi, S. Krishnan, J. Han, Y. Kim, A. Shahriar and J. Lee, "Electrical Characterization and Material Evaluation of Nitrogen Incorporated ZrO_2 (ZrO_xN_y) Gate Dielectric in TaN-gated NMOSFET's with High Temperature Forming Gas Annealing," IEEE Trans. On Electron Devices, vol. 50, no. 2, p. 333 – 340, February 2003.

85. Rino Choi, Katsunori Onishi, Chang Seok Kang, Hag-Ju Cho, Y.H. Kim, Siddharth Krishnan, M. S. Akbar and Jack C. Lee, " Effects of Deuterium Anneal on MOSFETs with HfO_2 Gate Dielectrics," IEEE Electron Device Letter, vol. 24, no. 3, p. 144, March 2003.

86. Katsunori Onishi, Chang Seok Kang, Rino Choi, Hag-Ju Cho, Young Hee Kim, Siddharth Krishnan, Mohammad Akbar, and Jack C. Lee, "Performance of polysilicon gate HfO_2 MOSFET's on (100) and (111) silicon substrates," IEEE Electron Device Letter, vol. 24, no. 4, p. 254, April 2003.

87. M.S. Akbar, S. Gopalan, H.-J. Cho, K. Onishi, R. Choi, C.S. Kang, Y.H. Kim, J. Han, S. Krishnan, and J. C. Lee, "High Performance TaN/HfSiON/Si MOSCAP and MOSFET Prepared by Low Thermal Budget NH_3 Post-Deposition Anneal," Applied Physics Letters, vol. 82, no.11, pp.1757, March 17 2003

88. K. Onishi, R. Choi, C. Kang, H. Cho, Y. Kim, R. Nieh, J. Han, S. Krishnan, M. Akbar, and J. Lee, "Bias-temperature Instabilities of Polysilicon Gate HfO_2 MOSFET's." IEEE Trans. On Electron Devices, vol. 50, no. 6, p. 1517, June 2003.

89. Chang Seok Kang, H.-J. Cho, R. Choi, K. Onishi, Y.H. Kim, M. S. Akbar, and J. C. Lee, "Characterization of resistivity and work function of sputtered-TaN film for gate electrode applications", Journal of Vacuum Science and Technology, vol. 21, issue #5, p. 2026, September/October 2003.

90. Y. H. Kim, and J. C. Lee, "Reliability Characteristics of high-k dielectrics" invited paper in the Microelectronics Reliability Journal, Volume 44, Issue 2, Pages 183-193, Feb. 2004.

91. Chang Seok Kang, Hag-Ju Cho, Rino Choi, Young-Hee Kim, Chang Yong Kang, Se Jong Rhee, Changhwan Choi, Mohammad Shahariar Akbar, and Jack C. Lee "The Electrical and Material Characterization of Hafnium Oxynitride Gate Dielectrics with TaN-Gate Electrode" IEEE Transactions on Electron Devices, Vol. 51, No. 2, P220-227, FEBRUARY 2004.

92. C.Y. Kang, Hag-Ju Cho, Rino Choi, Chang Seok Kang, Young Hee Kim, Se Jong Rhee, Chang Hwan Choi, Shahriar M. Akbar, and Jack C. Lee, "Effects of dielectric structure of HfO2 on carrier generation rate in Si substrate and channel mobility", App Phy. Lett., vol 84, 12, pp. 2148-2150, 2004.

93. R. Jha, J. Gurganos, Y. H. Kim, R. Choi, J. Lee and V. Misra, "A Capacitance Based Methodology for Extracting Workfunction of Metal Electrodes on High-K Dielectrics," IEEE Electron Device Letters, vol. 25, no. 6, p. 420, June 2004.

94. Rino Choi, Chang Seok Kang, Hag-Ju Cho, Young-Hee Kim, Mohammad S. Akbar, and Jack C. Lee "Effects of high temperature forming gas anneal on the characteristics

of MOSFET with HfO_2 gate stacks," Applied Physics Letter, Vol. 84, Issue 24, p4839-4841, June 14, 2004.

95. S. J. Rhee, C. Y. Kang, C. S. Kang, R. Choi, C. Choi, M. Akbar and J. Lee, "'Effect of Varying Interfacial Oxide and High-k Layer Thicknesses for HfO_2 Metal Oxide Semiconductor Field Effect Transistor" Applied Physics Letter, Vol. 85, p1286, 2004.

96. C.M. Osburn, S.A. Campbell, E. Eisenbraun, E. Garfunkel, T. Gustafson, A. Kingon, D.-L. Kwong, J. Lee, G. Lucovsky, T.P. Ma, J.P. Maria, V. Misra, G. Parsons, D. Schlom, and S. Stemmer, "Materials and Processes for High k Gate Stack", Semiconductor Fabtech Magazine, 2004.

97. Se Jong Rhee, Chang Yong Kang, Chang Seok Kang, Chang Hwan Choi, Rino Choi, Mohammad S. Akbar, and Jack C. Lee, "Threshold Voltage Instability Characteristics under Positive Dynamic Stress in Ultra Thin HfO_2 Metal Oxide Semiconductor Field Effect Transistors," Applied Physics Letters, vol. 85, no. 15, p. 3184, October 2004.

98. M. S Akbar, H. -J. Cho, R. Choi, C. S. Kang, C.Y. Kang, C. H. Choi, S. J. Rhee, Y. H. Kim and Jack C. Lee "Optimized NH_3 Annealing Process for High Quality HfSiON Gate Oxide", in IEEE Electron Device Letters, vol. 25 (7), pp. 465-467, 2004.

99. Akbar, M.S.; Moumen, N.; Barnett, J.; Lee, B.-H.; Lee, J.C, "Mobility Improvement after HCI Post-Deposition Cleaning of High-k Dielectric A Potential Issue in Wet Etching of Dual Metal Gate Process Technology," IEEE Electron Devices Letters, vol. 26, no. 3, p. 163, March 2005.

100. Rino Choi, Se Jong Rhee, Jack C. Lee, Byoung Hun Lee, Gennadi Bersuker, "Charge trapping and detrapping characteristics in high-k gate dielectric under static and dynamic stress," Electron Dev. Lett. vol 26 (3), p197, 2005.

101. M. S. Akbar, Naim Moumen, Joel Barnett, Johnny Sim and Jack C. Lee, "Effect of NH_3 surface nitridation temperature on mobility of ultrathin atomic layer deposited HfO_2", Appl. Phys. Lett. 86 (2005).

102. C. H. Choi, C.S. Kang, C.Y. Kang, S.J. Rhee, M.S. Akbar, S.A. Krishnan, M. Zhang, and Jack C. Lee, "Positive Bias Temperature Instability Effects of Hf-Based nMOFETs with Various Nitrogen and Silicon Profiles", IEEE Electron Device Letter (EDL), Vol., 26, No.1, p32, 2005.

103. Akbar, M.S.; Choi, C.H.; Rhee, S.J.; Krishnan, S.A.; Kang, C.Y.; Zhang, M.H.; Lee, T.; Ok, I.J.; Zhu, F.; Kim, H.-S.; Lee, J.C., "Electrical Performance and Reliability Improvement by Using Compositionally Varying Bi-Layer Structure of PVD HfSixOy Dielectric," IEEE Electron Devices Letters, vol. 26, no. 3, p. 166, March 2005.

104. Chang Yong Kang, Pat Lysaght, Rino Choi, Byoung Hun Lee, Chang Seok Kang, Se Jong Rhee, Chang Hwan Choi, Shahriar M. Akbar and Jack C.

Lee, “Nickel-Silicide Phase Effects on Flatband Voltage Shift and Equivalent Oxide Thickness Decrease of Hafnium Silicon Oxynitride Metal Silicon Oxide Capacitors,” Applied Physics Letter, vol. 86, article no. 222906, 2005.

105. Chang Yong Kang, Se Jong Rhee, Chang Hwan Choi, Chang Seok Kang, Rino Choi, Mohammad S. Akbar, Manhong Zang, Siddarth A. Krishnan and Jack C. Lee, “Effects of Nitrogen-Incorporated Interface Layer on the Transient Characteristics of Hafnium Oxide n-Metal Oxide Semiconductor Field Effect Transistors,” Applied Physics Letter, vol. 86, article no. 1236506, 2005.

106. Chang Yong Kang, Se Jong Rhee, Chang Hwan Choi, Shariar M. Abkar, Manhong Zhang, Taekhwi Lee, Injo Ok and Jack C. Lee, “Effects of Tantalum Penetration through Hafnium Oxide Layer on Carrier Generation Rate in Silicon Substrate and Carrier Mobility Degradation,” Applied Physics Letter, vol. 86, article no. 012901, 2005.

107. Changhwan Choi, Chang Yong Kang, Se Jong Rhee, Mohammad Shahariar Abkar, Siddarth A. Krishna, Manhong Zhang, Hyungseob Kim, Tackhwi Lee, Feng Zhu, Injo Ok, and Jack C. Lee, "Aggressively Scaled Ultra-Thin Undoped HfO2 Gate Dielectric (EOT < 0.7nm) with TaN Gate Electrode Using Engineered Interface Layer", IEEE Electron Device Letter (EDL), Vol., 26, No.7, p454, 2005.

108. Changhwan Choi, C.S. Kang, C.Y. Kang, S.J.Rhee, M.S. Akbar, S.A. Krishnan, M. Zhang, and Jack C. Lee, "Positive Bias Temperature Instability Effects of Hf-Based nMOFETs with Various Nitrogen and Silicon Profiles", IEEE Electron Device Letter (EDL), Vol., 26, No.1, p32, 2005.

109. Mohammad S. Akbar, Naim Moumen, Joel Barnett, Byoung Hun Lee, and Jack C. Lee, “Improvement in Bias Instabilities of MOCVD Hf-silicate by dilute HCl (500:1) Post-Deposition Rinsing and its effect after High Pressure H_2 Anneal”, in Appl. Phys. Lett. 87, 252903 (2005).

110. Chang Yong Kang, Pat Lysaght, Rino Choi, Byoung Hun Lee, Se Jong Rhee, Chang Hwan Choi, M. S. Akbar, and Jack C. Lee, "Nickel-silicide phase effects on flatband voltage shift and equivalent oxide thickness decrease of hafnium silicon oxynitride metal-silicon-oxide capacitors", Appl. Phys. Lett. 86, 222906 (2005).

111. M. S. Akbar, Naim Moumen, Jeff Peterson, Joel Barnett, Muhammad Hussain and Jack C Lee, “Effect of Precursor Pulse Time on Charge Trapping and Mobility of ALD HfO_2”, Electrochemical Society, 2005.

112. M. H. Zhang, S. J. Rhee, C. Y. Kang, C. H. Choi, M. S. Akbar, S. A. Krishnan, T. Lee, I. J. Ok, F. Zhu, H. S. Kim, and Jack C. Lee, “Improved electrical and material characteristics of HfTaO gate dielectrics with high crystallization temperature,” Applied Physics Letters, 87, 232901 (2005).

113. Se Jong Rhee, Chang Yong Kang, Chang Hwan Choi, Manhong Zhang, and Jack C. Lee, “Material and electrical analysis of hafnium titania bilayer dielectric metal-oxide-semiconductor field-effect transistors,” J. Vac. Sci. Technol. B 23, 2561 (2005).

114. Yanxia Lin, Mehmet C. Öztürk, Bei Chen, Se Jong Rhee, Jack C. Lee, and Veena Misra, ”Impact of Ge on integration of HfO_2 and metal gate electrodes on strained Si channels,” Appl. Phys. Lett. 87, 071903 (2005).

115. (Invited Paper) Se Jong Rhee and Jack C. Lee “Threshold voltage instability characteristics of HfO2 dielectrics n-MOSFETs” IEEE Microelectronic Reliability, 45, p1051-1060, 2005.

116. Feng Zhu, Se Jong Rhee, Chang Yong Kang, Chang Hwan Choi, Akbar, M.S., Krishnan, S.A., Manhong Zhang, Hyoung-Sub Kim, Tackwhi Lee, Ok, I., and J.C. Lee, "Improving channel carrier mobility and immunity to charge trapping of high-k NMOSFET by using stacked Y2O3/HfO2 gate dielectric" Volume 26, Issue 12, Dec. 2005.

117. S. J. Rhee, F. Zhu, H. S. Kim, C. H. Choi, C. Y. Kang, M. Zhang, T. Lee, I. Ok, S. Krishnan, and J. C. Lee, “Hafnium Titanate bilayer structure multimetal dielectric nMOSCAPs”, IEEE Electron Device Letters, vol. 27, issue. 4, p. 225, April 2006.

118. S. J. Rhee, F. Zhu, H. S. Kim, C. Y. Kang, C. H. Choi, M. Zhang, T. Lee, I. Ok, S. Krishnan, and J. C. Lee, “Systematic analysis of silicon oxynitride interfacial layer and its effects on electrical characteristics of high-*k* HfO_2 transistor,” Appl. Physics Letters, 88, 153515, 2006.

119. M. S. Akbar, Naim Moumen, Jeff Peterson, Joel Barnett, Muhammad Hussain and Jack C Lee, “Optimization of Precursor Time in Improving Bulk Trapping Properties of ALD HfO_2 Gate Stacks” Applied Physics Letter, vol. 88, article no. 082901, March 2006.

120. Siddarth A. Krishnan, Manuel Quevedo, Rusty Harris, Paul D. Kirsch, Rino Choi, Byoung Hun Lee, Gennadi Bersuker and Jack C. Lee, “NBTI Dependence on Dielectric Thickness and Nitrogen concentration in Ultra-scaled HfSiON Dielectric/ ALD-TiN Gate Stacks”, JJAP, Vol. 45, No. 4B, 2006.

121. M. S. Akbar, C. H. Choi, S. J. Rhee, S. Krishnan, C. Kang, M. H. Zhang, T. Lee, I. J. Ok, F. Zhu, H. –S. Kim, and Jack C. Lee, “Investigation of Transient Relaxation under Static and Dynamic Stress in Hf-based Gate Oxides”, IEEE Transaction in Electron Device Letters, vol. 53, no. 5, p. 1200-1207, May 2006.

122. C. Y. Kang, R. Choi, S. C. Song, C. D. Young, G. Bersuker, B. H. Lee and J. C. Lee, "Transient Bi-Carrier Response in High-k Dielectrics and its Impact on Transient Charge Effects in High-k Complementary Metal Oxide Semiconductor Devices" Applied Phys. Lett. 88, 162905 (2006).

123. M. H. Zhang, F. Zhu, T. Lee, H. S. Kim, I. J. Ok, G. Thareja, L.Yu, and Jack C. Lee "Fluorine passivation in poly-Si/TaN/HfO_2 through ion implantation", Applied Physics Letters, 89 (142909) 2006.

124. Injo Ok, Hyoung-sub Kim, Manhong Zhang, Chang-Yong Kang, Se Jong Rhee, Changhwan Choi, Siddarth A. Krishnan, Tackhwi Lee, Feng Zhu, Gaurav Thareja, and Jack C. Lee, "Metal Gate – HfO2 MOS Structures on GaAs Substrate with and without Si interlayer", IEEE Electron Device Letters, 27(3), pp. 145-147, March 2006.

125. Hyoung-sub Kim, Injo Ok, Manhong Zhang, Changhwan Choi, Tackhwi Lee, Feng Zhu, Gaurav Thareja, L. Yu and Jack C. Lee, "Ultrathin HfO2 (EOT= 1.1nm) MOS capacitors on n-GaAs substrate with germanium passivation," Applied Physics Letters, 88, p. 252906, 2006.

126. M. H. Zhang, I. J.Ok , H. S. Kim, F. Zhu, T. Lee, G. Thareja, L. Yu, and Jack C. Lee, "Electrical characteristics of sputter deposited $Hf_{1-x}Si_xO$/Si/GaAs gate stacks," Applied Physics Letters 89, p. 042902, 2006.

127. Feng Zhu, Chang Yong Kang, Se Jong Rhee, Chang Hwan Choi, Siddarth A. Krishnan, Manhong Zhang, Hyoung-Sub Kim, Taekhwi Lee, Injo Ok, Gaurav Thareja, and Jack C. Lee, "Mechanism of improved channel carrier mobility for stacked Y2O3 /HfO2 gate dielectric", Applied Physics Letters, 89, 257642, 2006.

128. Tackhwi Lee, Se Jong Rhee, Chang Yong Kang, Feng Zhu, Hyoung-sub Kim, Changhwan Choi, Injo Ok, Manhong Zhang, Siddarth Krishnan, Gaurav Thareja, and Jack C. Lee "Structural Advantage for the EOT Scaling and Improved Electron Channel Mobility by Incorporating Dysprosium Oxide (Dy2O3) Into HfO2 n-MOSFETs" IEEE Electron Device Letters, Vol. 27, No. 8, P.640-643, August 2006.

129. Hyoung-Sub Kim, Injo Ok, Manhong Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tasi, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee, "Depletion-mode GaAs metal-oxide-semiconductor field-effect transistor with HfO_2 dielectric and germanium interfacial passivation layer," *Appl. Phys. Lett.*, Vol. 89, pp. 222904, 2006.

130. Hyoung-Sub Kim, Injo Ok, Manhong Zhang, Tackhwi Lee, Feng Zhu, Lu Yu and Jack C. Lee, "Metal gate-HfO_2 metal-oxide-semiconductor capacitors on n-GaAs substrate with silicon/germanium interfacial passivation layers," *Appl. Phys. Lett.*, Vol. 89, pp. 222903, 2006.

131. G. Thareja, H. Wen, R. Harris, P. Majhi, B. Lee, and Jack Lee, "NMOS Compatible Workfunction of TaN Metal Gate with Gadolinium Oxide Buffer Layer on Hf-Based Dielectrics," IEEE Electron Devices Letters, vol. 27, no. 10, p. 802, October 2006.

132. M. S. Akbar and J. Lee, “A Novel Approach in Separating the Roles of Electrons and Holes in Degradation of Hf-based MOSFET Devices by Using Stress-Anneal Technique,” IEEE Electron Devices Letters, vol. 28, no. 2, February 2007.

133. J. Lee (Invited Paper) "MOSCAP's and MOSFET's on III-V Channel Materials with Si, Ge and SiGe Interface Passivation Layer", Electrochemical Society Transactions, Volume 6, "Silicon Nitride, Silicon Dioxide, and Emerging Dielectrics 9", April 2007.

134. M. S. Akbar, C. H. Choi, S. J. Rhee, S. Krishnan, C. Kang, M. H. Zhang, T. Lee, I. J. Ok, F. Zhu, H. –S. Kim, and Jack C. Lee, “A Novel Approach in Separating the roles of Electrons and Holes in causing Degradation in Hf-based MOSFET Devices by using Stress-Anneal Technique”, in IEEE Electron Device Letter, vol. 28 (2), pp.132-134, 2007.

135. Feng Zhu, S. Koveshnikov, I. Ok, H.S. Kim, V. Tokranov, M. Yakimov, S. Oktyabrsky, M. Zhang, T. Lee, G. Thareja, L. Yu, W. Tsai and J. C. Lee, “Depletion-mode GaAs metal-oxide-semiconductor field-effect transistor with amorphous silicon interface passivation layer and thin HfO2 gate oxide,” Applied Physics Letters, 91, 043507 (2007).

136. Hyoung-Sub Kim, Injo Ok, Manhong Zhang, F. Zhu, S. Park, J. Yum, Han Zhao, and Jack C. Lee, “Gate oxide scaling down in HfO_2-GaAs metal-oxide-semiconductor capacitor using germanium interfacial passivation layer,” *Appl. Phys. Lett.*, Vol. 91, pp. 042904, 2007.

137. M. H. Zhang, M. Oye, B. Cobb, F. Zhu, H. S. Kim, I. J. Ok, J. Hurst, S. Lewis, A. Holmes, J. C. Lee, S. Koveshnikov, W. Tsai, M. Yakimov, V. Torkanov, S. Oktyabrsky, “Importance of controlling oxygen incorporation into HfO_2/Si/n-GaAs gate stacks” *J. Appl. Phys*. . 101, 034103 (2007).

138. Sachin Joshi, Cristiano Krug, Dawei Heh, Hoon Joo Na, Harlan R Harris, Jung Woo Oh, Paul D. Kirsch, Prashant Majhi, Byoung Hun Lee, Hsing-Huang Tseng, Raj Jammy, Jack C. Lee and Sanjay K. Banerjee, “Improved Ge Surface Passivation with Ultrathin SiO_X Enabling High Mobility Surface Channel PMOSFETs Featuring a HfSiO/WN gate stack,” Electron Devices Letters, vol. 28, p. 308, April 2007.

139. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao and Jack C. Lee, “Temperature Effects of Si Interface Passivation Layer Deposition on High-k III-V Metal–Oxide–Semiconductor Characteristics.” Applied physics letters, 91, 2007.

140. Han Zhao, Hyoung-Sub Kim, Feng Zhu, Manhong Zhang, Injo OK, Sung Il Park, Jung Hwan Yum and Jack C Lee, “Metal-oxide-semiconductor capacitors on GaAs with germanium nitride passivation layer”, Applied Physics Letters, 91, 172101, (2007)

141. Sung Il Park, InJo Ok, Hyoung-sub Kim, Feng Zhu, Manhong Zhang, Jung Hwan Yum, Zhao Han, and Jack C. Lee, “Optimization of electrical characteristics of TiO2-

incorporated HfO2 n-type doped gallium arsenide metal oxide semiconductor capacitor with silicon interface passivation layer", in Applied Physics Letters 91, 081908(2007).

142. Feng Zhu, S. Koveshnikov, I. Ok, H.S. Kim, M. Zhang, T. Lee, G. Thareja, L. Yu, V. Tokranov, M. Yakimov, and S. Oktyabrsky, W. Tsai and J. C. Lee, "Depletion-mode GaAs N-MOSFETs with amorphous silicon interface passivation layer and thin HfO_2 gate oxide," Applied Physics Letters, 91, 043507 (2007)

143. M. H. Zhang, F. Zhu, H. S. Kim, I. J. Ok and Jack C. Lee, "Fluorine passivation in gate stacks of poly-Si/TaN/HfO_2 (and HfSiON/HfO_2)/Si through gate ion implantation", IEEE Electron Device Letters, 28, 195 (2007).

144. Hyoung-Sub Kim, Injo Ok, Manhong Zhang, F. Zhu, S. Park, J. Yum, Han Zhao, and Jack C. Lee, "Gate oxide scaling down in HfO_2-GaAs metal-oxide-semiconductor capacitor using germanium interfacial passivation layer," Appl. Phys. Lett., Vol. 91, pp. 042904, (2007).

145. Han Zhao, Hyoung-Sub Kim, Feng Zhu, Manhong Zhang, Injo OK, Sung Il Park, Jung Hwan Yum, and Jack C. Lee, "Metal-oxide-semiconductor capacitors on GaAs with germanium nitride passivation layer", Applied Physics Letters, 91, 172101 (2007)

146. Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, J. Oh, P. Majhi, and Jack C. Lee, "Flatband voltage instability characteristics of HfO_2-based GaAs metal-oxide-semiconductor capacitors with a thin Ge layer," Appl. Phys. Lett., Vol. 92, pp. 102904, (2008).

147. Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, J. Oh, P. Majhi, and Jack C. Lee, "Inversion-type enhancement-mode HfO_2-based GaAs metal-oxide-semiconductor field effect transistors with a thin Ge layer," Appl. Phys. Lett., Vol. 92, pp. 032907, (2008).

148. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, N. Goel and W. Tsai, C. K. Gaspe, M.B. Santos, and Jack C. Lee, "Metal gate: HfO_2 metal-oxide-semiconductor structures on high-indium-content InGaAs substrate using physical vapor deposition." Appl. Phys. Lett. 92, 112904 (2008).

149. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, and Jack C. Lee, "Influence of the substrate orientation on the electrical and material properties of GaAs metal-oxide-semiconductor (MOS) Capacitors and self-aligned transistors using HfO_2 and silicon interface passivation layer (IPL)" Appl. Phys. Lett. 92, 1 (2008)

150. InJo Ok , H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, N. Goel and W. Tsai, C.K. Gaspe, M.B. Santos, and Jack C. Lee, "Self-aligned n-channel metal-oxide-semiconductor field effect transistor on high-indium-

content $In_{0.53}Ga_{0.47}As$ and InP using physical vapor deposition HfO_2 and silicon interface passivation Layer." Appl. Phys. Lett. 92, 202903 (2008)

151. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao and Jack C. Lee, "Self-aligned n- channel GaAs metal–oxide–semiconductor field-effect transistors (MOSFETs) Using HfO_2 and silicon interface passivation layer: post metal annealing optimization." Microelectronics Engineering (2008).

152. Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, P. Majhi, N. Goel, W. Tsai, C. K. Gaspe, M. B. Santos, and Jack C. Lee, "A study of Metal-Oxide-Semiconductor Capacitors on GaAs, In0.53Ga0.47As, InAs, and InSb Substrates using a Germanium Interfacial Passivation Layer," Appl. Phys. Lett., (2008).

153. K. T. Lee, C. Y. Kang, B. S. Ju, R. Choi, K. S. Min, O. S. Yoo, B. H. Lee, R. Jammy, J.C. Lee, H. D. Lee, Y.H. Jeong, "Effects of In Situ O2 Plasma Treatment on off-State Leakage and Reliability in Metal-Gate/High- k Dielectric MOSFETs", IEEE Electron Device Letters, vol. 29, pp. 565, Jun. 2008.

154. Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, P. Majhi, and Jack C. Lee, "HfO_2-based InP n-channel metal-oxide-semiconductor field-effect transistors and metal-oxide-semiconductor capacitors using a germanium interfacial passivation layer," Appl. Phys. Lett., 93, 102906 (2008)

155. Han Zhao, Davood Shahrjerdi, Feng Zhu, Manhong Zhang, Hyoung-Sub Kim, Injo OK, Jung Hwan Yum, Sung Il Park, Sanjay K. Banerjee, and Jack C. Lee, "Gate-first inversion-type InP metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al_2O_3 gate dielectric", Applied Physics Letters, 92, 233508 (2008)

156. Han Zhao, Davood Shahrjerdi, Feng Zhu, Hyoung-Sub Kim, Injo OK, Manghong Zhang, Jung Hwan Yum, Sanjay K. Banerjee, and Jack C. Lee, "Inversion-type indium phosphide metal-oxide-semiconductor field-effect transistors with equivalent oxide thickness of 12 Å using stacked $HfAlO_x/HfO_2$ gate dielectric", Applied Physics Letters, 92, 253506 (2008)

157. Han Zhao, Davood Shahrjerdi, Feng Zhu, Hyoung-Sub Kim, Injo OK, Manhong Zhang, Jung Hwan Yum, Sanjay K. Banerjee and Jack C Lee, "Inversion-type InP MOSFETs with EOT of 21 Å using atomic layer deposited Al_2O_3 gate dielectric", Electrochemical and solid-state letters, 11, H233, (2008)

158. Han Zhao, Yen-Ting Chen, Jung Hwan Yum, Niti Goel, Jack C Lee, "Effect of channel doping concentration and thickness on device performance for $In_{0.53}Ga_{0.47}As$ MOS transistors with atomic-layer-deposited Al_2O_3 dielectrics", Applied Physics Letters, 94, 093505 (2009)

159. Han Zhao, Yen-Ting Chen, Jung Hwan Yum, Yanzhen Wang, Niti Goel, Jack C Lee, "High performance $In_{0.7}Ga_{0.3}As$ metal-oxide-semiconductor transistors with mobility > 4400 cm^2/Vs using InP barrier layer", Applied Physics Letters, 94, 193502 (2009)

160. Han Zhao, Jung Hwan Yum, Yen-Ting Chen, and Jack C Lee, "$In_{0.53}Ga_{0.47}As$ n-MOSFETs with ALD Al_2O_3, HfO_2 and $LaAlO_3$ gate dielectrics", Journal of Vacuum Science and Technology B, 27, 2024, (2009)

161. Feng Zhu, Han Zhao, I. Ok, H.S. Kim, M. Zhang, S. Park, J. Yum, Niti Goel, C.K. Gaspe, M.B. Santos, W. Tsai and Jack C. Lee, "Effects of anneal and silicon interface passivation layer thickness on device characteristics of $In_{0.53}Ga_{0.47}As$ n-MOSFETs with HfO_2 gate oxide", Electrochemical and Solid-State Letters, 12, H131 (2009)

162. Feng Zhu, Han Zhao, I. Ok, H.S. Kim, J. Yum, Niti Goel, C.K. Gaspe, M.B. Santos, W. Tsai, and Jack C. Lee, "A high performance $In_{0.53}Ga_{0.47}As$ Metal-Oxide-Semiconductor Field Effect Transistor with silicon interface passivation layer", Applied Physics Letters, 94, 013511 (2009)

163. Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, and Jack C. Lee, "Metal-oxide-semiconductor field-effect-transistors on indium phosphide using HfO_2 and silicon passivation layer with equivalent oxide thickness of 18Å", APPLIED PHYSICS LETTERS 94, 213505, May 2009

164. Han Zhao, Yen-Ting Chen, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, Jack Lee, "High Performance InGaAs MOSFETs with High Mobility using InP Barrier Layer", Electrochemical Society Transactions, Vol. 25, Issue #7, p. 397-404 (2009)

165. H Zhao, J. Lee, et al, "Effects of gate-first and gate-last process on interface quality of $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors using atomic-layer-deposited Al_2O_3 and HfO_2 oxides", Applied Physics Letters, 95, 253501 (2009)

166. Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee "Improved electrical characteristics of TaN/Al2O3 / In0.53Ga0.47As metal-oxide-semiconductor field-effect transistors by fluorine incorporation", APPLIED PHYSICS LETTERS 95, 013501 (2009)

167. Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Effects of fluorine incorporation on the electrical properties of atomic-layer-deposited Al2O3 gate dielectric on InP substrate", Journal of The Electrochemical Society, 157 (3) G71-G75 January (2010)

168. Yen-Ting Chen, Han Zhao, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Fluorinated HfO2 gate dielectric engineering on In0.53Ga0.47As metal-oxide-semiconductor field-effect-transistors, APPLIED PHYSICS LETTERS 96, 103506, March (2010)

169. Yen-Ting Chen, Han Zhao, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Effects of fluorine incorporation into HfO2 gate dielectrics on InP and In0.53Ga0.47As metal-oxide-semiconductor field-effect-transistors," APPLIED PHYSICS LETTERS 96, 253502 (2010).

170. H Zhao, J. Lee, et al, "Effects of barrier layers on device performance of high mobility $In_{0.7}Ga_{0.3}As$ quantum-well metal-oxide-semiconductor field-effect-transistors", Applied Physics Letters, 96, 102101 (2010).

171. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee, "Scaling Properties of $In_{0.7}Ga_{0.3}As$ buried-channel MOSFETs with atomic layer deposited gate dielectric", Electronics Letters, vol. 46, no. 25 (2010).

172. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee, "Investigation of surface channel InGaAs MOSFETs with Al2O3 and ZrO2 ALD Gate Dielectric", Electrochemical Society Transactions 33 (3), 479 (2010).

173. C. Choi, J. Lee, "Scaling equivalent oxide thickness with flat band voltage (V_{FB}) modulation using *in situ* Ti and Hf interposed in a metal/high-*k* gate stack," Journal of Applied Physics, vol. 108, no. 1, 2010.

174. M.S. Park, K. T. Lee, C. Y. Kang, G. B. Choi, H.C. Sagong, C. W. Sohn, B. G. Min, J. Oh, P. Majhi, H. Tseng, J. Lee, J. S. Lee, R. Jammy, Y. H. Jeong, "The Effect of a Si Capping Layer on RF Characteristics of High-k/Metal Gate SiGe Channel pMOSFETs," IEEE Electron Device Letters, vol. 31, no. 10, p. 1104-1106, Oct. 2010.

175. Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Fei Xue, and Jack C Lee, "$In_{0.7}Ga_{0.3}As$ tunneling field-effect-transistors with a I_{on} of 50 mA/mm and a subthreshold swing of 86 mV/dec using HfO_2 gate oxide", Electron Device Letters, 31, 1392, (2010).

176. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee ,"InAs inserted InGaAs buried channel metal-oxide-semiconductor field-effect-transistors with atomic-layer-deposited gate dielectric ", Appl. Phys. Lett. 98, 082106 (2011).

177. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack C. Lee, "Effect of indium concentration on InGaAs channel metal-oxide-semiconductor field-effect transistors with atomic layer deposited gate dielectric", J. Vac. Sci. Technol. B 29, 040601 (2011).

178. Yen-Ting Chen, Han Zhao, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "ZrO2-based InP MOSFETs (EOT=1.2nm) Using Various Interfacial Dielectric Layers" Electrochemical Society Transactions 35(3), 375, May (2011).

179. Y. Wang, Y. Chen, H. Zhao, F. Xue, F. Zhou, and J. Lee, "Impact of SF_6 plasma treatment on performance of TaN-HfO_2-InP metal-oxide-semiconductor field-effect transistor ", Applied Physics Letters, 98, 043506, (2011).

180. Y. Wang, Y. Chen, H. Zhao, F. Xue, F. Zhou, and J. Lee, "Improved electrical properties of HfO_2-based gate dielectrics on InP substrate using Al_2O_3/HfO_2 and SF_6 plasma treatment", Electrochemical Solid-state Letters, 14, H291 (2011).

181. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack C. Lee, "High-k InGaAs metal-oxide-semiconductor field-effect-transistors with various barrier layer materials" Appl. Phys. Lett. Vol. 99, issue 3, p. 033507 - 033507-3, July 2011.

182. Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Fei Xue, and Jack C. Lee, "Improving the on-current of $In_{0.7}Ga_{0.3}As$ tunneling field-effect-transistors by p^{++}/n^{+} tunneling junction", Applied physics letters, 98, 093501, (2011).

183. Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Fei Xue, and Jack C. Lee, "InGaAs tunneling field-effect-transistors with atomic-layer-deposited gate oxides", IEEE Transactions on Electron Devices, vol. 58, no. 9, p. 2990-2995, Sept. 2011.

184. H. C. Sagong, C. Y. Kang, C. W. Sohn, K. Jeon, D. Choi, C-K Baek, J-S Lee, J. Lee and Y. Jeong, "Comprehensive Study of Quasi-Ballistic Transport in High-K/Metal Gate nMOSFETs," IEEE Electron Device Letters, vol. 31, no. 11, p. 1424, Nov. 2011.

185. Y. Chen, Y. Wang, F. Xue, F. Zhou, J. Lee, "Application of Post-HfO_2 Fluorine Plasma Treatment for Improvement of $In_{0.53}Ga_{0.47}As$ MOSFET Performance," IEEE Electron Device Letters, vol. 31, no. 11, p. 1531, Nov. 2011.

186. J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "Atomic layer deposited beryllium oxide: Effective passivation layer for III-V metal/oxide/semiconductor devices," Journal of Applied Physics, vol. 109, 064101 (2011).

187. J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, J. C. Lee and S. K. Banerjee, "Inversion Type InP Metal Oxide Semiconductor Field Effect Transistor Using Novel Atomic Layer Deposited BeO Gate Dielectric," Applied Physics Letters, 99, 033502 (2011).

188. J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, J. C. Lee and S. K. Banerjee, "Comparison of Self Cleaning Effect and Electrical Characteristics between Atomic Layer Deposited BeO and Al_2O_3 as an Interface Passivation Layer on GaAs MOS Devices," Journal of Vacuum Science and Technology, vol. 29, issue 6, p. 061501-6, Nov. 2011.

189. Yum J. H.; Akyol T.; Lei M.; Ferrer, D. A. Hudnall, Todd. W., Downer, M, Bielawski, C. W. Bersuker, G. Lee, J. C.; Banerjee, S. K., "A study of highly crystalline novel beryllium oxide film using atomic layer deposition ," Journal of Crystal Growth, vol. 334, issue 1, p. 126-133, Nov. 2011.

190. Jung Hwan Yum, Gennadi Bersuker, Tarik Akyol, D. A. Ferrer, Ming Lei, Keun Woo Park, Todd W. Hudnall, Mike C. Downer, Christopher W. Bielawski, Edward T. Yu, Jimmy Price, Jack C. Lee and Sanjay K. Banerjee, *"Epitaxial ALD BeO: Efficient Oxygen Diffusion Barrier for EOT Scaling and Reliability Improvement*," IEEE Transaction on Electron Devices, vol. 58, issue 12, p. 4384-4392, Dec. 2011.

191. Yanzhen Wang, Yen-Ting Chen, Fei Xue, Fei Zhou, and Jack C. Lee, "HfO_2 dielectrics engineering using low power SF_6 plasma on InP and $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistors", Applied Physics Letters, 100, 243508 (2012).

192. Yanzhen Wang, Yen-Ting Chen, Fei Xue, Fei Zhou, and Jack C. Lee, "Effects of SF_6 plasma treatment on electrical characteristics of TaN-Al_2O_3-InP metal-oxide-semiconductor field-effect transistor", Applied Physics Letters, 101, 063505 (2012).

193. Yanzhen Wang, Yen-Ting Chen, Fei Xue, Fei Zhou, Yao-Feng Chang, and Jack C. Lee, "MOSFETs on InP substrate with $LaAlO_3/HfO_2$ bilayer of different $LaAlO_3$ thickness and single $La_xAl_{1-x}O$ layer with different La doping level", Electrochemical Society Transactions, 50 (2012).

194. Yanzhen Wang, Burt Fowler, Yen-Ting Chen, Fei Xue, Fei Zhou, Yao-Feng Chang, and Jack C. Lee, "Effect of hydrogen/deuterium incorporation on electroforming voltage of SiO_x resistive random access memory", Applied Physics Letters, 101, 183505 (2012).

195. Yanzhen Wang, Yen-Ting Chen, Fei Xue, Fei Zhou, Yao-Feng Chang, Burt Fowler, and Jack C. Lee, "Memory switching properties of e-beam evaporated SiO_x on N++ Si substrate" Applied Physics Letters, 100, 083502 (2012).

196. Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Physical and Electrical Analysis of Post-HfO2 Fluorine Plasma Treatment for Improvement of In0.53Ga0.47As MOSFETs Performance", IEEE Trans. Electron Devices Vol. 59, No., 139, 2012.

197. Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Optimization of Fluorine Plasma Treatment for Interface Improvement on HfO2/In0.53Ga0.47As MOSFETs", Special Issue (Organo-Fluorine Chemical Science) of Appl. Sci. Vol. 2(1), 233, 2012 (Invited).

198. L. Morassi, G. Verzellesi, H. Zhao, J.C. Lee, D. Veksler, G. Bersuker, "Errors Limiting Split-CV Mobility Extraction Accuracy in Buried-Channel InGaAs MOSFETs", IEEE Transactions on Electron Devices, vol. 59(4), pp. 1068-1075, Apr. 2012.

199. M. Hanna, H. Zhao and J. Lee, “Poole Frenkel current and Schottky emission in SiN gate dielectric in AlGaN/GaN metal insulator semiconductor heterostructure field effect transistors,” Appl. Phys. Lett. 101, 153504 (2012).

200. L. Morassi, G. Verzellesi, H. Zhao, J.C. Lee, D. Veksler, G. Bersuker, “Engineering barrier and buffer layers in InGaAs quantum-well MOSFETs”, IEEE Transactions on Electron Devices, vol. 59, no. 12, p. 3651-3654, 2012.

201. Yao-Feng Chang, Yen-Ting Chen, Fei Xue, Yanzhen Wang, Fei Zhou, Burt Fowler, and Jack C. Lee, “Study of polarity effect in SiOx-based resistive switching memory”, Appl. Phys. Lett., 101, 052111 (2012).

202. Yao-Feng Chang, Pai-Yu Chen, Burt Fowler, Yen-Ting Chen, Fei Xue, Yanzhen Wang, Fei Zhou, and Jack C. Lee, “Understanding the resistive switching characteristics and mechanism in active SiOx-based resistive switching memory”, J. Appl. Phys., 112, 123702 (2012).

203. Fei Xue, Aiting Jiang, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee, “Channel Thickness Dependence of InGaAs Quantum-Well Field-Effect Transistors with High-κ Gate Dielectrics,” *IEEE Electron Device Lett*., Vol. 33, No. 9, 1255 (2012).

204. Fei Xue, Aiting Jiang, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee, “Sub-50nm In0.7Ga0.3As MOSFETs with various barrier layer materials”, *IEEE Electron Device Lett*. Vol. 33, No. 1, 32 (2012).

205. Fei Xue, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Yao-Feng Chang, Burt Fowler and Jack Lee, “ The Effect of Plasma Treatment on Reducing Electroforming Voltage of Silicon Oxide RRAM”, Electrochemical Society Transactions, vol. 45, No. 6,245 (2012).

206. Yen-Ting Chen, Burt Fowler, Yanzhen Wang, Fei Xue, Fei Zhou, Yao-Feng Chang, Pai-Yu Chen, and Jack C. Lee, “Tristate Operation in Resistive Switching of SiO2 Thin Films,” IEEE Electron Devices Letters, VOL. 33, NO. 12, p. 1702, December 2012.

207. Yen-Ting Chen, Burt Fowler, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Random process of filamentary growth and localized switching mechanism in resistive switching of SiOx thin films", ECS Journal of Solid State Science and Technology 1 (3) P1-P4 (2012).

208. Chang-Woo Sohn, Chang Yong Kang, Myung-Dong Ko, , Do-Young Choi, Hyun Chul Sagong, Eui-Young Jeong, Chan-Hoon Park, Sang-Hyun Lee, Ye-Ram Kim, Chang-Ki Baek, Jeong-Soo Lee, Jack C. Lee, and Yoon-Ha Jeong, “Analytical Model of S/D Series Resistance in Trigate FinFETs with Polygonal Epitaxy”, IEEE Transactions on Electron Devices, vol. 60, issue 4, p.1302-1309, April 2013.

209. Yen-Ting Chen, Burt Fowler, Yao-Feng Chang, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, “Reduced electroforming voltage and enhanced programming stability in resistive switching of SiO_2 thin film”, ECS Solid State Letters, 2(5) N18, 2013.

210. Yao-Feng Chang, P. Y. Chen, Fei Zhou, Fei Xue, Burt Fowler, Edward T. Yu, and Jack C. Lee, “Investigation of edge- and bulk-related resistive switching behaviors and backward-scan effects in SiO_x-based resistive switching memory”, Appl. Phys. Lett., 103, 193508 (2013).

211. Yao-Feng Chang, Li Ji, Zhuo-Jie Wu, Fei Zhou, Yanzhen Wang, Fei Xue, Burt Fowler, Edward T. Yu, Paul S. Ho, and Jack C. Lee, “Oxygen-induced bi-modal failure phenomenon in SiOx-based resistive switching memory”, Appl. Phys. Lett., 103, 033521 (2013).

212. Li Ji, Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Tsung-Ming Tsai, Kuan-Chang Chang, Min-Chen Chen, Ting-Chang Chang, Simon M. Sze, Edward T. Yu and Jack C. Lee, “Integrated One Diode–One Resistor Architecture in Nanopillar SiOx Resistive Switching Memory by Nanosphere Lithography”, Nano Lett., 14 p. 813, (2014).

213. Fei Xue, Aiting Jiang, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Yao-Feng Chang and Jack Lee, “Non-planar InGaAs Gate-Wrapped-Around Field-Effective-Transistors,” IEEE Transactions on Electron Devices, vol. 61, issue 7, p. 2332, July 2014.

214. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Intrinsic SiOx-based unipolar resistive switching memory Part I: Oxide stoichiometry effects on reversible switching and program window optimization" J. Appl. Phys. 116, 043708 (2014).

215. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Intrinsic SiOx-based unipolar resistive switching memory Part II: Thermal effects on charge transport and characterization of multilevel programing" J. Appl. Phys. 116, 043709 (2014).

216. (Highlighted as News & Views in the same issue) Li Ji, Martin D. McDaniel, Shijun Wang, Agham B. Posadas, Xiaohan Li, Haiyu Huang, Jack C. Lee, Alexander A. Demkov, John G. Ekerdt, Allen J. Bard and Edward T. Yu, "A Silicon-based photocathode for water reduction with an expitaxial SrTiO3 protection layer and a nanostructured catalyst", Nature Nanotechnology, Vol 10, (2015), p 84-90.

217. Fei Zhou, Yao-Feng Chang, Yanzhen Wang, Ying-Chen Chen, Fei Xue, Burt Fowler, and Jack C. Lee, "Discussion on device structures and SU-8 encapsulation for SiO_x random access memory operation in air", *Appl. Phys. Lett.*, 105, 163506 (2014).

218. Fei Zhou, Yao-Feng Chang, Kwangsub Byun, Burt Fowler, and Jack C. Lee, "Characterization of external resistance effect and performance optimization in unipolar-type SiO_x-based resistive switching memory", *Appl. Phys. Lett.*, 105, 133501 (2014).

219. Burt W. Fowler, Yao-Feng Chang, Fei Zhou, Yanzhen Wang, Pai-Yu Chen, Fei Xue, Yen-Ting Chen, Brad Bringhurst, Scott Pozder, and Jack C. Lee, "Recent Progress on Understanding Electroforming and Resistive Switching in Silicon Dioxide Resistive Memory Devices" RSC advances 5, 21215 (2015).

220. Fei Zhou, Yao-Feng Chang, Kwangsub Byun, Burt Fowler, Jack C. Lee, "Stabilization of Multiple Resistance Levels by Current-Sweep in SiO_x-based Resistive Switching Memory" *Appl. Phys. Lett.*, 106, 063508 (2015).

221. Yao-Feng Chang, Burt Fowler, Fei Zhou, and Jack C. Lee, "The Intrinsic Unipolar SiOx-based Resistive Switching Memory: Characterization, Mechanism and Applications" ECS Transactions 69 (5), 149-164 (2015).

222. Fei Zhou, Lauren Guckert, Yao-Feng Chang, Earl Swartzlander, and Jack C. Lee, "Bidirectional Voltage Biased Implication Operations Using SiO_x Based Unipolar Memristors" Applied Physics Letters, 107 (18), 183501 (2015).

223. Fei Zhou, Yao-Feng Chang, Ying-Chen Chen, Xiaohan Wu, Ye Zhang, Burt Fowler and Jack C. Lee, "A Study of Interfacial Resistive Switching Mechanism by Proton Exchange Reactions on SiOx layer" Physical Chemistry Chemical Physics, 18, 700 - 703 (2016).

224. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou and Jack C. Lee, "Study of self-compliance behaviors and internal filament characteristics in intrinsic SiOx-based resistive switching memory," Applied Physics Letters, 2016.

225. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, Simon M. Sze, and Jack C. Lee, "A Synaptic Device Built in One Diode-One Resistor (1D-1R) Architecture with Intrinsic SiO_x-based Resistive Switching Memory", Nano Devices and Sensors, ISBN: 978-1-5015-0153-1, (2016).

226. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Xiaohan Wu, Yen-Ting Chen, Yanzhen Wang, Fei Xue, and Jack C. Lee, "Resistive Switching Characteristics and Mechanisms in Silicon Oxide Memory Devices", Nano Devices and Sensors, ISBN: 978-1-5015-0153-1, (2016).

227. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Chih-Hung Pan, Ting-Chang Chang and Jack C. Lee, "Demonstration of Synaptic Behaviors and Resistive Switching Characterizations by Proton Exchange Reactions in Silicon Oxide" Scientific Reports, 6, 21268 (2016). (doi: 10.1038/srep21268)

228. Yao-Feng Chang,Burt Fowler, Ying-Chen Chen and Jack C. Lee, “Proton exchange reactions in SiO x-based resistive switching memory: Review and insights from impedance spectroscopy” Progress in Solid State Chemistry, 1-11 (2016).

229. Ying-Chen Chen, Yao-Feng Chang, Xiaohan Wu, Meiqi Guo, Fei Zhou, Burt Fowler, and Jack C. Lee, "Characterization of SiOx/HfOx bilayer Resistive-Switching Memory Devices" ECS Transaction *72(2): 25-33; doi:10.1149/07202.0025ecst* (2016).

230. Y.F. Chang, B. Fowler, F. Zhou, Y.C. Chen, J.C. Lee, “Study of self-compliance behaviors and internal filament characteristics in intrinsic SiOx-based resistive switching memory,” *Applied Physics Letters*, 108, 033504 (2016).

231. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, Simon M. Sze, and Jack C. Lee, "A Synaptic Device Built in One Diode-One Resistor (1D-1R) Architecture with Intrinsic SiO_x-based Resistive Switching Memory", Physical Sciences Reviews (2016).

232. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Xiaohan Wu, Yen-Ting Chen, Yanzhen Wang, Fei Xue, and Jack C. Lee, "Resistive Switching Characteristics and Mechanisms in Silicon Oxide Memory Devices", Physical Sciences Reviews, DOI: 10.1515/psr-2016-0011, 2016.

233. Li Ji, Hsien-Yi Hsu, Xiaohan Li, Kai Huang, Ye Zhang, Jack C. Lee, Allen J. Bard and Edward T. Yu, “Localized dielectric breakdown and antireflection coating in metal–oxide–semiconductor photoelectrodes,” Nature Materials, 07 November 2016/ DOI 10.1038/nmat4801.

234. Y.-C. Chen, Y. F. Chang, CY Lin, X Wu, G Xu, B Fowler, TC Chang, JC Lee, “Built-in Nonlinear Characteristics of Low Power Operating One-Resistor Selector-Less RRAM By Stacking Engineering”, ECS Transactions 80 (10), 923-931 (2017).

235. Ying-Chen Chen, Yao-Feng Chang, Xiaohan Wu, Fei Zhou, Meiqi Guo, Chih-Yang Lin, Cheng-Chih Hsieh, Burt Fowler, Ting-Chang Chang, and Jack C. Lee, “Dynamic Conductance Characteristics in HfOx-based Resistive Random-Access Memory,” Royal Society of Chemistry Advances, vol. 7, issue 21 (2017).

236. Yao-Feng Chang, Fei Zhou, Burt W. Fowler, Ying-Chen Chen, Cheng-Chih Hsieh, Lauren Guckert, Earl E. Swartzlander, Jack C. Lee, "Memcomputing (Memristor + Computing) in Intrinsic SiOx-Based Resistive Switching Memory: Arithmetic Operations for Logic Applications," IEEE Transactions on Electron Devices, 64 (7), 2977-2983 (2017).

237. Meiqi Guo, Ying-Chen Chen, Chih-Yang Lin, Yao-Feng Chang, Burt Fowler, Q. Q. Li, Jack C. Lee, Y. G. Zhao, “Unidirectional Threshold Resistive Switching in Au/NiO/Nb: $SrTiO_3$ Devices,” Applied Physics Letters, vol. 110, issue 23, no. 233504, June 2017.

238. (Front Cover) Li Ji, Hsien-Yi Hsu, Xiaohan Li, Kai Huang, Ye Zhang, Jack C. Lee, Allen J. Bard and Edward T. Yu, "Localized dielectric breakdown and antireflection coating in metal-oxide-semiconductor photoelectrodes," Nature Materials, 1 (2017) p127.

239. Ruijing Ge, Xiaohan Wu, Myungsoo Kim, Jianping Shi, Sushant Sonde, Li Tao, Yanfeng Zhang, Jack C. Lee, and Deji Akinwande, "Atomristor: Nonvolatile Resistance Switching in Atomic Sheets of Transition Metal Dichalcogenides," Nano Letters, 18 (1) p. 434-441, 2018.

240. Li Ji, Hsien-Yi Hsu, Jack C. Lee, Allen J. Bard, Edward T. Yu, "High performance photodetectors based on solution-processed epitaxial grown hybrid halide perovskites," Nano Letters, 18(2) p. 994-1000, 2018.

241. Y.-C. Chen, Y.-F. Chang, J. Lee, "Selector-Less Graphite Memristor: Intrinsic Nonlinear Behavior with Gap Design Method for Array Applications", Electrochemical Society Transactions, 85 (1), 11-19 (2018).

242. Ying-Chen Chen, Chih-Yang Lin, Hui-Chun Huang, Sungjun Kim, Burt Fowler, Yao-Feng Chang, Xiaohan Wu, Gaobo Xu, Ting-Chang Chang, and Jack C. Lee. "Internal Filament Modulation in Low-dielectric Gap Design for Built-in Selector-less Resistive Switching Memory Application." *Journal of Physics D: Applied Physics*, vol. 51, Issue 5, Feb. 2018.

243. Myungsoo Kim, Ruijing Ge, Xiaohan Wu, Xing Lan, Jesse Tice, Jack C. Lee and Deji Akinwande, "Zero-static power RF Switches Based on MoS2 Atomristors," Nature Communications, June 2018.

244. Ying-Chen Chen, Yao-Feng Chang, Hui-Chun Huang and Jack Lee, "Effects of ambient sensing on SiOx-based resistive switching and resilience modulation by stacking engineering," Electronic Materials and Processing of Electrochemical Society Journal of Solid-State Science and Technology, July 2018.

245. Ying-Chen Chen, Szu-Tung Hu, Chih-Yang Lin, Burt Fowler, Hui-Chun Huang, Chao-Cheng Lin, Sungjun Kim,Yao-Feng Chang, and Jack C. Lee, "Graphite-based Selectorless RRAM: Improvable Intrinsic Nonlinearity for Array Applications", *Nanoscale* 2018.

246. Yao-Feng Chang, Burt W Fowler, Ying-Chen Chen, Zhi-Yang Lin, Gaobo Xu, Huichun Huang, Jia Chen, Sungjun Kim, Yi Li and Jack C. Lee "Beyond SiOx: An Active Electronics Resurgence and Biomimetic Reactive Oxygen Species Production and Regulation from Mitochondrion," Journal of Materials Chemistry C (2018).

247. Ruijing Ge, Xiaohan Wu, Myungsoo Kim, Jianping Shi, Sushant Sonde, Li Tao, Yanfeng Zhang, Jack C Lee, Deji Akinwande "Atomristor: nonvolatile resistance

switching in atomic sheets of transition metal dichalcogenides", Nano letters 18 (1), 434-441. 2018.

248. Ying-Chen Chen, Chao-Cheng Lin, Sungjun Kim, and Jack C. Lee, "Selectorless Oxide-based Resistive Switching Memory with Nonuniform Dielectric for Low Power Crossbar Array Applications" Electrochemical Society ECS Transactions, 2019.

249. Ying-Chen Chen, Hui-Chun Huang, Chih-Yang Lin, Szu-Tung Hu, Yao-Feng Chang and Jack C. Lee "Selectorless Resistive Switching Memory: Non-uniform Dielectric Architecture and Seasoning Effect Determination for Low Power Array Applications" *AIP Advances* (2019) (Featured on cover)

250. Ying-Chen Chen, Chao-Cheng Lin, Szu-Tung Hu, Chih-Yang Lin, Burt Fowler, and Jack Lee "A Novel Resistive Switching Identification Method through Relaxation Characteristics for Sneak-path-constrained Selectorless RRAM application", *Scientific Reports* (2019).

251. Xiaohan Wu, Ruijing Ge, Po-An Chen, Harry Chou, Zhepeng Zhang, Yanfeng Zhang, Sanjay Banerjee, Meng-Hsueh Chiang, Jack C. Lee, Deji Akinwande "Thinnest Nonvolatile Memory Based on Monolayer h-BN", Advanced Materials 31 (15), 1806790. 2019.

252. Myungsoo Kim, Emiliano Pallecchi, Ruijing Ge, Xiaohan Wu, Guillaume Ducournau, Jack C. Lee, Henri Happy, Deji Akinwande, "Analogue switches made from boron nitride monolayers for application in 5G and terahertz communication systems", Nature Electronics vol. 3, p. 479-485 (2020).

253. X. Wu, R. Ge, Y. Huang, D. Akinwande, and J. C. Lee, "Resistance state evolution under constant electric stress on a MoS_2 non-volatile resistive switching device," *The Royal Society of Chemistry (RSC) Advances*, vol. 10, no. 69, pp. 42249-42255, 2020.

254. Hyojong Cho, Ji-Ho Ryu, Chandreswar Mahata, Muhammad Ismail, Ying-Chen Chen, Yao-Feng Chang, Seongjae Cho, Alexey N Mikhaylov, Jack C Lee, Sungjun Kim, "Bipolar resistive switching with unidirectional selector function in nitride/oxide heterostructures" Applied Physics Letters vol. 53 (43) p. 435102 (1-6), 2020.

255. Mostafa Rahimi Azghadi, Ying-Chen Chen, Jason K. Eshraghian, Jia Chen, Chih-Yang Lin, Amirali Amirsoleimani, Adnan Mehonic, Anthony J Kenyon, Burt Fowler, Jack C. Lee, Yao-Feng Chang, "CMOS and Memristive Hardware for Neuromorphic Computing" Advanced Intelligent Systems, p. 1900189: 1-24 (2020).

256. Ying-Chen Chen, Chih-Yang Lin, Hyojong Cho, Sungjun Kim, Burt Fowler, and Jack C. Lee, "Current-Sweep Operation on Nonlinear Selectorless RRAM for Multilevel Cell Applications" Journal of Electronic Materials, vol. 49, no. 6, p. 3499-

3503 (2020).

257. Yang, Hanjie; Wang, Yang; Zou, Xingli; Bai, Rongxu; Han, Sheng; Wu, Zecheng; Han, Qi; Zhang, Yu; Zhu, Hao; Chen, Lin; Lu, Xionggang; Sun, Qing-Qing; Lee, Jack; Yu, Edward; Akinwande, Deji; Ji, Li, "Growth mechanisms and morphology engineering of atomic layer deposited WS2" accepted to ACS Applied Materials & Interfaces, August 2021.

258. Ying-Chen Chen, Jack Lee, Chih-Yang Lin, "Dual-functional Hybrid Selectorless RRAM and Selection Device for Memory Array Application" *IEEE Transactions on Electron Device*, volume 68, issue 9, p. 4363-4367, Sept. 2021.

259. Hanjie Yang, Yang Wang, Xingli Zou, Rong-Xu Bai, Sheng Han, Zecheng Wu, Qi Han, Yu Zhang, Hao Zhu, Lin Chen, Xionggang Lu, Qingqing Sun, Jack C. Lee, Edward T. Yu, Deji Akinwande, and Li Ji, "Growth Mechanisms and Morphology Engineering of Atomic Layer-Deposited WS_2", ACS Appl. Mater. Interfaces, (2021).

260. Ruijing Ge, Xiaohan Wu, Liangbo Liang, Yuqian Gu, Emmanuel Okogbue, Harry Chou, Jianping Shi, Yanfeng Zhang, Sanjay K. Banerjee, Yeonwoong Jung, Jack C. Lee, Deji Akinwande "A library of atomically thin 2D nanomaterials with resistive switching characteristics" *Advanced Materials*. 2021.

261. Ying-Chen Chen, Chao-Cheng Lin, Yao-Feng Chang, Yao-Feng Chang, "Post-Moore Memory Technology: Sneak Path Current (SPC) Phenomena on RRAM Crossbar Array and Solutions", Micromachines 12 (1), 50 (2021).

262. Y. Huang, X. Wu, Y. Gu, R. Ge, D. Akinwande, and J. C. Lee, "On the stochastic nature of conductive points formation and their effects on reliability of MoS2 RRAM: experimental characterization and Monte Carlo simulation," *Microelectronics Reliability*, 126, 114274, 2021.

263. Y. Gu, M. I. Serna, S. Mohan, A. Londoño-Calderon, T. Ahmed, Y. Huang, J. Lee, S. Walia, M. T. Pettes, K. M. Liechti, and D. Akinwande, "Sulfurization Engineering of One-step Low-temperature MoS2 and WS2 Thin Films for Memristor Device Applications" *Advanced Electronic Material*, 8(2): 2100515, 2021.

264. Hanjie Yang, Yang Wang, Xingli Zou, Rong-Xu Bai, Sheng Han, Zecheng Wu, Qi Han, Yu Zhang, Hao Zhu, Lin Chen, Xionggang Lu, Qingqing Sun, Jack C. Lee, Edward T. Yu, Deji Akinwande, and Li Ji, "Wafer-scale synthesis of WS_2 films with in-situ controllable p-type doping by atomic layer deposition", Research, Volume 2021, Article ID 9862483, Dec. 2021.

265. Zecheng Wu, Yu Zhang, Shiqiang Lu, Rongxu Bai, Na Gao, Kai Huang, Shen Hu, Qingqing Sun, David Wei Zhang, Jack C. Lee, Edward T. Yu, and Li Ji, "Amorphous semi-insulating Al-doped In_2O_3 growth by atomic layer deposition for thin-film transistors," Journal of Vacuum Science & Technology A, Volume 40, Issue 4,

042402, May 12, 2022.

266. Xiaohan Wu, Yuqian Gu, Ruijing Ge, Martha I. Serna, Yifu Huang, Jack C. Lee, and Deji Akinwande, "Electron irradiation-induced defects for reliability improvement in monolayer MoS2-based conductive-point memory devices". *npj 2D Materials and Applications*, *6*(1), 1-12, 2022.

267. Alam, Md Hasibul; Chowdhury, Sayema; Roy, Anupam; Wu, Xiaohan; Ge, Ruijing; Rodder, Michael; Chen, Jun; Lu, Yang; Stern, Chen; Houben, Lothar; Chrostowski, Robert; Burlison, Scott; Yang, Sung Jin; Serna, Martha; Dodabalapur, Ananth; Mangolini, Filippo; Naveh, Doron; Lee, Jack C.; Banerjee, Sanjay; Warner, Jamie; Akinwande, Deji "Wafer-Scalable Single Layer Amorphous Molybdenum Trioxide", *ACS Nano* 2022, 16, 3, 3756–3767, February 21, 2022.

268. Y. Huang, R. Hopkins, D. Janosky, Y.-C. Chen, Y.-F. Chang and J. C. Lee. "Unveiling the Temperature Impact in Analog Memristor for Neuromorphic Computing Applications". *IEEE Transactions on Emerging Topics in Computational Intelligence*, (Under review)

Refereed Conference Publications

1. S. Holland, I-C Chen, J. Lee, Y. Fong, K.K. Young, and C. Hu, "Time-Dependent Breakdown of Thin Oxides," Electrochemical Society Meeting, vol. 86-2, p. 599 - 600, Fall 1986.

2. Y. Fong, I-C Chen, S. Holland, J. Lee and C. Hu, "Dynamic Stressing of Thin Oxides," IEEE International Electron Devices Meeting Technical Digest, p. 664 - 667, December 1986.

3. K. Mayaram, J. Lee, T.Y. Chan and C. Hu, "An Analytical Perspective of LDD MOSFETs," 1986 Symposium on VLSI Technology, no. VI-1, p. 61 - 62, May 1986.

4. J. Lee, I-C Chen, S. Holland, Y. Fong and C. Hu, "Oxide Defect Density, Failure Rate and Screen Yield," 1986 Symposium on VLSI Technology, no. VI-5, p. 69 - 70, May 1986.

5. I-C Chen, J. Lee and C. Hu, "Accelerated Testing of Silicon Dioxide Wearout," 1987 Symposium on VLSI Technology, no. IV-2, p. 23 - 24, May 1987.

6. J. Lee, I-C Chen and C. Hu, "Statistical Modeling of Silicon Dioxide Reliability," IEEE International Reliability Physics Symposium, 26th annual proceeding, p. 131 - 138, April 1988 [Best Paper Award].

7. J. Lee and C. Hu, "Low-Pressure Chemical Vapor Deposited Oxide Process for MOS Device Application," 1988 Symposium on VLSI Technology, no. V-8, p. 49 - 50, May 1988.

8. C. Hu, P. Ko, P. Lee, J. Lee, N. Cheung and B. Liew, "IC Reliability Prediction," SRC Technical Program Conference, Extended Abstract, p. 240, October 1988.

9. R. Moazzami, J. Lee, I-C Chen and C. Hu, "Projecting the Minimum Acceptable Oxide Thickness for Time-Dependent Dielectric Breakdown," IEEE International Electron Devices Meeting Technical Digest, p. 710 - 713, December 1988.

10. J. Carrano, C. Sudhama, J. Lee, A. Tasch and W. Miller, "Electrical and Reliability Characteristics of Lead-Zirconate-Titanate (PZT) Ferroelectric Thin Films for DRAM Application," IEEE International Electron Devices Meeting Technical Digest, p. 255 - 258, December 1989.

11. J. Carrano, C. Sudhama, J. Lee and A. Tasch, "Electrical and Reliability Properties of PZT Thin Films for ULSI DRAM Applications," SEMATECH Centers of Excellence Coordination Meeting, March 20-22, 1990 (Best Paper Award).

12. J. Lin, K. Park, S. Batra, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain, G. Lux, "Effects of Arsenic Segregation and Electron Trapping on the Capacitance-Voltage Behavior of Polysilicon and Polycide Gates," Materials Research Society Proceeding, vol. 182, p. 195 - 200, April 1990.

13. C. Sudhama, J. Carrano, L. Parker, V. Chikarmane, J. Lee, A. Tasch, W. Miller, N. Abt and W. Shepherd, "Scaling Properties in the Electrical and Reliability Characteristics of Lead-Zirconate-Titanate (PZT) Ferroelectric Thin Film Capacitors," Proc. of the Spring Meeting of the Materials Research Society, vol. 200, p. 331 - 336, April 1990.

14. H. Hwang, W. Ting, D.L. Kwong and J. Lee, "High Quality Ultrathin Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N_2O," Solid State Devices Meeting, p. 1155 - 1156, August 1990.

15. H. Hwang, W. Ting, B. Maiti, D. L. Kwong and J. Lee, "Electrical Characteristics of Ultrathin Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N_2O," SRC Technical Program Conference, Extended Abstract, p. 91 - 94, October 1990.

16. V. Chikarmane, C. Sudhama, J. Carrano, J. Lee and A. Tasch, " Material Characterization of Sol-Gel Derived PZT Films for ULSI DRAM Applications," Proc. of SRC Technical Program Conference, p. 139 - 142, October 1990.

17. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "Electrical Characteristics of Ultrathin Oxynitride Gate Dielectric Prepared by Rapid Thermal Oxidation of Si in N_2O," Electrochemical Society Meeting, Extended Abstract # 312, October 1990.

18. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "Electrical and Reliability Characteristics of Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N_2O," IEEE

International Electron Devices Meeting Technical Digest, p. 421 - 424, December 1990.

19. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "Deign Issues for Achieving Latchup-Free, Deep Trench-Isolated, Bulk, Non-Epitaxial, Submicron CMOS," IEEE International Electron Devices Meeting Technical Digest, p. 185 - 188, December 1990.

20. V. Chikarmane, C. Sudhama, J. Lee, and A. Tasch, "The Effects of Pb Compensation and Thermal Processing on the Characteristics of DC-Magnetron Sputtered Lead Zirconate Titanate Thin Films," Proc. of the Spring Meeting of the Materials Research Society, Vol. 230, p. 297 - 300, April 1991.

21. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "Ultrathin Oxynitride Gate Dielectric Prepared by Rapid Thermal Oxidation in N_2O for ULSI Applications," Proc. of the Spring Meeting of the Materials Research Society, p. 379 - 384, April 1991.

22. J. Lin, K. Park, S. Batra, S. Banerjee, J. Lee and G. Lux, "Effects of $TiSi_2$ Formation on Boron Penetration Through Gate Oxides in MOS Devices Under Rapid Thermal Processing," Proc. of the Spring Meeting of the Materials Research Society, p. 152 - 155, April 1991.

23. H. Hwang, W. Ting, D. L. Kwong, and J. Lee, "Excellent Reliability Characteristics of Submicron MOSFETs with Oxynitride Gate Dielectric Prepared by Rapid Thermal Oxidation in N_2O," SPIE Optical Engineering Conference, May 8-10, 1991.

24. C. Sudhama, V. Chikarmane, J. Kim, J. Lee and A. Tasch, "Measurement Techniques for Characterization of Ferroelectric Thin Films for Memory Applications," SPIE Optical Engineering Conference, May 8-10, 1991.

25. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "The Effects of Pb Compensation and Thermal Processing on the Phase Content and Electrical Characteristics of DC-Magnetron Sputtered PZT Thin Films," SPIE Optical Engineering Conference, May 8-10, 1991.

26. J. Lin, K. Park, S. Batra, S. Banerjee, J. Lee and G. Lux, "Effects of $TiSi_2$ Formation on Boron Penetration through Gate Oxides in MOS Devices," SPIE Optical Engineering Conference, May 8-10, 1991.

27. B. Maiti and J. Lee, "Stacked Thermal/LPCVD Oxide for Ultra-thin Gate Dielectric Application," SPIE Optical Engineering Conference, May 8-10, 1991.

28. B. Maiti and J. Lee, "The Effects of Post-Deposition Annealing on Dielectric Integrity of Thin Chemical Vapor Deposited Oxides," SPIE Optical Engineering Conference, May 8-10, 1991.

29. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "The Effects of Deposition Temperature and Annealing on the Material and Electrical Characteristics of DC-Magnetron Sputtered PZT Thin Films Capacitors," Electronic Materials Conference, Technical Program Abstract, p. 2 - 7, June, 1991.

30. K. Picone, S. Batra, K. Park, M. Lobo, S. Bhattacharya, J. Lee and S. Banerjee, "Leakage Characteristics and Lateral Uniformity of Ultra-Shallow Junctions Formed Using Polysilicon and Amorphous Silicon Diffusion Source," Electronic Materials Conference, June, 1991

31. H. Hwang, W. Ting, D. L. Kwong, J. Lee, "Electrical and Reliability Characteristics of Submicron nMOSFET's with Oxynitride Gate Dielectrics Prepared by Rapid Thermal Oxidation in N_2O," Device Research Conference, p. IVB-6 - IVB-7, June, 1991.

32. C. Sudhama, V. Chikarmane, J. Kim, J. Lee and A. Tasch, "Electrically Induced Improvement in the Properties of Thin Ferroelectric Films for NVRAM and DRAM Cells," Proceedings of the 10th Annual Symposium on Electronic Materials, Processing and Characterization Conference, June 3-4, 1991.

33. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "Electrical Characteristics and Structure Property Relationships in DC-Magnetron Sputtered PZT Thin Film Capacitors Annealed in Oxygen and Nitrogen Ambient for ULSI DRAM Applications, " 10th Annual Symposium on Electronic Materials Processing and Characterization, June 1991.

34. C. Maziar and J. Lee, "Team Teaching a Multi-Section Introductory Electronics Course," Proceedings of the 1991 Frontiers in Education Conference, p.709 West Lafayette, IN, September 21-24, 1991.

35. V. Chikarmane, J. Kim, C. Sudhama, J. Lee and A. Tasch, "Growth and Electrical Characterization of $Pb(Zr_xTi_{1-x})O_3$ Thin Films for Memory Applications," 3rd Annual New Mexico Symposium on Ceramics and Advanced Materials, October 24, 1991.

36. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "Effects of Post-deposition Annealing Ambient on the Electrical Characteristics and Phase-Transformation Kinetics of Sputtered Lead Zirconate Titanate (65/35)Thin Film Capacitors," American Vacuum Society 38th Annual Symposium, Seattle, WA, November, 1991.

37. C. Sudhama, J. Kim, V. Chikarmane, J. Lee and A. Tasch, "The Effects of La Doping on the Electrical Properties of Sol-Gel Derived Ferroelectric Lead-Zirconate-Titanate (PZT) for ULSI DRAM Application," American Vacuum Society 38th Annual Symposium, Seattle, WA, November 1991.

38. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "The Role of the PZT-Pt Interface in the Anomalous Phase Transformation Kinetics in Sputtered Thin Film

Capacitors at sub-200nm Thicknesses," Proceeding of the Fall Meeting of the Materials Research Society, Vol. 243, p. 367 - 372, December 1991.

39. C. Sudhama, J. Kim, V. Chikarmane, J. Lee and A. Tasch, "Polarity and Area Dependence of Reliability Characteristics of Sputtered and Sol-Gel Derived Thin PLZT Films for DRAM Applications," Proceeding of the Fall Meeting of the Materials Research Society, Vol. 243, p. 147 - 152, December 1991.

40. V. Chikarmane, J. Kim, C. Sudhama, J. Lee and A. Tasch, "The Dependence of Device Electrical Properties on the Zr/Ti Ratio in Reactively Sputtered Ferroelectric $Pb(Zr_xTi_{1-x})O_3$ Thin FIlms for Memory Applications," Minerals, Metals and Materials Society (TMS) Annual Meeting, San Diego, CA, March 1992.

41. J. Lee, V. Chikarmane, C. Sudhama, J. Kim and A. Tasch, "Sputtered PZT Thin Films for Memory Applications," 4th International Symposium on Integrated Ferroelectrics, Monterey, CA, March 1992, Invited Paper.

42. W. Chen, J. Lin, S. Banerjee and J. Lee, "Thermal Stability of Cobalt Disilicide for Self-Aligned Silicide Applications," Spring Meeting of Materials Research Society, Mat. Res. Soc. Symp. Proc., vol. 260, p.163 - 167, April 1992.

43. J. Lin, W. Chen, S. Banerjee and J. Lee, "Study of SITOX (SIlicidation Through OXide) Process and its Application to Advanced CMOS Devices," Spring Meeting of Materials Research Society, Mat. Res. Soc. Symp. Proc., vol. 260, p.623 - 628, April 1992.

44. M. Hao, J. Lee, I.C. Chen and C. Teng, "Reliability of Submicron MOSFET's with Deposited Gate Oxides Under F-N Injection and Hot-Carrier Stress," Spring Meeting of Materials Research Society, Mat. Res. Soc. Symp. Proc., vol. 265, p. 237 - 242, Sept. 1992.

45. H. Hwang and J. Lee, "Excellent Boron Diffusion Barrier Characteristics of Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N_2O," Spring Meeting of Materials Research Society, April 1992.

46. B. Maiti and J. Lee, "Electrical and Reliability Characteristics of Silicon-Rich Oxide for Non-volatile Memory Applications," Spring Meeting of Materials Research Society, vol. 265, p. 255 - 260, April 1992.

47. J. Kim, V. Chikarmane, C. Sudhama, J. Lee and A. Tasch, "The Impact of Device Asymmetry on the Fatigue-Endurance of Ferroelectric PZT for Memory Applications," Spring Meeting of Materials Research Society, vol. 265, p. 313 - 318, April 1992.

48. B. Maiti and J. Lee, "Highly-Reliable Stacked Thermal/LPCVD Oxides for Ultrathin Gate Dielectric Applications," Spring Meeting of Materials Research Society, vol. 265, p. 261 - 266, April 1992.

49. C. Sudhama, J. Kim, V. Chikarmane, R. Khamankar, J. Lee and A. Tasch, "Optimization of Pb Compensation with Thickness-Scaling of Thin Sputtered PZT Films in the 200nm Range for Memory Applications," Electronic Materials Conference, June 1992.

50. J. Lin, W. Chen, S. Banerjee and J. Lee, "Cobalt Disilicide as a Dopant Source for Polysilicon Gates in MOS Devices," Electronic Materials Conference, June 1992, Journal of Electronic Materials, vol. 22, No. 6, p. 667 - 673, 1993.

51. B. Maiti and J. Lee, "A New Low-Thermal Budget Process for Ultrathin Oxynitride Dielectric," Electronic Materials Conference, June 1992.

52. J. Kim, V. Chikarmane, C. Sudhama, R. Khamankur and J. Lee, "The Enhancement of Lifetime of Sputtered Lead Zirconate Titanate Thin Film Capacitors Under A.C. Stressing," Electronic Materials Conference, June 1992.

53. V. Chikarmane, C. Sudhama, J. Kim, R. Khamankar and J. Lee, "Sputtered ZPT Thin Films with Low-Thermal Budget for I.C. Applications," Electronic Materials Conference, June 1992.

54. B. Maiti, M.Y. Hao and J. Lee, "Incorporation of Nitrogen into Oxynitride Dielectrics through Thermal Nitridation of Silicon," Spring Meeting of Materials Research Society, vol. 309, p.3 - 8, 1993.

55. W. Chen, J. Lin, S. Banerjee and J. Lee, "The Impact of Pre-Silicidation Heat Treatment and Dopant Effects on the Thermal Stability of $CoSi_2$ Polycide during Rapid Thermal Annealing," Materials Research Society Symposia Proceeding, vol. 303, p. 81 - 86, 1993.

56. W. Chen J. Lin, S. Banerjee and J. Lee, "Using $CoSi_2$/Polysilicon Polycide Structure as a Gate Diffusion Source in Rapid Thermal Processing," Materials Research Society Symposia Proceeding, vol. 303, p. 271 - 276, 1993.

57. J. Lin, W. Chen, S. Banerjee and J. Lee, "Enhanced Boron Diffusion in Silicon Using $CoSi_2$ Diffusion Source and Rapid Thermal Processing," Materials Research Society Symposia Proceeding, vol. 303, p. 265 - 270, 1993.

58. J. Kim, C. Sudhama, R. Khamankar and J. Lee, "Ultra-Thin (65nm) Sputtered PZT Films for ULSI DRAMs," Materials Research Society Symposium Proceedings, vol. 310, p.473 - 478, 1993.

59. J. Kim, R. Khamankar, C. Sudhama, J. Lee, S. Summerfelt and B. Gnade, "Investigation of Electrode Materials for Metal-Ferroelectrics-Pt Capacitors for DRAM Applications," 184th Meeting of Electrochemical Society Meeting, Extended Abstracts, vol. 93-2, p. 269 - 270, Oct. 1993.

60. W. M. Chen, J. C. Lee, and M. R. Frost, " Silicided p-n junction fabricated by silicidation through silicon buffer layer and dopant drive-out process ," Mat. Res. Soc. Symp. Proc., vol. 320, p. 47 - 51, 1993.

61. J. Lee, C. Sudhama, J. Kim and R. Khamankar, "High Dielectric Constant Ferroelectric Thin Films for DRAM Applications," International Conference on Solid State Devices and Materials, Chiba, Japan, 1993(Invited Paper).

62. C. Sudhama, R. Khamankar, J. Kim, J. C. Lee, P. D. Maniar, R. Moazzami, R. E. Jones and C. J. Mogab, "Novel Methods for the Reliability Testing of Ferroelectric DRAM Storage Capacitors," 32nd Annual IEEE International Reliability Physics Proceedings, p. 238 - 242, 1994.

63. J. Kim, C. Sudhama, R. Khamankar, B. Jiang, J. Lee, P. Maniar, R. Moazzami, R. Jones and C. J. Mogab, "La Doped PZT Thin Films for Gigabit DRAM Technology," 1994 Symposium on VLSI Tech. Digest, Honolulu, June 1994 and published in VLSI Tech. Digest, p. 151 - 152, 1994.

64. R. Khamankar, J. Kim, C. Sudhama and J. Lee, "Effect of Deposition Temperature on Material and Electrical Properties of PZT Thin Films for DRAM Applications," International Symposium on Integrated Ferroelectrics, 1994, published in Integrated Ferroelectrics, 1994.

65. K. Lai, M. Y. Hao, W. M. Chen, and J. Lee, "Surface Cleaning Effects on Reliability for Devices with Ultrathin Oxides or Oxynitrides," Proceedings of SPIE Conference on Microelectronics Manufacturing '94, vol. 2334, p. 137-143, Oct. 1994.

66. R. Khamankar, J. Kim, B. Jiang, and J. Lee, "Effects ac Stress on Charge and Voltage Decay Rates of PZT Thin Film Capacitors for DRAM Applications," Material Research Symposium Fall Meeting, Boston, MA, Nov. 1994.

67. B. Jiang, J. Kim, R. Khamankar, I. Lee, and J. Lee, "Effects of Electron-beam Irradiation on PZT/PLZT Thin Film Capacitors," Material Research Symposium Fall Meeting, Boston, MA, Nov. 1994.

68. J. Kim, B. Jiang, R. Khamankar, I. Lee, J. Lee, P. Maniar, R. Moazzami, and R. Jones, "Effects of Microstructure on the Electrical Characteristics of Sol-Gel Derived PZT Thin Films," Material Research Symposium Fall Meeting, Boston, MA, Nov. 1994

69. R. Khamankar, J. Kim, B. Jiang, J. Lee, P. Maniar, R. Moazzami, R. Jones, "Impact of Process Damages on Performance of High Dielectric Constant PLZT Capacitor for ULSI DRAM Applications," IEEE International Electron Devices Meeting Technical Digest, p. 337 - 339, Dec. 1994.

70. M. Y. Hao, K. Lai, W. M. Chen and J. Lee, "Reliability Characteristics and Surface Preparation Technique for Ultra-thin (33 Å - 87 Å) Oxides and Oxynitrides," IEEE International Electron Devices Meeting Technical Digest, p. 601 - 603, Dec. 1994.

71. W. M. Chen, J. Lin and J. Lee, "A Novel $CoSi_2$ Thin Film Process with Improved Thickness Scalability and Thermal Stability," IEEE International Electron Devices Meeting Technical Digest, p. 691 - 695, Dec. 1994.

72. K. Lai, A. Chou, K. Kumar, P. Chowdhury, M. Hao, W. Chen, M. Gardner, J. Fulford and J. Lee, "Breakdown Mechanisms and Stress-Induced Leakage Current in Ultra-thin Oxides and N_2O Oxynitrides," Eleventh Biennial University/ Government / Industry Microelectronics Symposium, May 1995.

73. C. Sudhama, J. Kim, V. Chikarmane, R. Khamankar, J. Lee and A. Tasch, "Optimization of Pb Compensation with Thickness-Scaling of Thin Sputtered PZT Films in the 200nm Range for Memory Applications," Journal of Electronic Materials.

74. R. Khamankar, B. Jiang, R. Tsu, W. Hsu, J. Nulman, S. Summerfelt, M. Anthony and J. Lee, "A Novel Low-Temperature Process for High Dielectric Constant BST Thin Films for ULSI DRAM Applications," presented at the 1995 Symposium on VLSI Technology, Kyoto, Japan, May 1995 and published in VLSI Techn. Digest, p. 127 - 128, 1995.

75. Jack C. Lee, Anthony Chou, Kafai Lai and Kiran Kumar, "N_2O-Based tunnel oxides", Proceedings of SPIE Conference on Microelectronics Manufacturing '95, vol. 2636, p. 182.

76. Kafai Lai, Anthony Chou, Kiran Kumar, Mark Gardner, Jim Fulford, and Jack C. Lee, "Effects of gate doping species, concentration, and microstructure on the electrical and reliability characteristics of ultrathin oxides and N_2O-oxynitrides", Proceedings of 1995 International Semiconductor Device Research Symposium, Dec. 1995.

77. Kafai Lai, Kiran Kumar, Anthony I. Chou, and Jack C. Lee, "Effects of oxide exposure, photoresist and dopant activation on the plasma damage immunity of ultrathin oxides and oxynitrides", Tech. Dig. IEEE Int. Elec. Dev. Mtg. Tech. Dig., p. 319, 1995.

78. T. Chen, V. Balu, B. Jiang, S. Kuah and J. Lee, "Stability of Reaactive DC-Sputtered Ir and IrO_2 Thin Films in Various Ambients,"presented at the Int. Symp. on Integrated Ferroelectrics, March 18-20, Tempe, AZ, 1996 and published in ISIF Extended Abstract, p. 48C, 1996.

79. B. Jiang and J. Lee, "Modeling Ferroelectric Capacitor Switching Using Parallel-Element Model," presented at the Int. Symp. on Integrated Ferroelectrics, March 18-20, Tempe, AZ, 1996 and published in ISIF Extended Abstract, p. 49C, 1996.

80. V. Balu, T. Chen, B. Jiang, S. Kuah and J. Lee, P. Chu, R. Joens, P. Zurcher, D. Taylor and S. Gillespie, "Electrode Materials for Ferroelectic Capacitors: Properties of Reactive DC Sputtered IrO_2 Thin Films," 1996 Materials Research Society Spring Meeting, San Francisco, CA, April 8-12, 1996; abstract no. T4.3, 1996 MRS Abstract Proceeding, p. 337, 1996 and published in MRS Symposium Proceedings, Ferroelectric thin films V, p.169, 1996.

81. B. Jiang, V. Balu, T. Chen, S. Kuah, and J. Lee, "Polarization Relaation in PZT/PLZT Thin Film Capacitors, " 1996 Materials Research Society Spring Meeting, San Francisco, CA, April 8-12, 1996; abstract no. T6.3, 1996 MRS Abstract Proceeding, p. 340, 1996.

82. B. Jiang, V. Balu, T. Chen, Jack Lee, P. Chu, R. Jones, P. Zurcher, D. Taylor, M. Kottke, and S. Gillespie, "A New Electrode Technology for High-Density Nonvolatile Ferroelectric (SrBi2Ta2O9) Memories," presented at the 1996 Symposium on VLSI Technology, Honolulu, June 1996 and published in VLSI Techn. Digest, p. 26-27, 1996.

83. C. Lin, A. Chou, K. Kumar, P. Chowdhury, and J. C. Lee, "Leakage current, reliability characteristics and boron penetration of ultra-thin (32-36Å) O_2-oxide and N_2O/NO-Oxynitrides, Tech. Dig. IEEE Int. Elec. Dev. Mtg. Tech. Dig., 1996, p-331.

84. C. Lin, A. Chou, B. Doyle, H. R. Soleimani, and J. C. Lee, "Effect of nitrogen implant on gate oxide reliability," 27th IEEE Semiconductor Interface Specialists Conference, San Diego, CA, 1996.

85. Tung-Sheng Chen, Venkatasubramani Balu, Bo Jiang, Shao-Hong Kuah, and Jack Lee, “Stability of reactive DC-sputtered Ir and IrO_2 thin films in various ambients,” International Symposium on Integrated Ferroelectrics (ISIF), 1996.

86. Tung-Sheng Chen, Daniel Hadad, Venkatasubramani Balu, Bo Jiang, Shao-Hong Kuah, Paul McIntyre, Scott Summerfelt, Mark Anthony, and Jack Lee, “Ir-electroded BST thin film capacitors for 1 giga-bit DRAM application,” Tech. Dig. IEEE Int. Elec. Dev. Mtg. (IEDM), p. 679, 1996.

87. Shaohong Kuah, Venkatasubramani Balu, Tung-Sheng Chen, Bo Jiang, Daniel Hadad, Bruce White, Robert Jones, Peter Zurcher, Bradley Melnick, Sherry Gillespie and Jack C. Lee, “Interaction of Ir and IrO_2 Thin Films with Polysilicon, W and WSi_x”. The 9th International Symposium on Integrated Ferroelectrics (ISIF), p. 150C, Mar 2-5, 1997.

88. Daniel Hadad, Tung-Sheng Chen, Venkatasubramani Balu, Bo Jiang, ShaoHong Kuah, Paul McIntyre, Scott Summerfelt, Mark Anthony and Jack C. Lee, “The Effects ofForming Gas Anneal on the Electrical Characteristics of Ir-Electroded BST Thin Film Capacitors” The 9th International Symposium on Integrated Ferroelectrics (ISIF), p. 152C, Mar 2-5, 1997.

89. A. Chou, C. Lin, K. Kumar, P. Chowdhury, M. Garder, M. Gilmer, J. Fulford, and J. C. Lee, "The effects of nitrogen implant into gate electrode on the characteristics of dual-gate MOSFETS with ultra-thin oxide and oxynitrides," International Reliability Physics Symposium, 1997.

90. Bo Jiang, P. Zurcher, R. Jones, S. Gillespie, and J. Lee, "Computationally Efficient Ferroelectric Capacitor Model for Circuit Simulation," presented at the 1997 Symposium on VLSI Technology, Kyoto, Japan, June 1997 and published in VLSI Tech. Digest, p. 141-142, 1997.

91. Chou, Chan Lin, Keith Zawadzki, Yongjoo Jeon, Aaron Lucas and Jack Lee, "Enhanced oxidation rate of oxynitrides during RTP in N_2O," the 28th IEEE Semiconductor Interface Specialists Conference, Charleston, SC, 1997.

92. Venkatasubramani Balu, Tung-Sheng Chen, Shylaja Katakam, Jian-Hung Lee, Bruce White, Sufi Zafar, Bo Jiang, Peter Zurcher, Robert E. Jones and Jack C. Lee, "Dielectric Dispersion in Barium Strontium Titanate Thin Film capacitors with Ir electrodes", Presented at the 10th International Symposium on Integrated Ferroelectrics, March 1-4, 1998, Published in the Integrated Ferroelectrics.

93. Tung-Sheng Chen, Venkatasubramani Balu, Shylaja Katakam, Jian-Hung Lee, B. White, S. Zafar, B. Jiang, P. Zurcher, R. Jones and Jack C. Lee, "Study of $SrTiO_3$ Thin Films on Ir Bottom Electrodes for Ultra-large scale Integrated DRAM application" Presented at the 10th International Symposium on Integrated Ferroelectrics, Mar 1-4, 1998, Published in the Integrated Ferroelectrics.

94. Tung-Sheng Chen, Venkatasubramani Balu, Shylaja Katakam, Jian-Hung Lee, Jeong Hee Han, Robert E. Jones, Sherry Gillespie and Jack C. Lee, "Dynamic Stressing Effects on Reliability of Strontium Titanate Thin Film Capacitors for High-density Memory Applications" 1998 Symposium on VLSI Technology Digest of Technical Papers, p. 54, (1998).

95. Keith Zawadzki, Wen Jie Qi, Yongjoo Jeon, Byoung Hun Lee, Aaron Lucas, Renee Nieh, and Jack Lee, "Sputtered BST Thin Films for Alternative High K Gate Dielectrics", Proceedings of American Vacuum Society Symposium, Austin, 1998.

96. Byoung Hun Lee, Yongjoo Jeon, Keith Zawadzki, Wen-Jie Qi, Renee Nieh, Aaron Lucas and Jack Lee, "Leakage characteristics of TiO2 films", Proceedings of American Vacuum Society Symposium, Austin, 1998.

97. Yongjoo Jeon, Keith Zawadzki, Byoung Hun Lee, Venkatsubramani Balu, and Jack Lee, "Alternative Gate Dielectric with BST/TiO2(Barrier Layer) Stacked Structure", Abstracts of MRS Symposium on Rapid thermal and Integrated Processing, San Fransisco, April 10, p.370, 1998.

98. Byoung Hun Lee, Yongjoo Jeon, Aaron Lucas, Mark Gilmer, Mark Gardner, Jim Fair and Jack C. Lee, "Comparative study of TiO_2 and Ta_2O_5 on JVD nitride as an alternative gate dielectrics", 29th IEEE Semiconductor Interface Specialists Conference, December 1998.

99. Jian-Hung Lee, Venkatasubramani Balu, Tung-Sheng Chen, Jeong Hee Hanand Jack C. Lee, "N2O Processed Ferroelectric Thin Films", MRS Symposium Proceedings, Ferroelectric thin films VII, 1998.

100. Yongjoo Jeon, Byoung Hun Lee, Keith Zawadzki, Wen-Jie Qi, Aaron Lucas, Renee Nieh and Jack Lee, "Effect of Barrier layer on the Electrical and Reliability Characteristics of High-k gate dielectric films", IEEE Tech. Dig. Of International Electron Devices Meeting, p. 707, December 1998.

101. Jeong Hee Han, Venkatasubramani Balu, Jian-Hung Lee, Razak Mohammedali, Sundar Gopalan, Chun-Hui Wong and Jack C. Lee, "Effect of N_2O on RF-magnetron sputtered $SrTiO_3$ films for ULSI DRAM applcation," Presented at the 11th International Symposium on Integrated Ferroelectrics, March 1999.

102. Renee Nieh, Wen-Jie Qi, Yongjoo Jeon, Byoung Hun Lee, Aaron Lucas and Jack C. Lee," Nitrogen implantation to suppress growth of interfacial oxide in MOCVD BST and sputtered BST films", Proceedings of MRS spring meeting,1999.

103. J. Lee, "ZrO_2 Thin Films for Gate Dielectric Applications" an Invited Talk to be presented at the Taiwan Future Development Conference, Hsin-Chu, Taiwan, June 24, 1999.

104. J. Lee, "ZrO_2 and Zr-Silicate Ultra-thin Gate Dielectrics" an Invited Talk to be presented at the SEMATECH Gate Stacked Workshop, Austin TX, July 22, 1999.

105. J. Lee, "High-K Gate Dielectrics" an Invited Talk to be presented at the SPIE's 1999 Symposium and Education Program on Microelectronic Manufacturing, Santa Clara, CA September 22, 1999.

106. J. Lee, "High-K Films for Gate Dielectric" an Invited Talk to be presented at the First International Workshop on Dielectric Thin Films for Future ULSI Devices: Science and Technology, Tokyo, Japan, October 22-23, 1999.

107. B. Lee, L. Kang, W. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. Lee, "Ultrathin Hafnium oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application," IEEE Tech. Dig. Of International Electron Devices Meeting, p. 133, December 1999.

108. W. Qi, R. Nieh, B. Lee, L. Kang, Y. Jeon, K. Onishi, T. Ngai, S. Banerjee, and J. Lee, "MOSCAP and MOSFET Characteristics Using ZrO_2 Gate Dielectric Deposited

Directly on Si", IEEE Tech. Dig. Of International Electron Devices Meeting, p. 145, December 1999.

109. L. Kang, B. Lee, W. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, and J. Lee, "Highly Reliable Thin Hafnium Oxide Gate Dielectric," presented at the Materials Research Symposium, Fall 1999.

110. B. Lee, L. Kang, W. Qi, R. Nieh, Y. Jeon, and J. Lee, "Electrical Characteristics of Ultra-Thin Hafnium Oxide Gate Dielectric", Proceedings of the 30th IEEE Semiconductor Interface Specialists Conference, December 1999.

111. W. Qi, R. Nieh, B. Lee, L. Kang, Y. Jeon and J. Lee, "Study on ZrO_2 Deposited Directly on Si as an Alternative Gate Dielectric Material", Proceedings of Materials Research Symposium, vol. 606, 2000.

112. W. Qi, K. Zawadzki, R. Nieh, Y. Jeon, B. Lee, A. Lucas, L. Kang, and J. Lee, "A study on Hysteresis Effect of Barrium Strontium Titanate Thin Films for Alternative Gate Dielectric Application," Proceedings of Materials Research Symposium, vol. 606, 2000.

113. W. Qi, R. Nieh, B. Lee, L. Kang, Y. Jeon, K. Onishi, S. Gopalan, and J. Lee, "Temperature Effect on the Reliability of ZrO_2 Gate Dielectric Deposited Directly on Silicon," IEEE International Reliability Physics Symposium, p. 72, April 2000.

114. Wen-Jie Qi, Byoung Hun Lee, Renee Nieh, Laegu Kang, Yongjoo Jeon, Katsu Onishi, and Jack C. Lee, "High-k gate dielectrics", Proc. SPIE Vol. 3881, p. 24-32, Microelectronic Device Technology III, 2000.

115. Laegu Kang, Yongjoo Jeon, Katsunori Onishi, Byoung Hun Lee, Wen-Jie Qi, Renee Nieh, Sundar Gopalan, and Jack C. Lee, "Single-layer Thin HfO_2 Gate Dielectric with n+-Polysilicon Gate," Symposium on VLSI Technology, pp. 44, 2000.

116. Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Katsunori Onishi, Laegu Kang, Yongjoo Jeon, Jack C. Lee, Vidya Kaushik, Bich-Yen Neuyen, Lata Prabhu, Kurt Eigenbeiser, and Jeff Finder,"Performance of MOSFETs with ultra-thin ZrO_2 and Zr silicate gate dielectrics," Symposium on VLSI Technology, pp. 40, 2000.

117. Y. –Y. Fan, S. Mudani, W. Qi, J. C. Lee, A. F. Tasch, L. F. Register, and S. K. Banerjee, "Modeling high k gate current from p-type Si inversion layers", Proceedings of 58th Device Research Conference, p.63, 2000.

118. T. Ngai, W. J. Qi, X. Chen, R. Sharma, J. L. Fretwell, J. C. Lee, S. K. Banerjee, "SiGe and Si PMOSFET's characteristics with ZrO_2 gate dielectric", Proceedings of 58th Device Research Conference, p.21, 2000.

119. J.M. Leng, S.Li, J.L. Opsal, B.H. Lee, and J.C. Lee, "Interface between c-Si and the High-k dielectric HfO2: Characterization by rotating compensator spectroscopic ellipsometry (RCSE)", Proceedings of the First International Conference on Microelectronics and Interfaces, 2000.

120. Renee Nieh, Wen-Jie Qi, Byoung Hun Lee, Laegu kang, Yongjoo Jeon, Katsunori Onishi, and Jack C. Lee, "Processing effect and electrical characteristics of ZrO2 formed by RTP oxidation of Zr", ECS spring meeting, Ontario, 2000.

121. J. Lee, "ZrO_2 and HfO_2 Gate Dielectrics," an Invited Talk at PASSS Symposium, Portland OR August 18, 2000.

122. J. Lee, "Ultra-thin High-K Gate Dielectrics," an Invited Talk at IBM Yorktown Research Center Seminar Series, NY September 28, 2000.

123. J. Lee, "Reliability Issues of ZrO2 and HfO2 for Gate Dielectrics Applications," an Invited Talk at the SRC Topic Research Conference, Stanford CA October 30-Nov. 1, 2000.

124. Laegu Kang, Katsunori Onishi, Yongjoo Jeon, Byoung Hun Lee, Changseok Kang, Wen-Jie Qi, Renee Nieh, Sundar Gopalan, Rino Choi, and Jack C. Lee, "MOSFET Devices with Polysilicon on Single-Layer HfO_2 High-K Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 35, 2000.

125. Byoung Hun Lee,Rino Choi, Laegu Kang, Sundar Gopalan, Renee Nieh, Katsunori Onishi, Yongjoo Jeon, Wen-Jie Qi, Changseok Kang, and Jack C Lee, "Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8-12Å)", International Electron Devices Meeting, IEDM Technical Digest, p. 39, 2000.

126. J. Lee, "Scaling of Gate Dielectrics and the Impact of High-K Dielectrics," an Invited Talk at The ULIS'2001 Workshop (2nd European Workshop on Ultimate Integration of Silicon) Grenoble, France January 18-19, 2001.

127. J. Lee, "High-Dielectric Gate Dielectrics" an Invited Talk at the 6th Workshop on Formation, Characterization and Reliability of Ultrathin Silicon Oxide, held at Atagawa, Sizuoka, Japan, p. 55, January 26-27, 2001.

128. J. Lee, "Alternative Gate Dielectrics for Future CMOS Devices" an Invited Talk at the Cypress Semiconductor Workshop, San Jose, CA March 7, 2001.

129. J. Lee, "Future Gate Dielectrics Materials" an Invited Talk in the "Rapid Thermal and Other Short-Time Processing Technologies" Session at the 199th Electrochemical Society (ECS) Meeting, Washington D.C., March 25-30, 2001.

130. J. Lee, "High-K Gate Dielectric Devices" (keynote speaker) 2001 Symposium on Nano Device Technology, Hsinchu, Taiwan, April 23-25, 2001.

131. R. Choi, C. Kang, B. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and J. Lee, "High-Quality Ultra-thin HfO_2 Gate Dielectric MOSFETs with TaN Electrode and Nitridation Surface Preparation," Tech. Dig. of Symposium on VLSI Technology (Highlight Session), p. 15, June 2001.

132. K. Onishi, L. Kang, R. Choi, E. Dharmarajan, S. Gopalan, Y. Jeon, C. Kang, B. Lee, R. Nieh, and J. Lee, "Dopant Penetration Effects on Polysilicon Gate HfO_2 MOSFETs," Tech. Dig. of Symposium on VLSI Technology, p. 131, June 2001.

133. T. Ngai, K. Onishi, R. Choi, C. Kang, J. Fretwell, X. Chen, J. Chen, J. Lee and S. Banerjee, "Electrical Properties of HfO_2 Gate Dielectric on SiGe," Electronic Materials Conference, June 2001.

134. J. Lee, "High-K Gate Dielectrics: ZrO_2 and HfO_2" an Invited Talk presented at the Distinguished Lectures Series of the Electron Devices Society, Kansai Chapter, Kyoto, Japan, June 15, 2001.

135. Easwar Dharmarajan, Wen-Jie Qi, Renee Nieh, Laegu Kang, Katsunori Onishi, and Jack C. Lee, "Ultra-Thin Zirconium Silicate Films With Good Physical and Electrical Properties for Gate Dielectric Applications," MRS fall meeting 2000.

136. Renee Nieh, Katsunori Onishi, Rino Choi, Hag-Ju Cho, Chang Seok Kang, Sundar Gopalan, Siddarth Krishna, and Jack C. Lee, "Performance Effects of Two Nitrogen Incorporation Techniques on TaN/HfO_2 and poly/HfO_2 MOSCAP and MOSFET Devices" 1st International Workshop on Gate Insulator (IWGI) Tokyo, p. 70, Japan, November 1-2, 2001.

137. S. Gopalan, E. Dharmarajan, K. Onishi, R. Nieh, C. S. Kang, R. Choi, H-J. Cho and J. C. Lee, "Ultra-thin Hafnium Silicate films with TaN and Polysilicon gates for gate dielectric application", IEEE Semiconductor Interface Specialist Conference (SISC) Proceedings, p. 11, November 2001.

138. H. Cho, C. Kang, K. Onishi, S. Gopalan, R. Nieh, E. Dharmarajan, and J. Lee, "Novel Nitrogen Profile Engineering for Improved TaN/ HfO_2/Si MOSFET Performance" International Electron Devices Meeting (IEDM Technical Digest), p. 655, 2001.

139. K. Onishi, C. Kang, R. Choi, H. Cho, S. Gopalan, R. Nieh, E. Dharmarajan, and J. Lee, "Reliability Characteristics, including NBTI, of Polysilicon Gate MOSFET's," International Electron Devices Meeting (IEDM Technical Digest), p. 659, 2001.

140. J. Lee, "High-K Gate Dielectrics (HfO_2 and ZrO_2), Semicon Korea Technical Program Digest, p. 155, February 2002.

141. C.M. Osburn, S.K. Han, I. Kim, S. Campbell, E. Garfunkel, T. Gustafson, J. Hauser, T.-J. King, A. Kingon, D.-L. Kwong, S.J. Lee, C.H. Lee, J. Lee, C.S. Kang, K. Onishi,

R. Choi, G. Lucovsky, J.G. Hong, T.P. Ma, W. Zhu, Z. Luo, J.P. Maria, D. Wicaksana, V. Misra, J.J. Lee, Y.S. Suh, G. Parsons, D. Niu, and S. Stemmer, "Integration Issues with High k Gate Stacks" an invited to VLSI Symposium of The Electrochemical Society Meeting, Spring 2002.

142. C. Kang, H. Cho, K. Onishi, R. Choi, R. Nieh, S. Gopalan, S. Krishnan, and J. Lee, "Improved Thermal Stability and Device Perfromance of Ultra-thin (EOT < 10 Å) Gate Dielectric MOSFET's by Using Hafnium Oxynitride (HfO_xN_y)," 2002 Symposium on VLSI Technology, p. 146, June 2002.

142. R. Nieh, S. Krishnan, H. Cho, C. Kang, S. Gopalan, K. Onishi, R. Choi, and J. Lee, "Comparison between ultra-thin ZrO_2 and ZrO_xN_y gate dielectrics in TaN or poly-gated NMOSCAP and NMOSFET devices," 2002 Symposium on VLSI Technology, p. 186, June 2002.

143. K. Onishi, C. Kang, R. Choi, H. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J. Lee, "Effects of High-Temperature Forming Gas Anneal on HfO_2 MOSFET Performance," The 2002 Symposium on VLSI Technology, p. 22, June 2002.

144. Q. Lu, H. Takeuchi, X. Meng, T. King, C. Hu, K. Onihi, H. Cho, and J. Lee, "Improved Performance of Ultra-thin HfO_2 CMOSFETs Using Poly-SiGe Gate," 2002 Symposium on VLSI Technology, p. 86, June 2002.

145. K. Onishi, C. Kang, R. Choi, H. Cho, S. Gopalan, R. Nieh, S. Krishnan and J. Lee, "Charging Effects on Reliability of HfO_2 Devices with Polysilicon Gate Electrode," Proceeding of International Reliability Physics Symposium, pp. 419-420, 2002.

146. Q. Lu, H. Takeuchi, R. Lin, T. King, C. Hu, K. Onishi, R. Choi, C. Kang and J. Lee, "Hot Carrier Reliability of n-MOSFET with Ultra-thin HfO_2 Gate Dielectric and Poly-Si Gate," 2002 International Reliability Physics Symposium Proceedings, p429 (2002).

147. R. Choi, K. Onishi, C. S. Kang, R. Nieh, S. Gopalan, H.-J. Cho, S. Krishnan, and J. C. Lee, "High Quality MOSFETs Fabrication with HfO_2 Gate Dielectric and TaN Gate Electrode", 60th Device Research Conference at the University of California, Santa Barbara, June 24-26, 2002, p. 193.

148. S. Gopalan, R. Choi, K. Onishi, R. Nieh, C. Kang, H. Cho, S. Krishnan, and J. Lee, "Impact of NH_3 Pre-treatment on the Electrical and Reliability Characteristics of Ultra-thin Hafnium Silicate Films Prepared by Re-oxidation Method," 60th Device Research Conference at the University of California, Santa Barbara, June 24-26, 2002, p. 195.

149. K. Onishi, R. Choi, C. Kang, H. Cho, Y. Kim, R. Nieh, J. Han, S. Krishnan, A. Shahriar and J. Lee, "Charge Trapping and Interfacial Degradation of Polysilicon Gate HfO_2 NMOSFET's," Gate Stack Engineering Working Group Symposium, October 16-18, 2002.

150. J. Lee, "Nitrogen Incorporation and High-Temperature Forming Gas Anneal for High-K Gate Dielectrics," an Invited Paper in 202nd Meeting of the Electrochemical Society, p. 171, October 20-25, 2002.

151. J. Lee, "Effects of Interface States and Charge Trapping on Performance of High-K Dielectric Devices," an Invited Paper in the 33rd IEEE Semiconductor Interface Specialists Conference, December 5-7, 2002.

152. C. Kang, H. Cho, K. Onishi, R. Choi, Y. Kim, R. Nieh, J. Han, S. Krishnan and J. Lee, "Nitrogen Concentration Effects and Performance Improvement of MOSFETs Using Thermally Stable HfO_xN_y Gate Dielectrics," International Electron Devices Meeting (IEDM), p. 865, December 2002.

153. Y. Kim, K. Onishi, C. Kang, R. Choi, H. Cho, R. Nieh, J. Han, S. Krishnan and J. Lee, "Hard and Soft-Breakdown Characteristics of Ultra-Thin HfO_2 Under Dynamic and Constant Voltage Stress," International Electron Devices Meeting (IEDM), p. 629, December 2002.

155. R. Choi, K. Onishi, C. Kang, S. Gopalan, R. Nieh, Y. Kim, J. Han, S. Krishnan, H. Cho, A. Shahriar, and J. Lee "'"Fabrication of High Quality Ultra-thin HfO_2 Gate Dielectric MOSFETs Using Deuterium Anneal," International Electron Devices Meeting (IEDM), p. 613, December 2002.

156. Y. H. Kim, K. Onishi, C. S. Kang, R. Choi, H. -J. Cho, S. Krishnan, M. Akbar, and J. C. Lee, "Dynamic Reliability Characteristics of Ultra-Thin HfO_2," Highlight Session of 2003 International Reliability Physics Symposium, p. 46, March 2003.

157. H. Cho, C. Kang, M. Akbar, K. Onishi, Y. Kim, R. Choi, and J. Lee, "Application of Top HfSiON Layer for Improved Poly-Gated HfO_2 PMOSFET Performance," the 61st Device Research Conference (section II.B), p. 37, June 23-25, 2003.

158. Y. H. Kim, K. Onishi, C. S. Kang, R. Choi, H. -J. Cho, M. S. Akbar, and J. C. Lee, "Polarity Dependence of the Reliability Characteristics of HfO_2 with Poly-Si Gate Electrode", the 61st Device Research Conference proceeding (DRC), p.57, 2003.

159. Y. H. Kim, K. Onishi, C. S. Kang, R. Choi, H. -J. Cho, and J. C. Lee, "The Effects of Forming Gas Anneal Temperature and Dielectrics Leakage Current on TDDB Properties of HfO_2 Devices" Electrochemical Society Proceeding (ECS), October 2003.

160. H.-J. Cho, C.Y. Kang, C.S. Kang, Y.H. Kim, R. Choi, A. Shahriar, C.H. Choi, S.J. Rhee and J. C. Lee, "Effects of NH_3 Annealing on High-k HfSiON/HfO_2 Gate Stack Dielectrics," Electrochemical Society Proceeding (ECS), October 2003.

161. C.S. Kang, H.-J. Cho, Y.H. Kim, R. Choi, A. Shahriar, C.Y. Kang, C.H. Choi, S.J. Rhee and J. C. Lee, "Characterization of resistivity and work function of sputtered-TaN

film for gate electrode applications," Electrochemical Society Proceeding (ECS), October 2003.

162. Jack C. Lee, "Hf-based Dielectrics and Reliability" Invited Paper presented at the SRC Topical Research Conference, October 2003.

163. J. Lee, "Hf-based High-K Dielectrics" Invited Paper presented at the International Workshop on Gate Insulator, Tokyo, Japan, Nov. 2003.

164. Y. H. Kim, R. Choi, R. Jha, J.H. Lee, V. Misra and J. C. Lee, "Interface Tunneling Mechanism of HfO_2 /Dual Metal Gate Stack with Varying Interface Layer Thickness and Different Bias Polarities", 34th IEEE Semiconductor Interface Specialists Conference, p. 45, December 2003.

165. J. Lee, "High-K Dielectrics and MOSFET Characteristics", Invited Paper at IEEE International Electron Devices Meeting, Section 4, no. 4, p. 95, December 2003.

166. H. Cho and J. Lee, "The Effects of Nitrogen in HfO_2 for Improved MOSFET Performance" presented at the 2003 International Semiconductor Device Research Symposium, Washington D.C. December 2003.

167. C.M. Osburn, S.A. Campbell, E. Eisenbraun, E. Garfunkel, T. Gustafson, A. Kingon, D.-L. Kwong, J. Lee, G. Lucovsky, T.P. Ma, J.P. Maria, V. Misra, G. Parsons, D. Schlom, and S. Stemmer, "Materials and Processes for High k Gate Stack", International Forum on Semiconductor Technology, Paris, February 2004.

168. Y. H. Kim, R. Choi, R. Jha, J.H. Lee, V. Misra and J. C. Lee. "Effects of Gate Electrodes and Barrier Heights on the Breakdown Characteristics and Weibull Slopes of HfO_2 MOS Devices" 2004 International Reliability Physics Symposium, p. 595, 2004.

169. C. Y. Kang, H. -J. Cho, C. S. Kang, R. Choi, Y. H. Kim, S. J. Rhee, C. H. Choi, A. Shahriar and J. C. Lee, "Effects of Thin SiN Interface Layer on Transient I-V Characteristics and Stress Induced Degradation of High-k Dielectrics," 2004 International Reliability Physics Symposium, p. 587, 2004.

170. Se Jong Rhee, Young Hee Kim, Chang Yong Kang, Chang Seok Kang, Hag-Ju Cho, Rino Choi, Chang Hwan Choi, Mohammad S. Akbar, and Jack C. Lee, "Dynamic Positive Bias Temperature Instability Characteristics of Ultra-Thin HfO_2 NMOSFET," 2004 International Reliability Physics Symposium, p. 269, 2004.

171. C. S. Kang, C. Choi, C. Y. Kang, S. J. Rhee, Y. H. Kim, S. Akbar, J. Lee, "Advantage and Concerns of Si and N Incorporation", Sematech Gate Stack Workshop Digest, Sect. 1, p. 1, March 2004.

172. R. Choi, B. Lee, G. Brown, P. Zeitzoff, J. H. Sim, and J. C. Lee, “Polarity Dependence of Dielectrics Wearout Properties for Hf-based High-K Dielectrics,” Sematech Gate Stack Workshop Digest, Sect. 1, p. 4, March 2004.

173. C. Choi, C.S. Kang, C. Y. Kang, R. Choi, Y. Kim, S. J. Rhee, M. Akbar and J. Lee, “The Effects of Nitrogen and Silicon Profile on High-K MOSFET Performance and Bias Temperature Instability,” 2004 Symposium on VLSI Technology, p. 214, June 2004.

174. Y. Kim, R. Choi, R. Jha, J. H. Lee, V. Misra and J. Lee, “Effects of Barrier Height and the Nature of Bi-Layer Structure on the Reliability of High-K Dielectrics with Dual Metal Gate (Ru & Ru-Ta alloy) Technology,” 2004 Symposium on VLSI Technology, p. 138, June 2004.

175. Rino Choi, B. H. Lee, G. Brown, P. Zeitzoff, J. H. Sim, and J. C.Lee, "Polarity dependence of FN Stress induced degradation on NMOSFETs with Polysilicon Gate and HfSiON Gate Dielectrics," to be presented at the 11th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2004), p. 21, 2004.

176. Rino Choi, Byoung Hun Lee, K. Matthews, J. H. Sim, G. Bersuker, L. Larson and Jack C. Lee, "Relaxation of FN stress induced Vth shift at NMOSFETs with HfSiON Gate Dielectric and TiN Gate Electrode," 62nd annual Device Research Conference (2004 DRC), p. 14, 2004.

177. Se Jong Rhee, Chang Yong Kang, Young Hee Kim, Chang Seok Kang, Hag-Ju Cho, Rino Choi, Chang Hwan Choi, Mohammad S. Akbar, and Jack C. Lee, "Threshold Voltage Instability of Ultra-Thin HfO_2 NMOSFETs : Characteristics of Polarity Dependences," 62nd annual Device Research Conference (2004 DRC), p. 101, 2004.

178. Y. H. Kim, R. Choi, R. Jha, J.H. Lee, V. Misra, and J. C. Lee, “Reliability of High-K Dielectrics and Its Dependence on Gate Electrode and Interfacial / High-K Bi-Layer Structure” to be published at the 15th European Symposium on Reliability of Electronic Devices, Failure Physics and Analysis, October 2004.

179. C. Y. Kang, R. Choi, J. H. Sim, C. Young, B. H. Lee, G. Bersuker, and Jack C. Lee, “Charge Trapping Effects in HfSiON Dielectrics on the Ring Oscillator Circuit and the Single Stage Inverter Operation,” Technical Digest of International Electron Devices Meeting (IEDM), p. 485, December 2004.

180. Se Jong Rhee, Chang Seok Kang, Chang Hwan Choi, Chang Yong Kang, Siddarth Krishnan, Manhong Zhang, Mohammad S. Akbar and Jack C. Lee, “Improved Electrical and Material Characteristics of Hafnium Titanate Multi-metal Oxide n-MOSFETs with Ultra-Thin-EOT (~8Å) Gate Dielectric Application” Technical Digest of International Electron Devices Meeting (IEDM), p. 837, December 2004.

181. Se Jong Rhee, Chang Seok Kang, Chang Yong Kang, Chang Hwan Choi, Manhong Zhang, Siddarth Krishnan, Mohammad S. Akbar and Jack C. Lee "Charge Compensation Effect in Hafnium Titanate Multi-metal Oxide n-MOSFETs," IEEE Semiconductor Interface Specialists Conference, p. 50-51, 2004.

182. C. Choi, C. Y. Kang, S. Rhee, M. Akbar, S. Krishnan, M. Zhang and J. Lee, "A Suppression of Interfacial Oxide Formation by Oxygen-Scavenging Technique to Reduce EOT to < 0.7nm of "Undoped" HfO_2 / Si Gate Stacks" IEEE Semiconductor Interface Specialists Conference, 2004.

183. C. Y. Kang, R. Choi, B. H. Lee, G. Bersuker, and Jack C. Lee, "A Study of Charge Trapping Dynamics in HfSiON Dielectrics Using the Single Stage Inverter Circuit" IEEE Semiconductor Interface Specialists Conference, December 2004.

184. Invited Paper -Jack C. Lee , *C.* Kang, S. Rhee, C. Choi, S. Krishnan, I. Ok, M. Akbar, H. Kim, F. Zhu, M. Zhang, T. Lee, "Hafnium-based High-K Dielectrics" VLSI Technology (VLSI-TSA-Tech), 2005 IEEE VLSI-TSA International Symposium on Page(s):122 – 125, April 2005.

185. Invited Paper - Jack C. Lee, S. Rhee, C. Kang, C. Choi, S. Krishnan, I. Ok, M. Akbar, H. Kim, F. Zhu, M. Zhang, T. Lee, "Process Effects and Characterization of Hf-Based Dielectrics, "Electrochemical Society 207th meeting, May 2005.

186. M. S. Akbar, Naim Moumen, Joel Barnett, Byoung-Hun Lee, and Jack C. Lee, "Effects of High-k Post Deposition Cleaning in Improving CMOS Bias Instabilities and Mobility. A Potential Issue in Reliability of Dual Metal Gate Technology", IEEE International Reliability Physics Symposium, pp. 640, 2005.

187. C. Y. Kang, S. J. Rhee, C. H. Choi, M. S. Akbar, H. -S. Kim, M. Zhang, T. Lee, I. Ok, F. Zhu, and J. C. Lee, "Effects of Optimized Nitrogen Tailoring in High-k dielectrics on Impurity Penetration and Stress Induced Device Degradation", IEEE International Reliability Physics Symposium, p. 628, 2005.

188. Siddarth Krishnan, Jeff J. Peterson, Chadwin D. Young, George Brown, Rino Choi, Rusty Harris, Jang Hoan Sim, Peter Zeitzoff, Paul Kirsch, Jim Gutt, Hong Jyh Li, Ken Matthews, Jack C. Lee, Byoung Hun Lee, and Gennadi Bersuker "Dominant SILC mechanisms in HfO_2/TiN Gate nMOS and pMOS transistors", and, Proceedings of 43rd Annual IEEE International Reliability Physics Symposium, Page(s): 642 – 643, 2005.

189. Changhwan Choi, Chang Yong Kang, Se Jong Rhee, Mohammad Shahariar Abkar, Siddarth A. Krishna, Manhong Zhang, Hyungseob Kim, Tackhwi Lee, Feng Zhu, Injo Ok, Sergei Koveshnikov and Jack C. Lee, "Fabrication of TaN-gated Ultra-Thin MOSFETs (EOT <1.0nm) with HfO2 using a Novel Oxygen Scavenging Process for Sub 65nm Application" Symposium on VLSI Technology, Kyoto, Japan, p. 226, 2005.

190. J. Lee, “High-K Dielectrics – processes and reliability,” IEEE Solid-State Circuits Society Fort Collins, Aug. 5, 2005.

191. M. S. Akbar, Naim Moumen, Jeff Peterson, Joel Barnett, Muhammad Hussain and Jack C Lee, “Effect of Precursor Pulse Time on Charge Trapping and Mobility of ALD HfO_2”, 207th Electrochemical Society (ECS) Meeting, pp. 161, 2005.

192. Se Jong Rhee, Hyoung-Sub Kim, Chang Yong Kang, Chang Hwan Choi, Manhong Zhang, Feng Zhu, Tackhwi Lee, Injo Ok, Mohammad S. Akbar, Siddarth A. Krishnan, and Jack C. Lee, “Optimization and Reliability Characteristics of TiO_2/HfO_2 Multi-metal Dielectric MOSFETs” Symposium on VLSI Technology, Kyoto, Japan, p. 168, 2005.

193. Se Jong Rhee, Hyoung-Sub Kim, Chang Yong Kang, Chang Hwan Choi, M. S. Akbar, Manhong Zhang, Tackwhi Lee, Injo Ok, Feng Zhu, Siddarth A. Krishnan, and Jack C. Lee, "Structural Optimization and Electrical Characteristics of Ultra-thin Gadolinium (Gd_2O_3) Incorporated HfO_2 n-MOSFETs,” 63rd annual Device Research Conference (2005 DRC), p. 219, 2005.

194. Siddarth A. Krishnan, M.A. Quevedo-Lopez, Rino Choi, Paul Kirsch, Chadwin Young, Rusty Harris, Jeff J. Peterson, Hong-Jyh Li, Byoung Hun Lee and Jack C. Lee “Charge Trapping Dependence on the Physical Structure of Ultra-thin ALD-HfSiON/TiN Gate Stacks”, International Integrated Reliability Workshop (IIRW) proceedings, p. 89, October 2005.

195. Siddarth A. Krishnan, Manuel Quevedo, Rusty Harris, Paul D. Kirsch, Rino Choi, Byoung Hun Lee, Gennadi Bersuker, Jeff Peterson, Hong-Jyh Li, Chadwin Young and Jack C. Lee, “NBTI Dependence on Dielectric Thickness in Ultra-scaled HfSiO Dielectric/ALD-TiN Gate Stacks”, Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, p. 23, 2005.

196. J. Lee, “Future of High-K Dielectrics” (Invited Talk) Electron Device Society Mini-Colloquium at UCF, p. 31, February 23-25, 2006.

197. Chang Yong Kang, Jack Lee, “Carrier Recombination in High-k Dielectrics and its Impact on Transient Charge Effects in High-k Devices”, Advanced Gate Stack Engineering Working Group Biannual Meeting, March 2006.

198. Feng Zhu, C.Y Kang, S.J. Rhee, C.H. Choi, S.A. Krishnan, M. Zhang, H.S. Kim, T. Lee, I. Ok, G. Thareja, and J.C. Lee, "Improving carrier mobility and reliability characteristics of high-k NMOSFET by using stacked Y2O3/HfO2 gate dielectric", Proceedings of IEEE International Reliability Physics Symposium, p659, 2006.

199. C. Y. Kang, R. Choi, S. C. Song, C. D. Young, G. Bersuker, B. H. Lee, and J. C. Lee, "Carrier Recombination in High-k Dielectrics and its

Impact on Transient Charge Effects in High-k Devices", Proceedings of IEEE International Reliability Physics Symposium, p. 657, 2006.

200. J. Lee, (Invited Talk) “High-K Gate Dielectrics,” Symposium on VLSI Technology Short Course Series, Honolulu, HI, June 12-15, 2006.

201. InJo Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, G. Thareja, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee "Depletion-Mode MOSFET on n-GaAs substrate with HfO2 and Silicon Interface Passivation", IEEE Device Research Conference, pp. 45-46, 2006.

202. Feng Zhu, S. Koveshnikov, I. Ok, H.S. Kim,V. Tokranov, M. Yakimov, S. Oktyabrsky, W. Tsai and J. C. Lee, "Enhancement and Depletion-mode GaAs N-MOSFETs with stacked HfO2/Y2O3 gate dielectric", Digest of Device Research Conference, p. 83, 2006.

203. H.S. Kim, I. Ok, M. Zhang, T. Lee, F. Zhu, G. Tharaja, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee, “Germanium passivation for high-k dielectric III-V MOSFETs and temperature dependence of dielectric leakage current,” IEEE Device Research Conference, p. 87, 2006.

204. Tackhwi Lee; Se Jong Rhee; Chang Yong Kang; Feng Zhu; Manhong Zhang; Hyoung-sub Kim; Changhwan Choi; Injo Ok; Sergei Koveshnikov; Hokyung Park; Lee, J.C., “Improved MOSFET characteristics by Incorporating Laminated Dysprosium (Dy2O3) Dielectric into HfO2 Gate Stack,” IEEE Device Research Conference, Page(s): 69 – 70, June 2006.

205. H. Park, H. C. Wen, M. Chang, M. Jo, R. Choi, B. H. Lee, S.C. Song, C. Y. Kang, T. Lee, G. Brown, J. C. Lee and H. Hwang, “Thermal stability of metal electrodes and its impact on gate dielectric characteristics,” Solid State Devices Meeting, 2006.

206. Keynote Speech – Jack C. Lee, “MOS and MOSFET Structures on III-V Substrate with Interface Passivation Layer”, 3rd Annual International Symposium on Advanced Gate Stack Technology, September 2006.

207. Invited Paper - C.M. Osburn, S.A. Campbell, A. Demkov, E. Eisenbraun, E. Garfunkel, T. Gustafsson, A.I. Kingon, J. Lee, D.J. Lichtenwalner, G. Lucovsky, T.P. Ma, J.P. Maria, V. Misra, R.J. Nemanich, G.N. Parsons, D.G. Schlom, S. Stemmer, R.M. Wallace, and J. Whitten, "Materials and Processes for High k Gate Stacks: Results from the FEP Transition Center,", Electrochemical Society Transactions, 3(3), 389, October 2006.

208. Michael M. Oye, Davood Shahrjerdi, Jeffrey B. Hurst, Shannon D. Lewis, Sagnik Dey, David Q. Kelly, Sachin Joshi, Injo Ok, Terry J. Mattord, Jack C. Lee, Archie L. Holmes Jr., and Sanjay K. Banerjee, “Molecular-beam Epitaxy Growth of Ge and GaAs on

Silicon substrates for High-k III-V MOSFET applications," the 24th North American Conference on Molecular Beam Epitaxy, October 2006.

209. G. Thareja, J. Lee, A. V. Y. Thean, V. Vartanian, B. Y. Nguyen, "NBTI Reliability of Strained SOI MOSFETs," 32nd International Symposium for Testing and Failure Analysis, November 2006.

210. InJo Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee "Self-Aligned n- and p-channel GaAs MOSFETs on Undoped and P-type Substrates Using HfO_2 and Silicon Interface Passivation Layer", IEEE International Electron Devices Meeting, p. 829, 2006.

211. InJo Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, and Jack C. Lee "Metal Gate HfO2 MOS Structures on GaAs Substrate with SiGe Interface Passivation Layer", IEEE Semiconductor Interface Specialists Conference, 2006.

212. Feng Zhu, S. Koveshnikov, I. Ok, H.S. Kim, M. Zhang, V. Tokranov, M. Yakimov, S. Oktyabrsky, W. Tsai and J. C. Lee, "Investigation of charge trapping properties of high-κ on GaAs with silicon interface passivation layer", IEEE Semiconductor Interface Specialists Conference 2006.

213. M. H. Zhang, F. Zhu , I. J.Ok , H. S. Kim, L.Yu, M. Oye, J.Hurst, B. Cobb, S. Lewis, A. Holmes and Jack C. Lee, "Criticality of controlling oxygen incorporation into HfO_2/Si/GaAs gate stacks" IEEE Semiconductor Interface Specialists Conference 2006.

214. H.-S. Kim, I. Ok, M. Zhang, F. Zhu, L. Yu, T. Lee, and Jack C. Lee, "The Effects of Germanium Interfacial Passivation Layer Thickness on Electrical Characteristics of HfO_2 MOSCAP on GaAs Substrate" IEEE Semiconductor Interface Specialists Conference, p. 28, 2006.

215. H. J. Na, C. Krug, S. Joshi, D. Heh, R. D. Kirsh, R. Choi, B. H. Lee, R. Jammy, S. Banerjee, and J. Lee, "Improved Passivation and Characterization of Ge/HfSiO Interface Enabling Surface Channel Ge pFETs," IEEE Semiconductor Interface Specialists Conference, session 8, no. 3, 2006.

216. Invited Paper -- Jack C. Lee, "III-V Channel High-K MOSFETs" Technical Digest of SEMI Technology Symposium (STS) Korea, p. 285, January 31, 2007.

217. S. Joshi, C. Krug, D. Heh, H. Na, H. Harris, J. Oh, P. Kirsch, P. Majhi, B. Lee, H. Tseng, R. Jammy, J. Kee and S. Banerjee, "Improved Ge Surface Passivation with Ultrathin SiOx Enabling High Mobility Surface Channel PMOSFETs Featuring a HfSiO/WN Gate Stack," 37th Conference on the Physics and Chemistry of Semiconductor Interfaces, February 2007.

218. S. Koveshnikov, S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Moore, W. Tsai, F. Zhu, J.C. Lee, “Metal-Oxide-Semiconductor Field Effect Transistors with InGaAs and GaAs/InGaAs Channels and High-k Gate Dielectric,” Materials Research Society Symposium, San Francisco, April 2007.

219. J. Lee (Invited talk) "MOSCAP's and MOSFET's on III-V Channel Materials with Si, Ge and SiGe Interface Passivation Layer", Electrochemical Society Meeting, May 7, 2007.

220. J. Lee (Invited Talk) " III-V Channel Materials with Si, Ge and SiGe Interface Passivation Layer", Ohio State University Distinguished Lecture Series, May 24, 2007.

221. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee “Metal Gate – HfO_2 MOS Structures on InGaAs Substrate with Varying Si Interface Passivation Layers and PDA Conditions”, Conference on the Physics and Chemistry of Semiconductor Interfaces, 2007

222. Feng Zhu, Injo Ok, Hyoung-sub Kim, Manhong Zhang, Sung Il Park, Jung Hwan Yum and Jack C. Lee, “Investigation of the passivation mechanism of ultra-thin silicon interface layer for III-V MOS devices,” Conference on the Physics and Chemistry of Semiconductor Interfaces (PCSI) (2007).

223. S. Oktyabrsky, S. Koveshnikov, V. Tokranov, M. Yakimov, R. Kambhampati, H. Bakhru, F. Zhu, J. Lee, and W. Tsai, "InGaAs and GaAs/InGaAs Channel Enhancement Mode n-MOSFETs With HfO2 Gate Oxide and a-Si Interface Passivation Layer," Device Research Conference, June 19, 2007.

224. Hyoung-Sub Kim, Injo Ok, Feng Zhu, M. Zhang, S. Park, J. Yum, H. Zhao, and Jack C. Lee, “n- and p-channel TaN/HfO_2 MOSFETs on GaAs substrate using a germanium interfacial passivation layer,” *The 65th annual Device Research Conf.*, pp. 99, 2007.

225. Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee, “HfO_2-based Metal-Oxide-Semiconductor Capacitors on n-InGaAs Substrate with a Thin Germanium Passivation Layer,” *The International Conference on Compound Semiconductor Manufacturing Technology*, pp. 69, 2007.

226. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee “Hydrogen Incorporation of Metal Gate HfO_2 MOS Structures on $In_{0.2}Ga_{0.8}As$ Substrate with Si Interface Passivation Layer”, International Conference on Compound Semiconductor Manufacturing Technology, 2007.

227. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee, “Metal Gate HfO2 MOS

Structures on InGaAs Substrate with Varying Si Interface Passivation Layer and PDA Condition," J. Vac. Sci. Technol. B 25, Jul/Aug 2007.

228. Injo Ok, Hyung-sub Kim, Manhong Zhang, Feng Zhu, Sung-il Park, Junghwan Yum, Han Zhao and Jack C. Lee, "Post Metal Annealing Optimization of Self-Aligned n-channel GaAs MOSFETs Using HfO2 and Silicon Interface Passivation Layer," International Symposium on Advanced Gate Stack Technology, September 2007.

229. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, and Jack C. Lee, "Influence of the substrate orientation on the electrical and material properties of GaAs MOSFETs Using HfO2 and Silicon Interface Passivation Layer," Semiconductor Interface Specialists Conference (SISC), December 2007.

230. Manhong Zhang, I. Ok, H. Kim, F. Zhu, and J. Lee, "Mechanism of V_{fb} shift in SiO2 and Hf-based gate dielectric stacks by capping Gd2O3," Semiconductor Interface Specialists Conference (SISC), December 2007.

231. Tackhwi Lee, Jack C. Lee and Sanjay K. Banerjee, "Characterization of Dysprosium oxide (Dy_2O_3) incorporated HfO_2 gate oxide devices" Semiconductor Interface Specialists Conference (SISC), December 2007.

232. InJo Ok, H. Kim, M. Zhang, F. Zhu, H. Zhao, S. Park, J. Yum, Domingo Garcia, Prashant Majhi, N. Goel and W. Tsai, C.K. Gaspe, M.B. Santos, and Jack C. Lee, "Self-Aligned n-channel MOSFET on InP and In0.53Ga0.47As Using Physical Vapor Deposition HfO2 and Silicon Interface Passivation Layer." IEEE Device Research Conference, June 2008.

233. Manhong Zhang, Feng Zhu, In-Jo Ok, Hyoung- Kim, Han Zhao, Jack C. Lee "Mechanism of flatband voltage shift capping Me_2O_3 (Me=Gd, Y, Dy)", IEEE Device Research Conference June 2008.

234. Feng Zhu, Injo Ok, Hyoung-sub Kim, Manhong Zhang, Sung Il Park, Jung Hwan Yum, Han Zhao and Jack C. Lee, "Can GaAs MOS device match with its silicon counterpart in interface quality by using silicon interface passivation layer and HfO_2 gate oxide?" Electronic Materials Conference (EMC) (2008).

235. Jack Lee (Invited Paper), "$In_{0.53}Ga_{0.47}As$ n-MOSFETs with Si interface passivation layer and HfO_2 gate oxide" 5th International Symposium on Advanced Gate Stack Technology, Sep. 2008.

236. Feng Zhu, H. Zhao, I. Ok, H.S. Kim, M. Zhang, S. Park, J. Yum, S. Koveshnikov, V. Tokranov, M. Yakimov, S. Oktyabrsky, W. Tsai and Jack C. Lee, "Charge trapping and wearout characteristics of self-aligned enhancement-mode GaAs n-MOSFET with Si interface passivation layer and HfO_2 gate oxide", Compound Semiconductor IC Symposium (CSICS) 2008.

237. Feng Zhu, Han Zhao, H.S. Kim, I. Ok, J. Yum and Jack C. Lee, “The effects of silicon interface passivation layer thickness on device characteristics of InP enhancement-mode nMOSFETs with HfO_2 gate oxide”, IEEE SISC Semiconductor Interface Specialists Conference 2008

238. Feng Zhu, Han Zhao, H.S. Kim, I. Ok, J. Yum and Jack C. Lee, “A high performance enhancement-mode $In_{0.53}Ga_{0.47}As$ nMOSFET with directly sputtered HfO_2 gate oxide”, IEEE SISC Semiconductor Interface Specialists Conference 2008

239. H. Zhao, D. Shahrjerdi, F. Zhu, H.S. Kim, J. Yum, S. Banerjee and J. C. Lee “Atomic-layer-deposited Al_2O_3 gate dielectrics on InP using sulfur passivation”, 50th Electronic Materials Conference, (2008)

240. H. Zhao, D. Shahrjerdi, F. Zhu, H.S. Kim, J. Yum, S. Banerjee and J. C. Lee “ALD Al_2O_3 based MOSFETs on undoped and p-type $In_{0.53}Ga_{0.47}As$ substrates”, 39th IEEE Semiconductor Interface Specialists Conference, (2008)

241. H. Zhao, Y. Chen, J. Yum, Y. Wang, N. Goel, S. Koveshnikov, W. Tsai, and J. C. Lee, “HfO_2-Based $In_{0.53}Ga_{0.47}As$ MOSFETs (EOT≈10Å) Using Various Interfacial Dielectric Layers”, IEEE Device Research Conference, (2009)

242. Han Zhao, Jung Hwan Yum, Yen-Ting Chen, and Jack C Lee “$In_{0.53}Ga_{0.47}As$ n-MOSFETs with ALD Al_2O_3, HfO_2 and $LaAlO_3$ gate dielectrics”, 36th Conference on the Physics and Chemistry of Semiconductor Interfaces, (2009)

243. Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "$In_{0.53}Ga_{0.47}As$ MOSFETs with CF4 plasma treatment and Al_2O_3 gate oxide", International Symposium on Advanced Gate Stack Technology (ISAGST), August 2009

244. Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, and Jack C. Lee, "Atomic-layer-deposited HfO_2 gate dielectrics on InP using silicon interface passivation layer" Electronic Materials Conference (EMC) 2009

245. Han Zhao, Yen-Ting Chen, Jung Hwan Yum, and Jack C Lee “Channel Doping Concentration and Thickness Dependence of Device Performance for $In_{0.53}Ga_{0.47}As$ n-MOSFETs with ALD Al_2O_3 dielectrics”, 2009 Materials Research Society Spring Meeting

246. Han Zhao, and Jack C Lee, “Self-aligned $In_{0.53}Ga_{0.47}As$ MOSFETs with Atomic Layer Deposited Al_2O_3, ZrO_2, and Stacked Al_2O_3/ZrO_2 Gate Dielectrics”, 2009 International Conference on IC Design and Technology

247. J. Lee (Invited Paper) “High-K III-V MOSFETs” 1st International Symposium on Integrated Ferroelectrics and Functionalities ($ISIF^2$), in Colorado Springs, CO, September 27-30, 2009

248. J. Lee, H. Zhao, Y. Chen, J. Yum, F. Xue, F. Zhou and Y. Wang, (Invited Paper) “High Performance InGaAs MOSFETs with High Mobility using InP Barrier Layer" 216th Electrochemical Society Meeting (E10 - ULSI Process Integration) in Vienna, Austria, October 2009.

249. J. Huang, N. Goel, H. Zhao, C. Y. Kang, K.S. Min, G. Bersuker, S. Oktyabrsky, S. Koveshnikov, Jack C. Lee, P. Majhi, W. Tsai, P. D. Kirsch, H. H. Tseng and R. Jammy, “InGaAs MOSFET Performance and Reliability Improvement by Simultaneous Reduction of Oxide and Interface Charge in ALD (La)AlO_x/ZrO_2 Gate Stack”, IEEE International Electron Devices Meeting IEDM 13.5, 2009

250. K.S. Min, C.Y. Kang, C. Park, C.S. Park, B. J. Park, J. B. Park, M. M. Hussain, Jack C. Lee, B. H. Lee, P. Kirsch, H-H, Tseng, R. Jammy, and G. Y. Yeom, “A Novel Damage-Free High-k Etch Technique Using Neutral Beam Assisted Atomic Layer Etching (NBALE) for sub-32nm Technology Node Low Power Metal Gate/High-K Dielectric CMOSFETs” IEEE International Electron Devices Meeting IEDM 17.4, 2009.

251. Han Zhao, Ning Kong, Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, Sanjay K. Banerjee and Jack C. Lee, “Effects of InP barrier layer thicknesses and different ALD oxides on device performance of $In_{0.7}Ga_{0.3}As$ MOSFETs”, IEEE Device Research Conference, (2010).

252. H. Zhao, N. Goel, J. Huang, Y. Chen, J. Yum, Y. Wang, F. Zhou, F. Xue, and J. Lee, “Factors Enhancing $In_{0.7}Ga_{0.3}As$ MOSFETs and Tunneling FETs Device performance” IEEE Device Research Conference, (2010).

253. (Invited Paper) Jack Lee, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, “Investigation of III-V n-MOSFETs with ALD high-k gate oxides”, 4th International Workshop on High-k dielectrics on High Carrier Mobility Channel Materials, (2010)

254. Y. Wang, H. Zhao, Y. Chen, F. Xue, F. Zhou, and J. Lee, "Atomic-Layer-Deposition HfO2Based InP n-Channel MOSFETs Using Different Thicknesses of Al2O3 as Interfacial Passivation Layer", Electrochemical Society (ECS) Transactions, Vol. 33, 487, Oct. 2010.

255. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou and Jack C. Lee, “Investigation of surface channel InGaAs MOSFETs with Al_2O_3 and ZrO_2 ALD Gate Dielectric”, Electrochemical Society Transactions. 33(3), 487, (Oct. 2010)

256. [Best Student Paper Award] F. Xue, H. Zhao, Y. Chen, Y. Wang, F. Zhou and J. Lee, "InAs and $In_{0.7}Ga_{0.3}As$ buried channel MOSFETs with ALD gate dielectrics" 41th IEEE Semiconductor Interface Specialists Conference, (Dec. 2010)

257. F. Xue, H. Zhao, Y. Chen, Y. Wang, F. Zhou and J. Lee "Investigation of ALD Al_2O_3 and ZrO_2 Gate Dielectric InGaAs Surface Channel MOSFETs with Large EOT Range" 2010 Materials Research Society Fall Meeting, Nov. 2010.

258. (Invited paper) J. C. Lee, H. Zhao, Y. Chen, Y. Wang, F. Xue, and F. Zhou, "Buried-channel $In_{0.7}Ga_{0.3}As$ MOSFETs and vertical $In_{0.7}Ga_{0.3}As$ tunneling FETs for beyond CMOS applications," Electrochemical Society (ECS) Transactions, Vol. 33, Oct. 2010.

259. Yen-Ting Chen, Han Zhao, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Improved Electrical Performance of Fluorinated HfO2 dielectrics on In0.53Ga0.47As MOSFETs" Materials Research Society (MRS) November 2010.

260. Y. Wang, Y. Chen, H. Zhao, F. Xue, F. Zhou, and J. Lee, "Improved Electrical Characteristics of ALD HfO2, Al2O3 Based n-Channel MOSFETs on InP Substrate with Postgate SF_6 Plasma Treatment ", IEEE Semiconductor Interface Specialists Conference, Dec. 2010.

261. (Invited Keynote Speaker) Jack C Lee, "High-K Dielectrics / High-Mobility Channel MOSFETs," SEMINATEC Workshop, Campinas, Brazil, March 24-25, 2011.

262. Yen-Ting Chen, Han Zhao, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "ZrO2-based InP MOSFETs (EOT = 1.2nm) Using Various Interfacial Dielectric Layers", the Electrochemical Society (ECS) the 219th meeting May 2011.

263. J. Huang, N. Goel, P. Lysaght, D. Veksler, P. Nagaiah[a], S. Oktyabrsky, , J. Price, H. Zhao, Y.T. Chen, J. C. Lee, J. C. Woicik, P. Majhi, P. D. Kirsch, and R. Jammy, "Detailed High-k/$In_{0.53}Ga_{0.47}As$ Interface Understanding to Enable Improved $In_{0.53}Ga_{0.47}As$ Gate Stack Quality" 2011 VLSI-TSA Symposium, June 2011.

264. Luca Morassi, Giovanni Verzellesi, Paolo Pavan, Dmitry Veksler, Injo Ok, Han Zhao, Jack C. Lee and Gennadi Bersuker, "Experimental/numerical investigation of buried-channel InGaA MOS-HEMTs with Al_2O_3 gate dielectric," IPRM 2011 --- 23th International Conference on Indium Phosphide and Related Materials, Berlin, Germany, May 2011.

265. L. Morassi, G. Verzellesi, P. Pavan, D. Veksler, I. Ok, H. Zhao, J.C. Lee, G. Bersuker, "Experimental/numerical investigation of buried-channel InGaAs MOS-HEMTs with Al_2O_3 gate dielectric", Proc. of the 23th International Conference on Indium Phosphide and Related Materials (IPRM 2011), Berlin (Germany), May 2011, pp. 103-105.

266. L. Morassi, G. Verzellesi, L. Larcher, H. Zhao, J.C. Lee, "Errors affecting split-CV mobility measurements in InGaAs MOS-HEMTs", Proc. of the 23th International

Conference on Indium Phosphide and Related Materials (IPRM 2011), Berlin (Germany), May 2011, pp. 327-329.

267. T. Akyol, J. H. Yum, D. A. Ferrer, M. Lei, M. Downer, C. W. Bielawski, T. W. Hudnall, G. Bersuker, J. Lee and S. Banerjee, "Introduction of ALD Beryllium Oxide Gate Dielectric for III-V MOS Devices," Device Research Conference, Santa Barbara, 2011.

268. Hao Tang, Patrice Rannou, Ryan A. Mesch, Lei Zhu, Edward T. Yu, Jack C. Lee, and C. Grant Willson, "Mobility Enhancement in Mesophases of Liquid Crystalline Organic Semiconductors," Organic Microelectronics & Optoelectronics Workshop VII in San Francisco, July 18-20, 2011.

269. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee, "In0.7Ga0.3As tunneling field-effect-transistors with LaAlO3 and ZrO2 high-k dielectrics", Electrochemical Society meeting (2011).

270. (Invited Paper) Jack C. Lee, F. Xue, Y. Chen, Y. Wang, and F. Zhou, "High-K Dielectrics / High-Mobility Channel MOSFETs" Electrochemical Society meeting (2011).

271. Y. Wang, H. Zhao, Y. Chen, F. Xue, F. Zhou, and J. Lee, "SF_6 plasma treated high k dielectrics engineering on InP metal-oxide-semiconductor field-effect-transistors", 220th ECS Meeting, October 2011, Boston, MA.

272. J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, J. C. Lee and S. K. Banerjee, "ALD Beryllium Oxide as a High-k Gate Dielectric for III-V MOS Devices," Session A-44, the 2011 Atomic Layer Deposition Conference.

273. J. Yum, "ALD Beryllium Oxide: Novel Barrier Layer for High Performance Gate Stacks on Si and High Mobility Substrates," IEEE International Electron Devices Meeting Technical Digest, p. 638-641, 2011.

274. F. Xue, Y. Chen, Y. Wang, F. Zhou, B. Fowler, and J. Lee, "The Effect of Plasma Treatment on Reducing Electroforming Voltage of Silicon Oxide RRAM", 221st ECS Meeting in Seattle, Washington (May 6 -10, 2012).

275. Y. T. Chen, J. Huang, J. Price, P. Lysaght, D. Veksler, C. Weiland, J. C. Woicik, G. Bersuker, R. Hill, J. Oh, N. Goel, P. D. Kirsch, R. Jammy, and J. C. Lee, "III-V Gate Stack Interface Improvement to Enable High Mobility 11nm node CMOS", International Symposium on VLSI Technology, Systems and Applications, Hsin-Chu, R.O.C., 2012.

276. Yao-Feng Chang, Yen-Ting Chen, Fei Xue, Yanzhen Wang, Fei Zhou, Burt Fowler, and Jack C. Lee, "Study of SiOx-based Complementary Resistive Switching Memristor", Device Research Conference, June 18-20 (2012).

277. Y. Wang, Y. Chen, F. Xue, F. Zhou, and J. Lee, "MOSFETs on InP substrate with $LaAlO_3/HfO_2$ bilayer of different $LaAlO_3$ thickness and single $La_xAl_{1-x}O$ layer with different La doping level", 222th ECS meeting (Honolulu HI, Oct. 2012).

278. (Invited talk) Jack Lee, Fei Xue, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Yao-Feng Chang and Jack Lee, "Excellent Device performance of III-V Channel Field-Effect-Transistors with High-k Gate Dielectrics," Technical Digest of World Congress of Nano-Science and Technologies, Qingdao, China September 2012.

279. Mina J. Hanna, Han Zhao, and Jack C. Lee, "Hysteresis-like effect in AlGaN/GaN MISFETs with SiN gate dielectric," International workshop on nitride semiconductors, Sapporo, Japan, Oct. 2012.

280. X. Sun, N. Xu, F. Xue, A. Alian, F. Andrieu, B.Y. Nguyen, T. Poiroux, O. Faynot, J. Lee, S.Cui and T. P .Ma, "AC Transconductance: A Novel Method to Characterize Oxide Traps in Advanced FETs without a Body Contact" IEEE International Electron Devices Meeting (IEDM), p.19.4.1-19.4.4, Dec. 2012.

281. Fei Xue, Aiting Jiang, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Yaofeng Chang and Jack Lee, "Excellent Device performance of 3D $In_{0.53}Ga_{0.47}As$ Gate-Wrap-Around Field-Effect-Transistors with High-k Gate Dielectrics," IEEE International Electron Devices Meeting (IEDM), p.27.5.1-27.5.4, Dec. 2012.

282. Yao-Feng Chang, Yen-Ting Chen, Fei Xue, Yanzhen Wang, Fei Zhou, Pai-Yu Chen, Burt Fowler, and Jack C. Lee, "Study of device architecture and multilevel characteristics in SiOx-based resistive switching memory", IEEE Semiconductor Interface Specialists Conference, December 6-8 (2012).

283. Yao-Feng Chang, Pai-Yu Chen, Burt Fowler, Yen-Ting Chen, Fei Xue, Yanzhen Wang, Fei Zhou, and Jack C. Lee, "Study of ambient effect in active SiOx-based resistive switching memory", International Symposium on VLSI Technology, Systems and Applications, April 22-24 (2013).

284. Yao-Feng Chang, Ying-Chen Chen, Ji Li, Fei Xue, Yanzhen Wang, Fei Zhou, Burt Fowler and Jack C. Lee, "Comprehensive Trap-Level Study in SiOx-based Resistive Switching Memory", Device Research Conference, June 23-26 (2013).

285. Yao-Feng Chang, Li Ji, Pai-Yu Chen, Fei Zhou, Fei Xue, Burt Fowler, Edward T. Yu, Jack C. Lee, "Study of SiO_x-Based Resistive Switching Memory by Nano-Sphere Lithography", IEEE Semiconductor Interface Specialists Conference, December 5-7 (2013).

286. Li Ji, Yao-Feng Chang, Ying-Chen Chen, Fei Zhou, Tsung-Ming Tsai, Kuan-Chang Chang, Min-Chen Chen, Ting-Chang Chang, Burt Fowler, Jack C. Lee, Edward T. Yu, "Optimization of High Density One Diode - One Resistor Architecture in Nano-Pillar SiO_x-Based Resistive Switching Memory by Nano-Sphere Lithography", *Materials Research Society Spring Meeting*, April 21-25 (2014).

287. Yao-Feng Chang, Li Ji, Ying-Chen Chen, Fei Zhou, Tsung-Ming Tsai, Kuan-Chang Chang, Min-Chen Chen, Ting-Chang Chang, Burt Fowler, Edward T. Yu and Jack C. Lee, "High-density nano-pillar SiOx-based resistive switching memory using nano-sphere lithography to fabricate a one diode - one resistor (1D-1R) architecture", IEEE International Symposium on VLSI Technology, Systems and Applications, April 28-30 (2014).

288. (Invited Paper) Fei Zhou, Fei Xue, Yao-Feng Chang and Jack Lee, "III-V Gate-Wrap-Around Field-Effect-Transistors with High-k Gate Dielectrics," Device Research Conference, June 22-25, 2014.

289. Yao-Feng Chang, B. Fowler, Y. Chen, L. Ji, F. Zhou and Jack Lee, "The Voltage-Triggered SET Mechanism and Self-Compliance Characteristics in Intrinsic Unipolar SiO_x-Based Resistive Switching Memory," Device Research Conference, June 22-25, 2014.

290. Fei Zhou, Yao-Feng Chang, Burt Fowler, and Jack C. Lee, "Characteristics of PECVD SiO_xN_{1-x} for Resistive Memory Application" International Conference on Metallurgical Coatings & Thin Films, April 28 - May 2 (ICMCTF 2014).

291. Fei Zhou, Yao-Feng Chang, Burt Fowler, and Jack C. Lee, "Discussion on Backward Voltage Sweep Set Effect in SiO_x Resistive Memory" 32nd International Conference on the Physics of Semiconductors (ICPS 2014), August 10-15.

292. Yao-Feng Chang, Burt Fowler, Li Ji, Ying-Chen Chen, Fei Zhou, Edward T. Yu, and Jack C. Lee, "Comprehensive Study of Intrinsic Unipolar SiO_x-Based RRAM Characteristics and Self-Compliance Characteristics in High-Density Nano Pillar-Type 1D-1R Architecture" 32nd International Conference on the Physics of Semiconductors (ICPS 2014), August 10-15.

293. Li Ji, Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Tsung-Ming Tsai, Kuan-Chang Chang, Min-Chen Chen, Ting-Chang Chang, Simon M. Sze, Edward T. Yu, and Jack C. Lee, "Resistive Switching of SiO_X with One Diode-One Resistor Nanopillar Architecture Fabricated via Nanosphere Lithography", IEEE Device Research Conference, June 22-25 (2014).

294. Li Ji, Martin D. McDaniel, Li Tao, Xiaohan Li, Agham B. Posadas, Yao-Feng Chang, Alexander A. Demkov, John G. Ekerdt, Deji Akinwande, Rodney S. Ruoff, Jack C. Lee and Edward T. Yu, "Atomic Scale Engineering of Metal-Oxide-Semiconductor Photoelectrodes for Energy Harvesting Application Integrated with Graphene and

Epitaxy SrTiO3," 2014 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, December 15th-17th, 2014.

295. Yao-Feng Chang, Burt Fowler, Fei Zhou, Kwangsub Byun, Jack C. Lee, "Study of SiOx-Based Resistive Switching Memory (ReRAM) in Integrated One Diode – One Resistor (1D-1R) Architecture" IEEE Semiconductor Interface Specialists Conference (SISC), December 10-13 (2014).

296. (Invited Talk) J. Lee, "Advantages and Challenges of FinFET Devices and Technologies," Northern California Chapter American Vacuum Society Conference, Sept. 25, 2014.

297. K. Byun, F. Zhou, B. Fowler, Y.F. Chang, and J.C. Lee "Electrical characteristics of Si nanocrystal filament in unipolar SiO_x based RRAM," 45th IEEE Semiconductor Interface Specialists Conference (SISC), Dec. 2014.

298. Yao-Feng Chang, Burt Fowler, Fei Zhou, Kwangsub Byun, Jack C. Lee, "Study of SiOx-Based Resistive Switching Memory (ReRAM) in Integrated One Diode – One Resistor (1D-1R) Architecture" 45th IEEE Semiconductor Interface Specialists Conference (SISC), December 10-13 (2014).

299. Yao-Feng Chang, Burt Fowler, Fei Zhou, Kwangsub Byun, Jack C. Lee, "Understanding Electroforming and Resistive Switching in Silicon Dioxide Resistive Memory Devices" American Physical Society (APS) March Meeting 2015.

300. Yao-Feng Chang, Burt Fowler, Fei Zhou, Kwangsub Byun, and Jack C. Lee, "Comprehensive study of intrinsic unipolar SiO_x-based ReRAM characteristics and resistive switching mechanism in TiW/SiO_x/TiW structure" International Symposium on VLSI Technology, Systems and Applications (2015 VLSI-TSA) April 2015.

301. [Best Student Papers Award] Yao-Feng Chang, Burt Fowler, Fei Zhou, Jack C. Lee, "Study of SiOx-Based Resistive Switching Memory (ReRAM) in Integrated One Diode – One Resistor (1D-1R) Architecture," 4th International Symposium on Next-Generation Electronics (IEEE ISNE 2015) at National Taiwan University of Science and Technology in Taipei, Taiwan from May 4-6, 2015.

302. (Invited Talk) Yao-Feng Chang, Burt Fowler, Fei Zhou, and Jack C. Lee, "The Intrinsic Unipolar SiO_x-based Resistive Switching Memory: Characterization, Mechanism and Applications" ECS Fall Meeting (2015).

303. (Invited Talk) Yao-Feng Chang, "Intrinsic Unipolar SiO_x-Based Resistive Switching Memory: Characterization, Mechanism and Applications" International Symposium on Next-Generation Electronics, Taipei, Taiwan, May 4 - 6 (2015).

304. Kwangsub Byun, Ying Wang, Bruce Adams, Jack Lee, "Laser Curing and Ink-Jet Processes for Fabricating SiOx RRAM Structures," 43rd International Conference on the Physics and Chemistry of Surfaces & Interfaces (PCSI-43), 2016.

305. (Best Paper Award Finalist) Ying-Chen Chen, Yao-Feng Chang, Burt Fowler, Fei Zhou, Xiaohan Wu, Cheng-Chih Hsieh, Heng-Lu Chang, Chih-Hung Pan, Min-Chen Chen, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, and Jack C. Lee, "Comprehensive Study of Intrinsic Unipolar SiO_x-Based ReRAM Characteristics in AC Frequency Response and Low Voltage (< 2V) Operation" International Symposium on VLSI Technology, Systems and Applications (VLSI- TSA) 2016.

306. Ying-Chen Chen, Yao-Feng Chang, Xiaohan Wu, MeiqiGuo, Fei Zhou, Burt Fowler, Jack C Lee, "Characterization of SiOx/HfOx bilayer Resistive-Switching Memory Devices," *Electrochemical Society (ECS) Meeting*, 2016.

307. Meiqi Guo, Ying-Chen Chen, Yao-Feng Chang, Xiaohan Wu, Burt Fowler, Yonggang Zhao and Jack C. Lee, "Characteristics of Electrically Driven Metal-Insulator-Transition (E-MIT) in Nb-doped SrTiO3 and HfO2-based Selector Devices," Device Research Conference (DRC) (2016).

308. Fei Zhou, Ying-Chen Chen, Xiaohan Wu, MeiqiGuo, Burt Fowler, Jack Lee "The Role of Oxygen Deficiency in SiO_x Based Resistive Memory," *International Conference on Metallurgical Coatings and Thin Films (ICMCTF)*, 2016.

309. (Invited) Ying-Chen Chen, Xiaohan Wu, MeiqiGuo, Fei Zhou, Yao-Feng Chang, Burt Fowler, Chih-Hung Pan, Ting-Chang Chang, Jack C Lee, "Memcomputing (Memristor+ Computing) in Intrinsic SiOx-Based Resistive Switching Memory", 230th Meeting of The Electrochemical Society (2016).

310. Ying-Chen Chen, Xiaohan Wu, Meiqi Guo, Fei Zhou, Yao-Feng Chang**, Burt Fowler, Chih-Hung Pan, Ting-Chang Chang, and Jack C. Lee, "Memcomputing (Memristor + Computing) in Intrinsic SiO_x-Based Resistive Switching Memory" PRiME 2016 (Invited Talk).

311. (Best Student Paper Award) Chih-Yang Lin, Ying-Chen Chen, Meiqi Guo, Chih-Hung Pan, Fu-Yuan Jin, Cheng Chih Hsieh, Xiaohan Wu, Min-Chen Chen, Yao-Feng Chang, Fei Zhou, Burt Fowler, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, Yonggang Zhao, Simon M. Sze, Sanjay Banerjee, Jack C. Lee, "A Universal Model for Interface-type Threshold Switching Phenomena by Comprehensive Study of Vanadium Oxide-Based Selector", International Symposium on VLSI Technology, Systems and Applications (2017 VLSI-TSA), Hsinchu, Taiwan, April 24-27, (2017).

312. Sungjun Kim, Yao-Feng Chang*, Ying-Chen Chen, Byung-Gook Park, and Jack C. Lee, "Resistive Switching Characteristics and Mechanisms in Silicon Oxide and Silicon Nitride Memristors", China RRAM International Workshop (2017).

313. Y.-C. Chen, YF Chang, CY Lin, X Wu, G Xu, B Fowler, TC Chang, JC Lee, "Built-in Nonlinear Characteristics of Low Power Operating One-Resistor Selector-Less RRAM By Stacking Engineering", 232nd Meeting of The Electrochemical Society (2017).

314. Jia Chen, Sungjun Kim, Ying-Chen Chen, Min-Hwi Kim, Yi Li, Xiang-Shui Miao, Yao-Feng Chang, Byung-Gook Park, Jack C. Lee, "Synaptic Properties Considering Temperature Effect in HfOx-Based Memristor – Demonstration of Homo-thermal Synaptic Behaviors", International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA) (2018).

315. Ying-Chen Chen, Xiaohan Wu, Yao-Feng Chang, Jack C Lee, "Nonlinearity Enhancement by Positive Pulse Stress in Multilevel Cell Selectorless RRAM Applications", 76th Device Research Conference (DRC). 2018.

316. Y.-C. Chen, C.-Y. Lin, Y.-F. Chang, T.-C. Chang, J. Lee, "Selector-Less Graphite Memristor: Intrinsic Nonlinear Behavior with Gap Design Method for Array Applications," 233rd Meeting of The Electrochemical Society (2018).

317. Ruijing Ge, Xiaohan Wu, Myungsoo Kim, Po-An Chen, Jianping Shi, Junho Choi, Xiaoqin Li, Yanfeng Zhang, Meng-Hsueh Chiang, Jack C. Lee and Deji Akinwande, "Atomristors: Memory Effect in Atomically-thin Sheets and Record Solid-state RF Switches," IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, December 1-5, 2018.

318. Ying-Chen Chen, Chih-Yang Lin, Yao-Feng Chang and Jack C. Lee, "Energy Efficient Nonlinear Selectorless RRAM by Current Sweep Operation for Crossbar Array Applications," IEEE Semiconductor Interface Specialists Conference (SISC), San Diego CA, December 5-8, 2018.

319. Ying-Chen Chen, Szu-Tung Hu, Chao-Cheng Lin, Jack C. Lee, "Resistive Switching Early Failure and Gap Identification in Bilayer Selectorless RRAM Applications" 77th Device Research Conference (DRC), 2019.

320. Y.C. Chen, C.Y. Lin, H.C. Huang and J. C. Lee "Energy Efficient Operation Schemes of Nonlinear Selectorless RRAM for Crossbar Array Applications" 61st Electronic Materials Conference (EMC), 2019.

321. Ying-Chen Chen, Chao-Cheng Lin, Sungjun Kim, Yao-Feng Chang, Jack Lee, "Non-Uniform Dielectric Selectorless Resistive Switching Memory and Reliability Determination for Low Power Array Applications" 235th Meeting of The Electrochemical Society, 2019.

322. Xiaohan Wu, Ruijing Ge, Po-An Chen, Meng-Hsueh Chiang, Deji Akinwande, Jack C. Lee, "Non-Volatile Resistance Switching Phenomenon in Monolayer h-BN", 236th Electrochemical Society ECS Meeting, 2019. (Invited talk)

323. Myungsoo Kim, Emiliano Pallecchi, Ruijing Ge, Xiaohan Wu, Vanessa Avramovic, Etienne Okada, Jack C. Lee, Henri Happy, and Deji Akinwande, "Non-volatile RF and mm-wave Switches based on monolayer hBN" International Electron Devices Meeting (IEDM) Dec. 2019.

324. Saban Hus, Ruijing Ge, Xiaohan Wu, Yuqian Gu, Jack C Lee, An-Ping Li, Deji Akinwande, "Atomic Level Investigation of Resistance Switching in 2D Memory Devices", 235th Electrochemical Society ECS Meeting. 2019.

325. Xiaohan Wu, Ruijing Ge, Deji Akinwande and Jack C. Lee, "Non-volatile resistance switching behavior in monolayer two-dimensional materials", Electronic Materials Conference EMC 2020.

326. Y. Huang, X. Wu, R. Ge, D. Akinwande, J. C. Lee, "Modeling of temperature distribution in 2D MoS2-based non-volatile resistance switching devices," *51st IEEE Semiconductor Interface Specialists Conference (SISC)*, 2020.

327. Xiaohan Wu, Ruijing Ge, Deji Akinwande and Jack C. Lee, "Understanding of Multiple Resistance States by Current-sweep Measurement and Compliance Current Modulation in 2D MoS2-based Non-volatile Resistance Switching Devices", Device Research Conference DRC 2020.

328. Xiaohan Wu, Ruijing Ge, Myungsoo Kim, Deji Akinwande and Jack C. Lee, "Atomristors: Non-volatile Resistance Switching in 2D monolayers", Proceedings of the 2020 Pan Pac Microelectronics Symposium.

329. Xiaohan Wu, Ruijing Ge, Deji Akinwande and Jack C. Lee, "Non-volatile Resistance Switching in Monolayer 2D Atomic Sheets", Electronic Materials Science Nov. 5-7, 2020.

330. Xiaohan Wu, Ruijing Ge, Myungsoo Kim, Deji Akinwande and Jack C. Lee, "The Applications of 2D Monolayer-based Atomristors in Non-volatile Memory, RF switches and Neuromorphic Computing", MRS Spring/Fall Meeting, Nov. 27-Dec. 5, 2020.

331. Xiaohan Wu, Ruijing Ge, Myungsoo Kim, Deji Akinwande and Jack C. Lee, "Atomristors: Non-volatile Resistance Switching Behavior in 2D Monolayers and the Applications in Memory, RF Switch and Neuromorphic Computing", TechConnect World Innovation Conference, June 12-14, 2021.

332. Yao-Feng Chang, Ilya Karpov, Reed Hopkins, David Janosky, Jacob Medeiros, Benjamin Sherrill, Jiahan Zhang, Yifu Huang, Tanmoy Pramanik, Albert Chen, Tony Acosta, Abdullah Guler, James A O'Donnell, Pedro A Quintero, Nathan Strutt, Oleg Golonzka, Chris Connor, Jack C Lee, Jeffrey Hicks, "A Comprehensive Study of Enhanced Characteristics with Localized Transition in Interface-type Vanadium-based Devices" International Reliability Physics Symposium (IRPS), March 21- March 24, (2021).

333. Xiaohan Wu, Ruijing Ge, Yuqian Gu, Saban M. Hus, Jack C. Lee and Deji Akinwande "A Library of Atomristors: Non-Volatile Resistive Switching Phenomenon in 2D Atomic Sheets", Device Research Conference *2021*. (Invited talk)

334. Xiaohan Wu, Ruijing Ge, Yuqian Gu, Emmanuel Okogbue, Jianping Shi, Abhay Shivayogimath, Peter Bøggild, Timothy J. Booth, Yanfeng Zhang, Yeonwoong Jung, Jack C. Lee and Deji Akinwande "Universal Non-Volatile Resistive Switching Behavior in 2D Metal Dichalcogenides Featuring Unique Conductive-Point Random Access Memory Effect", Electron Devices Technology and Manufacturing Conference (EDTM) 2021.

335. Xiaohan Wu, Ruijing Ge, Myungsoo Kim, Deji Akinwande and Jack C. Lee "Atomristors: Non-volatile Resistance Switching Behavior in 2D Monolayers", *TechConnect World Innovation Conference 2021*.

336. Xiaohan Wu, Ruijing Ge, Deji Akinwande and Jack C. Lee "Toward Universal 2D Memory: Conductive-Point Resistive Switching in Non-Metallic Atomic Layers", *Electronic Materials Conference June 23-25, 2021*.

337. Y. Huang, X. Wu, Y. Gu, R. Ge, J. Zhang, Y. F. Chang, D. Akinwande, and J. C. Lee, "Monte Carlo and Circuit-Level Simulation of 2D Memristors for Neuromorphic Computing", *2021 IEEE 16th Nanotechnology Materials and Devices Conference (NMDC)*, 1-5, 2021.

338. Y. Huang, Y. Gu, X. Wu, R. Ge, Y.-F. Chang, X. Wang, J. Zhang, D. Akinwande and J. C. Lee, "ReSe2-based RRAM and Circuit-level Model for Neuromorphic Computing", *Frontiers in Nanotechnology*, 89, 2021.

339. Y. Huang, X. Wu, Y. Gu, R. Ge, J. Zhang, Y.-F. Chang, D. Akinwande and J. C. Lee. "2D ReSe2 RRAM and Analog Model for Neuromorphic Computing". *52nd IEEE Semiconductor Interface Specialists Conference (SISC)*, 2021.

PATENTS ISSUED

1. B. Doyle and J. Lee, "Method for Forming a High Dielectric Constant Insulator in the Fabrication of an Integrated Circuit, " (issued April 6, 1999, US 5,891,798)
2. M. Gardner, M. Gilmer, J. Fulford and J. Lee, "Semiconductor Device Having a Tri-Layer Gate Insulating Dielectric," (issued May 2000, US 6,057,584)
3. M. Gardner, J. Fulford and J. Lee, "Semiconductor Having a PMOS Device Having Source/Drain Region Formed using a Heavy Atom P-type Implant and Method of Manufacturing Thereof," (issued January 11, 2000, US 6,013,546).
4. M. Gardner, J. Fulford and J. Lee, "Semiconductor Device with Asymmetric PMOS Source/Drain Implant and Method of Manufacture Thereof" (issued Nov. 14, 2000, US 6,146,934)
5. B. Doyle and J. Lee, "Method for Forming a High Dielectric Constant Insulator in the Fabrication of an Integrated Circuit" (issued Oct. 2001, US6,306,742)

6. Jack Lee and Han Zhao, “Tunnel Field Effect Transistor (TFET) with Lateral Oxidation,” (issued Mar. 26, 2016, US 9,293,591).
7. Jack Lee and Han Zhao, “Tunnel Field Effect Transistor (TFET) with Lateral Oxidation,” (issued Dec. 26, 2017, US 9,853,135).
8. Jack C. Lee and Fei Xue, “Three-Dimensional Gate-Wrap-Around Field Effect Transistor” (issued June 2, 2015, US 9,048,330)
9. Jack C. Lee and Fei Xue, “Vertical III-V Nanowire Field-Effect Transistor Using Nanosphere Lithography,” (issued Dec. 8, 2015, US 9,209,271).
10. Deji Akinwande, Xiaohan Wu, Ruijing Ge and Jack C. Lee, Non-volatile Resistance Switching in Monolayer Atomic Sheets. *Serial No. 62/548,295, Aug. 2017*

Book / Book Chapters

1. Xiaohan Wu, Ruijing Ge, Deji Akinwande, Jack C. Lee “Memristors based on 2D monolayer materials”, Memristors. Published by Intech 2021.

2. Ruijing Ge, Xiaohan Wu, Myungsoo Kim, Jack C. Lee and Deji Akinwande, “2D Materials based Non-volatile Resistive Memories and RF Switches”, *Emerging 2D Materials and Devices for the Internet of Things: Information, Sensing and Energy Applications*, 1st Edition. ISBN: 978-012-81-8386-1, Published by Elsevier, June 2020.

3. Cheng Chih Hsieh, Yao-Feng Chang, Ying-Chen Chen, Chih-Yang Lin, Meiqi Guo, Fei Zhou, Burt Fowler, Ting-Chang Chang, Sanjay Banerjee, Jack C. Lee, “Memristor and Memristive Neural Networks: Review of Recently Progress on Memcomputing (Memristor + Computing) Applications in Intrinsic SiOx-Based Resistive Switching Memory”, ISBN: 978-953-51-5481-5, InTech (2018).

4. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, Simon M. Sze, and Jack C. Lee, "A Synaptic Device Built in One Diode-One Resistor (1D-1R) Architecture with Intrinsic SiOx-based Resistive Switching Memory", Nano Devices and Sensors, Published by De Gruyter publisher, March (2016).

5. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, Simon M. Sze, and Jack C. Lee, "A Synaptic Device Built in One Diode-One Resistor (1D-1R) Architecture with Intrinsic SiOx-based Resistive Switching Memory", *Nano Devices and Sensors*, p. 91-112, ISBN: 978-1-5015-0153-1, Published by De Gruyter, (March 2016).

6. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Xiaohan Wu, Yen-Ting Chen, Yanzhen Wang, Fei Xue, and Jack C. Lee, “Resistive Switching Characteristics and Mechanisms in Silicon Oxide Memory Devices,” *Nano Devices and Sensors*, p. 73-90, ISBN: 978-1-5015-0153-1, Published by De Gruyter publisher, (March 2016).

7. Y. H. Kim and J. Lee, “Hf-Based High-K Dielectrics, Process Development, Performance Characterization and Reliability,” ISBN: 9781598290042, Morgan and Claypool Publishers (Jan. 2006).

8. K. Onishi and J. Lee, "High-*k* Transistor Characteristics" in the book entitled, "High k Gate Dielectrics" (Ed. Michel Houssa), ISBN:0-7503-0906-7, published by IOP Publishing Ltd (2004).