PTO/AIA/15 (10-17)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	10018-01-0015-US-DIV1
First Named Inventor	Mei Lan GUO
Title	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS
Priority Mail Express® Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [✔] **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. [ ] **Applicant asserts small entity status.** See 37 CFR 1.27
3. [ ] **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. [✔] **Specification** [*Total Pages* 34] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. [✔] **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 20]
6. **Inventor's Oath or Declaration** [*Total Pages* 3] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. [ ] Newly executed (original or copy)
   b. [✔] A copy from a prior application (37 CFR 1.63(d))
7. [✔] **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   [ ] Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. [ ] Computer Readable Form (CRF)
   b. [ ] Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

ADDRESS TO: **Commissioner for Patents**
P.O. Box 1450
Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PAPERS

10. [ ] **Assignment Papers** (cover sheet & document(s))
    Name of Assignee Yangtze Memory Technologies Co., Ltd.
11. [ ] **37 CFR 3.73(c) Statement** (*when there is an assignee*) [✔] **Power of Attorney**
12. [ ] **English Translation Document** (*if applicable*)
13. [✔] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    [ ] Copies of citations attached
14. [ ] **Preliminary Amendment**
15. [ ] **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. [ ] **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. [ ] **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. [ ] **Other:**

***Note**: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

[✔] The address associated with Customer Number: 153988 **OR** [ ] Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Zhiwei Zou/	Date	1/17/2020
Name (Print/Type)	Zhiwei Zou	Registration No. (Attorney/Agent)	66,041

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/17 (01-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

FEE TRANSMITTAL

		Complete if known	
		Application Number	
		Filing Date	
☐ Applicant asserts small entity status. See 37 CFR 1.27.		First Named Inventor	Mei Lan GUO
☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.		Examiner Name	To Be Assigned
		Art Unit	To Be Assigned
TOTAL AMOUNT OF PAYMENT	($) 1720	Practitioner Docket No.	10018-01-0015-US-DIV1

METHOD OF PAYMENT (check all that apply)

☐ Check ■ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

■ Deposit Account Deposit Account Number: 602227 Deposit Account Name: BAYES DEPOSIT ACCOUNT

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

■ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☐ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	300	150*	75	660	330	165	760	380	190	1720
Design	200	100	50	160	80	40	600	300	150	
Plant	200	100	50	420	210	105	620	310	155	
Reissue	300	150	75	660	330	165	2,200	1,100	550	
Provisional	280	140	70	0	0	0	0	0	0	

* The $150 small entity status filing fee for a utility application is further reduced to $75 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	100	50	25
Each independent claim over 3 (including Reissues)	460	230	115
Multiple dependent claims	820	410	205

Total Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
20	-20 or HP =	0 x	0.00	=	

HP = highest number of total claims paid for, if greater than 20.

Multiple Dependent Claims	
Fee ($)	**Fee Paid ($)**

Indep. Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
3	-3 or HP =	0 x	0.00	=	

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	**Extra Sheets**	**Number of each additional 50 or fraction thereof**		**Fee ($)**		**Fee Paid ($)**
20 - 100 =	/ 50 =	(round **up** to a whole number)	x		=	

4. OTHER FEE(S) **Fees Paid ($)**

Non-English specification, $130 fee (no small or micro entity discount) _____

Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity) _____

Other (e.g., late filing surcharge): _____ _____

SUBMITTED BY

Signature	/Zhiwei Zou/	Registration No. (Attorney/Agent) 66,041	Telephone
Name (Print/Type)	Zhiwei Zou		Date 1/17/2020

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0015-US-DIV1
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Mei Lan		Guo	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	Wuhan	Country of Residence i	CN

Mailing Address of Inventor:

Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan	State/Province	
Postal Code		Country i	CN

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yushi		Hu	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Wuhan	Country of Residence i	CN

Mailing Address of Inventor:

Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan	State/Province	
Postal Code		Country i	CN

Inventor 3 Remove

Legal Name

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0015-US-DIV1
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ji		Xia	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Wuhan	Country of Residence i	CN

Mailing Address of Inventor:

Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan	**State/Province**	
Postal Code		**Country** i	CN

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hongbin		Zhu	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Wuhan	Country of Residence i	CN

Mailing Address of Inventor:

Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan	**State/Province**	
Postal Code		**Country** i	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	153988		
Email Address	uspto@bayes.law	Add Email	Remove Email

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0015-US-DIV1
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME	

Application Information:

Title of the Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		
Attorney Docket Number	10018-01-0015-US-DIV1	**Small Entity Status Claimed** ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	20	**Suggested Figure for Publication (if any)**	1

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	153988		

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0015-US-DIV1
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Division of	16149103	2018-10-01
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16149103	Continuation of	PCT/CN2018/101482	2018-08-21

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0015-US-DIV1
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0015-US-DIV1
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	YANGTZE MEMORY TECHNOLOGIES CO., LTD.		
Mailing Address Information For Applicant:			
Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan	**State/Province**	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0015-US-DIV1
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Zhiwei Zou/			Date (YYYY-MM-DD)	2020-01-17
First Name	Zhiwei	Last Name	Zou	Registration Number	66,041

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0015-US-DIV1
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Micron Ex. 1016, p. 10
Micron v. YMTC
IPR2025-00191

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ABSTRACT

Embodiments of three-dimensional (3D) memory devices having through array contacts (TACs) and methods for forming the same are disclosed. In an example, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A first opening extending vertically through the dielectric stack is formed. A spacer is formed on a sidewall of the first opening. A TAC extending vertically through the dielectric stack is formed by depositing a conductor layer in contact with the spacer in the first opening. A slit extending vertically through the dielectric stack is formed after forming the TAC. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

Micron Ex. 1016, p. 12
Micron v. YMTC
IPR2025-00191

WHAT IS CLAIMED IS:

1. A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs;

a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack; and

a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack,

wherein the TAC comprises a conductor layer and a spacer in a plurality of shallow recesses abutting a sidewall of the TAC.

2. The 3D memory device of claim 1, wherein the spacer is further over the sidewall of the TAC.

3. The 3D memory device of claim 1, wherein the TAC is in an inner region of the memory stack.

4. The 3D memory device of claim 1, further comprising a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.

5. The 3D memory device of claim 4, wherein the dielectric layer in the dummy channel structure and the spacer in the TAC comprise silicon oxide.

6. The 3D memory device of claim 1, further comprising:

a peripheral device on the substrate; and

a peripheral contact outside of the memory stack and in contact with the peripheral device.

7. The 3D memory device of claim 1, further comprising a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack.

Micron Ex. 1016, p. 13
Micron v. YMTC
IPR2025-00191

8. The 3D memory device of claim 1, wherein the memory stack comprises:

a lower memory deck on the substrate; and

an upper memory deck above the lower memory deck.

9. The 3D memory device of claim 8, wherein the channel structure comprises:

a lower channel structure extending vertically through the lower memory deck;

an upper channel structure extending vertically through the upper memory deck; and

an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.

10. The 3D memory device of claim 1, further comprising:

a staircase structure at one side of the memory stack; and

a plurality of word line contacts each in contact with a respective one of the conductor layers of the conductor/dielectric layer pairs in the staircase structure.

11. A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs;

a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack; and

a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack,

wherein the TAC comprises a conductor layer and a spacer over a sidewall of the TAC.

12. The 3D memory device of claim 11, wherein the spacer is further in a plurality of shallow recesses abutting the sidewall of the TAC.

13. The 3D memory device of claim 11, further comprising a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.

14. The 3D memory device of claim 11, further comprising:

Micron Ex. 1016, p. 14
Micron v. YMTC
IPR2025-00191

a peripheral device on the substrate; and

a peripheral contact outside of the memory stack and in contact with the peripheral device.

15. A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs;

a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;

a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack; and

a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.

16. The 3D memory device of claim 15, further comprising:

a peripheral device on the substrate; and

a peripheral contact outside of the memory stack and in contact with the peripheral device.

17. The 3D memory device of claim 16, wherein each of the TAC and peripheral contact comprises a spacer with a nominally same thickness.

18. The 3D memory device of claim 17, wherein the dielectric layer in the dummy channel structure and the spacers in the TAC and peripheral contact comprise silicon oxide.

19. The 3D memory device of claim 15, wherein the memory stack comprises:

a lower memory deck on the substrate; and

an upper memory deck above the lower memory deck.

20. The 3D memory device of claim 19, wherein the channel structure comprises:

a lower channel structure extending vertically through the lower memory deck;

an upper channel structure extending vertically through the upper memory deck; and

an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.

Micron Ex. 1016, p. 16
Micron v. YMTC
IPR2025-00191

THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is divisional of U.S. Application No. 16/149,103, filed on October 1, 2018, entitled "THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME," which is continuation of International Application No. PCT/CN2018/101482, filed on August 21, 2018, entitled "THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME," both of which are hereby incorporated by reference in their entireties.

BACKGROUND

[0002] Embodiments of the present disclosure relate to three-dimensional (3D) memory devices and fabrication methods thereof.

[0003] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As a result, memory density for planar memory cells approaches an upper limit.

[0004] A 3D memory architecture can address the density limitation in planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array.

SUMMARY

[0005] Embodiments of 3D memory devices and fabrication methods thereof are disclosed herein.

[0006] In one example, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A first opening extending vertically through the dielectric stack is formed. A spacer is

Micron Ex. 1016, p. 17
Micron v. YMTC
IPR2025-00191

formed on a sidewall of the first opening. A through array contact (TAC) extending vertically through the dielectric stack is formed by depositing a conductor layer in contact with the spacer in the first opening. A slit extending vertically through the dielectric stack is formed after forming the TAC. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0007] In another example, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A dummy channel structure extending vertically through the dielectric stack is formed. A first opening through the dielectric stack and a second opening outside of the dielectric stack are simultaneously etched. A first spacer on a sidewall of the first opening and a second spacer on a sidewall of the second opening are simultaneously formed. A conductor layer is deposited (i) filling in the first opening to form a TAC and (ii) filling in the second opening to form a peripheral contact. A slit extending vertically through the dielectric stack is formed after forming the TAC and peripheral device. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0008] In still another example, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A first opening through the dielectric stack, a second opening outside of the dielectric stack, and a third opening through the dielectric stack are simultaneously etched. A lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings. A dielectric layer is deposited (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening. Parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening are removed. A conductor layer is deposited (i) filling in the first opening to form a TAC and (ii) filling in the second opening to form a peripheral contact. A slit extending vertically through the

Micron Ex. 1016, p. 18
Micron v. YMTC
IPR2025-00191

dielectric stack is formed after forming the TAC and peripheral device. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0009] In a different example, a 3D memory device includes a substrate, a memory stack on the substrate including a plurality of conductor/dielectric layer pairs, a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack, a TAC extending vertically through the conductor/dielectric layer pairs in the memory stack, and a dummy channel structure fully filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0011] FIG. 1 illustrates a cross-section of an exemplary 3D memory device, according to some embodiments of the present disclosure.

[0012] FIGs. 2A–2E illustrate an exemplary fabrication process for forming channel structures of a 3D memory device, according to some embodiments of the present disclosure.

[0013] FIGs. 3A–3F illustrate exemplary fabrication processes for forming TACs, peripheral contacts, and dummy channel structures of a 3D memory device, according to various embodiments of the present disclosure.

[0014] FIGs. 4A–4C illustrate another exemplary fabrication process for forming TACs, peripheral contacts, and dummy channel structures of a 3D memory device, according to some embodiments of the present disclosure.

[0015] FIGs. 5A–5B illustrate an exemplary fabrication process for forming a slit structure and word line contacts of a 3D memory device, according to some embodiments of the present disclosure.

[0016] FIG. 6 is a flowchart of an exemplary method for forming a 3D memory device, according to some embodiments.

Micron Ex. 1016, p. 19
Micron v. YMTC
IPR2025-00191

[0017] FIG. 7A is a flowchart of an exemplary method for forming a spacer on a sidewall of an opening, according to some embodiments of the present disclosure.

[0018] FIG. 7B is a flowchart of another exemplary method for forming a spacer on a sidewall of an opening, according to some embodiments of the present disclosure.

[0019] FIG. 8 is a flowchart of another exemplary method for forming a 3D memory device, according to some embodiments of the present disclosure.

[0020] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0021] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0022] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0023] In general, terminology may be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term "based on" may be understood as not necessarily intended

Micron Ex. 1016, p. 20
Micron v. YMTC
IPR2025-00191

to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0024] It should be readily understood that the meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something but also includes the meaning of "on" something with an intermediate feature or a layer therebetween, and that "above" or "over" not only means the meaning of "above" or "over" something but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

[0025] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0026] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0027] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend laterally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an

Micron Ex. 1016, p. 21
Micron v. YMTC
IPR2025-00191

interconnect layer can include one or more conductor and contact layers (in which interconnect lines and/or via contacts are formed) and one or more dielectric layers.

[0028] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term "about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0029] As used herein, the term "3D memory device" refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND memory strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term "vertical/vertically" means nominally perpendicular to the lateral surface of a substrate.

[0030] In some 3D memory devices, interconnects can include through array contacts (TACs) for providing vertical interconnects between the stacked memory array device and peripheral device (e.g., for power bus and metal routing), thereby reducing metal levels and shrinking die size. TACs can be formed within barrier structures, which preserves a dielectric stack region within a memory stack for ease of etching the openings of the TACs. However, the regions enclosed by the barrier structures take up large area in the core array region where memory strings can be formed and also have a negative impact on the resistance of word lines. Moreover, the existing fabrication processes for forming the barrier structures become more challenging for the next-generation 3D memory devices (e.g., having 128 levels or more), which have less process margin.

[0031] Various embodiments in accordance with the present disclosure provide a 3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures. For example, by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost. More process

Micron Ex. 1016, p. 22
Micron v. YMTC
IPR2025-00191

margin can also be obtained due to the elimination of etching and alignment steps for making the barrier structures, which enables high process extendibility for both current and future generations of 3D memory devices. Moreover, various embodiments of methods for forming the 3D memory device disclosed herein can allow TACs to be formed in the same fabrication process(es) for making other structures (e.g., peripheral contacts and/or dummy channel structures) and thus, further simplify the fabrication flow and reduce process cost.

[0032] FIG. 1 illustrates a cross-section of an exemplary 3D memory device 100, according to some embodiments of the present disclosure. 3D memory device 100 can include a substrate 102, which can include silicon (e.g., single crystalline silicon), silicon germanium (SiGe), gallium arsenide (GaAs), germanium (Ge), silicon on insulator (SOI), or any other suitable materials. In some embodiments, substrate 102 is a thinned substrate (e.g., a semiconductor layer), which was thinned from a normal thickness by grinding, wet/dry etching, chemical mechanical polishing (CMP), or any combination thereof.

[0033] 3D memory device 100 can include a memory stack 104 above substrate 102. Memory stack 104 can be a stacked storage structure through which memory strings (e.g., NAND memory strings 106) are formed. In some embodiments, memory stack 104 includes a plurality of conductor/dielectric layer pairs stacked vertically above substrate 102. Each conductor/dielectric layer pair can include a conductor layer 110 and a dielectric layer 112. That is, memory stack 104 can include interleaved conductor layers 110 and dielectric layers 112 stacked vertically. As shown in FIG. 1, each NAND memory string 106 extends vertically through interleaved conductor layers 110 and dielectric layers 112 in memory stack 104. In some embodiments, 3D memory device 100 is a NAND Flash memory device in which memory cells are provided at intersections of NAND memory strings 106 and conductor layers 110 (functioning as word lines) of 3D memory device 100. The number of conductor/dielectric layer pairs in memory stack 104 (e.g., 32, 64, 96, or 128) can set the number of memory cells in 3D memory device 100.

[0034] Conductor layers 110 can each have the same thickness or have different thicknesses. Similarly, dielectric layers 112 can each have the same thickness or have different thicknesses. Conductor layers 110 can include conductive materials including,

Micron Ex. 1016, p. 23
Micron v. YMTC
IPR2025-00191

but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), polycrystalline silicon (polysilicon), doped silicon, silicides, or any combination thereof. Dielectric layers 112 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In some embodiments, conductor layers 110 include metals, such as W, and dielectric layers 112 include silicon oxide. It is understood that a silicon oxide film (not shown), such as an in-situ steam generation (ISSG) silicon oxide, is formed between substrate 102 (e.g., a silicon substrate) and memory stack 104, according to some embodiments.

[0035] It is noted that *x*, *y*, and z axes are added to FIG. 1 to further illustrate the spatial relationship of the components in 3D memory device 100. The *x*-, *y*-, and *z*-directions are perpendicular to one another. Substrate 102 includes two lateral surfaces (e.g., a top surface and a bottom surface) extending laterally in the *x*-direction and *y*-direction (the lateral direction) in the *x*-*y* plane. As used herein, whether one component (e.g., a layer or a device) is "on," "above," or "below" another component (e.g., a layer or a device) of a semiconductor device (e.g., 3D memory device 100) is determined relative to the substrate (e.g., substrate 102) of the semiconductor device in the *z*-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the *z*-direction. The same notion for describing spatial relationship is applied throughout the present disclosure.

[0036] In some embodiments, 3D memory device 100 is part of a monolithic 3D memory device, in which the components of the monolithic 3D memory device (e.g., memory cells and peripheral devices) are formed on a single substrate (e.g., substrate 102). Peripheral devices 111, such as any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 100, can be formed on substrate 102 as well, outside of memory stack 104. Peripheral device 111 can be formed "on" substrate 102, where the entirety or part of peripheral device 111 is formed in substrate 102 (e.g., below the top surface of substrate 102) and/or directly on substrate 102. Peripheral device 111 can include one or more of a page buffer, a decoder (e.g., a row decoder and a column decoder), a sense amplifier, a driver, a charge pump, a current or voltage reference, or any active or passive components of the circuits (e.g., transistors, diodes, resistors, or capacitors). Isolation regions (e.g., shallow trench

Micron Ex. 1016, p. 24
Micron v. YMTC
IPR2025-00191

isolations (STIs)) and doped regions (e.g., source regions and drain regions of the transistors) can be formed in substrate 102 as well, outside of memory stack 104.

[0037] As shown in FIG. 1, memory stack 104 can include an inner region 116 (also known as a "core array region") and an outer region 118 (also known as a "staircase region"). In some embodiments, inner region 116 is the center region of memory stack 104 where an array of NAND memory strings 106 are formed through the conductor/dielectric layer pairs, and outer region 118 is the remaining region of memory stack 104 surrounding inner region 116 (including the sides and edges) without NAND memory strings 106.

[0038] As shown in FIG. 1, each NAND memory string 106 can include a channel structure 108 extending vertically through the conductor/dielectric layer pairs in inner region 116 of memory stack 104. Channel structure 108 can include a channel hole filled with semiconductor materials (e.g., forming a semiconductor channel) and dielectric materials (e.g., forming a memory film). In some embodiments, the semiconductor channel includes silicon, such as amorphous silicon, polysilicon, or single crystalline silicon. In some embodiments, the memory film is a composite layer including a tunneling layer, a storage layer (also known as a "charge trap/storage layer"), and a blocking layer. Each NAND memory string 106 can have a cylinder shape (e.g., a pillar shape). The semiconductor channel, tunneling layer, storage layer, and blocking layer are arranged along a direction from the center toward the outer surface of the pillar in this order, according to some embodiments. The tunneling layer can include silicon oxide, silicon oxynitride, or any combination thereof. The storage layer can include silicon nitride, silicon oxynitride, silicon, or any combination thereof. The blocking layer can include silicon oxide, silicon oxynitride, high dielectric constant (high-k) dielectrics, or any combination thereof.

[0039] In some embodiments, NAND memory strings 106 include a plurality of control gates (each being part of a word line/conductor layer 110) for NAND memory strings 106. Conductor layer 110 in each conductor/dielectric layer pair can function as a control gate for memory cells of NAND memory string 106. Conductor layer 110 can include multiple control gates for multiple NAND memory strings 106 and can extend laterally as a word line ending in outer region 118 of memory stack 104.

Micron Ex. 1016, p. 25
Micron v. YMTC
IPR2025-00191

[0040] In some embodiments, NAND memory string 106 includes two plugs 117 and 119 at a respective end in the vertical direction. Each plug 117 or 119 can be in contact with a respective end of channel structure 108. Plug 117 can include a semiconductor material, such as silicon, that is epitaxially grown from substrate 102. Plug 117 can function as the channel controlled by a source select gate of NAND memory string 106. Plug 117 can be at the lower end of NAND memory string 106 and in contact with channel structure 108 (e.g., on the upper end of channel structure 108). As used herein, the "upper end" of a component (e.g., NAND memory string 106) is the end father away from substrate 102 in the *z*-direction, and the "lower end" of the component (e.g., NAND memory string 106) is the end closer to substrate 102 in the *z*-direction when substrate 102 is positioned in the lowest plane of 3D memory device 100.

[0041] Plug 119 can include semiconductor materials (e.g., polysilicon) or conductor materials (e.g., metals). In some embodiments, plug 119 includes an opening filled with titanium/titanium nitride (Ti/TiN as a barrier layer) and tungsten (as a conductor). By covering the upper end of channel structure 108 during the fabrication of 3D memory device 100, plug 119 can function as an etch stop layer to prevent etching of dielectrics filled in channel structure 108, such as silicon oxide and silicon nitride. In some embodiments, plug 119 functions as the drain of NAND memory string 106.

[0042] In some embodiments, memory stack 104 includes a lower memory deck 120 disposed on substrate 102 and an upper memory deck 122 disposed above lower memory deck 120. A joint layer 124 can be disposed vertically between and electrically isolate lower memory deck 120 and upper memory deck 122. Each of lower and upper memory deck 120 and 122 can have the same or different number of conductor/dielectric layer pairs. Joint layer 124 can include dielectrics, such as silicon oxide. By separating memory stack 104 into lower and upper memory decks 120 and 122, or even more memory decks in some embodiments, channel structure 108 of NAND memory string 106 can be jointed by multiple channel structures, each of which is separately formed through a respective memory deck, to increase process yield. As shown in FIG. 1, channel structure 108 of NAND memory sting 106 includes a lower channel structure 126 extending vertically through lower memory deck 120 and an upper channel structure 128 extending vertically through upper memory deck. In some embodiments, an inter-deck plug 130 is disposed vertically between and in contact with lower channel structure 126

Micron Ex. 1016, p. 26
Micron v. YMTC
IPR2025-00191

and upper channel structure 128. Inter-deck plug 130 can include semiconductor materials, such as polysilicon, and joint (e.g., electrically connect) lower and upper channel structures 126 and 128 to form channel structure 108. That is, NAND memory string 106 can include plug 117, lower channel structure 126, inter-deck plug 130, upper channel structure 128, and plug 119 from bottom to top in this order.

[0043] In some embodiments, 3D memory device 100 further includes slit structures 132. Each slit structure 132 can extend vertically through the conductor/dielectric layer pairs in memory stack 104. Slit structure 132 can also extend laterally (e.g., in the *y*-direction) to separate memory stack 104 into multiple blocks. Slit structure 132 can include an opening (slit) filled with conductive materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), silicides, or any combination thereof. Slit structure 132 can further include a spacer having dielectric materials, such as silicon oxide, laterally between the filled conductive materials and memory stack 104 to electrically insulate the filled conductive materials from surrounding conductor layers 110 in memory stack 104. As a result, slit structures 132 can separate 3D memory device 100 into multiple memory blocks and/or memory fingers.

[0044] In some embodiments, slit structure 132 functions as the source contact for NAND memory strings 106 in the same memory block or the same memory finger that share the same array common source. Slit structure 132 can thus be referred to as a "common source contact" of multiple NAND memory strings 106. In some embodiments, substrate 102 includes a doped region 134 (including p-type or n-type dopants at a desired doping level), and the lower end of slit structure 132 is in contact with doped region 134 of substrate 102. Slit structure 132 thus can electrically connect to NAND memory strings 106 by doped region 134.

[0045] As shown in FIG. 1, 3D memory device 100 further includes TACs 136 each extending vertically through the conductor/dielectric layer pairs in memory stack 104. Each TAC 136 can extend vertically through interleaved conductor layers 110 and dielectric layers 112. In some embodiments, TAC 136 can extend through the entire thickness of memory stack 104, (e.g., all the conductor/dielectric layer pairs in the vertical direction). In some embodiments, TAC 136 further extends through at least part of substrate 102. TAC 136 can carry electrical signals from and/or to 3D memory device 100, such as part of the power bus, with shorten interconnect routing. In some

Micron Ex. 1016, p. 27
Micron v. YMTC
IPR2025-00191

embodiments, TAC 136 can provide electrical connections between 3D memory device 100 and peripheral device 111 and/or between back-end-of-line (BEOL) interconnects (not shown) and peripheral device 111. TAC 136 can also provide mechanical support to memory stack 104.

[0046] TAC 136 can include a vertical opening through memory stack 104 and that is filled with filling materials. In some embodiments, TAC 136 includes a spacer 138 on a sidewall of the opening and a conductor layer 140 in contact with spacer 138 in the opening. Conductor layer 140 can include conductive materials, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Spacer 138 can electrically insulate conductor layer 140 of TAC 136 from surrounding conductor layers 110 in memory stack 104. In some embodiments, TAC 136 has a substantially circular shape in the plan view, and conductor layer 140 and spacer 138 are disposed radially from the center of TAC 136 in this order. Spacer 138 of TAC 136 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

[0047] As shown in FIG. 1, at least on one side in the lateral direction (e.g., in the *y*-direction), outer region 118 of memory stack 104 can include a staircase structure 142. In some embodiments, another staircase structure (not shown) is disposed on the opposite side of memory stack 104 in the *y*-direction. Each "level" of staircase structure 142 can include one or more conductor/dielectric layer pairs, each including conductor layer 110 and dielectric layer 112. The top layer in each level of staircase structure 142 can be conductor layer 110 for interconnection in the vertical direction. In some embodiments, each two adjacent levels of staircase structure 142 are offset by a nominally same distance in the vertical direction and a nominally same distance in the lateral direction. For each two adjacent levels of staircase structure 142, the first level (and conductor layer and dielectric layer therein) that is closer to substrate 102 can extend laterally further than the second level (and conductor layer and dielectric layer therein), thereby forming a "landing area" on the first level for interconnection in the vertical direction.

[0048] Staircase structure 142 can be used for landing word line contacts 144 and/or for balancing load in certain processes during fabrication (e.g., etching and chemical mechanical polishing (CMP)) by dummy channel structures 146 therethrough. The lower end of each word line contact 144 can be in contact with top conductor layer 110 (word

Micron Ex. 1016, p. 28
Micron v. YMTC
IPR2025-00191

line) in a respective level of staircase structure 142 to individually address a corresponding word line of 3D memory device 100. Word line contact 144 can include an opening (e.g., a via hole or a trench) extending vertical through one or more dielectric layers and filled with conductive materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof.

[0049] Dummy channel structure 146 can extend vertically through memory stack 104 and have a vertical opening filled with the same materials as those in channel structure 108. Different from channel structures 108, a contact is not formed on dummy channel structure 146 to provide electrical connections with other components of 3D memory device 100, according to some embodiments. In some embodiments, dummy channel structure 146 is fully filled with dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. Thus, dummy channel structures 146 cannot be used for forming memory cells in 3D memory device 100. Instead, dummy channel structures 146 can provide mechanical support to the memory array structures, e.g., memory stack 104. Although dummy channel structures 146 are disposed in outer region 118 of memory stack 104 as shown in FIG. 1, it is understood that dummy channel structures 146 can be formed in inner region 116 of memory stack 104 as well. In some embodiments, dummy channel structure 146 is fully filled with a dielectric layer, such as a silicon oxide layer, and extends vertically through the conductor/dielectric layer pairs in memory stack 104, either in inner region 116 or in outer region 118.

[0050] As shown in FIG. 1, 3D memory device 100 can further include peripheral contacts 148 extending vertically through one or more dielectric layers and in contact with peripheral devices 111 outside of memory stack 104. Peripheral contact 148 can provide electrical connections with peripheral devices 111. Peripheral contact 148 can include a vertical opening filled with filling materials. In some embodiments, similar to TAC 136, peripheral contact 148 includes a spacer 150 on a sidewall of the opening and a conductor layer 152 in contact with spacer 150 in the opening. Conductor layer 152 can include conductive materials, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. In some embodiments, peripheral contact 148 has a substantially circular shape in the plan view, and conductor layer 152 and spacer 150 are disposed radially from the center of peripheral contact 148 in this order. Spacer 150 of

Micron Ex. 1016, p. 29
Micron v. YMTC
IPR2025-00191

peripheral contact 148 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In some embodiments, spacer 150 of peripheral contact 148 and spacer 138 of TAC 136 have nominally the same thickness in the lateral direction (e.g., radial direction). In some embodiments, both spacer 150 of peripheral contact 148 and spacer 138 of TAC 136 include silicon oxide.

[0051] It is understood that 3D memory device 100 can include additional components and structures not shown in FIG. 1 including, but not limited to, other local contacts and interconnects in one or more BEOL interconnect layers above memory stack 104 and/or below substrate 102.

[0052] FIGs. 2A–2E illustrate an exemplary fabrication process for forming channel structures of a 3D memory device, according to some embodiments of the present disclosure. FIGs. 3A–3F illustrate exemplary fabrication processes for forming TACs, peripheral contacts, and dummy channel structures of a 3D memory device, according to various embodiments of the present disclosure. FIGs. 4A–4C illustrate another exemplary fabrication process for forming TACs, peripheral contacts, and dummy channel structures of a 3D memory device, according to some embodiments of the present disclosure. FIGs. 5A–5B illustrate an exemplary fabrication process for forming a slit structure and word line contacts of a 3D memory device, according to some embodiments of the present disclosure. FIG. 6 is a flowchart of an exemplary method 600 for forming a 3D memory device, according to some embodiments. FIG. 8 is a flowchart of another exemplary method 800 for forming a 3D memory device, according to some embodiments of the present disclosure. Examples of the 3D memory device depicted in FIGs. 2-6 and 8 include 3D memory device 100 depicted in FIG. 1. FIGs. 2-6 and 8 will be described together. It is understood that the operations shown in methods 600 and 800 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. Further, some of the operations may be performed simultaneously, or in a different order than shown in FIGs. 6 and 8.

[0053] Referring to FIG. 6, method 600 starts at operation 602, in which a dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. The substrate can be a silicon substrate. In some embodiments, a lower dielectric deck is formed first, followed by the formation of a joint layer. An upper dielectric deck can then

be formed on the joint layer to form the dielectric stack. Method 600 proceeds to operation 604, as illustrated in FIG. 6, in which a channel structure extending vertically through the dielectric stack is formed. In some embodiments, a lower channel structure extending vertically through the lower dielectric deck is formed. An inter-deck plug can then be formed on the lower channel structure in the joint layer. Once the upper dielectric deck is formed, an upper channel structure extending vertically through the upper dielectric deck can be formed and jointed with the lower channel structure by the inter-deck plug, thereby forming the channel structure. In some embodiments, a staircase structure is formed at one side of the dielectric stack.

[0054] As illustrated in FIG. 2A, a lower dielectric deck 204 including a plurality of dielectric/sacrificial layer pairs is formed on a silicon substrate 202. In some embodiments, sacrificial layers 206 and dielectric layers 208 are alternatingly deposited by one or more thin film deposition processes including, but not limited to, physical vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), or any combination thereof. In some embodiments, sacrificial layers 206 include silicon nitride, and dielectric layers 208 include silicon oxide. It is understood that the sequence of depositing sacrificial layers 206 and dielectric layers 208 is not limited. The deposition can start with sacrificial layer 206 or dielectric layer 208 and can end with sacrificial layer 206 or dielectric layer 208.

[0055] As illustrated in FIG. 2B, an array of lower channel structures 210 are formed, each of which extends vertically through interleaved sacrificial layers 206 and dielectric layers 208 in lower dielectric deck 204. In some embodiments, fabrication processes to form lower channel structure 210 include forming a channel hole through interleaved sacrificial layers 206 and dielectric layers 208 in lower dielectric deck 204 using dry etching/and or wet etching, such as deep reactive-ion etching (DRIE), followed by filling the channel hole with a plurality of layers, such as a dielectric layer and a semiconductor layer, using thin film deposition processes. In some embodiments, the dielectric layer is a composite dielectric layer, such as a combination of multiple dielectric layers including, but not limited to, a tunneling layer, a storage layer, and a blocking layer. The tunneling layer can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. The storage layer can include materials for storing charge for memory operation. The storage layer materials can

Micron Ex. 1016, p. 31
Micron v. YMTC
IPR2025-00191

include, but not limited to, silicon nitride, silicon oxynitride, a combination of silicon oxide and silicon nitride, or any combination thereof. The blocking layer can include dielectric materials including, but not limited to, silicon oxide or a combination of silicon oxide/silicon oxynitride/silicon oxide (ONO). The blocking layer can further include a high-k dielectric layer, such as an aluminum oxide (Al_2O_3) layer. The semiconductor layer can include polysilicon, serving as a semiconductor channel. The semiconductor layer and dielectric layer can be formed by processes such as ALD, CVD, PVD, or any combination thereof.

[0056] As illustrated in FIG. 2B, a joint layer 212 is formed on lower dielectric deck 204 by depositing a dielectric layer, such as a silicon oxide layer, using thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof. An array of inter-deck plugs 214 are formed in joint layer 212 and in contact with array of lower channel structures 210, respectively. Inter-deck plugs 214 can be formed by patterning and etching openings through joint layer 212, followed by deposition of semiconductor materials, such as polysilicon, using thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof.

[0057] As illustrated in FIG. 2C, an upper dielectric deck 216 is formed on joint layer 212 and above lower dielectric deck 204. A dielectric stack 218 including lower dielectric deck 204 and upper dielectric deck 216 can thus be formed. The same fabrication processes for forming lower dielectric deck 204 can be used for forming upper dielectric deck 216 and thus, are not repeated again.

[0058] As illustrated in FIG. 2D, an array of upper channel structures 220 each extending vertically through upper dielectric deck 216 are formed and in contact with array of inter-deck plugs 214, respectively. An array of channel structures 222 each including lower channel structure 210 and upper channel structure 220 that are electrically connected by inter-deck plug 214 are thus formed. The same fabrication processes for forming lower channel structures 210 can be used for forming upper channel structures 220 and thus, are not repeated.

[0059] As illustrated in FIG. 2E, staircase structures 224 are formed on the sides of dielectric stack 218. Staircase structure 224 can be formed by the so-called "trim-etch" processes, which, in each cycle, trim (e.g., etching incrementally and inwardly, often from all directions) a patterned photoresist layer, followed by etching the exposed

Micron Ex. 1016, p. 32
Micron v. YMTC
IPR2025-00191

portions of the dielectric/sacrificial layer pair using the trimmed photoresist layer as an etch mask to form one step of staircase structure 224.

[0060] Method 600 proceeds to operation 606, as illustrated in FIG 6, in which a dummy channel structure extending vertically through the dielectric stack is formed. As illustrated in FIG. 3A, an array of dummy channel structures 302 are formed through dielectric layer 218. Dummy channel structure 302 can be formed by first etching an opening through dielectric stack 218 and/or one or more dielectric layers using wet etching and/or dry etching, such as DRIE. In some embodiments, the opening is then fully filled with a dielectric layer, such as a silicon oxide layer, using one or more thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof. In some embodiments, dummy channel structures 302 are formed simultaneously with channel structures 222 in the same fabrication steps, such that the opening of each dummy channel structure 302 is filled with at least some of the materials filling in channel structures 222.

[0061] Method 600 proceeds to operation 608, as illustrated in FIG 6, in which a first opening through the dielectric stack and a second opening outside of the dielectric stack are simultaneously etched. As illustrated in FIG. 3B, first openings (TAC holes) 304 each extending vertically through the dielectric/sacrificial layer pairs in dielectric stack 218 are formed by wet etching and/or drying etching of interleaved dielectric layers 208 and sacrificial layers 206 (e.g., silicon nitride and silicon oxide). In some embodiments, TAC holes 304 are etched using DRIE. Second openings (peripheral contact holes) 306 can be simultaneously formed by the same wet etching and/or drying etching process, such as DRIE, to etch through one or more dielectric layers (e.g., silicon oxide and/or silicon nitride) outside of dielectric stack 218. The depths of TAC hole 304 and peripheral contact hole 306 in the vertical direction can be nominally the same. The lateral dimensions of TAC hole 304 and peripheral contact hole 306, such as the diameters, can be nominally the same or different in various embodiments. For example, the diameter of TAC hole 304 is greater than the diameter of peripheral contact hole 306, according to some embodiments.

[0062] As shown in FIG. 3B, TAC hole 304 and peripheral contact hole 306 can reach to silicon substrate 202, and the lower end of peripheral contact hole 306 can be in contact with a peripheral device 307 formed on silicon substrate 202. In some embodiments,

peripheral device 307 includes transistors, which can be formed by a plurality of processes including, but not limited to, photolithography, dry/wet etch, thin film deposition, thermal growth, implantation, CMP, and any other suitable processes. In some embodiments, doped regions are formed in silicon substrate 202 by ion implantation and/or thermal diffusion, which function, for example, as source regions and/or drain regions of the transistors. In some embodiments, isolation regions (e.g., STIs) are also formed in silicon substrate 202 by wet etching and/or dry etching and thin film deposition processes. The fabrication process for forming peripheral device 307 can occur at any fabrication stage prior to the etching of peripheral contact hole 306.

[0063] Method 600 proceeds to operation 610, as illustrated in FIG 6, in which a first spacer and a second spacer are simultaneously formed on sidewalls of the first opening and the second opening, respectively. FIG. 7A is a flowchart of an exemplary method for forming a spacer on a sidewall of an opening, according to some embodiments. Referring to FIG. 7A, at operation 702, to form the first spacer, a dielectric layer is deposited on the sidewall and bottom surface of the first opening. At operation 704, part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The deposition of the dielectric layer can include ALD, and the removal of the part of the dielectric layer can include anisotropic etching on the bottom surface of the first opening.

[0064] As illustrated in FIG. 3C, a first spacer 308 is formed on the sidewall, but not the bottom surface, of TAC hole 304. A dielectric layer can be first deposited into TAC hole 304 using one or more thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof, which covers the sidewall and bottom surface of TAC hole 304. The part of the dielectric layer deposited on the bottom surface, but not on the sidewall, of TAC hole 304 can then be etched through using "bottom punch" processes. In some embodiments, a silicon oxide layer can be deposited on the sidewall and bottom surface of TAC hole 304 using ALD, and the part of the silicon oxide layer deposited on the bottom surface of TAC hole 304 can be removed using any suitable anisotropic etching directed to the bottom surface of TAC hole 304. In one example, a bias with a sufficient voltage level may be added to DRIE to etch through the silicon oxide layer on the bottom surface, but not through the sidewall, of TAC hole 304. Second spacer 310 can be simultaneously formed on the sidewall, but not the bottom surface, of peripheral contact hole 306, using the same deposition and bottom punch processes. In some embodiments,

the thicknesses of first spacer 308 and second spacer 310 are nominally the same in the lateral direction (e.g., radial direction).

[0065] FIG. 7B is a flowchart of another exemplary method for forming a spacer on a sidewall of an opening, according to some embodiments. Referring to FIG. 7B, at operation 706, to form the first spacer on the sidewall of the first opening, a plurality of shallow recesses are first formed by removing parts of the sacrificial layers abutting the sidewall of the first opening. At operation 708, a dielectric layer is deposited filling in the shallow recesses and on the sidewall and a bottom surface of the first opening. At operation 710, part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The removal of the part of the dielectric layer includes isotropic etching on the sidewall and the bottom surface of the first opening, according to some embodiments.

[0066] Different from the example illustrated in FIG. 3C in which first spacer 308 is formed by ALD deposition and bottom punch processes, FIGs. 3D-3E illustrate another example in which a first spacer 314 is formed by any deposition process, followed by an etch-back process. As illustrated in FIG. 3D, parts of sacrificial layers 206 in dielectric stack 218 that abut the sidewall of TAC hole 304 are removed by wet etching and/or dry etching, such as using a wet etchant for silicon nitride. A plurality of shallow recesses 312 can then be formed along the sidewall of TAC hole 304. The degree of the etching, i.e., the lateral dimension of shallow recess, can be controlled by the etching rate and/or etching time. The sacrificial layer partial removal process can provide space for a thicker dielectric layer deposition in the next step.

[0067] As illustrated in FIG. 3E, a first spacer 314 is formed on the sidewall, but not the bottom surface, of TAC hole 304. A dielectric layer can be first deposited into TAC hole 304 using one or more thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof, which fills in shallow recesses 312 (as shown in FIG. 3D) and covers the sidewall and bottom surface of TAC hole 304. The part of the dielectric layer deposited on the bottom surface of TAC hole 304 can be then removed using etch-back processes. In some embodiments, isotropic etching can be applied to etch the dielectric layer deposited on both the sidewall and the bottom surface of TAC hole 304. Because the dielectric layer is substantially thicker along the sidewall (filling in shallow recesses 312) than on the bottom surface, when the part of the dielectric layer on the bottom

Micron Ex. 1016, p. 35
Micron v. YMTC
IPR2025-00191

surface has been etched through, the part of the dielectric layer on the sidewall can be partially etched, leaving first spacer 314 covering only the sidewall of TAC hole 304. In other words, the thickened dielectric layer along the sidewall is etched-back, leaving a thinner dielectric layer as first spacer 314, according to some embodiments. The etching rate and/or etching time of any suitable isotropic etching process can be controlled to fully etch through the dielectric layer on the bottom surface of TAC hole 304, but partially etch back the dielectric layer on the sidewall of TAC hole 304.

[0068] Method 600 proceeds to operation 612, as illustrated in FIG 6, in which a conductor layer is deposited in the first opening to form a TAC and in the second opening to form a peripheral contact. In some embodiments, the conductor layer is a composite layer including an adhesion/barrier layer and a conductor. As illustrated in FIG. 3F, a conductor layer 316 is deposited in TAC hole 304 (as shown in FIGs. 3C-3E) to fill the remaining space of TAC hole 304, thereby forming a TAC 318 extending vertically through dielectric stack 218. In some embodiments, an adhesion/barrier layer is first formed along first spacer 308/314 by depositing titanium/titanium nitride (Ti/TiN) or titanium/tantalum nitride (Ta/TaN) using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination thereof. A conductor can then be formed in the remaining space of TAC hole 304 by depositing metals, such as tungsten, using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination thereof. A conductor layer 320 can be simultaneously formed in peripheral contact hole 306 (as shown in FIGs. 3C-3E) to form a peripheral contact 322 in contact with peripheral device 307, using the same deposition processes. The excess conductor layer after deposition can be removed by CMP.

[0069] Method 600 proceeds to operation 614, as illustrated in FIG 6, in which a slit extending vertically through the dielectric stack is formed after the formation of the TAC. Method 600 proceeds to operation 616, as illustrated in FIG 6, in which a memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers. In some embodiments, a slit structure is formed by depositing a conductor layer in the slit after the formation of the memory stack. In some embodiments, a plurality of word line contacts each in contact with a respective one of

Micron Ex. 1016, p. 36
Micron v. YMTC
IPR2025-00191

the conductor layers of the conductor/dielectric layer pairs in the staircase structure are formed.

[0070] As illustrated in FIG. 5A, an opening (slit) can be etched through the dielectric/sacrificial layer pairs in dielectric stack 218 (as shown in FIGs. 3-4). The slit can be formed by wet etching and/or dry etching of dielectrics (e.g., silicon oxide and silicon nitride). The opening can be used as the pathway for gate replacement processes that replace sacrificial layers 206 in dielectric stack 218 with conductor layers 502 to form a plurality of conductor/dielectric layer pairs. The replacement of sacrificial layers 206 with conductor layers 502 can be performed by wet etching sacrificial layers 206 (e.g., silicon nitride) selective to dielectric layers 208 (e.g., silicon oxide) and filling the structure with conductor layers 502 (e.g., W). Conductor layers 502 can be deposited by PVD, CVD, ALD, electrochemical depositions, or any combination thereof. Conductor layers 502 can include conductive materials including, but not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. As a result, after the gate replacement processes, dielectric stack 218 in FIGs. 3-4 becomes memory stack 504 including the conductor/dielectric layer pairs, i.e., interleaved conductor layers 502 and dielectric layers 208, on silicon substrate 202.

[0071] As illustrated in FIG. 5A, a slit structure 506 is formed by filling (e.g., depositing) conductive materials into the slit by PVD, CVD, ALD, electrochemical depositions, or any combination thereof. Slit structure 506 can include conductive materials including, but not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. In some embodiments, a dielectric layer (e.g., a silicon oxide layer) is formed first between the conductive materials of slit structure 506 and conductor layers 502 surrounding slit structure 506 as a spacer. The lower end of slit structure 506 can be in contact with a doped region 507, which can be formed in silicon substrate 202 using ion implantation and/or thermal diffusion.

[0072] As illustrated in FIG. 5B, each word line contact 508 is in contact with a respective one of conductor layers 502 of the conductor/dielectric layer pairs in staircase structure 224. Word line contacts 508 are formed through one or more dielectric layers by first etching vertical openings (e.g., by wet etching and/or dry etching), followed by filling the openings with conductive materials using ALD, CVD, PVD, electrochemical depositions, or any combination thereof. In some embodiments, other conductive

Micron Ex. 1016, p. 37
Micron v. YMTC
IPR2025-00191

materials are filled in the openings to function as an adhesion/barrier layer. Etching of dielectric layers to form the openings of word line contacts 508 can be controlled by etch stop at a different material. For example, etching of dielectric layers can be stopped when reaching to conductor layers 502 in staircase structure 224.

[0073] FIG. 8 is a flowchart of another exemplary method 800 for forming a 3D memory device, according to some embodiments of the present disclosure. Operations 802, 804, 814, and 816 are similar to operations 602, 604, 614, and 616, respectively, and thus are not repeated. Method 800 proceeds to operation 806, as illustrated in FIG 8, in which a first opening through the dielectric stack, a second opening outside of the dielectric stack, and a third opening through the dielectric stack are simultaneously etched. In some embodiments, the lateral dimension (e.g., diameter) of the third opening is smaller than lateral dimensions of the first and second openings. Each of the first, second, and third openings has a nominally circular shape in the plan view, according to some embodiments.

[0074] As illustrated in FIG. 4A, a first opening (TAC hole) 402, a second opening (peripheral contact hole) 404, and a third opening (dummy channel hole) 406 are simultaneously formed, each of which reaches to silicon substrate 202. The lower end of peripheral contact hole 404 can be in contact with a peripheral device 405 formed on silicon substrate 202. TAC hole 402 and dummy channel hole 406 can be etched through interleaved sacrificial layers 206 and dielectric layers 208 (e.g., silicon nitride and silicon oxide) in dielectric stack 218 using wet etching and/or dry etching, and peripheral contact hole 404 can be simultaneously etched through one or more dielectric layers (e.g., silicon oxide) using the same wet etching and/or dry etching process. In some embodiments, TAC hole 402, peripheral contact hole 404, and dummy channel hole 406 are etched using DRIE at the same time. The depths of TAC hole 402, peripheral contact hole 404, and dummy channel hole 406 in the vertical direction can be nominally the same. In some embodiments, each of TAC hole 402, peripheral contact hole 404, and dummy channel hole 406 has a substantially circular shape in the plan view. The lateral dimensions (e.g., diameters) of TAC hole 402, peripheral contact hole 404, and dummy channel hole 406 can be controlled by patterning process and/or etching parameters, such as etching rate and etching time. In some embodiments, in the plan view, the diameter of dummy channel hole 406 is smaller than the diameter of TAC hole 402 and the diameter

of peripheral contact hole 404. In some embodiments, the diameter of peripheral contact hole 404 is smaller than the diameter of TAC hole 402 in the plan view.

[0075] Method 800 proceeds to operation 808, as illustrated in FIG 8, in which a dielectric layer is deposited (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening. Method 800 proceeds to operation 810, as illustrated in FIG 8, in which parts of the dielectric layer deposited on the bottom surfaces of the first and second openings are removed.

[0076] As illustrated in FIG. 4B, a dielectric layer (e.g., silicon oxide) is deposited into TAC hole 402, peripheral contact hole 404, and dummy channel hole 406 using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination thereof. Due to the different lateral dimensions of TAC hole 402, peripheral contact hole 404, and dummy channel hole 406, by controlling the deposition parameters, such as the deposition rate and/or deposition time, the deposited dielectric layer can fully fill in dummy channel hole 406 to form a dummy channel structure 408, but only partially fill in TAC hole 402 and peripheral contact hole 404 to form a first spacer 410 and a second spacer 412, respectively, on the sidewalls of TAC hole 402 and peripheral contact hole 404. Dummy channel structure 408 is thus formed extending vertically through dielectric stack 218. As described above, parts of the dielectric layer deposited on the bottom surfaces of TAC hole 402 and peripheral contact hole 404 can be removed (i.e., etched through) using the bottom punch process, such as high bias DRIE. As a result, first and second spacers 410 and 412 are formed on the sidewalls, but not the bottom surfaces, of TAC hole 402 and peripheral contact hole 404, respectively. In some embodiments, the simultaneously formed first and second spacers 410 and 412 have nominally the same thickness in the radial direction in the plan view.

[0077] Method 800 proceeds to operation 812, as illustrated in FIG 8, in which a conductor layer is deposited (i) filling in the first opening to form a TAC and (ii) filling in the second opening to form a peripheral contact. As illustrated in FIG. 4C, a conductor layer 414 is deposited in TAC hole 402 (as shown in FIG. 4B) to fill the remaining space of TAC hole 402, thereby forming a TAC 416 extending vertically through dielectric stack 218. In some embodiments, an adhesion/barrier layer is first formed along first spacer 410 by depositing Ti/TiN or Ta/TaN using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination

Micron Ex. 1016, p. 39
Micron v. YMTC
IPR2025-00191

thereof. A conductor can then be formed in the remaining space of TAC hole 402 by depositing metals, such as tungsten, using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination thereof. A conductor layer 418 can be simultaneously formed in peripheral contact hole 404 (as shown in FIG. 4B) to form a peripheral contact 420 in contact with peripheral device 405, using the same deposition processes. The excess conductor layer after deposition can be removed by CMP.

[0078] According to one aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A first opening extending vertically through the dielectric stack is formed. A spacer is formed on a sidewall of the first opening. A TAC extending vertically through the dielectric stack is formed by depositing a conductor layer in contact with the spacer in the first opening. A slit extending vertically through the dielectric stack is formed after forming the TAC. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0079] In some embodiments, a staircase structure is formed at one edge of the dielectric stack prior to forming the first opening. A plurality of word line contacts each in contact with a respective one of the conductor layers of the conductor/dielectric layer pairs in the staircase structure are formed, according to some embodiments.

[0080] In some embodiments, a slit structure is formed by depositing a conductor layer in the slit.

[0081] In some embodiments, a dummy channel structure extending vertically through the dielectric stack is formed prior to forming the first opening.

[0082] In some embodiments, to form the first opening, the first opening through the dielectric stack and a second opening outside of the dielectric stack are simultaneously etched. In some embodiments, to form the TAC, the conductor layer is deposited in the first opening to form the TAC and in the second opening to form a peripheral contact.

[0083] In some embodiments, to form the spacer on the sidewall of first opening, a dielectric layer is deposited on the sidewall and a bottom surface of the first opening, and

Micron Ex. 1016, p. 40
Micron v. YMTC
IPR2025-00191

part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The deposition of the dielectric layer includes ALD, and the removal of the part of the dielectric layer includes anisotropic etching on the bottom surface of the first opening, according to some embodiments.

[0084] In some embodiments, to form the spacer on the sidewall of first opening, a plurality of shallow recesses are formed by removing parts of the sacrificial layers abut the sidewall of the first opening, a dielectric layer is deposited filling in the shallow recesses and on the sidewall and a bottom surface of the first opening, and part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The removal of the part of the dielectric layer includes isotropic etching on the sidewall and the bottom surface of the first opening, according to some embodiments.

[0085] In some embodiments, to form the first opening, the first opening through the dielectric stack, a second opening outside of the dielectric stack, and a third opening through the dielectric stack are simultaneously etched. A lateral dimension of the third opening can be smaller than lateral dimensions of the first and second openings.

[0086] In some embodiments, to form the spacer on the sidewall of the first opening, a dielectric layer is deposited (i) fully filling in the third opening to form a dummy channel structure and (2) partially filling in the first opening and the second opening, and parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening are removed. Each of the first, second, and third openings can have a nominally circular shape in the plan view.

[0087] In some embodiments, the dielectric layers in the dielectric/sacrificial layer pairs include silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs include silicon nitride, and the spacer includes silicon oxide.

[0088] According to another aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A dummy channel structure extending vertically through the dielectric stack is formed. A first opening through the dielectric stack and a second opening outside of the dielectric stack are simultaneously etched. A first spacer on a sidewall of the first opening and a second spacer on a sidewall of the second opening are simultaneously formed. A conductor layer is deposited (i) filling in

Micron Ex. 1016, p. 41
Micron v. YMTC
IPR2025-00191

the first opening to form a TAC and (ii) filling in the second opening to form a peripheral contact. A slit extending vertically through the dielectric stack is formed after forming the TAC and peripheral device. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0089] In some embodiments, a staircase structure is formed at one edge of the dielectric stack prior to forming the dummy channel structure. A plurality of word line contacts each in contact with a respective one of the conductor layers of the conductor/dielectric layer pairs in the staircase structure are formed, according to some embodiments.

[0090] In some embodiments, a slit structure is formed by depositing a conductor layer in the slit.

[0091] In some embodiments, to form the first spacer on the sidewall of the first opening, a dielectric layer is deposited on the sidewall and a bottom surface of the first opening, and part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The deposition of the dielectric layer includes ALD, and the removal of the part of the dielectric layer includes anisotropic etching on the bottom surface of the first opening, according to some embodiments.

[0092] In some embodiments, to form the spacer on the sidewall of first opening, a plurality of shallow recesses are formed by removing parts of the sacrificial layers abutting the sidewall of the first opening, a dielectric layer is deposited filling in the shallow recesses and on the sidewall and a bottom surface of the first opening, and part of the dielectric layer that is deposited on the bottom surface of the first opening is removed. The removal of the part of the dielectric layer includes isotropic etching on the sidewall and the bottom surface of the first opening, according to some embodiments.

[0093] In some embodiments, the dielectric layers in the dielectric/sacrificial layer pairs include silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs include silicon nitride, and the first and second spacers include silicon oxide.

[0094] According to still another aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A dielectric stack including a plurality of dielectric/sacrificial layer pairs is formed on a substrate. A channel structure extending vertically through the dielectric stack is formed. A first opening through the dielectric

stack, a second opening outside of the dielectric stack, and a third opening through the dielectric stack are simultaneously etched. A lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings. A dielectric layer is deposited (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening. Parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening are removed. A conductor layer is deposited (i) filling in the first opening to form a TAC and (ii) filling in the second opening to form a peripheral contact. A slit extending vertically through the dielectric stack is formed after forming the TAC and peripheral device. A memory stack including a plurality of conductor/dielectric layer pairs is formed on the substrate by replacing, through the slit, the sacrificial layers in the dielectric/sacrificial layer pairs with a plurality of conductor layers.

[0095] In some embodiments, a staircase structure is formed at one edge of the dielectric stack prior to etching the first, second, and third openings. A plurality of word line contacts each in contact with a respective one of the conductor layers of the conductor/dielectric layer pairs in the staircase structure are formed, according to some embodiments.

[0096] In some embodiments, a slit structure is formed by depositing a conductor layer in the slit.

[0097] In some embodiments, each of the first, second, and third openings has a nominally circular shape in the plan view.

[0098] In some embodiments, the dielectric layers in the dielectric/sacrificial layer pairs includes silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs includes silicon nitride, and the dielectric layer filling the first, second, and third openings include silicon oxide.

[0099] According to yet another aspect of the present disclosure, a 3D memory device includes a substrate, a memory stack on the substrate including a plurality of conductor/dielectric layer pairs, a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack, a TAC extending vertically through the conductor/dielectric layer pairs in the memory stack, and a dummy channel structure fully filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.

Micron Ex. 1016, p. 43
Micron v. YMTC
IPR2025-00191

[0100] In some embodiments, the 3D memory device further includes a peripheral device on the substrate, and a peripheral contact outside of the memory stack and in contact with the peripheral device.

[0101] In some embodiments, each of the TAC and peripheral contact includes a spacer with a nominally same thickness. The dielectric layer in the dummy channel structure and the spacers in the TAC and peripheral contact include silicon oxide, according to some embodiments.

[0102] In some embodiments, the 3D memory device further includes a lower memory deck on the substrate and an upper memory deck above the lower memory stack. In some embodiments, the channel structure includes a lower channel structure extending vertically through the lower memory deck, an upper channel structure extending vertically through the upper memory deck, and an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.

[0103] In some embodiments, the 3D memory device further includes a staircase structure at one edge of the memory stack, and a plurality of word line contacts each in contact with a respective one of the conductor layers of the conductor/dielectric layer pairs in the staircase structure.

[0104] The foregoing description of the specific embodiments will so reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

[0105] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries

Micron Ex. 1016, p. 44
Micron v. YMTC
IPR2025-00191

can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0106] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0107] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

Micron Ex. 1016, p. 45
Micron v. YMTC
IPR2025-00191

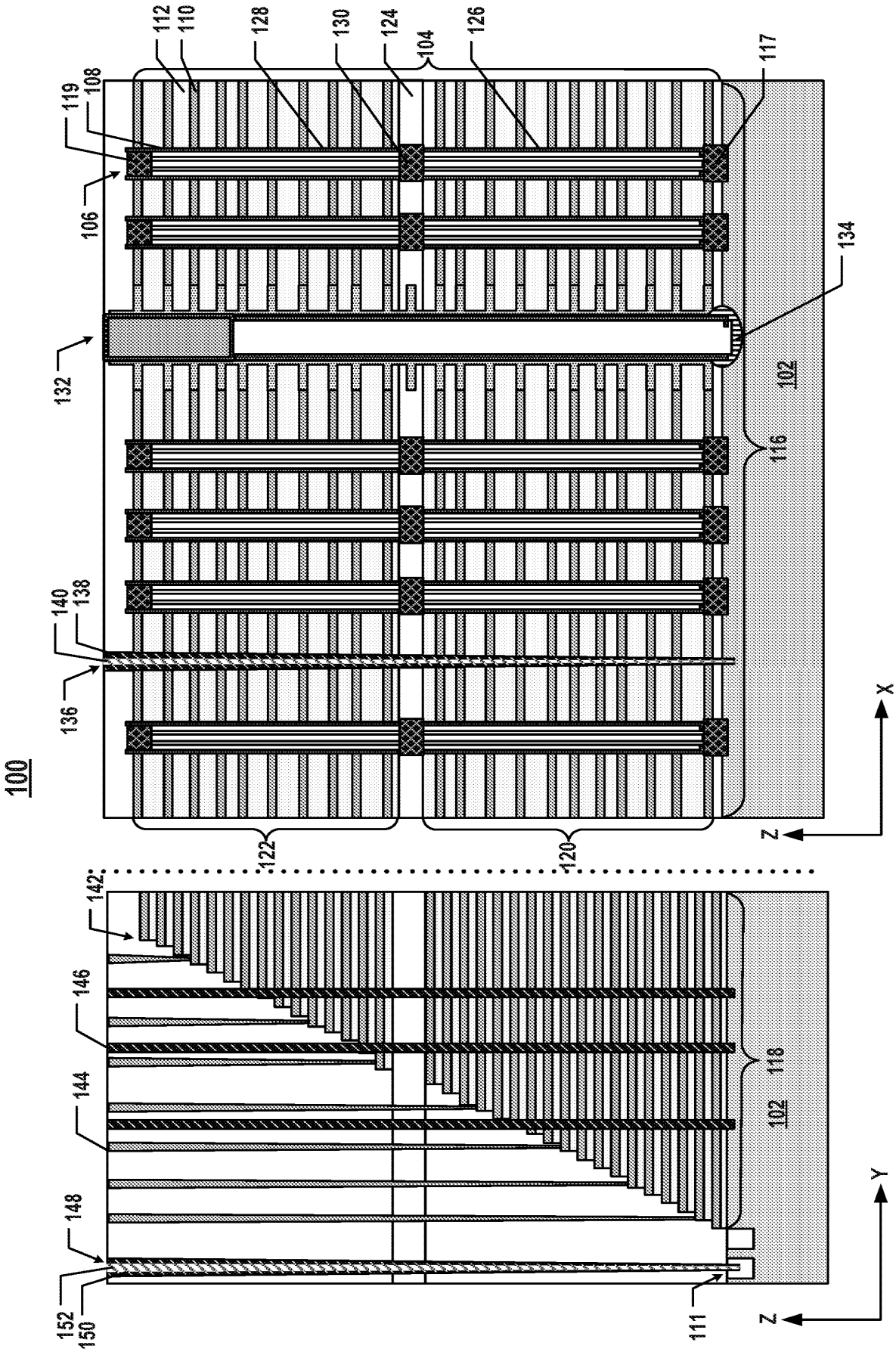

100
112
110
128
130
124
104
126
117
108
119
106
134
132
102
116
140
138
136
122
120
X
Z
142
146
144
148
152
150
111
118
102
Y
Z

FIG. 1

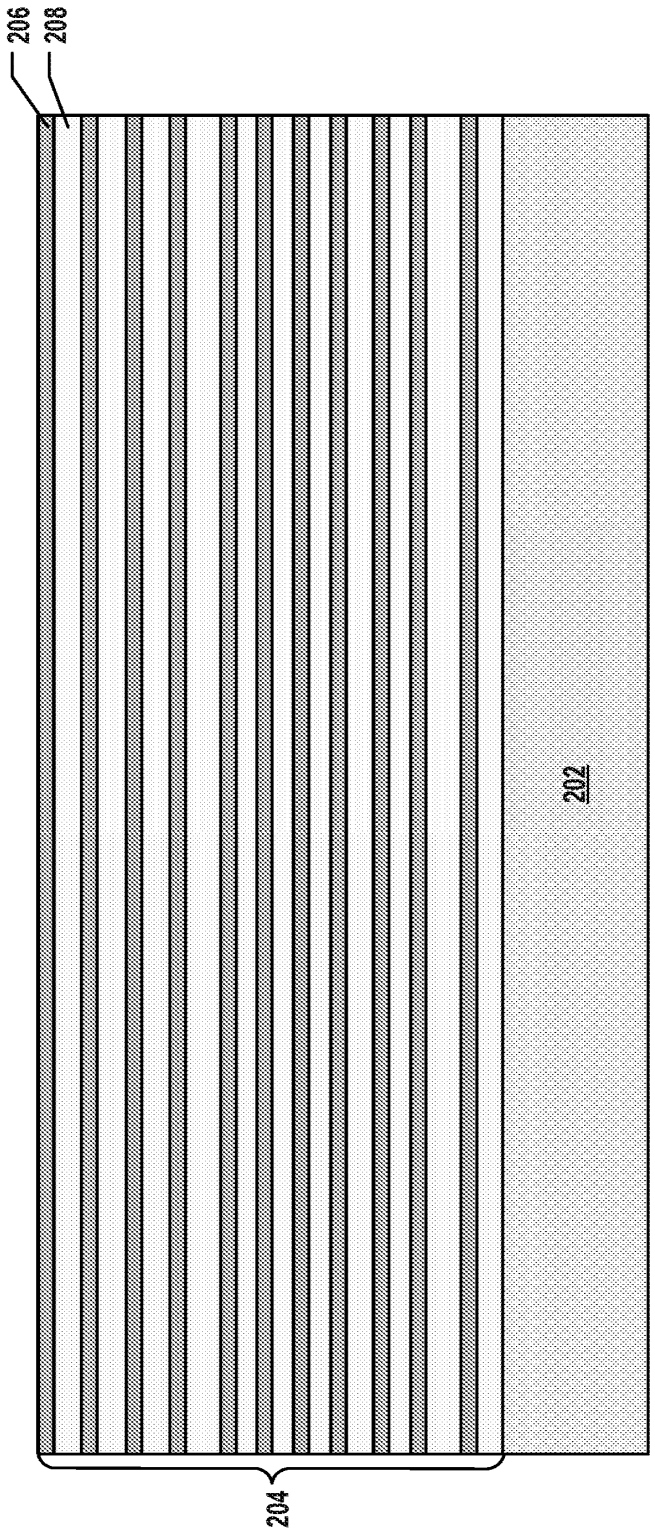


FIG. 2A

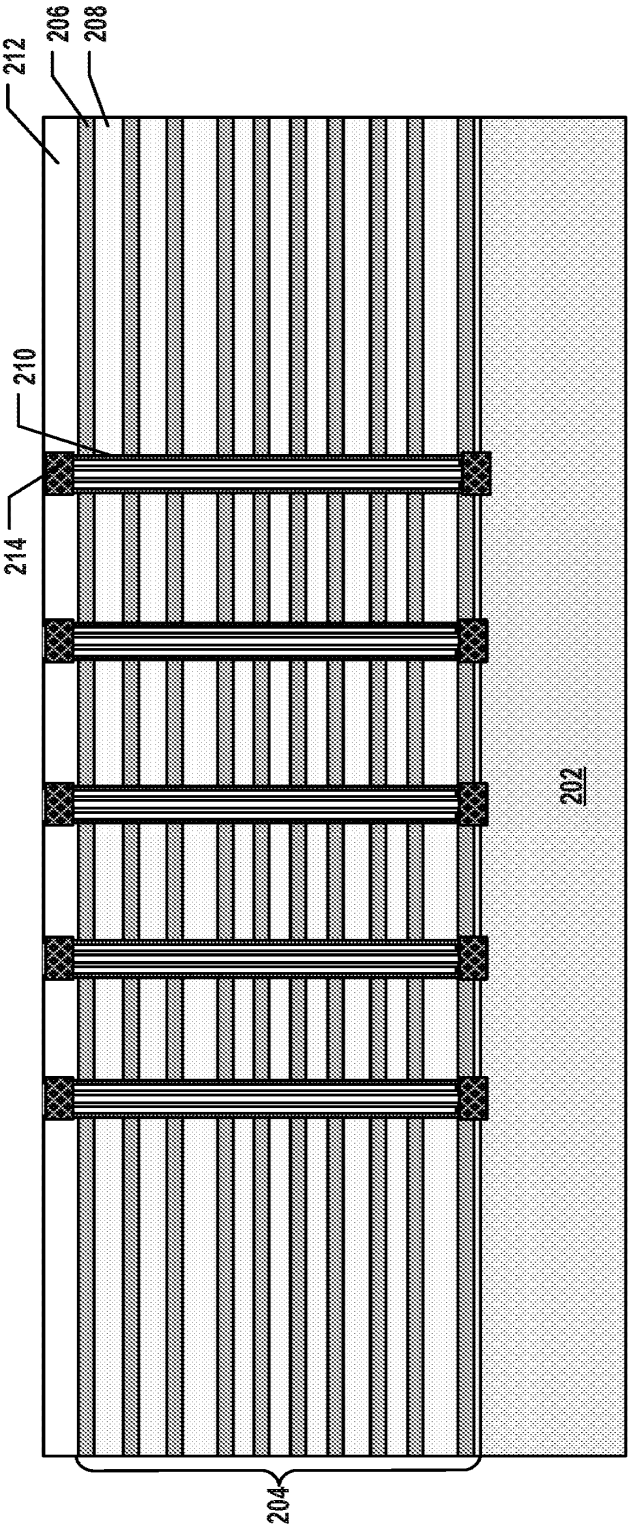


FIG. 2B

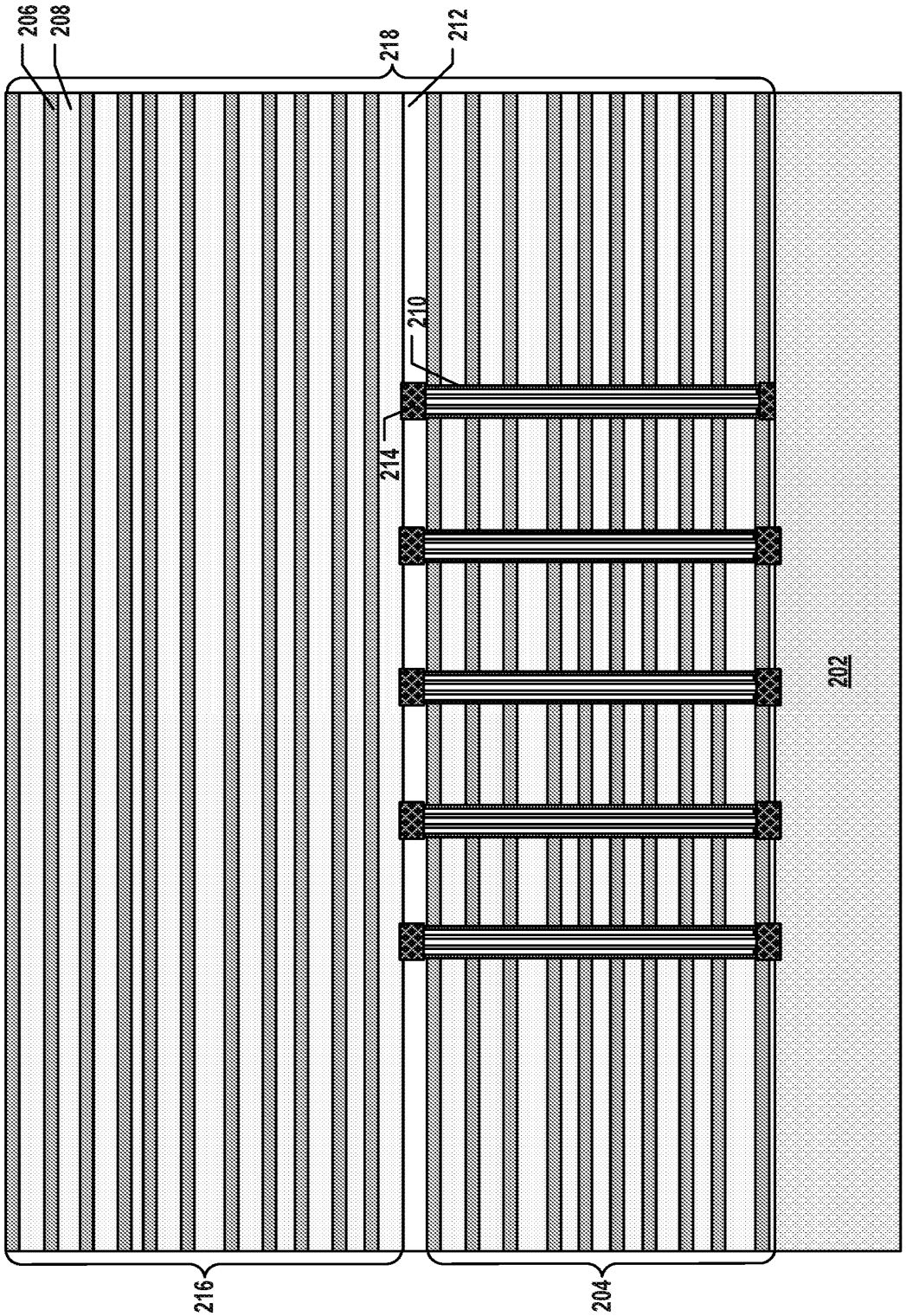


FIG.2C

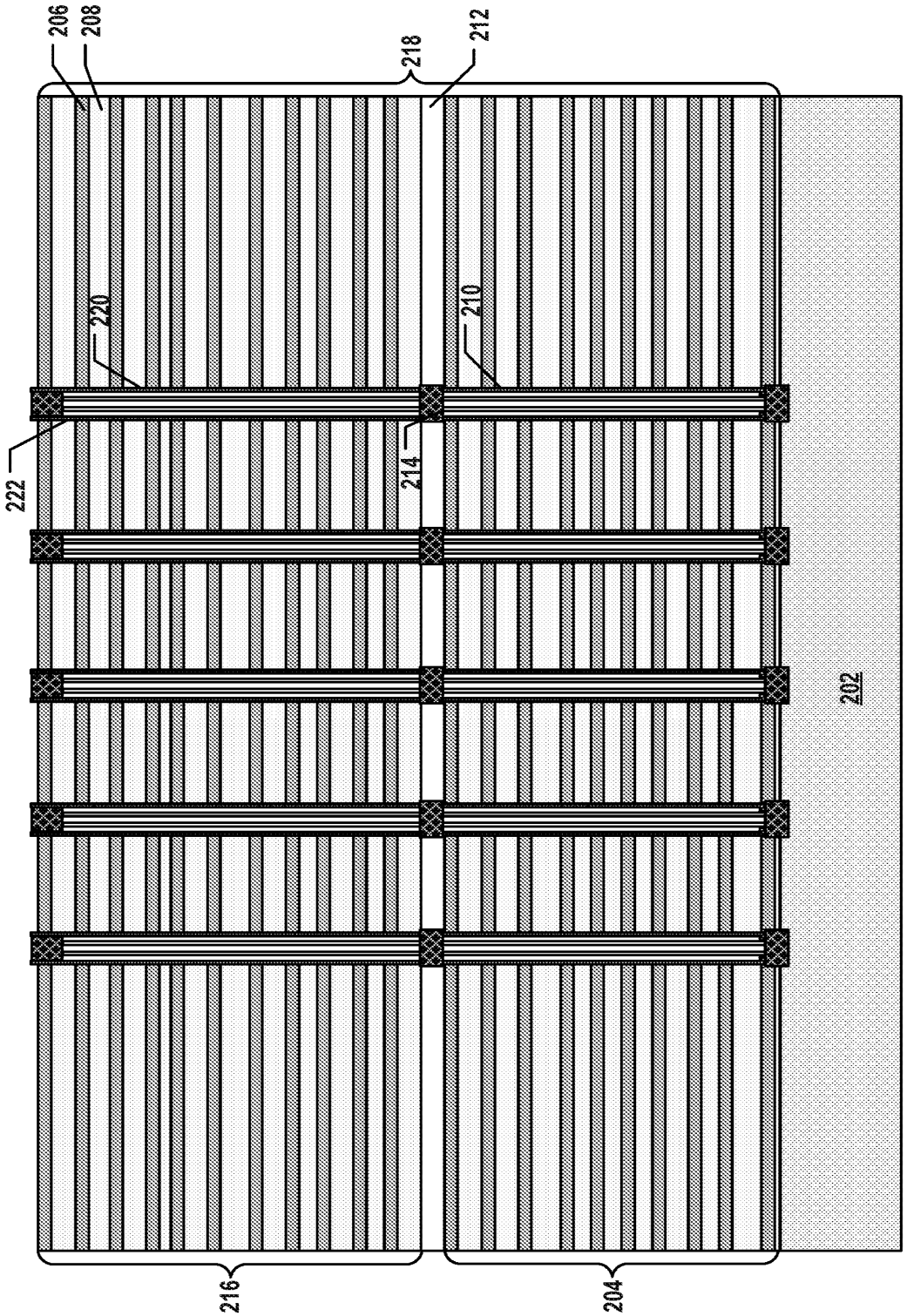


FIG. 2D

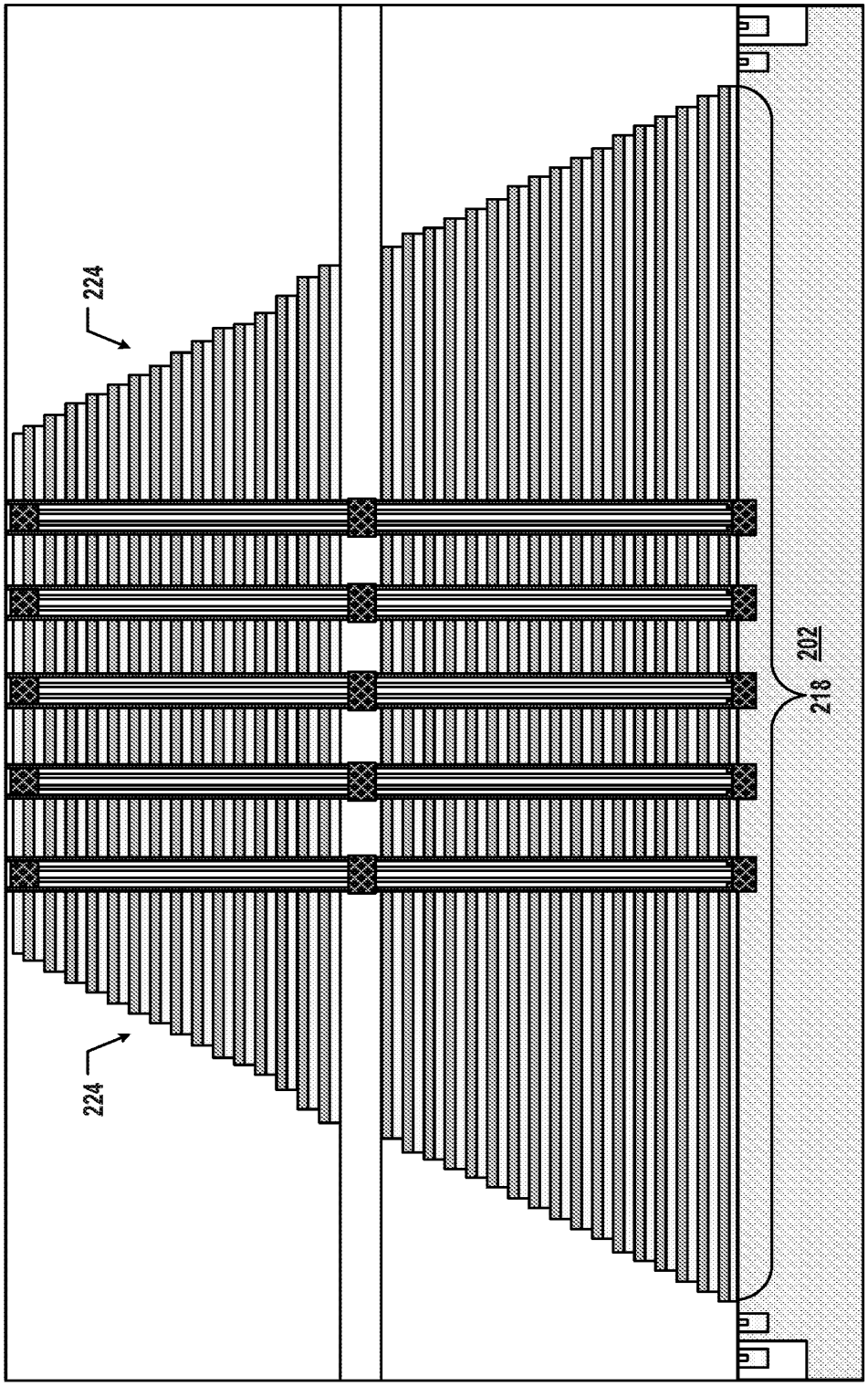


FIG. 2E

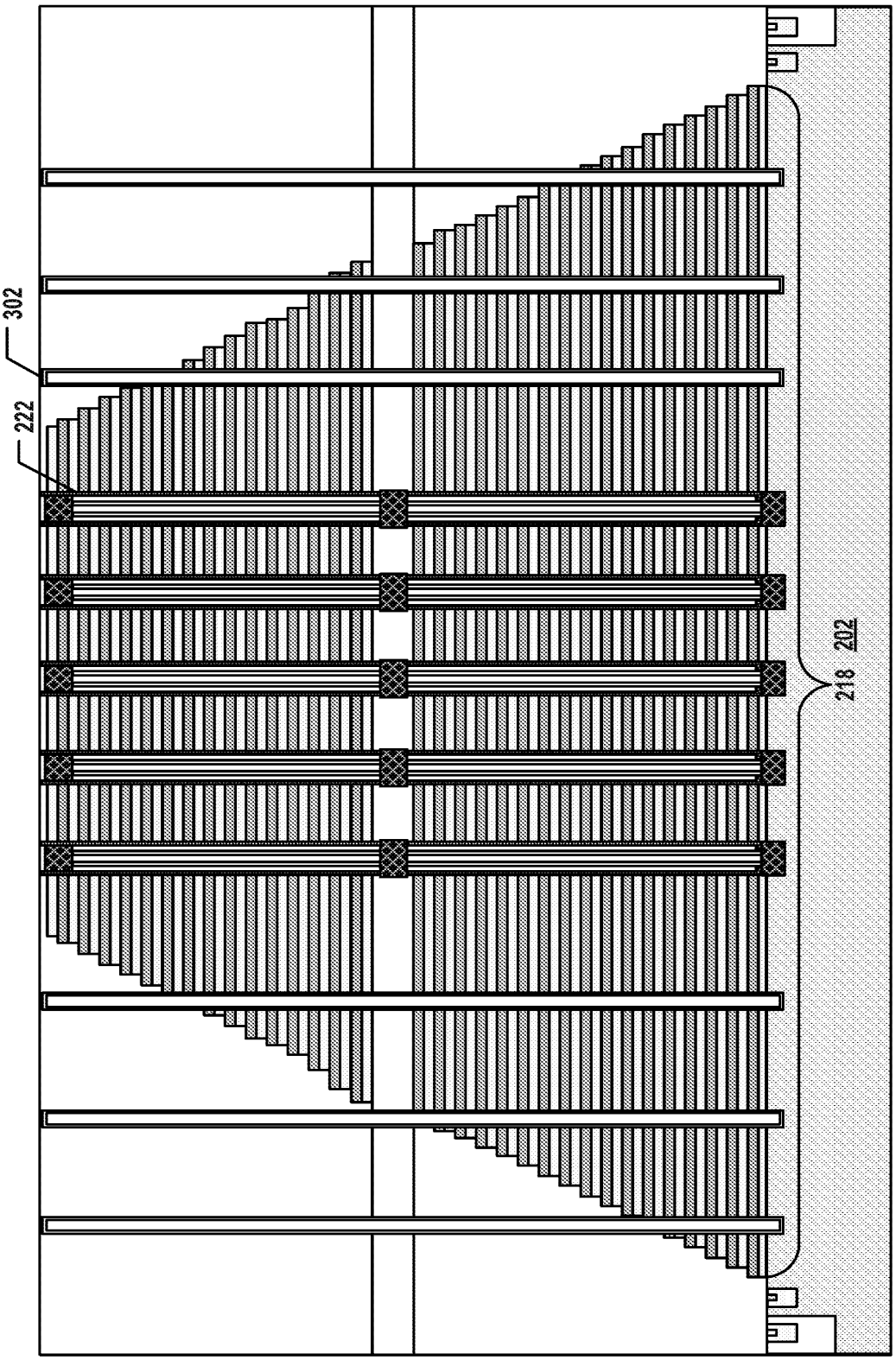


FIG. 3A

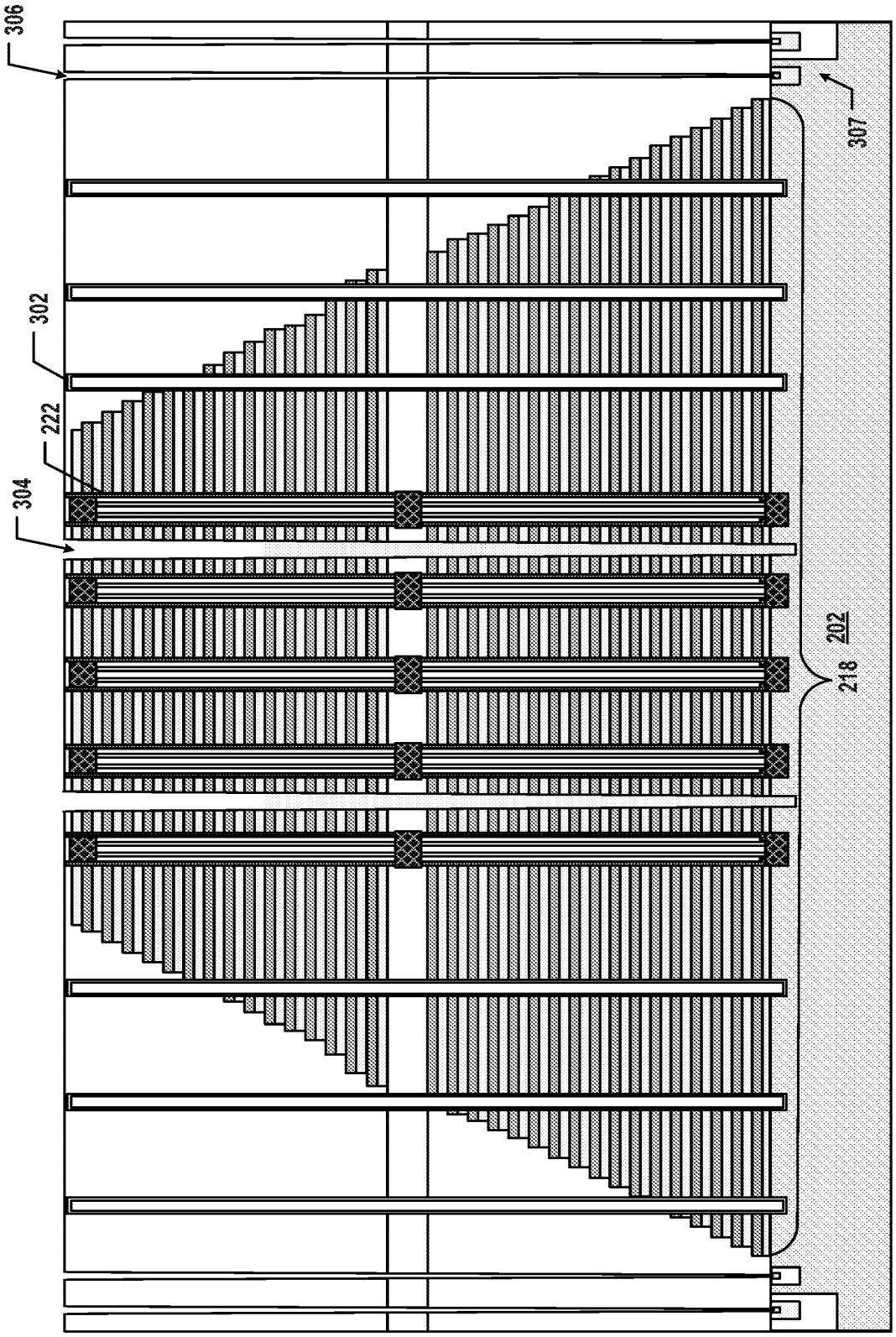


FIG. 3B

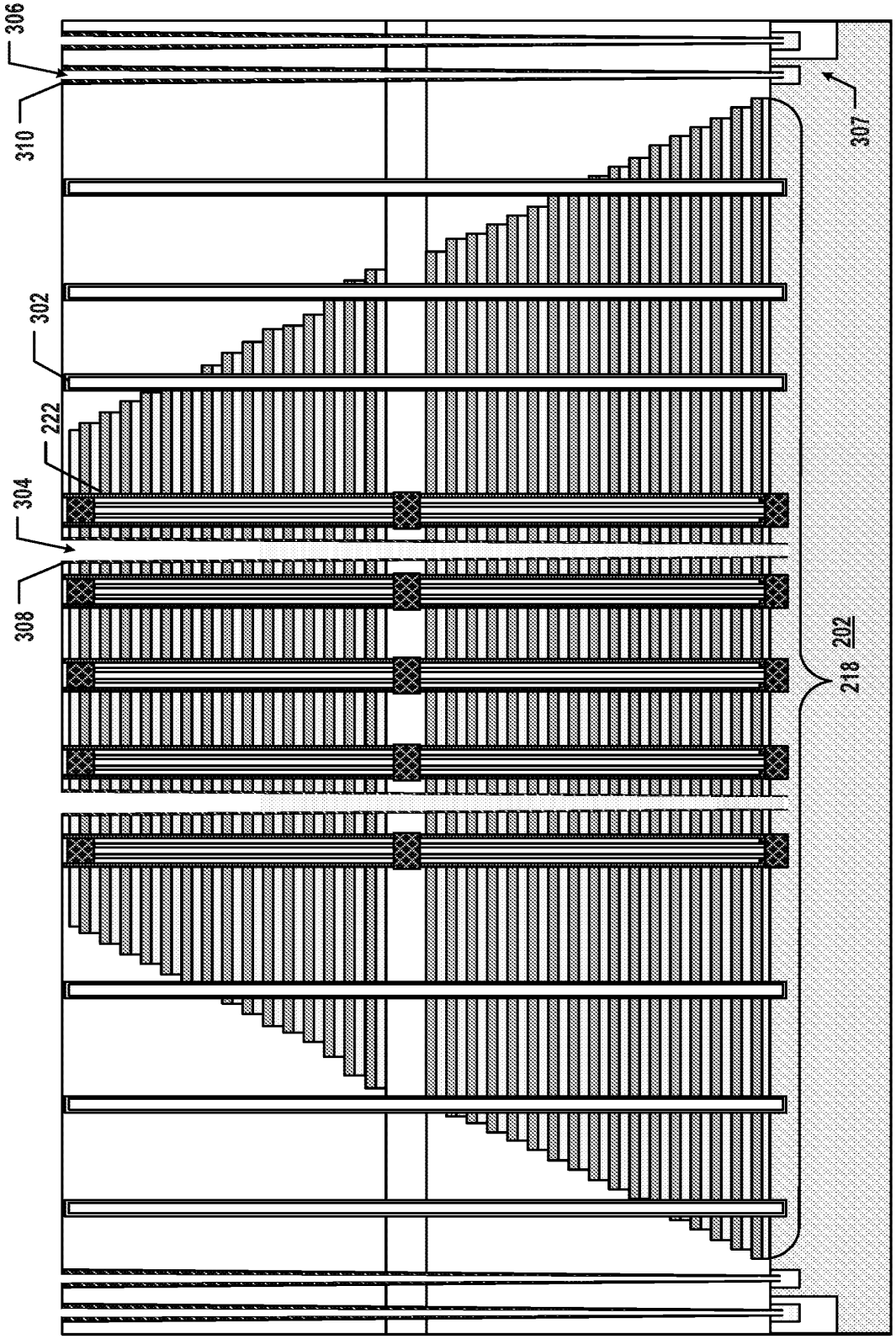


FIG. 3C

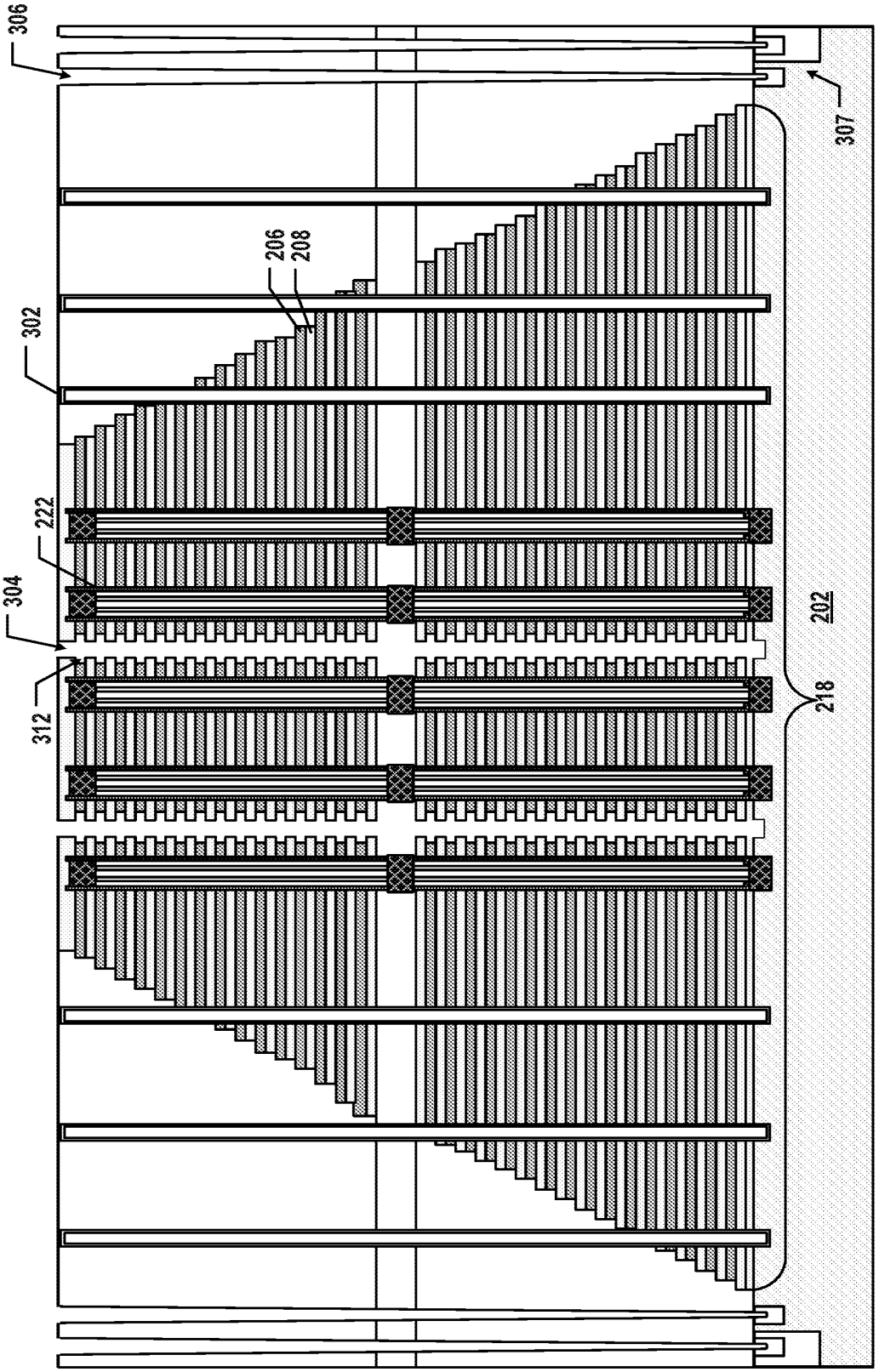


FIG. 3D

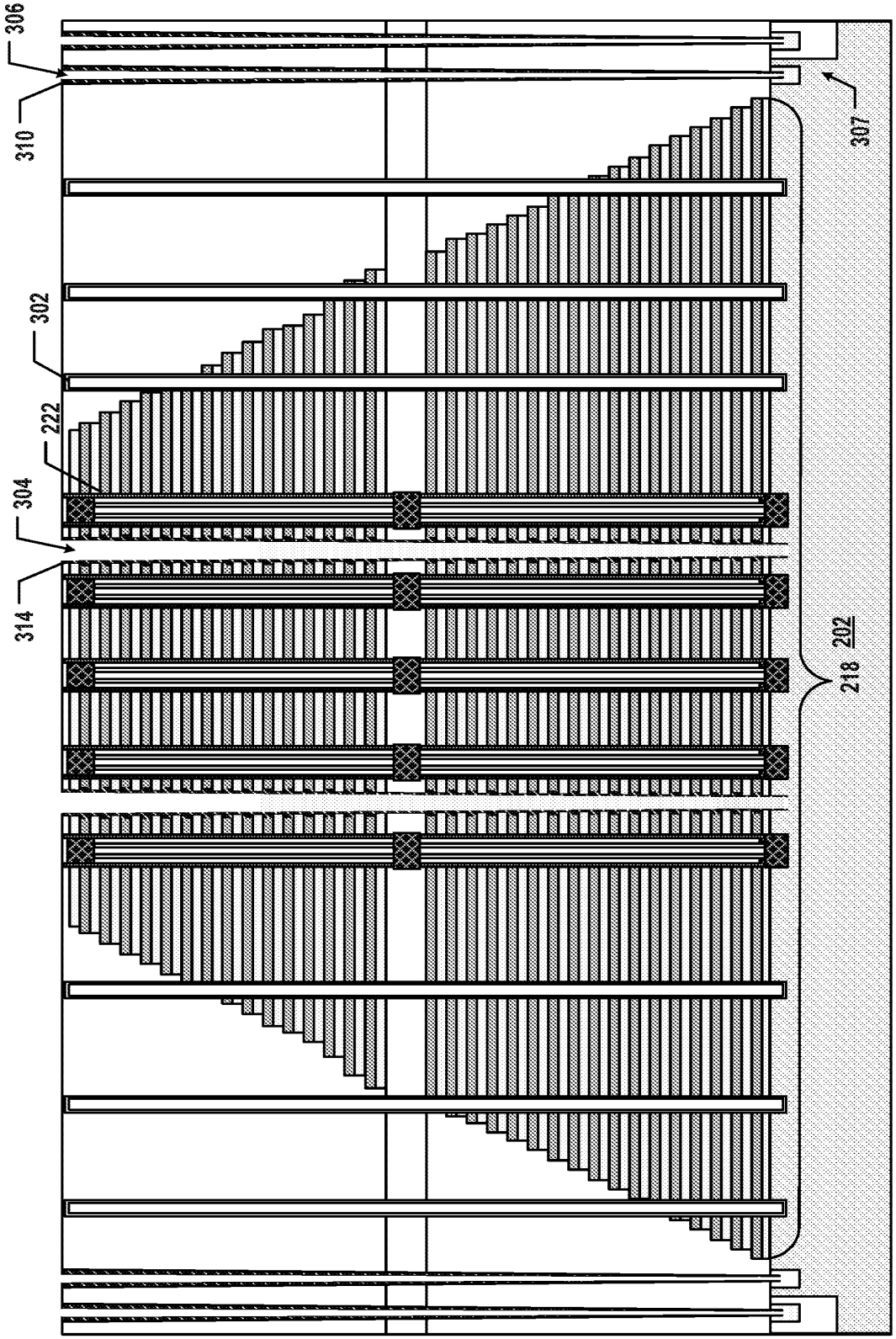


FIG. 3E

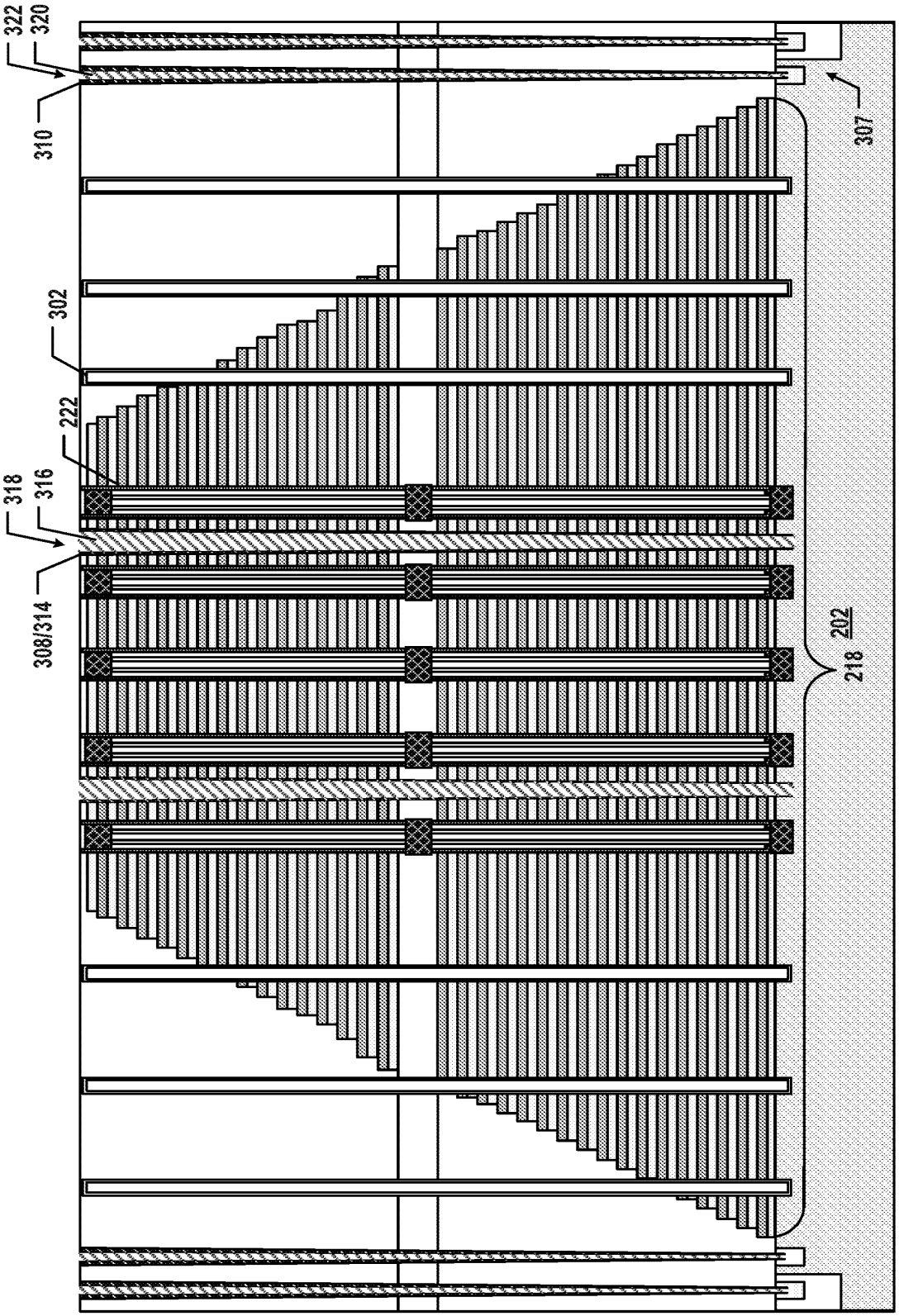


FIG. 3F

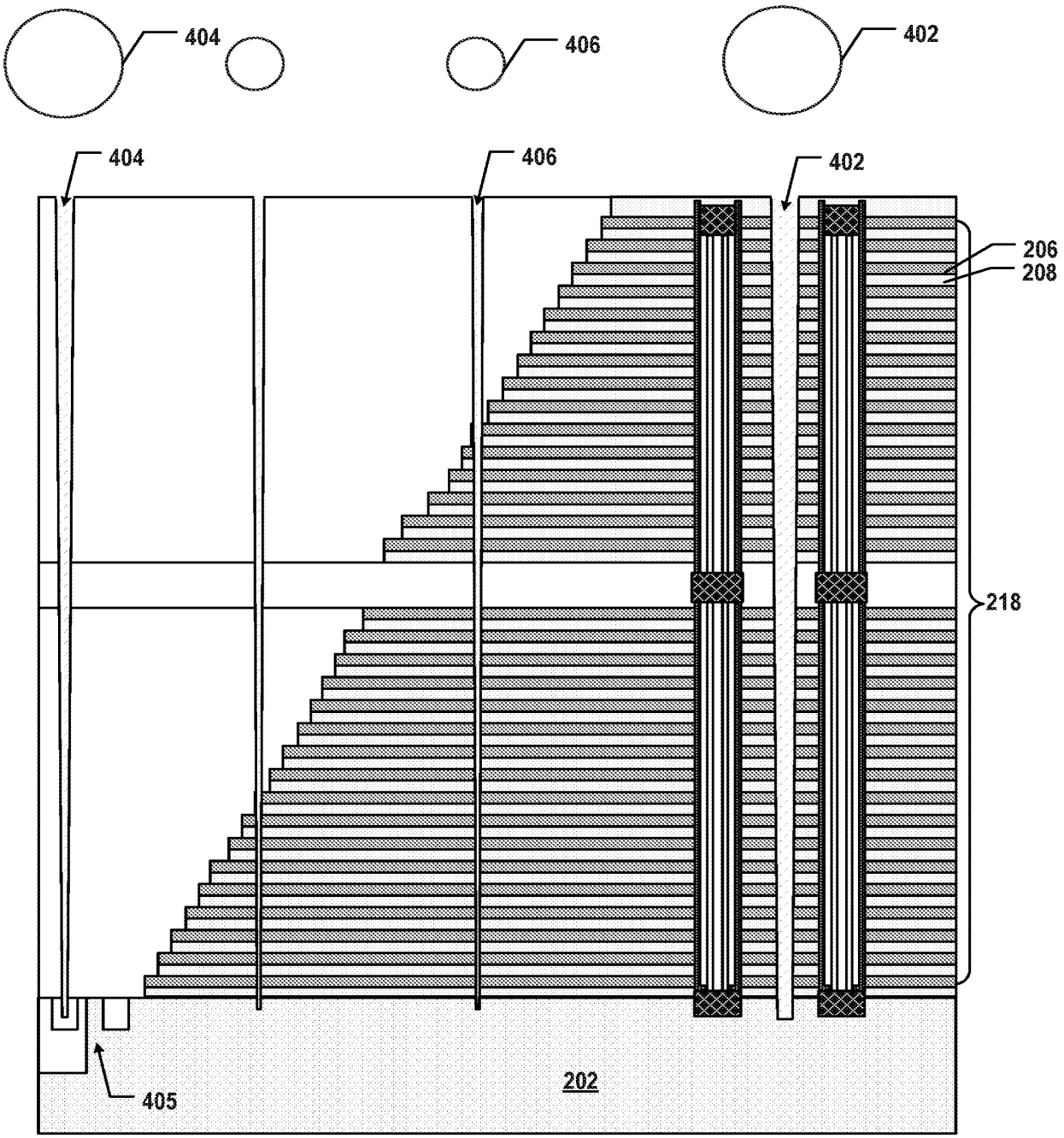


FIG. 4A

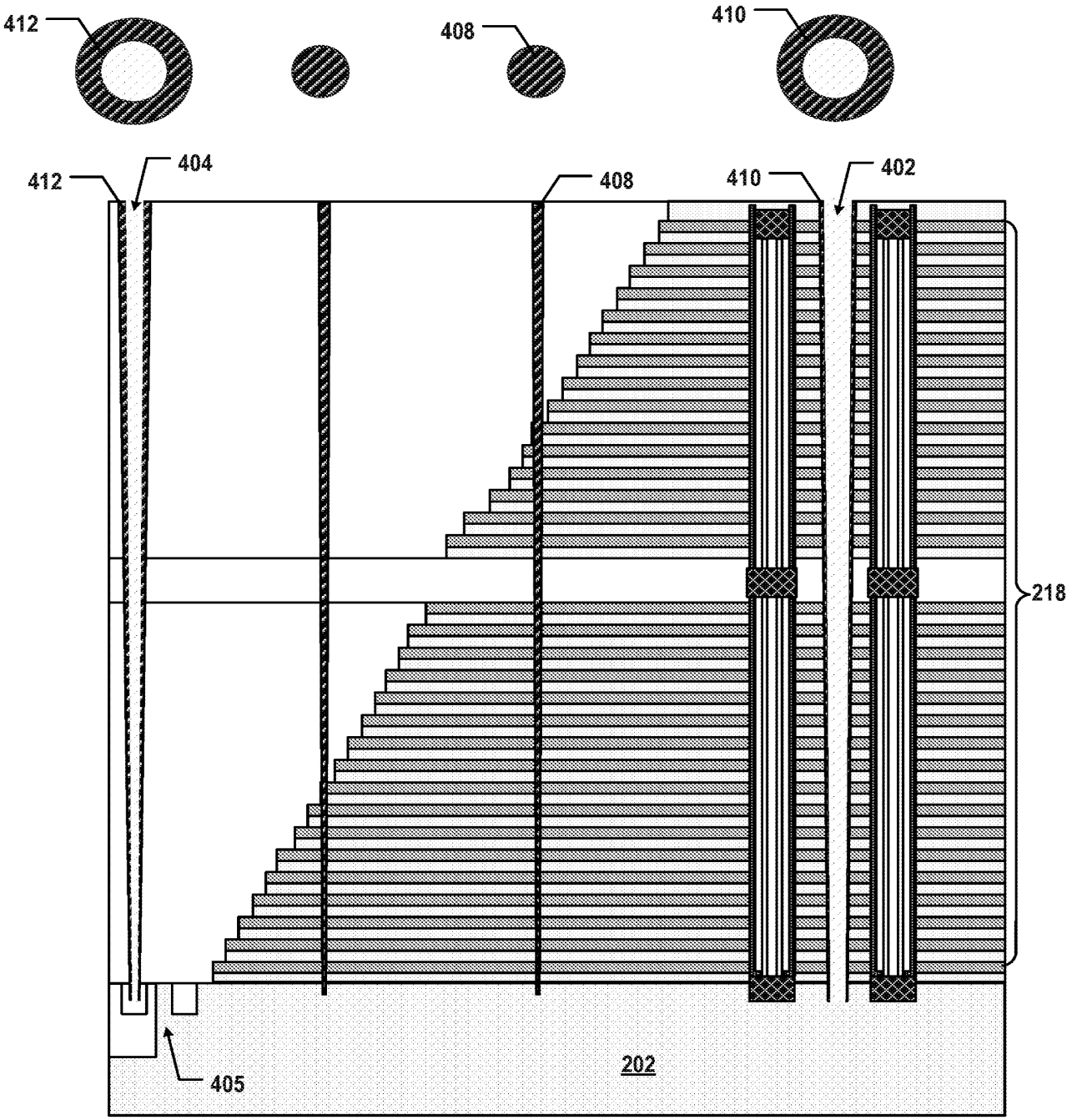


FIG. 4B

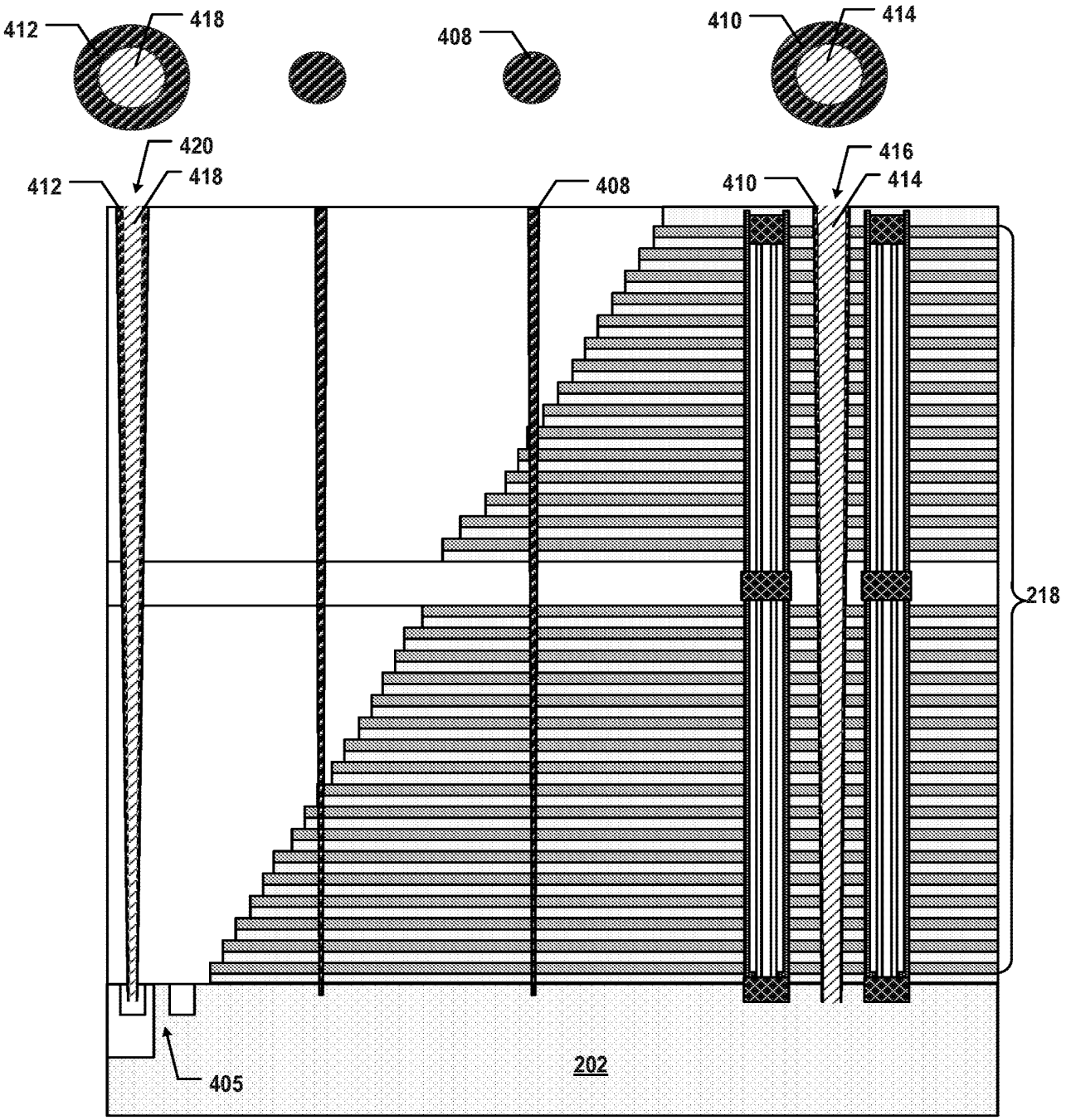


FIG. 4C

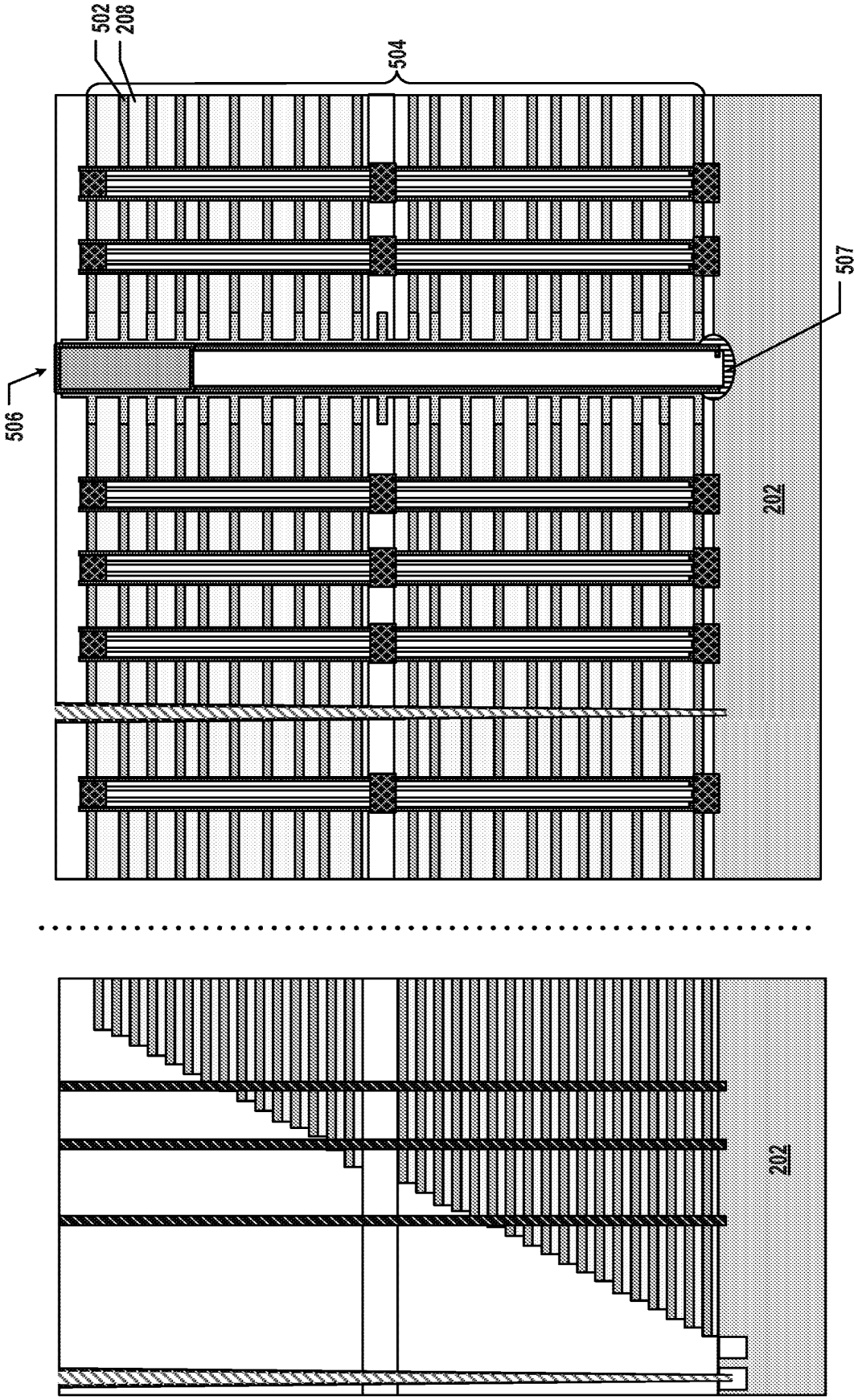


FIG. 5A

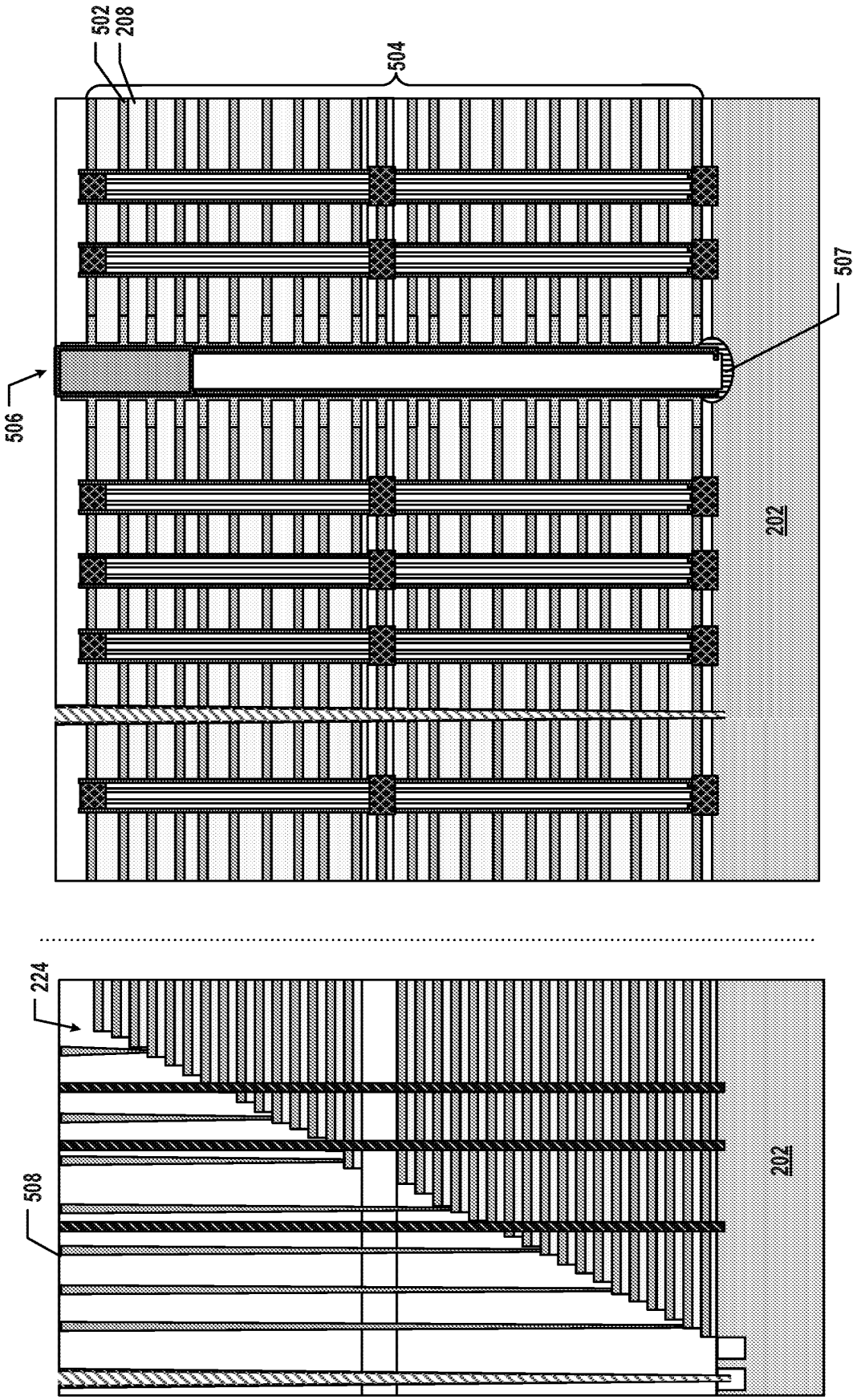


FIG. 5B

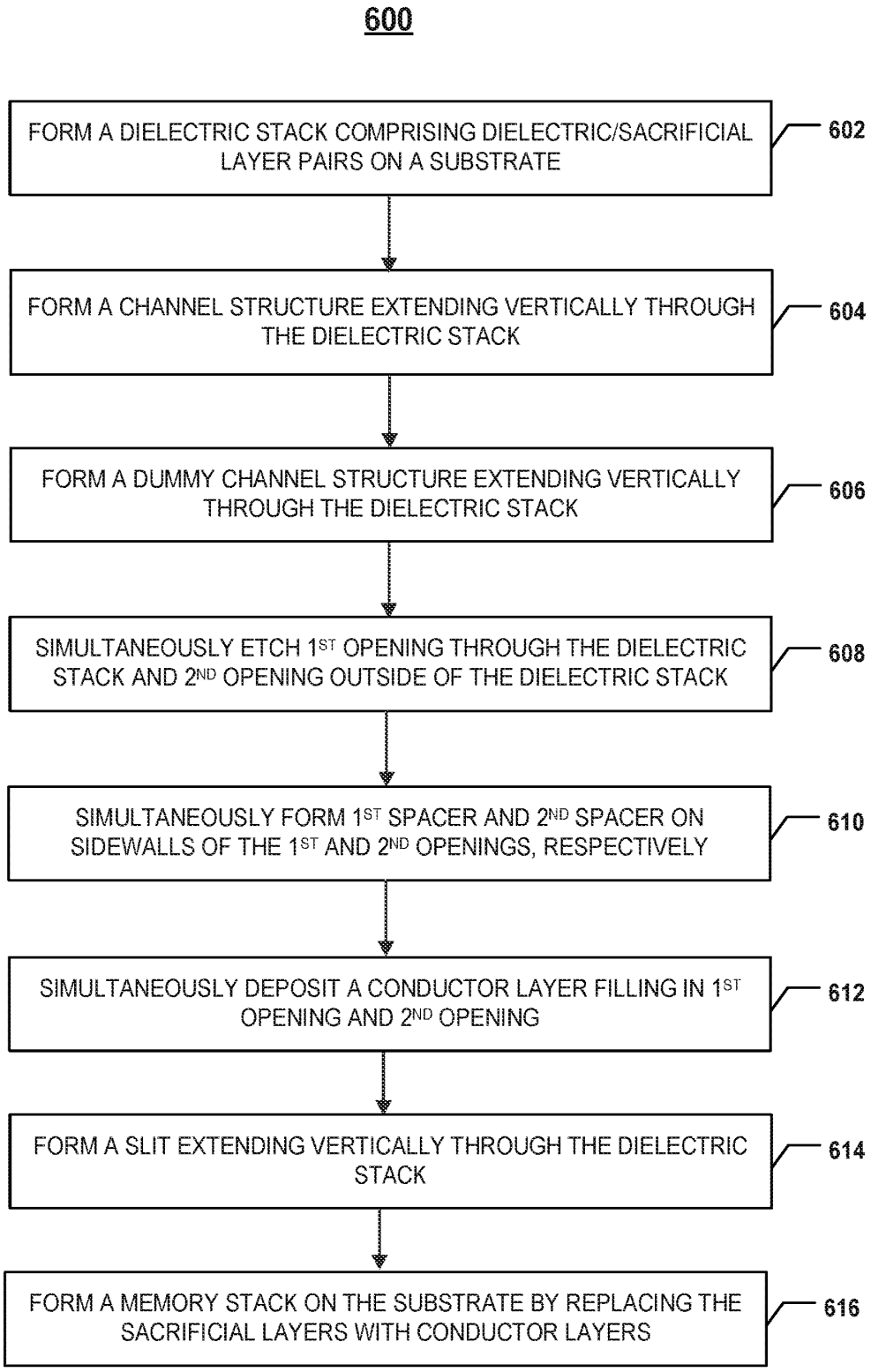

600
FORM A DIELECTRIC STACK COMPRISING DIELECTRIC/SACRIFICIAL LAYER PAIRS ON A SUBSTRATE
602
FORM A CHANNEL STRUCTURE EXTENDING VERTICALLY THROUGH THE DIELECTRIC STACK
604
FORM A DUMMY CHANNEL STRUCTURE EXTENDING VERTICALLY THROUGH THE DIELECTRIC STACK
606
SIMULTANEOUSLY ETCH 1ST OPENING THROUGH THE DIELECTRIC STACK AND 2ND OPENING OUTSIDE OF THE DIELECTRIC STACK
608
SIMULTANEOUSLY FORM 1ST SPACER AND 2ND SPACER ON SIDEWALLS OF THE 1ST AND 2ND OPENINGS, RESPECTIVELY
610
SIMULTANEOUSLY DEPOSIT A CONDUCTOR LAYER FILLING IN 1ST OPENING AND 2ND OPENING
612
FORM A SLIT EXTENDING VERTICALLY THROUGH THE DIELECTRIC STACK
614
FORM A MEMORY STACK ON THE SUBSTRATE BY REPLACING THE SACRIFICIAL LAYERS WITH CONDUCTOR LAYERS
616

FIG. 6

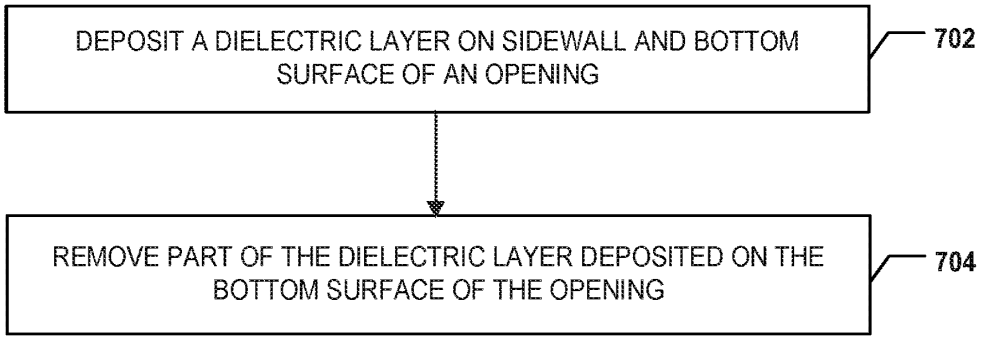

DEPOSIT A DIELECTRIC LAYER ON SIDEWALL AND BOTTOM SURFACE OF AN OPENING
702
REMOVE PART OF THE DIELECTRIC LAYER DEPOSITED ON THE BOTTOM SURFACE OF THE OPENING
704

FIG. 7A

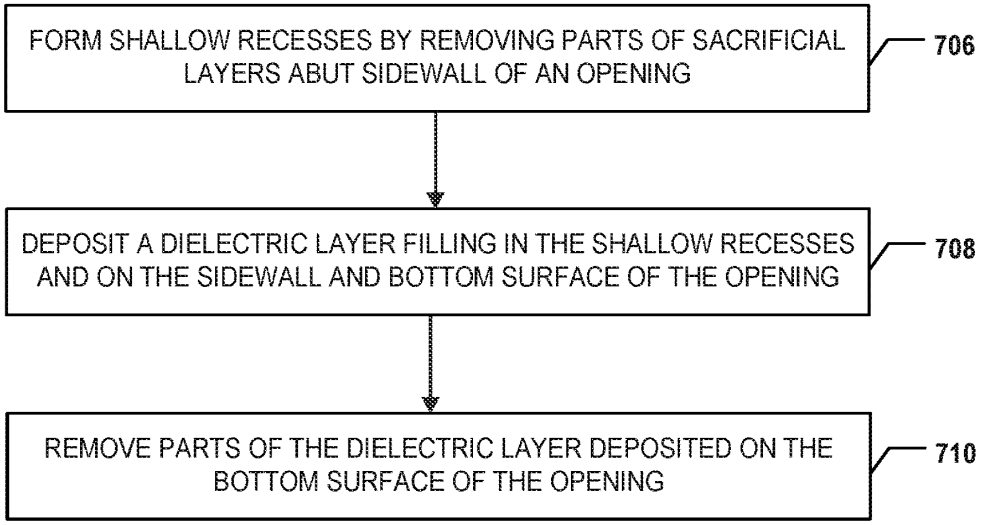

FORM SHALLOW RECESSES BY REMOVING PARTS OF SACRIFICIAL LAYERS ABUT SIDEWALL OF AN OPENING
706
DEPOSIT A DIELECTRIC LAYER FILLING IN THE SHALLOW RECESSES AND ON THE SIDEWALL AND BOTTOM SURFACE OF THE OPENING
708
REMOVE PARTS OF THE DIELECTRIC LAYER DEPOSITED ON THE BOTTOM SURFACE OF THE OPENING
710

FIG. 7B

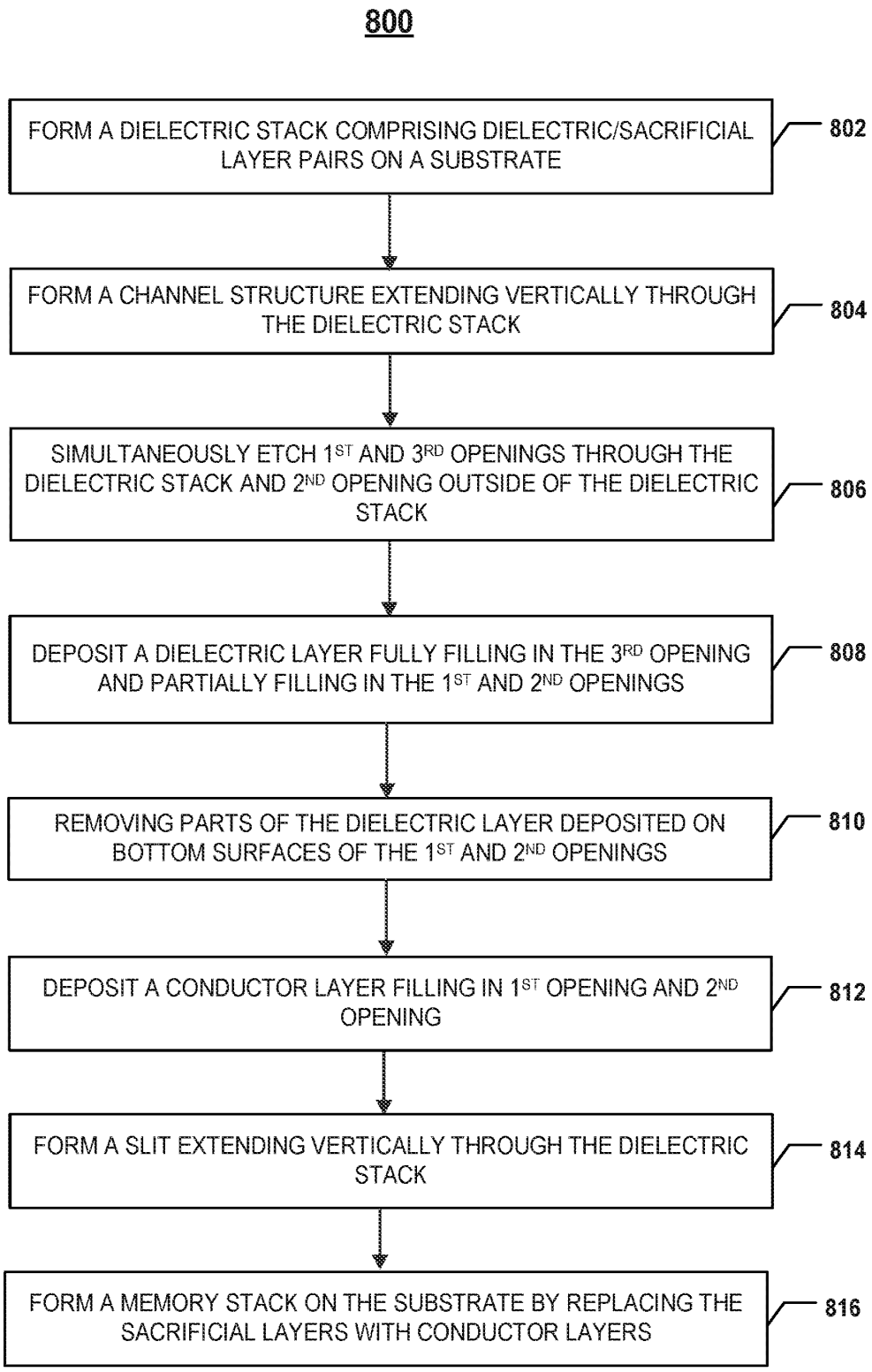

800
FORM A DIELECTRIC STACK COMPRISING DIELECTRIC/SACRIFICIAL LAYER PAIRS ON A SUBSTRATE
802
FORM A CHANNEL STRUCTURE EXTENDING VERTICALLY THROUGH THE DIELECTRIC STACK
804
SIMULTANEOUSLY ETCH 1ST AND 3RD OPENINGS THROUGH THE DIELECTRIC STACK AND 2ND OPENING OUTSIDE OF THE DIELECTRIC STACK
806
DEPOSIT A DIELECTRIC LAYER FULLY FILLING IN THE 3RD OPENING AND PARTIALLY FILLING IN THE 1ST AND 2ND OPENINGS
808
REMOVING PARTS OF THE DIELECTRIC LAYER DEPOSITED ON BOTTOM SURFACES OF THE 1ST AND 2ND OPENINGS
810
DEPOSIT A CONDUCTOR LAYER FILLING IN 1ST OPENING AND 2ND OPENING
812
FORM A SLIT EXTENDING VERTICALLY THROUGH THE DIELECTRIC STACK
814
FORM A MEMORY STACK ON THE SUBSTRATE BY REPLACING THE SACRIFICIAL LAYERS WITH CONDUCTOR LAYERS
816

FIG. 8

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☒ The attached application, or

☐ United States application or PCT international application number _____

filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 153988** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

Micron Ex. 1016, p. 67
Micron v. YMTC
IPR2025-00191

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Mei Lau Guo Date: 2018.9.5

Signature of Inventor:

Inventor: Yushi Hu Date: 2018.08.22

Signature of Inventor:

Inventor: Ji Xia Date: 2018/8/22

Signature of Inventor: Ji Xia

Inventor: Hongbin Zhu Date: 2018/8/29

Signature of Inventor:

Micron Ex. 1016, p. 68
Micron v. YMTC
IPR2025-00191

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	Mei Lan GUO
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	10018-01-0015-US-DIV1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20170125430	A1	2017-05-04	NISHIKAWA et al.	
	2	20140175532	A1	2014-06-26	Chen	
	3	20160099255	A1	2016-04-07	Lai	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	108377660	CN	A	2018-08-07	SANDISK TECHNOLOGIES LLC		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV1

	2	108140644	CN	A	2018-06-08	SANDISK TECHNOLOGIES LLC		
	3	106920794	CN	A	2017-07-04	YANGTZE MEMORY TECH CO LTD		
	4	106910746	CN	A	2017-06-30	YANGTZE MEMORY TECH CO LTD		
	5	106920796	CN	A	2017-07-04	YANGTZE MEMORY TECH CO LTD		
	6	106256005	CN	A	2016-12-21	SANDISK TECHNOLOGIES INC		
	7	107771356	CN	A	2018-03-06	SANDISK TECHNOLOGIES INC		

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Search Report issued in corresponding International Application No. PCT/CN2018/101482, mailed May 5, 2019, 5 pages	
	2	Written Opinion of the International Searching Authority issued in corresponding International Application No. PCT/CN2018/101482, mailed May 5, 2019, 4 pages	

If you wish to add additional non-patent literature document citation information please click the Add button Add

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV1

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2020-01-17
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan GUO
Filer:	Zhiwei Zou/Anna O'Connor
Attorney Docket Number:	10018-01-0015-US-DIV1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1720**

Electronic Acknowledgement Receipt

EFS ID:	38322655
Application Number:	16745342
International Application Number:	
Confirmation Number:	2958
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan GUO
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0015-US-DIV1
Receipt Date:	17-JAN-2020
Filing Date:	
Time Stamp:	00:47:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1720
RAM confirmation Number	E20201G147511926
Deposit Account	602227
Authorized User	Anna O'Connor

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	10018-01-0015-US-DIV1_UtilityPatentAppTransmittal.pdf	369118 0fb080b23692df4c120c48a5e82297009b72ca66	no	2
Warnings:					
Information:					
2	Application Data Sheet	10018-01-0015-US-DIV1_ADS.pdf	1829279 28feceeb1d3d0e096456aa0600191dc7899da90c	no	9
Warnings:					
Information:					
3		10018-01-0015-US-DIV1_FINALApplication.pdf	189262 da90f70bb65eba0246f35c4ec8fea80553a86add	yes	34

Multipart Description/PDF files in .zip description

Document Description	Start	End
Abstract	34	34
Claims	30	33
Specification	1	29

Warnings:					
Information:					
4	Drawings-only black and white line drawings	10018-01-0015-US-DIV1_FINALDrawings.pdf	148793 89a0c09504ec17c9128cff07840d42654c8a29de	no	20
Warnings:					
Information:					
5	Oath or Declaration filed	10018-01-0015-US_SignedFormalPapers.pdf	4566449 b2556008c56fba9052ebebb08081adacacb941bb	no	3

Warnings:					
Information:					
6	Power of Attorney	10018-01-0015-US-DIV1_GenPOA.pdf	330156 687f6a638c1f40351021fc2508bdb41fbc9bcd21	no	2
Warnings:					
Information:					
7	Information Disclosure Statement (IDS) Form (SB08)	10018-01-0015-US-DIV1_IDS-SB08.pdf	612571 7cd463e3f342af1c907e9f1d6524956e662ce19b	no	5
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	34833 e4a596e9ad295af341a7da58b9d359152a524728	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	8080461	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DocCode – SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 16745342 Document Date: 01/17/2020

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

- Drawing

At the time of document entry (noted above):

- USPTO employees may access SCORE content via DAV or via the SCORE web page.
- External customers may access SCORE content via PAIR using the Supplemental Content tab.

Form Revision Date: March 1, 2019

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5916141

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
MEI LAN GUO	09/05/2018
YUSHI HU	08/22/2018
JI XIA	08/22/2018
HONGBIN ZHU	08/29/2018

RECEIVING PARTY DATA

Name:	YANGTZE MEMORY TECHNOLOGIES CO., LTD.
Street Address:	18 GAOXIN 4TH ROAD
Internal Address:	EAST LAKE HIGH-TECH DEVELOPMENT ZONE
City:	WUHAN, HUBEI
State/Country:	CHINA

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	16745342

CORRESPONDENCE DATA

Fax Number: (703)821-8128

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 703-995-9887
Email: uspto@bayes.law
Correspondent Name: BAYES PLLC
Address Line 1: 1765 GREENSBORO STATION PLACE
Address Line 2: SUITE 900
Address Line 4: MCLEAN, VIRGINIA 22102

ATTORNEY DOCKET NUMBER:	10018-01-0015-US-DIV1
NAME OF SUBMITTER:	ZHIWEI ZOU
SIGNATURE:	/Zhiwei Zou/
DATE SIGNED:	01/17/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 3

source=10018-01-0015-US_SignedFormalPapers#page1.tif
source=10018-01-0015-US_SignedFormalPapers#page2.tif
source=10018-01-0015-US_SignedFormalPapers#page3.tif

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☒ The attached application, or

☐ United States application or PCT international application number _____

filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 153988** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

Micron Ex. 1016, p. 83
Micron v. YMTC
IPR2025-00191

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Mei Lan Guo Date: 2018.9.5

Signature of Inventor:

Inventor: Yushi Hu Date: 2018.08.22

Signature of Inventor:

Inventor: Ji Xia Date: 2018/8/22

Signature of Inventor: Ji Xia

Inventor: Hongbin Zhu Date: 2018/8/29

Signature of Inventor:

Micron Ex. 1016, p. 84
Micron v. YMTC
IPR2025-00191

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	
Filing Date	
First Named Inventor	Mei Lan GUO
Title	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	10018-01-0015-US-DIV1

SIGNATURE of Applicant or Patent Practitioner

Signature	/Zhiwei Zou/	Date (Optional)	1/17/2020
Name	Zhiwei Zou	Registration Number	66,041
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 153988

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Simon	Date (Optional)	
Name	SIMON SHI-NING YANG		
Title	CEO		

NOTE: Signature – This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of One forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/745,342

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/745,342	01/17/2020	2812	1720	10018-01-0015-US-DIV1	20	3

CONFIRMATION NO. 2958

FILING RECEIPT

OC000000114637894

153988
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

Date Mailed: 02/13/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Mei Lan Guo, Wuhan, CHINA;
Yushi Hu, Wuhan, CHINA;
Ji Xia, Wuhan, CHINA;
Hongbin Zhu, Wuhan, CHINA;

Applicant(s)

YANGTZE MEMORY TECHNOLOGIES CO., LTD., Wuhan, CHINA;

Power of Attorney: The patent practitioners associated with Customer Number 153988

Domestic Priority data as claimed by applicant

This application is a DIV of 16/149,103 10/01/2018 PAT 10566336
which is a CON of PCT/CN2018/101482 08/21/2018

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Micron Ex. 1016, p. 88
Micron v. YMTC
IPR2025-00191

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/11/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/745,342**

Projected Publication Date: 05/21/2020

Non-Publication Request: No

Early Publication Request: No

Title

THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

Micron Ex. 1016, p. 89
Micron v. YMTC
IPR2025-00191

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

Micron Ex. 1016, p. 90
Micron v. YMTC
IPR2025-00191

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Micron Ex. 1016, p. 91
Micron v. YMTC
IPR2025-00191

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/745,342	01/17/2020	Mei Lan Guo	10018-01-0015-US-DIV1

CONFIRMATION NO. 2958

153988
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

PUBLICATION NOTICE

OC000000117168447

Title:THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

Publication No.US-2020-0161321-A1
Publication Date:05/21/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Micron Ex. 1016, p. 92
Micron v. YMTC
IPR2025-00191

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/745,342	01/17/2020	Mei Lan Guo	10018-01-0015-US-DIV1	2958

153988 7590 09/25/2020
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

EXAMINER
TRAN, DZUNG

ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
09/25/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 16/745,342	Applicant(s) Guo et al.	
	Examiner DZUNG T TRAN	Art Unit 2829	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 01/17/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☐ Claim(s) _____ is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☑ Claim(s) 1-20 are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Micron Ex. 1016, p. 94
Micron v. YMTC
IPR2025-00191

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

REQUIREMENT FOR UNITY OF INVENTION

1. As provided in 37 CFR 1.475(a), a national stage application shall relate to one invention only or to a group of inventions so linked as to form a single general inventive concept ("requirement of unity of invention"). Where a group of inventions is claimed in a national stage application, the requirement of unity of invention shall be fulfilled only when there is a technical relationship among those inventions involving one or more of the same or corresponding special technical features. The expression "special technical features" shall mean those technical features that define a contribution which each of the claimed inventions, considered as a whole, makes over the prior art.

The determination whether a group of inventions is so linked as to form a single general inventive concept shall be made without regard to whether the inventions are claimed in separate claims or as alternatives within a single claim. See 37 CFR 1.475(e).

WHEN CLAIMS ARE DIRECTED TO MULTIPLE CATEGORIES OF INVENTIONS

As provided in 37 CFR 1.475(b), a national stage application containing claims to different categories of invention will be considered to have unity of invention if the claims are drawn only to one of the following combinations of categories:

(1) A product and a process specially adapted for the manufacture of said product; or

(2) A product and process of use of said product; or

(3) A product, a process specially adapted for the manufacture of the said product, and a use of the said product; or

(4) A process and an apparatus or means specifically designed for carrying out the said process; or

(5) A product, a process specially adapted for the manufacture of the said product, and an apparatus or means specifically designed for carrying out the said process.

Otherwise, unity of invention might not be present. See 37 CFR 1.475(c).

2. Restriction is required under 35 U.S.C. 121 and 372.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

In accordance with 37 CFR 1.499, applicant is required, in reply to this action, to elect a single invention to which the claims must be restricted.

Group I: as shown in claims 1-14, comprising a three-dimensional (3D) device having a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack.

Group II: as shown in claims 15-20, comprising a three-dimensional (3D) device having a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.

Inventions Group I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)).

3. The groups of inventions listed above do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Group I-II lack unity of invention because the groups do not share the same or corresponding technical feature. The limitations disclosed in group II invention are not the same or corresponding special technical features in group I invention. For example, in claim 15 of the instance case, the limitation "a dummy channel structure filled with a dielectric layer" which corresponding the special technical features of Group II is not disclosed in Group I invention. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

4. Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

5. The election of an invention or species may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention or species.

6. Should applicant traverse on the ground that the inventions have unity of invention (37 CFR 1.475(a)), applicant must provide reasons in support thereof. Applicant may submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. Where such evidence or admission is provided by applicant, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DZUNG T TRAN whose telephone number is (571) 270-3911. The examiner can normally be reached on M-F 8 AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DZUNG TRAN/

Primary Examiner, Art Unit 2829

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/745,342	Guo et al.
	Examiner	**Art Unit**
	DZUNG T TRAN	2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/22/2020								
	1	÷								
	2	÷								
	3	÷								
	4	÷								
	5	÷								
	6	÷								
	7	÷								
	8	÷								
	9	÷								
	10	÷								
	11	÷								
	12	÷								
	13	÷								
	14	÷								
	15	÷								
	16	÷								
	17	÷								
	18	÷								
	19	÷								
	20	÷								

Micron Ex. 1016, p. 100
Micron v. YMTC
IPR2025-00191

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16745342
Filing Date	2020-01-17
First Named Inventor	Mei Lan GUO
Art Unit	2829
Examiner Name	TRAN, DZUNG
Attorney Docket Number	10018-01-0015-US-DIV1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20150206895	A1	2015-07-23	OH et al.	
	2	20150179660	A1	2015-06-25	Yada et al.	
	3	20130264631	A1	2013-10-10	Alsmeier et al.	
	4	20120280304	A1	2012-11-08	LEE et al.	
	5	20120119287	A1	2012-05-17	PARK et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16745342
	Filing Date	2020-01-17
	First Named Inventor	Mei Lan GUO
	Art Unit	2829
	Examiner Name	TRAN, DZUNG
	Attorney Docket Number	10018-01-0015-US-DIV1

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16745342
	Filing Date	2020-01-17
	First Named Inventor	Mei Lan GUO
	Art Unit	2829
	Examiner Name	TRAN, DZUNG
	Attorney Docket Number	10018-01-0015-US-DIV1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2020-09-25
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	40676210
Application Number:	16745342
International Application Number:	
Confirmation Number:	2958
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0015-US-DIV1
Receipt Date:	25-SEP-2020
Filing Date:	17-JAN-2020
Time Stamp:	17:15:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	10018-01-0015-US-DIV1_IDS2-SB08.pdf	612099 e4df9e02552b3c894b8bce9e1827fc00a49a5d23	no	4

Warnings:

Information:	
Total Files Size (in bytes):	612099

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant :	Mei Lan Guo	Art Unit :	2829
Serial No. :	16/745,342	Examiner :	TRAN, DZUNG
Filed :	Janurary 17, 2020	Conf. No. :	2958
Title :	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME		

U.S. Patent and Trademark Office
Customer Window, **Mail Stop Amendment**
Randolph Building
401 Dulany Street
Alexandria, VA 22314

REPLY TO RESTRICTION REQUIREMENT OF SEPTEMBER 25, 2020

The Office Action mailed September 25, 2020, was a Restriction Requirement requiring election between the following groups:

Group I: Claims 1-14 drawn, according to the Office Action, to a three-dimensional (3D) device having a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack; and

Group II: Claims 15-20 drawn, according to the Office Action, to a three-dimensional (3D) device having a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.

In response to the restriction requirement, Applicant respectfully elects Group I, claims 1-14, without traverse, and without prejudice to the presentation of the claims of Group II in later applications.

Conclusion

All the stated grounds of restriction have been properly accommodated. Applicant therefore respectfully requests that the Examiner consider and allow the elected claims. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2227.

Prompt and favorable consideration of this Response is respectfully requested.

Respectfully submitted,

BAYES PLLC

/Zhiwei Zou/___

Zhiwei Zou
Attorney for Applicant
Registration No. 66,041

Date: September 30, 2020

1765 Greensboro Station Place, Suite 900
McLean, VA 22102
(703) 995-9887

Electronic Acknowledgement Receipt

EFS ID:	40726851
Application Number:	16745342
International Application Number:	
Confirmation Number:	2958
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0015-US-DIV1
Receipt Date:	30-SEP-2020
Filing Date:	17-JAN-2020
Time Stamp:	18:40:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	10018-01-0015-US-DIV1_ResponseRR_09-25-20.pdf	24525 13cdbd4349d42601a379895db5066e42b6cd1d85	no	2

Warnings:

Information:	
Total Files Size (in bytes):	24525

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/745,342	01/17/2020	Mei Lan Guo	10018-01-0015-US-DIV1	2958

153988 7590 12/03/2020
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

EXAMINER
TRAN, DZUNG

ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
12/03/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 16/745,342	Applicant(s) Guo et al.	
	Examiner DZUNG T TRAN	Art Unit 2829	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 09/30/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) 15-20 is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-14 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☑ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Micron Ex. 1016, p. 112
Micron v. YMTC
IPR2025-00191

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Status of the Claims

1. Applicant's election, without traverse, of Group I, claims 1-14 in the reply filed on September 30th, 2020 is acknowledged. Non-elected invention of Group II, claims 15-20 have been withdrawn from consideration. Claims 1-20 are pending.

Action on merits of Group I, claims 1-14 as follows.

Priority

2. Receipt is acknowledged of certified copies of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statements (IDSs) submitted on January 17th, 2020 and September 25, 2020 have been considered by the examiner.

Drawings

4. The drawings filed on 01/17/2020 are acceptable.

Specification

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102/103

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

7. Claims 1-3, 11-12 are rejected under 35 U.S.C. 102(a)(1) as being clearly anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over Lee (US 2012/0280304, hereinafter as Lee '304).

Regarding Claim 1, Lee '304 teaches a three-dimensional (3D) memory device, comprising:

a substrate (Fig. 23, (100); [0066]);

a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs (Fig. 23, (140/110); [0076]-[0077]);

a channel structure (Fig. 23, (730); [0095]) extending vertically through the conductor/dielectric layer pairs in the memory stack; and

a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack, wherein the TAC comprises a conductor layer (Fig. 23, (170); [0087]) and a spacer (Fig. 23, (162); [0097]) in a plurality of shallow recesses abutting a sidewall of the TAC. Examiner considers the protrusion regions "162" is the spacer portion in a plurality of shallow recesses abutting the sidewall of the TAC.

Regarding Claim 11, Lee '304 teaches a three-dimensional (3D) memory device, comprising:

a substrate (Fig. 23, (100); [0066]);

a memory stack on the substrate comprising a plurality of conductor/dielectric layer pairs (Fig. 23, (140/110); [0076]-[0077]);

a channel structure (Fig. 23, (730); [0095]) extending vertically through the conductor/dielectric layer pairs in the memory stack; and

a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack, wherein the TAC comprises a conductor layer (Fig. 23, (170); [0087]) and a spacer (or a sidewall insulation layer, Fig. 23, (160); [0051]) over a sidewall of the TAC.

FIG. 23

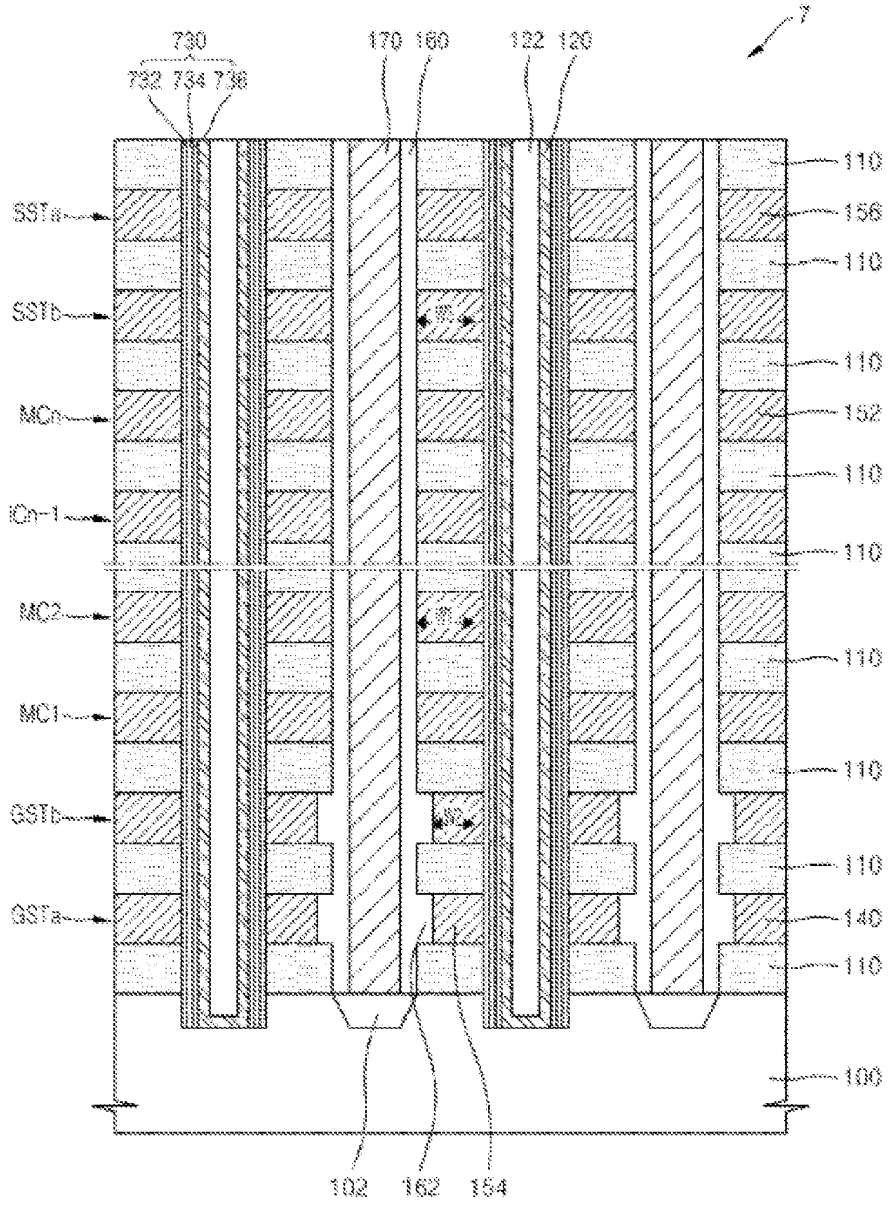


Fig. 23 (Lee '304)

Regarding Claim 2, Lee '304 teaches the spacer (Fig. 23, (160); [0095]) is further over the sidewall of the TAC.

Regarding Claim 3, Lee '304 teaches the TAC (170/160) is in an inner region of the memory stack (730) (see Fig. 23).

Regarding Claim 12, Lee '304 teaches the spacer (Fig. 23, (162); [0097]) is further in a plurality of shallow recesses abutting the sidewall of the TAC. Examiner considers the protrusion regions "162" is the spacer portion in a plurality of shallow recesses abutting the sidewall of the TAC.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 4-7, 13 and 14 are rejected under 35 U.S.C. 103 as being unpatentable over Lee '304 as applied to claim 1 above, and further in view of Nishikawa (US 2017/0125430, hereinafter as Nishi '430).

Regarding Claims 4 and 13, Lee '304 is shown to teach all the features of the claim with the exception of explicitly the features: "a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack".

However, Nishi '430 teaches a dummy channel structure (Fig. 5, (7P); [0080]) filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs (32/46) in

the memory stack. Examiner considers the dielectric support pillars (7P) is the dummy channel structure.

Thus, it would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Lee '304 by having a dummy channel structure for the purpose of providing structural support to the memory device structure (see para. [0095]) as suggested by Nishi '430.

Regarding Claim 5, Nishi '430 teaches the dielectric layer in the dummy channel structure and the spacer in the TAC comprise silicon oxide (see para. [0082]).

Regarding Claims 6 and 14, Nishi '430 teaches a peripheral device (Fig. 11, (400); [0029]) on the substrate (Fig. 11, (9); [0029]); and a peripheral contact (Fig. 11, (476); [0115]) outside of the memory stack and in contact with the peripheral device (405; [0133]).

Regarding Claim 7, Nishi '430 teaches a slit structure (Fig. 9, (179); [0083]) extending vertically through the conductor/dielectric layer pairs in the memory stack.

10. Claims 8-10 are rejected under 35 U.S.C. 103 as being unpatentable over Lee '304 as applied to claim 1 above, and further in view of Pachamuthu (US 2015/0236038, hereinafter as Pacha '038).

Regarding Claim 8, Nishi '430 teaches a lower memory deck on the substrate (see Fig. 1).

Thus, Lee '304 and Nishi are shown to teach all the features of the claim with the exception of explicitly the features: "an upper memory deck above the lower memory deck".

However, Pacha '038 teaches an upper memory deck (Fig. 15, (232/242); [0099]) above the lower memory deck (Fig. 15, (132/146); [0099]).

Thus, it would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Lee '304 and Nishi '430 by having an upper memory deck above the lower memory deck in order to form a vertical stack of multilevel memory arrays above a single substrate, with no intervening substrates (see para. [0001] and [0039]) as suggested by Pacha '038.

Regarding Claim 9, Nishi '430 teaches a lower channel structure (730) extending vertically through the lower memory deck (see Fig. 23).

Furthermore, Pacha '038 teaches an upper channel structure (Fig. 32, (260); [0141]) extending vertically through the upper memory deck; and an inter-deck plug (doped semiconductor regions 163; [0140]) disposed vertically between and in contact with the lower channel structure and the upper channel structure.

Regarding Claim 10, Nishi '430 teaches a staircase structure at one side of the memory stack (see Fig. 32); and a plurality of word line contacts (Fig. 32, (286); [0147]) each in contact with a respective one of the conductor layers (146; [0150]) of the conductor/dielectric layer pairs in the staircase structure.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to semiconductor devices:

Amono (US 2018/0331118 A1)

Lu et al. (US 2017/0062454 A1)

Toyama et al. (US 2017/0179152 A1)

Liu et al. (US 2016/0322381 A1)

Yada et al. (US 2015/0179660 A1)

12. For applicant's benefit portions of the cited reference(s) have been cited to aid in the review of the rejection(s). While every attempt has been made to be thorough and consistent within the rejection it is noted that the *PRIOR ART MUST BE CONSIDERED IN ITS ENTIRETY, INCLUDING DISCLOSURES THAT TEACH AWAY FROM THE CLAIMS.* See MPEP 2141.02 VI.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DZUNG T TRAN whose telephone number is (571) 270-3911. The examiner can normally be reached on M-F 8 AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DZUNG TRAN/
Primary Examiner, Art Unit 2829

Notice of References Cited	Application/Control No. 16/745,342	Applicant(s)/Patent Under Reexamination Guo et al.	
	Examiner DZUNG T TRAN	Art Unit 2829	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20150236038-A1	08-2015	PACHAMUTHU; Jayavel	H01L27/11524	257/326
*	B	US-20180331118-A1	11-2018	AMANO; Fumitaka	H01L21/76858	1/1
*	C	US-20170062454-A1	03-2017	LU; Zhenyu	H01L29/7926	1/1
*	D	US-20170179152-A1	06-2017	TOYAMA; Fumiaki	H01L27/11582	1/1
*	E	US-20160322381-A1	11-2016	Liu; Jin	H01L29/40114	1/1
*	F	US-20150179660-A1	06-2015	Yada; Shinsuke	H01L21/02164	257/321
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Micron Ex. 1016, p. 122
Micron v. YMTC
IPR2025-00191

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/745,342	Guo et al.
	Examiner	**Art Unit**
	DZUNG T TRAN	2829

CPC - Searched*		
Symbol	**Date**	**Examiner**

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**
H01L 27/11531; 27/11524; 27/11529; 27/11556; 27/1157; 27/11573; 21/76816; 23/5226; 23/5283	06/18/2020 (Updated on 11/28/2020)	DT

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
257	314	06/18/2020	DT

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Conducted inventor name searching	06/18/2020	DT
Text searching	06/18/2020	DT
Text searching	09/22/2020	DT
Text searching	11/28/2020	DT

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

Micron Ex. 1016, p. 123
Micron v. YMTC
IPR2025-00191

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/745,342	Guo et al.
	Examiner	**Art Unit**
	DZUNG T TRAN	2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/22/2020	11/30/2020							
	1	÷	✓							
	2	÷	✓							
	3	÷	✓							
	4	÷	✓							
	5	÷	✓							
	6	÷	✓							
	7	÷	✓							
	8	÷	✓							
	9	÷	✓							
	10	÷	✓							
	11	÷	✓							
	12	÷	✓							
	13	÷	✓							
	14	÷	✓							
	15	÷	N							
	16	÷	N							
	17	÷	N							
	18	÷	N							
	19	÷	N							
	20	÷	N							

Micron Ex. 1016, p. 124
Micron v. YMTC
IPR2025-00191

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20170125430	A1	2017-05-04	NISHIKAWA et al.	
	2	20140175532	A1	2014-06-26	Chen	
	3	20160099255	A1	2016-04-07	Lai	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	108377660	CN	A	2018-08-07	SANDISK TECHNOLOGIES LLC		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.T/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV1

	2	108140644	CN	A	2018-06-08	SANDISK TECHNOLOGIES LLC		
	3	106920794	CN	A	2017-07-04	YANGTZE MEMORY TECH CO LTD		
	4	106910746	CN	A	2017-06-30	YANGTZE MEMORY TECH CO LTD		
	5	106920796	CN	A	2017-07-04	YANGTZE MEMORY TECH CO LTD		
	6	106256005	CN	A	2016-12-21	SANDISK TECHNOLOGIES INC		
	7	107771356	CN	A	2018-03-06	SANDISK TECHNOLOGIES INC		

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Search Report issued in corresponding International Application No. PCT/CN2018/101482, mailed May 5, 2019, 5 pages	
	2	Written Opinion of the International Searching Authority issued in corresponding International Application No. PCT/CN2018/101482, mailed May 5, 2019, 4 pages	

If you wish to add additional non-patent literature document citation information please click the Add button Add

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.T/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV1

EXAMINER SIGNATURE			
Examiner Signature	/DZUNG TRAN/	Date Considered	09/22/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.T/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Mei Lan GUO
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	10018-01-0015-US-DIV1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

X A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2020-01-17
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.T/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.T/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2,319	((("LIU") near3 ("Jun"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/11/19 14:24
S2	4,485	(257/315).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 14:25
S3	4,485	(257/315).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 14:30
S4	4,483	S3 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 14:30
S5	4,240	S4 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 14:31
S6	2,125	S5 and (bit near line)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 14:31
S7	2,319	((("LIU") near3 ("Jun"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/11/19 14:45
S8	1,023	S7 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 14:45
S9	8	S8 and (memory near stack)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 14:46
S10	1	(12/262223).APP.	USPAT; USOCR	OR	OFF	2019/11/19 14:47
S11	56	("20070132049" | "20070229166" | "20080151611" | "20080165567" | "5559425" | "5680038" | "6128214" | "6493258" | "6504750" | "6724654" | "6870755" | "7433226").PN. OR ("7835173").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 14:47

S12	56	("20070132049" | "20070229166" | "20080151611" | "20080165567" | "5559425" | "5680038" | "6128214" | "6493258" | "6504750" | "6724654" | "6870755" | "7433226").PN. OR ("7835173").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 14:48
S13	4,043	H01L27/11556.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 15:07
S14	2,171	H01L27/11556.CPC.	US-PGPUB	OR	OFF	2019/11/19 15:07
S15	2,745	H01L27/11524.CPC.	US-PGPUB	OR	OFF	2019/11/19 15:30
S16	2,472	S15 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 15:31
S17	2,461	S16 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 15:31
S18	2,355	S17 and (bit line)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 15:31
S19	1,775	S18 and stacK$3	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 15:31
S20	917	H01L27/11529.CPC.	US-PGPUB	OR	OFF	2019/11/19 15:55
S21	1,694	H01L27/11529.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 15:55
S22	931	H01L27/11531.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 16:21
S23	1,396	H01L27/11531.CPC.	US-PGPUB; USPAT; USOCR; JPO; DERWENT	OR	OFF	2019/11/19 16:21
S24	1,396	H01L27/11531.CPC.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/11/19 16:21
S25	1,903	H01L27/11531.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2019/11/19 16:21

			JPO; DERWENT; IBM_TDB			
S26	1,759	H01L27/11548.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/11/19 16:22
S27	8,526	H01L27/1157.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/11/19 17:02
S28	2,355	H01L27/1157.CPC.	US-PGPUB	OR	OFF	2019/11/19 17:03
S29	1,788	S28 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 17:03
S30	2,355	H01L27/1157.CPC.	US-PGPUB	OR	OFF	2019/11/19 17:06
S31	1,741	H01L27/11573.CPC.	US-PGPUB	OR	OFF	2019/11/19 17:06
S32	1,105	H01L27/11575.CPC.	US-PGPUB	OR	OFF	2019/11/19 17:51
S33	1,971	H01L27/11575.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 17:51
S34	7,516	H01L27/11582.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 18:20
S35	4,196	H01L27/11582.CPC.	US-PGPUB	OR	OFF	2019/11/19 18:20
S36	3,296	S35 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 18:20
S37	3,260	S36 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 18:20
S38	2,337	S37 and (bit near line)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 18:20

S39	1,159	S38 and stack	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/19 18:21
S40	1,324	(257/314).CCLS.	US-PGPUB	OR	OFF	2019/11/20 06:10
S41	142	((("GUO") near3 ("Mei") near3 ("Lan")) OR (("HU") near3 ("Yushi")) OR (("XIA") near3 ("Ji")) OR (("ZHU") near3 ("Hongbin"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/11/20 06:10
S42	2,770	H01L21/76816.CPC.	US-PGPUB	OR	OFF	2019/11/20 06:19
S43	2,391	S42 and @pd<"20180821"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/20 06:19
S44	4,923	H01L21/76877.CPC.	US-PGPUB	OR	OFF	2019/11/20 07:00
S45	4,252	S44 and @pd<"20180821"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/20 07:00
S46	1,826	S45 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/20 07:00
S47	5,604	H01L23/5226.CPC.	US-PGPUB	OR	OFF	2019/11/20 07:49
S48	4,538	S47 and @pd<"20180821"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/20 07:49
S49	2,126	S48 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/11/20 07:49
S50	1,937	H01L23/5283.CPC.	US-PGPUB	OR	OFF	2019/11/20 07:49
S51	3	("20140175532" | "20160099255" | "20170125430").PN.	US-PGPUB; USPAT	OR	OFF	2019/11/20 08:10
S52	2,775	H01L27/11524.CPC.	US-PGPUB	OR	OFF	2019/12/18 10:42
S53	2,477	S52 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/12/18 10:42
S54	2,464	S53 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/12/18 10:42
S55	2,358	S54 and (bit line)	US-PGPUB; USPAT; USOCR	OR	OFF	2019/12/18 11:00

S56	925	H01L27/11529.CPC.	US-PGPUB	OR	OFF	2019/12/18 11:01
S57	1,715	H01L27/11529.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/12/18 11:02
S58	4,129	H01L27/11556.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/12/18 12:06
S59	2,225	H01L27/11556.CPC.	US-PGPUB	OR	OFF	2019/12/18 12:06
S60	2,407	H01L27/1157.CPC.	US-PGPUB	OR	OFF	2019/12/18 12:06
S61	1,800	S60 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/12/18 12:07
S62	6	("20140175532" | "20160099255" | "20170125430").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/12/18 15:05
S64	1	("9449987").PN.	USPAT; USOCR	OR	OFF	2019/12/18 17:54
S65	0	(14/995017).APP.	US-PGPUB; USOCR	OR	OFF	2019/12/18 17:54
S66	2	"14832579"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/12/18 17:55
S67	1	("20170052258").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/12/18 17:57
S68	0	(14/995017).APP.	US-PGPUB; USOCR	OR	OFF	2019/12/18 18:12
S69	72	("20070210338" | "20070252201" | "20090230449" | "20090242967" | "20100044778" | "20100112769" | "20100120214" | "20100155810" | "20100155818" | "20100181610" | "20100207195" | "20100320528" | "20110076819" | "20110133606" | "20110266606" | "20120001247" | "20120001249" | "20120001250" | "20120012920" | "20120119287" | "20130264631" | "20140061849" | "20140199815" | "20150076584" | "20150179660" | "5915167" | "7005350" | "7023739" | "7177191" | "7221588" | "7233522" |	US-PGPUB; USPAT; USOCR	OR	OFF	2019/12/18 18:13

		"7514321" | "7575973" | "7696559" | "7745265" | "7808038" | "7848145" | "7851851" | "8008710" | "8053829" | "8187936" | "8394716" | "9023719" | "9305934").PN. OR ("9449987").URPN.				
S70	1	("9449987").PN.	USPAT; USOCR	OR	OFF	2019/12/18 18:13
S71	179	((("GUO") near3 ("Mei") near3 ("Lan")) OR (("HU") near3 ("Yushi")) OR (("XIA") near3 ("Ji")) OR (("ZHU") near3 ("Hongbin"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/06/18 08:41
S72	1,326	(257/314).CCLS.	US-PGPUB	OR	OFF	2020/06/18 08:43
S73	2,120	H01L27/11531.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/06/18 08:47
S74	3,081	H01L21/76816.CPC.	US-PGPUB	OR	OFF	2020/06/18 09:16
S75	2,449	S74 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 09:16
S76	753,089	"55" and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 09:16
S77	1,242	S75 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 09:16
S78	1,033	S75 and (bit data)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 09:18
S79	1,421	S77 S78	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 09:18
S80	5,390	H01L21/76877.CPC.	US-PGPUB	OR	OFF	2020/06/18 09:58
S81	4,301	S80 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 09:59

S82	1,852	S81 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 09:59
S83	6,379	H01L23/5226.CPC.	US-PGPUB	OR	OFF	2020/06/18 09:59
S84	4,603	S83 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 10:00
S85	2,159	S84 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 10:00
S86	2,210	H01L23/5283.CPC.	US-PGPUB	OR	OFF	2020/06/18 10:51
S87	2,984	H01L27/11524.CPC.	US-PGPUB	OR	OFF	2020/06/18 10:52
S88	2,481	S87 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 10:53
S89	2,468	S88 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 10:53
S90	2,270	S89 and (bit data)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 10:53
S91	990	H01L27/11529.CPC.	US-PGPUB	OR	OFF	2020/06/18 12:01
S92	1,832	H01L27/11529.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 12:01
S93	4,636	H01L27/11556.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 12:01
S94	2,504	H01L27/11556.CPC.	US-PGPUB	OR	OFF	2020/06/18 12:02
S95	1,755	S94 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 12:02
S96	0	H01L27/11557.CPC.	US-PGPUB	OR	OFF	2020/06/18 12:53
S97	2,710	H01L27/1157.CPC.	US-PGPUB	OR	OFF	2020/06/18 12:53
S98	1,803	S97 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/06/18 12:53

S99	2,006	H01L27/11573.CPC.	US-PGPUB	OR	OFF	2020/06/18 12:54
S100	5,136	H01L27/11582.CPC.	US-PGPUB	OR	OFF	2020/09/22 06:28
S101	3,325	S100 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/22 06:28
S102	3,285	S101 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/22 06:28
S103	3,067	S102 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/22 06:29
S104	2,215	S103 and (bit near line)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/09/22 06:29
S105	5	("20120119287" | "20120280304" | "20130264631" | "20150179660" | "20150206895").PN.	US-PGPUB; USPAT	OR	OFF	2020/11/28 11:07
S106	2,576	((("LIU") near3 ("Jun"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/11/28 11:08
S107	3,495	(257/314).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:08
S108	3,490	S107 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:09
S109	3,341	S108 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:09
S110	2,939	S109 and (bit line)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:09
S111	1,833,537	6and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:09
S112	1,965	S110 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:09
S113	2,193	H01L27/11531.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2020/11/28 12:06

			DERWENT; IBM_TDB			
S114	3,229	H01L21/76816.CPC.	US-PGPUB	OR	OFF	2020/11/28 12:09
S115	2,457	S114 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 12:09
S116	1,254	S115 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 12:09
S117	2,039	S115 and (bit line)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 12:09
S118	2,197	S116 S117	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 12:09
S119	5,627	H01L21/76877.CPC.	US-PGPUB	OR	OFF	2020/11/28 13:07
S120	4,301	S119 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 13:07
S121	1,929	S120 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 13:07
S122	8	("20130264631" | "20160099255" | "20120280304" | "20150206895" | "20140175532" | "20150179660" | "20170125430" | "20120119287").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 13:30
S123	1	("20200161321").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 13:31
S124	3	S122 and dummy	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 14:19
S125	6,821	H01L23/5226.CPC.	US-PGPUB	OR	OFF	2020/11/28 14:33
S126	4,604	S125 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 14:33
S127	2,431	S126 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 14:33
S128	1,975	S127 and (bit line)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 14:33

S129	1	(14/133979).APP.	USPAT; USOCR	OR	OFF	2020/11/28 16:37
S130	72	("20070210338" | "20070252201" | "20090230449" | "20090230454" | "20090242967" | "20100044778" | "20100112769" | "20100120214" | "20100155810" | "20100155818" | "20100181610" | "20100207195" | "20100320528" | "20110076819" | "20110133606" | "20110266606" | "20110303970" | "20120001247" | "20120001249" | "20120001250" | "20120012920" | "20120032245" | "20120208347" | "20130089974" | "20130264631" | "7005350" | "7023739" | "7177191" | "7221588" | "7233522" | "7514321" | "7575973" | "7696559" | "7745265" | "7808038" | "7848145" | "7851851" | "8008710" | "8053829" | "8187936" | "8394716").PN. OR ("9449983").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 16:37
S131	85	("10008570" | "10121794" | "10553599" | "10559588" | "20030047755" | "20030122204" | "20030155582" | "20030219933" | "20040041192" | "20040063286" | "20040125629" | "20040251488" | "20050062098" | "20080012065" | "20090321855" | "20100109071" | "20110045657" | "20110287612" | "20120023894" | "20120068247" | "20120276702" | "20130009236" | "20130089974" | "20130134492" | "20140225160" | "20140225181" | "20140264525" | "20150129954" | "20150179660" | "20160049421" | "20160099250" | "20160118391" | "20160141294" | "20160181264" | "20160260733" | "20160358933" | "20170062454" | "20170110464" | "20170110470" | "20170162591" | "20170229472" | "20170338243" | "20170365613" | "20180122906" | "20190252405" | "20190326313" | "5915167" | "6274490" | "6372569" | "6677213" | "6777274" | "6833306" | "6881994" | "7005350" | "7012299" | "7202119" | "8187936" | "8829593" | "8884357" | "8946023" | "9023719" | "9136130" | "9177966" | "9230980"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 16:47

		| "9230987" | "9305932" | "9331093" | "9356031" | "9425299" | "9449980" | "9449983" | "9460931" | "9478495" | "9502471" | "9570463" | "9576975" | "9627395" | "9627403" | "9691884" | "9698153" | "9728551" | "9780108" | "9853043" | "9876025" | "9941295").PN. OR ("10797060").URPN.				
S132	72	("10115735" | "10355017" | "20060157797" | "20070155074" | "20070210338" | "20070252201" | "20080096328" | "20080116583" | "20090230449" | "20090242967" | "20100044778" | "20100090286" | "20100112769" | "20100120214" | "20100155810" | "20100155818" | "20100181610" | "20100207195" | "20100320528" | "20110076819" | "20110133606" | "20110233688" | "20110266606" | "20120001247" | "20120001249" | "20120001250" | "20120012920" | "20120119287" | "20120168877" | "20120261756" | "20120280290" | "20130140669" | "20130161746" | "20130181264" | "20130217190" | "20130264631" | "20130320417" | "20140117421" | "20140154846" | "20150008520" | "20150206945" | "20150214058" | "20150364490" | "20160163702" | "20160260712" | "20160351709" | "20180331118" | "5915167" | "6319782" | "6323525" | "7005350" | "7023739" | "7177191" | "7221588" | "7233522" | "7514321" | "7575973" | "7696559" | "7745265" | "7808038" | "7848145" | "7851851" | "8008710" | "8053829" | "8187936" | "8394716" | "9023719" | "9305934" | "9449983" | "9460931" | "9601503" | "9859422").PN. OR ("10770459").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 16:47
S133	0	(15/873101).APP.	US-PGPUB; USOCR	OR	OFF	2020/11/28 16:55
S134	10	("6169019" | "20170133398" | "5945350" | "20160351709" | "20030190497" | "5576579" | "5942799" | "6229211" |	US-PGPUB; USOCR	OR	OFF	2020/11/28 16:57

		"20180040476" | "5847463" | "6268299" | "20180245215" | "20060084247" | "5874353" | "20150138862" | "20030025206" | "20020140103" | "20030194859").PN.				
S135	1	("20180331118").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 16:59
S136	1	(15/080269).APP.	US-PGPUB; USOCR	OR	OFF	2020/11/28 17:01
S137	1	("20160204117").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 17:02
S138	1	(14/862916).APP.	US-PGPUB; USOCR	OR	OFF	2020/11/28 17:03
S139	1	("20160322381").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 17:03
S140	1	(14/611785).APP.	US-PGPUB; USOCR	OR	OFF	2020/11/28 17:04
S141	1	("20150236038").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 17:04

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S63	1	(form$3 near2 spacer near3 sidewall near3 first near open$3) and (form$3 near3 array ear contact near2 extend$3 near vertically tnear3 dielectric near stack near3 conductor near layer near4 spacer near3 first near open$3) and (after near form$3 TAC near2 form$3 near2 slit near extend$3 near vertically near3 dielectric near stack).clm.	USPAT	OR	OFF	2019/12/18 15:52

11/30/2020 6:41:07 AM
H:\East search\16_745342_memory string.wsp

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16745342
Filing Date	2020-01-17
First Named Inventor	Mei Lan GUO
Art Unit	2829
Examiner Name	TRAN, DZUNG
Attorney Docket Number	10018-01-0015-US-DIV1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20150206895	A1	2015-07-23	OH et al.	
	2	20150179660	A1	2015-06-25	Yada et al.	
	3	20130264631	A1	2013-10-10	Alsmeier et al.	
	4	20120280304	A1	2012-11-08	LEE et al.	
	5	20120119287	A1	2012-05-17	PARK et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.T/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16745342
	Filing Date	2020-01-17
	First Named Inventor	Mei Lan GUO
	Art Unit	2829
	Examiner Name	TRAN, DZUNG
	Attorney Docket Number	10018-01-0015-US-DIV1

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/DZUNG TRAN/	Date Considered	11/28/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.T/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16745342
	Filing Date	2020-01-17
	First Named Inventor	Mei Lan GUO
	Art Unit	2829
	Examiner Name	TRAN, DZUNG
	Attorney Docket Number	10018-01-0015-US-DIV1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

X A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2020-09-25
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.T/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.T/

UNITED STATES PATENT AND TRADEMARK OFFICE

USPTO Automated Interview Request (AIR)

Jan 18 2021

This paper requesting to schedule and/or conduct an interview is appropriate because:

This submission is requested to be accepted as an authorization for this interview to communicate via the internet. Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned concerning scheduling of the interview via video conference, instant messaging, or electronic mail, and to conduct the interview in accordance with office practice including video conferencing.

Name(s):
Zhiwei Zou

S-signature:
/Zhiwei Zou/

Registration Number:
66041

U.S. Application Number:
16745342

Confirmation Number:
2958

E-mail Address:
wayne.zou@bayes.law

Phone Number:
+1 5139676043

Proposed Time of Interview:
2-1-2021 1:30 PM ET

Alternative Proposed Time(s) of Interview:
2-2-2021 1:30 PM ET

Alternative Proposed Time(s) of Interview:
1-29-2021 1:30 PM ET

Prefered Interview Type:
Telephonic

I am the applicant or applicant's representative for this application.

Topic for Discussion:
Proposed amendments

uspto UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/745,342	01/17/2020	Mei Lan Guo	10018-01-0015-US-DIV1	2958

153988 7590 02/03/2021
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

EXAMINER
TRAN, DZUNG

ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
02/03/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

PTOL-90A (Rev. 04/07)

Applicant-Initiated Interview Summary	**Application No.** 16/745,342	**Applicant(s)** Guo et al.		
	Examiner DZUNG T TRAN	**Art Unit** 2829	**AIA (First Inventor to File) Status** Yes	**Page** 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
DZUNG T TRAN	Primary Examiner	Telephonic
WAYNE ZOU	Attorney	

Date of Interview: 29 January 2021

Issues Discussed:

35 U.S.C. 103

On January 29th, 2021, the Applicant's representative (Dr. Wayne Zou) participated in a telephonic interview with Examiner Dzung Tran. Claims 1 and 11 were discussed with respect to the 102/103 rejection. The applicant's representative proposed to amend independent claims 1 and 11 to overcome the 102/103 rejection. Examiner agrees that the proposed amendment overcome the current art (US 2012/0280304). Examiner will do further search when the amended claims are filed. No agreement as to allowability was reached during the interview.

/DZUNG TRAN/ Primary Examiner, Art Unit 2829	

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Micron Ex. 1016, p. 148
Micron v. YMTC
IPR2025-00191

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Mei Lan Guo *et al.*	Confirmation No.: 2958
Applicant: YANGTZE MEMORY TECHNOLOGIES CO. LTD.	Art Unit: 2829
Application No.: 16/745,342	Examiner: Dzung Tran
Filing Date: January 17, 2020	Atty. Docket: 10018-01-0015-US-DIV1

Title: **THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME**

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated December 3, 2020, Applicant submits the following Amendment and Remarks.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks and Arguments begin on page 6 of this paper.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2227.

Electronic Acknowledgement Receipt

EFS ID:	42035296
Application Number:	16745342
International Application Number:	
Confirmation Number:	2958
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0015-US-DIV1
Receipt Date:	26-FEB-2021
Filing Date:	17-JAN-2020
Time Stamp:	17:23:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		10018-01-0015-US-DIV1_AmendmentandReplyUnder.pdf	876200 6780918442325b557118690a15574212861e35b0	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	6	10
	Claims	2	5
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1

Warnings:	
Information:	
Total Files Size (in bytes):	876200

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendments, claims 1-11, 13, 14, and 21-27 are pending in the application, with claims 1, 11, and 21 being independent claims. Claims 1, 4, 7, 10, 11, and 13 are hereby amended. Claims 12 and 15-20 are hereby canceled without prejudice to or disclaimer of the subject matter therein. New claims 21-27 are hereby added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Throughout the arguments, Applicant reminds the Examiner that the claims are given their broadest reasonable meaning in view of the specification, and any paraphrasing of the claim features is not to be interpreted as reading any features into, or characterizing of, the claims.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Examiner Interview

Applicant's representative, Zhiwei Zou (Reg. No. 66,041), thanks Examiner Tran for the courtesy of a telephone interview with him on January 29, 2021. During the interview, the parties discussed the rejections under 35 U.S.C. §§ 102 and 103 and the proposed amendments to independent claims. Examiner Tran agreed that the proposed amendments, as reflected and further developed in this Amendment and Reply, appear to overcome the rejections under 35 U.S.C. §§ 102 and 103.

Rejections under 35 U.S.C. §§ 102 and 103

Claims 1-3, 11, and 12 were rejected under 35 U.S.C. § 102(a)(1) as being allegedly anticipated by or, in the alternative, under 35 U.S.C. § 103 as being allegedly unpatentable over U.S. Patent Application Publication No. 2012/0280304, in the name of Lee (hereinafter "Lee"). Claims 4-7, 13, and 14 were rejected under 35 U.S.C. § 103 as being allegedly unpatentable over Lee in view of U.S. Patent Application Publication No. 2017/0125430 in the name of Nishikawa (hereinafter "Nishikawa"). Claims 8-10 were rejected under 35 U.S.C. § 103 as being allegedly unpatentable over Lee in view of U.S. Patent Application Publication No. 2015/0236038 in the name of Pachamuthu (hereinafter "Pachamuthu"). Applicant respectfully transverse the rejections.

Micron Ex. 1016, p. 152
Micron v. YMTC
IPR2025-00191

Claims 1-10

Without acquiescing to propriety of the rejection and to expedite the prosecution, Applicant has amended independent claim 1 to clarify its distinguishing features. For example, independent claim 1 now recites, among other things, "**each of** the plurality of conductive layers having **a respective** shallow recess."[1] Support may be found, among other places, at paragraphs [0066] and [0067] of the specification and FIGs. 3D and 3E of the present application.

As discussed with the Examiner during the January 29, 2021 telephone interview, Lee fails to teach or suggest the above-noted distinguishing features. As shown in FIG. 14 of Lee reproduced below for ease of reference, only some of the interlayer conductive layers 140 (e.g., the second conductive layers 144) have the recess portions 143, while other interlayer conductive layers 140 (e.g., the first conductive layer 142) do not have the recess portions 143. In fact, Lee explicitly discloses that "**the interlayer conductive layers 140 may include**, for example, **a first conductive layer 142 that does <u>not</u> have the recess protion143**, and a second interlayer conductive layer 144 having the recess portion 143." (Lee, at [0084]). As a result, Lee fails to teach or suggests that each of the interlayer conductive layers 140 has a respective recess portion 143, as required by amended claim 1.

Other cited references, either alone or in any combination, also fail to teach or suggest the above-noted distinguishing features, and the Office Action points to no such alleged teachings. As such, other cited references fail to cure the deficiencies of Lee.

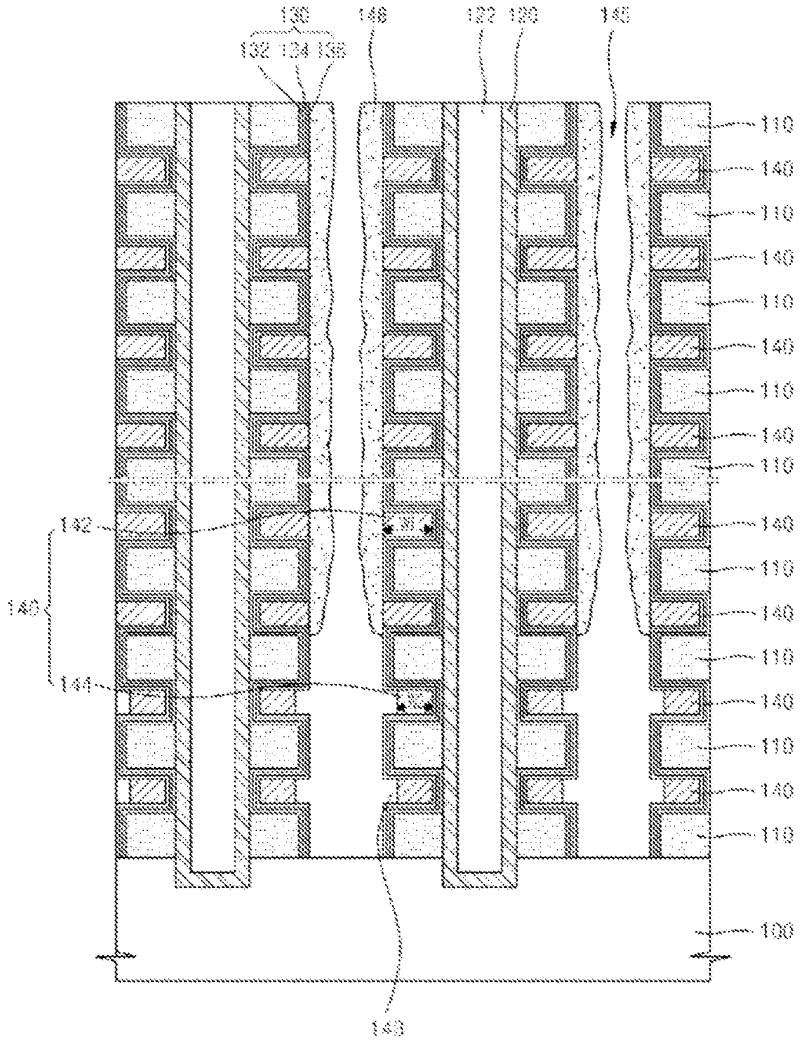
At least based on the above arguments, Applicant respectfully submits that independent claim 1 is patentable over the cited references. Dependent claims 2-10 are patentable over the cited references because they recite all of the features of claim 1 from which they depend, as well as for their additional distinguishing features.

---

[1] All emphasis added unless otherwise noted.

Micron Ex. 1016, p. 153
Micron v. YMTC
IPR2025-00191

FIG. 14



Claims 11, 13, and 14

Without acquiescing to propriety of the rejection and to expedite the prosecution, Applicant has amended independent claim 11 to clarify its distinguishing features. For example, independent claim 11 now recites, among other things, "**none of** the plurality of conductive layers having a shallow recess." Support may be found, among other places, in FIGs. 3B and 3C of the present application.

Micron Ex. 1016, p. 154
Micron v. YMTC
IPR2025-00191

As discussed with the Examiner during the January 29, 2021 telephone interview, Lee fails to teach or suggest the above-noted distinguishing features. As shown in FIG. 14 of Lee reproduced above, some of the interlayer conductive layers 140 (e.g., the second conductive layers 144) have the recess portions 143. (Lee, at [0084]). Thus, Lee fails to teach or suggests "none of the plurality of conductive layers having a shallow recess," as recited in amended claim 11.

Other cited references, either alone or in any combination, also fail to teach or suggest the above-noted distinguishing features, and the Office Action points to no such alleged teachings. As such, other cited references fail to cure the deficiencies of Lee.

At least based on the above arguments, Applicant respectfully submits that independent claim 11 is patentable over the cited references. Dependent claims 13 and 14 are patentable over the cited references because they recite all of the features of claim 11 from which they depend, as well as for their additional distinguishing features.

Accordingly, Applicant respectfully requests that the rejections of claims 1-11, 13, and 14 under 35 U.S.C. §§ 102 and 103 be reconsidered and withdrawn.

New Claims

New claims 21-27 is hereby added. Support for new claims 21-27 can be found throughout the originally filed specification, claims, and figures.

Dependent claims 21 and 22 should be found allowable over the cited references because they recite all of the features of claim 1 or 11 from which they depend, as well as for their additional distinguishing features.

Independent claim 23 recites, among other things, **both** a "source contact" and a "TAC" each extending vertically through the memory stack. Regardless of whether the common source line 170 of Lee is interpreted as the claimed source contact **or** the TAC, Lee fails to disclose **both** the source contact and TAC, as recited in claim 23. Other cited references also fail to cure the deficiencies of Lee. Thus, claim 23 is patentable over the cited references.

Dependent claims 24-27 should be found allowable over the cited references because they recite all of the features of claim 23 from which they depend, as well as for their additional distinguishing features.

Micron Ex. 1016, p. 155
Micron v. YMTC
IPR2025-00191

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider the presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

BAYES PLLC

/Zhiwei Zou/

Zhiwei Zou
Attorney for Applicant
Registration No. 66,041

Date: February 26, 2021

1765 Greensboro Station Place, Suite 900
McLean, VA 22102
(703) 995-9887

Micron Ex. 1016, p. 156
Micron v. YMTC
IPR2025-00191

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack on the substrate comprising interleaved a plurality of conductive layers and dielectric layers, each of the plurality of conductive layers having a respective shallow recess ~~a plurality of conductor/dielectric layer pairs~~;

a channel structure extending vertically through ~~the conductor/dielectric layer pairs in~~ the memory stack; and

a through array contact (TAC) extending vertically through ~~the conductor/dielectric layer pairs in~~ the memory stack,

wherein the TAC comprises a conductor layer and a spacer in the [[a]] plurality of shallow recesses abutting a sidewall of the TAC.

2. (Original) The 3D memory device of claim 1, wherein the spacer is further over the sidewall of the TAC.

3. (Original) The 3D memory device of claim 1, wherein the TAC is in an inner region of the memory stack.

4. (Currently Amended) The 3D memory device of claim 1, further comprising a dummy channel structure filled with a dielectric layer and extending vertically through ~~the conductor/dielectric layer pairs in~~ the memory stack.

5. (Original) The 3D memory device of claim 4, wherein the dielectric layer in the dummy channel structure and the spacer in the TAC comprise silicon oxide.

6. (Original) The 3D memory device of claim 1, further comprising:

Micron Ex. 1016, p. 157
Micron v. YMTC
IPR2025-00191

a peripheral device on the substrate; and

a peripheral contact outside of the memory stack and in contact with the peripheral device.

7. (Currently Amended) The 3D memory device of claim 1, further comprising a slit structure extending vertically through ~~the conductor/dielectric layer pairs in~~ the memory stack.

8. (Original) The 3D memory device of claim 1, wherein the memory stack comprises:

a lower memory deck on the substrate; and

an upper memory deck above the lower memory deck.

9. (Original) The 3D memory device of claim 8, wherein the channel structure comprises:

a lower channel structure extending vertically through the lower memory deck;

an upper channel structure extending vertically through the upper memory deck; and

an inter-deck plug disposed vertically between and in contact with the lower channel structure and the upper channel structure.

10. (Currently Amended) The 3D memory device of claim 1, further comprising:

a staircase structure at one side of the memory stack; and

a plurality of word line contacts each in contact with a respective one of the ~~conductor~~ plurality of conductive layers ~~of the conductor/dielectric layer pairs~~ in the staircase structure.

11. (Currently Amended) A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack on the substrate comprising interleaved a plurality of conductive layers and dielectric layers, none of the plurality of conductive layers having a shallow recess ~~a plurality of conductor/dielectric layer pairs~~;

a channel structure extending vertically through ~~the conductor/dielectric layer pairs in~~ the memory stack; and

Micron Ex. 1016, p. 158
Micron v. YMTC
IPR2025-00191

a through array contact (TAC) extending vertically through ~~the conductor/dielectric layer pairs in~~ the memory stack,

wherein the TAC comprises a conductor layer and a spacer over a sidewall of the TAC.

12. (Canceled)

13. (Currently Amended) The 3D memory device of claim 11, further comprising a dummy channel structure filled with a dielectric layer and extending vertically through ~~the conductor/dielectric layer pairs in~~ the memory stack.

14. (Original) The 3D memory device of claim 11, further comprising:

a peripheral device on the substrate; and

a peripheral contact outside of the memory stack and in contact with the peripheral device.

15-20. (Canceled)

21. (New) The 3D memory device of claim 1, wherein the TAC has a circular shape in a plan view.

22. (New) The 3D memory device of claim 11, wherein the TAC has a circular shape in a plan view.

23. (New) A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack on the substrate comprising interleaved a plurality of conductive layers and dielectric layers;

a channel structure extending vertically through the memory stack;

a source contact extending vertically through the memory stack; and

a through array contact (TAC) extending vertically through the memory stack,

Micron Ex. 1016, p. 159
Micron v. YMTC
IPR2025-00191

wherein the TAC comprises a conductor layer and a spacer in a plurality of shallow recesses abutting a sidewall of the TAC.

24. (New) The 3D memory device of claim 23, wherein the TAC has a circular shape in a plan view.

25. (New) The 3D memory device of claim 23, further comprising a dummy channel structure filled with a dielectric layer and extending vertically through the memory stack.

26. (New) The 3D memory device of claim 25, wherein the dielectric layer in the dummy channel structure and the spacer in the TAC comprise silicon oxide.

27. (New) The 3D memory device of claim 23, further comprising:

a peripheral device on the substrate; and

a peripheral contact outside of the memory stack and in contact with the peripheral device.

Micron Ex. 1016, p. 160
Micron v. YMTC
IPR2025-00191

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

153988 7590 03/10/2021
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

EXAMINER
TRAN, DZUNG

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/10/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/745,342	01/17/2020	Mei Lan Guo	10018-01-0015-US-DIV1	2958

TITLE OF INVENTION: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/10/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

Micron Ex. 1016, p. 161
Micron v. YMTC
IPR2025-00191

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

153988 7590 03/10/2021
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/745,342	01/17/2020	Mei Lan Guo	10018-01-0015-US-DIV1	2958

TITLE OF INVENTION: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/10/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, DZUNG	2829	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Micron Ex. 1016, p. 162
Micron v. YMTC
IPR2025-00191

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/745,342	01/17/2020	Mei Lan Guo	10018-01-0015-US-DIV1	2958

153988 7590 03/10/2021
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

EXAMINER
TRAN, DZUNG

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/10/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Micron Ex. 1016, p. 163
Micron v. YMTC
IPR2025-00191

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/745,342	Applicant(s) Guo et al.	
	Examiner DZUNG T TRAN	Art Unit 2829	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 02/26/2021.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-11,13-14 and 21-27 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☑ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/DZUNG TRAN/
Primary Examiner, Art Unit 2829

Micron Ex. 1016, p. 165
Micron v. YMTC
IPR2025-00191

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Response to Amendment

1. This office action is in response to Amendment filed on 02/26/2021.

Claims 1, 4, 7, 10-11 and 13 have been amended.

Claims 12 and 15-20 have been cancelled.

New Claims 21-27 have been added.

Response to Arguments/Reason

2. Applicant's arguments, with regards to claims 1-11, 13-14 and new claims 21-27, filed on 02/26/2021 have been fully considered and they are persuasive. Particularly, on pages 6-9 of the Applicant's Response, applicants argued that Lee '034 and Nishi '430 do not disclose the limitations of independent claim including: "a memory stack on the substrate comprising interleaved a plurality of conductive layers and dielectric layers, each of the plurality of conductive layers having a respective shallow recess; a channel structure extending vertically through the memory stack". The Examiner finds the arguments are persuasive. Therefore, the Examiner made decision to allow these limitations over the prior art of record.

Allowable Subject Matter

3. Claims 1-11, 13-14 and 21-27 are allowed.

4. The following is an examiner's statement of reasons for allowance: the whole application meets all formal and substantive requirements and the language of the claims is enabled by, and finds adequate descriptive support in, the application disclosure as originally filed. Concerning 35 U.S.C. § 102 and § 103 requirements, the application meets all requirements.

5. Regarding claims 1, 11 and 23, the known prior art does not teach the claim as a whole. In particular, the prior art does not disclose or fairly suggest the limitation: "a memory stack on the substrate comprising interleaved a plurality of conductive layers and dielectric layers, each of the plurality of conductive layers having a respective shallow recess; a channel structure extending vertically through the memory stack" in combination with the remaining limitations called for in claim 1.

6. None of the prior art on record contains such a limitation, nor given the prior art on record is it obvious to one of ordinary skill in the art to add said limitations as called for in claims 1, 11 and 23. Therefore, claims 1, 11 and 23 are allowed as it is not anticipated by or obvious over the teachings of the prior art on record. Furthermore, claims 2-10, 13-14, 21-22 and 24-27 are also allowed as they depend from an allowed base claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DZUNG T TRAN whose telephone number is (571) 270-3911. The examiner can normally be reached on M-F 8 AM-5PM.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DZUNG TRAN/
Primary Examiner, Art Unit 2829

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/745,342	Guo et al.
	Examiner	**Art Unit**
	DZUNG T TRAN	2829

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L 27/11531; 27/11524; 27/11529; 27/11556; 27/1157; 27/11573; 27/11582; 21/76816; 76877; 23/5226; 23/5283;	03/04/2021	DT

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
257	314	06/18/2020 (Updated on 03/04/2021)	DT

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Conducted inventor name searching	06/18/2020 (Updated on 03/04/2021)	DT
Text searching	06/18/2020	DT
Text searching	09/22/2020	DT
Text searching	11/28/2020	DT
Text searching	03/04/2021	DT

Micron Ex. 1016, p. 169
Micron v. YMTC
IPR2025-00191

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/745,342	Guo et al.
	Examiner	**Art Unit**
	DZUNG T TRAN	2829

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
	Conducted interference key words searching (see East search print out)	03/04/2021	DT

Micron Ex. 1016, p. 170
Micron v. YMTC
IPR2025-00191

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/745,342	Guo et al.
	Examiner	**Art Unit**
	DZUNG T TRAN	2829

CPC

Symbol					Type	Version
H01L	/	27	/	11531	F	2013-01-01
H01L	/	21	/	76816	I	2013-01-01
H01L	/	21	/	76877	I	2013-01-01
H01L	/	23	/	5226	I	2013-01-01
H01L	/	23	/	5283	I	2013-01-01
H01L	/	27	/	11524	I	2013-01-01
H01L	/	27	/	11529	I	2013-01-01
H01L	/	27	/	11556	I	2013-01-01
H01L	/	27	/	1157	I	2013-01-01
H01L	/	27	/	11573	I	2013-01-01
H01L	/	27	/	11582	I	2013-01-01

CPC Combination Sets

Symbol					Type	Set	Ranking	Version
	/		/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/DZUNG TRAN/ Primary Examiner, Art Unit 2829 (Primary Examiner)	04 March 2021 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3D

U.S. Patent and Trademark Office

Part of Paper No.: 20210304

Micron Ex. 1016, p. 171
Micron v. YMTC
IPR2025-00191

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/745,342	Guo et al.
	Examiner	**Art Unit**
	DZUNG T TRAN	2829

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L	/	27	/	11531

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
257	314

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/DZUNG TRAN/ Primary Examiner, Art Unit 2829 (Primary Examiner)	04 March 2021 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3D

U.S. Patent and Trademark Office

Part of Paper No.: 20210304

Micron Ex. 1016, p. 172
Micron v. YMTC
IPR2025-00191

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/745,342	Guo et al.
	Examiner	**Art Unit**
	DZUNG T TRAN	2829

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10		19										
2	2	11	11		20										
3	3		12	14	21										
4	4	12	13	15	22										
5	5	13	14	16	23										
6	6		15	17	24										
7	7		16	18	25										
8	8		17	19	26										
9	9		18	20	27										

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/DZUNG TRAN/ Primary Examiner, Art Unit 2829 (Primary Examiner)	04 March 2021 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3D

U.S. Patent and Trademark Office Part of Paper No.: 20210304

Micron Ex. 1016, p. 173
Micron v. YMTC
IPR2025-00191

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/745,342	Guo et al.
	Examiner	**Art Unit**
	DZUNG T TRAN	2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/22/2020	11/30/2020	03/04/2021						
1	1	÷	✓	=						
2	2	÷	✓	=						
3	3	÷	✓	=						
4	4	÷	✓	=						
5	5	÷	✓	=						
6	6	÷	✓	=						
7	7	÷	✓	=						
8	8	÷	✓	=						
9	9	÷	✓	=						
10	10	÷	✓	=						
11	11	÷	✓	=						
	12	÷	✓	-						
12	13	÷	✓	=						
13	14	÷	✓	=						
	15	÷	N	-						
	16	÷	N	-						
	17	÷	N	-						
	18	÷	N	-						
	19	÷	N	-						
	20	÷	N	-						
14	21			=						
15	22			=						
16	23			=						
17	24			=						
18	25			=						
19	26			=						
20	27			=						

Micron Ex. 1016, p. 174
Micron v. YMTC
IPR2025-00191

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S105	5	("20120119287" | "20120280304" | "20130264631" | "20150179660" | "20150206895").PN.	US-PGPUB; USPAT	OR	OFF	2020/11/28 11:07
S106	2,576	((("LIU") near3 ("Jun"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/11/28 11:08
S107	3,495	(257/314).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:08
S108	3,490	S107 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:09
S109	3,341	S108 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:09
S110	2,939	S109 and (bit line)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:09
S111	1,833,537	6and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:09
S112	1,965	S110 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 11:09
S113	2,193	H01L27/11531.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/11/28 12:06
S114	3,229	H01L21/76816.CPC.	US-PGPUB	OR	OFF	2020/11/28 12:09
S115	2,457	S114 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 12:09
S116	1,254	S115 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 12:09

S117	2,039	S115 and (bit line)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 12:09
S118	2,197	S116 S117	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 12:09
S119	5,627	H01L21/76877.CPC.	US-PGPUB	OR	OFF	2020/11/28 13:07
S120	4,301	S119 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 13:07
S121	1,929	S120 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 13:07
S122	8	("20130264631" | "20160099255" | "20120280304" | "20150206895" | "20140175532" | "20150179660" | "20170125430" | "20120119287").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 13:30
S123	1	("20200161321").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 13:31
S124	3	S122 and dummy	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 14:19
S125	6,821	H01L23/5226.CPC.	US-PGPUB	OR	OFF	2020/11/28 14:33
S126	4,604	S125 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 14:33
S127	2,431	S126 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 14:33
S128	1,975	S127 and (bit line)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 14:33
S129	1	(14/133979).APP.	USPAT; USOCR	OR	OFF	2020/11/28 16:37
S130	72	("20070210338" | "20070252201" | "20090230449" | "20090230454" | "20090242967" | "20100044778" | "20100112769" | "20100120214" | "20100155810" | "20100155818" | "20100181610" | "20100207195" | "20100320528" | "20110076819" | "20110133606" | "20110266606" | "20110303970" | "20120001247" |	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 16:37

		"20120001249" | "20120001250" | "20120012920" | "20120032245" | "20120208347" | "20130089974" | "20130264631" | "7005350" | "7023739" | "7177191" | "7221588" | "7233522" | "7514321" | "7575973" | "7696559" | "7745265" | "7808038" | "7848145" | "7851851" | "8008710" | "8053829" | "8187936" | "8394716").PN. OR ("9449983").URPN.				
S131	85	("10008570" | "10121794" | "10553599" | "10559588" | "20030047755" | "20030122204" | "20030155582" | "20030219933" | "20040041192" | "20040063286" | "20040125629" | "20040251488" | "20050062098" | "20080012065" | "20090321855" | "20100109071" | "20110045657" | "20110287612" | "20120023894" | "20120068247" | "20120276702" | "20130009236" | "20130089974" | "20130134492" | "20140225160" | "20140225181" | "20140264525" | "20150129954" | "20150179660" | "20160049421" | "20160099250" | "20160118391" | "20160141294" | "20160181264" | "20160260733" | "20160358933" | "20170062454" | "20170110464" | "20170110470" | "20170162591" | "20170229472" | "20170338243" | "20170365613" | "20180122906" | "20190252405" | "20190326313" | "5915167" | "6274490" | "6372569" | "6677213" | "6777274" | "6833306" | "6881994" | "7005350" | "7012299" | "7202119" | "8187936" | "8829593" | "8884357" | "8946023" | "9023719" | "9136130" | "9177966" | "9230980" | "9230987" | "9305932" | "9331093" | "9356031" | "9425299" | "9449980" | "9449983" | "9460931" | "9478495" | "9502471" | "9570463" | "9576975" | "9627395" | "9627403" | "9691884" | "9698153" | "9728551" | "9780108" | "9853043" | "9876025" | "9941295").PN. OR ("10797060").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 16:47

S132	72	("10115735" | "10355017" | "20060157797" | "20070155074" | "20070210338" | "20070252201" | "20080096328" | "20080116583" | "20090230449" | "20090242967" | "20100044778" | "20100090286" | "20100112769" | "20100120214" | "20100155810" | "20100155818" | "20100181610" | "20100207195" | "20100320528" | "20110076819" | "20110133606" | "20110233688" | "20110266606" | "20120001247" | "20120001249" | "20120001250" | "20120012920" | "20120119287" | "20120168877" | "20120261756" | "20120280290" | "20130140669" | "20130161746" | "20130181264" | "20130217190" | "20130264631" | "20130320417" | "20140117421" | "20140154846" | "20150008520" | "20150206945" | "20150214058" | "20150364490" | "20160163702" | "20160260712" | "20160351709" | "20180331118" | "5915167" | "6319782" | "6323525" | "7005350" | "7023739" | "7177191" | "7221588" | "7233522" | "7514321" | "7575973" | "7696559" | "7745265" | "7808038" | "7848145" | "7851851" | "8008710" | "8053829" | "8187936" | "8394716" | "9023719" | "9305934" | "9449983" | "9460931" | "9601503" | "9859422").PN. OR ("10770459").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 16:47
S133	0	(15/873101).APP.	US-PGPUB; USOCR	OR	OFF	2020/11/28 16:55
S134	10	("6169019" | "20170133398" | "5945350" | "20160351709" | "20030190497" | "5576579" | "5942799" | "6229211" | "20180040476" | "5847463" | "6268299" | "20180245215" | "20060084247" | "5874353" | "20150138862" | "20030025206" | "20020140103" | "20030194859").PN.	US-PGPUB; USOCR	OR	OFF	2020/11/28 16:57
S135	1	("20180331118").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 16:59

S136	1	(15/080269).APP.	US-PGPUB; USOCR	OR	OFF	2020/11/28 17:01
S137	1	("20160204117").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 17:02
S138	1	(14/862916).APP.	US-PGPUB; USOCR	OR	OFF	2020/11/28 17:03
S139	1	("20160322381").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 17:03
S140	1	(14/611785).APP.	US-PGPUB; USOCR	OR	OFF	2020/11/28 17:04
S141	1	("20150236038").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/11/28 17:04
S142	14	(US-20170125430-$ or US-20150179660-$ or US-20180122906-$ or US-20120119287-$ or US-20170062454-$ or US-20180331118-$ or US-20160204117-$ or US-20160322381-$ or US-20150236038-$).did. or (US-8664761-$ or US-9449987-$ or US-10453798-$ or US-9806093-$ or US-10381322-$).did.	US-PGPUB; USPAT	OR	OFF	2020/11/30 10:31
S143	2	(("20120280304") or ("20200161321")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2021/01/29 13:50
S144	220	((("GUO") near3 ("Mei") near3 ("Lan")) OR (("HU") near3 ("Yushi")) OR (("XIA") near3 ("Ji")) OR (("ZHU") near3 ("Hongbin"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2021/03/04 10:34
S145	1,549	(257/315).CCLS.	US-PGPUB	OR	OFF	2021/03/04 10:34
S146	1,326	(257/314).CCLS.	US-PGPUB	OR	OFF	2021/03/04 10:38
S147	1,027	H01L27/11531.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 11:25
S148	1,027	H01L27/11531.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 11:25
S149	3,337	H01L21/76816.CPC.	US-PGPUB	OR	OFF	2021/03/04 11:32

S150	2,461	S149 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 11:32
S151	1,249	S150 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 11:32
S152	5,796	H01L21/76877.CPC.	US-PGPUB	OR	OFF	2021/03/04 11:46
S153	4,304	S152 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 11:46
S154	1,932	S153 and stacK$3	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 11:47
S155	7,132	H01L23/5226.CPC.	US-PGPUB	OR	OFF	2021/03/04 13:26
S156	4,606	S155 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 13:26
S157	2,161	S156 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 13:26
S158	0	H01L23/5283.CPC1	US-PGPUB	OR	OFF	2021/03/04 13:27
S159	2,521	H01L23/5283.CPC.	US-PGPUB	OR	OFF	2021/03/04 13:27
S160	1,622	S159 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 13:29
S161	3,255	H01L27/11524.CPC.	US-PGPUB	OR	OFF	2021/03/04 14:19
S162	2,481	S161 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 14:19
S163	2,468	S162 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 14:19
S164	1,852	S163 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 14:20
S165	2,019	H01L27/11529.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 14:20
S166	5,634	H01L27/11556.CPC.	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 14:59

S167	3,084	H01L27/11556.CPC.	US-PGPUB	OR	OFF	2021/03/04 14:59
S168	1,760	S167 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 15:00
S169	3,129	H01L27/1157.CPC.	US-PGPUB	OR	OFF	2021/03/04 15:05
S170	1,803	S169 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 15:08
S171	2,336	H01L27/11573.CPC.	US-PGPUB	OR	OFF	2021/03/04 15:45
S172	1,379	S171 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 15:45
S173	5,703	H01L27/11582.CPC.	US-PGPUB	OR	OFF	2021/03/04 15:46
S174	3,326	S173 and @pd<"20180914"	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 15:46
S175	3,286	S174 and (memory string)	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 15:46
S176	3,067	S175 and stack$3	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 15:46
S177	2,423	S176 and (hole recess$3)	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 15:46
S178	2,354	S177 and (bit line)	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 15:47
S179	2,251	S178 and (word data)	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 15:47
S180	1	("20120098048").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2021/03/04 16:48

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S181	0	(memory near stack$3 near2 substrate near2 interleav$3 near2 plurality near2 conduct$3 near layers near2 dielectric near layers near4	USPAT	OR	OFF	2021/03/04 15:21

		plurality near2 conduct$4 near layers near3 respect$3 near shallow near recess) and (channel near structure near extend$3 near vertically near2 memory near stack$3).clm.				

3/4/2021 5:29:22 PM
H:\East search\16_745342_memory string.wsp

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

153988 7590 03/10/2021
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Anna J. O'Connor	(Typed or printed name)
/Anna J. O'Connor/	(Signature)
May 27, 2021 E-FILED	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/745,342	01/17/2020	Mei Lan Guo	10018-01-0015-US-DIV1	2958

TITLE OF INVENTION: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/10/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, DZUNG	2829	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 BAYES PLLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)
YANGTZE MEMORY TECHNOLOGIES CO., LTD.	WUHAN, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 60-2227

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date 5/27/2021

Typed or printed name Zhiwei Zou Registration No. 66,041

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Micron Ex. 1016, p. 183
Micron v. YMTC
IPR2025-00191

Electronic Patent Application Fee Transmittal

Application Number:	16745342
Filing Date:	17-Jan-2020
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Filer:	Zhiwei Zou/Anna O'Connor
Attorney Docket Number:	10018-01-0015-US-DIV1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1200**

Electronic Acknowledgement Receipt

EFS ID:	42843739
Application Number:	16745342
International Application Number:	
Confirmation Number:	2958
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Mei Lan Guo
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0015-US-DIV1
Receipt Date:	27-MAY-2021
Filing Date:	17-JAN-2020
Time Stamp:	22:08:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1200
RAM confirmation Number	E20215QM08330777
Deposit Account	602227
Authorized User	Anna O'Connor

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	10018-01-0015-US-DIV1_IFTransmittal.pdf	291448 2960b363d1396845ff432e163dd6353589cb2ee6	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30353 981092af7326e299d1e667231e2c98dc45053ada	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	321801	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/745,342	06/29/2021	11049866	10018-01-0015-US-DIV1	2958

153988 7590 06/09/2021

Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Mei Lan Guo, Wuhan, CHINA;
YANGTZE MEMORY TECHNOLOGIES CO., LTD., Wuhan, CHINA;
Yushi Hu, Wuhan, CHINA;
Ji Xia, Wuhan, CHINA;
Hongbin Zhu, Wuhan, CHINA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IR103 (Rev. 10/09)