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Chevallier

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[45] Date of Patent: Aug. 31, 1999

[54] **SEGMENTED NON-VOLATILE MEMORY ARRAY HAVING MULTIPLE SOURCES**

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[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **09/031,972**

[22] Filed: **Feb. 26, 1998**

Related U.S. Application Data

[63] Continuation of application No. 08/814,326, Mar. 11, 1997, Pat. No. 5,793,087.

[51] **Int. Cl.**[6] **H01L 29/78**; G11C 7/00

[52] **U.S. Cl.** **257/390**; 257/401; 257/920; 365/185.12; 365/218

[58] **Field of Search** 365/218, 185.11, 365/185.12; 257/390, 401, 314, 315, 316, 920

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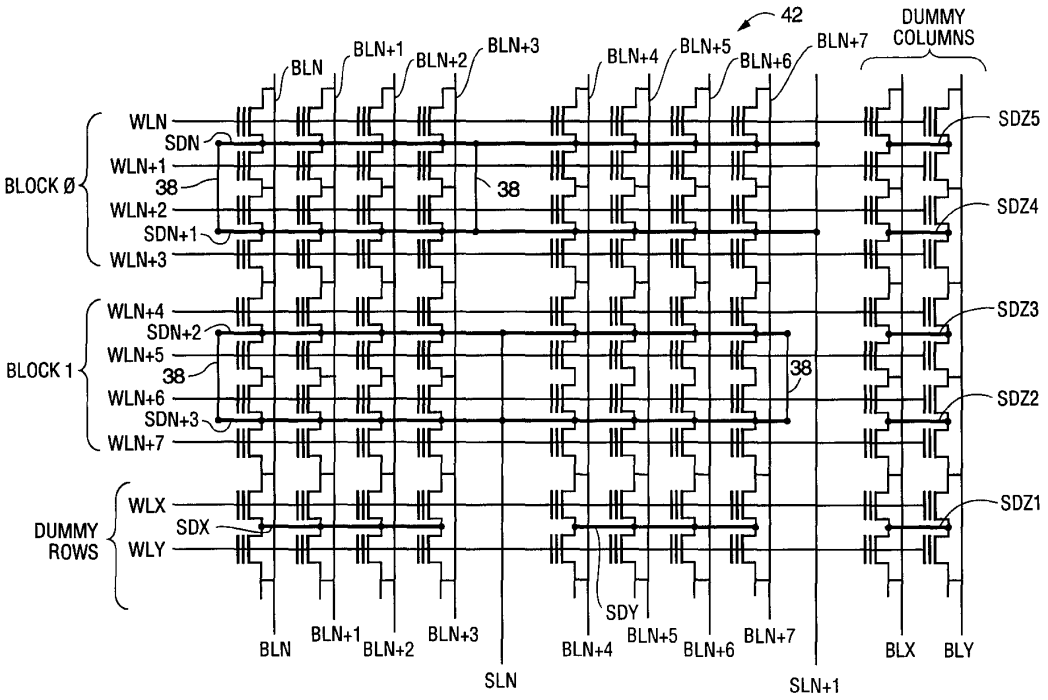
Primary Examiner—Donald L. Monin, Jr.

Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth P.A.

[57] **ABSTRACT**

An arrangement of non-volatile memory cells, such as flash memory cells which includes erase blocks which can be separately erased and which require a reduced amount of circuit area. The erase blocks each include an array of the cells arranged in rows and columns. Each cell in a row has its control gate connected to a common word line and its drain connected to a common bit line. All of the sources of one of the erase blocks are connected together by a source line structure which includes non-metallic source lines, such as doped semiconductor lines, which run generally parallel with respect to the word line and interconnect the sources of cell located in a row. The source line structure further includes at least one metallic source line which functions to interconnect the source regions of cells located in one of the erase block cell columns. The metallic source line of one of the erase blocks extends over, but is not connected to, the adjacent erase block, with the source lines of the erase blocks preferably being connected to a common source line decoder used to control the status of a selected one of the source lines so that a selected one of the erase blocks can be erased.

3 Claims, 12 Drawing Sheets



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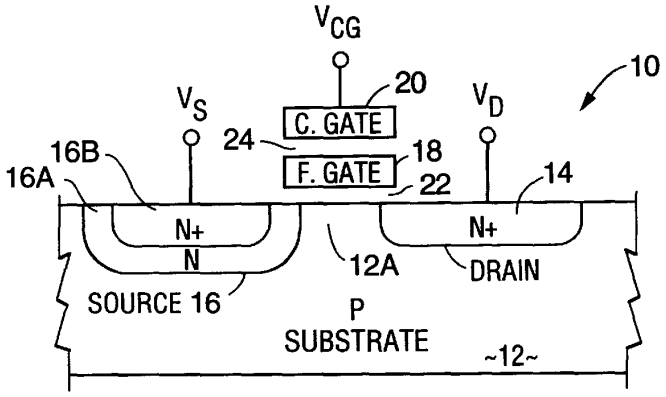

FIG. 1
(PRIOR ART)

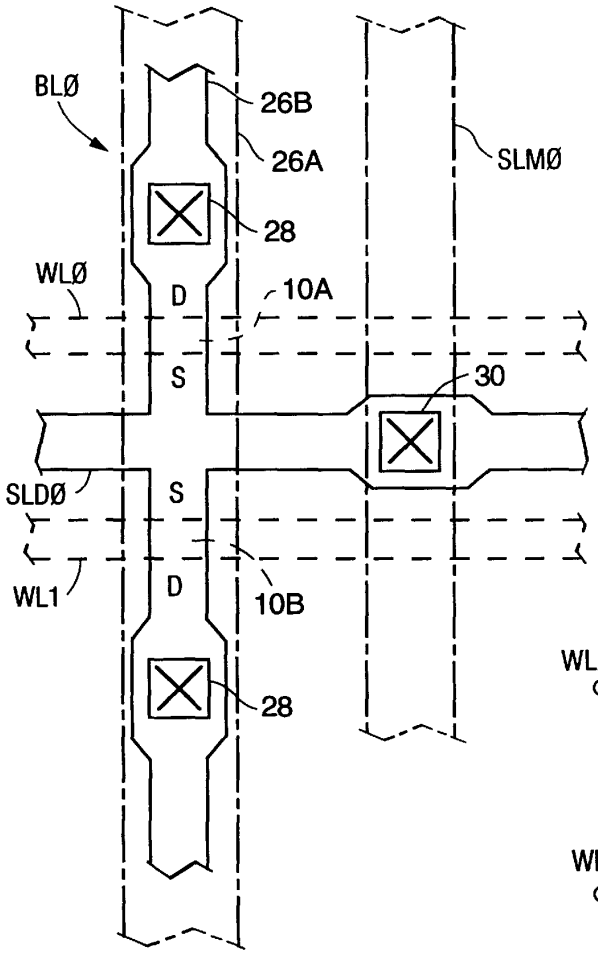

FIG. 2A
(PRIOR ART)

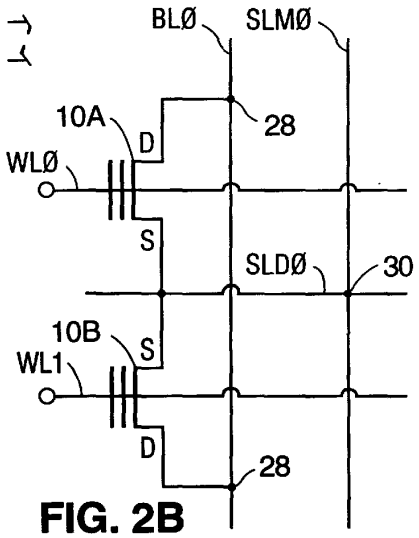

FIG. 2B
(PRIOR ART)

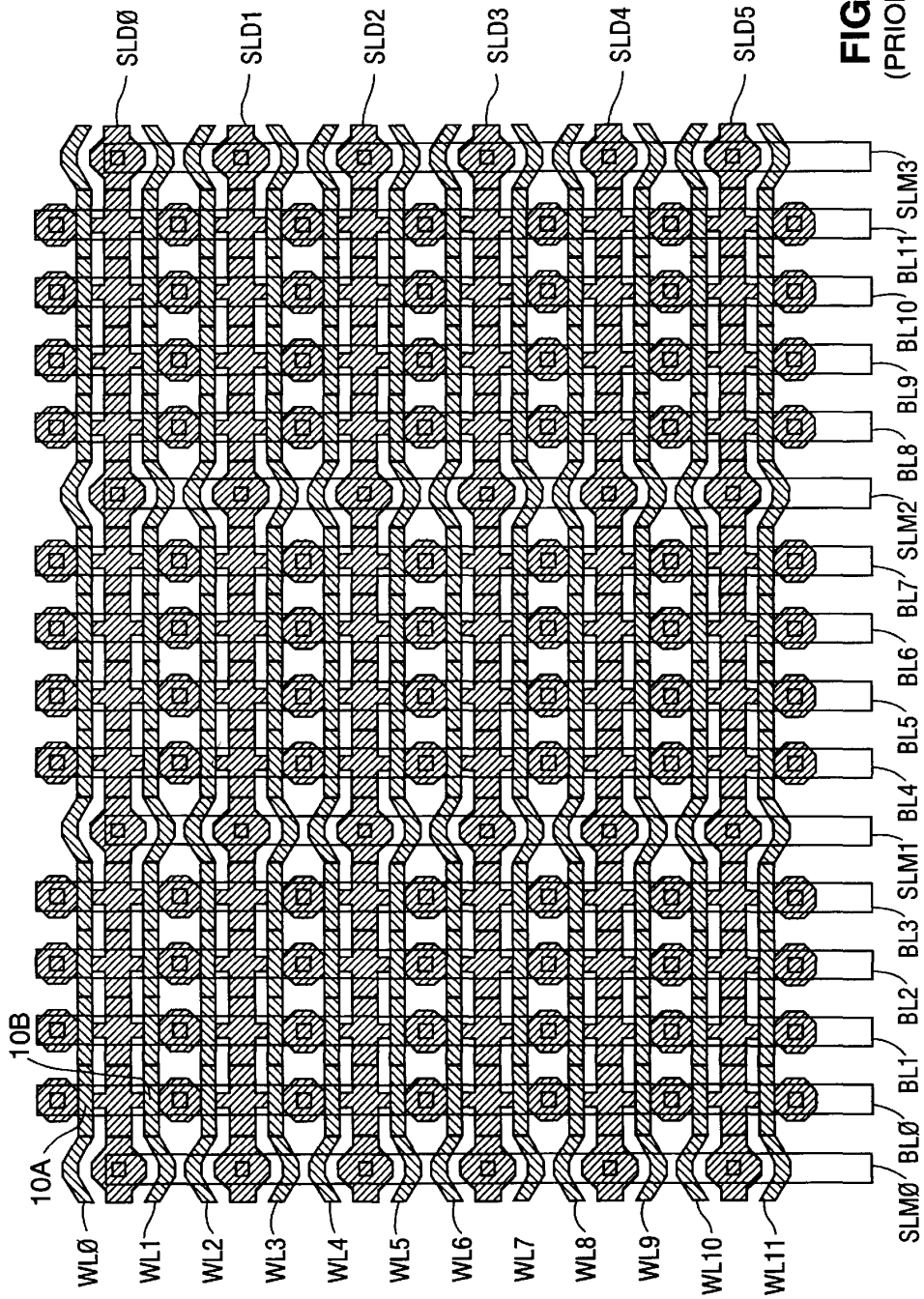

FIG. 3A
(PRIOR ART)

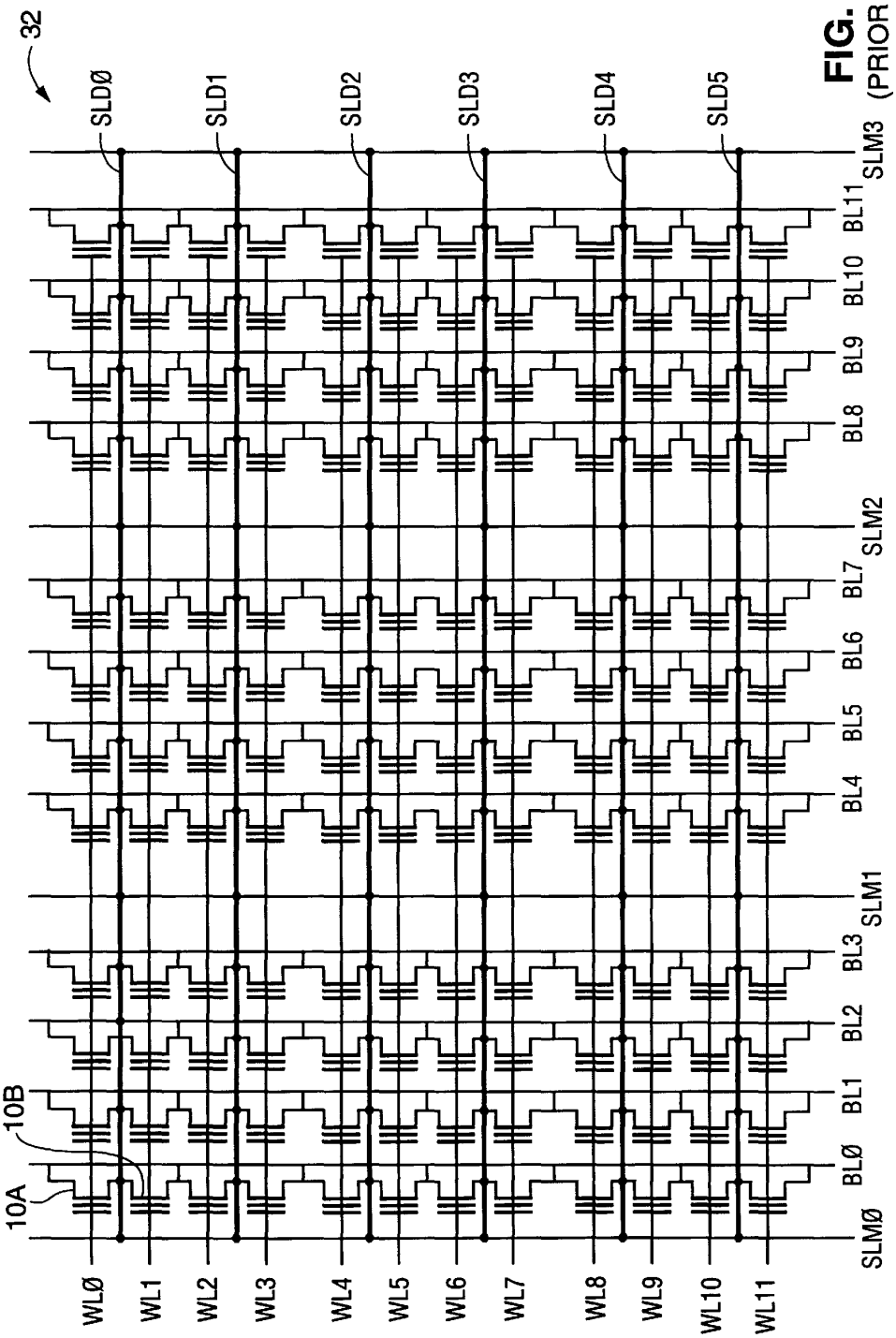

FIG. 3B (PRIOR ART)

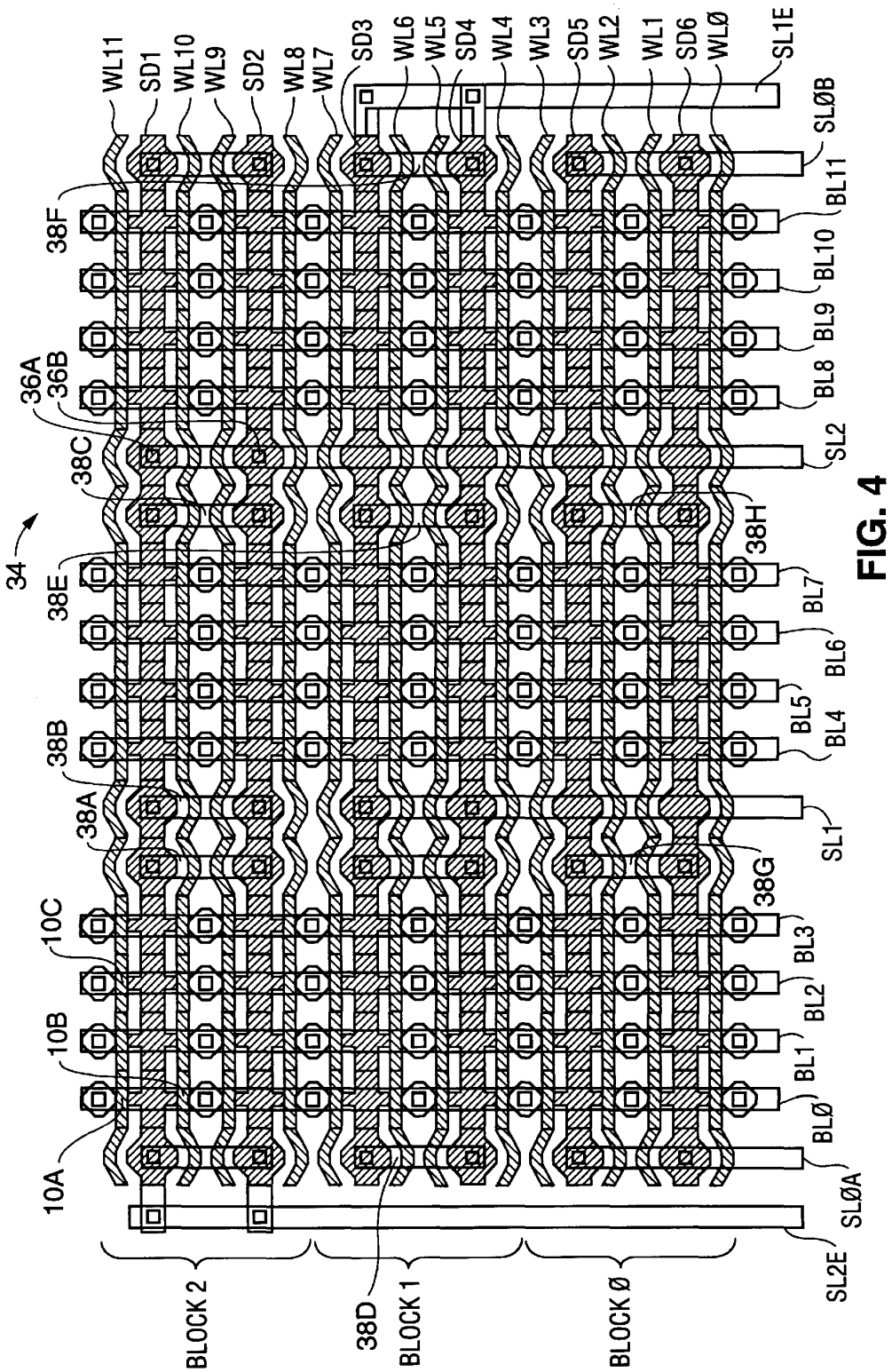
WL11
SD1
WL10
WL9
SD2
WL8
WL7
SD3
WL6
WL5
SD4
WL4
WL3
SD5
WL2
WL1
SD6
WLØ
SL1E
SLØB
BL11
BL10
BL9
BL8
SL2
BL7
BL6
BL5
BL4
SL1
BL3
BL2
BL1
BLØ
SLØA
SL2E
38F
36A
36B
38C
34
38E
38B
38A
10C
10B
10A
38H
38G
38D
BLOCK 2
BLOCK 1
BLOCK Ø

FIG. 4

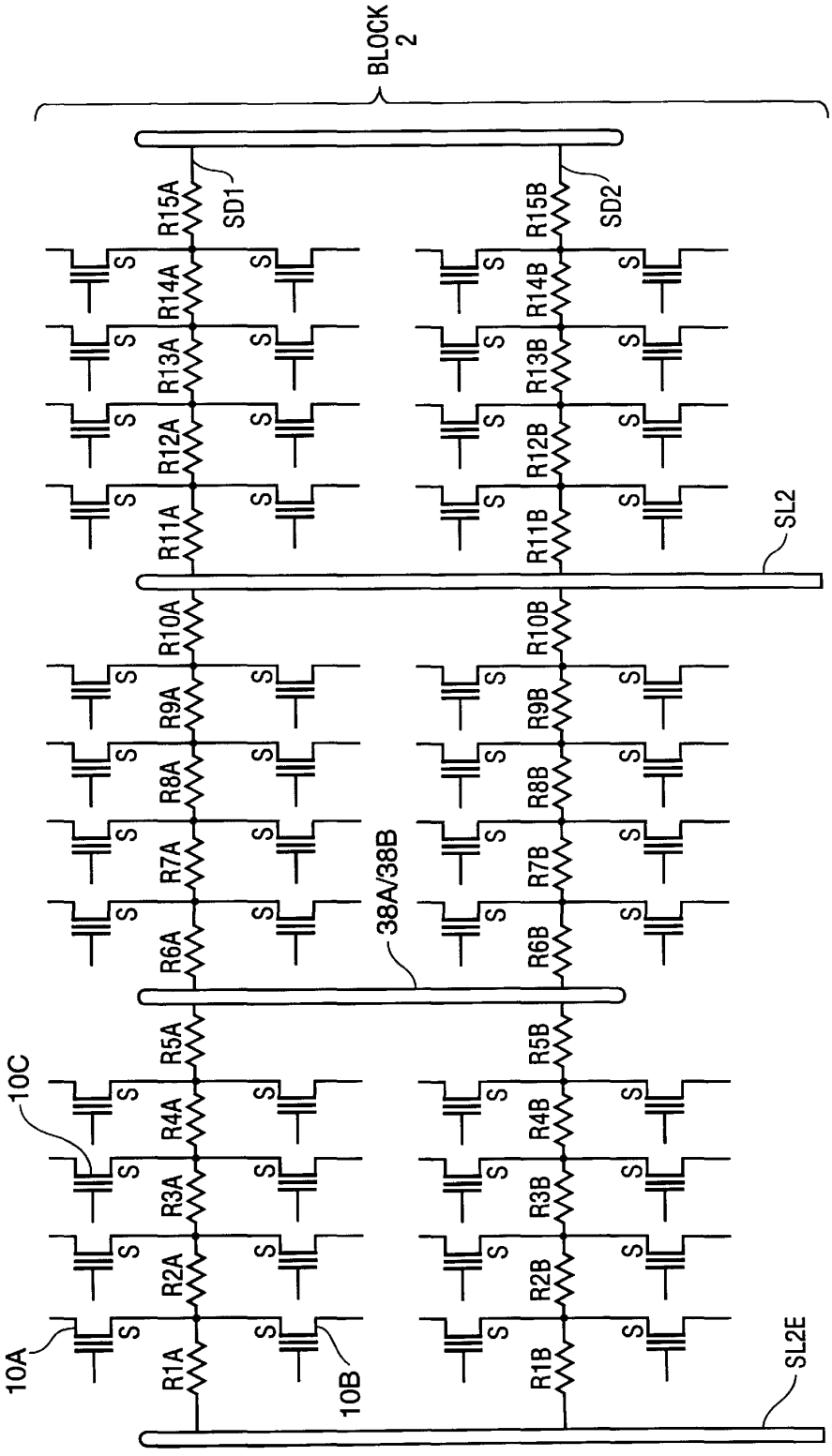
BLOCK 2
SD1
SD2
R15A
R15B
R14A
R14B
R13A
R13B
R12A
R12B
R11A
R11B
SL2
R10A
R10B
R9A
R9B
R8A
R8B
R7A
R7B
R6A
R6B
38A/38B
R5A
R5B
R4A
R4B
R3A
R3B
R2A
R2B
R1A
R1B
10C
10A
10B
SL2E
S

FIG. 5

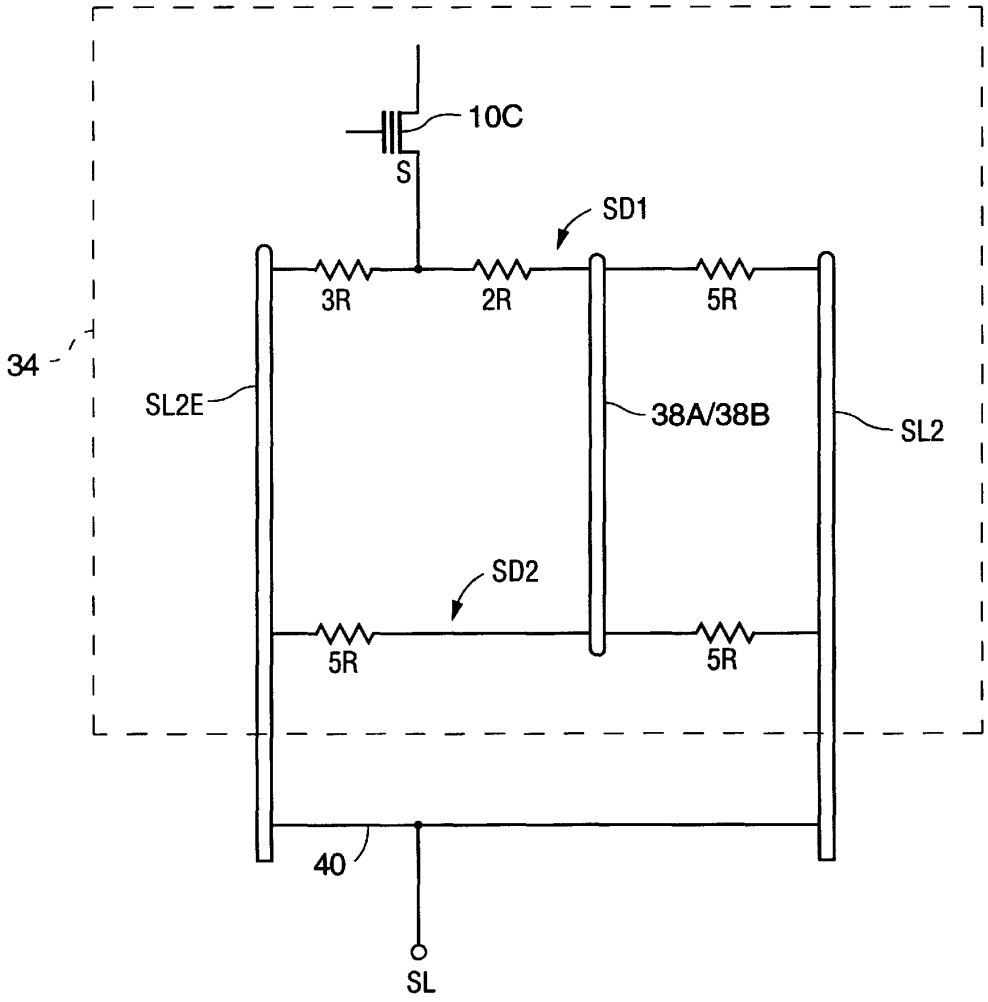

FIG. 6

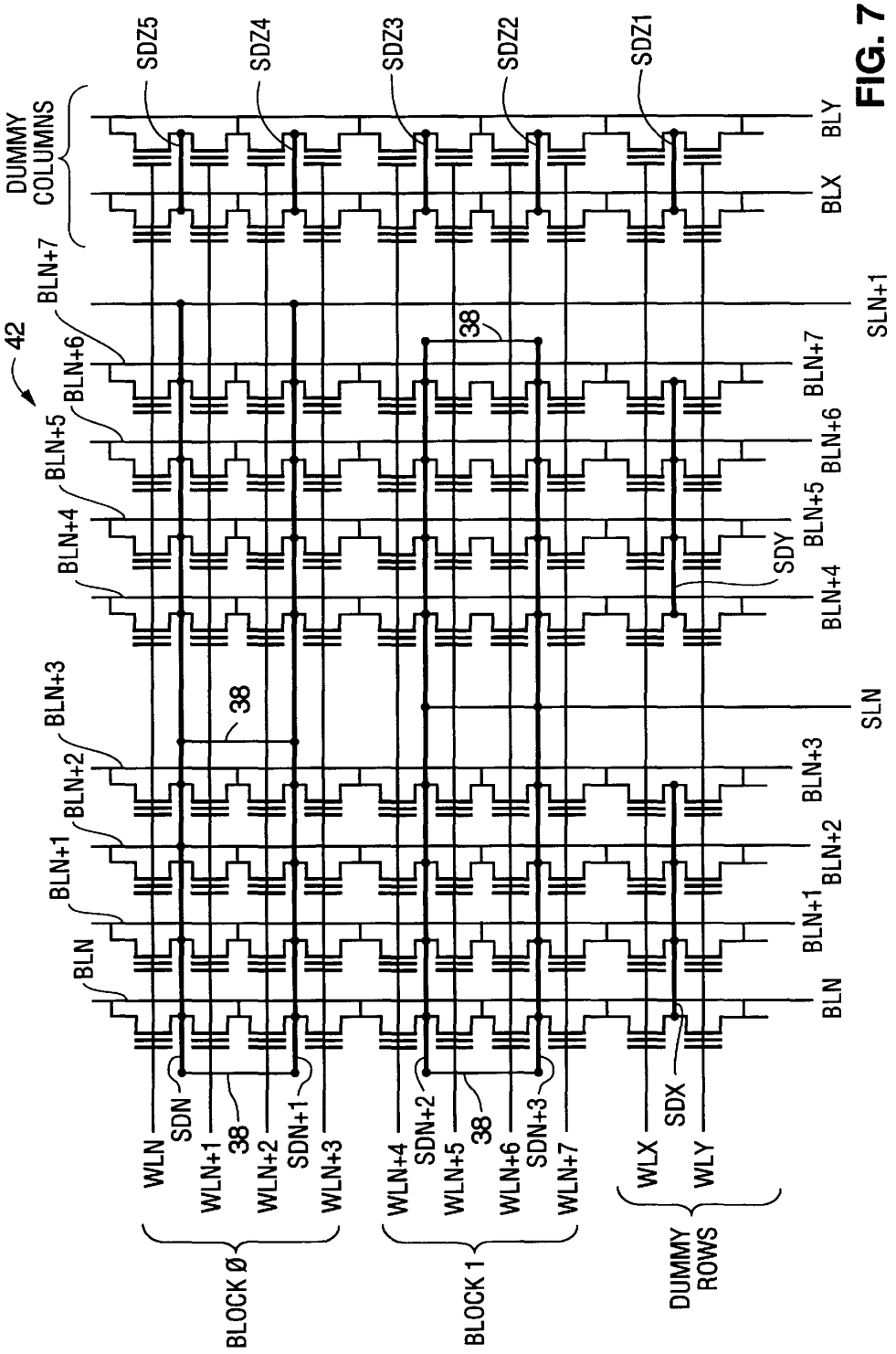
SDZ5
SDZ4
SDZ3
SDZ2
SDZ1
DUMMY COLUMNS
BLY
BLX
BLN+7
SLN+1
42
38
BLN+6
BLN+5
BLN+4
SDY
BLN+3
SLN
BLN+2
BLN+1
BLN
WLN
SDN
WLN+1
WLN+2
SDN+1
WLN+3
WLN+4
SDN+2
WLN+5
WLN+6
SDN+3
WLN+7
WLX
SDX
WLY
BLOCK Ø
BLOCK 1
DUMMY ROWS

FIG. 7

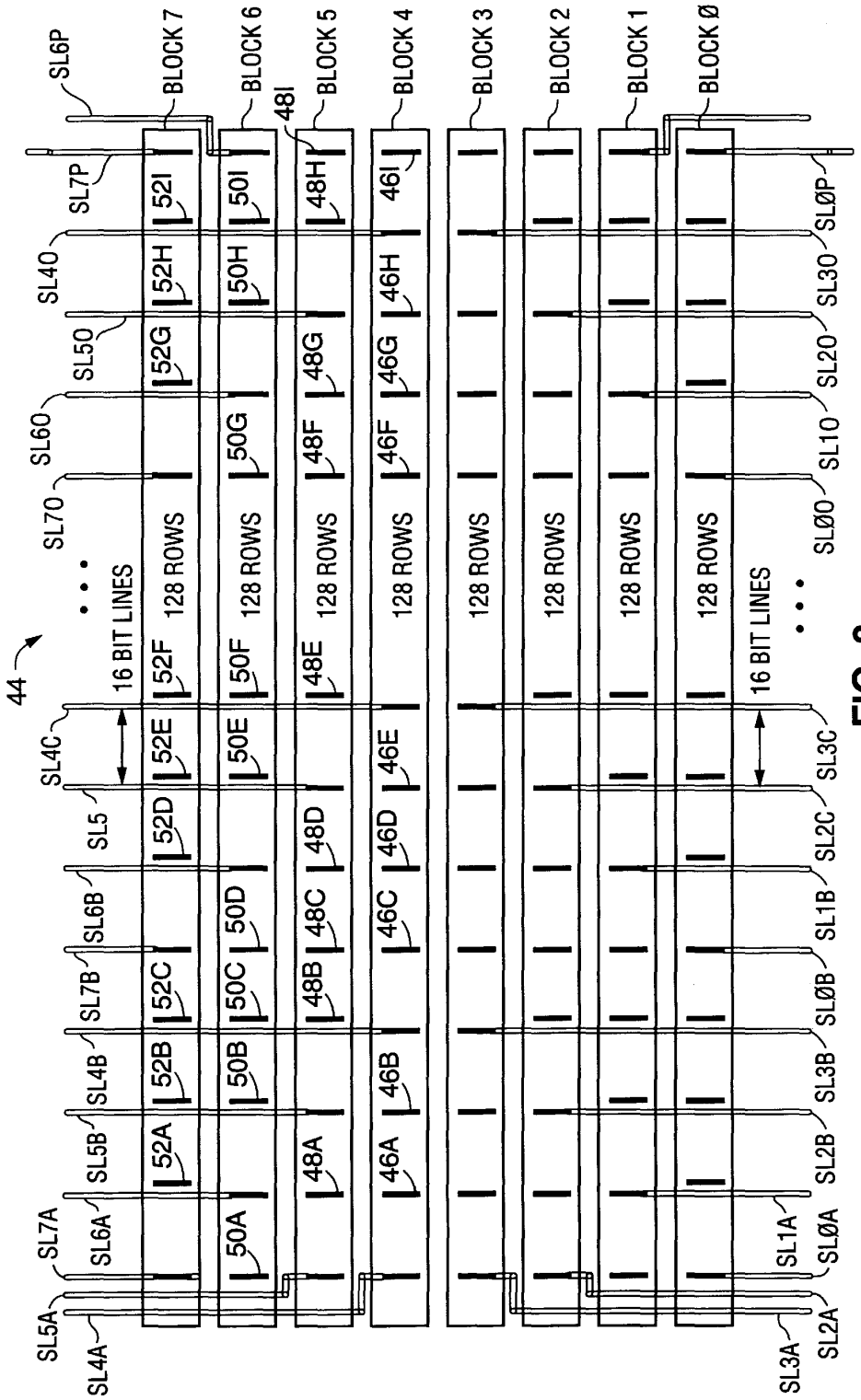
44
BLOCK 7
BLOCK 6
BLOCK 5
BLOCK 4
BLOCK 3
BLOCK 2
BLOCK 1
BLOCK Ø
128 ROWS
16 BIT LINES
SL6P
SL7P
SL40
SL50
SL60
SL70
SL4C
SL5
SL6B
SL7B
SL4B
SL5B
SL7A
SL6A
SL5A
SL4A
SLØP
SL30
SL20
SL10
SLØ0
SL3C
SL2C
SL1B
SLØB
SL3B
SL2B
SL1A
SLØA
SL3A
SL2A
48I
52I
50I
48H
46I
52H
50H
46H
52G
50G
48G
46G
52F
50F
48F
46F
52E
50E
48E
46E
52D
50D
48D
46D
52C
50C
48C
46C
52B
50B
48B
46B
52A
50A
48A
46A

FIG. 8

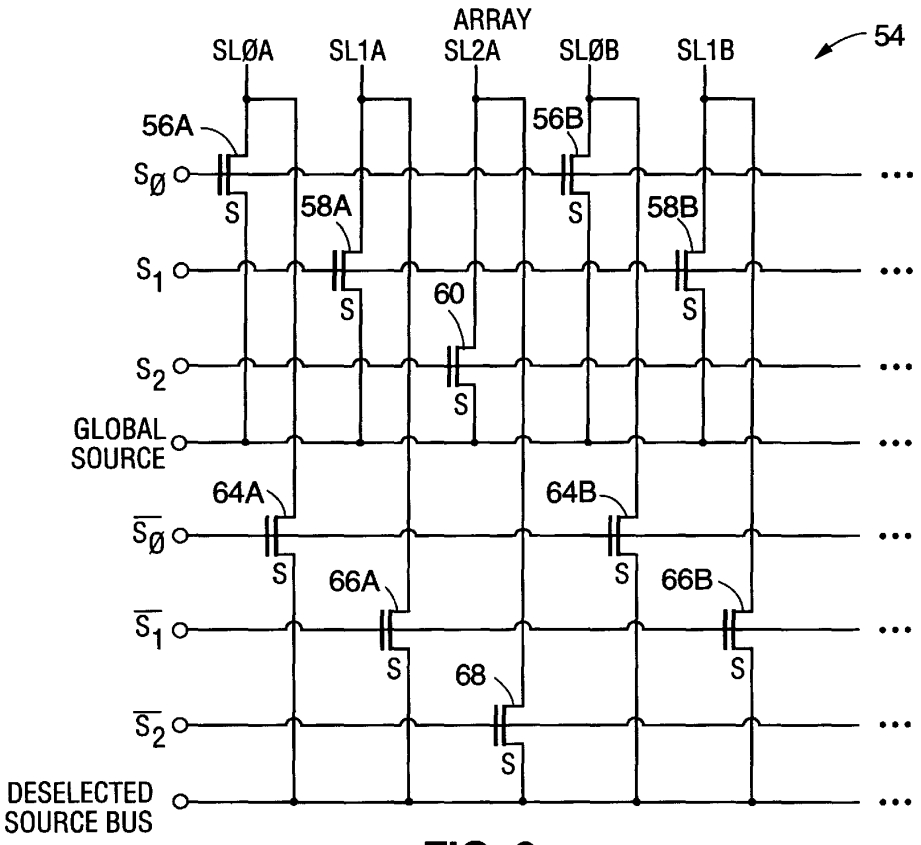
ARRAY
SLØA
SL1A
SL2A
SLØB
SL1B
54
56A
56B
SØ
S
58A
58B
S1
60
S2
GLOBAL SOURCE
64A
64B
S̄Ø
66A
66B
S̄1
68
S̄2
DESELECTED SOURCE BUS

FIG. 9

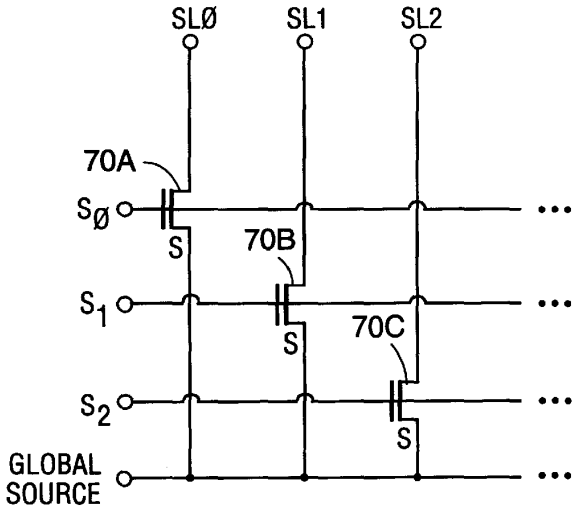
SLØ
SL1
SL2
70A
SØ
S
70B
S1
70C
S2
GLOBAL SOURCE

FIG. 10

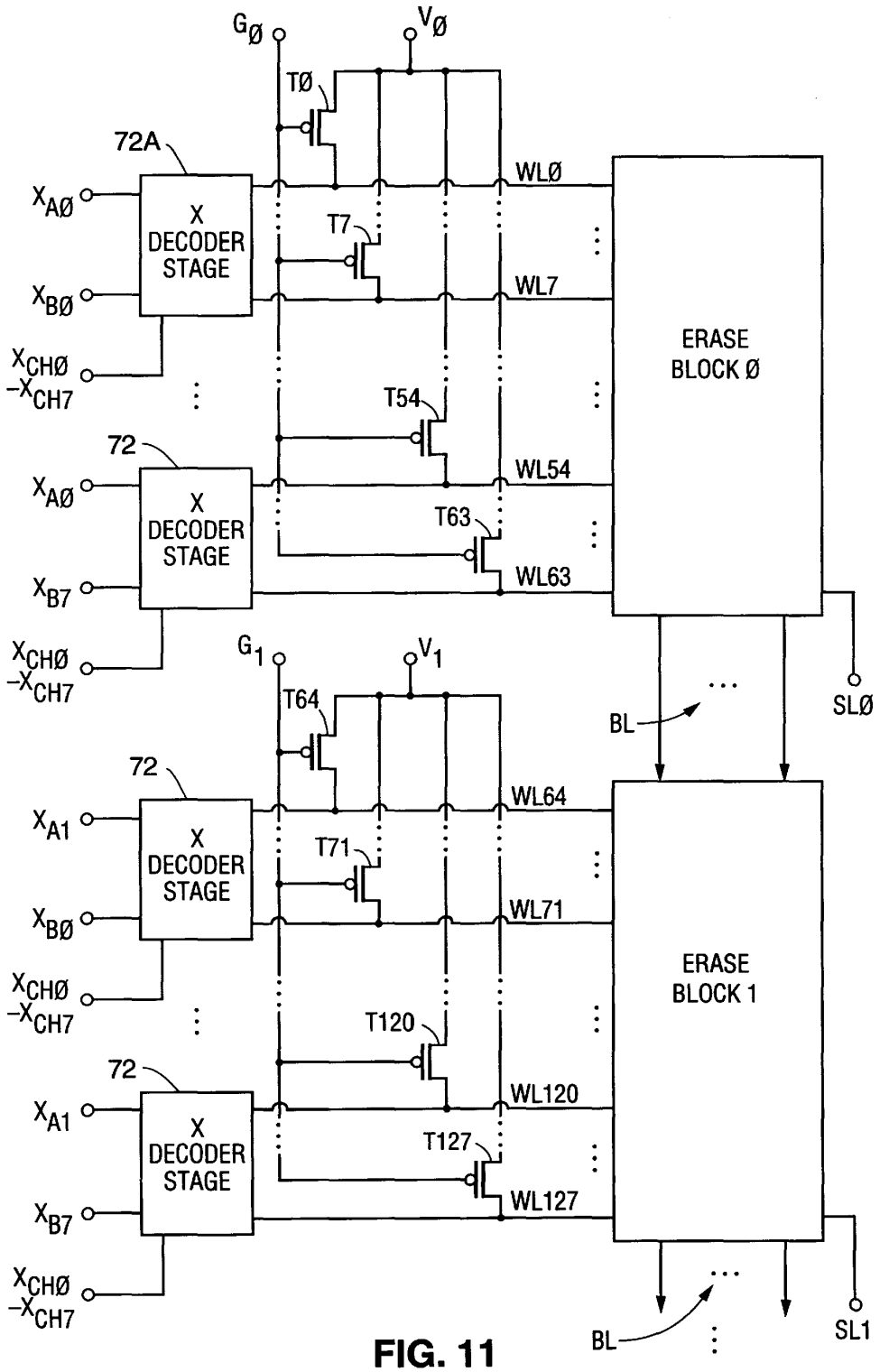
GØ
VØ
TØ
72A
XAØ
XBØ
XCHØ
-XCH7
X DECODER STAGE
WLØ
T7
WL7
ERASE BLOCK Ø
T54
72
WL54
T63
WL63
XB7
G1
V1
T64
BL
SLØ
WL64
T71
WL71
ERASE BLOCK 1
XA1
T120
WL120
T127
WL127
SL1

FIG. 11

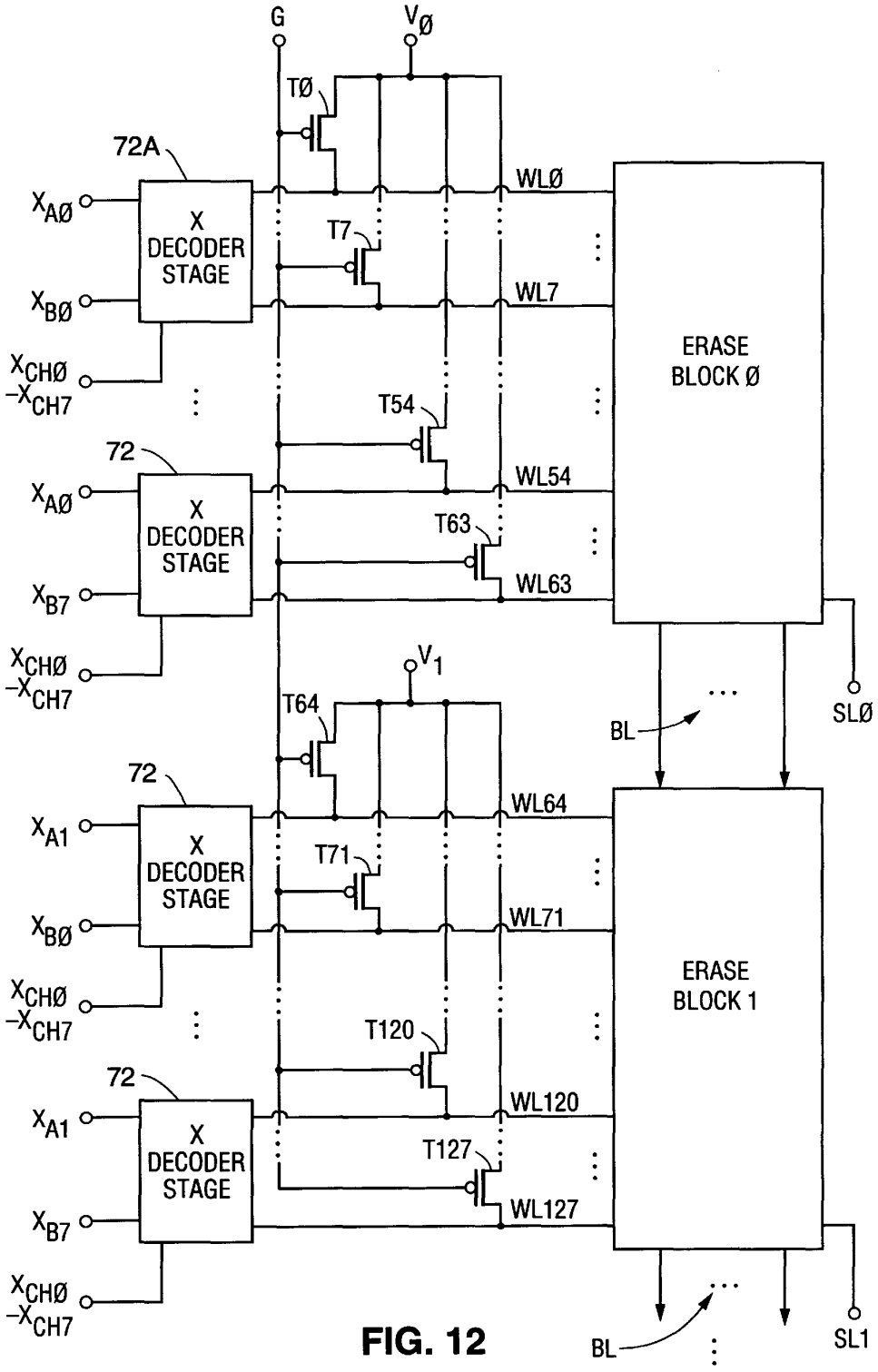
G
$V_Ø$
TØ
72A
$X_{AØ}$
$X_{BØ}$
$X_{CHØ}$
$-X_{CH7}$
X DECODER STAGE
T7
WLØ
WL7
ERASE BLOCK Ø
T54
72
WL54
T63
X_{B7}
WL63
V_1
T64
BL
SLØ
WL64
X_{A1}
T71
WL71
ERASE BLOCK 1
T120
WL120
T127
WL127
SL1

FIG. 12

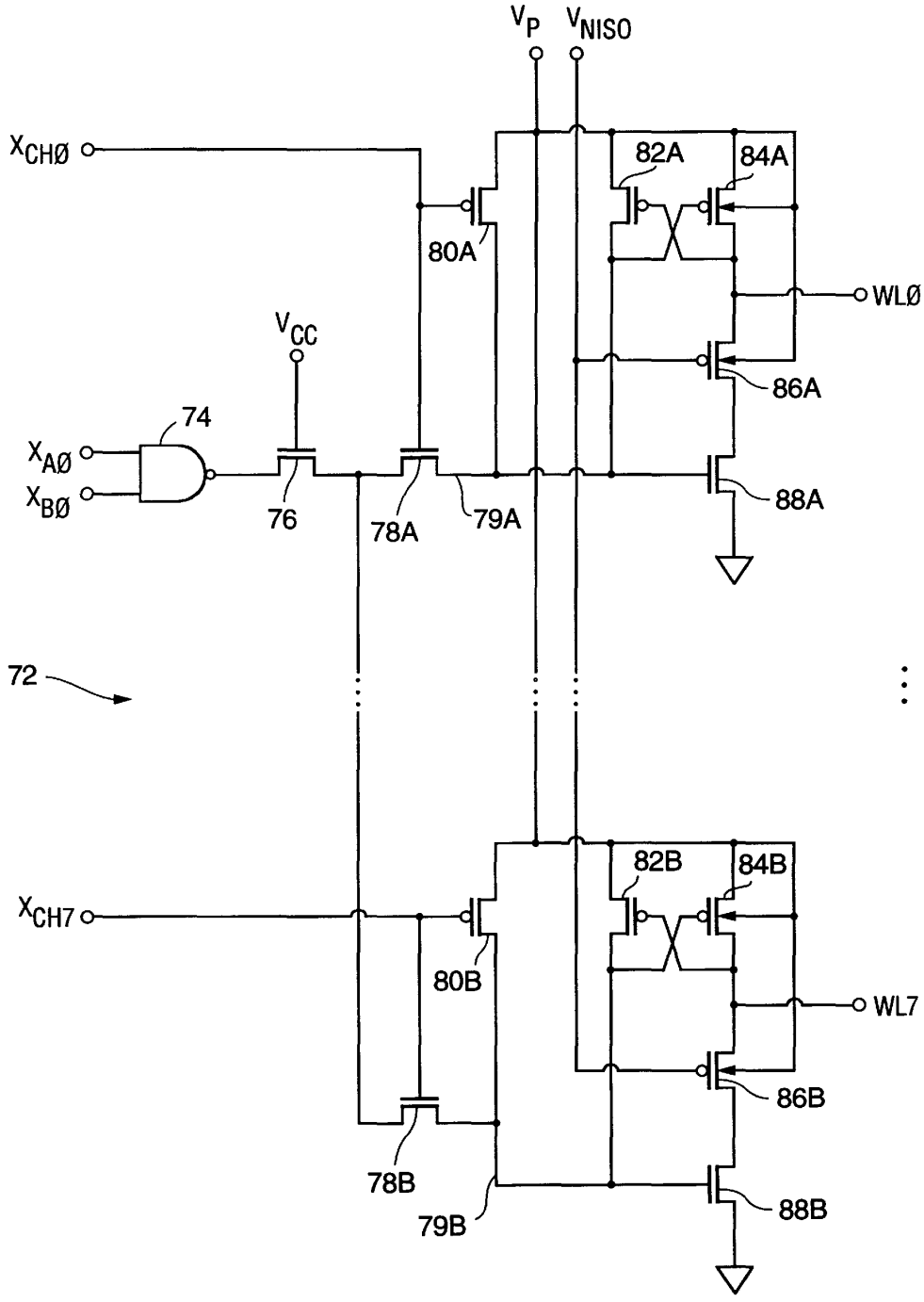
V_P
V_{NISO}
$X_{CH\emptyset}$
82A
84A
80A
WL$\emptyset$
V_{CC}
86A
74
$X_{A\emptyset}$
$X_{B\emptyset}$
76
78A
79A
88A
72
82B
84B
X_{CH7}
80B
WL7
86B
78B
79B
88B

FIG. 13

SEGMENTED NON-VOLATILE MEMORY ARRAY HAVING MULTIPLE SOURCES

This application is a continuation of U.S. patent application Ser. No. 08/814,326, filed Mar. 11, 1997 (the '326 Application) now U.S. Pat. No. 5,793,087. The '326 Application is incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates generally to semiconductor memory systems and in particular to a segmented non-volatile memory array having multiple sources so that blocks of the array can be erased separately.

BACKGROUND ART

Non-volatile semiconductor memory systems have become increasingly popular, including flash memory systems. FIG. **1** is a simplified diagram of the cross-section of a typical flash memory cell **10**. Cell **10** is an N-channel device formed in a P-type substrate **12**. An N-type drain region **14** is formed in substrate **12** as is an N-type source region **16**. Source region **16** includes an N-type region **16**A formed in the substrate **12** having a an N+-type region **16**B formed inside region **16**A so as to form a graded source region **16**.

The drain and regions source **14** and **16** are spaced apart from one another so as to form a channel region **12**A in the substrate intermediate the two regions. A floating gate **18** is disposed above the channel region **12**A and a control gate **20** is disposed above the floating gate **18**. The floating gate is separated from the channel region **12**A by a thin (100 Å) gate oxide layer **22**. The floating and control gates **18** and **20** are typically both formed from doped poly silicon. The control gate **20** is separated from the floating gate **18** by an interpoly dielectric layer **24**. Other than being capacitively coupled to other elements of cell **10**, the floating gate **18** is electrically isolated from the rest of the cell. Table 1 below shows typical conditions for performing program, read and erase operations on flash cell **10**.

TABLE 1

OPERATION	SOURCE (V_S)	DRAIN (V_P)	CONTROL GATE (V_S)
READ	ground	+1.5 volts	+5 volts
PROGRAM	ground	+6 volts	+12 volts
ERASE	+12 volts	float	ground

If cell **10** is in an erased state, the cell will have a threshold voltage, called an erased threshold voltage, which is typically approximately +2 volts. If the cell is in a programmed state, the cell will have a programmed threshold voltage of typically approximately +6 volts. In a read operation, the control-gate-to-source voltage of the cell is +5 volts as can be seen from Table 1, above. The drain **14** will be connected to a small positive voltage of typically +1.5 volts and the source **16** is grounded. Thus, if the cell **10** is in a programmed state, the cell will not conduct current in the read operation since the gate-to-source voltage of +5 volts is less than the programmed threshold voltage of +6 volts. If the cell is in an erased state, the gate to source voltage will exceed the erased threshold voltage so that the cell will conduct current. The presence or absence of cell current in a read operation is detected by a sense amplifier so that the state of the cell can be determined.

In order to program the flash cell **10**, Table 1 indicates that the source **16** is grounded and the drain **14** is connected to +6 volts. The control gate **20** is connected to a high voltage such as +12 volts.

The combination of conditions will cause electrons to travel from the source **16** towards the drain **14**. Some of these electrons will possess sufficient energy to pass through the gate oxide **22** towards the positive voltage on the control gate **20**. Those electrons, sometimes referred to as hot electrons, will be deposited on the floating gate **18** and will remain there until the cell **10** is erased. The presence of electrons on the floating gate **18** will tend to increase the threshold voltage of the cell, as previously noted.

A cell is erased, as indicated by Table 1, by floating the drain **14** and applying a large positive voltage, such as +12 volts, to the source **16**. The control gate **20** is left disconnected (floating). This combination causes electrons stored on the floating gate **18** to pass through the thin gate oxide **22** and to be transferred to the source **16**. The physical mechanism for the transfer is commonly referred to as Fowler Nordheim tunneling.

In a flash memory system, the flash cells **10** are arranged in a cell array which typically includes several rows and several columns of cells. Each of the rows has an associated word line connected to the control gate **20** of the cells **10** located in the row. Each of the columns has an associate bit line connected to the drain **14** of each cell located in the column. The sources **16** of all of the cells of the array are usually connected in common, but as will be explained, the sources may be separately connected.

FIG. **2**A is a simplified plan view of a conventional layout of a pair of flash cells **10**A and **10**B of a cell array. FIG. **2**B is a schematic diagram of cells **10**A and **10**B of FIG. **2**A. As can be seen in FIG. **2**B, cells **10**A and **10**B have their respective sources connected in common. Typically, the two sources are actually a single source region shared by the two cells **10**A and **10**B. Cells **10**A and **10**B are located in a common array column and in separated rows. The column has an associated bit line BL**0** which is connected to the drains of cells **10**A and **10**B. Cell **10**A is in a row having an associated word line WL**0** connected to its control gate **20** and cell **10**B is in an adjacent row having its control gate **20** connected to an associated word line WL**1**.

The bit lines, including bit line BL**0**, extend vertically along the array and include an underlying diffusion component **26**A of doped semiconductor material and an overlying metal line component **26**B. The metal line component **26**B makes electrical contact with the diffusion component **26**A every two cells **10** by way of contacts **28**. The source lines have a horizontal segment SLD**0** which runs generally parallel to the word lines and is made of doped semiconductor material. The source lines also have a vertical segment SLM**0** which runs generally parallel to the bit lines and is formed from metal. The horizontal and vertical components SLD**0** and SLM**0** are electrically connected by way of a contact **30** located at the intersection of the two segments every two rows of the array.

Cell **10**A has its control gate **20** connected to horizontal word line WL**0**, a doped polysilicon line which extends across the array. Cell **10**B has its control gate **20** connected to horizontal word line WL**1** which also extends across the array. A flash cell (**10**A, **10**B) is formed at the intersection of the each of the word lines and bit lines.

FIG. **3**A is a simplified plan view of the layout of a relatively small conventional flash cell array **32** and FIG. **3**B is a schematic diagram of the FIG. **3**A array. Array **32** is comprised of twelve rows, each having an associated horizontal polysilicon word line WL**0**–WL**11**. The array also has

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twelve columns, with each column having an associated metal bit line BL0–BL11. Array 32 also includes four vertical metal source lines SLM0–SLM3 which are connected in common to the six horizontal diffused source lines SLD0–SLD5. Each metal source line SLMN is connected to the diffused source lines SLDN every two rows. The metal source lines SLM are spaced every four columns. For example, adjacent metal source lines SLM0 and SLM1 are separated by four bit lines BL0–BL3.

The metal source lines SLM0–SLM3 are electrically connected together by circuitry (not depicted) external to array 32. Thus, all of the source lines of the array are nominally at the same electrical potential. However, the horizontal diffused source lines SLD0–SLD5 have a relatively high resistance, in comparison to the metal source lines. This high resistance can have an adverse impact upon memory operations, particularly programming and reading operations. The use of multiple metal source lines functions to reduce the overall source line resistance. However, each metal line occupies a significant amount of integrated circuit area so that the use of multiple metal source lines will increase the die area and thereby effectively increase the cost of manufacturing the cell array.

Flash memory systems are typically erased in bulk. That means that either all or a large part of the array are erased at the same time. By way of example, the entire array 32 of FIGS. 3A and 3B would be erased in a single operation. As indicated by Table 1, this can be accomplished by applying +12 volts to the common source lines SLM0–SLM3, grounding all of the word lines WLN0–WLN11 and floating all of the bit lines BL0–BL11.

There exist conventional memory arrays which provide the capability of erasing less than the entire array. This feature is particularly useful in many memory applications where it is desirable to retain some data stored in the memory while erasing and then reprogramming other data in the memory. The :capability of erasing less than the entire memory is typically accomplished by electrically isolating the source lines of individual blocks of the memory array. A particular block is erased by applying a high voltage, such as +12 volts (Table 1) to the source line associated with the block being erased. The word lines of the block to be erased are grounded and the bit lines of the block are left floating. As is known, the word lines and source lines of the erase blocks not being erased, the deselected erase blocks, are grounded so that the cells in the deselected erase blocks are not erased.

U.S. Pat. No. 5,126,808 entitle "Flash EEPROM ARRAY WITH PAGED ERASE ARCHITECTURE" discloses a few conventional techniques for providing the capability of erasing less than the entire array. Typically, the array includes segments or blocks having separate associated source lines. For relatively large erase blocks, it is conventional to use more than a single metal source line for each block so as to reduce the source line resistance. However, as previously noted, every additional metal source line will increase the area of the integrated circuit.

In order to reduce the number of source lines exiting an erase block, some conventional arrays utilize decoding circuitry located within the array itself. In that event, the decoding circuitry would be connected to receive various source lines as input and would provide a single output based upon the particular erase block being accessed. One disadvantage of this approach is that decode circuitry usually utilizes conventional transistors which are frequently difficult to implement in the interior of a flash cell array.

The present invention overcomes the above-described limitations of conventional flash cell arrays. The disclosed arrays are divided into separate erase blocks which permits less than the entire array to be erased. In addition, the overall source resistance of the disclosed array can be reduced to a level similar to that of an array which is not divided into separate erase blocks. This latter advantage is particularly applicable for relatively large arrays. Further, these advantages are achieved without greatly increasing the integrated circuit area. These and other advantages of the subject invention will be apparent to those skilled in the art upon a reading of the following Detailed Description of the Invention together with the drawings.

SUMMARY OF THE INVENTION

An arrangement of non-volatile memory cells, such as flash memory cells, is disclosed. The arrangement includes a plurality of erase blocks, with each of the blocks including an array of cells which can be erased separately from the cells of the remaining erase blocks.

The cells of each erase block are arranged into an array of rows and columns of cells. The cells located in one of the rows have their control gates connected to a common word line and the cells located in one of the columns have their drains connected to common bit lines. Preferably, the bit lines are common to all of the erase blocks. The sources of is the cells located in one of the erase blocks are connected together by a common source line structure. The source line structure includes non-metallic source lines, typically doped semiconductor lines which are generally parallel with the word lines. The doped semiconductor lines interconnect the sources of cells located in a common row. Typically, the cells are arranged so that cells in a pair of adjacent rows have common source regions so that one of the non-metallic source lines interconnects the sources of a pair of rows.

The source line structure of each of the erase blocks further includes a metallic source line positioned to interconnect the non-metallic source lines. The metallic source line are typically aligned in a parallel relationship with the bit lines of the erase block. Thus, the source regions of the cells in a particular erase block are interconnected by both the metallic and non-metallic source lines, thereby reducing the overall source line resistance while minimizing the area required by the structure.

The plurality of erase blocks each include first and second opposite block edges extending generally parallel with the cell rows. The plurality of erase blocks includes first and second ones of the erase blocks which are positioned relative to one another so that the first block edge of the first erase block is facing the second block edge of the second erase block. The metallic source line of the first erase block extends across the first edge of the first erase block, across the second edge of the second erase block and across the first edge of the first erase block. The metallic source line of the second erase block also extends over the first edge of the second erase block. Preferably, the metallic source lines of the first and second erase blocks are coupled to a common erase source decoder means which functions to control the metal source lines so that the erase blocks may be independently erased.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified cross-sectional view of a conventional flash memory cell.

FIG. 2A is a plan view of the conventional layout of a pair of flash memory cells.

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FIG. **2**B is a schematic diagram of the conventional pair of flash memory cells of FIG. **2**A.

FIG. **3**A is a plan view of the conventional layout of an array of flash memory cells.

FIG. **3**B is a schematic diagram of the memory cell array of FIG. **3**A.

FIG. **4** is a plan view of a layout of one embodiment of a flash memory cell array arrangement; in accordance with the present invention.

FIG. **5** is a schematic diagram of showing an equivalent circuit for one of the erase blocks of the FIG. **4** array arrangement.

FIG. **6** is a schematic diagram showing an equivalent circuit for determining the worst case source line resistance for an exemplary cell of the FIG. **4** array arrangement.

FIG. **7** is a schematic diagram of another embodiment of a flash memory cell array arrangement in accordance with the present invention.

FIG. **8** is a diagram illustrating the layout of a flash memory cell array arrangement in accordance with the present invention having eight separate erase blocks and depicting the location of the metal source connect lines and the metal source straps.

FIG. **9** is a schematic diagram of an erase source decoder circuit for use with an array having three erase blocks.

FIG. **10** is a schematic diagram of an alternative erase source decoder circuit.

FIG. **11** is a block diagram of a segmented flash array arrangement utilizing negative gate erase techniques.

FIG. **12** is a block diagram of an alternative embodiment blocked flash array arrangement utilizing negative gate erase techniques.

FIG. **13** is a schematic diagram of one of the X Decoder Stages used in the array arrangements of FIGS. **11** and **12**.

DETAILED DESCRIPTION OF THE INVENTION

Referring again to the drawings, FIG. **4** is a plan view of the layout of a portion of a flash cell array **34** in accordance with the present invention. Array **34** is comprised of cells **10** as depicted in FIG. **1**. A typical array would be much larger than exemplary array **34**. The array is divided into rows and columns. The cells **10** located in a particular row have their control gates all connected to an associated word line. The cells **10** located in a particular column have their drain regions connected to a particular bit line.

Array **34** includes three erase blocks (sometimes referred to as erase segments), Blocks **0**–**2**, each of which has separate source lines that permit each of the erase blocks to be separately erased. Each erase block includes four separate rows of flash cells **10**. By way of example, Blocks **0**–**2** includes four rows associated with word lines WL**0**–WL**3**, WL**4**–WL**7** and WL**8**–WL**11**, respectively. Further, all of the erase blocks include a set of twelve common columns of cells, namely, the twelve columns associated with bit lines BL**0**–BL**11**. Thus, each of the erase blocks can be viewed as including an array of flash cells. Bit lines BL**0**–BL**11** are common to all three erase blocks.

Array **34** is fabricated using a single metal layer process so as to simplify the fabrication process. As is well known, in a single metal layer process, it is not possible for two metal tracks to cross over one another. Typically, connections are made in one direction, such as the vertical direction, using metal tracks and in another direction, such as the horizontal direction, using non-metal tracks, such as doped semiconductor tracks.

The erase blocks each include a source line structure which is connected to all of the source regions of the cells located in the erase blocks. The source line structure includes a plurality of horizontal source lines which function to interconnect all of the source regions of cells located in one of the rows. The source line structure further includes vertical source lines and source straps which function to interconnect all of the source regions of cells located in one of the columns. The horizontal source lines are doped semiconductor source line segments intermediate two adjacent word lines. By way of example, Erase Block **2** includes a first horizontal doped semiconductor segment SD**1** intermediate word lines WL**10** and WL**11** and a second doped segment SD**2** intermediate word lines WL**8** and WL**9**. The two doped source line segments: SD**1** and SD**2** of Erase Block **2** extend across the entire width of the array and contact the common source regions of cells **10** on either side of the source line segments. Thus, for example, source line segment SD**1** of erase Block **2** is connected to the common source regions of cell **10**A and **10**B in the rows associated with word lines WL**11** and WL**10**, respectively, and to all of the other cells located in those rows. Doped source line segment SD**2** is connected to the common source regions in the cell **10** located in the two rows associated with word lines WL**8** and WL**9**.

The two doped source line segments SD**1** and SD**2** of Erase Block **2** are connected to a vertical metal source line SL**2** by way of contacts **36**A and **36**B. Metal source line SL**2** extends over Erase Blocks **0** and **1** and out of the array **34** so that the sources of the cells in Erase Block **2** can be connected to a source line decoder circuit (not depicted) external to the array **34**. Line SL**2** does not make contact with either erase Block **0** and **1**.

FIG. **5** is a schematic diagram showing the series resistances associated with the doped source lines SD**1** and SD**2** of Erase Block **2**. Source line SD**1** is represented by series-connected resistors R**1**A–R**15**A of equal value, with each resistor representing the source line resistance between adjacent cell columns. Similarly, resistors R**1**B–R**15**B represent the source line resistance of doped source lines SD**2**. In order to reduce the adverse effects of such resistance, the doped segments are periodically connected together a fixed number of bit lines by a vertical metal track. In the FIG. **4** embodiment, the doped segments SD**1** and SD**2** of erase Block **2** are connected together at one location by metal source line SL**2** intermediate bit lines BL**7** and BL**8**. The diffused segments SD**1** and SD**2** are further connected together at a location intermediate bit lines BL**3** and BL**4** by a pair of metal source straps **38**A and **38**B. Preferably, the doped source lines are connected together by either a metal source line or a metal source strap every N number of bit lines, with N being equal to four in the FIG. **4** embodiment. Although two straps may be used at one location to simplify fabrication, the two straps are electrically equivalent to a single strap so that the second strap may be deleted. Similarly, source strap **38**C is positioned adjacent metal source line SL**2** and thus also does not function to reduce the resistance, but is present to simplify the manufacturing process.

As can be seen in FIGS. **4** and **5**, each erase block is provided with multiple source lines. The metal source lines extend out from the array **34** and are electrically connected together and to a source line decoder circuit (not depicted) which permits a selected erase block to be erased. As can be seen in FIGS. **4** and **5**, Erase Block **2** includes the

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previously-described metal source line SL2 and an edge metal source line SL2E which is electrically connected to the two doped source lines SD1 and SD2 at the edge of array **34**. The edge metal source lines SLE2 is electrically connected to metal source line SL2 outside the array, typically near the source line decoder circuit.

Erase Block **1** (FIG. **4**) includes four rows of cells **10** associated with word lines WL4–WL7 and a pair of doped source lines SD3 and SD4. Lines SD3 and SD4 are connected together at one location intermediate bit lines BL3 and BL4 by a metal source line SL1. Metal source line SL1 extends over, but does not make electrical contact with, erase Block **0** and extends out of the array **34** for connection to the source line decoder circuitry external to the array **34**.

Erase Block **1** further includes a metal source strap **38**D located four bit lines over from metal source line SL1 and adjacent to bit line BL0. A further metal source strap **38**E is located four bit lines away in the opposite direction, intermediate bit lines BL7 and BL8. Another metal source strap **38**F is located another four bit lines away adjacent bit line BL11. Finally, a second metal source line SL1E, located at the edge of the array, functions to connected the doped source lines SD4 and SD5 together and to the source line decoder external to the array. Erase Block **0** includes a pair of doped source lines SD5 and SD6 which are associated with four rows of cells **10**. Each row has an associated word line WL0–WL3. Block **0** includes the same twelve columns as are present in Blocks **1** and **2** including the columns associated with bit lines BL0–BL11. A first metal source line SL0A is connected to the doped source line segments SD5 and SD6 at a location adjacent bit line BL0. A second metal source line SL0B located adjacent bit line SL0B is located at the other end of the array adjacent bit line BL11. Since the two metal bit lines SL0A and SL0B are located at the opposite ends of that array, it is not necessary to provide edge metal source lines, such as lines SL0E and SL1E used in connection with Blocks **0** and **1**. Erase Block **0** includes a first metal source strap **38**G located adjacent bit line BL3 and a second metal source line **38**H, both interconnecting the diffused source lines SD5 and SD6.

As previously noted, the metal lines of the array occupy a significant amount of chip area. Thus, in order to reduce the amount of area occupied by the metal source lines and the metal source straps, the two lines and straps are positioned in vertical alignment where possible. By way of example, metal source line SL1 and metal source strap **38**B are in alignment so that the horizontal area occupied is reduced. As a further example, metal source line SL0A and metal source strap **38**D are aligned so as to conserve space.

The FIG. **5** diagram of Erase Block **2** illustrates that no cell is more than two bit lines BLN away from either metal source line going to the outside (as SL2E or SL2) or a strap (as **38**A or **38**B). This limits the maximum source line resistance for a worst case cell **10**, such as cell **10**C, to less three time R, where R is equal to the value of any of the individual source line resistances R1A–R15A. The metal source straps **38** interconnecting the doped source lines SD1 and SD2 function to further reduce the maximum source line resistance. The metal source straps and the metal source lines are located such that they alternate a fixed number of bit lines, such as four bit lines in the FIG. **4** and **5** embodiment.

It can be seen from examination of the FIG. **5** array that cell **10**A will have a source line resistance not greater than the value of equivalent resistor R1A. Other cells **10** of the array will have a greater resistance, with the overall performance of the array being limited by the cell with the worst case resistance. FIG. **6** is schematic diagram of an equivalent circuit of a portion of erase Block **2** of the FIG. **4** and **5** array. Exemplary cell **10**C is shown since this cell is located such that it is among the cells which will have the largest source line resistance. Cell **10**C is disposed three equivalent resistances (R1A–R3A) away from metal source line SL2E hence the resistor value **3**R is shown connected between the cell and the source line. Cell **10**C is further disposed two equivalent resistances (R4A–R5A) away from metal source strap **38**A/**38**B hence the value **2**R shown connected to the cell. The strap **38**A/**38**B is shown connected to the metal source line SL2 by way of parallel resistors **5**R which represent equivalent resistors R6A–R10A and R6B–R10B, respectively. Finally, equivalent resistor SR representing resistors R1B–R5B, is shown connected metal source line SL2E and metal strap **38**A/**38**B. The two metal source lines SL2E and SL2 are connected together by a line **40** external to array **34**.

The total effective resistance between the source of cell **10**C and the source line SL for erase Block **2** can readily be calculated using simple arithmetic. The total effective resistance is equal to parallel combination of 3R|| (2R+5R/3). This give an effective approximate equivalent source resistance of 1.6R. If the metal source strap were deleted, the worst case cell would be cell **10**E, with an equivalent source resistance of approximately 2.5R.

FIG. **7** depicts a portion of another array **42** in accordance with the present invention. Only a corner portion of the array is depicted, including a portion of an Erase Block **0** and an Erase Block **1**. Erase Block **1** has one metal source line SLN depicted, with there being additional metal source lines also associated with Block **1**. Erase Block **0** has one metal source line SLN+1 depicted, with there being additional metal source lines associated with Block **1**. Those lines, which extend over Block **0** but do not make contact to Block **0**, are also not depicted in that portion of array **42** shown in FIG. **7**.

As was the case with the FIG. **4** embodiment, the doped source lines of each erase block are connected together every four bit lines by either a metal source line or by a metal source strap. By way of example, erase Block **0** has two associated doped source lines SDN and SDN+1 which are connected together by metal straps **38** and source lines SLN+1 every four bit lines.

In a typical flash cell array, cells located at the edge of the array are much more subject to processing variations than the cells not located at the edge. Because of this, it is common to refrain from using the cells at the array edge. Such cells, which extend around the perimeter of the array, are sometimes referred to as dummy cells. Array **42** is surrounded by dummy cells including the two columns of cells depicted in FIG. **7** at one edge of the array and two columns not depicted at the opposite edge of the array. The depicted columns are associated with bit lines BLX and BLY. In addition, array **42** includes two rows of dummy cells located at opposite edges of the array, including two rows not depicted and two rows shown in FIG. **7**. The depicted rows are associated with word lines WLX and WLY.

The dummy cells have doped source lines which interconnect the source regions of the dummy cells. The doped source lines include lines SDZ1–SDZ5 of the two dummy columns and lines SDX and SDY of the two dummy rows. Typically, the bit lines BLX and BLY are not accessed since the dummy cells are not supposed to be programmed. If the source lines of the dummy cells, such as source line SDZ5

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were to be connected to the source lines of the array, such as line SDN, the dummy cells would be erased when the array is erased. Since the dummy cells cannot be programmed but would otherwise be erased, the dummy cells are likely to become overerased so that they will conduct cell current even when the associated word line is grounded. The flow of current through an overerased cell will usually prevent proper operation of the array by creating a leakage path between the sources of different erase blocks. In order to ensure proper operation of the array of the present invention, the doped source lines of the dummy rows should not be in electrical contact with the doped source lines of the corresponding rows of the functional cells of the array. By way of example, diffused source line SDN of the rows associated with word lines WLN and WLN+1 does not extend to the diffused source line SDZ**5**.

In addition, the dummy cells located in the dummy rows would have a tendency to be erased when functional cells located in the same column are repetitively programmed. This phenomenon is sometimes referred to as bit line disturb where the dummy cells sharing a bit line with functioning cells would have some tendency to become overerased and thus become leaky. In order to reduce the likelihood of this occurring, the length of the source lines of the dummy cells are made short so as to minimize the possibility of a leakage path between bit lines. By way of example, source lines SDX and SDY of the two dummy rows are not connected so as to minimize any adverse effects of bit line disturb.

FIG. **8** show a further embodiment of an array **44** in accordance with the present invention showing essentially only the source line connections. Array **44** is comprised of eight erase Blocks 0–7, with each of the erase blocks having 128 rows of flash cells. Thus, array **44** has a total of 1024 rows of cells. Array **44** also has 1024 columns of cells so that the total array capacity is one Megabit. Each erase block can be considered an array of cells having 128 rows and 1024 columns. As can be seen from FIG. **8**, erase Blocks **0–3** and erase Blocks **4–7** are mirror images of one another.

Each of the erase blocks has several vertical metal source lines SLN which are electrically connected to all of the horizontal doped source lines (not depicted) of the erase block. The metal source lines SLN are provided a minimum of every 64 bit lines for each erase block, with the variation being due to the presence of edge metal bit lines. By way of example, Erase Block **4** will have 16 metal source lines, including lines SL**4**A; SL**4**B, SL**4**C . . . and SL**4**O. Each of the erase blocks also includes several metal source straps which electrically connect all of the diffused source lines of the erase block together. Erase Block **4** includes, for example, metal straps **46**A–**46**I. The metal source straps are internal to the erase blocks and do not extend past the edges of the associated erase block. There are typically three metal source straps intermediate adjacent metal source lines so that there is either a metal source strap or a metal source line located every 16 bit lines of each erase block.

The metal source lines SL**4**A–SL**4**O of Erase Block **4** extend over Erase Blocks **5–7** and away from array **44** where they are connected together to form a common source line for Erase Block **4**. The metal source lines from Block **4** extend over the other blocks along a path which is parallel with the bit lines of the block and orthogonal to the word lines. As will be explained, the metal source lines from Erase Block **4** (and the other erase blocks) are coupled to a source lined decoder circuit external to array **44** (not depicted).

Erase Block **5** includes metal source lines SL**5**A–SL**5** which are also spaced apart about every 64 bit lines. The metal source lines of Erase Block **5** extend over Erase Blocks **6** and **7** and out of array **44** where they are electrically connected to the source line decoder. Erase Block **5** also includes metal source straps **48**A–**48**I. The straps, like the straps of Block **4**, interconnect all of the horizontal doped source lines of Block **5**. There are typically three metal source straps intermediate adjacent metal source lines, with there being either a metal source line or a metal source strap every sixteen bit lines.

Erase Blocks **6** and **7** include metal source lines (SL**6**A–SL**6**P and SL7A–SL7P, respectively) and metal source straps (**50**A–**50**I and **52**A–**52**I, respectively) which are positioned in the same manner as the lines and straps in Blocks **4** and **5**. Note that the location of the metal source straps are selected so that they generally align with the metal source lines of adjacent erase blocks. By way of example, metal source straps **52**B, **50**B, and **46**B of Erase Blocks **7**, **6** and **4**, respectively, are generally aligned with metal source line SL**5**B of Block **5**. As a further example, metal source straps **46**C, **48**C and **50**D are generally aligned with metal source line SL7B.

As previously noted, Blocks **0–3** and Blocks **4–7** are arranged so that they are mirror images of one another. The metal source lines of Blocks **0–3** all extend toward to lower edge of array **44** and the metal source lines of Blocks **4–7** all extend in the opposite direction towards the top edge of the array. By dividing the erase blocks into two groups of blocks with each group of blocks having metal source lines extending in the opposite direction, a reduction in the amount of chip area occupied by the metal source lines is reduced. By way of example, metal source line SL**3**C of Erase Block **3** and metal source line SL**4**C of Erase Block **4** can be made to occupy the same vertical path on array **44** since they extend in opposite directions.

FIG. **9** is a schematic diagram of an exemplary section of one embodiment of a source line decoder circuit **54** which can be used in connection with an array having a total of three erase blocks. Circuit **54** includes a set of N channel source line decode transistors **56**, **58** and **60** connected to the respective source lines of the array. The function of the decode transistors is to connect the source lines coming from a common selected erase block of the array to the same desired potential/condition and to connect the source lines from the deselected erase blocks to a desired potential/condition.

By way of example, the source lines from Erase Block **0**, including depicted lines SL**0**A and SL**0**B are connected to decode transistors **56**A and **56**B, respectively. Transistors **56**A and **56**B, and other decode transistors not depicted which are connected to any additional source lines of Erase Block **0** and have their gates connected to a common line which carries control signal S_0. Source lines from Erase Block **1**, including depicted lines SL**1**A and SL**1**B, are connected to decode transistors **58**A and **58**B, respectively. Transistors **58**A and **58**B, and any other transistors not depicted which are connected to any additional source lines of Erase Block **1**, have their gates connected to a common line which carries control signal S_1. Erase Block **2** has one source line SL**2**A depicted in FIG. **9** which is connected to transistor **60**. A control line carrying signal S_2 is connected to the gate of transistors **60** and to the gate of any additional decode transistors which receive other source lines of Erase Block **2**. All of the transistors of source decoder circuit **54** controlled by control signals S_0, S_1 and S_2 have their source electrodes connected to a common Global Source line.

Each of the source lines of Erase Blocks **0**, **1** and **2** are also connected to separate N channel transistors **64**, **66** and **68**

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which function to selectively connect the source lines to a common Deselected Source Bus. As will be explained, the Deselected Source Bus may be set to some voltage or may be grounded. By way of example, transistors **64**A and **64**B are connected to source lines SL**0**A and SL**0**B of Erase Block **0**. The gates of transistors **64**A and **64**B are controlled by signal $\overline{S}_0$ which is the complement of signal S_0. Source lines SL**1**A and SL**1**B of Erase Block **1** are connected to transistors **66**A and **66**B, respectively, with transistors **66**A and **66**B having their gates connected to a common line which carries signal $\overline{S}_1$, the complement of signal S_1. Transistor **68** is controlled by signal $\overline{S}_2$, the complement of signal S_2, and is connected to source line SL**2**A of Erase Block **2**.

Table 2 below shows the manner in which the source decoder circuit **54** is controlled in basic memory operations. In a memory read operation, all of the source lines of all of the erase blocks are to be connected to ground. Thus, as can be seen from

TABLE 2

ERASE SOURCE DECODER

SIGNAL	READ (BLOCK 0)	PROGRAM (BLOCK 0)	ERASE (BLOCK 0)
S_0	+5 volts	+5 volts	+12 volts
S_1	+5 volts	+5 volts	0 volts
S_2	+5 volts	+5 volts	0 volts
$\overline{S}_0$	0 volts	0 volts	0 volts
$\overline{S}_1$	0 volts	0 volts	+12 volts
$\overline{S}_2$	0 volts	0 volts	+12 volts
GLOBAL SOURCE	0 volts	0 volts	+10 volts
SL0	0 volts	0 volts	+10 volts
SL1	0 volts	0 volts	0 volts
SL2	0 volts	0 volts	0 volts

Table 2, signals S_0, S_1 and S_2 are made active (connected to voltage V_{cc}) so that transistors **56**A, **56**B, **58**A, **56**B and **60** are all rendered conductive. The Global Source signal is brought to ground level so that all of the source lines of the array (SL**0**, SL**1** and SL**2**) are at ground level.

Table 3 below shows the conditions for the other portions of the array, including word lines and bit lines, for carrying out memory read, program and erase operations. As can be seen from Tables 2 and 3, and as noted above, in memory read operations, the selected source line (the source lines of the erase block containing the cells to be read) are grounded as are the deselected source lines (the source lines of the other erase blocks). This is accomplished by setting signals **S0**, **S1** and **S2** to +5 volts which causes-transistors **56**A, **58**A, **60**, **56**B and **58**A to be conductive thereby connecting all three source lines SL**0**, SL**1** and SL**2** to the Global Source line. The Global Source line is at ground potential so that all of the source lines are grounded. Signals $\overline{S}$**0**, $\overline{S}$**1** and $\overline{S}$**2** are all at ground potential during read operations so that transistors **64**A, **66**A, **68**, **64**B and **66**B are off.

TABLE 3

FUNCTION	READ	PROGRAM	ERASE
SELECTED WORD LINE	+5 volts	+11 volts	N/A
DESELECTED WORD LINE SELECTED BLOCK	0 volts	0 volts	0 volts
DESELECTED BIT LINE	+1 volt	Data = 0 +6 volts Data = 1 0 volts	N/A
DESELECTED BIT LINE	float	float	float
SELECTED SOURCE LINE	0 volts	0 volts	+10 volts
DESELECTED SOURCE LINE	0 volts	0 volts	0 volts

In addition, the wore line associated with the cells being read (the selected word line) is connected to +5 volts and all of the other word lines in the array are grounded. The bit lines of the cells being read (eight cells if the memory word length is eight bits) are connected to a small positive voltage such as +1 volt. All other bit lines of the array are left floating, as can also be seen from Table 3. This combination of conditions will cause the selected cells to either conduct or not conduct current based upon their programmed state.

In order to program a cell (or cells), a relatively large positive voltage of +11 volts is applied to the word line associated with the cell being programmed. All of the other word lines of the array, including those in the same erase block, are grounded. The bit line of the cell to be programmed is connected to +6 volts. If the cell is to be left in the erased state, the bit line is connected to +1 volt. As shown in Table 3, the deselected bit lines are all left floating during programming operations.

As previously noted, an important feature of the present invention is to provide an array which contains separate erase blocks which can be independently erased. Table 2, above, shows the conditions of the erase source decoder when an exemplary erase block, Erase Block **0**, is being erased. The Global Source line is set to +10 volts. In addition, signal S_0 is set to +12 volts so that transistors **56**A and **56**B have sufficient gate voltage to apply the +10 volts present on the Global Source line to the source lines SL**0**A and SL**0**B associated with the selected erase block, Erase Block 0. The deselected source lines, those associated with the other erase blocks, are all grounded by setting signals $\overline{S}_1$ and $\overline{S}_2$ to +12 volts thereby turning on transistors **66**A, **68**, **66**B. In addition, the Deselected Source Bus is grounded so that the deselected source lines SL**1**A, SL**1**B and SL**2**A are all at ground potential.

Table 3, above, shows the conditions of the remainder of the array in erase operations. All of the word lines, including those of the erase block being erased and the other erase blocks, are grounded. In addition, all of the bit lines of the array are left floating. Under these conditions, all of the cells in Erase Block **0** will be erased.

Table 3 illustrates one set of conditions for reading, programming and erasing a flash array. In that example, a cell is erased by connecting the selected source line to +10 volts, the selected word line to ground and floating the selected bit line. An alternative erase technique can be used wherein a negative voltage is applied to the word line of the cells being erased. That voltage is typically −10 volts. The bit line is left floating and a relatively small voltage V_A, such as +5 volts, is applied to the source line of the erase block. As will be explained, the deselected source lines are left

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floating rather than being grounded as is done in conventional arrays having separate erase blocks. By floating the deselected source lines, certain defects can exist in one erase block which do not interfere with the operation of the remaining erase blocks.

FIG. **10** depicts an alternative erase source decoder. Table 4 below shows the various signals used in

TABLE 4

ERASE SOURCE DECODER

SIGNAL	READ (BLOCK 0)	PROGRAM (BLOCK 0)	ERASE (BLOCK 0)
S_0	+5 volts	+11 volts	+11 volts
S_1	0 volts	0 volts	0 volts
S_2	0 volts	0 volts	0 volts
GLOBAL SOURCE	0 volts	0 volts	V_A
SL0	float	float	V_A
SL1	float	float	float
SL2	0 volts	0 volts	float

the FIG. **10** decoder, when the decoder is used in connection with an array utilizing negative gate erase. Referring to FIG. **10**, each erase block has a separate source line SL**0**, SL**1**, SL**2** connected to a separate transistors **70**A, **70**B and **70**C, respectively of the decoder. Transistors **70**A, **70**B and **70**C are controlled by signals S_0, S_1 and S_2, respectively in the event the erase blocks have more than one source line, additional decode transistors are included. Thus, for example, if Erase Block **0** were to have additional source lines, they would each be connected to a transistor controlled by signal S_0.

As can be seen from Table 4, when cells in Erase Block **0** are to be read, signal S_0 is set to +5 volts thereby turning on transistor **70**A (and any other transistors that may be connected to a source line of Erase Block **0**). Signals S_1 and S_2 remain at ground level so that the transistors connected to the remaining erase blocks, including transistors **70**B and **70**A, are left off. Conducting transistor **70**A will connect the source line SLO of Erase Block **0** to the Global Source line which is, in turn, connected to ground. A positive voltage of +5 volts is connected to the word line associated with the cells being read and the bit lines are connected to a small positive voltage of typically +1 volts. This will cause current to flow or not to flow in the cells being read depending upon whether the cells are in an erased or programmed state. Table 3, above, shows the conditions for the deselected word lines and bit lines during read operations.

In a programming operation where cells in Erase Block **0** are to be programmed, Table 4 indicates that transistor **70**A is turned on and transistors **70**B and **70**C are left off. The Global Source line is set to ground potential so that transistor **70**A will cause the source line SL**0** to be at ground potential. The deselected source lines SL**1** and SL**2** will be floating. The word line associated with the cells being programmed is set to a relatively large positive voltage of typically +11 volts. Since this voltage (+11 volts) is generated for programming, the voltage is available for generating signal S_0 used to on transistor **70**A. Signal S_0 could also be +5 volts since transistor **70**A is switching at a voltage near ground potential. Further, the bit line associated with the cells to be programmed will be set to a medium level voltage such as +6 volts. If the cell is to be left in the erased state, the associated bit line is grounded. This combination of conditions will permit the selected cells of Erase Block **0** to be programmed. Continuing, Table 4 indicates that all the cells of Erase Block **0** are erased by setting signals S_0, S_1 and S_2 such that transistor **70**A of the FIG. **10** erase decoder is made conductive and the remaining transistors **70**B and **70**A are off. The Global Source line is set to a relatively low positive voltage V_A which is typically approximately +5 volts or some other value which will not be so large as to result in cell voltage break down. Thus, source line SLO of Erase Block **0** will be at voltage V_A and the source lines of the remaining erase blocks, lines SL**1** and SL**2** will be floating. The word lines of Erase Block **0** are all set to a relatively large negative voltage, such as −10 volts, and the bit lines of the array are all left floating. This will result in all of the cells of Erase Block **0** being erased by way of the previously-described negative gate erase technique.

It is possible that a failure of a cell in one erase block will adversely affect operation of the remaining erase blocks. Under certain conditions, a flash cell will conduct current when it should be non-conducting. By way of example, if a cell has been over erased, the cell will have a negative threshold voltage so that the cell will conduct even when the gate-source voltage is 0 volts. Other conditions may occur which will cause a cell to be "leaky" and conduct current when the cell should be non-conductive. When a cell of a deselected erase block is improperly conducting current, the cell has a tendency to clamp the bit line voltage to the source voltage. This can cause the bit line voltage to approach ground potential should the source lines of the deselected erase blocks be set to ground potential as is illustrated in Tables 2 and 3, above. Since the bit lines are common to all of the erase blocks in an array, a defective cell in one block will have a tendency to interfere with the reading, erasure and programming of the other blocks. By floating the source lines of deselected erase blocks during program or read operations, as shown in Table 4, the adverse affects of a leaky or over erased cell in the deselected blocks on the cells of selected erase blocks will be greatly reduced.

FIG. **11** depicts a flash cell array arrangement adapted to utilize negative gate erase techniques. Exemplary Erase Blocks **0**–**1** are depicted, with there being a total of eight erase blocks, including Erase Blocks **2**–**7** which are not shown. Each erase block has sixty-four word lines WL, a set of bit lines BL common to all of the erase blocks and separate source lines. The word lines are grouped in eights, with each group of eight being connected to a separate X Decoder Stage **72**. Thus, for example, X Decoder Stage **72**A is connected to word lines WL**0**–WL**7**. There are a total of **512** word lines WL**0**–WL**511**, with word lines WL**0**–WL**63** being associated with Erase Block **0** and word lines WL**64**–WL**127** being associated with Erase Block **1** and the remaining word lines WL**128**–WL**511** being associated with the remaining six erase blocks that are not depicted.

Each of the word lines WL**0**–WL**511** also has a separate respective P channel erase transistor T**0**–T**511** connected to it, with the transistors associated with one of the erase blocks being controlled by a common control signal. Thus, erase transistors T**0**–T**63** of Erase Block **0** have their gates connected to a line that carries control signal G**0** and erase transistors T**64**–T**127** of Erase Block **1** have their gates connected to a common line that carries control signal G**1**. In addition, all of the erase transistors associated with an erase block have their sources connected to a common voltage line. Thus, for example, erase transistors T**0**–T**63** are all have their sources connected to a common line that carries a voltage V_0.

The details of the X Decoder Stages **72** of FIG. **11** are shown in FIG. **13**. As will be explained in greater detail, the X Decoder Stages **72** provide outputs which are either at a positive voltage equal to the X Decoder Stage **72** supply

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voltage V_P, ground potential or a high impedance (at least more than 10k Ω). The high impedance state of the X Decoder Stages **72** is used when the erase transistors **T0**–**T511** function to apply a negative voltage to the word lines of an erase block during an erase operation, as will be explained in greater detail.

The conditions for carrying out read, program and erase operations on the FIG. **11** array arrangement are set forth in Table 5, below. Erase Block **0** is

TABLE 5

FUNCTION	READ	PROGRAM	ERASE
G_0	+5 volts	+11 volts	−12 volts
V_0	+5 volts	+11 volts	−10 volts
G_1	+5 volts	+11 volts	0 volts
V_1	+5 volts	+11 volts	0 volts
X-DECODER SUPPLY V_P	+5 volts	+11 volts	0 volts
WL-BLOCK 0 (SELECTED BLOCK)	selected +5 volts deselected 0 volts	selected +11 volts deselected 0 volts	−10 volts
WL-BLOCK 1 (DESELECTED BLOCKS)	0 volts	0 volts	0 − V_T
SL0	0 volts	0 volts	V_A
SL1 (DESELECTED SOURCES)	0 volts float	0 volts float	V_B float
V_{NISO}	−2 volts	−2 volts	0 volts

the selected erase block in the Table 5 example. As can be seen from Table 5, if a memory read operation is to occur in Erase Block **0**, all of the control signals connected to the gates of the P channel erase transistors **T0**–**T127** (and the erase transistors **T128**–**T511** not depicted) are connected to a positive voltage of +5 volts. That includes signal G_0 associated with the selected Erase Block **0** and signal G_1 associated with the deselected Erase Block **1**. In addition, the voltages V_0 and V_1 applied to the drains of the P channel erase transistors are all set to +5 volts. The positive voltages applied to the erase transistors causes the transistors to be non-conductive. Accordingly, the state of the word lines will be determined by the X Decoder Stages **72** during memory read operations.

Referring again to FIG. **13**, further details of the X Decoder Stage **72** will now be described. The entire X Decoder, which is not depicted, functions to receive nine of the sixteen address bits for the array and decodes those address bit so as to select one of the 512 word lines in memory read and programming operations. The remaining address bits for the memory are used by a Y Decoder (not depicted) to select the appropriate bit lines. X Decoder Stages **72** represent the output portion of the X Decoder for the array. Each X Decoder stage **72** is associated with eight word lines so that there will be a total of sixty-four X Decoder Stages **72**, with eight X Decoder Stages **72** being associated with each of the eight erase blocks. The exemplary FIG. **13** circuitry for X Decoder Stage **72**A is associated with eight word lines WL**0**–WL**7** of Erase Block 0.

In order to select one of the **512** word lines, each of the X Decoder Stages **72** receives a total of twenty-four predecode signals. These predecode signals are developed by predecoding circuitry (not depicted) which receives the nine address bits supplied to the X Decoder and converts the nine address bits to twenty-four predecode signals, including signals X_{A0}–X_{A7}, X_{B0}–X_{B7} and X_{CH0}–X_{CH7}. Signals X_{A0}–X_{A7} and X_{B0}–X_{B7} are used in combinations of two to select one of the sixty-four X Decoder Stages **72**. Signals X_{CH0}–X_{CH7} are provided to each of the sixty-four X Decode Stages **72** to select one of the eight word lines associated with each stage. By way of example, X

Decode Stage **72**A of FIG. **13** receives predecode signals X_{A0} and X_{B0} which function to select that stage from the sixty-four stages. Stage **72**A also receives predecode signals X_{CH0}–X_{CH7} which are used to select one of the eight word lines WL**0**–WL**7** associated with Stage **72**A.

The construction and operation of exemplary X Decode Stage **72**A of FIG. **13** will now be described since such description is helpful in understanding Table 5. Predecode signals X_{A0} and X_{B0} are connected to the inputs of a NAND gate **74**, the output of which is connected to a level shifting pass transistor **76** which will pass any voltage having a magnitude which is below the supply voltage V_{CC} connected to its gate. Pass transistor **76** is, in turn, connected to a total of eight additional pass transistors, including N channel transistor **78**A associated with decode circuitry for word line WL**0** and including N channel transistor **78**B associated with decode circuitry for word line WL**7**.

Transistor **78**A has its gate connected to receive predecode signal X_{CH0}, with predecode signal X_{CH0} also being connected to the gate of a P channel transistor **80**A. Transistor **80**A is connected between transistor **78**A and the X Decoder supply voltage V_P. Transistors **78**A and **80**A are connected to a common node **79**A which is near ground potential when predecode signals X_{A0}, X_{B0} and X_{CH0} are all at a high level, otherwise node **79**A is at a high level. Node **79**A is connected to the common gate connection of a P channel transistor **84**A and an N channel transistor **88**A. These transistors form an inverting stage, the output of which is connected to word line WL**0**. Transistor **84**A is connected between the X Decoder supply voltage V_P and the inverting stage output and transistor **88**A is connected between the output, by way of a P channel transistor **86**A, and the circuit common. As will be explained, transistor **86**A functions to protect N channel transistor **88**A from the negative voltage which is present on the word line WL**0** during erase operations.

In addition to being-connected to word line WL**0**, the output of the inverting stage is connected to the gate of a feedback P channel transistor **82**A, with transistor **82**A providing positive feedback which pulls the input of the inverting stage, node **79**A, towards supply voltage V_P when the output of the inverting stage, WL**0**, goes low. This ensures that node **79**A will be pulled up to a sufficiently high voltage to turn off P channel transistor **84**A.

The remaining seven sections (only the last section is depicted) of X Decoder Stage **72**A for driving word lines WL**1**–WL**7** are also connected to the output of NAND gate **74** and pass transistor **76**. Otherwise, the construction of the sections is the same. The seven sections each receive respective ones of predecode signals X_{CH1}–X_{CH7}, so that one of the eight word lines WL**0**–WL**7** can be selected.

Returning to the description of a read operation (Table 5 and FIG. **11**) in connection with Erase Block **0**, the signals G_0–G_7 applied to the gates of all of the P channel erase transistors **T0**–**T127** (and those not depicted) are set to +5 volts. Thus, the transistors will be non-conductive. In addition, the X Decoder supply voltage V_P is set to +5 volts. A read address is decoded causing predetermined predecode signals to become active. Assuming, for example, that a cell associated with word line WL**7** is to be read, the predecode signals X_{A0} and X_{B0} will go high thereby selecting X Decoder Stage **72**A. This will cause the output of pass transistor **76** to go low (FIG. **13**). In addition, predecode signal X_{CH7} will go high thereby turning on pass transistor

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78B and causing node 79B to go low. The remaining predecode signals, X_{CH0}–X_{CH6} will remain low. Transistor 84B will turn on so as to pull up selected word line WL7 to voltage V_P, which is set to +5 volts. Note that voltage V_{NISO} is set to −2 volts (Table 5) thereby causing P channel transistor 86B to be conductive. However, since transistor 88B is off, the word line WL7 voltage will still be +5 volts.

As indicated in Table 5, the deselected word lines in the selected Erase Block 0 are set to ground potential. This is accomplished by the nine bit address causing the X Decoder to set the predecode signals X_{CH0}–X_{CH6} to a low value, as previously noted. Thus, for example, signal X_{CH0} will cause transistor 78A to turn off thereby isolating node 79A from the low output of NAND gate 74. Signal X_{CH0} will also cause transistor 78A to become conductive and pull node 79A up to voltage V_{CC} less the threshold voltage of transistor 79A. This will cause transistor 88A to become conductive, thereby causing the voltage on word line WL0 to drop. This, in turn, will cause transistor 82A to turn on thereby pulling node 79A up further to voltage V_P.

As previously noted, voltage V_{NISO} is set to −2 volts so that transistor 86A will also be conductive. Accordingly, transistors 86A and 86B will both be conductive and will pull word line WL0 down to ground potential as will the corresponding transistors associated with deselected word lines WL1–WL6 of Erase Block 0.

With respect to the deselected word lines of the remaining erase blocks, Table 5 indicates that these word lines are also set to ground potential. For all of these deselected erase blocks, the predecode signals XA and XB will such that the output of the corresponding NAND gate 74 output will be at a high level. For those deselected word lines where predecode signal X_{CH7} is used, that predecode will be at a high level in the present example so that transistor 78 will be on thereby connecting the high output of NAND gate 74 to node 79. For those selected word lines where predecode signals X_{CH0}–X_{CH6} are used, those predecodes will be at a low level. This will cause the associated transistor 78 to be off thereby isolating node 79 from the output of the NAND gate 74. In addition, associated transistor 80 will be turned on by the low level predecode so that node 79 will be pulled up to voltage V_P. In either case, a high voltage at node 79 will cause the associated word line to be at ground potential.

As indicated by Table 5, in read operations, the selected source line, SL0 for Erase Block 0, is grounded. The source lines of the remaining Erase Blocks 1–7, including source line SL1, can also be grounded as shown in Table 5. However, preferably, the deselected source lines are left floating, as also shown in Table 5. This can be accomplished, for example, using the source decoder circuit of FIG. 9. With the array configured as described, a selected cell (or group of cells) associated with a word line (such as line WL7) of Erase Block 0 can be read.

Table 5 also shows the conditions for programming a cell or group of cells of the FIG. 11 array arrangement. Again, all of the P channel erase transistors T0–T511 are turned off since control signals G_0 and G_1 (and signals G_2–G_7 not depicted) are all set to a positive voltage (+11 volts). The X Decoder 72 supply voltage V_P is set to +11 volts and the decoding circuitry is caused to apply this voltage to the selected word line based upon the address being used in the programming operation. Thus, for example, if word line WL7 is the selected word line, predecode signals X_{A0}, X_{B0} and X_{CH7} (FIG. 13) are all at a high level so that transistor 84B will pull word line WL7 up to voltage V_P set to +11 volts.

The deselected word lines WL0–WL6 of selected Erase Block 0 are set to ground potential in the programming operation since the predecode signals X_{CH0}–X_{CH6} associated with the deselected word lines will be at a low level. Voltage V_{NISO} is set to −2 volts according to Table 5 therefore both transistors 86B and 88B will be turned on connecting these deselected word lines to ground as was the case during read operations. In addition, the word lines of the deselected erase blocks will be at ground potential for the same reasons previously set forth in connection with the description of an exemplary read operation. However, it is again preferable chat the source line of the deselected erase blocks be left floating in programming operations as is the case of these source lines during read operations.

In erase operation, a single erase block of the array may be erased as previously described. As can be seen in Table 5, if Erase Block 0 is the selected block to be erased, signal G_0 is set to −2 volts thereby turning on erase transistors T0–T63 (FIG. 12). In addition, voltage V_0 is set to −10 volts so that all sixty-four word lines of Erase Block 0 are connected to −10 volts by the associated erase transistor T0–T63.

As can also be seen from Table 5, all sixty-four of the X Decoder Stages 72 of the array have their common supply voltage V_P set to ground potential. In addition, voltage V_{NISO} is set to ground potential so that the P channel transistor 86 (FIG. 13) in each of the X Decoder Stages 72 is turned off thereby isolating the N channel transistors 88 from the negative voltage which is applied to the word lines of Selected Erase Block 0.

The erase transistors T64–T511 of the deselected erase blocks are all turned off since the voltage applied to the gates, including G_1, is at ground potential. In addition, the associated X Decoder Stage 72 output is isolated from the word lines so that the word lines of the deselected erase blocks will be at a high impedance level. The deselected word lines will assume a voltage ranging from ground potential to the threshold voltage V_T of the P channel transistor 84 located in the associated X Decoder Stage 72, as indicated in Table 5. This threshold voltage is typically +1 volt.

The source line of the selected Erase Block 0, source line SL0, is set to voltage V_A which is typically +5 volts. By way of example, the Global Source line of the FIG. 9 source decoder circuit will be set to voltage V_A and signal S0 is made to turn on transistors 56A and 56B. In addition, the voltage of the source lines associated with the deselected erase blocks, such as source line SL1, are set to a voltage V_B. This is accomplished by setting the Deselected Source Bus of the FIG. 9 decoder circuit to voltage V_B and turning on the transistors 66A, 66B and 68 associated with the deselected source lines. Voltage V_B is selected to be intermediate threshold voltage V_T and voltage V_A applied to the selected source line. Thus, if threshold voltage V_T is +1 volt and voltage V_A is +5 volts, V_B may be set to +3 volts. If voltage V_B is set too high, there will be an increased tendency for the cells of the deselected erase blocks to be slightly erased each time one of the other erase blocks is erased. This phenomena is sometimes referred to as source erase disturb. If, on the other hand, voltage V_B is too low, there will be a tendency to turn on the deselected flash cells, or to cause them to leak, since the control gate voltage of the flash cells will typically be at voltage V_T due to the previously described influence of the associated X Decoder Stage 72. These conditions will cause the selected Erase Block 0 to become erased. As also indicated by Table 5, the deselected source lines can also be placed in a floating state in erase operations.

FIG. 12 shows an alternative to the FIG. 11 flash array arrangement, with similar elements having the same numeri-

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cal designation. This array arrangement also utilizes negative gate erase during erase operations. However, rather than having a separate control signal G_0–G_7 for each of the eight Erase Blocks **0**–**7**, there is single control signal G common to all eight blocks. Other aspects of the FIG. **12** embodiment are the same as that of FIG. **11** with the exception of the differences noted in the following description. Thus, the FIG. **12** array arrangement is somewhat simpler to implement than is the FIG. **11** embodiment.

Table 6 shows the conditions for reading, programming and erasing the FIG. **12** array arrangement. In read operations, signal G is set to +5 volts so that all of the erase transistors T**0**–T**511** are turned off. Similarly, in program operations, signal G is set to +11 volts so that all of the erase transistors are turned off. The X Decoders stages **72** used in the FIG. **12** embodiment are the same used in the previously described FIG. **11** embodiment. Since the erase transistors T**0**–T**511** are in the same corresponding disabled state as in the FIG. **11** embodiment, the conditions created by the X Decoder Stages **72** in read and program operations are the same and need not be further described.

In erase operations, assume that Erase Block **0** is to

TABLE 6

FUNCTION	READ	PROGRAM	ERASE
G	+5 volts	+11 volts	−12 volts
V_0	+5 volts	+11 volts	−10 volts
V_1	+5 volts	+11 volts	0 volts
X-DECODER SUPPLY V_P	+5 volts	+11 volts	0 volts
WL-BLOCK 0	selected	selected	
(SELECTED	+5 volts	+11 volts	−10 volts
BLOCK)	deselected	deselected	
	0 volts	0 volts	
WL-BLOCK 1 (DESELECTED BLOCKS)	0 volts	0 volts	0 volts
SL0	0 volts	0 volts	V_A
SL1	0 volts	0 volts	V_B
(DESELECTED SOURCES)	float	float	float
V_{NISO}	−2 volts	−2 volts	0 volts

be erased. Common signal G is set to −12 volts and voltage V_0 associated with Erase Block **0** is set to −10 volts. Thus, erase transistors T**0**–T**63** are turned on thereby connecting all of the word lines WL**0**–WL**63** of Erase Block **0** to −10 volts. The deselected voltages, including V_1 are all set to ground potential. Thus, the remaining erase transistors T**63**–T**511** are all turned on thereby connecting all of the deselected word lines WL**64**–WL**511** to ground.

As also indicated by Table 6, the selected source line SL**0** is set to voltage V_A which, as previously noted, is typically +5 volts. The deselected source lines, including source line S**1**, are connected to voltage V_B which, as also previously noted, is set to +3 volts, a voltage selected to be greater than the threshold voltage of the X Decoder Stage **72** P channel transistor **86** (FIG. **13**) and lower than voltage V_A. Again, voltage V_{NISO} is set to 0 volts thereby turning off transistor **86** of the X Decoder Stages **72** and isolating the N channel transistors **88** from the negative voltage applied to the word lines WL**0**–WL**63** of Erase Block **0**. Although not set forth in Table 6, the bit lines common to all of the erase blocks are left floating. This combination of conditions will cause the cells of Erase Block **0** to be erased.

As indicated by Table 6, in erase operations, the deselected source lines can also be left floating. This approach is preferred since, as previously noted, a defect is a deselected erase block will not adversely affect the operation of the selected erase block.

Thus, a novel flash cell array arrangement divided into array segments having separate source lines has been disclosed. Although a various embodiments of the subject invention have been described in some detail, it is to be understood that certain changes can be made by those skilled in the art without departing from the spirit and scope of the invention as defined by the appended claims.

I claim:

1. A flash memory device comprising:

an array of memory cell floating gate transistors arranged in rows and columns;

horizontal semiconductor source lines coupled to sources of memory cell transistors located in the rows of the array;

vertical metal source lines coupled to the horizontal semiconductor source lines;

vertical metal source line straps coupled to the semiconductor source lines, the metal source lines and the metal source line straps are spaced horizontally along the semiconductor source lines to reduce a total resistance between a memory cell transistor and a vertical metal source line; and

a source line decoder circuit coupled to the vertical metal source lines for selectively coupling the vertical metal source lines of a first block of the array to a global source line, the source line decoder circuit also selectively decouples vertical metal source lines in a second block of the memory array from a voltage supply when the second block is not being accessed.

2. A flash memory device comprising:

an array of memory cells arranged in erasable blocks, each block having rows and columns, each memory cell comprising a floating gate transistor having a source, drain and gate;

a plurality of semiconductor source lines coupled to the sources of non-volatile memory cells located in a plurality of the rows of an erasable block;

a plurality of metal source lines coupled to the plurality of semiconductor source lines;

a plurality of metal source line straps coupled to the plurality of semiconductor source lines, the plurality of metal source lines and the plurality of metal source line straps are spaced along the plurality of semiconductor source lines; and

a source line decoder circuit coupled to the plurality of source lines for selectively coupling the plurality of source lines of an erasable block of the array to a global source line, the source line decoder circuit also selectively decouples the plurality of source lines in erasable blocks of the memory array from a voltage supply when those erasable blocks are not being accessed.

3. A flash memory device comprising:

a single metal interconnect layer;

an array of memory cell floating gate transistors arranged in rows and columns;

horizontal semiconductor source lines coupled to sources of memory cell transistors located in the rows of the array, the semiconductor source lines have a resistance R per unit length;

vertical metal source lines formed in the single metal interconnect layer and coupled to the horizontal semiconductor source lines;

vertical metal source line straps formed in the single metal interconnect layer and coupled to the semiconductor

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source lines, the metal source line straps are spaced horizontally along the semiconductor source lines to reduce a total resistance between a memory cell transistor and a vertical metal source line; and

a source line decoder circuit coupled to the vertical metal source lines for selectively coupling the vertical metal source lines of a first block of the array to a global source line, the source line decoder circuit also selectively decouples vertical metal source lines in a second block of the memory array from a voltage supply when the second block is not being accessed.

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