

Silicon Processing

for the VLSI Era
Volume 1—Process Technology

S. Wolf and R.N. Tauber



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**SILICON PROCESSING
FOR
THE VLSI ERA
VOLUME 1:
PROCESS TECHNOLOGY**

SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

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To my wife, Carrol Ann,
and my children, Jennifer Laura and Stanley Charles Ross

Stanley Wolf

To my wife, Barbara

Richard N. Tauber

PREFACE

SILICON PROCESSING FOR THE VLSI ERA is a text designed to provide a comprehensive and up-to-date treatment of this important and rapidly changing field. The text will consist of two volumes of which this book is the first, subtitled, *Process Technology*. Volume 2, subtitled, *Manufacturing Technology* is scheduled for publication in 1988. In this first volume, the individual processes utilized in the fabrication of silicon VLSI circuits are covered in depth (e.g. epitaxial growth, chemical vapor and physical vapor deposition of amorphous and polycrystalline films, thermal oxidation of silicon, diffusion, ion implantation, microlithography, and etching processes). In addition, chapters are also provided on technical subjects that are common to many of the individual processes, such as vacuum technology, properties of thin films, material characterization for VLSI, and the structured design of experiments for process optimization. The topics covered in the book are listed in more detail in the Table of Contents. In Volume 2, *Manufacturing Technology*, other issues related to VLSI fabrication such as process integration, process simulation, manufacturing yield, VLSI manufacturing facilities, assembly, packaging, and testing will be covered.

The purpose of writing this text was to provide professionals involved in the microelectronics industry with a single source that offers a complete overview of the technology associated with the manufacture of silicon integrated circuits. Other texts on the subject are available only in the form of specialized books (i.e. that treat just a small subset of all of the processes), or in the form of edited volumes (i.e. books in which a group of authors each contributes a small portion of the contents). Such edited volumes typically suffer from a lack of unity in the presented material from chapter-to-chapter, as well as an unevenness in writing style and level of presentation. In addition, in multi-disciplinary fields, such as microelectronic fabrication, it is difficult for most readers to follow technical arguments in such books, especially if the information is presented without defining each technical "buzzword" as it is first introduced. In our book we hope to overcome such drawbacks by treating the subject of VLSI fabrication from a unified and more pedagogical viewpoint, and by being careful to define technical terms when they are first used. The result is intended to be a *user friendly* book for workers who have come to the semiconductor industry after having been trained in but one of the many traditional technical disciplines.

An important technical breakthrough has occurred in publishing, that the authors also felt could be exploited in creating a unique book on silicon processing. That is, revolutionary electronic publishing techniques have recently become available, which can cut the time required to produce a published book from a finished manuscript. This task traditionally took 15-18 months, but can be now reduced to less than 4 months. If *traditional* techniques are used to produce books in such fast-breaking fields as VLSI fabrication, these books automatically possess a built-in obsolescence, even upon being first published. The authors took advantage of the *rapid production techniques*, and were able to successfully meet the reduced production-time schedule. As a result, they were able to include information contained in technical journals

and conferences which was available within four months of the book's publication date. Earlier books written on silicon processing, unfortunately, suffer from having had to undergo an 15-18 month production cycle. *This is the first book on the subject in which such time-delay effects have been eliminated from the production process!*

Written for the professional, the book belongs on the bookshelf of workers in several microelectronic disciplines. *Microelectronic fabrication engineers* who seek to develop a more complete perspective of the subject, or who are new to the field, will find it invaluable. *Integrated circuit designers, test engineers, and integrated circuit equipment designers*, who must understand VLSI processing issues to effectively interface with the fabrication environment, will also find it a uniquely useful reference. The book should also be very suitable as a text for graduate-level courses on silicon processing techniques, offered to students of electrical engineering, applied physics, and materials science. It is assumed that such students already possess a basic familiarity with semiconductor device physics. Problems are included at the end of each chapter to assist readers in gauging how well they have assimilated the material in the text.

The book is an outgrowth of an intensive seminar conducted by the authors through the Engineering Extension of the University of California, Irvine. In the first three years that it was offered, over three hundred engineers and managers from more than 75 companies and government agencies, enrolled in the course. Its fine reputation is attested to by the fact that many firms have sent participants each time the course has been offered, presumably based on the recommendations of earlier enrollees.

In setting out to create a comprehensive text on VLSI fabrication, the authors each contributed a set of unique and complementary skills to the project. Professor Wolf's proficiency as a teacher and writer were utilized to produce a clearly written and logically organized book. Some of this expertise was gained in authoring an earlier best-selling text *Electronic Measurements and Laboratory Practice*, Prentice-Hall, 1983. Dr. Tauber brought a technical expertise acquired from his long involvement in the semiconductor industry. He used this background to insure that the most important topics of VLSI fabrication were addressed, and that the information was up-to-date and presented in a technically correct fashion. Note that for over twenty years, Dr. Tauber has held positions at Bell Telephone Laboratories, Xerox, And Hughes Aircraft Company. Currently he directs advanced VLSI Fabrication efforts at the Microelectronics Center of TRW. The labor of the writing effort was divided between the authors in the following manner: Professor Wolf was responsible for writing Chapters 1, 2, 3, 9, 10, 12, 13, 15, 16, 17, and 18, and Dr. Tauber undertook the writing of Chapters 4, 5, 7, 8, 11, and 14. Material for Chap. 6 was jointly contributed by Andrew R. Coulson and Dr. Tauber.

A book of this length and diversity would not have been possible without the indirect and direct assistance of many other workers. To begin with, virtually all of the information presented in this text is based on the research efforts of a countless number of scientists and engineers. Their contributions are recognized to a small degree by citing some of their articles in the references given at the end of each chapter. The direct help came in a variety of forms, and was generously provided by many people. The text is a much better work as a result of this aid, and the authors express heartfelt thanks to those who gave of their time, energy, and intellect.

Each of the chapters was reviewed after the writing was completed. The engineers and scientists who participated in this review were numerous. Special thanks are given to Leonard Braun and Ethelyn Motley, who provided extensive and incisive editing services. We also thank Warren Flack, Stephen Franz, Kenneth Tokunaga, Dean Denison, Simon Prussin, and Vitus Matare for their critical reviews. Simon Prussin also provided clarification of many concepts during the course of numerous technical discussions with the authors, and can be rightly considered as being the technical underpinning of Chapters 1, 2, 8, and 9. Extra thanks are also

extended to Mark Miscione for bringing valuable technical input on the subject of the physics of microlithography, to Susan Curry for donating SEM photographs, and to Andrew Coulson for creating some of the drawings. Ada Mae Hardeman, of the Engineering Extension of the University of California, Irvine is owed special thanks for helping to make a success of the seminar from which this book grew. Otto Gruneberg, of QBI, Inc. was also a benefactor of the project. He graciously agreed to share his exhibition space with Lattice Press at Semicon-West, 1986, where the book made its debut.

Superlative computer support and access to computer resources was generously made available by Donald E. Carlile, Harry T. Hayes, and Dale Lambertson of the Personal Computer Support Section of the Electronic Systems Group of TRW. Henry Nicholas was a computer expert and friend who lit the fire of inspiration that led to the undertaking of the project. The management of the Electronics Systems Group and the Microelectronics Center of TRW, including most notably Dr. Barry Dunbridge and Phillip Reid, are warmly thanked for providing a supportive environment, conducive to producing such an intensive technical project. They made available technical literature and other resources to the authors, especially S. Wolf, who was able to avail himself of this generosity while writing during a Sabbatical leave from his teaching duties at California State University, Long Beach. Roy Montibon and Donald Strout of Visionary Art Resources, Inc., Santa Ana, CA designed the cover. Finally, we wish to thank Shirley Rome, Carrol Ann Wolf, and Barbara Tauber for typing the manuscript.

Stanley Wolf and Richard N. Tauber

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PROLOGUE

Since the creation of the first integrated circuit in 1960, there has been an ever increasing density of devices manufacturable on semiconductor substrates. Silicon technology has remained the dominant force in integrated circuit fabrication and is likely to retain this position for the foreseeable future. The number of devices manufactured on a chip exceeded the generally accepted definition of *very large scale integration*, or *VLSI* (i.e. more than 100,000 devices per chip), somewhere in the mid-70's (Fig. 1a). By 1986, this number had, in fact, grown to over 1 million devices per chip. The increasing device count was accompanied by a shrinking minimum feature size (Fig. 1b), which is expected to be smaller than $1\text{ }\mu\text{m}$ before 1990. Progress in VLSI manufacturing technology seems likely to continue to proceed in this manner, and even further reductions in the unit cost per function, and in the power-delay product of VLSI devices, are projected. The entire adventure of VLSI represents a remarkable application of scientific knowledge to the requirements of technology, and this book represents an enthusiastic report on the state-of-the-art of VLSI silicon processing, as practiced at the time of publication.

Figure 2 illustrates the sequence of steps that occurs in the course of manufacturing an integrated circuit. These steps can be grouped into two phases: 1) the design phase; and b) the fabrication phase. This book is concerned only with the fabrication phase of this undertaking, but it is useful to briefly outline the steps of the design phase. This provides a context which allows the reader to perceive the role of silicon processing, within the totality of integrated circuit manufacturing. Readers wishing to explore steps of the design phase in further detail, are referred to other technical literature, including the texts listed in Refs. 1-3 at the end of this prologue.

In the *design phase* of this sequence, the desired functions and necessary operating specifications of the circuit are initially decided upon. The chip is then designed from the "top

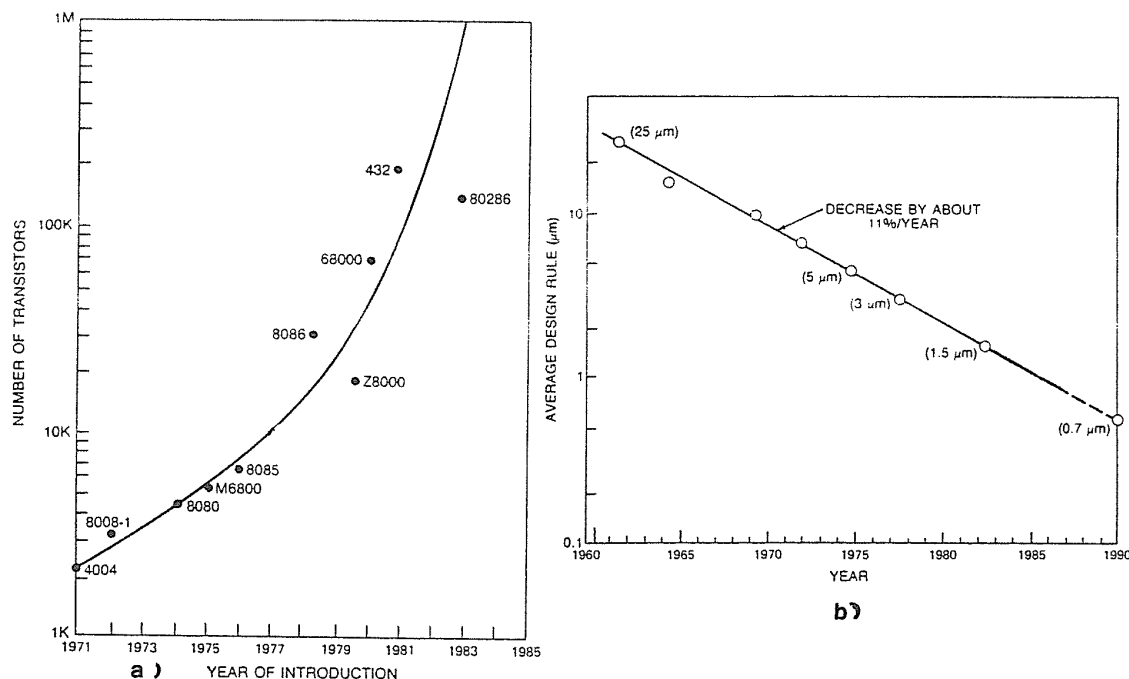


Fig. 1 (a) Increase in the number of transistors per microprocessor chip versus year of introduction, for a variety of 8-bit and 16 bit microprocessors, and (b) The decrease in minimum device feature size versus time on integrated circuits.

down". That is, the required large *functional blocks* are first identified. Next, their *sub-blocks* are selected, and then the *logic gates* needed to implement the sub-blocks are chosen. Each logic gate is designed by appropriately connecting devices (transistors, and in some cases resistors as well) that are ultimately slated for fabrication on the Si wafers. Upon completing these various levels of design, each is checked to insure that correct functionality has been achieved. When the designers are satisfied that each level of the design is correct, *test vectors*, that will be used to test the manufactured circuits, are generated from the schematic of the logic gates.

The circuit is then layed out. The *layout* consists of sets of patterns that will be transferred to the silicon wafer. The patterns correspond to device regions, or interconnect structures, and such patterns are sequentially transferred to the wafers through the use of photolithographic processes and a set of masks, as part of the wafer fabrication sequence (Fig. 4a). The result of each pattern transfer step is a set of features created on the wafer surface. These features are

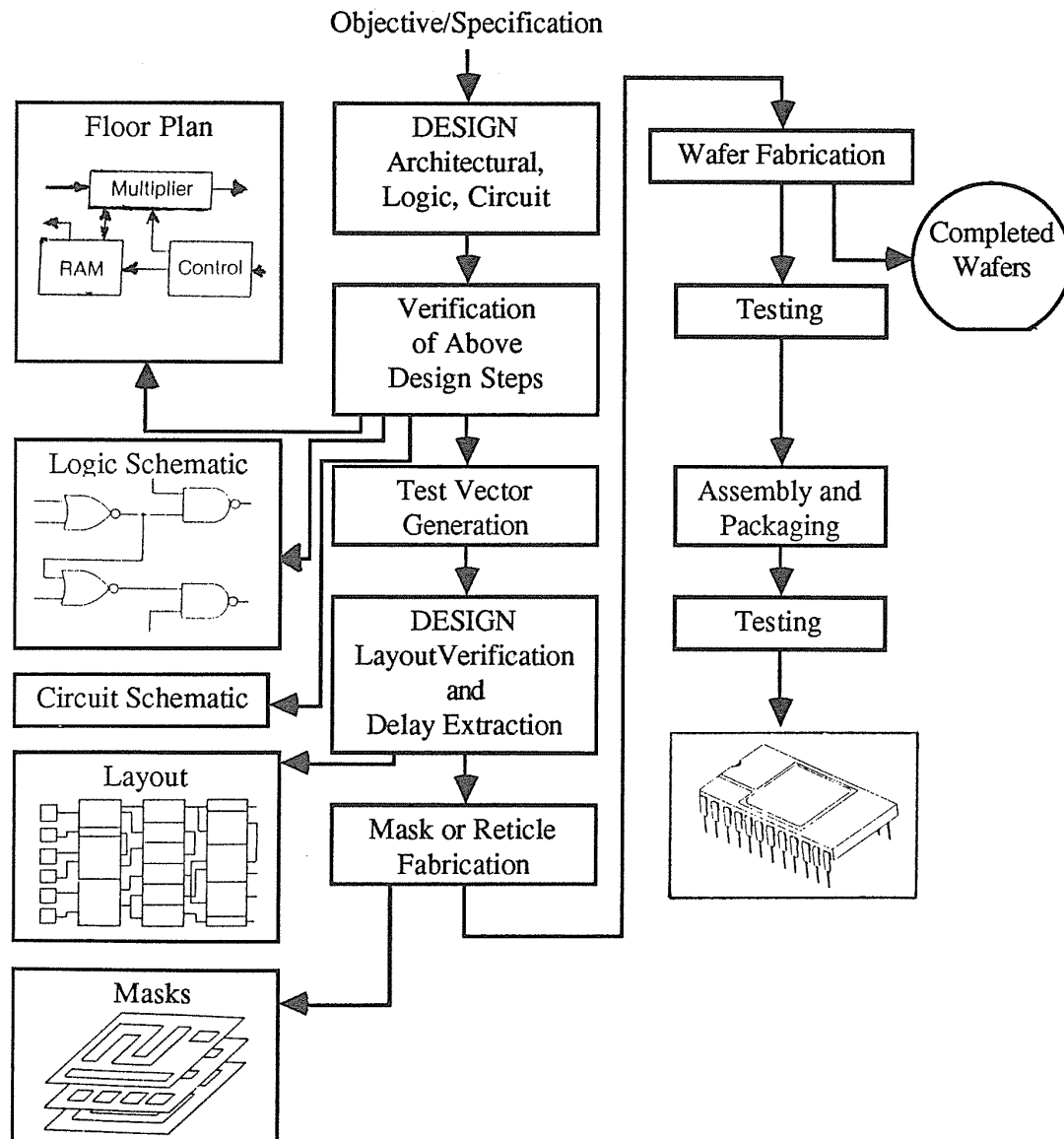


Fig. 2 Steps required for the manufacture of very large scale integrated circuits (VLSI).

generally either in the form of: a) an etched opening in a film (or region of the substrate); or b) a patterned feature of a film present on the surface (e.g. an interconnect line or pad). After the openings (or *windows*) are created by the pattern transfer step, either: a) controlled quantities of dopant are added to the silicon substrate through the openings, or b) another layer is deposited that makes contact to the underlying layer through the opening. In any case, device regions, and structures that interconnect device regions, are produced by the patterning processes and associated fabrication steps. A cross-section of a completed device, resulting from having carried out a sequence of such fabrication steps is shown in Fig. 4b.

The creation of the layout proceeds from the "bottom up". That is, a variety of typical devices are first layed out. Then, a set of cells representing the required primitive logic gates are created by interconnecting appropriate devices. Next, sub-blocks are generated by connecting these logic gates, and finally the functional blocks are layed out by connecting the sub-blocks. Power busses, clock-lines, input-output pads required by the circuit design are also incorporated during the layout process. The completed layout is then subjected to a set of *design rule checks* and *propagation delay simulations* to verify that correct implementation of the circuit has been

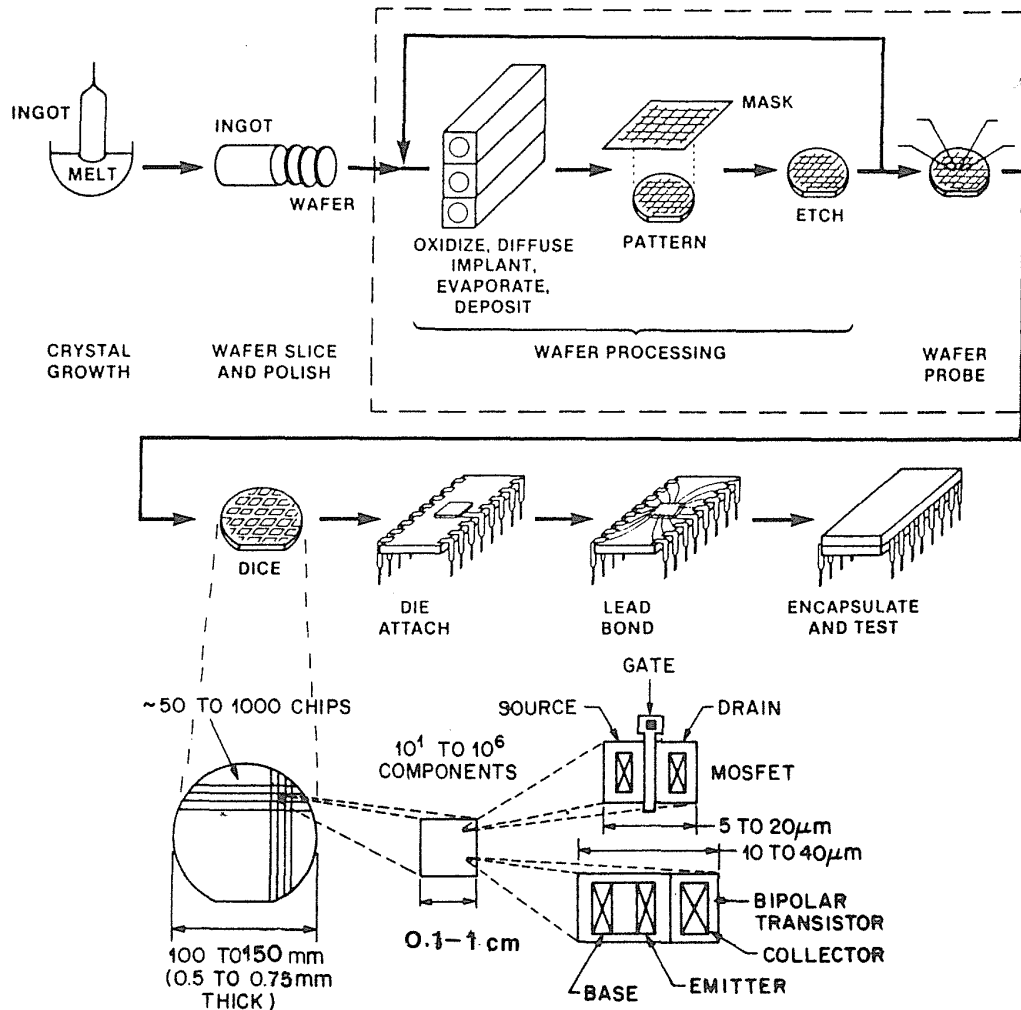


Fig. 3 The fabrication process sequence of integrated circuits.

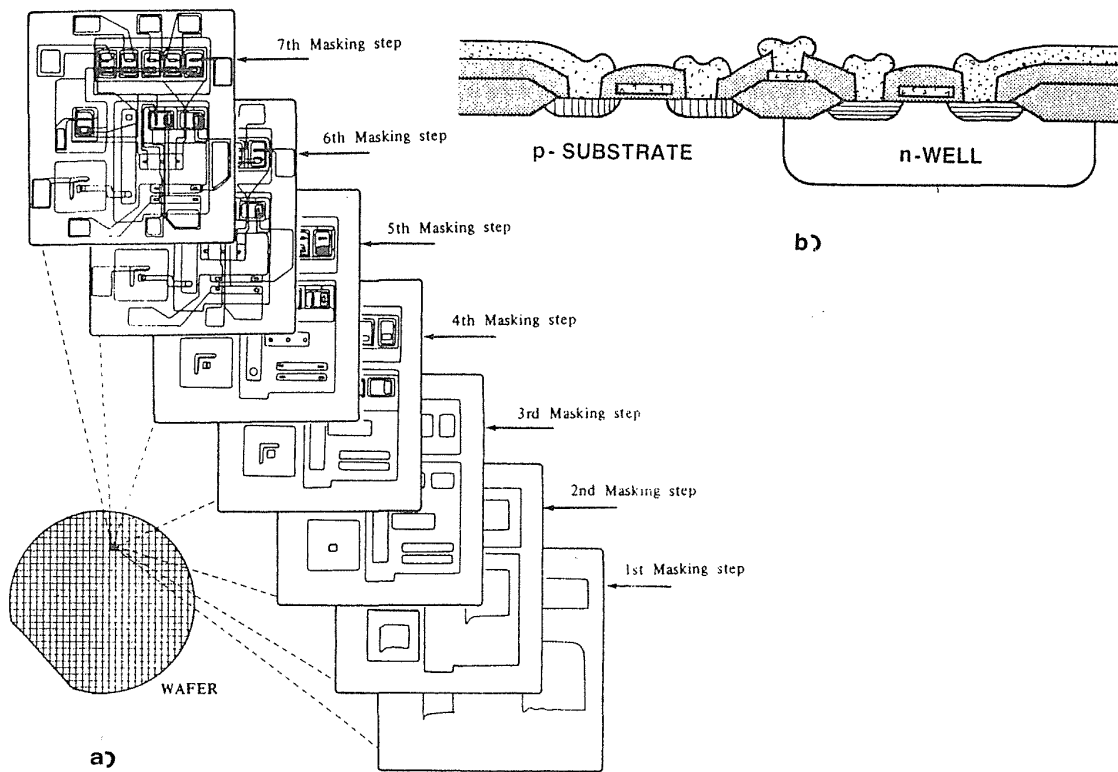


Fig. 4 (a) Example of the patterns transferred to a wafer during a seven-mask process sequence, and (b) Cross section of completed devices in a basic CMOS process.

achieved in layout form. After this checking procedure is completed, the layout information is ready to be used to generate a set of masks that will serve as tools for specifying the circuit patterns on silicon wafers. For VLSI circuits, layout information is stored on a computer.

In this two volume text, we describe the integrated circuit manufacturing steps that occur from the point at which the layout information becomes available (Fig. 3). That is, the first step of the manufacturing process considered in this book, is the set of the procedures utilized to convert the layout information, as stored on the computer, into a set of masks or reticles. All of the individual fabrication processes associated with creating patterns, introducing dopants, and depositing films on silicon substrates (to form integrated circuit features) are also subjects of this volume of our text. In addition, information about the manufacture of Si wafers (i.e. the *starting material* on which integrated circuits are fabricated), and direct supporting technologies (e.g. vacuum technology and material characterization) is also presented. In Volume 2 of this text, the remaining aspects silicon processing are covered, including process simulation, process integration, assembly, packaging, test, and it is thus aptly subtitled *Manufacturing Technology*.

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CHEMICAL VAPOR DEPOSITION of AMORPHOUS and POLYCRYSTALLINE THIN FILMS

Chemical vapor deposition (CVD) is defined as the formation of a non-volatile solid film on a substrate by the reaction of vapor phase chemicals (reactants) that contain the required constituents. The reactant gases are introduced into a reaction chamber and are decomposed and reacted at a heated surface to form the thin film. A wide variety of thin films utilized in VLSI fabrication is prepared by CVD^{1,2}. In Chap. 5, the growth of single-crystal silicon films by CVD epitaxial techniques is presented. The deposition of amorphous and polycrystalline thin films by CVD is the subject of this chapter (and to a lesser degree, of Chap. 11).

The deposition technology and equipment used to prepare such films by CVD will first be considered. Next a discussion of the properties and deposition conditions of some of the most widely used films deposited by CVD will be undertaken (including polycrystalline silicon, silicon dioxide, and silicon nitride). Information about the properties and deposition of refractory metals and their silicides by CVD is given in Chap. 11. Also note that the measurement of many of the properties of CVD films is virtually identical to the measurement of the same properties in other thin films. Thus, only the measurement of those properties that are unique to the specific thin films under discussion will be mentioned in this chapter. Readers should consult the index for information on various generic thin film measurement methods.

As discussed in Chap. 4, thin films are used in a host of different applications in VLSI fabrication, and can be prepared using a variety of techniques. Regardless of the method by which they are formed, however, the process must be economical (high throughput), and the resultant films must exhibit the following characteristics: a) good thickness uniformity; b) high purity and density; c) controlled composition and stoichiometries; d) high degree of structural perfection; e) good electrical properties; f) excellent adhesion; and g) good step coverage.

Specific deposition methods are developed to form such thin films, based on their potential capabilities for satisfying these demanding criteria. CVD processes are often selected over competing deposition techniques because they offer the following advantages: a) high purity deposits can be achieved; b) a great variety of chemical compositions can be deposited; c) some films cannot be deposited with adequate film properties by any other method; and d) good economy and process control are possible for many films.

This chapter was written by Andrew R. Coulson and Richard N. Tauber

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BASIC ASPECTS OF CHEMICAL VAPOR DEPOSITION

A CVD process can be summarized as consisting of the following sequence of steps: a) a given composition (and flow rate) of reactant gases and diluent inert gases is introduced into a reaction chamber; b) the gas species move to the substrate; c) the reactants are adsorbed on the substrate; d) the adatoms undergo migration and film-forming chemical reactions, and e) the gaseous by-products of the reaction are desorbed and removed from the reaction chamber. Energy to drive the reactions can be supplied by several methods (e.g. thermal, photons, or electrons), with thermal energy being the most commonly used.

In practice, the chemical reactions of the reactant gases leading to the formation of a solid material may take place not only on (or very close to) the wafer surface (*heterogeneous reaction*), but also in the gas phase (*homogeneous reaction*). Heterogeneous reactions are much more desirable, as such reactions occur selectively only on heated surfaces, and produce good quality films. Homogeneous reactions, on the other hand are undesirable, as they form *gas phase clusters* of the depositing material, which can result in poorly adhering, low density films, or defects in the depositing film. In addition, such reactions also consume reactants and can cause decreases in deposition rates. Thus, one important characteristic of a chemical reaction for CVD application is the degree to which heterogeneous reactions are favored over gas phase reactions.

Since the aforementioned steps of a CVD process are sequential, the one which occurs at the slowest rate will determine the rate of deposition. The steps can be grouped into 1) gas-phase processes, and 2) surface processes. As discussed in Chap. 5, the *gas phase phenomenon of interest* is the rate at which gases impinge on the substrate. This is modeled by the rate at which gases cross the boundary layer that separates the bulk regions of flowing gas and substrate surface. Such transport processes occur by gas-phase diffusion, which is proportional to the diffusivity of the gas, D , and concentration gradient across the boundary layer, dC/dx , see Chap. 5). The rate of mass transport is only relatively weakly influenced by temperature ($D \propto T^{1.5-2.0}$).

Several *surface processes* can be important once the gases arrive at the hot substrate surface, but the *surface reaction*, in general, can be modeled by a thermally activated phenomenon which proceeds at a rate, R , given by:

$$R = R_0 e^{-E_a/kT} \quad (1)$$

where R_0 is the frequency factor, E_a is the activation energy in eV, and T is temperature in °K (see Appendix 3). According to Eq. 1, the surface reaction rate increases with increasing temperature. For a given surface reaction, the temperature may rise high enough so that the reaction rate exceeds the rate at which reactant species arrive at the surface. In such cases, the reaction cannot proceed any more rapidly than the rate at which reactant gases are supplied to the substrate by mass transport, no matter how high the temperature is increased. This situation is referred to as a *mass-transport limited* deposition process.

On the other hand, at lower temperatures, the surface reaction rate is reduced, and eventually the arrival rate of reactants exceeds the rate at which they are consumed by the surface reaction process. Under such conditions the deposition rate is *reaction rate limited*. Thus, at high temperatures, the deposition is usually mass-transport limited, while at lower temperatures it is surface-reaction rate-limited (Fig. 1). In actual processes the temperature at which the deposition condition moves from one of these growth regimes to the other is dependent on the activation energy of the reaction, and the gas flow conditions in the reactor.

In processes that are run under *reaction rate-limited conditions*, the temperature of the

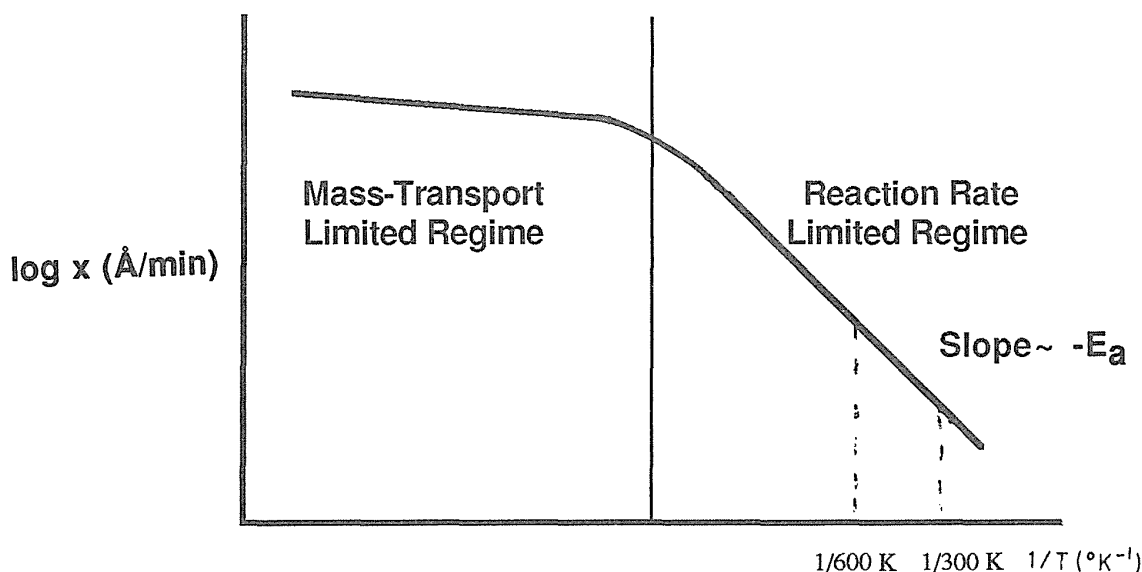


Fig. 1 Temperature dependence of growth rate for CVD films.

process is an important parameter. That is, uniform deposition rates throughout a reactor require conditions that maintain a constant reaction rate. This in turn implies that a constant temperature must also exist everywhere at all wafer surfaces. On the other hand, under such conditions the rate at which reactant species arrive at the surface is not as important, since their concentration does not limit the growth rate. Thus, it is not as critical that a reactor be designed to supply an equal flux of reactants to all locations of a wafer surface. It will be seen that in low-pressure CVD (LPCVD) reactors, wafers can be stacked vertically and at very close spacing because such systems operate in a reaction rate limited mode. The reason for this is as follows:

Under the low pressure of an LPCVD reactor (~ 1 torr) the diffusivity of the gas species is increased by a factor of 1000 over that at atmospheric pressure, and this is only partially offset by the fact that the boundary layer (the distance across which the reactants must diffuse) increases by less than the square root of the pressure. The net effect is that there is more than an order of magnitude increase in the transport of reactants to (and by-products away from) the substrate surface, and the rate-limiting step is thus the surface reaction⁴. Note, however, that since the surface reaction rate also generally increases with increasing surface concentration, non-uniform gas phase concentrations produced by local depletion of reactants within the reactor can result in deposition non-uniformities. An example of a such an effect is the depletion of reactants from a gas by their deposition on wafers located at the inlet of an end-feed reactor tube. Wafers near the outlet end are consequently exposed to gases containing lower concentrations of reactants than those at the inlet end of the tube.

In deposition processes that are *mass-transport limited*, however, the temperature control is not nearly as critical. As mentioned earlier, the mass transport process which limits the growth rate is only weakly dependent on temperature. On the other hand, it is very important that the same concentration of reactants be present in the bulk gas regions adjacent to all locations of a wafer, as the arrival rate is directly proportional to the concentration in the bulk gas. Thus, to insure films of uniform thickness across a wafer, reactors which are operated in the mass transport limited regime must be designed so that all locations of wafer surfaces and all wafers in a run are supplied with an equal flux of reactant species. Atmospheric pressure reactors that deposit SiO_2 at $\sim 400^\circ\text{C}$ operate in the mass-transport limited regime. The most widely used

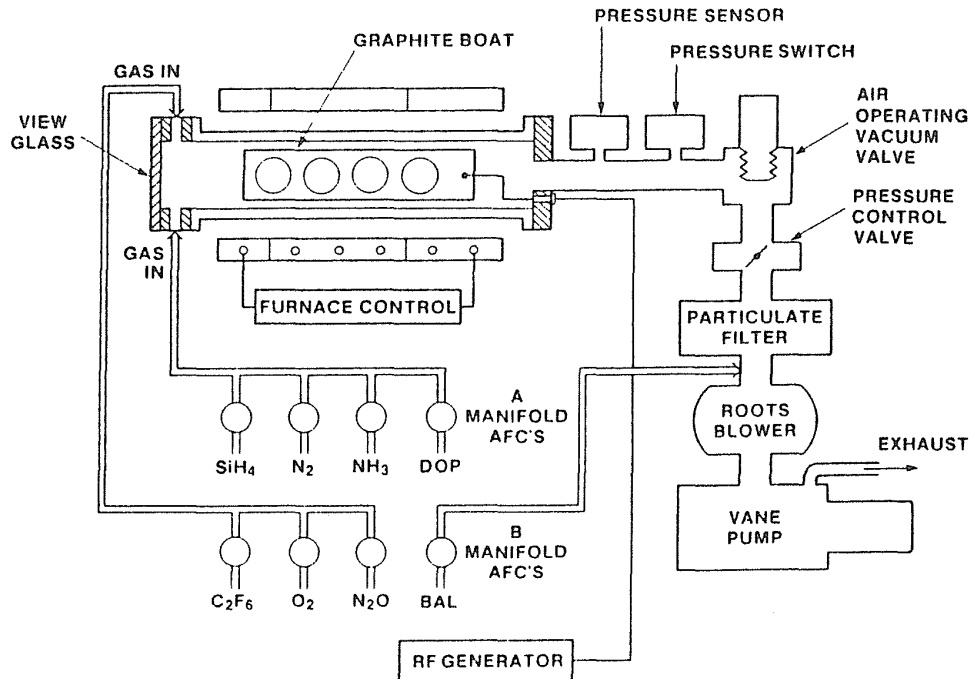


Fig. 2 Diagram of a typical commercial PECVD system. Courtesy of Pacific Western Systems.

APCVD reactor designs provide a uniform supply of reactants by horizontally positioning the wafers and moving them under a gas stream.

CHEMICAL VAPOR DEPOSITION SYSTEMS

Components of CVD Systems

A schematic diagram of a CVD system is shown in Fig. 2. Actually, this figure shows a plasma-enhanced [PECVD] system. Non-plasma enhanced CVD systems can be identically represented, minus the rf generator and matching network, and pump [in atmospheric systems]. CVD reactors are generally *open-flow* systems, in which gases continuously flow into the reaction chamber (where the deposition occurs), and gaseous by-products are exhausted together with unused reactant and diluent gases. Reactant gases are typically carried by diluent (*carrier*) gases such as H_2 , N_2 , or Ar. Corrosive and hazardous gases pumped from the chamber are removed from the exhaust gas flow by a *scrubber*, and the remainder are vented to the atmosphere.

CVD systems usually contain the following components: a) gas sources; b) gas feed lines; c) mass-flow controllers (for metering the gases into the system); d) a reaction chamber (or reactor); e) a method for heating the wafers onto which the film is to be deposited (and in some types of systems, for adding additional energy by other means); and f) temperature sensors. LPCVD and PECVD systems (to be defined) also contain pumps for establishing the reduced pressure and exhausting the gases from the chamber. With the exception of the reaction chamber configurations and mass-flow controllers, a discussion of the operating procedures of all of the components of CVD systems is undertaken in other chapters of the book since they find use in various wafer processing systems besides CVD equipment. As a result, only mass-flow controller operation is described in this section, and reactor configurations are covered in

later sections of this chapter.

Mass-flow Controllers

CVD reactors and other process systems (e.g. dry-etchers, diffusion furnaces), require that the rates of introduction of process gases into the process chambers be controlled. In some applications, this is achieved by adjusting the gas influx to maintain a constant chamber pressure. More commonly, the process gas flow is directly controlled. In the latter case, an instrument known as a *mass-flow controller* performs this function. Mass flow controllers consist of a mass-flowmeter, a controller, and a valve. They are located between the gas source and the chamber, where they can monitor and dispense the gases at predetermined rates.

Gas flow is measured in units of volume /unit-time, where the volume measurement assumes standard temperature and pressure. A flow of one *standard cubic centimeter per minute* (sccm) is thus defined as a flux of one cm³ of gas per minute at 273 °K and 760 torr. Since one mole of gas at STP occupies 22.414 liters, one sccm = (1 /22,414) moles /min.

The heart of the mass-flow controller is its mass flowmeter, of which there are two types, the *differential pressure type*, and the *thermal type*. The differential type relates a pressure drop at a flow restriction to mass rate of flow. In semiconductor applications, however, the thermal type is more widely used, as a result of its relatively rapid response time (e.g. 2-3 sec), and its low cost. We describe its operation in more detail.

The operation of thermal mass flowmeters relies on the ability of a flowing gas to transfer heat. A schematic of a mass-flow controller is shown in Fig. 3. The mass flowmeter consists of a small sensor tube in parallel with the larger main gas flow tube. A heating coil is wrapped around the sensor tube midway along its length, and temperature sensors (typically resistance thermometers) are located both upstream and downstream of the heated point. When gas is not flowing, and the heat input is constant, the temperatures at both sensors are equal. Flowing gas causes the temperature distribution in the sensor tube to change. The temperature downstream of the heater becomes higher than the temperature upstream since the flowing gas conducts heat away from the heated point. It can be shown that the mass flow, m_f , is given by:

$$m_f = (\kappa W_h \Delta T)^{1.25} \quad (1)$$

where W_h is the heater power, ΔT is the temperature difference between the points where the sensors are located ($\cong 1^\circ\text{C}$), and κ is a constant that depends on heat transfer coefficients, the specific heat of the gas, the density of the gas, and the thermal conductivity of the gas. It is assumed that these characteristics remain constant over the flow range measured, and hence mass rate can be obtained by measuring the temperature difference. Each of the resistance thermometers are connected to one arm of an unbalanced Wheatstone bridge, and the temperature difference is converted to a voltage signal. Calibration factors are used so that the voltage output derived from the sensor tube can express the flow (in units of sccm) through the entire flow controller. As the flow rate is determined, its value is compared by the controller to the setpoint value. If necessary, the controller adjusts the valve setting so that the flow returns to the specified value.

During the startup of a process from a condition of zero flow, the feedback and control loop operation is hindered by the slow response of the sensor (i.e. it takes time for the temperature sensors to heat). As a result, the initial gas flow may initially overshoot the setpoint value. Two techniques have been devised to reduce this problem. They are: 1) *setpoint ramping*, by which the setpoint value is slowly ramped up from zero to the final value during startup; and 2) use of *mass flow sensors* with much faster response times. Microscopic mass flow sensors micromachined on silicon substrates have been recently developed for this application³.

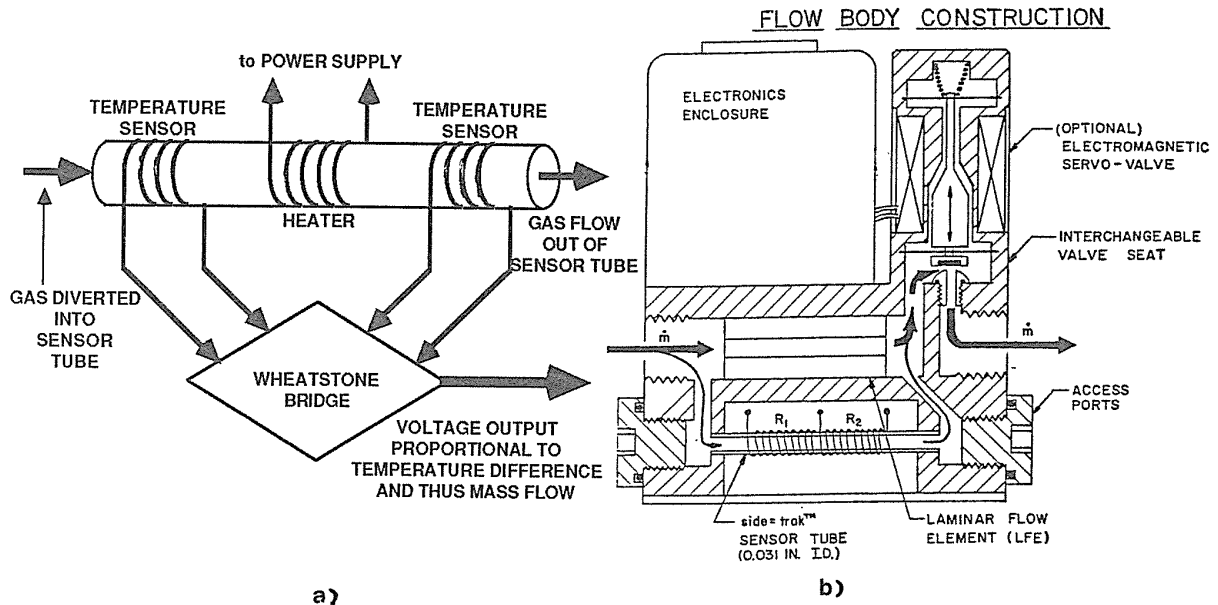


Fig. 3 (a) Operating principle, and (b) cutaway drawing of a mass flow controller. Courtesy of Sierra Instruments.

Due to their extremely small thermal mass, such sensors are capable of responding to heat flux differences (and hence to gas flow rate changes) in times on the order of milliseconds.

Some other requirements of mass flow controllers include: a) that they be immune to stray rf fields (in plasma equipment, for example); b) that they be extremely leak-tight, to prevent leakage of hazardous process gases; c) that they be resistant to damage by corrosive process gases; and d) that they be easy to clean and maintain.

Terminology of CVD Reactor Design

The design and operation of CVD reactors depends on a variety of factors, and hence they can be categorized in several ways. Figure 4 illustrates one way of grouping CVD reactor types. The first distinction between reactor types is whether they are *hot-wall* or *cold-wall* reactors, and this is dependent on the method used to heat the wafers. The next criterion used to distinguish reactor types is their pressure regime of operation (*atmospheric pressure* or *reduced pressure* reactors). Finally, the reduced pressure group is split into: a) low-pressure reactors (the so called *low-pressure CVD*, or *LPCVD* reactors, in which the energy input is entirely thermal); and b) those in which energy is partially supplied by a plasma as well (known as *plasma-enhanced CVD*, or *PECVD* reactors). Each of the reactor types in the two pressure regimes are further divided into sub-groups, defined by reactor configuration and method of heating.

Four methods of heating the wafers and their holder (e.g. a susceptor) have been adopted. They are: a) resistance heating; b) rf induction heating; c) energy from a glow discharge (plasma), and d) photons. Energy may be transferred either to the reactant gases themselves or to the

substrate. When radiant heating from resistance-heated coils surrounding the reaction tube is utilized, not only the wafers but also the reaction chamber walls become hot, and hence such designs are known as *hot-wall* reactors. In these systems, film forming reactions (and as a result, film deposition) occurs on reaction chamber walls as well as on substrates. This implies that such systems will require frequent cleaning.

On the other hand, energy input via infrared lamps mounted within the reactor or rf induction, primarily heats the wafers and susceptor, and does not cause appreciable heating of the reaction chamber walls. Consequently systems heated by these methods are termed *cold-wall* reactors. In some cold-wall systems, however, significant chamber wall heating can still take place, and provisions for cooling the walls must be implemented (e.g. by water cooling) to prevent reactions or depositions from occurring there.

Reactor geometry is constrained by the pressure regime and energy source used, and is an important factor in throughput. Since atmospheric pressure reactors by and large operate in the mass-transport limited regime, they must be designed so that an equal flux of reactants is delivered to each wafer. As a result wafers are never stacked vertically at close spacing, but are rather laid flat on a horizontal surface. An undesirable consequence of this design is the high susceptibility of the wafers to incorporate falling particles. LPCVD reactors are not constrained by the mass-transfer rate limitation, allowing designs that accomodate a large number of wafers per run. That is, wafers can be stacked side by side, only a few mm apart in a quartz reaction tube. Quartz wafer holders (boats) can hold up to 200 wafers. Since LPCVD reactors operate in the surface reaction limited mode, they must, however, be capable of precise temperature control. Table 1 summarizes the characteristics and applications of the various CVD reactor designs.

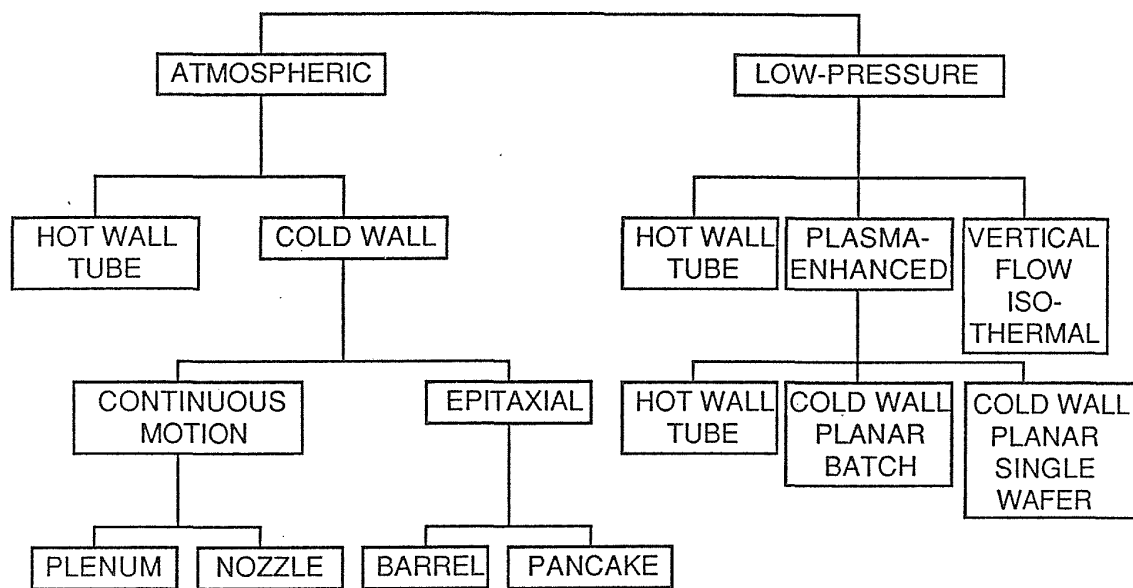


Fig. 4 CVD reactor types.

Table 1. CHARACTERISTICS and APPLICATIONS OF CVD REACTORS

PROCESS	ADVANTAGES	DISADVANTAGES	APPLICATIONS
APCVD (Low Temperature)	Simple Reactor, Fast Deposition, Low Temperature	Poor Step Coverage, Particle Contamination	Low Temperature Oxides, both doped and undoped
LPCVD	Excellent Purity and Uniformity, Conformal Step Coverage, Large Wafer Capacity	High Temperature Low Deposition Rate	High Temperature Oxides, both doped and undoped, Silicon Nitride, Poly-Si, W, WSi ₂
PECVD	Low Temperature, Fast Deposition, Good Step Coverage	Chemical (e.g. H ₂) and Particulate Contamination	Low Temperature Insulators over Metals, Passivation (Nitride)

Atmospheric Pressure CVD Reactors

Atmospheric pressure CVD reactors (APCVD) were the first to be used by the microelectronics industry^{4,5}. Operation at atmospheric pressures kept reactor design simple and allowed high film-deposition rates. APCVD, however, is susceptible to gas phase reactions, and the films typically exhibit poor step coverage. Since APCVD processes are also generally conducted in the mass-transport limited regime, the reactant flux to all parts of every substrate in the reactor must be precisely controlled. This places constraints on reactor geometry and gas flow patterns. Nevertheless, APCVD processes for deposition of oxides, nitrides and polysilicon were developed, only to be supplanted by superior LPCVD processes (see below). Currently, atmospheric reactors are primarily used for low-temperature oxide (LTO) deposition and epitaxy.

Figure 5 shows schematics of the two types of atmospheric systems. The first is the *horizontal tube type* (Fig. 5a). Such systems consist of a horizontal quartz tube, with the wafers

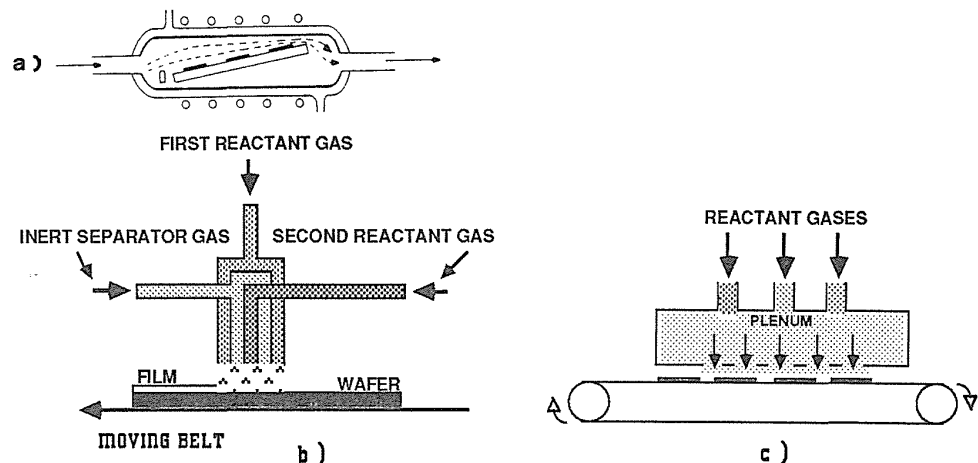


Fig. 5 (a) Horizontal tube APCVD reactor. (b) Gas injector type continuous processing APCVD reactors. (c) Plenum-type continuous processing APCVD reactor.

lying flat on a fixed horizontal plate, while gas flows parallel to the wafer surface. Reactant gases are metered into one end of the tube, and unused or by-product gases exhausted out through the other. Energy is supplied by radiant heating from resistance-heated coils that surround the tube (hot wall). It is possible to deposit polysilicon and SiO_2 in these systems, but as the systems suffer from low throughput, poor uniformity and particulate contamination, they find little use in VLSI fabrication.

The second AP type is the *continuous processing APCVD reactor* (Fig. 5b and c). This configuration is the most widely used design for depositing low temperature CVD SiO_2 films in production applications. Continuous processing APCVD reactors move the wafers at constant speed through a heated reactor(s), either on a moving plate or continuous conveyor belt. The deposition region is carefully isolated from outside air by curtains of flowing inert gas. Reactant gases may either: a) be mixed in a *plenum* (i.e. from the Latin, full), which is a confined volume filled with flowing process gases at a positive pressure (i.e. slightly greater than atmospheric pressure); or b) be injected from cooled, nitrogen shrouded nozzles, so that mixing occurs only millimeters above the wafer surface (thus reducing gas phase reactions).

Film deposition also takes place on the plate or belt, as well as on the wafers, so frequent cleaning of the system is necessary. At least one commercial system offers an *in situ* HF vapor clean, which allows the continuous belt to be cleaned without disassembly. Modern continuous belt reactors are capable of the thickness uniformity, low contamination, and high throughputs required of VLSI CVD SiO_2 films.

Low-Pressure Chemical Vapor Deposition Reactors

Low pressure chemical vapor deposition (LPCVD) in some cases is able to overcome the uniformity, step coverage, and particulate contamination limitations of early APCVD systems^{6,7,8}. By operating at medium vacuum (30-250 Pa or 0.25-2.0 torr), and higher temperatures (550-600°C), LPCVD reactors typically deposit films in the reaction rate limited regime. As described earlier, at reduced pressure the diffusivity of the reactant gas molecules is sufficiently increased so that mass-transfer to the substrate no longer limits the growth rate. The surface reaction rate is very sensitive to temperature (Eq. 1), but precise temperature control is relatively easy to achieve. The elimination of mass-transfer constraints on reactor design allows the reactor to be optimized for high wafer capacity. Low pressure operation also decreases gas phase reactions, making LPCVD films less subject to particulate contamination. LPCVD is used for depositing many types of films, including poly-Si, Si_3N_4 , SiO_2 , PSG, BPSG, and W.

The two main disadvantages of LPCVD are the relatively low deposition rates, and the relatively high operating temperatures. Attempting to increase deposition rates by increasing the reactant partial pressures, tends to initiate gas phase reactions. Attempting to operate at lower temperatures, results in unacceptably slow film deposition. LPCVD reactors are designed in two primary configurations: a) horizontal tube reactors; and b) vertical flow isothermal reactors.

Horizontal Tube LPCVD Reactors (Hot Wall)

Horizontal tube, hot wall reactors are the most widely used LPCVD reactors in VLSI processing. They are employed for depositing poly-Si, silicon nitride, and undoped and doped SiO_2 films. They find such broad applicability primarily because of their superior economy, throughput, uniformity, and ability to accommodate large diameter (e.g. 150 mm) wafers. Their main disadvantages are susceptibility to particulate contamination¹³ and low deposition rates.

Conventional LPCVD tube reactors are very similar to APCVD tube reactors, in that the wafers are radiantly heated by resistive heating coils surrounding the tube. Reactant gases are

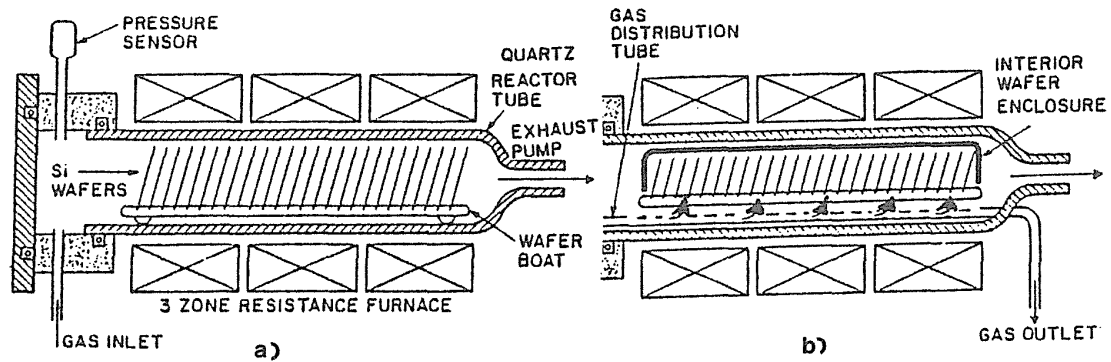


Fig. 6 (a) End feed LPCVD reactor. (b) Distributed-feed LPCVD reactor². Reprinted with permission of Semiconductor International.

also metered into one end of a horizontal quartz tube (using mass flow controllers), and reaction by products are pumped out the other. Vacuum pumps are used to establish the required reduced pressure, typically 0.25-2.0 torr, in the tube. An oil-sealed rotary mechanical pump is generally utilized, often augmented with a Roots pump. A pressure controller⁹, with feedback control of the gas flow or the pump inlet valve may be also be included.

The fact that LPCVD processes operate in a reaction rate limited regime allows wafers to be arranged differently inside the tube than in APCVD tube reactors (since equal mass transport to all parts of every wafer is no longer critical). That is, wafers are positioned vertically (Fig. 6) at very close spacing (e.g. 5-6 mm), perpendicular to the gas flow, in quartz boats (in a manner similar to that used in diffusion furnaces, as described in Chap. 7). Up to 200 wafers can be processed per run. The large number of wafers processed in a single process cycle allows greater throughput than with horizontal-tube APCVD reactors, in spite of the relatively low deposition rates of LPCVD processes (100-500Å/min).

Depletion effects which reduce gas phase concentrations as reactants are consumed by reactions on wafer surfaces, are still operative in such end-fed reactors. That is, wafers near the inlet are exposed to higher concentrations of reactant gases. As a result, deposition rates are greater on wafers placed near the inlet end of the tube. Since the reaction rates increase with increasing temperature, these deposition rate variations can be minimized by linearly increasing temperature along the length of the tube (e.g. by 25-40°C). Such temperature ramping compensates for the reactant gas depletion, and better thickness uniformity is obtained (Fig. 6a). Nonuniform temperatures along the tube length, however, will affect deposition temperature-dependent film properties. This is a particular problem for poly-Si and low-temperature (~400°C) deposition of doped SiO₂. Hence, conventional end-feed LPCVD reactors are used for high temperature deposition (800-850°C) of silicon nitrides and oxynitrides, and for undoped poly-Si films (~600°C), in which the temperature differential does not significantly impact film properties.

Another technique to alleviate the depletion effect, known as *distributed feed*, has been developed for hot-wall tube reactors. In this approach, special injection systems supply fresh reactants at a number of points along the length of the tube (Fig. 6b). Although this requires the use of specially designed quartzware, it allows the temperature along the tube to remain constant. Distributed feed LPCVD hot wall reactors are used for low-temperature (<600°C) deposition of SiO₂, PSG, and BPSG films, and *in situ* doped poly-Si films.

Vertical Flow Isothermal LPCVD Reactors (Cold-Wall)

The vertical flow isothermal LPCVD reactor further extends the distributed gas feed technique, so that each wafer receives an identical supply of fresh reactants¹⁰. Wafers are again stacked side by side, but are placed in perforated-quartz cages. The cages are positioned beneath long, perforated, quartz reaction-gas injector tubes (one tube for each reactant gas). Gas flows vertically from the injector tubes, through the cage perforations, past the wafers (parallel to the wafer surface, Fig. 7) and into exhaust slots below the cage. The size, number, and location of cage perforations are used to control the flow of reactant gases to the wafer surfaces. By properly optimizing cage perforation design, each wafer can be supplied with identical quantities of fresh reactants from the vertically adjacent injector tubes. Thus, this design can avoid the wafer-to-wafer reactant depletion effects of the end-feed tube reactors, requires no temperature ramping, produces highly uniform depositions, and reportedly achieves low particulate contamination.

Plasma Enhanced CVD: Physics, Chemistry, & Reactor Designs

The third and last of the major CVD deposition methods is categorized not only by pressure regime, but also by its method of energy input. Rather than relying solely on thermal energy to initiate and sustain chemical reactions, plasma enhanced CVD (or PECVD) uses an rf-induced glow discharge to transfer energy into the reactant gases, allowing the substrate to remain at a lower temperature than in APCVD or LPCVD processes. Lower substrate temperature is the major advantage of PECVD, and in fact, PECVD provides a method of depositing films on substrates that do not have the thermal stability to accept coating by other methods (the most important being the formation of silicon nitride and SiO_2 over metals). In addition, PECVD can enhance the deposition rate when compared to thermal reactions alone, and produce films of unique compositions and properties. Desirable properties such as good adhesion, low pinhole density, good, step coverage, adequate electrical properties, and compatibility with fine-line pattern transfer processes, have led to application of these films in VLSI.

The plasma (more correctly a *glow discharge*) is generated by the application of an rf field to a low pressure gas, thereby creating free electrons within the discharge region. There is a thorough discussion of glow discharge physics in Chap. 10. The electrons gain sufficient energy from

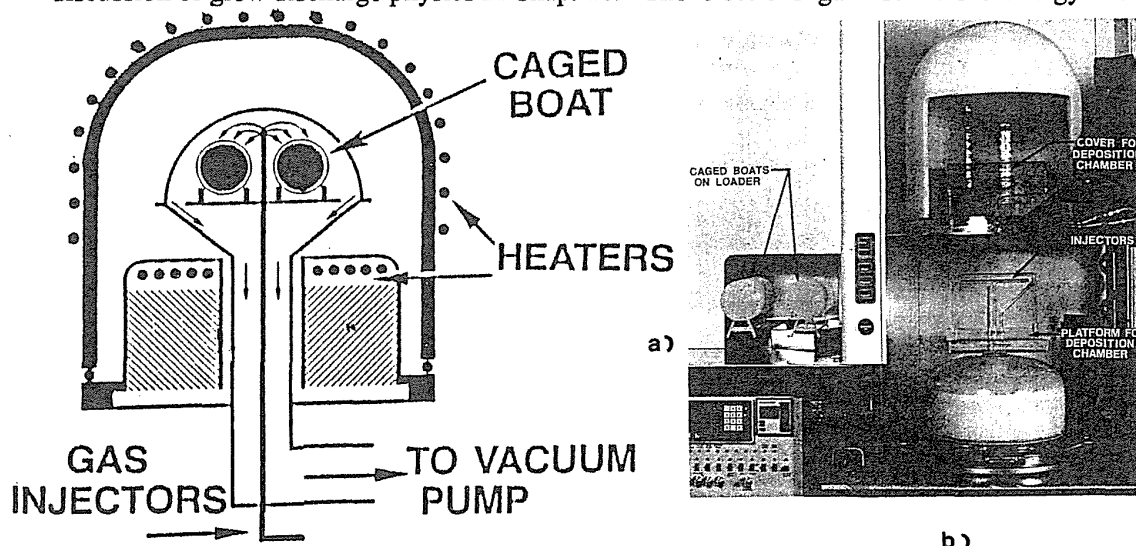


Fig. 7 Vertical isothermal LPCVD reactor. (a) Schematic drawing. (b) Photograph of system. Courtesy of Anicon, Inc.

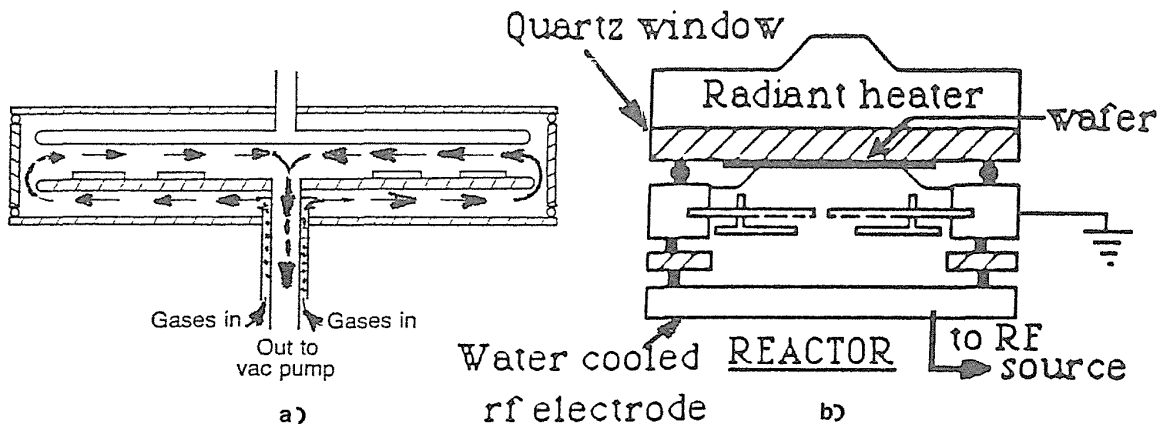


Fig. 8 (a) Radial flow reactor's inward flow (Reinberg design). Reprinted with permission of Semiconductor International¹³ (b) Single wafer PECVD reactor. Courtesy of CVD Spectrum, Inc.

the electric field so that when they collide with gas molecules, gas-phase dissociation and ionization of the reactant gases (e.g. silane and nitrogen or oxygen-containing species) then occurs.

The energetic species (predominantly radicals, as described in Chap. 16) are then adsorbed on the film surface. (Note that the radicals tend to have high sticking coefficients, and also appear to migrate easily along the surface after adsorption. These two factors can lead to excellent film conformality). Upon being adsorbed on the substrate, they are subjected to ion and electron bombardment, rearrangements, reactions with other adsorbed species, new bond formations and film formation and growth. Adatom rearrangement includes the diffusion of the adsorbed atoms onto stable sites and concurrent desorption of reaction products. Desorption rates are dependent on substrate temperature, and higher temperatures produce films with fewer entrapped by-products. Note that gas-phase nucleation should be avoided to reduce particulate contamination.

The fact that the radicals formed in the plasma discharge are highly reactive, presents some options as well as some problems, to the process engineer. PECVD films, in general, are not stoichiometric because the deposition reactions are so varied and complicated. Moreover, by-products and incidental species are incorporated into the resultant films (especially hydrogen, nitrogen, and oxygen), in addition to the desired products. Excessive incorporation of these contaminants may lead to outgassing and concomitant bubbling, cracking, or peeling during later thermal cycling, and to threshold shifts in MOS circuits.

A plasma process requires control and optimization of several deposition parameters besides those of an LPCVD process, including rf power density, frequency, and duty cycle. The deposition process is dependent in a very complex and interdependent way on these parameters, as well as on the usual parameters of gas composition, flow rates, temperature, and pressure. Furthermore, as with LPCVD, the PECVD method is surface reaction limited, and adequate substrate temperature control is thus necessary to ensure film thickness uniformity.

Three types of PECVD reactors are available: 1) the *parallel plate* type; 2) the *horizontal tube* type; and 3) the *single wafer* type. It should be noted that with one major exception, the discussion on glow discharges and rf diode sputtering in Chap. 10, and rf generated plasmas for dry etching in Chap. 16, applies to the production of rf generated plasma in PECVD reactors. Thus it is recommended that readers study these sections for information dealing with the generation of rf plasmas.

The one key difference in designing the reactor and electrode configuration in PECVD systems (compared to those in rf sputtering systems), is that in PECVD systems it is desired that the potential of both the powered and the grounded electrode(s), relative to the plasma, be

approximately equal. Rf tuning networks of PECVD systems therefore usually employ an inductor which shunts the powered electrode to ground to establish this condition. Grounding prevents the powered electrode from developing a larger self-bias, thereby maintaining approximately equal average potentials between the plasma and the powered and grounded electrodes. The walls of parallel plate reactors are made of either quartz, ceramic, or aluminum oxide coated steel, in order to place them at a floating potential with respect to the plasma. This minimizes wall bombardment and sputtering, which reduces contamination of the growing films. (Note that the quartz tube of tube PECVD reactors is an insulator, and thus does not require such coating).

Parallel Plate PECVD Reactors

The radial parallel plate reactor was developed by Reinberg⁵² in the early 1970's, and the first commercial model was offered in 1976. A schematic of this reactor type is shown in Fig. 8a. The reaction chamber is a short, vertically oriented cylinder, typically constructed of stainless steel. The rf power (at frequencies of 450 kHz-13.5 MHz) which establishes the plasma is applied to the upper electrode, and the wafers reside on the bottom grounded electrode, which can be rotated for improved uniformity, and be heated up to 400°C. The electrode spacing is typically 5 to 10 cm, and such systems operate in the pressure range of 0.1-5 torr. The reactants are introduced either through the center and removed from the periphery (Reinberg design), or from the periphery and removed from the center. Despite depletion effects, uniform deposition can be achieved by correctly balancing the plasma density and gas flows. Parallel plate systems, however, suffer from low throughput for large diameter wafers. In addition, particulates flaking off walls or the upper electrode, can fall onto the horizontally positioned wafers.

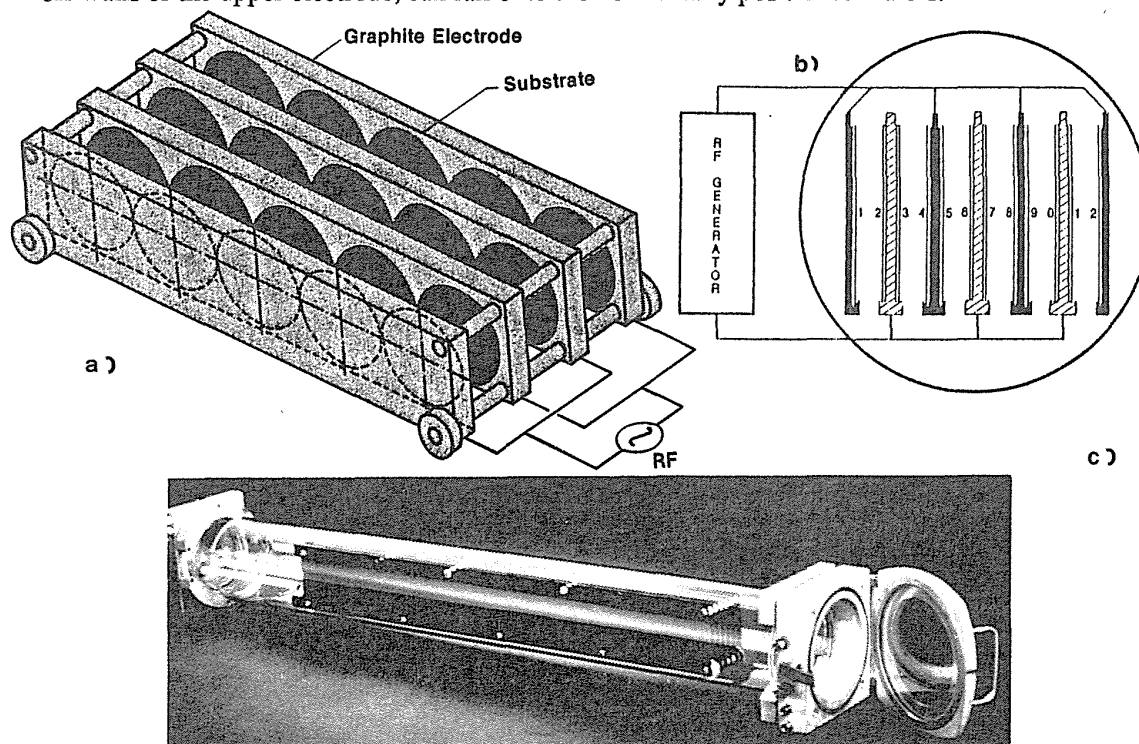


Fig. 9 (a) Long, multiple plate reactor generates plasma between the wafers facing each other on graphite electrodes¹⁴. (b) Cross section of electrode assembly and wafers shown in (a). Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet. (c) Photograph of tubular PECVD reactor. Courtesy of Pacific Western Systems.

Horizontal Tube PECVD Reactors

In 1979 a new PECVD reactor design, the *horizontal tube* reactor, was introduced. This design allows PECVD reactor throughputs to be greatly increased. The reactor resembles a "hot wall" LPCVD system. It consists of a long horizontal quartz tube that is radiantly heated. Gas is fed into one end, and flows linearly to the other. Special long rectangular graphite plates (Fig. 9) serve both as the electrodes that are needed to establish a plasma, and as holders of the wafers (the electrode configuration is also designed to provide a uniform plasma environment for each wafer, to ensure uniformity of deposition). These vertically-oriented graphite electrodes are stacked parallel to one another, side-by-side, with alternating plates serving as power and ground for the rf voltage. A plasma is formed in the space between each pair of plates.

The use of several long slabs allows an increased number of wafers (up to 120 100mm wafers) to be loaded into the reactor at one time. Most systems consist of two stacked deposition tubes. In addition, since the wafers are held vertically, most particulates do not fall on the wafer surfaces. The entire graphite assembly is withdrawn from the reactor for wafer loading, and then reinserted for processing. Care must be exercised, however, to prevent particulate contamination when loading and unloading wafers from these systems.

Tubular PECVD reactors, like horizontal tube LPCVD reactors, suffer from a depletion effect, but resultant deposition nonuniformities can be minimized by temperature ramping. Another technique used to combat depletion effect nonuniformities is to pulse the plasma, so that during the off phase of the duty cycle, fresh reactant gases fill the tube and replace depleted gases.

Single Wafer PECVD Reactors

The most recently introduced PECVD reactor is the single-wafer design (Fig. 8b). The reactor is load locked, offers cassette-to-cassette operation, provides rapid radiant heating of each wafer, and allows *in situ* monitoring of the film deposition. Wafers ≥ 200 mm can be accommodated. Little direct information on the operational characteristics of such reactors was available at the time of publication, but such reactors are clearly being designed to allow fabrication of large wafers in low-particulate, automated environments.

Photon-Induced Chemical Vapor Deposition

A final CVD method, which may fill the need for an extremely low temperature deposition process without the film composition problems of PECVD, is PHoton-induced Chemical Vapor Deposition (PHCVD). PHCVD uses high-energy, high-intensity photons to either heat the substrate surface, or to dissociate and excite reactant species in the gas phase. In the case of substrate surface heating, the reactant gases are transparent to the photons, and the potential for gas phase reactions is completely eliminated. In the case of reactant gas excitation, the energy of the photons can be chosen for efficient transfer of energy to either the reactant molecules themselves, or to a catalytic intermediary, such as mercury vapor. This technique enables deposition at extremely low (i.e. room) substrate temperatures. PHCVD films show good step coverage, but may suffer from low density and molecular contamination as a result of the low deposition temperature.

There are two classes of PHCVD reactors, depending on energy source: a) UV lamp; and b) laser. *UV lamp reactors*¹⁵ generally use mercury vapor for energy transfer between photons and the reactant gases. UV radiation at 2537Å is efficiently absorbed by mercury atoms, which then transfer energy to the reactant species. Deposition rates for UV PHCVD reactors are typically much slower than in other low temperature techniques. *Laser PHCVD reactors*¹⁶ offer the advantages of *frequency tunability* and a high intensity light source. Tunability is useful in that

specific photon energies targeted for particular dissociation reactions can be dialed in, enabling greater control of the deposition reaction. The energy from the high intensity laser also increases reaction rates. Laser PHCVD opens the possibility of CVD *writing* (i.e. patterned deposition by spatial control of the laser). Nevertheless, the deposition rates of current PHCVD processes are still too low to allow them to be adopted for production microelectronic applications.

POLYCRYSTALLINE SILICON: PROPERTIES AND CVD DEPOSITION METHODS

Polycrystalline silicon (also called *polysilicon*, *poly-Si* or *poly*) in thin film form has many important applications in integrated circuit technology. Heavily doped poly-Si films have been widely used as gate electrodes and interconnections in MOS circuits. Poly-Si is utilized in these roles because of its compatibility with subsequent high temperature processing, its excellent interface with thermal SiO₂ (low concentration of interface states), its higher reliability than Al gate materials⁵¹, and its ability to be deposited conformally over steep topography. In some such applications more than one layer of poly-Si is utilized, and a layer of SiO₂ must be thermally grown or deposited on the first layer to electrically isolate it from subsequent layers. More recently, VLSI MOS devices have been fabricated with high conductivity films deposited onto the poly-Si, to create interconnect structures with lower sheet resistances than are possible with poly-Si alone (see Chap. 11 for more information on this subject). Heavily doped poly-Si films are also utilized to form emitter structures in advanced bipolar technologies. Selective growth of poly-Si is being studied as a planarization technique for filling contact holes¹⁷. Lightly doped poly-Si films are used as high-value load resistors in static memories, and to refill trenches employed in dielectric isolation technologies. In this section the properties of poly-Si films and CVD methods for preparing such films are presented.

Properties of Polysilicon Thin Films

Physical Structure and Mechanical Properties of Poly-Si

Thin films of polycrystalline silicon are made up of small (on the order of 1000Å) single crystal regions (*crystallites* or *grains*) separated by grain boundaries. It is of interest to note that *as-deposited* poly-Si films can be amorphous or polycrystalline, but subsequently exhibit a polycrystalline structure if subjected to elevated temperatures after deposition. Polycrystalline silicon films exhibit many mechanical material properties close to those of bulk single-crystal Si (e.g. the density of poly-Si is 2.3 g/cm³, the coefficient of thermal expansion is 2x10⁻⁶/°C, and the temperature coefficient of resistance is 1x10⁻³/°C). The intrinsic stress in thin polysilicon films is compressive (e.g. the stress in 2000-5000Å films is 1-5x10⁹ dynes/cm² *compressive* over the range of doping from undoped material to 10²⁰ atoms/cm³, and annealing temperatures from 250–1100°C)¹⁸. The effect of deposition conditions and post-deposition annealing on poly-Si film structure is discussed in more detail in a later section.

The grain boundaries are composed of disordered atoms, and contain large numbers of defects due to incomplete bonding; while inside each grain, atoms are arranged in a periodic structure. The silicon material in the interior (bulk) of the grains consequently behaves similarly to that of bulk single crystal silicon (e.g. diffusion constants and substitutional impurity properties are assumed to be roughly identical). The defects and departure from periodicity at the grain boundaries, however, substantially alter the behavior of two important material properties of polysilicon, its diffusion characteristics, and its dopant distribution. That is, diffusion

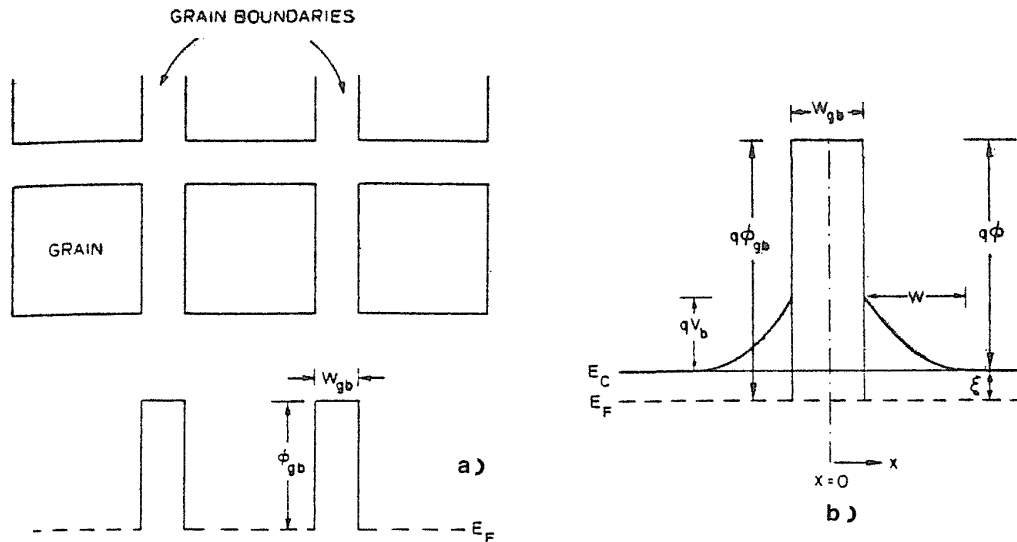


Fig. 10 (a) Schematic representation of potential barriers generated by the grain boundaries. (b) Energy band diagram near a grain boundary under zero applied voltage¹⁹. (© 1981, IEEE).

constants in grain boundary regions are significantly higher than those in single crystal regions. As a result, dopants are capable of diffusing much more rapidly along grain boundaries than through crystallites. Likewise, dopant redistribution is also impacted, as some dopants (e.g. As and P, but not B) exhibit segregation coefficients which favor their moving from single crystal regions into grain boundary regions at low temperatures, and back again at high temperatures¹⁹. See Chap. 4 for an introduction to thin film properties, and Chap. 8 for diffusion in poly-Si.

Electrical Properties of Polysilicon

The electrical properties of poly-Si films are functions of both their semiconductor nature and their polycrystalline structure and doping. That is, single crystal regions of poly-Si are assumed to behave electrically in a manner similar to bulk single crystal silicon. As in single crystal silicon, low resistivity is obtained through heavy doping with impurity atoms.

At a given dopant concentration, polysilicon exhibits significantly higher resistivity than single crystal silicon (except at very high dopant concentrations, where the resistivity is only slightly greater). This is primarily due to two mechanisms: 1) under heat treatment some of the dopant atoms (e.g. As and P, but not B) segregate to the grain boundaries, where they do not effectively produce free carriers. Thus, the concentration of dopant atoms remaining in single crystal regions, and thus still able to contribute charge carriers, is decreased; and 2) the grain boundaries are rich with incomplete bonds, which traps some free carriers at the grain boundaries. Not only does such trapping decrease the overall free carrier concentration, but the trapped charge in the grain boundaries causes local regions of neighboring single crystal material to become depleted of carriers (and creates local potential variations in the material). These changes in potential at grain boundaries (Fig. 10) are detrimental to carrier movement, and also lead to an increase in apparent resistivity. The grain boundary region itself, approximately 5-10 angstroms wide, can be modeled as a separate, amorphous silicon region with increased bandgap. This larger bandgap represents another potential barrier for charge carriers to overcome, although it is so narrow that quantum tunneling effects prevail. Finally, the defects in the grain boundaries decrease the carrier mobility, also causing the resistivity to increase.

Based on the above model for resistivity degradation effects, the behavior of poly-Si

resistivity as a function of dopant concentration and grain size, can be qualitatively understood. First, films with larger grain sizes (at the same dopant concentration) exhibit lower resistivity. That is, since surface area does not increase with grain size as quickly as volume, films with larger grains have proportionally smaller grain boundary densities, and thus less deviation from bulk-silicon resistivity values is observed. Second, grain size and dopant concentration effects interact to determine the degree to which each crystallite is depleted of free charge. Very small grains will become fully depleted more easily than larger grains, and high dopant concentrations result in narrower depleted regions, thus making full depletion of the grains more difficult. If the grains do become completely depleted, the resistivity increases dramatically. As a result, there is a sharp transition region between *very high resistivity*, where grain size is small and /or doping is low and the grains are completely depleted, and *lower resistivity*, where grain size is large and /or doping is high.

In practice, sheet resistances as low as 10-30 Ω /square may be obtained by several techniques (see below) in poly-Si films used in integrated circuits. Note that the work function of poly-Si, important in MOS device threshold voltage values, is also impacted by the doping level.

Chemical Vapor Deposition of Polysilicon

Poly-Si is generally deposited by the pyrolysis (i.e. thermal decomposition) of silane (SiH_4) in the temperature range 580-650°C. The main technique used to deposit poly-Si is LPCVD because of its uniformity, purity, and economy^{20,21}. The deposition reaction sequence is:

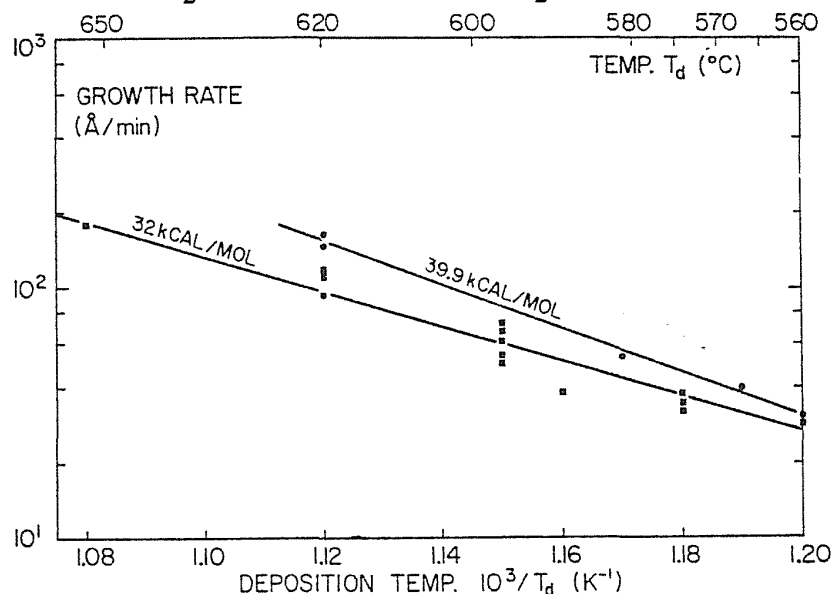
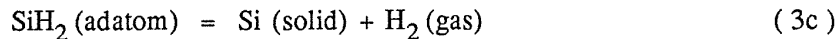
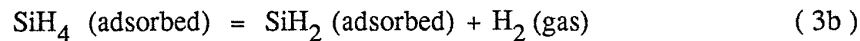
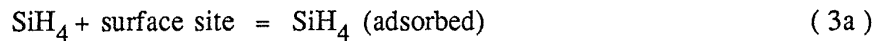
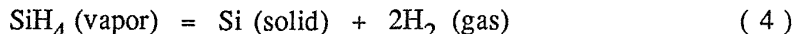


Fig. 11 Growth rate as a function of deposition temperature T_d for two different deposition conditions²⁰. (● 350 mtorr, $\text{SiH}_4 = 200 \text{ cm}^3/\text{min}$ and ■ 120 mtorr, $\text{SiH}_4 = 50 \text{ cm}^3/\text{min}$). Reprinted by permission of the publisher, the Electrochemical Society, Inc.

where adsorption of the SiH_4 is followed by decomposition to an intermediate compound, SiH_2 . Then, upon evolution of the remaining hydrogen, the solid film forms. The overall reaction is generally given as:



Three processes are commonly used in conventional LPCVD systems. The first uses 100% SiH_4 at total pressures from 0.3-1 torr, while the second uses approximately 25% SiH_4 in a nitrogen carrier at approximately the same pressures. A third technique, performed in vertical flow isothermal reactor configurations, uses 25% SiH_4 diluted in hydrogen, also at ~1 torr.

Deposition Parameters

The deposition rate shows an exponential dependence on temperature. Figure 11 is a plot of deposition rate vs. reciprocal temperature. Apparent activation energies are found to depend on the silane pressure and range from 1.36 to 1.7 eV. Depositions are limited to the 580-650°C range, since at higher temperatures gas phase reactions occur (leading to rough and loosely adhering films), and below 580°C the rate is too slow for practical use (<50 Å/min).

The polysilicon deposition rate depends on the silane (SiH_4) pressure as shown in Fig. 12. The dependence is not linear except for low values of pressure. Such behavior may be due to homogeneous reactions, adsorption of hydrogen on the surface sites, or transport phenomena. The total pressure in the reactor can be varied by: a) changing the flow rate of silane at constant pump speed; b) changing the pump speed at constant flow rate; and c) in processes which use diluted silane, by changing the nitrogen flow to adjust the silane concentration. It appears that changing pumping speed to control total pressure provides the best control of deposition rates.

In conventional LPCVD systems it is necessary to ramp the temperature by as much as 30°C from the gas inlet tube end to the outlet. This is done to overcome the effects of the depletion of SiH_4 , and the attendant decrease in deposition rate down the length of the tube. The increased deposition rate resulting from increased temperatures is intended to just compensate for the decrease due to silane depletion. A difficulty with this process is that poly-Si properties depend very strongly on deposition temperature, and will thus vary with wafer position along the tube. A newly designed vertical flow reactor (see section on LPCVD) circumvents this problem.

Polysilicon can be doped during deposition (*in-situ*), or after deposition by diffusion or ion implantation. The addition of diborane to the silane during deposition (boron doping) causes

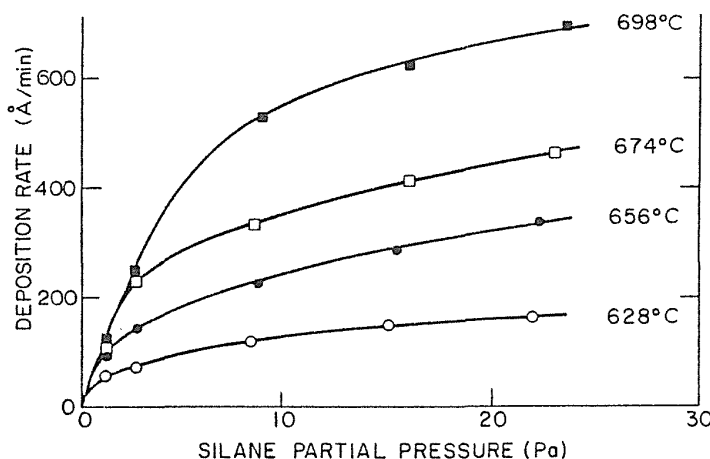


Fig. 12 The effect of silane concentration on the polysilicon deposition rate¹. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted with permission.

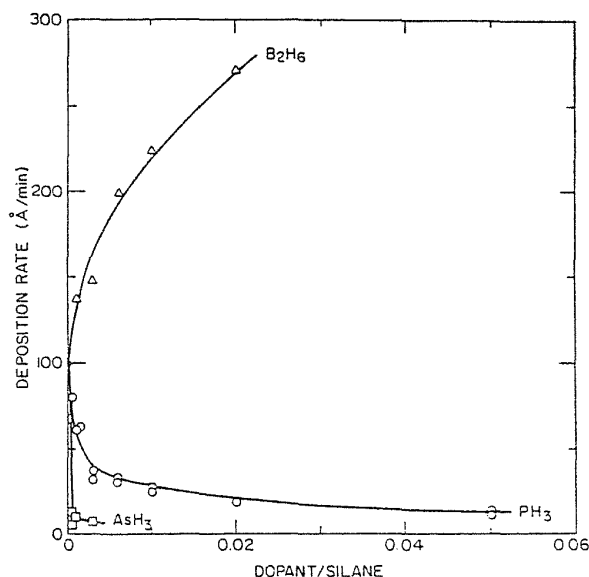


Fig. 13 The effect of dopants on the polysilicon deposition rate at 610°C¹. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted with permission.

rapid increases in the deposition rates, while addition of phosphine or arsine to the silane results in significant growth rate reductions. Figure 13 shows a plot of the deposition rate of polysilicon at 610°C as a function of the volume fraction of dopant added to the silane. *In-situ* doping of polysilicon has not been popular even though it is considerably less complex than post-deposition doping, because of the difficulty of maintaining thickness and doping uniformity from wafer to wafer and across the wafer. Meyerson and Olbricht have shown that the factor of 20 reduction in deposition rate, which is observed when a PH₃/SiH₄ ratio of 1:40 is used, can be attributed to the adsorption of a phosphine layer on the substrate²². This inhibits subsequent silane adsorption and heterogeneous silane decomposition.

Structure of Polysilicon: Deposition Condition Dependence

The structure and properties of poly-Si depend very much on the deposition temperature, the dopant type and concentration, and subsequent thermal cycling. At temperatures below 580°C, the as-deposited film is essentially amorphous²³. At temperatures above 580°C, the films deposit as polycrystalline, with preferred orientation. The {110} fiber axis with columnar grains is dominant in the 625°C range while the {100} predominates in the 675°C range. The {110}-preferred orientation also dominates at higher temperatures²⁴. Harbeke, *et al* found a {311}-preferred orientation for films deposited between 580-600°C²⁰. Films that are recrystallized at 900-1000°C from the amorphous state tend towards a strong {111} fiber texture (Fig. 14). It was also observed that the texture and grain size are exceptionally reproducible in films crystallized from the amorphous phase, and the average grain size is somewhat larger than in the as-deposited polycrystalline film. Figure 15 shows the average grain size of as deposited and recrystallized films (undoped and P-doped). In addition, it was found that as-deposited amorphous films tend to have a smoother surface than do films grown at 600°C (which occasionally show rough surfaces), and films grown at 620°C (which always show surface roughness). The smooth surfaces of the as-deposited amorphous films are maintained even after annealing at 900-1000°C. The penalty paid for achieving smoother surfaces is slower deposition rates at 580°C (~50 Å/min versus 100 Å/min at 600°C). The average grain size

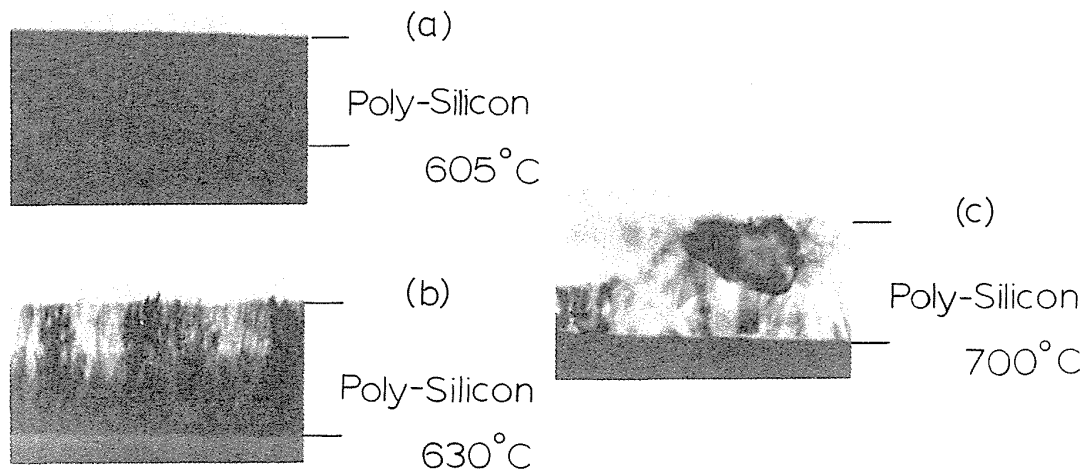


Fig. 14 TEM cross sections (60,000X) of polysilicon. (a) Amorphous structure deposited at 605°C. (b) Columnar structure deposited at 630°C. (c) Crystalline grains formed by annealing an amorphous sample at 700°C¹. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted with permission.

has been observed to increase with film thickness²⁶, and it was also found that the resistivity in boron doped films increases exponentially as thickness decreases.

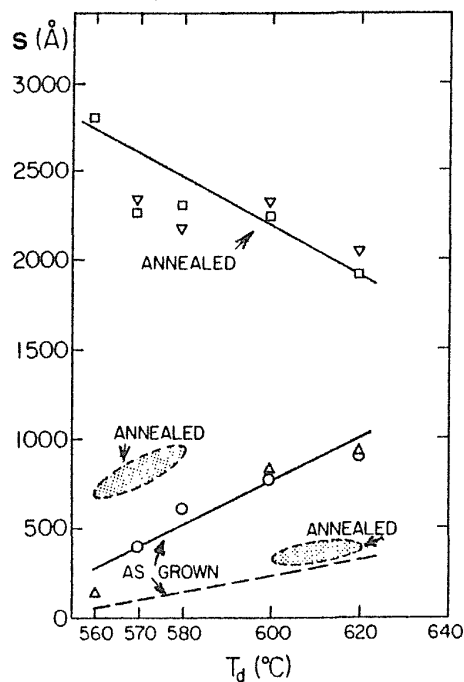


Fig. 15 Average crystallite size S for phosphorus-doped LPCVD silicon layers as-grown ($\circ$ = interface, Δ = surface), and annealed at 1000°C ($\diamond$ = interface, ∇ = surface) as a function of deposition temperature, T_d . Undoped layers (dashed lines) are shown for comparison. From G. Harbeke, *et al.*, RCA Review, 44, 287 (June, 1983).

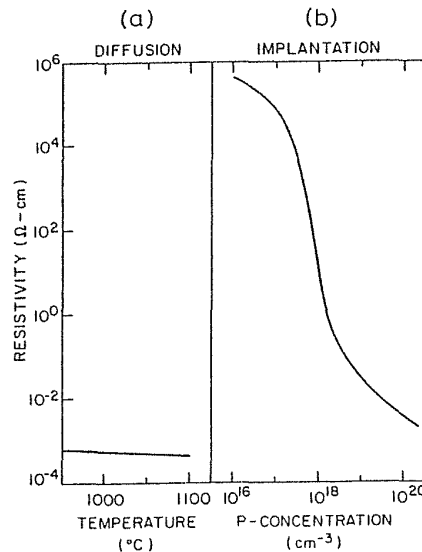


Fig. 16 Resistivity of P-doped polysilicon. (a) Diffusion, 1 h at the indicated temperature²⁵. Reprinted by permission of the publisher, the Electrochemical Society, Inc. (b) Implantation, 1 h anneal at 1100°C¹⁹. (© 1981, IEEE).

Doping Techniques for Polysilicon

Three techniques are used to dope polysilicon: 1) diffusion; 2) ion implantation; and 3) *in situ* doping. In most applications, poly-Si is deposited undoped, and is subsequently doped by diffusion or implantation.

Diffusion Doping of Polysilicon

Diffusion doping (see Chap. 8) is a relatively high-temperature process (900-1000°C) wherein a highly doped glass is grown or deposited on undoped polysilicon, and serves as a solid source for dopant diffusion. The advantage of this method is its ability to introduce very high concentrations of dopants into the poly-Si film (above solid-solubility limits, because of grain-boundary segregation effects), resulting in low resistivity. A high temperature diffusion doping step can also serve double duty as the polysilicon anneal step. Lower final resistivities have been reported for diffusion doping of as-deposited amorphous (low deposition temperature) poly-Si compared to as-deposited polycrystalline poly-Si (Fig. 16a). The disadvantages of diffusion doping are its high temperature and the possibility of increasing film surface roughness.

Ion Implantation Doping of Polysilicon

The second doping technique is ion implantation and subsequent anneal. See Chap. 9 for more on Ion Implantation. This method has the advantage of precise control of dopant dose, and is well suited for applications that do not require a maximally doped polysilicon film (e.g. high value load resistors used in static memories, or doping studies). The resistivity of heavily doped implanted poly-Si is about ten times higher than that of diffusion doped poly-Si (Fig. 16b). The implantation energy is generally selected so that the impurity peak is produced at the center of the film. A subsequent anneal step (e.g. ~900°C, 30 min) redistributes and activates the implanted dopant. Rapid thermal processing (see Chaps. 2 and 9) is also being investigated as an annealing and activating technique²⁸. With the increased diffusion rates of dopants along grain

boundaries, dopant redistribution and activation of implanted polysilicon can be achieved by RTP in less than 30 seconds at 1150°C. The advantage of using RTP is its short duration, which avoids redistributing dopants in the single crystal silicon substrate. Note that ion implantation of poly-Si with As, followed by a rapid-thermal processing step, has also been investigated as a method for forming shallow emitters in advanced bipolar technologies.

In Situ Doping of Polysilicon

In situ doping involves adding doping gases such as diborane and phosphine to the CVD reactant gases⁵⁰. Although combining doping and deposition in one step may appear simple, the control of film thickness, dopant uniformity, and deposition rate is greatly complicated by the addition of the dopant gases. Moreover, the physical properties of the film are affected. Adding phosphine can change the temperature dependence of the polycrystalline film structure, grain size, and grain orientation. In undoped films, it is reported that depositing an initially amorphous film results in superior structural perfection after anneal²¹. Note that for *in-situ* arsenic or phosphorus doped poly-Si, an oxide capping layer must either be deposited or thermally grown before or during the anneal cycle, in order to avoid outdiffusion of the dopant through the top surface of the polysilicon during the anneal. If the deposition temperature is high enough (>600°C) to result in an as-deposited polycrystalline film with sufficiently low resistivity, then the high temperature anneal step may be skipped altogether.

Oxidation of Polysilicon

Polysilicon, like single crystal silicon, can be thermally oxidized. Its oxidation rate depends on grain orientation, dopant type, and dopant concentration. In general, lightly doped poly-Si oxidizes more rapidly in wet O₂ than {111} or {100} single crystal silicon²⁹. Polysilicon heavily-doped with phosphorus oxidizes more rapidly than undoped poly-Si, but not as rapidly as heavily-doped single crystal Si²⁸. The ratio of poly-Si consumed during oxidation, to the thickness of the oxide, is about the same as in single-crystal Si (1:1.56).

Of particular importance in some applications (especially in which a double-poly, or even triple-poly structure is used) is that SiO₂ thermally grown on the poly-Si exhibits adequate breakdown strength. This strength is strongly influenced by the smoothness of the polysilicon surface prior to oxidation. That is, a rough surface leads to high local electric fields and lower oxide dielectric strength. Again, low temperature poly-Si depositions (<600°C) have been reported to produce smoother surfaces and grown oxides with higher breakdown voltages than obtained under higher temperature depositions. Another technique reported to increase the smoothness of the poly-Si /SiO₂ interface is to grow the oxide at higher temperatures. It is believed that the viscous flow of the oxide can moderate the surface roughness produced by oxidation. A method for reducing leakage and increasing the breakdown strength of oxides grown on phosphorus-doped poly-Si is to dope it to an optimum level ($\sim 6 \times 10^{20} \text{ cm}^{-3}$), with a high temperature anneal in an inert ambient ($\sim 1100^\circ\text{C}$, 10 min, N₂) prior to a 950°C oxidation³⁰. This is thought to improve interface flatness by phosphorus-enhanced grain growth during the anneal.

PROPERTIES AND DEPOSITION OF CVD SiO₂

Chemical vapor deposited (CVD) SiO₂ films, and their binary and ternary silicates, find wide use in VLSI processing. These materials are used as insulation between polysilicon and metal layers, between metal layers in multilevel metal systems, as getters, as diffusion sources, as diffusion and implantation masks, as capping layers to prevent outdiffusion, and as final

Table 2. PROPERTIES OF CVD AND THERMAL SILICON DIOXIDE¹

FILM TYPE:	THERMAL	PECVD	APCVD	SiCl ₂ H ₂ +N ₂ O	TEOS
Deposition Temp. (°C):	800-1200	200	450	900	700
Step Coverage:	conformal	good	poor	conformal	conformal
Stress (x10 ⁹ dynes/cm ²):	3C	3C-3T	3T	3T	1C
Dielectric Strength (10 ⁶ V/cm):	3 - 6	8	10	10	
Etch Rate (Å /min): (100:1, H ₂ O:HF)		400	60	30	30

passivation layers. In general, the deposited oxide films must exhibit uniform thickness and composition, low particulate and chemical contamination, good adhesion to the substrate, low stress to prevent cracking, good integrity for high dielectric breakdown, conformal step coverage for multilayer systems, low pinhole density, and high throughput for manufacturing.

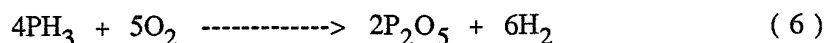
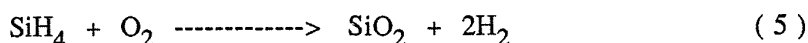
CVD silicon dioxide is an amorphous structure of SiO₄ tetrahedra with an empirical formula SiO₂. (See Chap. 7, section on *Properties of Silica Glass*.) Depending on the deposition conditions, as summarized in Table 2, CVD silicon dioxide may have lower density and slightly different stoichiometry from thermal silicon dioxide, causing changes in mechanical and electrical film properties (such as index of refraction, etch rate, stress, dielectric constant and high electric-field breakdown strength). Deposition at high temperatures, or use of a separate high temperature post-deposition anneal step (referred to as *densification*) can make the properties of CVD films approach those of thermal oxide.

Deviation of the CVD silicon dioxide film's refractive index, *n*, from that of the thermal SiO₂ value of 1.46 is an often used as an indicator of film quality. A value of *n* greater than 1.46 indicates a silicon rich film, while smaller values indicate a low density, porous film. CVD SiO₂ is deposited with or without dopants, and each type has unique properties and applications.

Chemical Reactions for CVD SiO₂ Formation

There are various reactions that can be used to prepare CVD SiO₂. The choice of reaction is dependent on the temperature requirements of the system, as well as the equipment available for the process. The deposition variables that are important for CVD SiO₂ include: temperature, pressure, reactant concentrations and their ratios, presence of dopant gases, system configuration, total gas flow, and wafer spacing. There are three temperature ranges in which SiO₂ is formed by CVD, each with its own chemical reactions and reactor configurations. These are: 1) low temperature deposition (300-450°C); 2) medium temperature deposition (650-750°C); and 3) high temperature deposition (~900°C).

The *low temperature deposition* of SiO₂ utilizes a reaction of silane and oxygen to form undoped SiO₂ films. The depositions are carried out in APCVD reactors (primarily of the continuous belt type), in distributed feed LPCVD reactors, or in PECVD reactors. The depletion effect precludes the use of conventional LPCVD for the SiH₄ + O₂ reaction. The addition of PH₃ to the gas flow forms P₂O₅, which is incorporated into the SiO₂ film to produce a phosphosilicate glass (PSG)³¹. The reactions are given by:

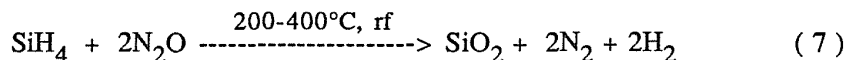


The reaction between silane and excess oxygen forms SiO_2 by heterogeneous surface reaction. Homogeneous gas-phase nucleation also occurs, leading to small SiO_2 particles that form a white powder on the reaction chamber walls (and which may potentially cause particulate contamination in the deposited films).

The deposition rate increases slowly with increased temperature between 310 and 450°C. An apparent activation energy of less than 0.4 eV has been measured which is indicative of a surface adsorption or gas phase diffusion deposition process. The deposition rate can be increased at constant temperature (up to a limit) by increasing the O_2 : SiH_4 ratio. Continued increase in the ratio eventually results in a decrease in deposition rate, as a result of O_2 being adsorbed on the substrate, thus inhibiting the SiH_4 decomposition.

Silicon dioxide films deposited at low temperatures exhibit lower densities than thermal SiO_2 , and have an index of refraction of ~ 1.44 . They also exhibit substantially higher etch rates in buffered hydrofluoric acid (HF) solutions than thermal SiO_2 . Subsequent heating of such films to temperatures between 700-1000°C causes *densification*. That is, this step causes the density of the material to increase from 2.1 g/cm³ to 2.2 g/cm³, the film thickness to decrease, and the etch rate in HF to decrease.

SiO_2 can also be deposited by a plasma enhanced reaction between SiH_4 and N_2O (nitrous oxide) or O_2 at temperatures between 200-400°C³²:

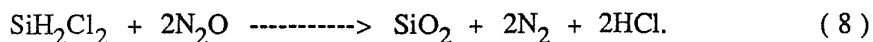


Nitrogen and/or hydrogen is often incorporated in PECVD SiO_2 . A low ratio of N_2O / SiH_4 will increase the index of refraction, due to large amounts of nitrogen incorporated in the film and the formation of silicon rich films. Nearly stoichiometric ($n = 1.46$) plasma oxide films can be achieved by reacting SiH_4 and O_2 mixtures. The buffered HF etch rate is a sensitive measure of the film's stoichiometry and density. Lower deposition temperatures and higher N_2O / SiH_4 ratios lead to less dense films and faster etch rates. As with nitride films, PECVD oxides also contain 2-10 at% H_2 in the form of Si-H, Si-O-H, and H-O-H³². The hydrogen concentration is a strong function of the deposition parameters. Low deposition temperatures, high rf power, and high carrier-gas flow rates are required to prevent gas phase nucleation and its attendant particulate problems.

Plasma oxide films are generally deposited in compressive stress, with values ranging between 1×10^8 - 4×10^9 dynes/cm², depending on deposition temperature and rate. Dielectric strengths of 4 - 8×10^6 V/cm, and dielectric constants ranging from 4-5 have been obtained. Low pinhole counts have been obtained with PECVD oxides, as have very conformal coatings. Adhesion to metal is also reported to be excellent³⁴.

In the *medium temperature range*, SiO_2 is deposited in LPCVD reactors by decomposing tetraethoxysilane, $\text{Si}(\text{OC}_2\text{H}_5)_4$, also known as *tetraethyl orthosilicate*, or *TEOS*. The deposition rate for TEOS shows an exponential increase with temperature in the range of 650-800°C with an apparent activation energy of 1.9 eV³³. This pronounced temperature dependence can lead to thickness control problems. The deposition rate is also dependent on the TEOS partial pressure. It is linearly dependent at low partial pressures, and tends to level off as the adsorbed TEOS saturates the surface. TEOS films generally show excellent conformality.

At *high temperatures* (near 900°C) SiO_2 is formed by an LPCVD process in which dichlorosilane and nitrous oxide are reacted⁸. The reaction is given by:



Such depositions produce films having excellent uniformity, and with properties close to those of thermal SiO_2 . High-temperature LPCVD is sometimes used to deposit SiO_2 over poly-Si.

Step Coverage of As-Deposited CVD SiO_2 Films

The manner in which a thin film covers (or conforms to) the underlying features on a substrate is an important characteristic of a deposited film. Film conformality of CVD films is a function of film species and reactor type, and deposition conditions. *Conformal coverage* is coverage in which equal film thickness exists over all substrate topography regardless of its slope (i.e. vertical and horizontal surfaces are coated with equal film thickness, Fig. 17a). The thickness of deposited films at any given point in the mass-transport limited case is dependent on the supply of reactants to that point, which itself is set by process pressure and adatom migration. The following model has been proposed to explain step coverage in terms of these parameters¹.

If adsorbed reactants are able to migrate rapidly across a substrate surface, they will be found with equal probability on any part of the substrate, regardless of topography. This situation results in conformal step coverage, as shown in Fig. 17a. Adatom mobility is a function of adatom species and energy. Both higher substrate temperature and ion bombardment of adatoms enhance adatom migration. Note that under the relatively high temperature conditions used to deposit LPCVD poly-Si and Si_3N_4 films, excellent (i.e. highly conformal) step coverage is usually achieved. Thus, only SiO_2 step coverage need be further considered in this discussion.

If on the other hand, reactant surface migration is slow, then the arrival flux of gaseous reactants at a given point becomes more important in determining the local film thickness. In such cases, it is useful to introduce the concept of the *arrival angle* to help model step coverage. That is, the flux of reactant molecules arriving from an angle between θ and $\theta + d\theta$ can be expressed as $P(\theta) d\theta$ (in a 2-dimensional analysis). Then the total flux arriving at any

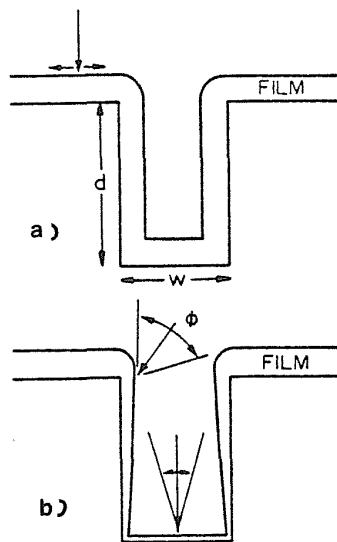


Fig. 17 Schematic diagrams showing types of step coverage. (a) Conformal coverage resulting from rapid surface migration; (b) Non-conformal coverage caused by no surface migration³³. Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet.

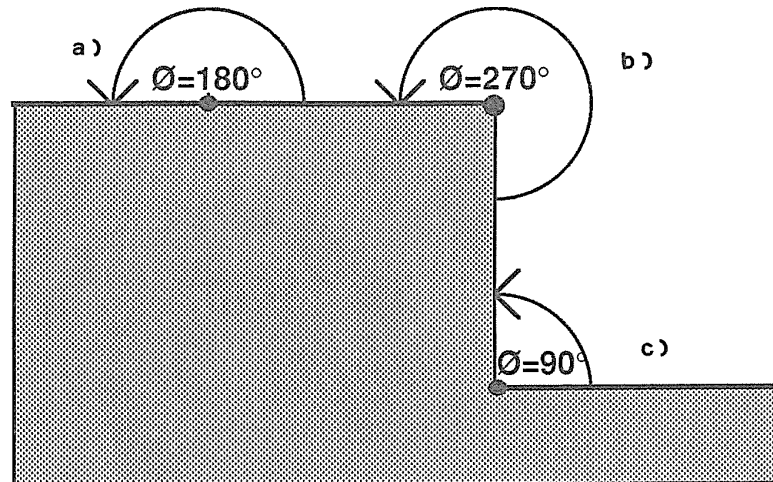


Fig. 18 The concept of *arrival angle* and its effect on step coverage. (a) 180° (b) 270° (c) 90° .

point is $\int_0^{2\pi} P(\theta) d\theta$. For an atmospheric pressure reactor, the mean free path for reactant gas molecules is short, and the frequent collisions of gas molecules with each other completely randomize their velocity vectors. Under such conditions, $P(\theta)$ is a constant, independent of the value of θ . However, $P(\theta)$ is zero for values of θ which are blocked by the substrate. For example, in Fig. 18a, $P(\theta)$ is zero for any angle from 180 - 360° , and constant for $0^\circ < \theta < 180^\circ$.

In short, the value of the flux integral (and thus the eventual film thickness), is directly proportional to the range of angles for which $P(\theta)$ is not zero. This range is called the *arrival angle*. As seen in Fig. 18b, at the top corner of a step, $P(\theta)$ is non-zero over a range of 270° . The resultant film thickness is $270/180$, or 1.5 times greater than for the planar case of Fig. 18a. Similarly in Fig. 18c (i.e. at the bottom corner of a step, or trench) the arrival angle is only 90° , and the film thickness is $90/180$, or one-half that of the planar case. This explains the thickness cross-section that is observed when APCVD SiO_2 is deposited over a sharp step (Fig. 19a). The film is thickest at the upper corner and thinnest at the bottom of the step. This causes the slope in SiO_2 films at the bottom corner to be $>90^\circ$ (i.e. a so-called *re-entrant angle*) making deposition and anisotropic etching of subsequently deposited films extremely difficult.

On the other hand, if the mean free path of the reactant gases is high (e.g. due to the low operating pressure of LPCVD and PECVD reactors), a *shadowing* effect can occur. That is, no longer do frequent collisions over very small distances randomize the gas molecule velocity vectors. Instead, reactant molecules experience few collisions, and follow straight line trajectories over distances comparable to substrate topography dimensions. Substrate surface features near to points being impinged upon can block the straight paths of reactant molecules. Thus such points can be *shadowed* from the reactant flux, and will experience less deposition, and thus less resulting film thickness, than those points which are not shadowed. The arrival angle for the given point now depends on the range of unobstructed *lines of sight* from that point to the reaction chamber (see Fig. 17b). In such long mean free path cases the arrival angle, and thus film thickness, decreases with depth into a trench (as shown in Fig. 17c).

The reactor type and deposition conditions impact step coverage insofar as reactant gas mean free path and adatom migration is affected. The reactor operating pressure determines mean free path lengths, while adatom migration is affected by substrate temperature and also by energy transfer method. For example, due to rapid surface migration, SiO_2 films prepared by TEOS

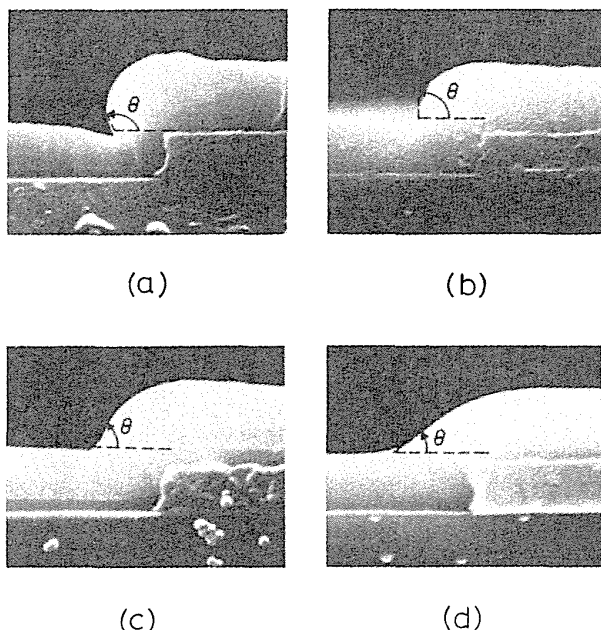


Fig. 19 SEM cross-sections (10,000X) of samples annealed in steam at 1100°C for 20 min for the following weight of phosphorus: (a) 0.0 wt.% P; (b) 2.2 wt.% P; (c) 4.6 wt.% P; 7.2 wt.% P.³³ Reprinted by permission of the publisher, the Electrochemical Society, Inc.

decomposition, or by the high temperature reaction of $\text{SiCl}_2\text{H}_2\text{-N}_2\text{O}$ under LPCVD conditions, exhibit nearly conformal coverage. Conversely, during low temperature deposition of SiO_2 by APCVD, almost no surface migration takes place, and step coverage is dependent only on the arrival angle (and is quite poor, as noted earlier). On the other hand, PECVD produces reactants which arrive at the substrate with more energy (obtained from the glow-discharge) than in APCVD. This results in increased adatom migration. Thus, improved step coverage by PECVD SiO_2 films can be obtained compared to APCVD depositions made at the same temperature. Note that the mechanisms of this model can also be applied to analyzing the step coverage effects seen in evaporated and sputtered films.

CVD and Applications of Undoped and Doped SiO_2 Films

Both undoped and doped films of SiO_2 are easily deposited at low temperatures. Doping of TEOS and high temperature CVD SiO_2 films is more difficult. As we shall see, doping of the SiO_2 can produce a variety of desirable film properties for some applications.

Undoped CVD SiO_2

Undoped CVD SiO_2 is similar to its thermally grown counterpart in many respects, with some exceptions being its as-deposited density and etch rate, and a lower quality SiO_2 /Si interface (higher density of interface states). Due to its poor interface qualities, CVD SiO_2 is therefore only used as a temporary structure if it is used in contact with single crystal silicon (e.g. as a capping layer over doped regions to prevent outdiffusion during thermal processes or as an ion-implantation mask). Its chief use, however, is as a permanent structure, whose function

is to increase the thickness of field oxides, or to provide isolation between conductors.

When the underlying conductor is able to withstand high temperatures (e.g. polysilicon or refractory metal silicides) one of the LPCVD methods may be utilized, because of their excellent uniformity, good step coverage, low particulate contamination, and high purity.

Often the film must be deposited over aluminum, and therefore the process must take place at less than 450°C. At these temperatures LPCVD reactions exhibit extremely low deposition rates (Fig. 20b). On the other hand the reaction of silane and oxygen mixtures at atmospheric pressure and temperatures from 300-500°C provides adequately high deposition rates. Therefore such APCVD processes are widely used, despite their particulate and step coverage problems. Undoped oxide can also be deposited by PECVD techniques, with generally improved step coverage as compared to APCVD.

Phosphosilicate Glass

Adding phosphorus dopant during the deposition, typically in the form of phosphine, PH_3 , forms phosphosilicate glass, or PSG. Since PSG consists of two compounds, P_2O_5 and SiO_2 , it is a *binary glass* (or binary silicate), and some of its properties are considerably different from those of undoped CVD SiO_2 . That is, APCVD PSG shows reduced stress and somewhat improved, though still relatively poor, step coverage as compared to undoped CVD SiO_2 . Moreover PSG is a diffusion barrier to moisture, and getters alkali ions. Finally PSG can be *flowed* at high temperatures to create a smoother surface topography, and thereby facilitate the step coverage of subsequently deposited films. The flow step is performed at 1000-1100°C, at pressures from 1-25 atm, and in gas ambients of H_2O , N_2 and O_2 . The glass becomes viscous and responds to surface tension forces, rounding sharp corners. The extent of flow is often measured as the reduction in slope angle of the flowed film surface over an underlying step (Fig. 19), and is a function of flow temperature and phosphorus concentration. Increasing temperature, duration of the flow step, or phosphorus concentration in the oxide will increase film flow. Note that for concentrations less than 6 wt% phosphorus, PSG does not readily flow.

It is relatively easy to incorporate the P_2O_5 into the PSG, as the $\text{SiH}_4:\text{PH}_3$ ratio in the gas flow controls the $\text{SiO}_2:\text{P}_2\text{O}_5$ ratio in the deposited film. PSG, however, becomes increasingly hygroscopic at high phosphorus levels. Thus, it is recommended that its concentration in the oxide film be limited to 6-8 wt% P to minimize phosphoric acid formation, and consequent Al corrosion. Rapid thermal processes have also been reported to successfully flow PSG. It should be noted, however, that if PSG is to be used as a final passivation layer (in which no glass flow

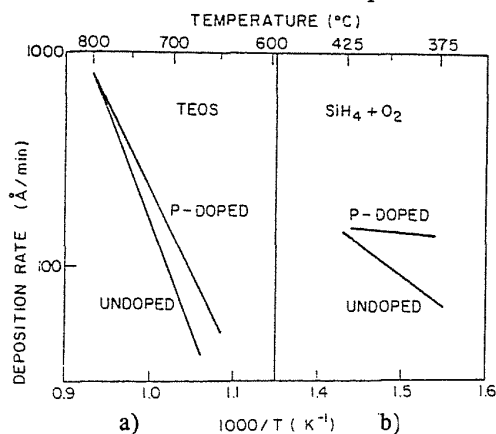


Fig. 20 Arrhenius plots for the deposition of (a) LPCVD TEOS, and (b) LPCVD SiO_2 (P-doped and undoped)³³. Reprinted with permission of the publisher, the Electrochemical Society, Inc.

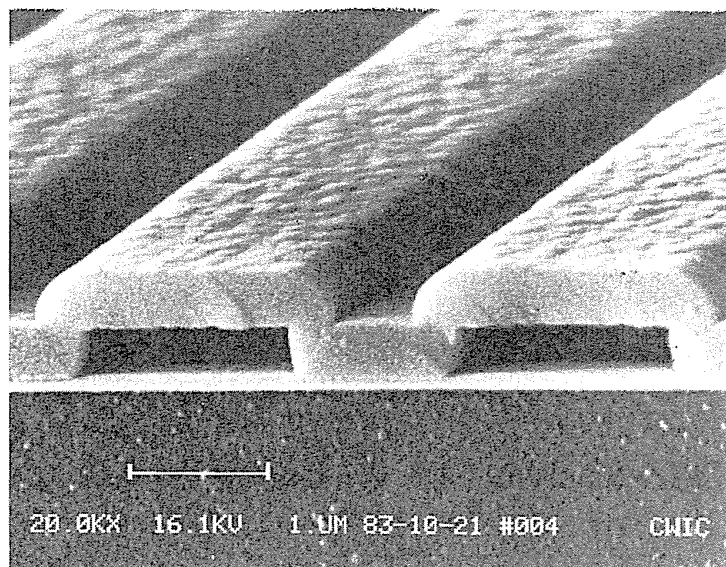


Fig. 21 SEM of PECVD oxide over polysilicon lines. Poly has been removed by wet etch to show detail¹². Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet.

is performed), the maximum permitted phosphorus content is 6 wt%. This is a precaution taken to again minimize the risk of phosphoric acid formation, particularly when in contact with Al.

PSG has been deposited in PECVD systems by the reaction of SiH_4 , N_2 , O_2 , and PH_3 with Ar as a carrier gas. It is reported that the films are more conformal (Fig. 21), crack resistant, and pinhole free than APCVD films³⁴. The phosphorus content is a function of the SiH_4/PH_3 ratio, deposition temperature and $\text{N}_2\text{O}/(\text{SiH}_4 + \text{PH}_3)$ ratio³⁵. The plasma PSG films can be flowed under conditions similar to those for flowing APCVD PSG films.

Borophosphosilicate Glass

Some VLSI processes would benefit from being performed at lower temperatures than those necessary for PSG reflow (1000-1100°C) because such high temperatures result in excessive diffusion of shallow junctions. Furthermore, radiation-hard MOS gate oxides cannot be exposed to high temperature processing (>900°C). But flowable glass is still very desirable for easing film coverage over abrupt steps in the substrate topography. Glass flow temperatures as low as

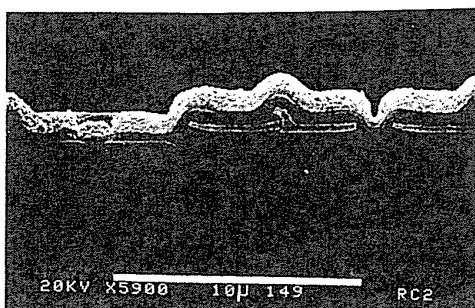


Fig. 22 Micrographs showing BPSG as the interlevel dielectric under the metal. Reprinted with permission of Semiconductor International².

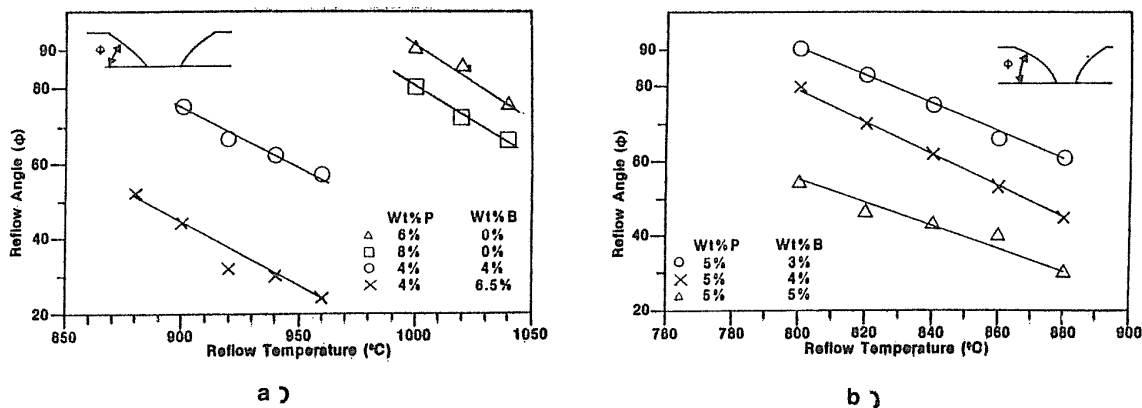


Fig. 23 (a) Reflow angle vs. reflow temperatures in a nitrogen ambient (30 min). (b) Reflow angle vs. reflow temperatures in a steam ambient (30 min). Reprinted by permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet³⁷.

700°C can be obtained by adding boron dopant (e.g. B_2H_6) to the PSG gas flow to form the ternary (three component) oxide system B_2O_3 - P_2O_5 - SiO_2 , borophosphosilicate glass, or BPSG³⁶ (Fig. 22).

BPSG flow depends upon film composition, flow temperature, flow time, and flow ambient. It has been reported that an increase in boron concentration of 1 wt% in BPSG decreases the required flow temperature by $\sim 40^\circ C$ ³⁶. A plot of required flow temperatures vs. BPSG dopant concentrations in LPCVD films is shown in Fig. 23. In general, increasing the P concentration beyond ~ 5 wt% does not further decrease BPSG flow temperatures. An upper limit on boron concentration is imposed by film stability. That is, BPSG films containing over 5 wt% boron tend to be very hygroscopic and unstable, and if used, should be flowed immediately following deposition. It has also been reported that rapid thermal annealing for 30 s at a temperature 100-175°C higher than that used in a conventional furnace step will result in equivalent BPSG flow³⁶. The ambient gas of the flow cycle also affects the flow mechanism. By using a steam ambient instead of N_2 , the minimum required flow temperature is reduced by $\sim 70^\circ C$ ³⁷.

In addition to exhibiting these low temperature flow properties, BPSG (like PSG) is an alkali ion getter and exhibits low stress. Because of its doping, however, BPSG can also be an unwanted diffusion source to underlying silicon. It is found that BPSG is primarily a source of phosphorus, and the phosphorus outdiffusion is increased at higher boron concentrations.

Besides being useful for isolation, passivation, and surface planarization, BPSG is also more attractive for use than PSG in a process known as *contact reflow*. Following anisotropic etching, contact holes have sharp upper corners which make them difficult to fill (Fig. 24a). By successfully rounding these sharp edges with a *second* thermal flow (or *reflow*) cycle (Fig. 24b), contact coverage by a subsequent metal film is significantly improved. (Note that two separate flow cycles are preferred to a single post-etch flow cycle, since the appropriate degree of flow desired in the second cycle is normally less than that required for the first flow step). The ambient is also usually inert, rather than oxidizing, in order to avoid SiO_2 growth in the contacts during the reflow step. Because flow depends on BPSG composition, precise control of dopant uniformity across substrates is necessary to ensure uniform flow and consequent control of contact size.

BPSG deposition reactions for APCVD⁴, LPCVD³⁸, and PECVD^{39, 40} processes have all been reported. If hot-wall LPCVD reactors are used, they must be equipped with distributed feed gas systems so that adequately uniform BPSG films can be deposited. During deposition, the

source gases for B and P compete with one another for inclusion into the final deposited film. This makes for a complex relation of reactant gas composition to eventual film doping³⁶.

The chemical composition of BPSG (and PSG), can be determined by several techniques, including the following: a) *wet chemical colorimetry*, which is the most accurate, analyzes the dissolved BPSG film; b) *x-ray photoelectron spectroscopy* (see Chap. 17), which is useful for determining the phosphorus content of the film; c) *Fourier transform infrared spectroscopy* (see Chaps. 1 and 5) which can measure boron levels quite accurately, but phosphorus levels less well accurately (due to the presence of a partially obscured phosphorus-oxygen absorption band); and d) *film etch rates in buffered HF*. Since the etch rate of BPSG in buffered HF depends on the concentration of both B and P in the film, a determination of the etch rate can provide a rapid, qualitative comparison of the composition between BPSG samples.

PROPERTIES AND CHEMICAL VAPOR DEPOSITION OF SILICON NITRIDE

Silicon nitride films are amorphous insulating materials that find three main applications in VLSI fabrication: 1) as final passivation and mechanical protective layers for integrated circuits, especially for parts encapsulated in plastic packages; 2) as a mask for the selective oxidation of silicon; and 3) as a gate dielectric material in MNOS devices. Silicon nitride also has a high dielectric constant (6-9 vs ~4.2 for CVD SiO₂), making it less attractive for interlevel insulation, because of the resultant higher capacitance between conductor layers.

Silicon nitride is highly suitable as a *passivation layer* because of its following properties: a) it behaves as a nearly impervious barrier to diffusion (in particular, moisture and sodium find it very difficult to diffuse through the nitride film); b) it can be prepared by PECVD to have a low compressive stress, which allows it to be subjected to severe environmental stress with less likelihood of delamination or cracking; c) its coverage of underlying metal is conformal; and d) it is deposited with acceptably low pinhole densities.

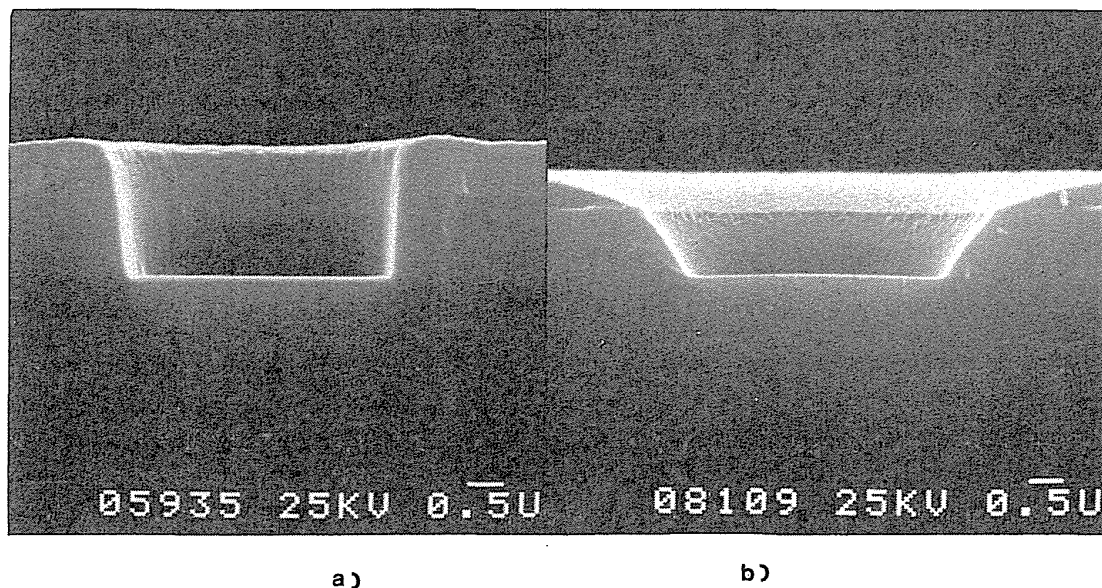


Fig. 24 (a) SEM of dry-etched contact window before reflow. (b) Reflowed BPSG film with 4 wt% P and 4 wt% B. Reflow was 930°C in N₂ for 25 min³⁷. Courtesy of Applied Materials, Inc.

Silicon nitride is useful as a *masking layer for selective oxidation*⁴⁴, since oxygen also finds it difficult to penetrate silicon nitride. That is, silicon nitride is deposited directly on a silicon substrate (actually onto a thin, thermal stress-relief SiO₂ layer, called a *pad oxide*) and patterned. The wafer is then subjected to an oxidation step. The silicon nitride itself oxidizes very slowly, but is not penetrated by the oxygen. As a result it protects the underlying Si from oxidizing, while allowing a thermal SiO₂ layer to grow on regions of exposed Si. For example, at 1000°C in steam for 10 hours, only a few hundred Å of silicon nitride is converted to SiO₂, while more than 1 µm of SiO₂ can be grown on the exposed silicon. The silicon nitride is removed after the oxidation step.

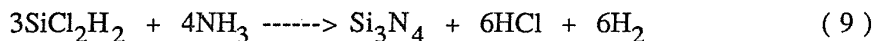
As shown in Table 3, two techniques are used for depositing silicon nitride. When used as a mask for selective oxidation or as a gate dielectric material in MNOS structures, silicon nitride is generally deposited by high-temperature (700-800°C) LPCVD techniques, for reasons of film uniformity and lower processing cost^{8,31}. When used as a passivation layer, the deposition process must be compatible with such low-melting-point metals as aluminum. Thus silicon nitride must be deposited by a low temperature process (300-400°C). For such applications PECVD is the deposition method of choice, as it can deposit nitride films at 200-400°C^{32,43,44}. PECVD silicon nitride, however, tends to be nonstoichiometric, and

Table 3. Properties of PECVD Silicon Nitride and High Temperature CVD Nitride

Property	HT-CVD—NP 900°C	PE-CVD—LP 300°C
Composition	Si ₃ N ₄	Si _x N _y H _z
Si/N ratio	0.75	0.8–1.0
Density	2.8–3.1 g/cm ³	2.5–2.8 g/cm ³
Refractive index	2.0–2.1	2.0–2.1
Dielectric constant	6–7	6–9
Dielectric strength	1 × 10 ⁷ V/cm	6 × 10 ⁶ V/cm
Bulk resistivity	10 ¹⁵ –10 ¹⁷ ohms/cm	10 ¹⁵ ohms/cm
Surface resistivity	> 10 ¹³ ohms/square	1 × 10 ¹³ ohms/square
Stress at 23°C on Si	1.2–1.8 × 10 ¹⁰ dyn/cm ² (tensile)	1–8 × 10 ⁹ dyn/cm ² (compressive)
Thermal expansion	4 × 10 ⁻⁶ /°C	> 4 < 7 × 10 ⁻⁶ /°C
Color, transmitted	None	Yellow
Step coverage	Fair	Conformal
H ₂ O permeability	Zero	Low–none
Thermal stability	Excellent	Variable > 400°C
Solution etch rate		
HFB 20–25°C	10–15 Å/min	200–300 Å/min
49% HF 23°C	80 Å/min	1500–3000 Å/min
85% H ₃ PO ₄ 155°C	15 Å/min	100–200 Å/min
85% H ₃ PO ₄ 180°C	120 Å/min	600–1000 Å/min
Plasma etch rate		
70% CF ₄ /30% O ₂ , 150 W, 100°C	200 Å/min	500 Å/min
Na ⁺ penetration	< 100 Å	< 100 Å
Na ⁺ retained in top 100 Å	> 99%	> 99%
IR absorption		
Si–N max	~ 870 cm ⁻¹	~ 830 cm ⁻¹
Si–H minor	—	2180 cm ⁻¹

contains substantial quantities of atomic H (10-30 at%). For this reason it is sometimes chemically represented as $\text{Si}_x\text{N}_y\text{H}_z$. Comparison of the refractive index of CVD silicon nitride with that of thermal silicon nitride gives a quick estimate of the stoichiometry of the CVD film. Higher refractive indices indicate silicon rich films. Table 3 compares the properties of LPCVD and PECVD silicon nitride films.

LPCVD silicon nitride is formed by reacting dichlorosilane (SiCl_2H_2) and ammonia (NH_3) at temperatures between 700-800°C according to the overall reaction:



Silicon nitride depositions by LPCVD are controlled by a large number of deposition parameters including, temperature, total pressure, reactant ratios, and temperature gradients in the reactor. The deposition rate increases with increasing total pressure, or SiCl_2H_2 partial pressure, but decreases as the $[\text{NH}_3] : [\text{SiCl}_2\text{H}_2]$ ratio gets larger. A temperature ramp, as discussed in the section on hot-wall tube LPCVD reactors, is required for obtaining uniform depositions. In general, LPCVD silicon nitride films have a high density (2.9-3.1 g/cm³), a dielectric constant of 6, and are more stoichiometric than PECVD silicon nitride films. Their etch rate in buffered HF is very slow (less than 10 Å/min), and their hydrogen content (up to 8 at%) is less than in PECVD films. In addition, they exhibit excellent step coverage and relatively low particulate contamination. Such films, however, have tensile stresses of $\sim 1 \times 10^{10}$ dynes/cm², which is about an order of magnitude higher than that of TEOS-deposited SiO_2 . This may cause LPCVD silicon nitride films greater than $\sim 2000\text{Å}$ to crack. Sufficient NH_3 is also needed to insure that all of the SiH_4 is consumed. If insufficient NH_3 is available, the films become silicon rich. As a result, depositions are usually carried out with significant excess flow of NH_3 . It should also be mentioned that, as described in Chap. 7, an anneal in hydrogen is often performed on MOS circuits to reduce the interface trapped charge density, Q_{it} , after the final Al layer is deposited and patterned. Since silicon nitride is such an impervious diffusion barrier, this anneal must be performed on wafers prior to depositing a silicon nitride passivation layer.

Silicon nitride deposition by PECVD was described by Sterling and Swann in 1965. The

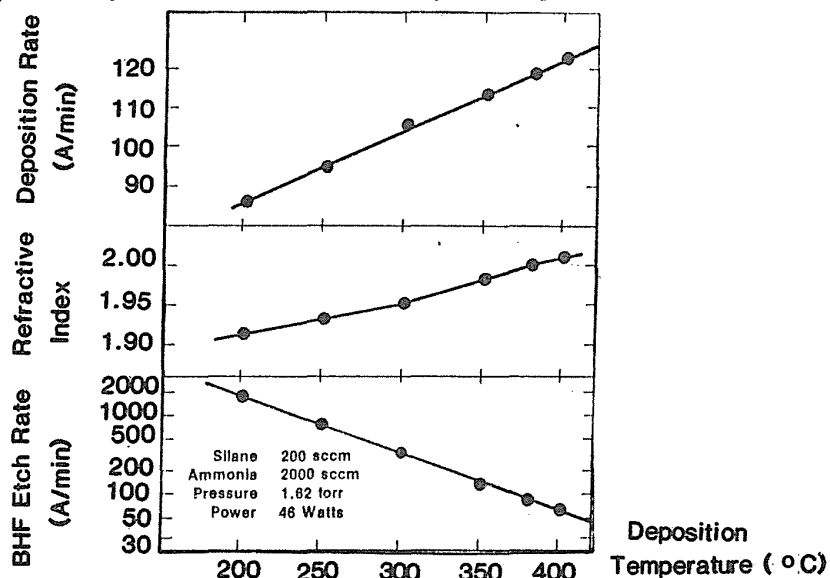
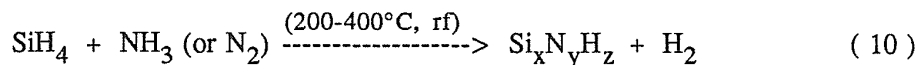


Fig. 25 Effect of deposition temperature on PECVD nitride parameters. Reprinted by permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet¹².

Table 4. CVD DEPOSITION REACTIONS

PRODUCT	REACTANTS	METHOD	TEMP (°C)	COMMENTS
Polysilicon	SiH ₄	LPCVD	580-650	may be <i>in situ</i> doped
Silicon Nitride	SiH ₄ + NH ₃	LPCVD	700-900	
	SiCl ₂ H ₂ + NH ₃	LPCVD	650-750	
	SiH ₄ + NH ₃	PECVD	200-350	
	SiH ₄ + N ₂	PECVD	200-350	
SiO ₂	SiH ₄ + O ₂	APCVD	300-500	poor step coverage
	SiH ₄ + O ₂	PECVD	200-350	good step coverage
	SiH ₄ + N ₂ O	PECVD	200-350	
	Si(OC ₂ H ₅) ₄ [TEOS]	LPCVD	650-750	liquid source, conformal
	SiCl ₂ H ₂ + N ₂ O	LPCVD	850-900	conformal
Doped SiO ₂	SiH ₄ + O ₂ + PH ₃	APCVD	300-500	PSG
	SiH ₄ + O ₂ + PH ₃	PECVD	300-500	PSG
	SiH ₄ + O ₂ + PH ₃ + B ₂ H ₆	APCVD	300-500	BPSG, low temperature flow
	SiH ₄ + O ₂ + PH ₃ + B ₂ H ₆	PECVD	300-500	BPSG, low temperature flow

overall deposition reaction is written as:



where silane and ammonia or nitrogen are reacted in a plasma at 200-400°C. The use of a high (100-1000:1) N₂: SiH₄ ratio is required to prevent silicon rich film formation (since the N₂ dissociation rate is much lower than that of silane). On the other hand, NH₃ dissociates much more readily, and thus lower NH₃: SiH₄ ratios can be used (e.g. 5-20:1).

The deposition rate depends strongly on rf power, gas flow, chamber pressure and frequency (Fig. 25). If a PECVD deposition process is to be developed, it would be useful to approach the problem with a statistically-based set of experiments as discussed in Chap. 18. A case study of such a process development effort is found in Ref. 44. The stress in PECVD silicon nitride films can also be changed by altering a variety of deposition conditions.

Infrared spectroscopy shows that an appreciable amount of hydrogen in the form of Si-H and N-H is found in PECVD silicon nitride films. The total amount of hydrogen can reach 18-22 at% in films deposited from SiH₄-NH₃ near 300°C. Lower hydrogen content is reportedly found in films from SiH₄-N₂¹². The presence of large quantities of hydrogen has been reported to be detrimental to IC devices. For example, significant threshold shifts are observed, and etching characteristics (both wet and dry) of the films are impacted. Another advantage of using N₂ rather than NH₃ is that it yields compressive silicon nitride films over a wider range of deposition conditions. Oxygen in the form of Si-O bonds has also been detected in PECVD silicon nitride films. Oxygen concentration increases as the deposition temperature decreases, and is believed to be due to moisture or oxygen released from the reaction chamber walls. Table 4 is a summary of the CVD reactions for poly-Si, SiO₂, PSG, BPSG, as well as silicon nitride.

OTHER DIELECTRIC FILMS DEPOSITED BY CVD

Silicon Oxynitrides

Materials can be prepared with characteristics between those of nitrides and oxides, and these are called silicon oxynitrides [$\text{SiO}_x\text{N}_y(\text{H}_z)$]. They are formed by reacting SiH_4 with N_2O and NH_3 . Properties can be tailored for improved thermal stability, low stress, and crack resistance⁴⁵. Such films are also less permeable to moisture and other contaminants than deposited oxides. The use of helium as a carrier gas is reported to increase the uniformity of the refractive index of the films⁴⁶. Silicon oxynitrides also are reported to exhibit good properties for use as low-temperature deposited insulators between Al conductors. Two-layer films of PECVD silicon oxynitride and silicon nitride have been used in multilevel interconnect planarization schemes utilizing the differential etch rates of the two materials⁴⁶.

SIPOS

Silicon rich oxide films (i.e. the so-called semi-insulating polycrystalline silicon, or SIPOS) can also be deposited in APCVD, LPCVD, and PECVD reactors. This material has been reported to be excellent for passivating high field transistors⁴⁸, and has been studied for use as an injector in electrically-erasable read-only memories (EEROMs)⁴⁹ as well as a material for forming emitters in advanced super-gain bipolar transistors⁵². The chemical composition of SIPOS is SiO_x , where x ranges from 0.48 to <2. Such films can be formed by keeping the O_2 : SiH_4 flow rate ratio to <3.5. The composition of the films can be analyzed with Auger emission spectroscopy (Chap. 17), with a thermal SiO_2 film as a standard.

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PROBLEMS

1. Exponential temperature dependence is alternately represented by the form $\exp(-E_a/kT)$, or by $\exp(-\Delta H/RT)$, where E_a is the value of the activation energy in electron volts, and ΔH is its value in Kcal /mole. Show that if $E_a = 1$ eV, the corresponding value of ΔH is 23 Kcal /mole.
2. If a film is deposited conformally into a window that is 0.5 μm high and 1.0 μm wide, sketch the film when it has a thickness of 2000Å, 5000Å, 10,000Å. If the coverage is like that shown in Fig. 19a, what will the deposited film look like when its thickness is 0.5 μm . What does this effect imply for the application of depositing conformal (and nonconformal) films over high aspect ratio windows?
3. Conjecture why diffusion doped polysilicon can exhibit lower resistivities than polysilicon doped with ion implantation.
4. The activation energy of the $\text{SiH}_4\text{-O}_2$ reaction is ~ 0.6 eV for undoped oxides, while that for the undoped TEOS reaction is ~ 1.9 eV. If the deposition rate of CVD SiO_2 by the $\text{SiH}_4\text{-O}_2$ reaction is 250Å /min at 400°C, and is the same for the TEOS reaction at 700°C, find the temperatures for both of these reactions at which the deposition rate will double.
5. As CVD reactors are being designed as single wafer machines (as opposed to batch deposition systems), comment on some of the problems that have to be overcome in single wafer designs.
6. The minimum temperature for flow in phosphorus-doped SiO_2 is $\sim 1000^\circ\text{C}$. For some VLSI fabrication processes, the maximum allowable temperature is 900°C. Suggest four techniques that are candidates for producing layers of dielectric material between two conducting layers that is planarized, without having to heat the wafers to 1000°C.
7. Explain the difference between the terms *flow* and *reflow*.
8. Summarize the differences in the properties of high-temperature deposited silicon nitride, and plasma-deposited silicon nitride.

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