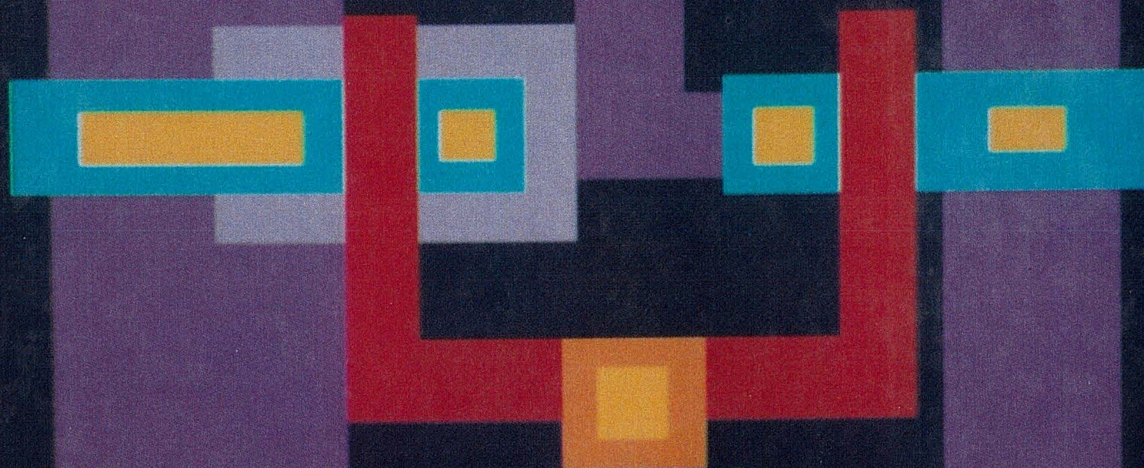


Silicon Processing

for the VLSI Era
Volume 2 - Process Integration



S. Wolf

SILICON PROCESSING
FOR
THE VLSI ERA
VOLUME 2:
PROCESS INTEGRATION

**SILICON PROCESSING
FOR
THE VLSI ERA**

**VOLUME 2:
PROCESS INTEGRATION**

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To my wife, Carrol Ann,
and my children, Jennifer Laura and Stanley Charles Ross

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PREFACE

SILICON PROCESSING FOR THE VLSI ERA is a text designed to provide a comprehensive and up-to-date treatment of this important and rapidly changing field. The text will consist of three volumes, of which this book is the second, subtitled, *Process Integration*. Volume 1, subtitled *Process Technology*, was published in 1986. Volume 3, to be subtitled *Assembly, Packaging and Manufacturing Technology* is scheduled for publication in 1993. In Volume 1, the individual processes utilized in the fabrication of silicon VLSI circuits are covered in depth (e.g., epitaxial growth, chemical vapor and physical vapor deposition of amorphous and polycrystalline films, thermal oxidation of silicon, diffusion, ion implantation, microlithography, and etching processes).

In this volume, we undertake to explain how the individual processes described in Volume 1 are combined in various ways to produce silicon integrated circuits. This task is referred to as *process integration*. The first part of the book deals with *sub-process integration*; that is, the effort involved in forming circuit structures that can be implemented into a variety of circuit types. These structures include *isolation structures* (Chap. 2), *metal-silicon contacts* (Chap. 3), and *device-interconnect structures* (Chap. 4).

The second part of the book covers the process integration tasks of full-device-type technologies, including *NMOS* (Chap. 5), *CMOS* (Chap. 6), *bipolar* and *BiCMOS* (Chap. 7), and *semiconductor memories* (Chap. 8). Chapter 9 describes the process simulation tools that are available for aiding in the process integration and development efforts.

Volume 3 will cover process control, VLSI manufacturing issues and facilities, contamination and yield, automation, assembly, packaging, and parametric testing.

The purpose of writing this text was to provide professionals involved in the microelectronics industry with a single source that offers a complete overview of the technology associated with the manufacture of silicon integrated circuits. Other texts on the subject are available only in the form of specialized books (i.e., that treat just a small subset of all of the processes), or in the form of edited volumes (i.e., books in which a group of authors each contributes a small portion of the contents).

Such edited volumes typically suffer from a lack of unity in the presented material from chapter-to-chapter, as well as an unevenness in writing style and level of presentation. In addition, in multi-disciplinary fields, such as microelectronic fabrication, it is difficult for most readers to follow technical arguments in such books,

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especially if the information is presented without defining each technical "buzzword" as it is first introduced.

In our books such drawbacks are avoided by treating the subject of VLSI fabrication from a unified and more pedagogical viewpoint, and by carefully defining technical terms when they are first introduced. The result is intended to be a user friendly book for workers who have come to the semiconductor industry after having been trained in but one of the many traditional technical disciplines.

An important technical breakthrough has occurred in publishing that the author also felt could be exploited in creating a unique book on silicon processing. That is, revolutionary electronic publishing techniques have recently become available, which can cut the time required to produce a published book from a finished manuscript. This task traditionally took 15-18 months, but can be now reduced to less than 3 months. If traditional techniques are used to produce books in such fast-breaking fields as VLSI fabrication, these books automatically possess a built-in obsolescence, even upon being first published.

We have taken advantage of these rapid production techniques, and have been able to successfully meet the reduced production-time schedule. As a result, information contained in technical journals and conferences which was available within three months of the book's publication date has been included.

Written for the professional, the book belongs on the bookshelf of workers in several microelectronic disciplines. Microelectronic fabrication engineers who seek to develop a more complete perspective of the subject, or who are new to the field, will find it invaluable. Integrated circuit designers, test engineers, and integrated circuit equipment designers, who must understand VLSI processing issues to effectively interface with the fabrication environment, will also find it a uniquely useful reference. The book should also be very suitable as a text for graduate-level courses on silicon processing techniques, offered to students of electrical engineering, applied physics, and materials science. It is assumed that such students already possess a basic familiarity with semiconductor device physics. Problems are included at the end of each chapter to assist readers in gauging how well they have assimilated the material in the text.

The book is an outgrowth of several intensive seminars conducted by the author through the Engineering Extension of the University of California, Irvine. Over one thousand engineers and managers from more than 75 companies and government agencies have enrolled in these short courses since they were first presented in 1984.

A book of this length and diversity would not have been possible without the indirect and direct assistance of many other workers. To begin, virtually all of the information presented in this text is based on the research efforts of a countless number of scientists and engineers. Their contributions are recognized to a small degree by citing some of their articles in the references given at the end of each chapter. The direct help came in a variety of forms, and was generously provided by many people. The text is a much better work as a result of this aid, and the authors express heartfelt thanks to those who gave of their time, energy, and intellect.

Each of the chapters was reviewed after the writing was completed. The engineers and scientists who participated in this review were numerous. The main reviewers are

listed on the page before the preface, and we would like to thank them once again at this point for their contributions. That is, the following professionals (each one an expert in the topic covered by the chapter they reviewed), read an entire chapter for technical correctness, and provided appropriate comments and corrections: Robert S. Blewer, John Y. Chen, Andrew R. Coulson, Haiping Dun, Terry Herndon, Michael Kump, Farhad K. Moghadam, Joseph R. Monkowski, Stan Swirhun, Al F. Tasch, Jr., and Samuel T. Wang. In addition, J. B. Price, of Spectrum CVD, Chris A. Mack, of the National Security Agency, and Sidney Marshall, Editor of Solid State Technology, provided other valuable technical and editorial input. Robert Shier, of VTC Corp., and Jim Cable of TRW also kindly provided the author with timely and valuable technical literature.

The copy editing of the book was undertaken by Mary Nadler, and the clarity and grammatical correctness of the prose owes a great deal to her professional efforts. The aesthetically pleasing graphics of the cover were designed by Roy Montibon of Visionary Art Resources, Inc., Santa Ana, CA.

Stanley Wolf

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effect of changing (especially reducing) the doping concentration at the surface of the Si (e.g., by varying the implant doses, the implanted species, and the dopant-activation-annealing steps following implant) has been reported to have a potentially significant negative impact on the value of ρ_c exhibited by a particular contact structure.

Finally, it should also be noted that if ρ_c values of $10 \Omega\text{-}\mu\text{m}^2$ or less can be obtained, then the value of R_{co} in devices with such contacts will probably not have much adverse effect on performance behavior, regardless of how small they are scaled. This important conclusion will be considered in more detail in section 3.8.

3.3.6 Use of a Simple Contact-Chain Structure to Monitor Contact Resistance

It should be briefly noted that an accurate value of R_{co} generally cannot be extracted from resistance data obtained from a simple *contact-chain structure*. That is, to determine R_{co} from the measurement of the total resistance of the contact chain shown in Fig. 3-12, the resistances of the metal-interconnect lines and the diffused region of the semiconductor must be subtracted from the measured resistance value. Since these resistances amount to a large fraction of the total measured value, the total contact resistance of the chain of contacts is obtained by subtracting two large numbers to obtain a smaller one. Such experimental data are therefore subject to large experimental errors.

Nevertheless, these kinds of contact chains are useful as test structures that can provide rapid monitoring of the contact-fabrication process. As long as the total measured-resistance value of such a contact chain is less than the specified value following a contact anneal step, the contact-fabrication process has probably been successfully performed.

3.4 THE EVOLUTION OF CONVENTIONAL METAL-TO-SILICON CONTACTS

Like other aspects of IC processing, the technology for fabricating metal-to-silicon contacts has had to evolve in order to keep pace with other advances in the process sequence. The technology we refer to as *conventional contact fabrication* involves the

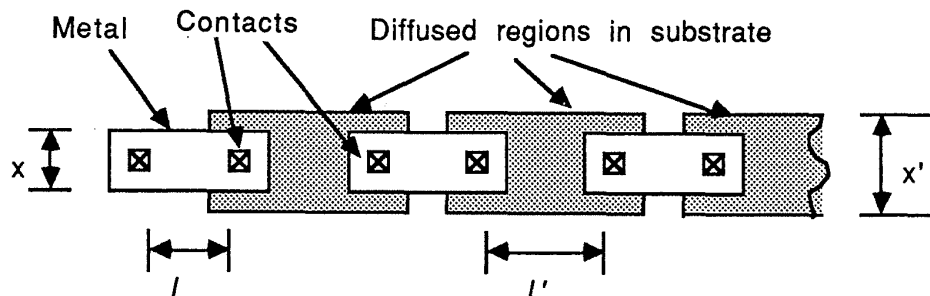


Fig. 3-12 Contact-chain. A test vehicle for monitoring contact resistance.

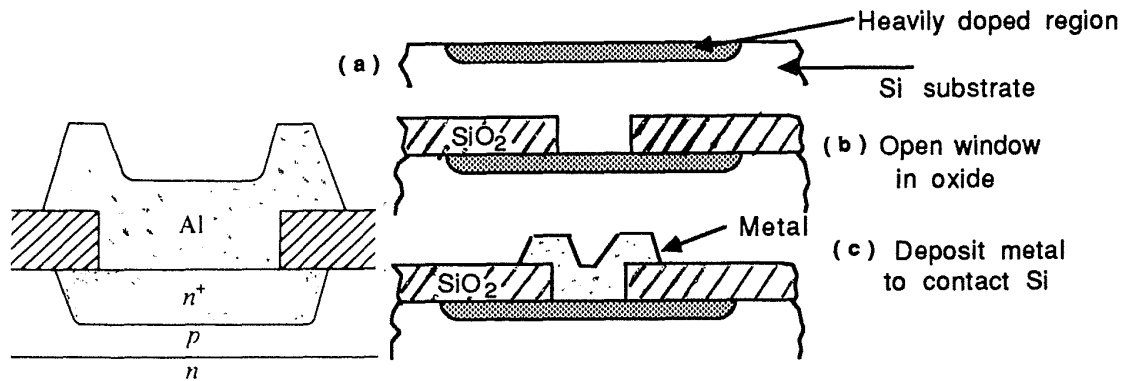


Fig. 3-13 Process sequence for forming conventional metal-semiconductor contact structure, in which the metal is deposited over a window in the passivating surface oxide.

fabrication of a contact to silicon at locations where a window has been etched in the oxide that covers and passivates the silicon surface (Fig. 3-13). While this type of contact has been used since integrated circuits were first invented, alternative contact structures have also been implemented recently. In this section we describe the evolution of the conventional contact structure, and show the reasons why alternative technologies were developed.

3.4.1 The Basic Process Sequence of Conventional Ohmic-Contact Structures to Silicon

Following is the basic sequence of steps involved in the formation of a metal-to-silicon contact structure for an integrated circuit:

1. Heavily doped regions, which extend relatively deeply into the silicon, are created in the silicon substrate in the locations where contacts are to be established.
2. A window (or *contact hole*) is etched in the oxide that covers the silicon wafer surface (typically, this is a thermal oxide or a CVD oxide/thermal oxide layer). The etching can be done using either wet or dry etching techniques.
3. Prior to deposition of the metal, the surface of the silicon is cleaned to remove the thin native-oxide layer that rapidly forms on a silicon surface whenever it is exposed to an oxygen-containing ambient.
4. The metal film is deposited onto the wafer surface and makes contact with the silicon wherever contact holes have been created in the oxide. In the simplest contact structures, the deposited metal is Al (or an Al:Si alloy). A variety of procedures have been developed to ensure that the deposited-metal

films adequately cover the sidewalls of the contact windows without severe thinning (i.e., thereby achieving good *step coverage* into the contact windows).

5. After deposition, the contact structure is subjected to a thermal cycle known as *sintering* or *annealing*. The purpose of this step is to bring the metal and the silicon surfaces into intimate contact. In the case of Al contacts, during sintering the Al film will consume any residual native oxide by chemically reacting with it (assuming that this residual film is not too thick).

3.4.2 Additional Details Concerning the Processing Steps

3.4.2.1 Formation of the Heavily Doped Regions in the Silicon.

As described earlier, in order for an ohmic contact to be formed at a metal-semiconductor interface, the surface of the semiconductor must be heavily doped, with the dopants having been usually selectively introduced through ion implantation or diffusion. A masking layer is used to restrict the introduction of dopants to the desired locations on the silicon surface. Such heavily doped regions may also form part of the transistor device structure (e.g., the source and drain regions in MOSFETs and the emitter regions in bipolar transistors).

The contact resistance is inversely proportional to the surface concentration of the dopant, and thus as heavy a doping as possible would seem desirable. However, the maximum doping concentration is limited by the solid solubility at the temperature at which the dopant is introduced. Clustering effects may also reduce the concentration of the electrically active impurities below the concentration of deposited dopant atoms. For example,⁸ arsenic atoms undergo such clustering if their concentration is above 10^{20} cm^{-3} . A model for As clustering is described in reference 9.

In advanced IC processing, it is necessary to form heavily doped regions that extend into the silicon to very shallow depths only. Since higher implant doses result in deeper junction depths, the dose cannot be chosen independently of the device design. The topic of shallow-junction formation and the problems associated with the fabrication of contacts to shallow junctions is explored in section 3.10.

3.4.2.2 Formation of Contact Openings (Etching). The formation of contact holes in the oxide that covers the wafer surface is also a key step in the fabrication of contact structures. The minimum size of the contact holes is usually determined by the minimum-resolution capability of the patterning technology, because this results in the smallest device sizes. As a result the patterning technology is generally pushed to its limits in the patterning of contact holes.

When the contact holes are larger than $\sim 2.0 \mu\text{m}$, wet etching has often been used to open them. Even in such contact holes, however, wetting and reactant product removal can be a problem. To partially overcome the wetting problem and to ensure better material flow into the vicinity of the reacting surface, mechanical or ultrasonic agitation

was introduced. Such wet-etching technology of SiO₂ films is described in more detail in Volume 1, chapter 15.

The isotropic nature of wet etching, however, made it ineffective for the patterning of smaller-sized contact holes. As a result, development of SiO₂ dry-etching processes had to be pursued (see Vol. 1, chap. 16). Dry etching, however, introduced a new set of problems, including polymer contamination, damage of the Si surface, and decrease of oxide etch rate with decrease in contact size. One consequence of the former effect was that either gases with less propensity for forming polymeric products would have to be found, or more complex processes to remove the polymers from the contact holes after etch, would have to be developed. Dry etching also exhibited selectivity problems, which became more significant as junctions grew shallower.

Several approaches were also proposed to alleviate the problems of damage to the silicon surface and redeposition of nonvolatile by-products from the chamber surfaces and wafer holders. One was to use isotropic (ion-bombardment-free) dry etching to remove surface damage and contaminants.¹⁰ Another combined a dry-etch step (to remove the first 80% of the contact oxide layer) and a buffered HF wet etch (to etch the remainder of the oxide film). This method, however, still presents the problem of wetting in small contact holes. One proposed solution to the wetting difficulty is to use an anhydrous-HF gas to remove the final oxide layer.^{11,134}

A process has been reported that uses a CHF₃/CO₂ dry-etch process to open the contact holes, followed by a two-step dry-etch cleaning procedure to remove the residual damage.^{12,13} Finally, an RTP process that repairs the silicon-crystal damage in the contact hole has also been described.¹⁴

As the contact hole size decreases below 1 μm there is a strong decrease in etch rate with contact size dimension. To avoid long overetch times, contact holes of identical dimension would need to be used if this problem was not solved. Reference 156 describes a dry-etch process which overcomes this limitation. By adding 10% Cl₂ to a CHF₃ plasma the effective fluorine to carbon ratio in small holes is kept constant, maintaining uniform etch rates, independent of contact hole size. Nevertheless, it is very common that only one contact size is used. Larger contacts are implemented with multiple contact windows.

3.4.2.3 Sidewall Contouring of the Contact Holes by Reflow. In addition to the need to ensure that the contact holes are opened and that silicon-surface damage and contamination are minimized, it is also important to give the contact hole a shape that will result in good step coverage by the metal that is deposited into it. In general, better step coverage will be obtained if the walls of the contact opening are sloped and the top corners are rounded, and several different approaches have been pursued to achieve these desired sidewall profiles.

One of the most popular involves *reflow of the contact hole dielectric layer*. Wafers are exposed to a high-temperature step after the contact holes have been opened. This causes the CVD doped-SiO₂ layer to flow slightly, producing rounded corners and sloped sidewalls in the contact holes (see Vol. 1, chap. 6). *Borophosphosilicate glass* (BPSG) flows at the lowest temperatures (800-850°C at atmospheric pressures), and even lower-

temperature reflow cycles (using high-pressure conditions) have reportedly been developed.¹⁵ Reflow using RTP has also been investigated.¹⁶ A recently introduced LPCVD reactor allows BPSG film deposition to be followed by an in situ flow step, which eliminates a process step and reduces the overall cycle time (although reflow must still be performed after contact holes have been opened).¹⁴¹ A study of the reflow mechanisms in BPSG films presented in reference 138. It indicates that reflow in BPSG film will cause sidewall overhang and reentrant angles at the base of the contact hole if the aspect ratio of the contact hole is larger than 0.393.

It has also been mentioned that it can be useful to grow a thin-oxide layer over the contact hole following patterning, but prior to reflow. The function of this oxide is to prevent autodoping of the contact regions during reflow by the BPSG film. This oxide would be grown at a lower temperature (e.g., 8 minutes in steam at 800°C) than the reflow temperature (e.g., 900°C).¹³⁵ Alternatively, the reflow can be done in a dry O₂ ambient to simultaneously grow the thin protective-oxide layer.¹⁴⁰

H. Ozaki et al., however, have described how the B₂O₃ in the BPSG film can react with the PH₃ (used as part of the gas ambient during reflow to redope the contacts in NMOS technology) to form a volatile compound of boron. This boron is then taken up by the oxide film that is grown in the contact openings during the reflow, resulting in a much thicker oxide in the contact hole following reflow.¹⁷ Consequently, another suggested approach for preventing contact-degradation effects during the reflow step is the deposition of diffusion-barrier materials (e.g., silicon nitride or TiN) over the opened contacts prior to the reflow step.¹⁵

3.4.2.4 Sidewall Contouring by Etching. Other sidewall-contouring processes involve the etching procedure used to pattern the contact holes. The first of these uses a wet etch (which is isotropic) to partially etch the oxide, and follows this with an anisotropic dry etch.¹⁸ The method yields a contact hole whose profile is sloped at the top but is vertical at the bottom. While good step coverage can be achieved in some applications, difficulty may be encountered in obtaining good wetting, especially for very small contacts. In addition, the sidewall profile may still have a sharp corner at the upper edge, which gives rise to step-coverage problems. A variation of this method is to use a triple layer (oxide/nitride/oxide). The top oxide is wet etched to provide a sloped contact-hole sidewall, and the nitride serves as an etch stop. The remaining nitride and oxide are then etched with a vertical dry-etch step.¹⁹

Another general approach involves the controlled erosion of photoresist (PR) that has been baked to produce a sloped PR wall.^{20,21} In this method, PR images of the contacts are exposed and developed using standard lithographic techniques. Following develop, the resist images are subjected to a postdevelop bake of ~150°C (Fig. 3-14a). The resist flows during the bake, relaxing the vertical resist profile. Etching the resist and oxide at approximately the same rate replicates the tapered-resist profile into the contact sidewall. While the bake-to-slope process is quite adequate for large contacts or vias (>2 μm), it is not easily scalable to smaller geometries. For such smaller contacts resist baking step becomes critical. Too little baking results in vertical contact profiles, while excessive baking can result in closed contacts. Furthermore, continued etching of

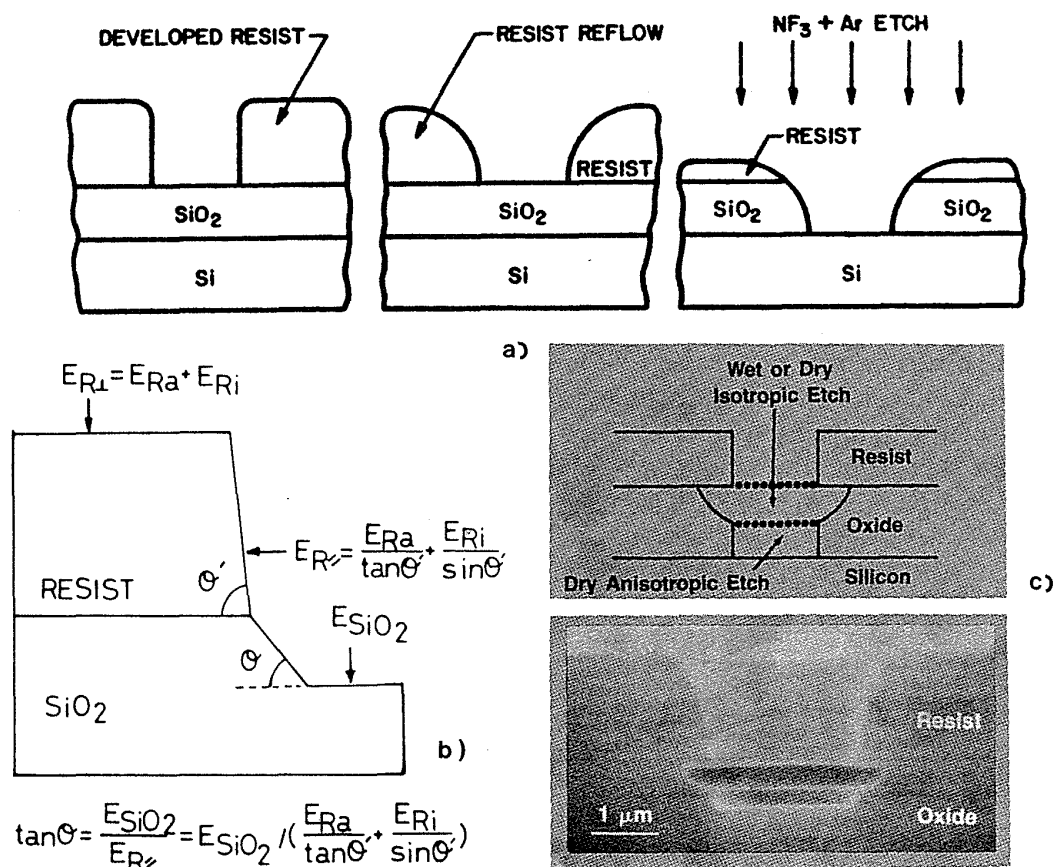


Fig. 3-14 (a) Tapered contact-hole etching by reflowing resist profile with a resist bake, followed by a dry etch to transfer the resist profile into the oxide. (b) Tapering of contact-window sidewall by optimizing the lateral to vertical etch rates of the resist mask.²⁵ Reprinted by permission of the publisher, The Electrochemical Society, Inc. (c) Sloping oxide sidewalls using a triode dry etcher.¹⁵² Reprinted with permission of Solid State Technology.

the contact results in continued growth in the contact diameter (although this effect can be alleviated somewhat by using a two-step etch process).²²

Several other, more controllable resist-erosion techniques have subsequently been described. In one, the effect of resist faceting (see Vol. 1, chap. 10) caused by the preferential sputtering of the resist corners was used to produce tapered-contact sidewalls.²³ Another method, developed by Jillie et al.,²⁴ uses a single-wafer etcher, and a two-step etch process to etch a multilevel-resist layer (i.e., consisting of a thin positive resist, an antireflection coating, and a thick PMMA). Good control over the sidewall slope has been reported, and a reflow step has also been used to round the top corners of the sidewall. The drawback to this approach is increased process complexity.

A third resist-erosion approach was reported by Kudoh et al.²⁵ In this procedure, etching of the contact oxide is carried out with a PR mask that has vertical sidewalls.

Oxygen is added to the CHF_3 gases being used to etch the oxide. The oxygen attacks the PR at a controlled rate, thereby producing lateral as well as vertical etching of the PR mask. More of the top SiO_2 is slowly exposed as vertical etching of the SiO_2 proceeds, and a sloped oxide sidewall is produced (Fig. 3-14b). Taper angles of $40\text{--}85^\circ$ were obtained by varying the oxygen concentration.

Another technique for tapering contact-hole sidewalls without using resist erosion involves implantation of the surface of the oxide following deposition. This damages the top layer of the oxide and causes it to etch more rapidly, even when dry etching is used. The faster-etching top-surface layer causes a slope in the sidewalls.

A final group of processes utilizes two or more dry-etch steps to obtain tapered-sidewall profiles. In one example, a high-rate isotropic SiO_2 etch (i.e., with a lateral-to-vertical etch-rate ratio of 0.9 to 1 being exhibited for doped oxides) is used to etch the top portion of the contact-oxide layer, and an anisotropic-etch process is used to remove the oxide from the bottom of the contact hole.²⁶ In another, a downflow etcher operated at 2.45 GHz is used to etch part of a doped SiO_2 layer in an isotropic manner using a $\text{CF}_4 + \text{O}_2$ mixture; this is followed by an RIE step to give a vertical profile for the bottom portion of the layer.²⁷ A method that uses a tri-electrode dry-etch chamber for this type of process is described in reference 152 (Fig. 3-14c).

The problem of end-point detection for contact holes can also be difficult. That is, if a timed etch is used, a sufficient overetch must be allowed to ensure that all the contacts are opened. However, this demands a high selectivity to the Si to prevent too much Si from being consumed during the overetch. End-point detection is difficult, because the total area of the contacts being etched is significantly smaller compared to other layers. A technique for electronically enhancing the weak end-point signal produced when the contacts are finally opened is described in reference 144.

3.4.2.5 Removal of the Native-Oxide Layer Prior to Metal Deposition. Before the metal is deposited into the contact openings, it is necessary to ensure that the exposed silicon surface is as free as possible of contamination or of a native-oxide layer. Silicon will grow a thin native oxide within a matter of seconds upon exposure to an oxygen-containing ambient or an oxidizing solution. This native oxide can represent an impediment to current flow through the contact interface, result-

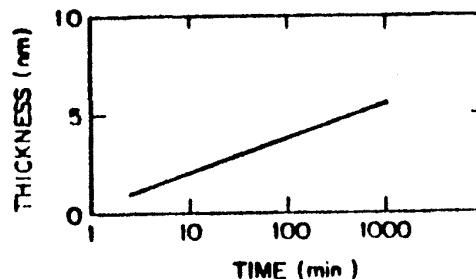


Fig. 3-15 Native oxide growth rate on Si exposed to room air.²⁸ Copyright 1984. Reprinted with permission of the AIOP.

ing in high resistance for ohmic contacts. Oxide films of minimum thickness (2–5Å) do not present a problem, since many contact metals (e.g., Al, Ti, Pt) can consume such thin oxide layers during the sinter step. Nevertheless, as shown in Fig. 3-15, the native-oxide layer can grow thicker than this value in 30 to 60 minutes* if the Si is exposed to atmosphere at room temperature.^{28,139} Consequently, techniques must normally be employed to remove native oxide layers on Si, and the metal must be deposited quickly enough after such premetal cleaning that the film does not have enough time to regrow.

A variety of techniques have been suggested for cleaning the Si prior to metal deposition. Polymers deposited during a dry-etch step used to etch the contact oxide are typically removed through a final oxygen-ashing step. This step may, however, may create a thin oxide layer on the exposed Si. The most widely used method for removing native-oxide layers on the Si involves dipping the wafer in a dilute H₂O:HF (100:1) solution for ~1 minute, followed by rinsing and drying and immediate insertion into the sputter or evaporation chamber. (The HF dip also serves to remove heavy-metal contamination that might occur as a result of the dry-etch process.)

It is acknowledged that this method is not perfect, since some SiO₂ will regrow on the Si during the rinse-and-dry step, and inadequate wetting may prevent complete removal of the native oxide in small-geometry contacts. Therefore, a technique of sputter-etching the contacts in the sputter chamber and depositing the metal before reexposing the contacts to atmospheric conditions is also frequently used in addition to the HF dip. Most sputtering systems currently provide the capability for performing such sputter etching.

However, some concerns have also been raised about sputter etching. For small, high-aspect-ratio contact holes, sputtering and redeposition of material from the contact sidewalls and the wafer surface may cause more oxide to be deposited onto the Si than is removed through the sputter-etch process (Fig. 3-16).²⁹ Two alternative procedures to overcome these concerns have therefore been suggested. The first involves an in situ, chemically driven dry-etch step to remove the native oxide. While this would eliminate the resputtering effect, it would require that sputtering equipment be designed with this extra capability; no such products have yet been commercially introduced. In the second approach, an anhydrous-HF gas could be used to remove the native oxide, as described in a previous section.

The effect of "dirty" Si surfaces prior to Al deposition has been studied by Faith et al.³⁰ These researchers showed that if the Si surface is not successfully cleaned prior to Al deposition, the post-sinter contact resistance will be an order of magnitude higher than if an effective pre-metal clean had been used. They also noted that clean contacts

*A recent report indicates that both moisture and oxygen must be present in air in order for the oxide to grow. Furthermore, if oxygen is present in DI water, a native oxide will also grow when Si wafers are immersed in it. Since the growth rate of native oxide decreases with the concentration of moisture, this may provide an approach to the control of native-oxide films on Si.¹⁴⁷ For example, virtually no native oxide was observed to grow during a seven day period of time when Si wafers were stored in air containing < 0.1 ppm moisture.

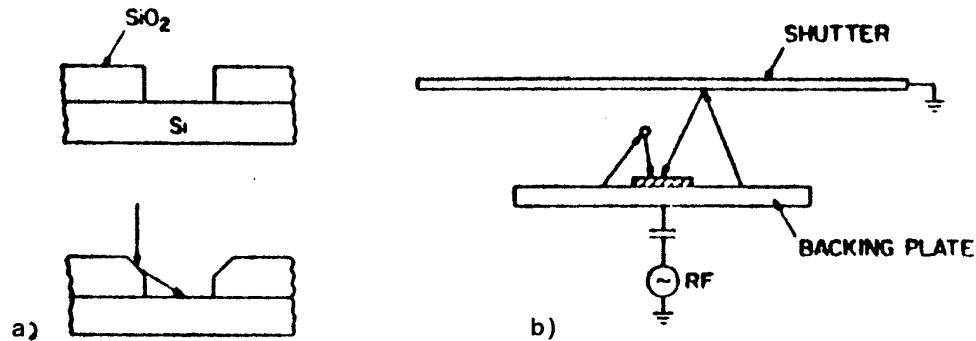


Fig. 3-16 Sources of contamination of Si surface at the bottom of the contact hole as a result of RIE. (a) Faceting occurs during anisotropic etching of contact openings. Material sputtered from the facet deposits in the contact opening at a rate that may exceed the rate of removal of the material from the bottom of the opening. (b) Backscattering of material sputtered from the backing plate may occur due to collisions with gas molecules of the glow discharge or from reflection from the shutter.²⁸ Copyright 1984. Reprinted with permission of the AIOP.

exhibit a lower contact resistance than dirty ones *prior* to the sinter step, and that this effect could be exploited to test the contacts prior to sintering. If a dirty interface were detected at that point, a decision to strip and rework the metal might still be possible, whereas this option would no longer be available once sintering had been performed. As described in the following section on contact sintering, ion-beam mixing has also been proposed as a way to disperse any native-oxide layers at the interface.

3.4.2.6 Metal Deposition and Patterning. The major issue in the deposition of metal for fabricating contacts is ensuring that adequate step coverage is obtained into the contact holes. When contact-hole sizes are comparable to the oxide thickness (i.e., when the holes have high aspect ratios), good step coverage can be difficult to achieve. The deposition process, as well as the profile of the contact-hole sidewalls, can significantly impact the quality of the step coverage. Several aspects of the metal-deposition procedure can also play a role in this issue.

First, the type of process selected for deposition is significant. Some CVD processes can completely fill high-aspect-ratio contact holes, even those with nearly vertical sidewalls, while physical vapor deposition (PVD) methods are not apt to fill the holes so well. This advantage has been exploited in filling contact holes with CVD W (selectively and through blanket deposition). Polysilicon and selectively grown epitaxial layers of Si are other CVD processes that have been reported for such contact-filling applications.

If films are needed that cannot be deposited by CVD, the conditions of the PVD process can be selected to give improved step coverage (see chap. 4 in this volume, and Vol. 1, chap. 10). For example, heating of the wafers to ~300-350°C has been shown to significantly improve the step coverage of sputtered Al films into contact holes. Full planarization (i.e., complete filling of the holes) has also been demonstrated by applying

even higher temperatures during sputter deposition (400-500°C). Laser planarization of Al films following deposition has also been developed to improve step coverage into contacts (see chap. 4).

In addition, sputtered Ti:W films have also been reported to give excellent step coverage. This method can be used to enhance the overall step coverage of contact structures – for example, if such a Ti:W film is used under a layer of Al. On the other hand, the problem of film thinning at the bottom corners of the contact window can produce reliability problems in contacts. Even if the top layer of Al appears to have been deposited with adequate step coverage, the diffusion-barrier layer, for instance might have been deposited with thin spots at these edges (Fig. 3-17). As a result, the contact could fail because the barrier layer was not thick enough at these locations to survive the sintering steps following deposition of the metal (see section 3.5).

The issues dealing with the patterning of the metallization layers used in contact structures are described in further detail in Volume 1, chapter 16.

3.4.2.7 Sintering the Contacts. As described earlier, the sintering or annealing of contacts (i.e., the alloying of contacts through treatment at an elevated temperature) is performed to allow any interface layer that exists between the metal and the Si to be consumed by a chemical reaction, and to allow the metal and Si to come into intimate contact through interdiffusion. The details of the various reactions that occur at specific metal-Si interfaces during the sinter cycle are described in the following sections examining the properties of each contact type. In this section we merely mention the several methods by which such intermixing of materials at the interface is performed.

The traditional method carries out the sinter step in a diffusion furnace, usually at 400-500°C for 10 to 30 minutes in the presence of H₂ or a *forming gas* (a mixture of H₂ (5-10 at%) and N₂ (95-90 at%)). Such gases are used because many metals are

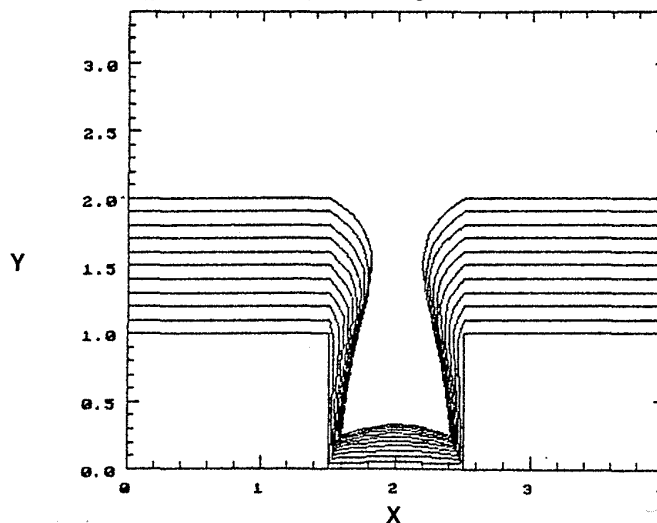


Fig. 3-17 Simulated metal coverage of a contact hole with vertical sidewalls, showing thinning at the bottom corners.

sensitive to oxygen at elevated temperatures, and because this step is also used to anneal out the surface states (i.e., interface traps at the oxide-Si interface) by tying up the dangling Si and oxygen bonds. The hydrogen is responsible for passivating and deactivating the interface traps.

More recently, alternative methods – including RTP, laser annealing, isothermal e-beam sintering, and ion-beam mixing – have also been investigated for performing this step. Although ion-beam mixing does not subject the contacts to elevated temperature, the chemical outcome is very similar to that in an alloying process. The technique involves the implantation of a relatively high dose of ions at an energy that is high enough to allow full penetration through the metal layer and into the Si substrate. If the species that is implanted is the same as the dopant of the junction to be formed, the junction and the contact can be fabricated simultaneously.³¹ Normally, the implant is followed by a furnace step (conventional or RTP) to repair the implant damage, and possibly to form a silicide or to distribute the implanted dopant.

3.4.3 Aluminum-Silicon Contact Characteristics

The contact structure consisting of pure Al deposited directly onto Si was adopted in the earliest stages of silicon technology primarily because of its simplicity, but also because it exhibits some other advantages. Al and Al alloy thin films are still the most common interconnect materials in silicon ICs today. Al-to-Si ohmic contacts can be fabricated with low values of contact resistance to both n^+ and p^+ Si, and both the contact and the interconnect structure can be fabricated through a single deposition step. Al is desirable as an interconnect material because it exhibits low resistivity ($\rho_{Al} = 2.7 \mu\Omega\text{-cm}$) and offers excellent compatibility with SiO_2 (i.e., Al will readily react with SiO_2 to form a thin layer of Al_2O_3 at the interface, thus promoting strong adhesion between the Al and the SiO_2). The Al thin films used for interconnects are typically 0.5-1.5 μm thick.

However, the Al-to-Si contact exhibits some poor contact characteristics and also introduces some limitations into the processing sequence. Because the melting point of Al (660°C) and the eutectic temperature of Al and Si mixtures (577°C) are so low, Al is a problematic material with respect to the maintenance of contact stability. Thus, the simple contact structure of pure Al-to-Si has had to be modified, especially for VLSI applications. In addition, Al must be introduced into the IC process sequence after all high-temperature processing has been completed.

3.4.3.1 The Kinetics of the Al-Si Interface During Sintering.

We noted earlier that a sinter step is performed after a contact metal film has been deposited and patterned. In the case of Al-Si contacts, such sintering causes the Al to react with the native-oxide layer that forms on the silicon surface. In the case of e-beam-evaporated Al films on MOS devices, sintering also anneals out the radiation damage at the SiO_2/Si (gate oxide/Si) interface from the x-rays generated by the evaporation process; see Vol. 1, chap. 9. As the Al reacts with the thin SiO_2 layer, Al_2O_3 is formed, and in a good ohmic contact, the native oxide is eventually completely

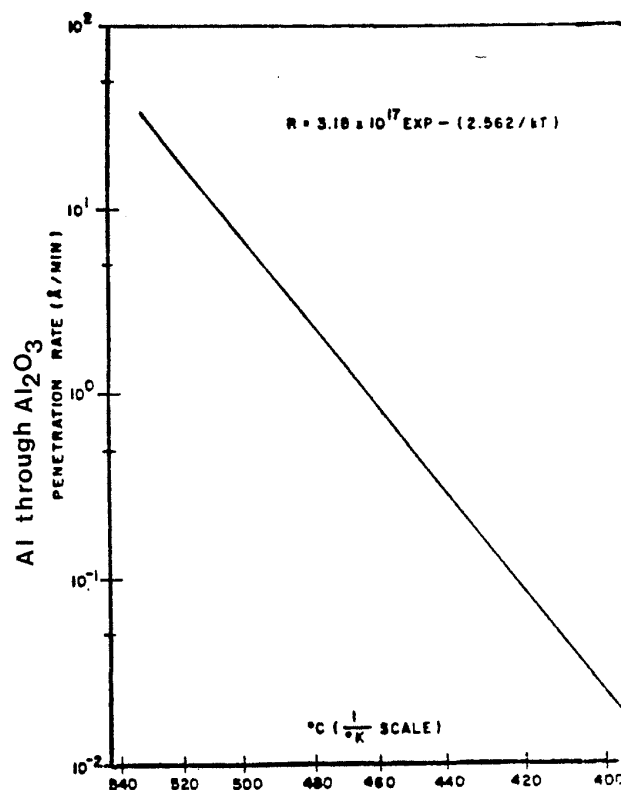


Fig. 3-18 Rate of reaction for $\text{Al} + \text{SiO}_2 \rightarrow \text{Al}_2\text{O}_3 + \text{Si}$.

consumed. Thereafter, Al diffuses through the resultant Al_2O_3 layer to reach the Si surface, forming an intimate metal-Si contact.

Note that Al must diffuse through the Al_2O_3 layer to reach the remaining SiO_2 . As the Al_2O_3 layer increases in thickness, it takes longer for the Al to penetrate it. Thus, if the native-oxide layer is too thick, the Al_2O_3 layer eventually also becomes too thick for Al to diffuse through it. In this case, not all of the SiO_2 will be consumed, and a poor ohmic contact will result (i.e., one that exhibits a high specific contact resistivity).

Figure 3-18 shows the penetration rate of Al through Al_2O_3 as a function of temperature. For acceptable sinter temperatures and sinter times (e.g., 450°C and 30 min.) the thickness of the Al_2O_3 should be in the 5-10 Å thickness range. Since the maximum Al_2O_3 thickness is of the order of the thickness of the native oxide that is consumed, an approximate upper limit to the allowable thickness of the native-oxide layer is set. The longer the silicon surface is exposed to an oxygen-containing ambient the thicker the native oxide will be (Fig. 3-15). This explains why surface-cleaning procedures in most contact processes are performed just prior to loading of the wafers into the deposition chamber for metal deposition.

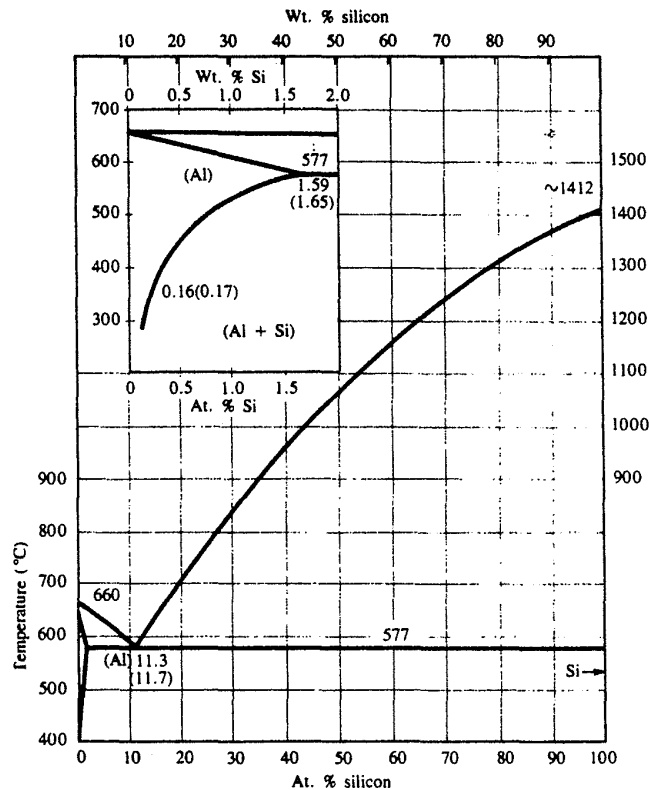


Fig. 3-19 Phase diagram of the aluminum-silicon system. The silicon-aluminum eutectic point occurs at a temperature of 577 °C. At contact-alloying temperatures between 450 and 500 °C, aluminum will absorb from 0.5 to 1% silicon. Copyright 1958, McGraw-Hill Book Company, with permission from ref. [161].

Since the use of a sinter step is inevitable when Al-Si contacts are fabricated, the other effects of this thermal cycle on the contact structure must also be considered. The phase diagram of the aluminum-silicon system (Fig. 3-19), indicates that the solubility of silicon in aluminum rises as the temperature increases (e.g., it is ~0.5 at% at 450°C, and ~1 at% at 500°C). This means that if a pure Al film were heated to 450°C and a source of silicon were provided, the Al would take up the silicon in solution until a concentration of 0.5 at% of Si was reached. The substrate serves as such a source, and the silicon will enter the Al by diffusion at such elevated temperatures. If silicon diffusion were slow and the contact was maintained at the elevated temperature for only a short time, not much silicon would enter the Al, so there would be no problem.

In the actual case of Al thin films (which are polycrystalline in structure), the grain boundaries of the polycrystalline Al film provide very fast diffusion paths for the Si at temperatures above 400°C. Figure 3-20 shows the diffusivity of Si in Al as a function of temperature, for both bulk and thin-film Al.³² The diffusivity in the thin-film Al is seen to be much faster. As a result, if a large volume of Al is available, a significant quantity of the Si from below the Al-silicon interface can diffuse into the Al film. Simultaneously, the Al from the film will move rapidly to fill the voids created by the

departing Si (Fig. 3-21). If the penetration of the Al is deeper than the *pn*-junction depth below the contact, the junction will exhibit large leakage currents or even become electrically shorted. This effect is referred to as *junction spiking*.

The depth to which Si is consumed and Al penetrates into the Si substrate can be calculated as a function of the thickness and width of a long Al line, the contact area, and the temperature and time of the sintering. As shown in Fig. 3-20, at temperatures in excess of 400°C the diffusion length in one minute exceeds 10 μm . The effect of the diffusion with respect to an actual contact structure is illustrated in Fig. 3-21. As a result of such diffusion, the silicon in a 16 μm^2 Al-Si contact would be consumed to a depth of $\sim 0.3 \mu\text{m}$ if the contact was exposed to a temperature of 500°C for 30 min (assuming uniform Si consumption across the contact area).³³ Consequently, junctions with depths of less than 0.3 μm would be shorted, rendering the devices inoperable.

In fact, since the Si consumption is not uniform across the entire contact area, the situation is even more severe than is portrayed by the above example. The native oxide that exists at the Si surface is not uniform in thickness but has local thin spots, or defects, as shown in Fig. 3-21. Thus, when the native oxide is consumed during sintering, it will first be removed at these thin spots, and Si will therefore be able to dissolve into the Al at these points. As a result, Al penetration, or *spikes* can occur to a depth of more than 1 μm . In (100)-oriented Si substrates, such spikes tend to move perpendicularly to the surface and are bounded by (111) planes. In addition, Al spiking occurs preferentially at the contact-hole edges, where stresses present in the Si lead to enhanced dissolution of the Si during contact sintering. If the Al is stripped after such sintering, the Si pits appear as shown in Fig. 3-22.

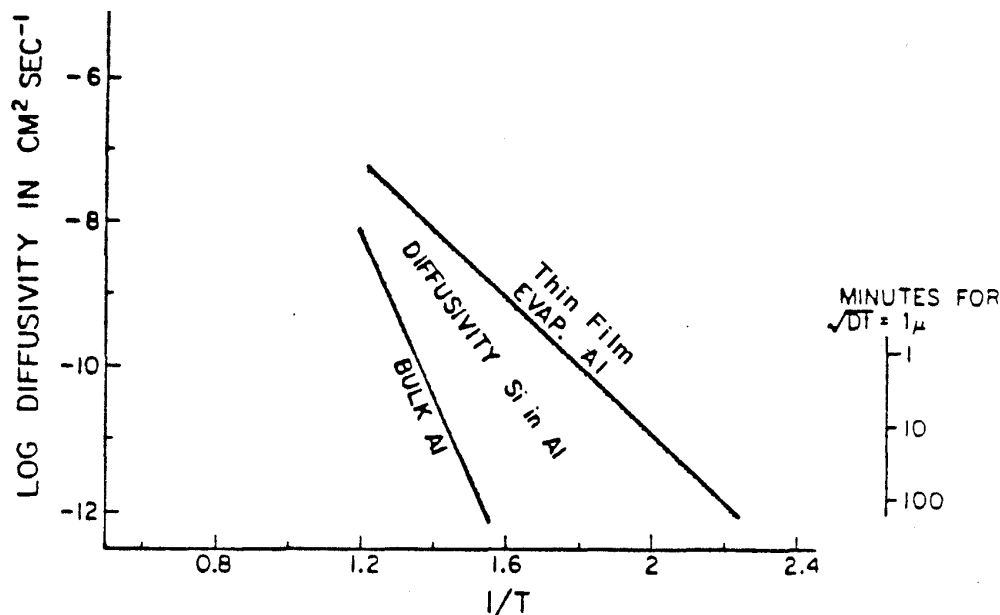


Fig. 3-20 Diffusivity of silicon in bulk and thin film aluminum.³² Copyright 1974. Reprinted with permission of the AIOP.

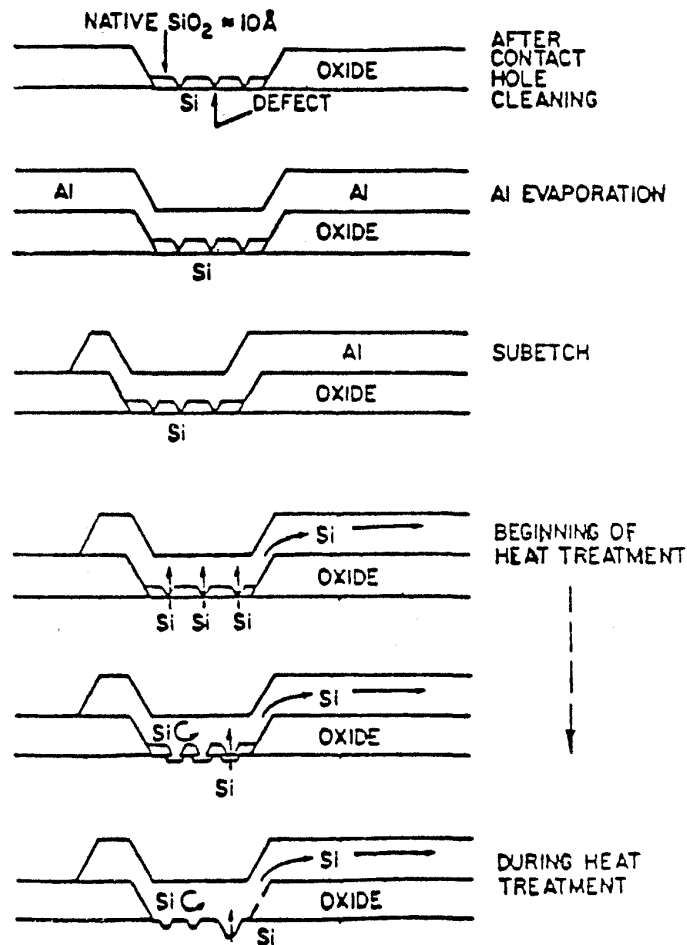


Fig. 3-21 Sequence of events during the sintering of Al-Si contacts that leads to Al junction spiking.

The pit dimensions is also observed to increase as the area of the contact hole is decreased.³⁴ This effect imposes a severe limitation on the usable combination of

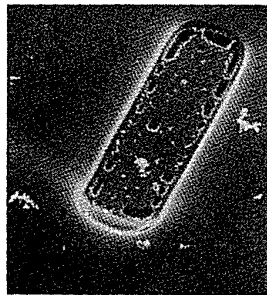


Fig. 3-22 SEM micrograph of Si pitting that exists after sintering of an Al-covered contact. (Al has been stripped after the sinter step.)¹⁶⁵

junction depth, x_j , and contact-hole size, d , or $x_j \gg 4.7d^{-0.8}$. More concisely, since junction depths of less than 200 nm are being utilized in advanced ICs, this type of contact cannot be used.

3.4.4 Use of Aluminum-Silicon Alloys to Reduce Junction Spiking

To alleviate the problem of junction spiking at contacts without abandoning the advantages of the simple Al-to-Si contact structure, Si can be added to the Al film as it is deposited. This is typically accomplished by sputter depositing the film from a single target containing both Al and Si, although coevaporation of Si and Al has also been used. If enough Si is added to the Al so that the concentration exceeds the Si solubility at the maximum process temperature, diffusion of Si into the Al will no longer occur, and junction spiking can be prevented. The amount of Si that must be added to accomplish such *presaturation* of Al with Si therefore depends on the maximum process temperature to which the contact structure will be exposed. Since this maximum temperature is normally less than 500°C, in most cases slightly more than 1 wt% Si is added. The change in resistivity of the Al, $\Delta\rho$, caused by such additions of Si is very small (i.e., $\Delta\rho$ for each percentage of Si added is only $0.07 \mu\Omega\text{-cm}$, and $\rho_{\text{pure Al}} = 2.7 \mu\Omega\text{-cm}$).

Such Al:Si alloys were widely adopted for fabricating the contacts and interconnects of NMOS integrated circuits. To improve the reliability of such contact structures, deeper junctions immediately below the contact opening were also employed in some processes. (These deep junctions were created by redoping the Si with phosphorus after the contacts were opened. Such redoping can be accomplished during the reflow step, by performing the reflow in an $\text{N}_2/\text{PH}_3/\text{O}_2$ ambient.¹⁷ Doing so allows the source/drain regions near the channel to be kept shallow for good device performance, while providing a deep junction under the contact to prevent junction spiking. This method cannot of course be used in the shallow source/drain regions of devices fabricated in the wells of CMOS structures (see chap. 6 on CMOS device structures).

Although the use of Al:Si instead of pure Al prevented junction spiking, it also introduced other problems. During the cooling cycle of a thermal anneal, the solid solubility of silicon in Al decreases with decreasing temperature. The aluminum thus becomes supersaturated with Si, which causes nucleation and growth of Si precipitates out of the Al:Si solution. Such precipitation occurs both at the Al-SiO₂ interface and the Al-Si interface in the contacts (preferentially around the contact hole edges where solid-phase epitaxial growth occurs easily). These precipitates consist of *p*-type silicon (since Al is a *p*-type dopant in Si), doped with Al to a concentration of $\sim 5 \times 10^{17} \text{ cm}^{-3}$.

If such precipitates form at a p^+ -Si-Al contact interface, they do not degrade the contact properties. On the other hand, if they form at the contact interface to n^+ -Si, an undesirable increase in contact resistance results. In practice, for contacts sizes of $3 \times 3 \mu\text{m}$ or greater, such effects are not significant, and Al:Si alloys can be used effectively. For smaller contacts, however, the increase in resistivity can be excessive.

In addition, the Si precipitates formed within the Al interconnect lines can increase the susceptibility of the lines to electromigration failure. That is, in narrow Al lines the precipitates can be large enough to obstruct a large fraction of the cross-sectional area of the metal line at random locations.^{35,36} The size of the Si precipitates in Al:1% Si alloys is about $0.4\text{ }\mu\text{m}$; if the films are cooled slowly, the precipitates can grow to be as large as $1.5\text{ }\mu\text{m}$. At locations where such precipitates are formed, a large flux-divergence in the current is produced. This can lead to early failure of the conductor by an electromigration-induced open circuit.

Al-Si contacts exhibit two other important limitations that would prevent their use in advanced VLSI applications, even if the problems above could be overcome. First, in IC technologies in which small-sized contacts and shallow junctions must both be used, Al:Si alloys cease to be completely effective in preventing junction spiking. The precipitation that occurs during the cooldown from the first thermal cycle (e.g., the sinter step) can cause the Al near the contact interface to contain an Si concentration that is lower than that needed for solid solubility during subsequent processing steps. When the wafer is heated again (e.g., during the deposition of the passivation film or during the die-attach or packaging process), Si from the substrate can diffuse into the Al.

Second, when high current densities are passed through Al-Si contacts, the electron current leads to the transport of Si from the contacts into the Al. This leads to spiking of the junction at the negative terminal and deposition of Si at the positive terminal. Such susceptibility to *contact electromigration failures* also increases as the contact area is reduced.

In summary, the simple Al-Si contact structure that was used extensively for NMOS IC fabrication has become increasingly less suitable for advanced CMOS and bipolar integrated circuits, even if an Al:Si alloy is used for the metallization. As a result, more elaborate contact structures that can overcome the limitations of the Al-Si contact have had to be developed.

3.4.5 Platinum Silicide-to-Silicon Contacts

An early approach to overcoming the junction-spiking problem of Al-Si contacts used a platinum-silicide layer (PtSi) between the Si and Al in the contact structure. Not only could such contacts withstand temperatures of $350\text{--}400^\circ\text{C}$ without junction spiking, but they also exhibited two other advantages over Al-Si contacts: (1) they offer a self-alignment capability, which restricts the formation of the PtSi layer to the region in the contact hole without there being a need for additional masking steps; and (2) they exhibit excellent electrical characteristics, due to the mechanism by which the silicide is formed. That is, the PtSi layer is formed by reacting a Pt layer in contact with Si at low temperatures ($250\text{--}400^\circ\text{C}$). Rapid diffusion and reaction of the Pt occur at such low temperatures, allowing the silicide to be produced. During the growth process, the original contaminants from the Pt-Si interface are swept to the surface of the newly formed silicide, and the PtSi-Si interface is buried beneath the original Si surface. As a result, an absolutely clean and intimate silicide-silicon contact is formed.³⁹

Platinum-silicide layers are able to provide low contact resistivity for ohmic contacts to both n^+ and p^+ Si (approximately a factor of two lower than the Al-to-Si contacts described in an earlier section), and they provide a film that is stable with respect to the silicon substrate for process temperatures in excess of 500°C. They also exhibit relatively high conductivities. For example, PtSi films of 60-nm thickness exhibit a sheet resistivity of $\sim 34 \mu\Omega\text{-cm}$.

The first application of PtSi contacts to silicon technology was reported by Hosack in 1972.³⁷ Since that time, numerous other noble and near-noble silicides (e.g., Pd_2Si , CoSi_2 , and NiSi), and refractory metal silicides (TiSi_2 , WSi_2 , MoSi_2 , and TaSi_2) have also been investigated for this purpose. The electronics industry, by and large, early on adopted PtSi-Si for Schottky diodes and ohmic contacts to bipolar transistors. (PtSi Schottky contacts will be described in section 3.7.) The properties and fabrication technology of CoSi_2 and TiSi_2 will also be described later, as these two silicides have been incorporated into advanced contact structures. A recent study on the applicability of Pd_2Si ohmic contacts has indicated that they may also offer many attractive benefits for VLSI applications.³⁸

3.4.5.1 Process Sequence Used to Form PtSi-Si Contacts. The process sequence used to form the PtSi layer in the contact hole (Fig. 3-23) includes the following steps:

1. After an opening is etched in the SiO_2 layer, the surface of the silicon is subjected to an additional cleaning step, such as a dip in dilute HF just prior to loading of the wafers into the sputter chamber, or preferably, an in situ sputter etch. This step is important, because a smooth PtSi-Si interface of uniform penetration requires a Si surface that is free of contaminants and has a minimal native oxide. (i.e., planar, very shallow PtSi-Si interfaces are needed to prevent junction penetration of shallow junctions by the growing silicide layer.) Figure 3-24 shows the effect of the surface quality on the smoothness of the PtSi-Si interface; it can be seen that a contaminated Si surface leads to a PtSi layer of irregular depth.^{40,41} It has also been reported that as long as the native oxide on the Si surface is less than 20 Å thick, the PtSi layer will form and, in doing so, will break up the oxide layer and sweep the oxygen to the PtSi surface. On the other hand, thicker native-oxide layers will inhibit the formation of PtSi.

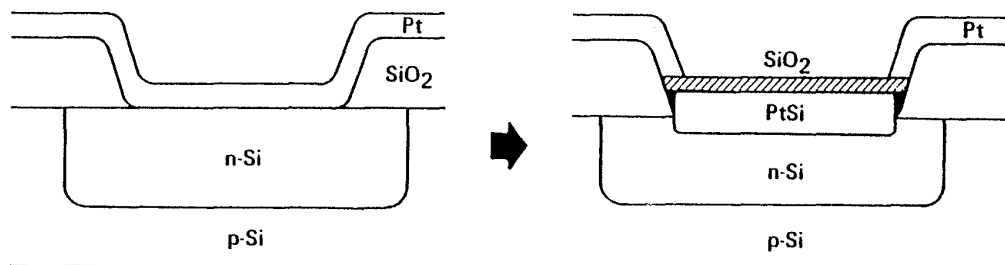


Fig. 3-23 Formation of self-aligned PtSi-Si contacts.

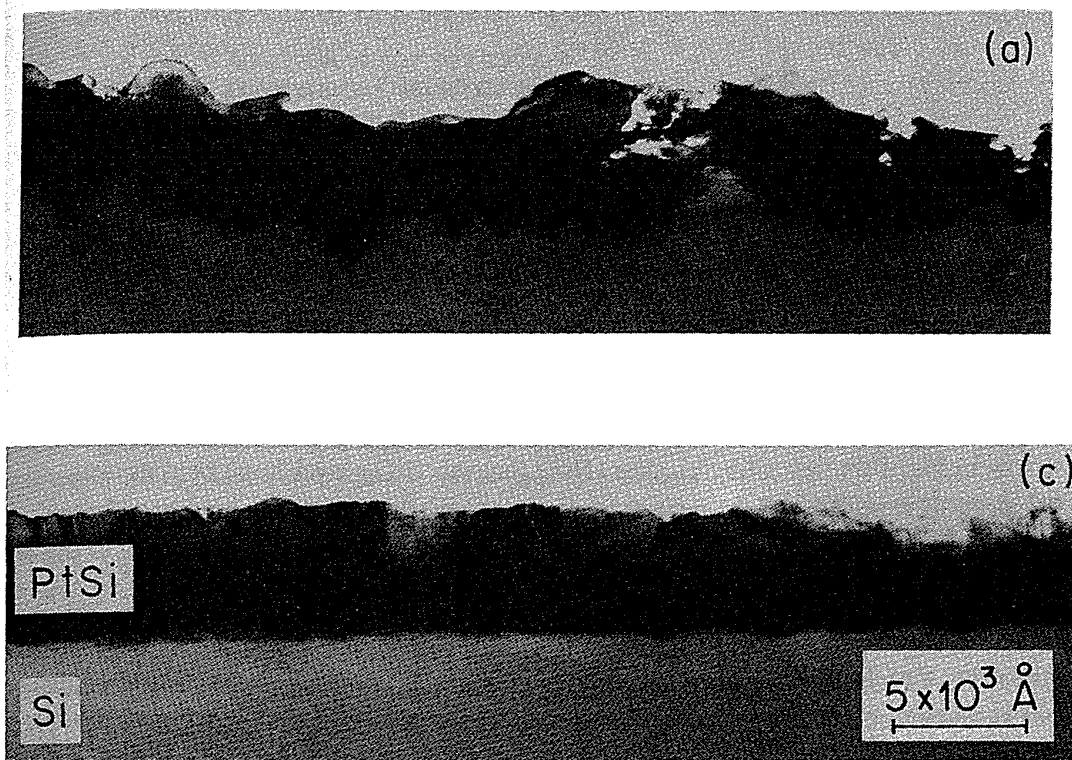


Fig. 3-24 The effect of the surface quality on the smoothness of the PtSi-Si interface. It can be seen that a contaminated Si surface leads to a PtSi layer of irregular depth. (a) shows the rough PtSi-Si interface grown from a severely contaminated surface. (c) shows a smooth, uniform PtSi-Si interface that results when the PtSi is formed on a clean Si film.⁴⁰ Copyright 1984. Reprinted with permission of the AIOP.

2. A thin Pt film is then sputter deposited onto the wafer surface to a thickness of 30-60 nm. This thickness range produces silicide layers thick enough to provide good contact properties but without consuming an excess amount of Si below the contact. In forming the silicide layer, Si is consumed to about the same depth as the thickness of the Pt film (e.g., 50 nm of Pt will react with ~60 nm of Si to form a 100-nm-thick PtSi film). A slow sputter-deposition technique (such as *rf sputtering*) is commonly employed in order to maintain adequate thickness control for such thin Pt layers. A clean Si surface (i.e., with a native oxide no thicker than ~10 Å) and a deposition process that does not allow oxygen to be incorporated into the Pt film are both critically important, since the growth of the PtSi layer can be inhibited by the presence of oxygen.

3. The silicide is then formed by heating the wafers in an N₂ ambient. During the annealing process, the Pt reacts with the Si in the contact hole to form

PtSi, but it does not react wherever it is in contact with the SiO_2 . Toward the end of this annealing step, some oxygen is introduced into the furnace. This causes a thin film of SiO_2 to grow on the surface of the just formed PtSi, but no such oxide is grown on the unreacted Pt regions. Various temperatures have reported for the annealing process, but 550°C for 10 minutes is typical. Chang et al., however, have reported that a three-temperature sequence at 200°C - 350°C - 550°C yields PtSi films with improved properties. (The formation and properties of the passivating-oxide film on top of the PtSi under various annealing conditions are also described by Chang.)⁴² An RTP process for reacting the Pt has also been published.⁴¹

4. The unreacted Pt is then stripped from the wafer surface by etching in a dilute aqua regia solution at 85°C . The aqua regia, however, does not attack the PtSi because of the protective layer of SiO_2 that was grown on it during the last part of the annealing process. Note that this SiO_2 layer must be removed prior to deposition of the next layer of metal onto the (sputter etching, e.g., has been effectively used for removal of this film).⁴³

3.4.5.2 Limitations of the PtSi-Si Contact Structure. Junctions under PtSi-Si interfaces exhibit no degradation (e.g., leakage or shorting) up to temperatures of 800°C . Unfortunately, when an Al layer is deposited onto the PtSi, such junctions undergo junction spiking failures if temperatures exceed 350°C . This occurs because above this temperature, the Al begins to react with the underlying PtSi, causing it to decompose and form various Pt-Al-Si intermetallic compounds. Once the aluminum-silicide reaction front reaches the silicide-Si interface, silicon pits and aluminum spikes are created almost immediately, and shallow junctions rapidly become shorted.

In the early days of IC processing, when device junctions were $0.5\ \mu\text{m}$ in depth (or deeper) and the contact areas were $>10\ \mu\text{m}^2$, such (Al-PtSi-Si) contacts were nevertheless able to maintain adequate junction stability if the annealing temperatures following metallization were limited to 400°C . When the device junctions became shallower than $0.25\ \mu\text{m}$, however, the Al-PtSi-Si contact (and all other near-noble silicide contacts) could no longer prevent junction spiking at annealing temperatures of 400°C . As a result, it became necessary to introduce yet another barrier layer between the PtSi and the Al to allow the contacts to survive temperatures exceeding 400°C (see Fig. 3-26a). Such so-called *diffusion barriers* will be described in the next section.

PtSi also has two other characteristics that also need to be mentioned. First, because PtSi layers agglomerate at temperatures above 800°C , post-Pt deposition temperatures are limited. Second, the formation of the PtSi occurs in a lateral, as well as a vertical direction. Thus, a 100-nm-thick PtSi layer also penetrates $\sim 100\ \text{nm}$ under the edge of the contact oxide window. In the case of a MOSFET with a gate length of $1.0\ \mu\text{m}$, this would reduce the nominal gate length by 20%. Several approaches have been investigated to minimize this effect, including the deposition of Si and Pt together and the deposition of an alloy of Pt and W (Fig. 3-25). These approaches are reviewed by Tu in reference 44.

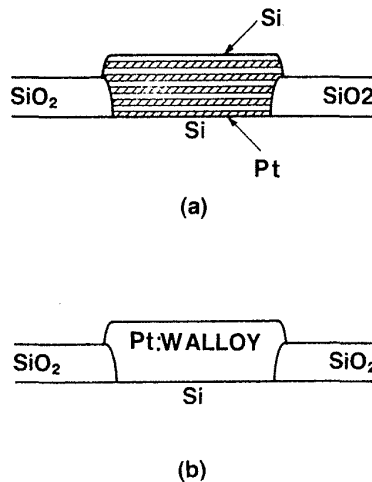


Fig. 3-25 Two approaches investigated to minimize the effect of excess Si consumption during PtSi formation: (a) the deposition of Si and Pt together, and (b) the deposition of an alloy of Pt and W.⁴⁴ Copyright 1981. Reprinted with permission of the AIOP.

3.5 DIFFUSION BARRIERS

3.5.1 Theory of Diffusion Barrier Layers

The intermixing of materials from two layers in contact (such as Al and Si) can be prevented by sandwiching another material between them (Fig. 3-26). The role of this third material is to prevent (or at least retard) the diffusion of the two original materials into each other, or to resist the tendency of a chemical reaction to form a new phase between the adjoining materials. In practice, the available diffusion barrier materials are not perfect: they are capable of extending the life of devices only to some degree, not indefinitely. The efficiency of such a diffusion barrier is therefore determined by how long it can extend the lifetime of the contact structure under various thermal treatments, compared to its lifetime without a diffusion barrier. End-of-contact-life (or *contact failure*) occurs when the junction under the contact is short-circuited (e.g., by junction spiking) or when the contact exhibits open-circuit or high-resistance behavior.*

A diffusion barrier used in IC fabrication is a thin film (i.e., material X between materials A and B in Fig. 3-26b) inserted between an overlying metal and an underlying

* Note that diffusion barriers are also used in many other applications besides microelectronics. For example, the paint on wood, the galvanizing on metal, and the wax coating on cardboard containers all serve the same purpose – that is, such barriers are used to protect the underlying materials by preventing diffusion of substances, such as moisture, that would degrade their properties.

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