

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: April 30, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00191
Patent 11,581,322

PATENT OWNER'S PRELIMINARY RESPONSE

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REGULATIONS

37 C.F.R.

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Exhibit List

Ex.	Description
2001	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)
2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
2004	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 14, 2025), ECF No. 243
2005	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending <i>Inter Partes</i> Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2006	Disclaimer in Patent Under 37 C.F.R. § 1.321(a)
2007	Declaration of Dr. Stephen A. Campbell ("Campbell")
2008	<i>Curriculum Vitae</i> of Dr. Stephen A. Campbell

Ex.	Description
2009	<i>Inside Solid State Drives (SSDs)</i> (Rino Micheloni et al. eds., 2d ed. 2018)
2010	RESERVED
2011	RESERVED
2012	RESERVED
2013	RESERVED
2014	RESERVED
2015	RESERVED
2016	RESERVED
2017	RESERVED
2018	Order Granting Motion to Consolidate, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Aug. 21, 2024), ECF No. 106
2019	RESERVED
2020	U.S. Patent Application Publication No. 2007/0358593 A1, Published Dec. 14, 2017

I. Introduction

Patent Owner Yangtze Memory Technologies Company, Ltd. (“YMTC”) respectfully submits this Preliminary Response to the Petition for *inter partes* review of U.S. Patent 11,581,322 (“’322 Patent”). As explained below, Petitioner has failed to carry its burden to show a reasonable likelihood that at least one of the challenged claims is unpatentable. Thus, the Board should deny the Petition and no IPR proceeding should be instituted.

The ’322 Patent describes and claims innovative methods for forming 3D memory structures with a vertical “through array contact,” or “TAC,” and “dummy channel structure” that extends through a stack of dielectric and sacrificial layers. ’322 Patent, 3:45-65, 5:6-9. The ’322 Patent claims such memory structures with (i) “dummy channel[s]” that provide mechanical support, and (ii) a TAC having “a substantially circular section.” *See id.*, cls. 3, 6, 8-10, 13-16, 19-20.

Petitioner asserts that the challenged claims are invalid in view of Nishikawa alone or in combination with Nishikawa2. Nishikawa does not disclose dummy channels or a TAC having a substantially circular section. Petitioner tries to supply those missing limitations by invoking the “general knowledge” of a person of ordinary skill in the art (POSITA). But “[t]he Court of Appeals for the Federal Circuit has held that the Board is permitted to rely on general knowledge to supply a missing claim limitation in an *inter partes* review, such as when ‘the missing

limitation in question [is] *unusually simple* and the technology *particularly straightforward*.” *Motorola Mobility LLC v. Lagan Precision Co.*, IPR2024-00688, Paper 7 at 29 (Oct. 28, 2024) (original alteration and emphases) (denying institution). Those exceptions do not apply here.

The claimed “dummy channels,” and TACs having “a substantially circular section” are not “unusually simple” and the field of 3D NAND memory manufacturing is not “particularly straightforward.” *Campbell* (Ex.2007) ¶28. They are highly technical and complex. *See DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018) (rejecting Board’s reliance on “common knowledge” to “supply a missing claim limitation” because wireless communications is not “particularly straightforward” technology) (citations omitted). Petitioner’s reliance on the “knowledge of a POSITA” to supply missing limitations is legal error.

Petitioner also relies on Nishikawa2 for the “circular section” TACs missing from Nishikawa, arguing for replacing Nishikawa’s trench structure with a circular TAC. But Petitioner ignores a critical feature of Nishikawa’s trench structure, which includes isolating two distinct wordlines at each conductive level of the stack. As a result, Petitioner’s proposed combination would result in a short circuit, rendering each memory cell inoperable for its intended purpose—

demonstrating that a POSITA would not have made the proposed combination.

Grounds 1 and 3 fail for this additional reason.

The Board should deny institution.

II. Background

A. 3D NAND Memories

3D NAND memory devices are “memory arrays” with memory cells stacked one on top of the other. Memory cells can be written or read by applying a voltage to corresponding conductors that run horizontally across the memory array, called “wordlines.” An exemplary 3D NAND memory is shown in Figure 5.20 of Exhibit 2009, which depicts a series of vertically stacked memory cells, each controlled by a “Control Gate” (the wordline) shown in red as “CG0” through “CG3.” Ex.2009, 119. The ends of the “Control Gates” are staggered to form a staircase that allows vertical vias to access and contact each wordline (CG0 to CG3) and connect them to peripheral devices.

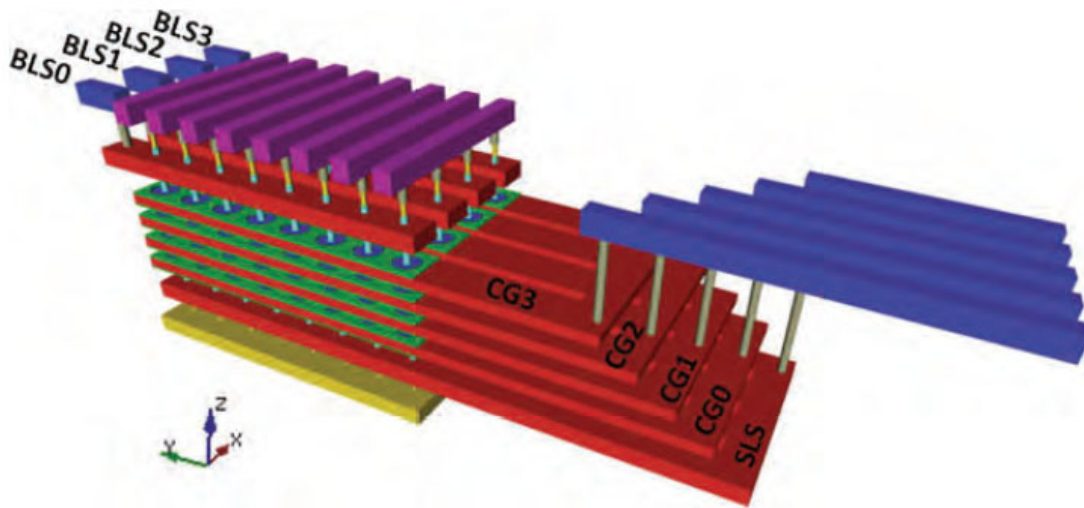


Fig. 5.20 C-FG NAND Flash array with fan-out

B. The '322 Patent (Ex.1001)

The '322 patent recognized that 3D memory devices require contacts that go vertically through the memory stack called “through array contacts” or “TACs” for “providing vertical interconnects between the stacked memory array device and peripheral device (e.g., for power bus and metal routing).” ’322 Patent, 4:58-62. In the past, these TACs were formed within a “barrier structure[]” to “preserve[] a dielectric stack region within a memory stack for ease of etching the openings of the TACs.” *Id.*, 4:62-65. The drawbacks of a “barrier structure[]” is that “the regions enclosed by the barrier structures take up large area in the core array region where memory strings can be formed.” *Id.*, 4:62-5:1; Campbell ¶23 (discussing prior art examples of barrier structures). TACs within a barrier structure “also have a negative impact on the resistance of word lines.” *Id.* “Moreover, the

existing fabrication processes for forming the barrier structures become more challenging for the next-generation 3D memory devices,” which “have less process margin.” *Id.*, 5:2-5.

The '322 Patent discloses a novel “3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures.” *Id.*, 5:6-9. The '322 Patent explains that, “by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost.” *Id.*, 5:9-12. In addition, “[m]ore process margin”—i.e., room for error—may “be obtained due to the elimination of etching and alignment steps for making the barrier structures.” *Id.*, 5:13-18. To “further simplify the fabrication flow and reduce process cost,” the '322 Patent teaches that the non-barrier structure TACs can be “formed in the same fabrication process(es) for making other structures” such as “peripheral contacts” outside of the memory stack. *Id.*, 5:17-23. As a result, the non-barrier structure TACs 416 can have a same shape as the peripheral contact 420, including a “substantially circular shape in the plan view,” as shown in Figure 4C below where the circular cross section of the TAC (green box) matches the circular cross section of the peripheral contact (blue box). *Id.*, 8:56-57; Campbell ¶24.

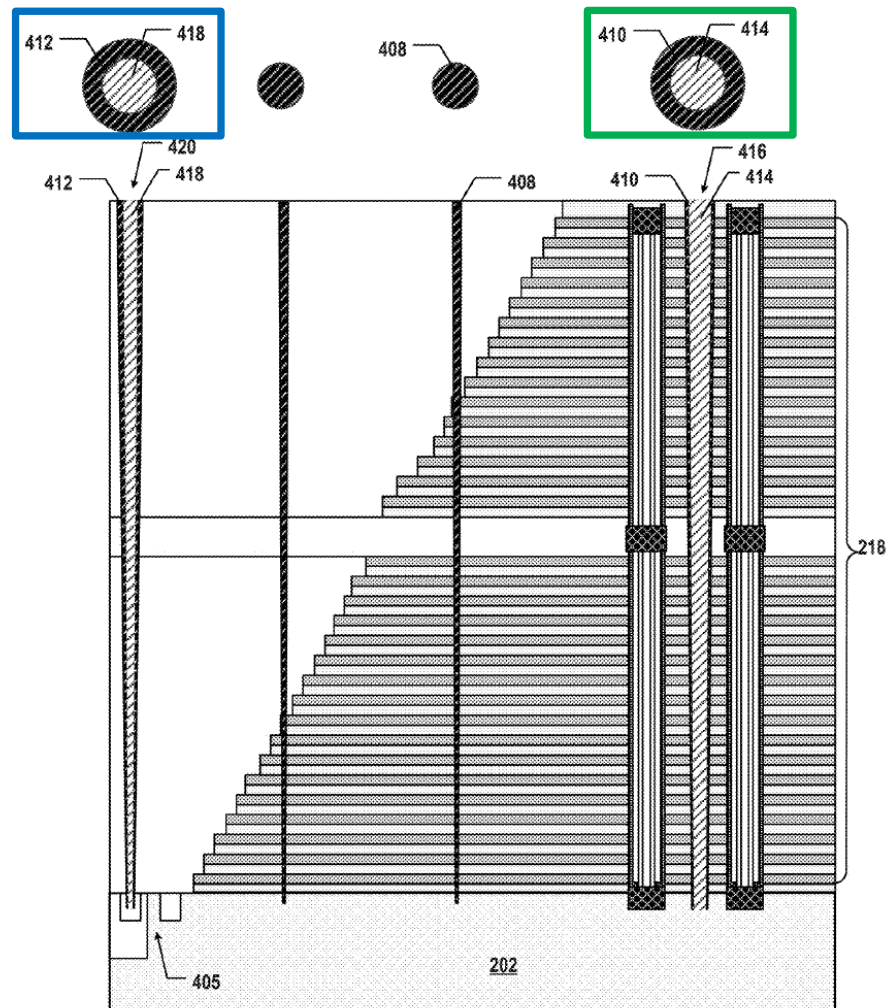


FIG. 4C

'322 Patent, Fig. 4C**C. Person of Ordinary Skill in the Art**

YMTC takes no position on the level of ordinary skill in the art for the purposes of this Preliminary Response, as the Petition has failed to establish a reasonable likelihood of prevailing under any reasonable definition of POSITA. Campbell ¶22.

D. Claim Construction

The prior art relied on in the Petition fails to disclose the subject matter of the challenged claims under any reasonable construction, including their plain meaning.¹

III. Grounds 1 and 3: Claims 3, 6, 8-10, 13-16, and 19-20 are not obvious based on Nishikawa alone or in combination with Nishikawa2.²**A. Nishikawa and the POSITA's Knowledge Do Not Teach or Suggest a "dummy channel structure... extending vertically through the conductor/dielectric layer pairs in the memory stack" (claims 3, 6, 14)**

Independent claim 14, and dependent claims 3 and 6, recite "a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack." Claims 15-20 depend from claim 14.

¹ Patent Owner reserves the right to advocate for claim constructions if the Board institutes review.

² YMTC disclaimed claims 1-2, 4-5, and 7. *See* Disclaimer in Patent Under 37 C.F.R. § 1.321(a) (Ex.2006). The Board cannot institute an IPR on a disclaimed claim. 37 C.F.R. § 42.107(e); *Intuitive Surgical, Inc. v. Ethicon LLC*, IPR2018-01248, Paper 7 at 2 n.1, 9-10 (Feb. 7, 2019). Thus, the Board cannot institute an IPR on claims 1-2, 4-5, and 7.

Petitioner acknowledges that Nishikawa does not disclose any dummy channels. Pet. 59; *see also id.* at 82. Nishikawa thus does not disclose dummy channel structures “extending vertically through the conductor/dielectric layer pairs in the memory stack,” as claimed.

Petitioner asserts that “a POSITA would have been motivated, with a reasonable expectation of success, to include dummy channels (of either the same materials or with a solid dielectric fill).” *Id.* Petitioner does not rely on combining Nishikawa’s teachings with any other prior art. Even in Ground 3, where Petitioner combines Nishikawa with Nishikawa2 for a “circular TAC” in claims 8 and 14, Petitioner states that “Ground 3 applies the same claim mapping and arguments as Ground 1.” Pet. 98. Thus, for all grounds, Petitioner relies exclusively on “the knowledge of a POSITA” to support its proposed modification of Nishikawa “to include dummy channels” that are indisputably missing from Nishikawa. Pet. 59.

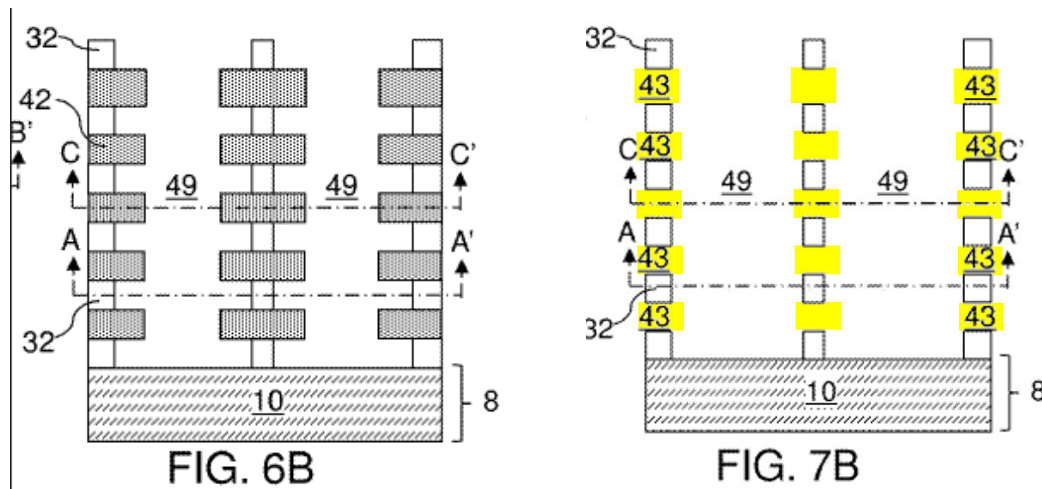
Petitioner’s reliance on the knowledge of a POSITA to supply the dummy channels missing from Nishikawa fails both legally and factually. As a matter of law, Petitioner’s reliance on general knowledge is misplaced because Petitioner has failed to demonstrate that “the missing limitation in question [is] *unusually simple* and the technology *particularly straightforward.*” *Motorola Mobility*, IPR2024-00688, Paper 7 at 29 (original alteration and emphases) (denying institution)

(citation omitted). To the contrary, forming a dummy channel structure involves complex semiconductor manufacturing processes, including “wet etching, and/or dry etching, such as DRIE” and “thin film deposition processes, such as ALD, CVD, PVD.” Campbell ¶28; ’322 patent, 12:10-27. And 3D NAND technology is plainly not “particularly straightforward.” *See DSS Tech. Mgmt.*, 885 F.3d at 1374 (rejecting Board’s reliance on “common knowledge” to “supply a missing claim limitation” because wireless communications is not “particularly straightforward” technology); Campbell ¶26. Petitioner’s reliance on “general knowledge” to supply the indisputably missing limitations directed to forming “dummy channels” is legal error. Petitioner’s arguments as to claims 3, 6, and 14 fail for this reason alone.

Petitioner’s argument fails on the facts too. Petitioner asserts that it would have been obvious to “include dummy channel structures to provide structural support” when using a “gate replacement process.” Pet. 60. According to Petitioner, “support pillars” are “necessary” in order to “perform [Nishikawa’s] gate replacement process.” Pet. 62. Petitioner is wrong. A POSITA would not be motivated to modify Nishikawa as proposed.

First, Nishikawa already discloses structures that provide support during its gate replacement process. *See* Nishikawa (Ex.1005) 10:10-12 (“[S]eparator dielectric structures 45 can provide structural support to the insulating layers 32

after formation of the interlayer cavities 43"). During the gate replacement process of Nishikawa, shown in Figure 7B as annotated below, "recesses 43" (yellow) are formed where the sacrificial material layers 42 once were. *Id.*, 10:8-10; Campbell ¶¶30-31. The separator dielectric structures 45, which are not shown in Figure 7B, "provide structural support to the insulating layers 32" to maintain recesses 43 (yellow) in the structure even after removal of the sacrificial material layers 42. Nishikawa 10:10-12; Campbell ¶31.



Nishikawa, Figs. 6B, 7B

Figures 7A and 7C illustrate top views of the device at the elevations shown, respectively, as A-A' and C-C' in Figure 7B. These figures show that the separator dielectric structures 45 connect to the insulating layers 32 (Fig. 7A) to provide support and maintain the recesses 43 (Fig. 7C).

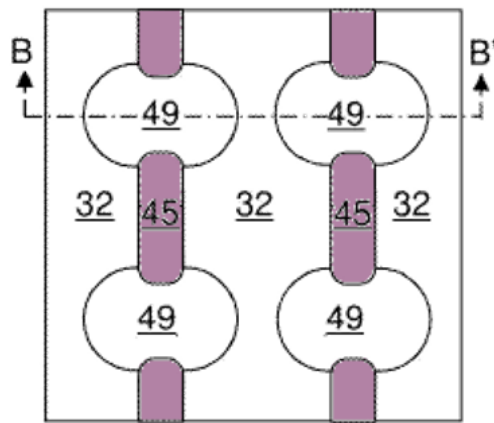


FIG. 7A

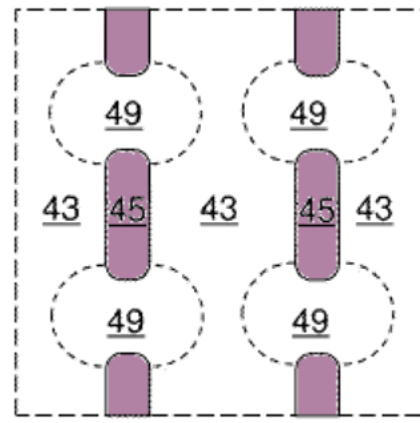
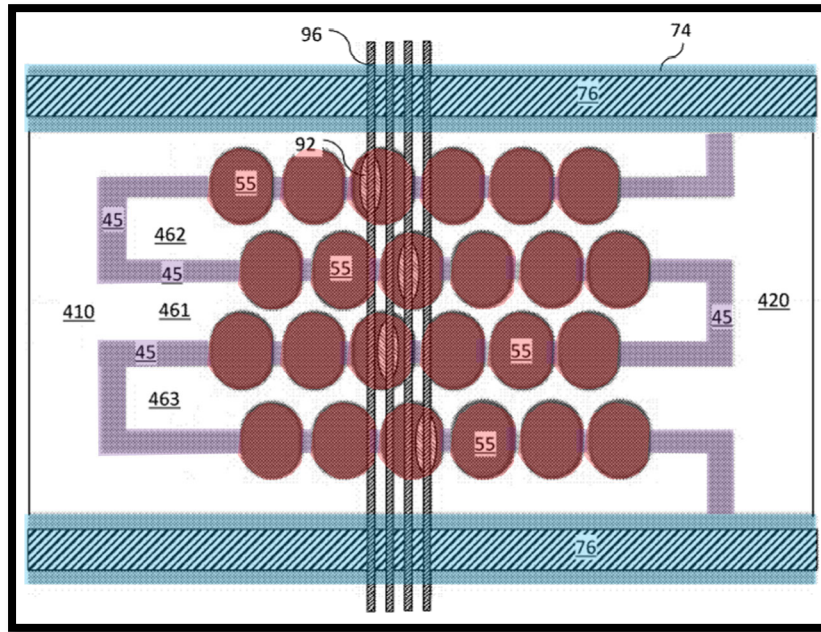


FIG. 7C

Nishikawa, Figs. 7A, 7C

If they did not, the insulating layers 32 would collapse into the recesses 43 below and the Figure 7B structure could not exist. Campbell ¶32.

As shown in Figure 16, below, the separator dielectric structures 45 (purple) in the final memory device are disposed throughout the device and are therefore able to provide sufficient structural support during the gate replacement process. *See* Nishikawa, 17:14-18 (“The separator dielectric structures 45 extend through the stack, contact portions of outer sidewalls of the memory stack structures 55, and laterally separate the control gate electrodes 46 of the plurality of charge storage elements.”).



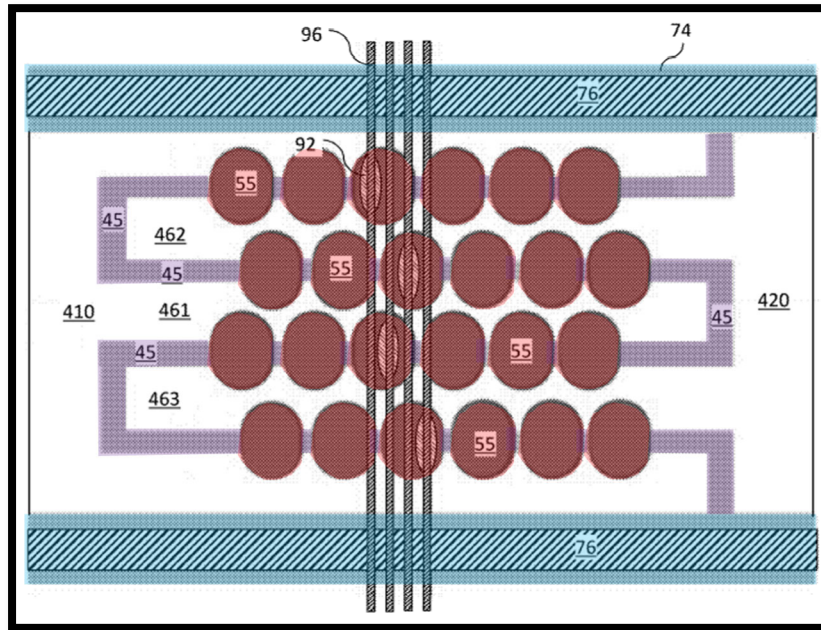
Nishikawa, Figure 16

Indeed, Petitioner has not alleged that separator dielectric structures 45—which are indisputably not the claimed “dummy channel structures”—are inadequate to provide the required support as expressly shown in Figure 10. Nor has Petitioner identified any other benefit to adding the claimed “dummy channel structures” to Nishikawa. *See, e.g.*, Pet. 59-60. A POSITA would not be motivated to “include dummy channels” as Petitioner proposes, because Nishikawa already includes a different structural support, and Petitioner identifies no other reason to include “dummy channels” other than to provide structural support. In other words, Petitioner fails to identify any evidence that adding “dummy channels” to Nishikawa would serve any purpose. *South-Tek Sys., LLC v. Engineered Corrosion Sols., LLC*, 748 F. App’x 1003, 1007 (Fed. Cir. 2018)

(agreeing with PTAB's finding of no motivation to combine because a POSITA would not have modified prior art to add a drain where the prior art "already includes a drum drip drain that serves this purpose" and would be "redundant").

Second, Petitioner does not provide any explanation about where (or how) the alleged dummy channels would be formed.³ As discussed, Nishikawa already discloses separator dielectric structures 45 (shown in purple below) that "extend through the stack." Nishikawa 17:14-18.

³ In a prior petition challenging the related '254 patent, Petitioner asserts that "it would have been obvious to implement some of [the prior art reference]'s channels as dummy channels." *Micron Tech., Inc. v. Yangtze Memory Techs. Co.*, IPR2025-00034, Paper 1 at 39 (Oct. 11, 2024). Here, Petitioner does not propose modifying any existing structures to be "dummy channels" and instead asserts only that a POSITA would "include dummy channels" with no further explanation about where or how such structures would be implemented. Pet. 59.



Nishikawa, Fig. 16

Petitioner fails to explain where Petitioner proposes that the additional proposed “dummy channels” would be formed “through the stack.” That is especially problematic given that there are the other structures already formed through the stack that provide structural support. Accommodating dummy channels “through the stack” would require either (1) increasing the size of the stack to create space for the dummy structures, or (2) decreasing the memory’s storage capacity by replacing functional “memory stack structures 55” (which serve as channels for the memory cells (Nishikawa 4:28-32)) or “contact via structures 66” (which provide external access to the word lines (*id.*, 6:45-47)) with *non*-functional dummy channels. Campbell ¶¶33-35. Petitioner does not argue that a POSITA would have sought to do either. Indeed, a POSITA would

recognize that either approach would be undesirable—and thus would not have been motivated to implement such a modification—especially where there is no need for the dummy channels at all, as discussed above. *Id.*

Third, adding dummy channels will add more processing steps and more complexity to the Nishikawa process. *Id.* ¶36. Petitioner's proposed modification therefore increases manufacturing complexity, without serving any beneficial purpose—while also either increasing device size or decreasing storage capacity, either of which is undesirable. *See supra*. Petitioner does not contend otherwise.

Petitioner resorts to citing five references—Nishikawa2, Masamori, Kai, Kim, and Park—that purportedly “confirm[] the knowledge of a POSITA” that “it was well known to include dummy channel structures to provide structural support.” Pet. 60-62. But just because dummy channels were purportedly “well known” does not mean a POSITA “would have been motivated to make the combinations or modifications” **to Nishikawa** to use dummy channels—especially when Nishikawa already has other structures that provide structural support. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”); *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) (conclusion that a combination “would have

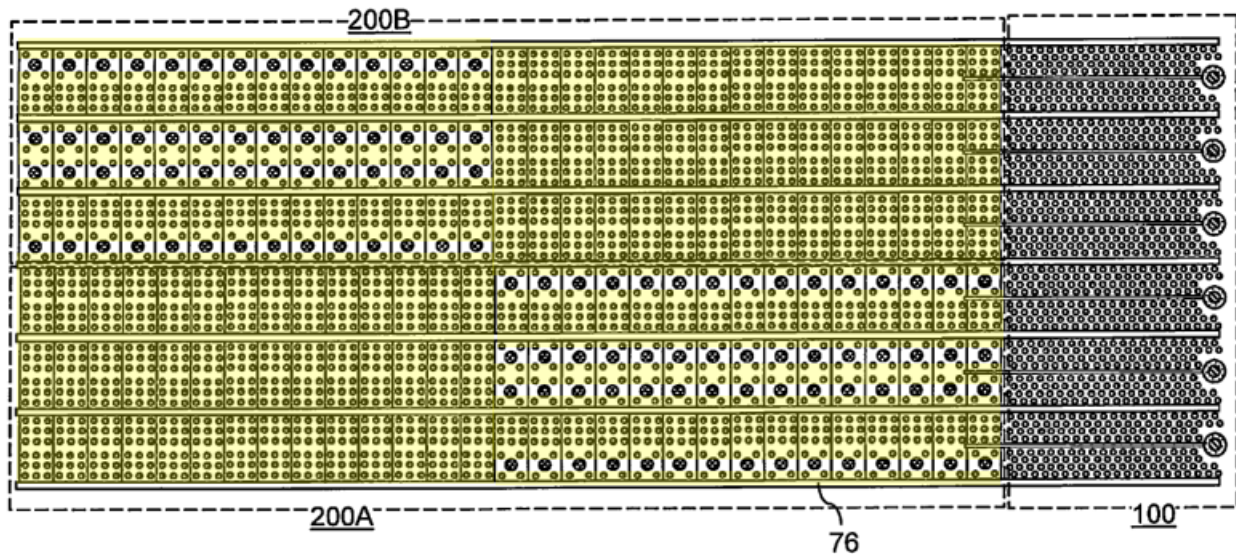
allowed for” a claimed limitation “is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention”) (citations omitted).

None of the five references Petitioner cites show that a POSITA would have added dummy channels to Nishikawa, where separator dielectric structures 45 already provide adequate structural support as discussed above. Campbell ¶¶37-43. Instead, all five references disclose, at most, devices with “regions” (that Nishikawa lacks) to accommodate the alleged “dummy channels.”

For example, Petitioner quotes Nishikawa2 as “recogniz[ing] the need for support structures.” Pet. 60 (citing Nishikawa2 (Ex.1046), 9:63-67 (“At least one dielectric pillar structure (not shown) can be formed through the entire set of the spacer material layers 42 and the insulating layers 32...”). But the cited passage merely describes the formation of a “not shown” dielectric pillar structure and says nothing about a “need” for support structures, let alone describe any motivation to add support structures to Nishikawa’s device that already has them. Nor does Petitioner assert that Nishikawa2 discloses dummy channels. *Id.*; Campbell ¶38.

Petitioner also cites to Masamori, which discloses “conductive support structures.” Masamori (Ex.1020), Cover (Title). Unlike Nishikawa, Masamori’s design does not include separator dielectric structures that provide structural support during the gate replacement process. Campbell ¶39. Masamori devotes an

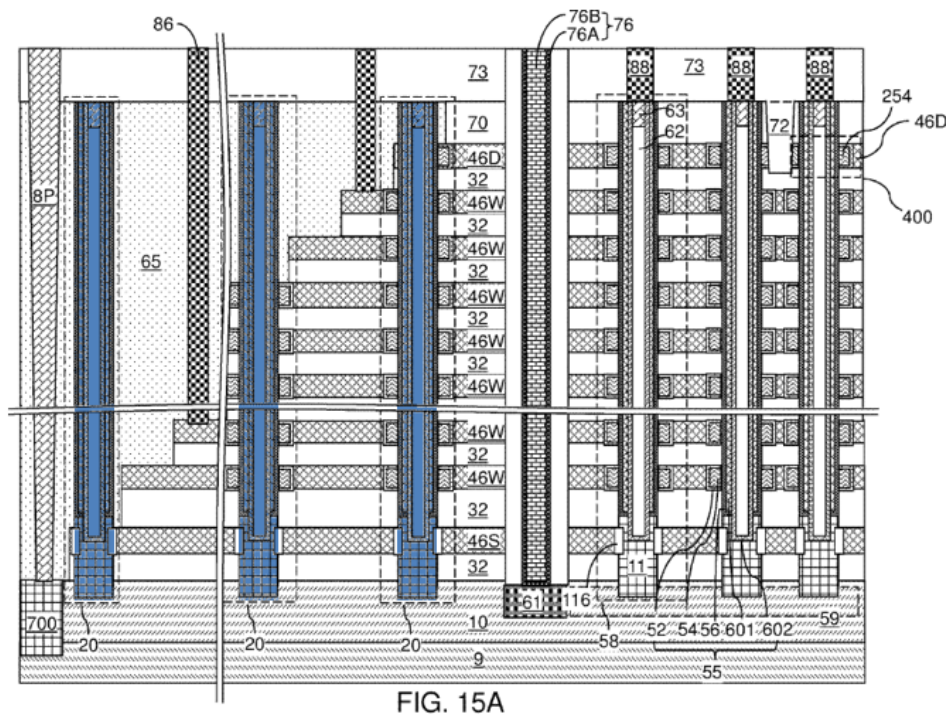
enormous area (yellow) (most of contact regions 200A, 200B) to these support structures, as shown in Figure 20B, annotated below. Further, mere disclosure of support structures in Masamori does not motivate modifying Nishikawa—a different design with separator dielectric structures 45 that already provide the structural support Petitioner asserts is needed for gate replacement. Campbell ¶39.



Masamori Fig. 20B

Petitioner's other references also do not support modifying Nishikawa. Kai discloses "support pillar structure[s] 20" taking up significant area in a "contact region 300" in a device that (unlike Nishikawa) (1) includes no separator dielectric structures supporting the other structures during gate replacement, and (2) has a very different layout than Nishikawa. Kai (Ex. 1027), Fig. 6A, 6:2-5, 16:28-31; *see also id.*, Fig. 15A (below) (showing "support pillar structure 20" (blue) only in the connection region); Campbell ¶40. Nothing in Kai (let alone the general

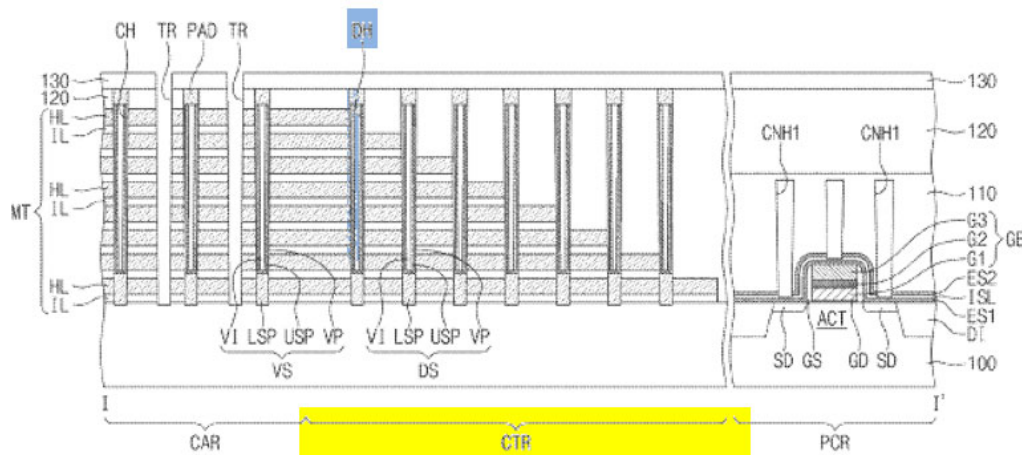
knowledge of a POSITA) motivates adding such structural supports to Nishikawa, which already includes separate supporting structures. Campbell ¶40.



Kai Fig. 15A (annotated)

Kim's Fig. 13, annotated below, similarly discloses that its "dummy holes DH" (blue) are in a "connection region CTR" (yellow). Kim 559 (Ex.1029) [0047] ("The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region CTR").

FIG. 13

**Kim Fig. 13 (annotated)**

Similarly, Park is about a “semiconductor device” that includes “dummy regions” separate from the rest of the memory. Park (Ex.1028), Abstract; Campbell ¶¶41-42.

Thus, at most, the cited references, Nishikawa2, Masamori, Kai, Kim, and Park, teach forming support structures in circuits that (1) have regions designed to accommodate them, such as huge portions of a “word line contact via region 200” (Masamori), “contact region” (Kai), “connector region CTR” (Kim), or “dummy region” (Park); and/or (2) lack a separator dielectric structure as existing support during the gate replacement process. Campbell ¶43. The Nishikawa device includes no such regions designed to accommodate dummy channels, and Petitioner fails to explain how, why, or where a POSITA would form such regions

in the Nishikawa device. Campbell ¶43. Petitioner's failure to provide any such explanation is particularly problematic because Nishikawa already devotes precious space to providing sufficient structural support. Campbell ¶¶44. Petitioner's argument to include "dummy channels" in Nishikawa is nothing more than hindsight reconstruction of the claimed invention, adding a feature to Nishikawa that it does not need without articulating why or how a POSITA would have done so. *In re Entresto*, 125 F.4th 1090, 1100 (Fed. Cir. 2025) (affirming claims to combination drug therapy as non-obviousness because there was no motivation to combine the separate therapies and challenger "impermissibly use[d] [claimed combination] as a starting point and 'retrace[d] the path of the inventor with hindsight'").

Petitioner's remaining arguments fail as well. Petitioner points to various alleged reasons why dummy channels are suitable to use as "support structures"—e.g., that they "can be made by the same process and at the same time as the active channels," "do not require connections to upper-level devices," and "provide[] additional structural support." Pet. 60-63. Petitioner misses the point. As discussed, Nishikawa already discloses that its separator dielectric structures 45 provide structural support for the memory array during the gate replacement process. *See supra*; Nishikawa, 10:10-12. Petitioner does not (as it cannot) argue that those separator dielectric structures 45 do not serve that purpose. *See supra*.

Thus, even if dummy channels may be suitable “support structures” in other semiconductor structures that do not have them, a POSITA would not be motivated to implement them in Nishikawa as Petitioner proposed. Campbell ¶44.

Petitioner also argues that dummy channels improve “uniform[ity]” and “reduce the likelihood of defective bits on the edge of the memory cell region, because the additional rows of dummy channel structures extend the memory cell pattern to include the dummy region on the edges.” Pet. 59. Petitioner cites nothing in Kai, Kim, Park, or anything else from the relevant timeframe that teaches “additional rows” that “extend[] the memory cell pattern.” *Id.* To the contrary, as discussed, those references do not disclose dummy structures in the memory cell area at all; they instead only disclose dummy channels *outside* of the memory cell. *See supra*; Campbell ¶45.⁴ And Petitioner ignores the fact that adding “additional rows” in the “memory cell pattern” will increase device size, which a POSITA would understand is not desirable. Campbell ¶46. To the extent that dummy structures may have benefits such as improving uniformity, such

⁴ Although Dr. Lee asserts that dummy channels can be employed “at the edge of the array” to provide support to mitigate abnormalities (Ex.1003, ¶141), he fails to show that this is a concern in Nishikawa, which has sufficient support structure. Campbell ¶44.

benefits stem from evenly spacing dummy structures throughout the device.

Petitioner provides no explanation how this would be implemented in Nishikawa, which already discloses separator dielectric structures 45 extending through the stack. *See supra*.

In short, Petitioner fails to identify evidence that a POSITA would be motivated to modify Nishikawa to add dummy channels as Petitioner proposes.

B. A POSITA Would Not Have Been Motivated to Modify Nishikawa To Render Obvious “a through array contact (TAC)” with “a substantially circular section” (Claims 8, 14, 19)

Independent claims 8 and 14, as well as dependent claim 19, recite a TAC comprising “a substantially circular section.” Claims 9-13 depend from claim 8, claims 15-18 and 20 depend from claim 14, and thus also include this limitation.

As Petitioner acknowledges, Nishikawa does not disclose a TAC comprising a substantially circular section as claimed. Pet. 43, 78. Nevertheless, Petitioner asserts that “it would have been obvious to implement Nishikawa’s TAC 76 as a circular TAC.”⁵ Pet. 78. Petitioner relies on the knowledge of a POSITA (Ground

⁵ For purposes of this Preliminary Response, Patent Owner does not challenge Petitioner’s characterization of Nishikawa’s trench 76 as a TAC. However, Patent Owner reserves the right to raise additional arguments and identify additional evidence should the Board institute review.

1) and a combination with Nishikawa2 (Ground 3). Pet. 43, 78 (Ground 1), 98 (Ground 3). Both grounds fail, legally and factually.

First, with regard to Petitioner's reliance on the knowledge of a POSITA (Ground 1), as discussed above, this is not a case where the missing limitation is "unusually simple" or "the technology particularly straightforward," so the general knowledge of a POSITA cannot supply the missing limitation. *Motorola Mobility*, IPR2024-00688, Paper 7 at 29 (denying institution). The claimed circular TAC absent from Nishikawa involves complex semiconductor processes and multiple etching and filling steps to form. '322 patent, 15:44-17:8, Figs. 4A-4C, 8; Campbell ¶50; *DSS Tech. Mgmt.*, 885 F.3d at 1374 (rejecting Board's reliance on "common knowledge" to "supply a missing claim limitation" because wireless communications is not "particularly straightforward" technology). And 3D NAND technology is plainly not "particularly straightforward." Campbell ¶50. Petitioner's reliance, in Ground 1, on "general knowledge" to supply the missing limitations directed to a TAC having a "substantially circular section" thus is legal error.

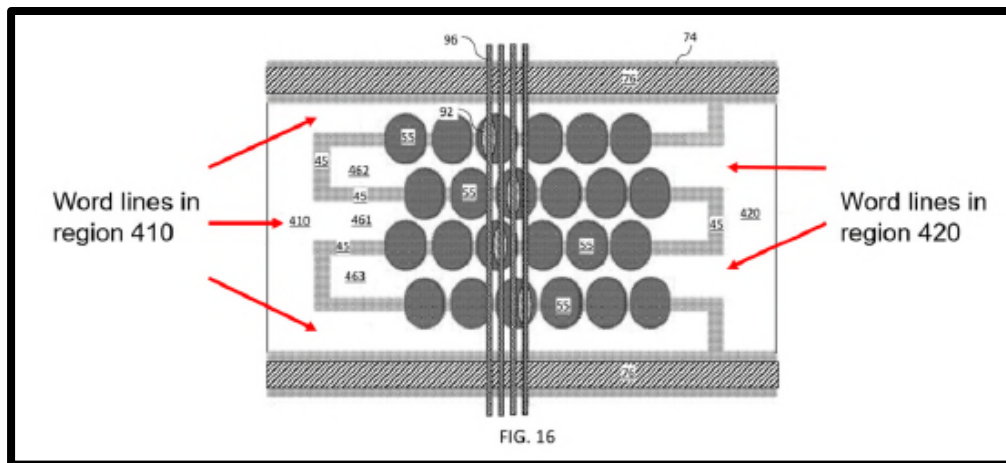
Second, in Ground 3, Petitioner asserts that Nishikawa and Nishikawa2 "present the same memory architecture and key components" and that their provisional applications were "filed only 5 days apart." Pet. 99. But this does not support Petitioner's argument. Indeed, the relative similarity and timing of the

disclosures are evidence that a POSITA would *not* have combined them. The named inventor, Masatoshi Nishikawa, had both patent disclosures in mind at the same time, but explicitly omitted the circular TAC from the Nishikawa patent that Petitioner relies on. In other words, by omitting such a structure from its disclosure, the Nishikawa inventors showed that they did not view a circular TAC to apply to the design in the Nishikawa patent. Any attempt to impart such a motivation to a POSITA is based on hindsight.

Third, even if Nishikawa2 discloses a circular TAC, mere knowledge of a feature does not mean a POSITA “would have been motivated to make the combinations or modifications” to Nishikawa to use a TAC having a substantially circular section—especially when the trench of Nishikawa has a specific purpose as discussed below. *See Belden*, 805 F.3d at 1073 (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”); *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) (conclusion that a combination “would have allowed for” a claimed limitation “is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention”) (citations omitted).

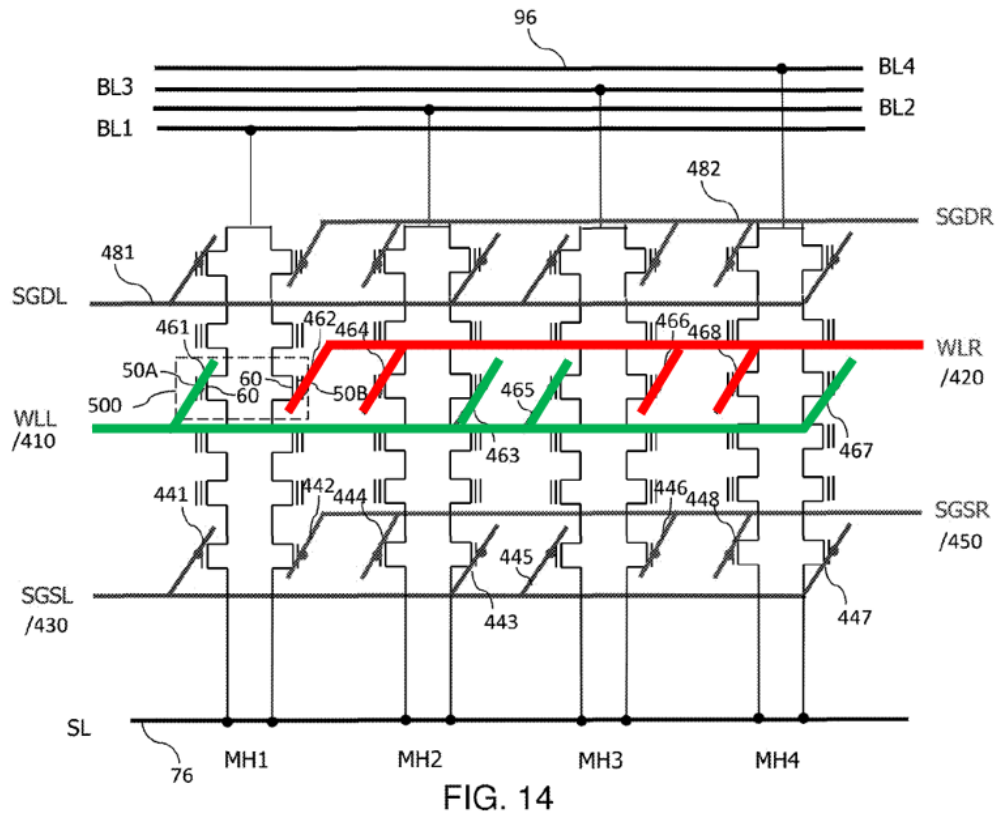
Petitioner's proposed substitution of a TAC having a "substantially circular section" is wrong factually as well, for altering Nishikawa's trench destroys its key function. "[A] proposed modification [is] inappropriate for an obviousness inquiry when the modification render[s] the prior art reference inoperable for its intended purpose." *In re Fritch*, 972 F.2d 1260, 1265 n.12 (Fed. Cir. 1992).

In Nishikawa, each level of control gate electrodes includes a first word line and a second word line that are separated by both the (1) trench structure 76 and (2) the separator dielectric structures 45. Nishikawa 15:31-32, Fig. 16. The first word line includes a comb shaped word line 410 having a plurality of prongs 461, 463, 465, 467 that extend from the stepped contact portion into the "device region." *Id.*, 15:31-37. Similarly, the second word line includes a comb shaped word line 420 having a plurality of prongs that extend into the device region 100. *Id.*, 15:37-42; Campbell ¶52. As shown in Petitioner's annotation of Nishikawa's Figure 16, reproduced below, the trench 76 together with the separator dielectric structures 45 divide the conductor material 46 into these two separate word lines 410 and 420 at every level of the stack. *See* Nishikawa 17:14-23.



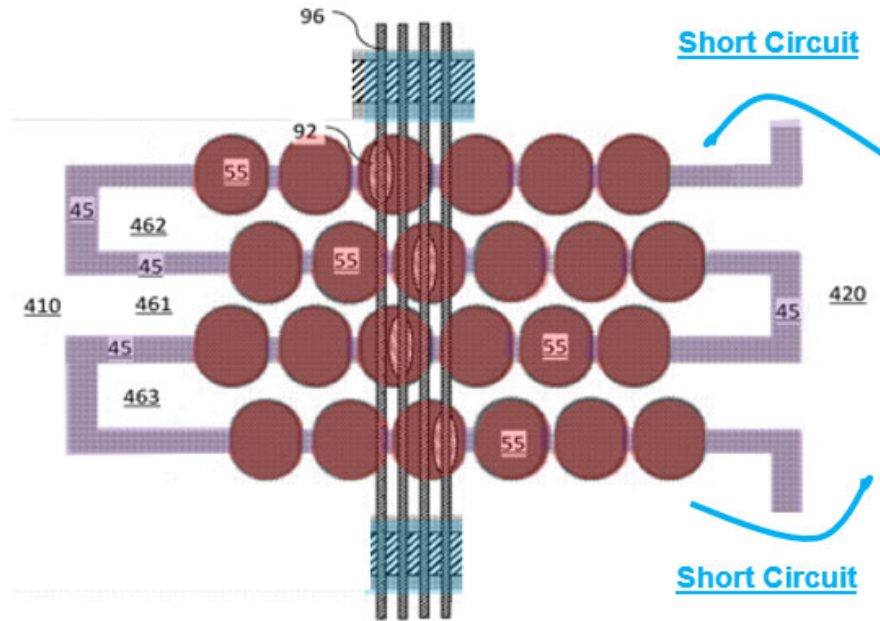
Petition at 57 (annotating Nishikawa, Fig. 16)

This separation provided in part by the trench structure 76 is crucial to the operation of Nishikawa's device. Campbell ¶53. The electrical separation allows for two wordlines at each layer, WLL/410 (green) and WLR/420 (red), as shown in Figure 14, below.



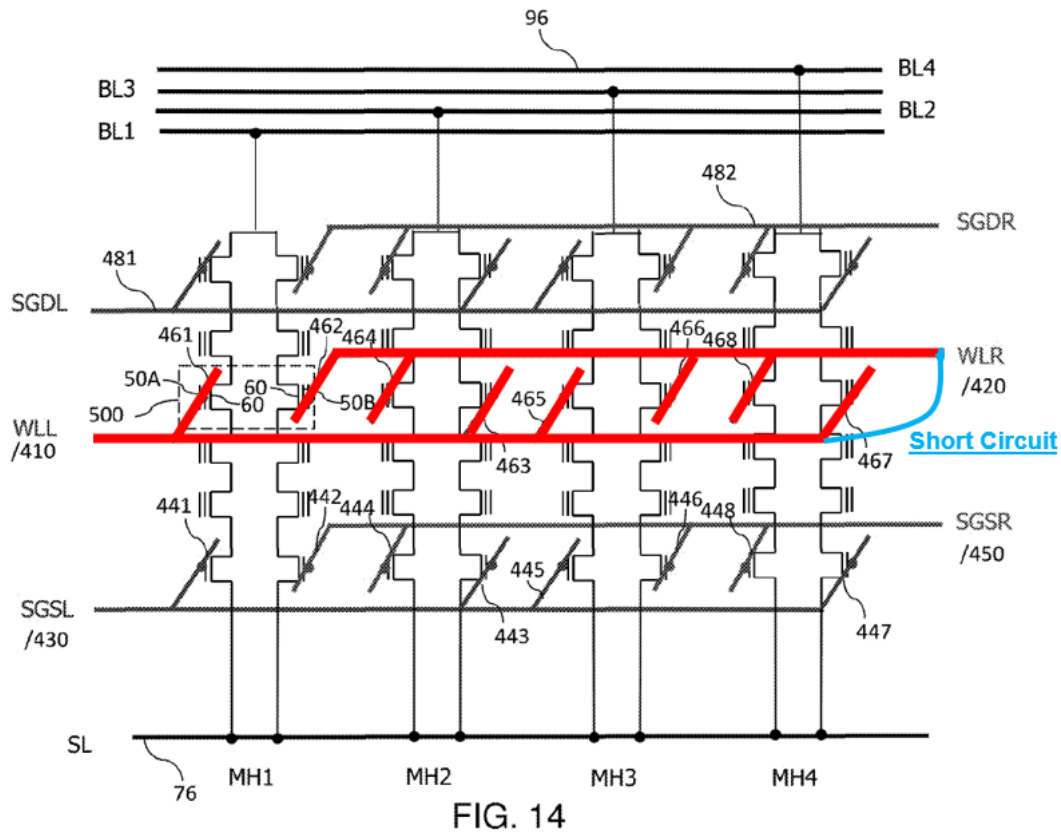
Nishikawa, Fig. 14 (annotated)

Without the trench structure 76 to maintain the separation between the wordlines WLL/410 and WLR/420, the memory would be inoperable because of a short circuit between the wordlines at every level. Campbell ¶54. For example, with a non-trench contact via 76, the two wordlines at each level would be connected at the top and bottom of Figure 16, as shown in a modified version below.



Campbell ¶55 (modifying Nishikawa Fig. 16)

As shown in Dr. Campbell's annotation of Figure 14 below, the NAND circuit structure could not perform as designed because the WLR/420 word line would be connected to the WLL/410 word line. Campbell ¶54. This short circuit would result in incorrect reads and writes from every memory cell in the circuit.



Campbell ¶54 (annotating Nishikawa, Fig. 14)

In proposing to dispense with Nishikawa's trenches, Petitioner does not address this issue at all. Pet. 43, 78. Nor does Nishikawa2's teaching that "openings 79 can have any *suitable* shape, such as circular, rectangular or elongated trench shape" (Nishikawa2 22:38-41, emphasis added) rectify this short-circuit problem of Petitioner's proposed modification. Campbell ¶56. In Nishikawa, a circular shape is *not suitable* for these reasons, and Petitioner makes *no attempt* to provide any evidence that it would have been suitable. See Pet. 43. Instead, Petitioner compares embodiments of Nishikawa and Nishikawa2 that explicitly show *trench* structures 76. Pet. 44 (comparing Nishikawa, Fig. 16 and

Nishikawa2, Fig. 17). But Nishikawa2's embodiments having a *trench* structure do not motivate changing Nishikawa's trench structure to a circular TAC.

Campbell ¶56. To the contrary, Nishikawa2's Figure 17 confirms to a POSITA that, to keep separation of the two wordlines at each level in that structure, the device requires a trench structure 76. *Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1358-60 (Fed. Cir. 2020) (affirming PTAB's finding of non-obviousness where IPR petitioner "failed to reconcile" "fundamental differences" where the proposed combination "would 'require the alteration of the principles of operation of [the primary reference] or would render [the primary reference] inoperable for its intended purpose").

For these reasons, Petitioner failed to show that a POSTIA would have modified Nishikawa to disclose a TAC with "a substantially circular section" as recited in claims 8, 14, and 19.

C. Nishikawa in View of a POSITA's Knowledge Does Not Render Obvious Claims 9-10, 13, 15-16, and 20

Because dependent claims 9-10, 13, 15-16, and 20 depend from a non-obvious claim (8, 14, or 19), claims 9-10, 13, 15-16, and 20 are non-obvious and the Board should deny the Petition for the dependent claims. *See In re Fine*, 837 F.2d 1071, 1076 (Fed. Cir. 1988) ("Dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious.");

IV. Grounds 2 and 4: Nishikawa, alone or with Nishikawa2, in View of Lu Does Not Render Obvious Claims 11-12 and 17-18.

Petitioner's challenge of dependent claims 11-12 and 17-18 in Grounds 2 and 4 relies on the failed Grounds 1 and 3 arguments for claims 8 and 14, respectively. Pet. 96-98, 100. Petitioner does not rely on Lu to teach any claim limitation in claims 8 and 14. Pet. 84-98, 100. Accordingly, Micron has not shown a reasonable likelihood that it would prevail in its challenge of claims 11-12, and 17-18 in Grounds 2 and 4 for the same reasons as discussed above for Grounds 1 and 3.

V. Conclusion

For the reasons set forth above, the Board should deny institution of Inter Partes Review.

Respectfully submitted,

Dated: April 30, 2025

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Preliminary Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(1) because the Patent Owner's Preliminary Response contains 4,937 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Preliminary Response exempted by 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 30th day of April, 2025, a true and correct copy of the foregoing **Patent Owner's Preliminary Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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