

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00191
Patent 11,581,322

**DECLARATION OF STEVE CAMPBELL
IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE**

Table of Contents

I.	Introduction and Qualifications	2
II.	Summary Of Materials Reviewed And Considered	4
III.	Understanding of Legal Standards.....	5
	A. Claim construction.....	6
	B. Obviousness.....	7
IV.	Level of Ordinary Skill in the Art.....	11
V.	Overview of the '322 patent.....	11
VI.	A POSITA would not have found claims 3, 6, 8-10, 13-16, 19-20 obvious in view of Nishikawa (Ground 1) or the combination of Nishikawa and Nishikawa2 (Ground 3).....	15
	A. Claims 3, 6, and 14 (“dummy channel structure... extending vertically through the conductor/dielectric layer pairs in the memory stack”).....	16
	B. Claims 8, 14, 19 (“a through array contact (TAC)” with “a substantially circular section”)	27
VII.	CONCLUSION	35

I. Introduction and Qualifications

1. I have been retained by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Petitioner”) to provide my opinion concerning the validity of U.S. Patent No. 11,581,322 (Ex. 1001).

2. I received my Bachelor’s degree in Physics from the University of St. Thomas (St. Paul, Minnesota) in 1975, and my M.S. and Ph.D. in Physics from Northwestern University (Evanston, Illinois) in 1978 and 1981, respectively. I then joined Sperry, now called Unisys, in 1981 as a CMOS process development engineer. In 1982, I was assigned the lead engineer for the 1.2 μm technology process development effort. In 1984 I was promoted to head of silicon research for the company. This involved a wide variety of process technologies for submicron CMOS.

3. In 1986, I joined the University of Minnesota as an Assistant Professor in the Electrical Engineering Department. My research at the University involved semiconductor processing, materials, and device structures. I raised more than \$100M in various grants and successful submissions to companies and industry consortiums such as the Semiconductor Research Association, as well as State and US government agencies including DARPA and the National Science Foundation. The first ten years of my career at the University concentrated on the development of rapid thermal annealing for 200

mm wafers, particle control in CVD systems, and the development of high uniformity rapid wafer annealing systems. The next ten years were dedicated to the invention and development of high permittivity (aka high-k) films for use as gate insulators. This is necessary to allow the development of deeply scaled CMOS devices. This technology has been widely adopted for nanoscale CMOS devices. In the last fifteen years at the University, my work involved the development of low-cost tandem photovoltaics and micro electromechanical systems (MEMS). The latter included a chronic deep brain sense/stimulation system and very high-speed mechanical switches. Finally, I developed processes for the fabrication of novel 2D materials such as black arsenic, and fabricated transistors using these materials. I retired from the University in 2021.

4. A brief summary of my work at the University would include:

- Approximately 200 publications
- The leading textbook on semiconductor technology. Currently in its fourth edition, *Fabrication Engineering at the Micro and Nanoscale* (Oxford 1996, 2000, 2008, 2013) is the dominant text on the topic.
- Honors from outside the University such as being named a Presidential Young Investigator by the National Science

Foundation and a Life Fellow by the Institute of Electrical and Electronic Engineers (IEEE).

- Honors within the University including outstanding service and outstanding teaching.
- As the Director of the University's Nanofabrication Center, I increased lab usage from 30 to more than 300 users, enabling millions of dollars research awards annually by Minnesota faculty, and leading to the construction of a new \$80M building with an expansive cleanroom facility.

5. Since retiring from the University, I have consulted with semiconductor companies including patent litigation.

6. Additional information regarding my education, technical experience and publications, including a list of the U.S. patents of which I am an inventor/coinventor, is included in my *Curriculum Vitae*, which I understand is attached as Exhibit 2008.

II. Summary Of Materials Reviewed And Considered

7. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor fabrication, I reviewed the following documents:

Ex.	Description
1001	United States Patent No. 11,581,322 (“the ’322 patent”)
1002	File History for the ’322 patent (“’322 FH”)
1003	Declaration of Jack C. Lee
1004	Curriculum Vitae of Jack C. Lee
1005	U.S. Patent 9,837,431 to Nishikawa et al. (“Nishikawa”)
1012	U.S. Patent 10,354,980 to Mushiga et al. (“Mushiga”)
1014	U.S. Patent No. 10,679,721 to Kim et al. (“Kim 721”)
1020	U.S. Patent No. 10,115,632 to Masamori et al. (“Masamori”)
1023	U.S. Patent No. 10,559,583 to Park et al. (“Park 583”)
1027	U.S. Patent 10,290,643 to Kai et al. (“Kai”)
1028	U.S. Patent 9,859,297 to Park et al. (“Park”)
1029	U.S. Patent Appl. Publ. 2018/0308559 to Kim et al. (“Kim”)
1046	U.S. Patent No. 9,935,123 to Nishikawa et al. (“Nishikawa2”)
2020	U.S. Patent Appl. Publ. 2017/0358593 to Yu et al. (“Yu”)

8. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the ’322 patent at the time of the invention, which I have been asked to assume is August 21, 2018.

III. Understanding of Legal Standards

9. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about

certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

10. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

A. Claim construction

11. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary.

12. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the

written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office ("USPTO"). I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Obviousness

13. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

14. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

15. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

16. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by

the invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

17. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated to make a combination includes whether he/she would select particular references in order to combine their elements.

18. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since

uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

19. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

20. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness.

IV. Level of Ordinary Skill in the Art

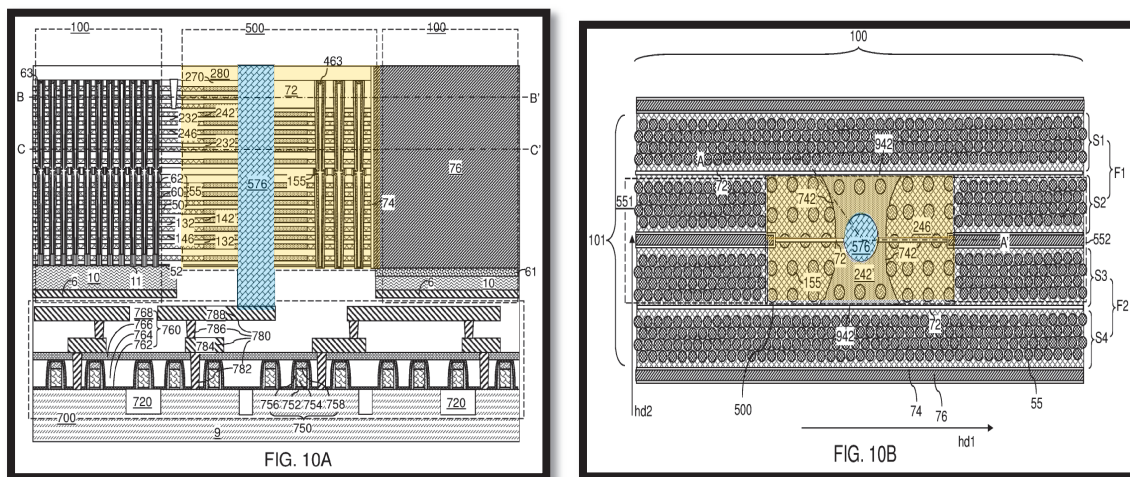
21. Dr. Lee defines a person of ordinary skill in the art (“POSITA”) as a person having “a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Ex. 1003 ¶ 36.

22. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art. In view of my educational background and work experience, I surpass Dr. Lee’s definition of a POSITA, and did so before August 21, 2018. Regardless of the precise definition of a POSITA, Grounds 1-4 of the Petition do not show the challenged claims obvious. I reserve the right to opine as to an alternative level of a POSITA in other proceedings or if the Board institutes review in this proceeding.

V. Overview of the ’322 patent

23. The ’322 patent recognized that 3D memory devices require contacts that go vertically through the memory stack called “through array contacts” or “TACs” for “providing vertical interconnects between the stacked memory array device and peripheral device (e.g., for power bus and metal routing).” ’322 patent, 4:58-62. In the past, these TACs were formed within a “barrier structure”

preserving a “dielectric stack region within a memory stack.” *Id.*, 4:62-65. The drawback of such a “barrier structure” is that “the regions enclosed by the barrier structures take up large area in the core array region where memory strings can be formed.” *Id.* at 4:62-5:1. An example TAC (blue) formed within a barrier structure (gold) is shown below in Figures 10A and 10B (annotated) from U.S. Patent Application Publication 2017/0358593 (Ex.(2020), “Yu”). Here, the TAC and barrier structure are formed in a region 500 “in which through-memory-level via structures that extend vertically through a memory-level assembly are subsequently formed.” Yu [0051].



TACs within a barrier structure “also have a negative impact on the resistance of word lines.” ’322 patent 4:62:5-1. “Moreover, the existing fabrication processes for forming the barrier structures become more challenging for the next generation 3D memory devices” which “have less process margin.” *Id.*, 5:2-5.

24. The '322 patent discloses a novel “3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures.” *Id.*, 5:6-9. The '322 patent explains that “by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost.” *Id.*, 5:9-12. In addition, “[m]ore process margin”—i.e., room for error—“may be obtained due to the elimination of etching and alignment steps for making the barrier structures.” *Id.*, 5:13-18. To “further simplify the fabrication flow and reduce process cost,” the '322 patent teaches that the non-barrier structure TACs can be “formed in the same fabrication process(es) for making other structures” such as “peripheral contacts” outside of the memory stack. *Id.*, 5:17-23. As a result, the non-barrier structure TACs 416 can have a same shape as the peripheral contact 420, including a “substantially circular shape in the plan view,” as shown in Figure 4C below where the circular cross section of the TAC (green box) matches the circular cross section of the peripheral contact (blue box). *Id.* 8:56-57.

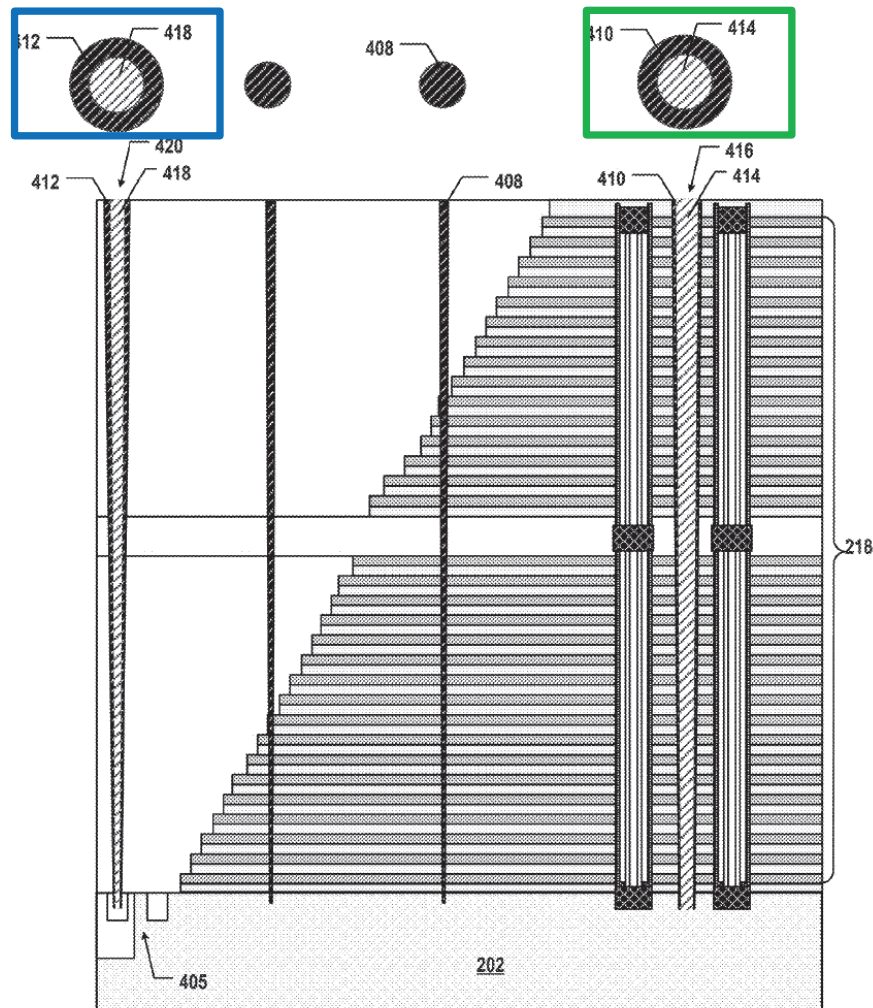
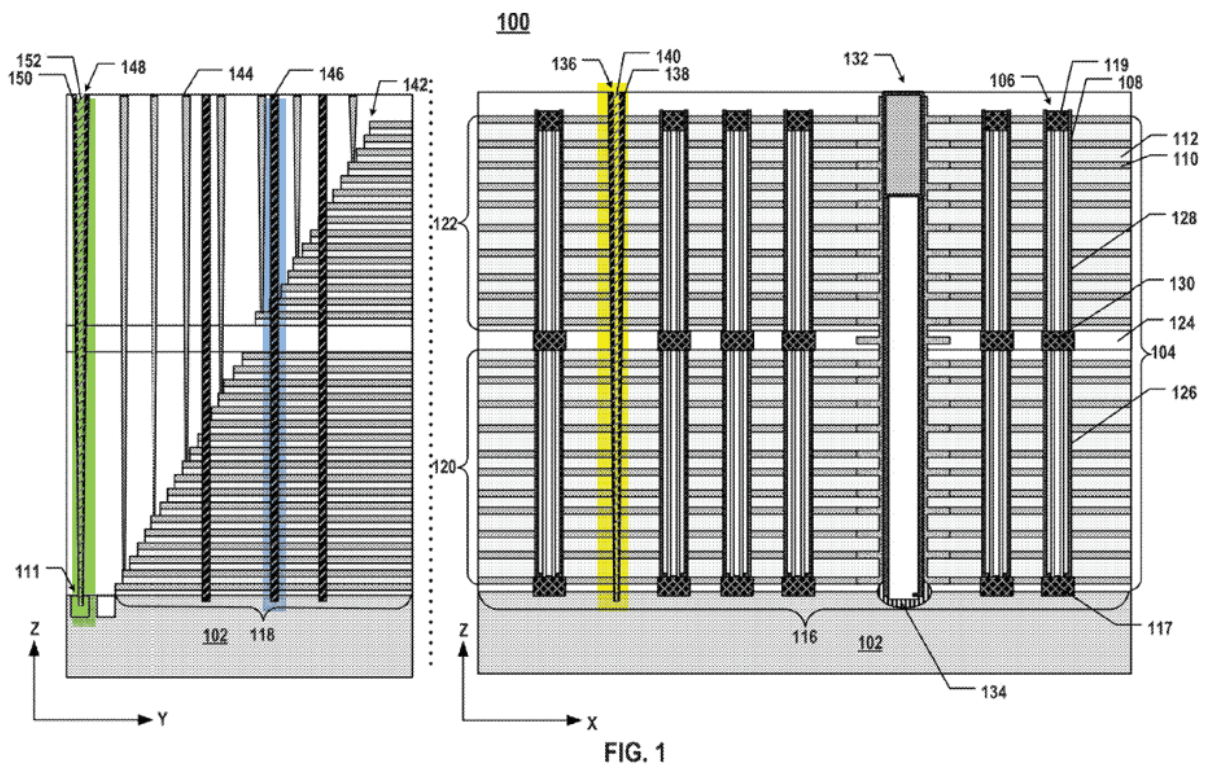


FIG. 4C

'322 patent, Figure 4C

25. Figure 1, reproduced below, illustrates a cross-section of an embodiment of a “memory stack 104” and a “staircase structure” 142. *Id.*, 8:63-65. As shown below, the memory device 100 includes a TAC 136 (yellow) that extends vertically through the stack to carry electrical signals to/from the memory device 100. *Id.*, 8:30-41. Unlike the prior art, TAC 136 is not “enclosed

by barrier structures.” *Id.*, 5:6-22. This allows the TACs to be “formed in the same fabrication process(es) for making other structures,” including those *outside* the memory array such as “peripheral contact 148” (green). *Id.*, 5:6-22; 12:28-49. In addition, “dummy channel structures 146” (blue) are “disposed in the outer region 118 of memory stack 104 as shown in Fig. 1” to “provide mechanical support to the memory array structures, e.g., memory stack 104.” *Id.*, 9:41-51.



VI. A POSITA would not have found claims 3, 6, 8-10, 13-16, 19-20 obvious in view of Nishikawa (Ground 1) or the combination of Nishikawa and Nishikawa2 (Ground 3).

26. As a general matter, Dr. Lee relies on the knowledge of a POSITA to supply at least two features missing from Nishikawa in relation to the challenged claims. In doing so, he relies on several patent documents from

around the same time as the '322 patent. As I discuss further below, I do not agree that these documents supply the missing features, and none of the missing features are simple. In fact, as I discuss more below, the field of 3D NAND memory manufacturing is not simple, as it pushes the limits of semiconductor fabrication in terms of size and complexity, and even seemingly small modifications can result in unforeseen problems.

A. Claims 3, 6, and 14 (“dummy channel structure... extending vertically through the conductor/dielectric layer pairs in the memory stack”)

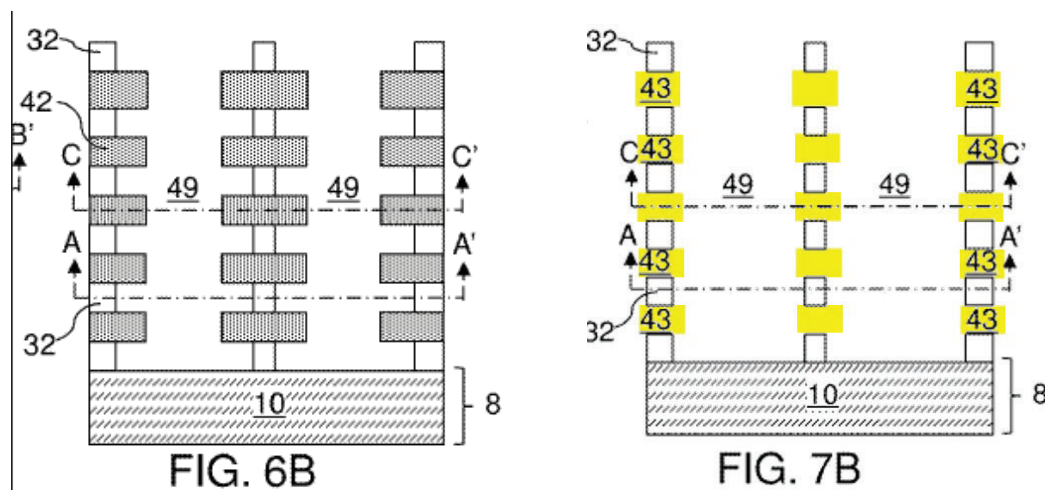
27. Independent claim 14, and dependent claims 3 and 6, recite “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.”

28. Dr. Lee opines that “a POSITA would have been motivated, with a reasonable expectation of success, to include dummy channels... in Nishikawa’s memory stack for several reasons.” Ex. 1003 ¶ 140. As an initial matter, I note that forming a dummy channel structure is not unusually simple, and involves complex semiconductor manufacturing processes, including “wet etching, and/or dry etching, such as DRIE” and “thin film deposition processes, such as ALD, CVD, PVD.” ’322 patent, 12:10-27.

29. I disagree with Dr. Lee. A POSITA would not have had any reason to add dummy channels to Nishikawa.

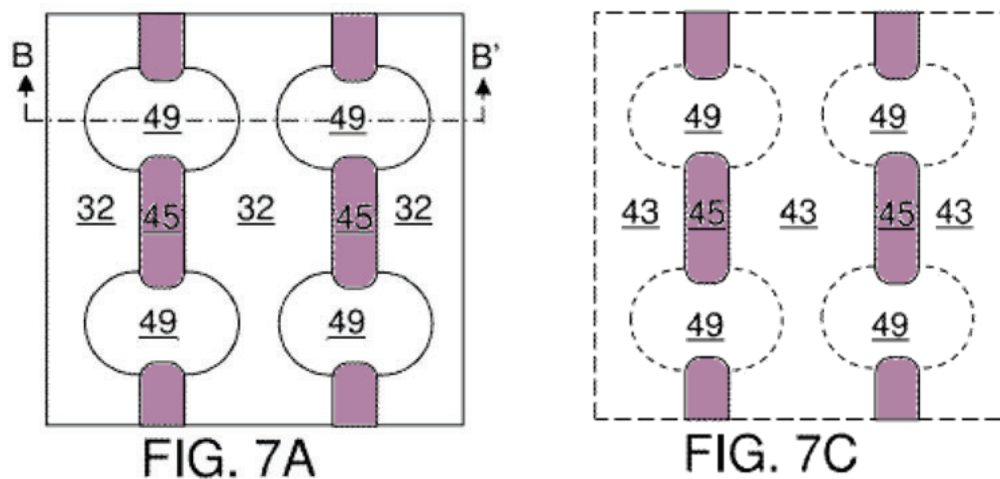
30. Dr. Lee asserts that “[d]ummy channels provide structure support, which is important during the gate line replacement process.” Ex. 1003 ¶ 143. But Dr. Lee omits that Nishikawa explicitly discloses that existing structures (not dummy channels) provide support during its gate replacement process. Specifically, Nishikawa discloses that “separator dielectric structures 45 can provide structural support to the insulating layers 32 after formation of the interlayer cavities 43.” Nishikawa 10:10-12.

31. During the gate replacement process of Nishikawa, shown in Figure 7B as annotated below, sacrificial material layers 42 are removed with an etching process, and “recesses 43” (yellow) are formed in their place (before the metal conductor layers, or gates, are inserted into the recesses). Nishikawa 10:8-10. During this intermediate stage with recesses between the insulating layers, the separator dielectric structures 45, which are not shown in Figure 7B, “provide structural support to the insulating layers 32” to maintain recesses 43 (yellow) in the structure even after removal of the sacrificial material layers 42. Nishikawa 10:10-12.



Nishikawa, Figures 6B, 7B

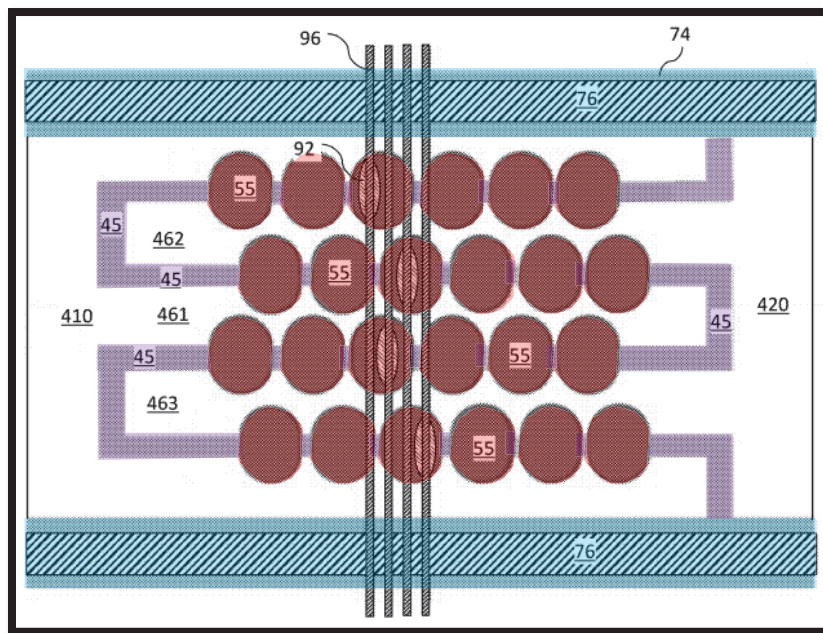
32. Figures 7A and 7C illustrate top views of the device at the elevations shown, respectively, as A-A' and C-C' in Figure 7B. These figures show the separator dielectric structures 45 connecting to the insulating layers 32 (Fig. 7A) to provide structural support and maintain the recesses 43 (Fig. 7C).



Nishikawa, Figures 7A, 7C

If they did not, the insulating layers 32 would collapse into the recesses 43 below and the Figure 7B structure could not exist.

33. As shown in Figure 16, below, the separator dielectric structures 45 (purple) in the final memory device are disposed throughout the device and are therefore able to provide sufficient structural support during the gate replacement process. *See Nishikawa 17:14-18* (“The separator dielectric structures 45 extend through the stack, contact portions of outer sidewalls of the memory stack structures 55, and laterally separate the control gate electrodes 46 of the plurality of charge storage elements.”).



Nishikawa, Figure 16

34. Dr. Lee does not assert any need for additional support during gate replacement, and does not assert that the separator dielectric structures are unable to provide sufficient support (which would be contrary to Nishikawa’s explicit

disclosure). Thus, there is no need for dummy channels, as they would serve no purpose.

35. Dr. Lee asserts that “one normally employs dummy channel structures at the edge of the array.” Ex. 1003 ¶ 141. But Dr. Lee does not motivate actual dummy channels at the edge of the array in Nishikawa, however, which does not disclose dummy channels and has no need for them. Dr. Lee makes no attempt to account for the fact that the stack is already occupied by structures. He does not assert, for example, that these functional structures would be modified to become dummy structures. This is important because accommodating dummy channels through the stack would require either (1) increasing the size of the stack to create space for the dummy structures while maintaining the existing structures, or (2) decreasing the memory’s storage capacity by replacing functional structures (i.e., “memory stack structures 55,” which serve as channels for the memory cells, Nishikawa 4:28-32, Fig. 1, or “contact via structures 66,” which provide external access to the word lines, *id.* 6:41-49, Fig. 1) with **non**-functional dummy channels. For example, replacing channels with dummy structures will significantly decrease the memory’s storage capacity because channels are a part of every memory cell. Either approach gives undesirable results, and especially so when no benefit is provided by the dummy structures because the device already has sufficient structural support.

36. And adding dummy channels to Nishikawa would require additional processing steps because these new structures would be formed with different structure than others. Although Dr. Lee cites to Exhibit 1027 (Kai) for the notion that “dummy channels can be made by the same process and at the same time as the active channels” (Ex. 1003 ¶ 147), Dr. Lee does not make any attempt to show that a POSITA would understand the cited portion of Kai to relate to Nishikawa’s design. In other words, even if Kai discloses dummy channels made by the same process and at the same time as active channels, Dr. Lee provides no reason that a POSITA would have formed such dummy channels in Nishikawa. It is my opinion that a POSITA would not have done so. And Dr. Lee does not propose to combine Kai with Nishikawa.

37. Instead of combining Nishikawa with any other reference, the Petition cites to five references—Nishikawa2, Masamori, Kai, Kim, and Park—that purportedly confirm “the knowledge of a POSITA.” Petition at 60-62. None of these references motivate adding dummy channels to Nishikawa, where existing structures provide adequate structural support. Instead, all three references disclose designs that, unlike Nishikawa, accommodate specific regions for what Dr. Lee describes as “dummy channels.” Ex. 1003 ¶ 144.

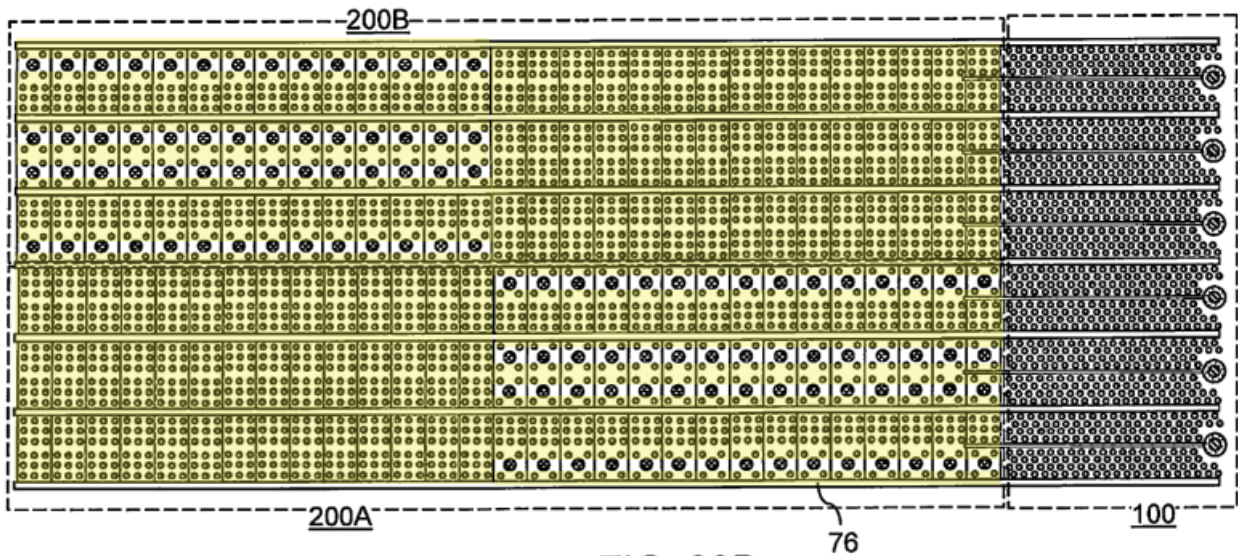
38. For example, Dr. Lee quotes Nishikawa2 as “recogniz[ing] th[e] known need” for support pillars during the gate replacement process. Ex. 1003

¶ 143 (citing Nishikawa2, 9:63-67 (“At least one dielectric pillar structure (not shown) can be formed through the entire set of the spacer material layers 42 and the insulating layers 32....”)). But the cited passage merely describes the formation of a “not shown” dielectric pillar structure and says nothing about a “need” for support structures, let alone describe any motivation to add support structures to Nishikawa’s device that already has them. Dr. Lee does not even assert that Nishikawa2 discloses dummy channels, but only asserts that a POSITA “would recognize” that dummy channels are “consistent with Nishikawa2’s ‘dielectric pillar structure’ statement.” Ex. 1003 ¶ 143.

Nevertheless, to the extent Dr. Lee intends to rely on Nishikawa2’s dielectric pillar structure, it contradicts any implication that such dummy channels are made with the same process as active channels (e.g., Ex. 1003 ¶ 147) because active channels are not simply dielectric pillars.

39. Dr. Lee also cites to Masamori, which discloses “conductive support structures.” Masamori (Ex. 1020), Cover (Title); *see* Ex. 1003 ¶ 146. Unlike Nishikawa, Masamori’s design does not include separator dielectric structures that provide structural support during the gate replacement process. And Figure 20B, annotated below, shows the huge costs of Masamori’s support structures. Specifically, Masamori devotes an enormous area (yellow) (most of contact regions 200A, 200B) to these support structures. But again, Dr. Lee does not

propose to combine Masamori with Nishikawa or motivate applying these teachings to Nishikawa. And in fact, a POSITA would not have applied Masamori's extremely different design to Nishikawa's design, which already included separator dielectric structures 45 that provide the structural support Dr. Lee asserts is needed for gate replacement.



Masamori Figure 20B

40. For further example, the Kai reference (Exhibit 1027) discloses “support pillars 20” (blue) taking up significant space in a “contact region 300” (yellow) in a device that (unlike Nishikawa) (1) includes no separator dielectric structures providing support during the gate replacement process, and (2) has a very different layout than Nishikawa. Kai, 6:2-5, Fig. 6A; *see also* Fig. 15A (below) (showing “support pillars 20” only in the contact region).

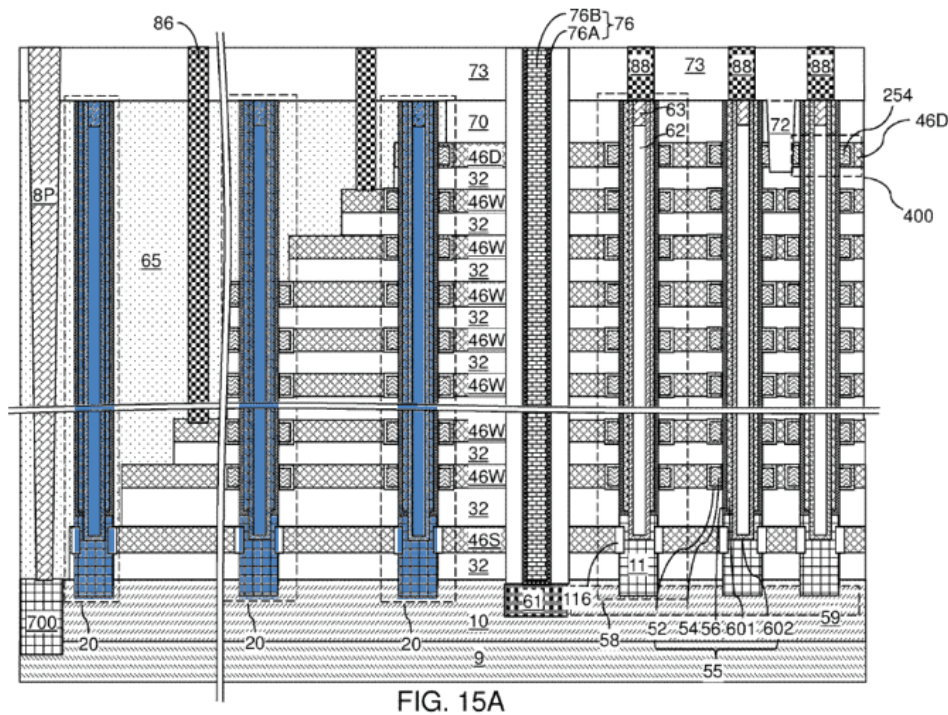
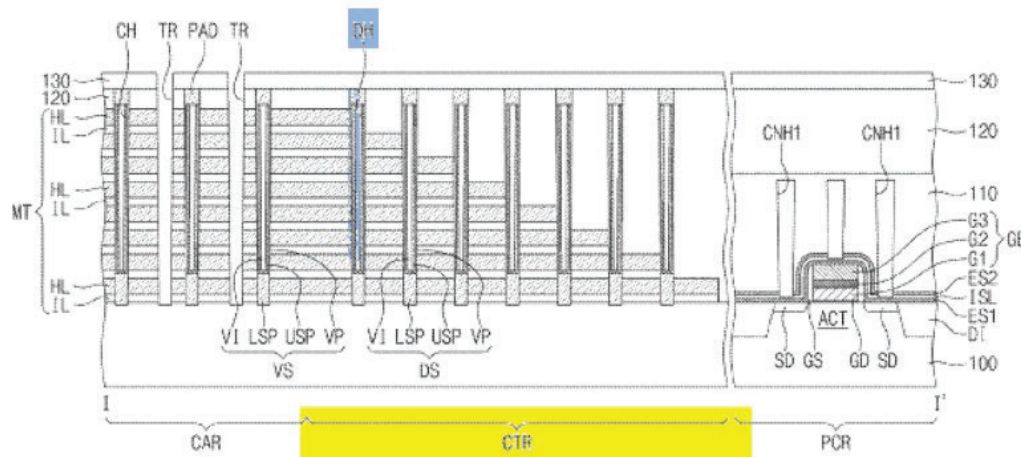


FIG. 15A

Kai Fig. 15A

41. Similarly, the Kim reference (Exhibit 1029) discloses “dummy holes DH” (blue) in a “connection region CTR” (yellow). Kim, Figure 13 (below), [0047]; *see* Petition at 44 (citing Kim [0047]) (“The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region STR”); *see also* Kim [0070] (“On the connection region CTR, a plurality of dummy holes DH may be formed.”).

FIG. 13



42. For its part, Park (Exhibit 1028), discloses separate “cell and dummy regions.” Park, Abstract. Park discloses “second channel structure 120b” that are “disposed on the wiring region” and “may not be provided as the portion of the memory cell.” *Id.*, 7:38-44.

43. To summarize, Nishikawa2, Masamori, Kai, Kim, and Park, teach structures in circuits that (1) have regions designed to accommodate them, such as huge portions of a “word line contact via region 200” (Masamori), “contact region” (Kai), “connector region CTR” (Kim), or “dummy region” (Park); and/or (2) lack a separator dielectric structure as existing support during the gate replacement process. The Petition does not explain how, where, or why a POSITA would have formed such regions in Nishikawa, which does not include any such region designed to accommodate dummy channels. None of

Nishikawa2, Masamori, Kai, Kim, or Park would have motivated a POSITA to add dummy channels to Nishikawa, which already has structures that provide the structural support that the Petition asserts would be provided by the dummy structures, and modifying structures within the memory cell array would require (1) additional processes to form the different pillar structure (e.g., Nishikawa2's "dielectric pillar structure") and (2) either removing functional pillars from the device or increasing the size of the device to accommodate additional structures.

44. The Petition asserts other supposed benefits to forming dummy channels in Nishikawa. For example, the Petition states that dummy channels are suitable to use as support structures because they "can be made by the same process and at the same time as the active channels," they "do not require connections to upper-level devices," and they provide "additional structural support." Pet. 60-63. But these supposed benefits all pre-suppose that there is a need for additional support structures in Nishikawa. For example, the fact that dummy structures do not require connections to upper-level devices means they are not functional within the device, and take up extra space where a functional pillar would be placed.

45. The Petition also asserts that dummy channels improve "uniform[ity]" and "reduce the likelihood of defective bits on the edge of the memory cell region, because the additional rows of dummy channel structures

extend the memory cell pattern to include the dummy region on the edges.” Pet.

59. It is not clear what the Petition means by “additional rows” in this sentence.

Further, Nishikawa does not include a dummy region. Nevertheless, this does not motivate adding dummy structures to Nishikawa, for similar reasons that Kai, Kim, and Park don’t motivate such a modification.

46. And again the supposed “uniformity” only seems to be provided pre-assuming a need for dummy structures in the first place, and specifically on when they are evenly spaced throughout the device, resulting in potentially enormous spatial expansion of Nishikawa’s device. I disagree that these supposed benefits would have motivated a POSITA to make the proposed modification to Nishikawa, which has no need for additional structural support.

B. Claims 8, 14, 19 (“a through array contact (TAC)” with “a substantially circular section”)

47. Independent claims 8 and 14, and dependent claim 19, recite a TAC comprising “a substantially circular section.” Claims 9-13 depend from claim 8, claims 15-18 and 20 depend from claim 14.

48. Nishikawa does not disclose a TAC comprising a substantially circular section as required in claims 8, 14, and 19.

49. Dr. Lee asserts that “it would have been obvious to implement Nishikawa’s TAC 76 as a circular TAC.” Ex. 1003 ¶ 180. In Ground 1, Dr. Lee does not combine Nishikawa with any other reference, but just relies on the

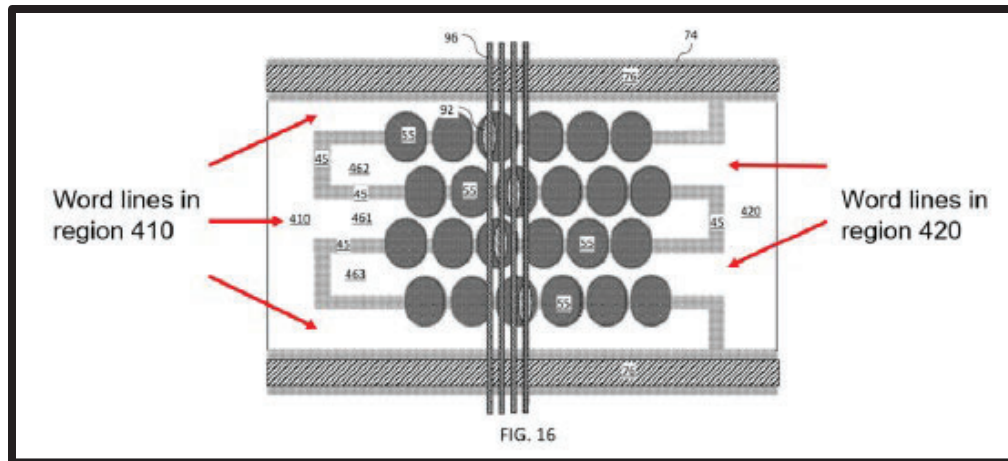
knowledge of a POSITA. Ex. 1003 ¶¶ 180, 193, 201. In Ground 3, Dr. Lee proposes to combine Nishikawa with Nishikawa2 to render this limitation obvious. Ex. 1003 ¶ 238. I disagree that either ground renders this limitation obvious.

50. As I discussed above, I note that forming a through array contact having a “substantially circular section” in a 3D NAND device is not unusually simple, and involves complex semiconductor manufacturing processes and multiple etching and filling steps. '322 patent, 15:44-17:8, Figures 4A-4C, Figure 8.

51. Additionally, a POSITA would not have been motivated to modify Nishikawa in the proposed manner—i.e., to substitute Nishikawa's trench structure 76 in favor of a circular pillar.¹ Specifically, altering Nishikawa's trench destroys its key function.

¹ For the purpose of this declaration, I have accepted for the sake of argument that Nishikawa's trench (as disclosed, or as modified into a circular pillar) would constitute a TAC because the proposed modification fails to render the claims obvious even accepting this premise. I reserve the ability to provide opinions on whether these structures are the claimed TACs issues in future testimony.

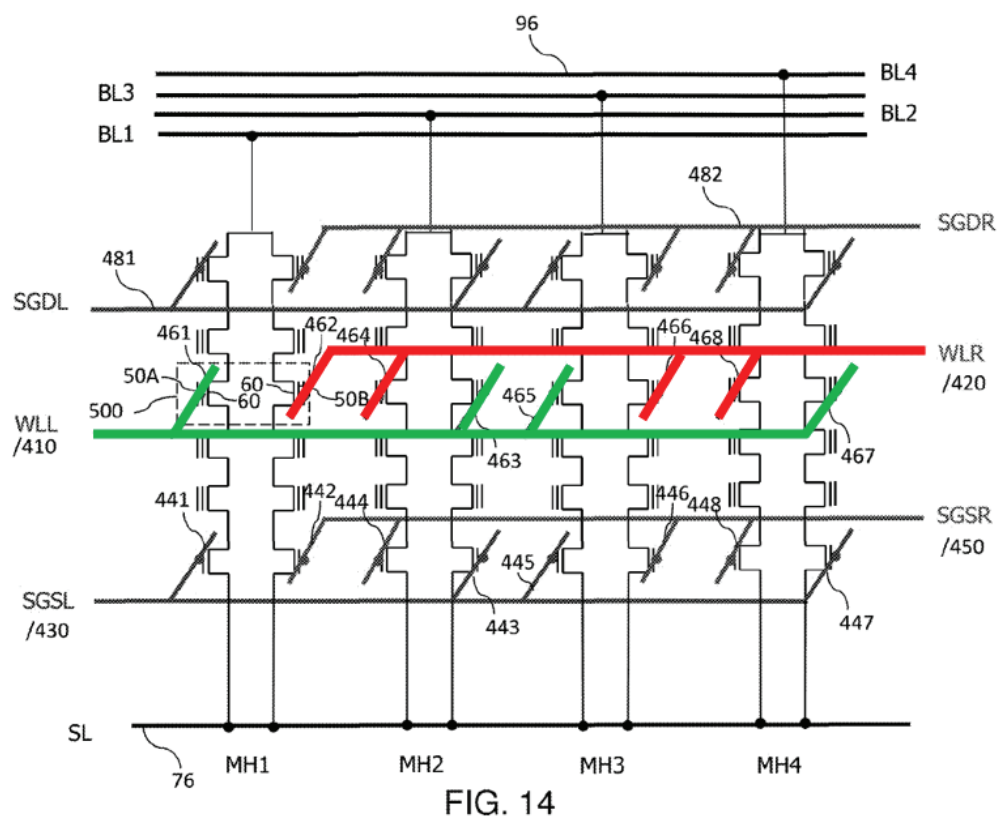
52. In Nishikawa, each level of control gate electrodes includes a first word line and a second word line that are separated by both the (1) trench structure 76 and (2) the separator dielectric structures 45. Nishikawa 15:31-32, Fig. 16. The first word line includes a comb shaped word line 410 having a plurality of prongs 461, 463, 465, 467 that extend from the stepped contact portion into the “device region.” *Id.* 15:31-37. Similarly, the second word line includes a comb shaped word line 420 having a plurality of prongs that extend into the device region 100. *Id.* 15:37-42. Dr. Lee annotates Figure 16, reproduced below, as including “word lines in region 410” and “word lines in region 420.” Ex. 1003 ¶ 136. Although his annotation is not correct, as 410 and 420 *are* word lines (not regions that contain multiple word lines) (Nishikawa 15:31-42), my focus for now is on the separation of these word lines (or regions as Dr. Lee calls them). Specifically, the trench 76 together with the separator dielectric structures 45 divide the conductor material 46 into these two separate word lines 410 and 420 at every level of the stack. *See* Nishikawa 17:14-23.



Ex. 1003 ¶ 136 (annotating Nishikawa, Fig. 16)

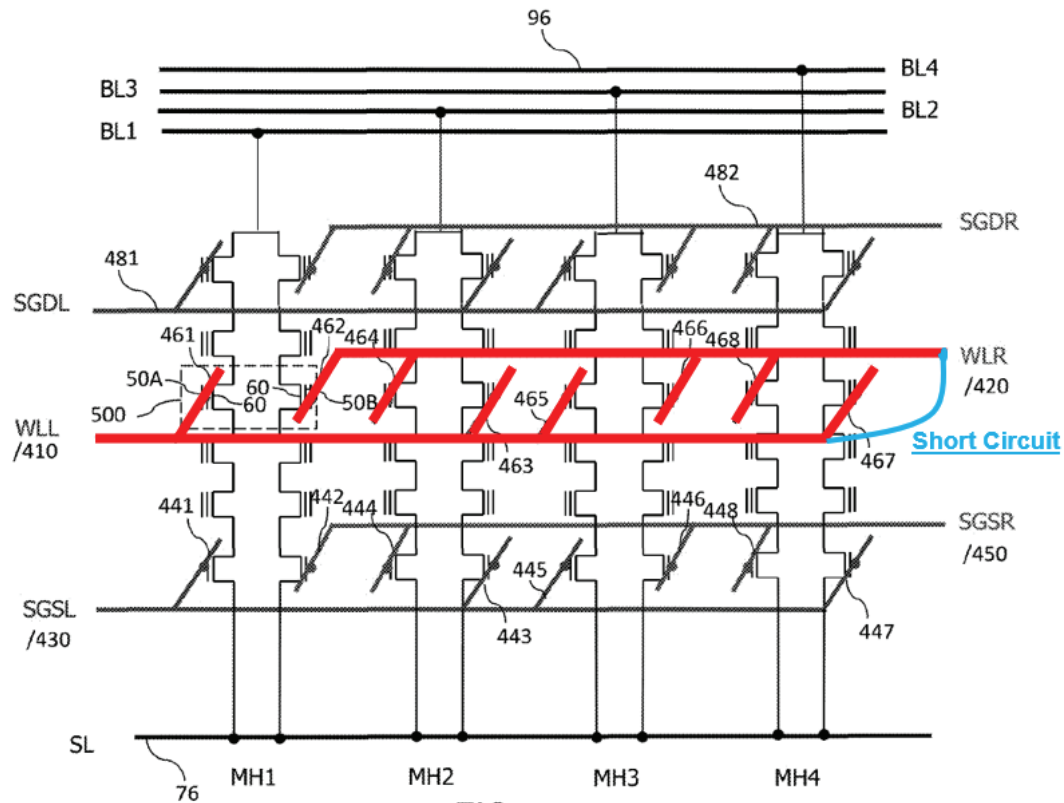
53. This separation is crucial to the operation of Nishikawa's device.

For example, the electrical separation allows for two wordlines at each layer, WLL/410 (green) and WLR/420 (red), as shown in Figure 14, below.



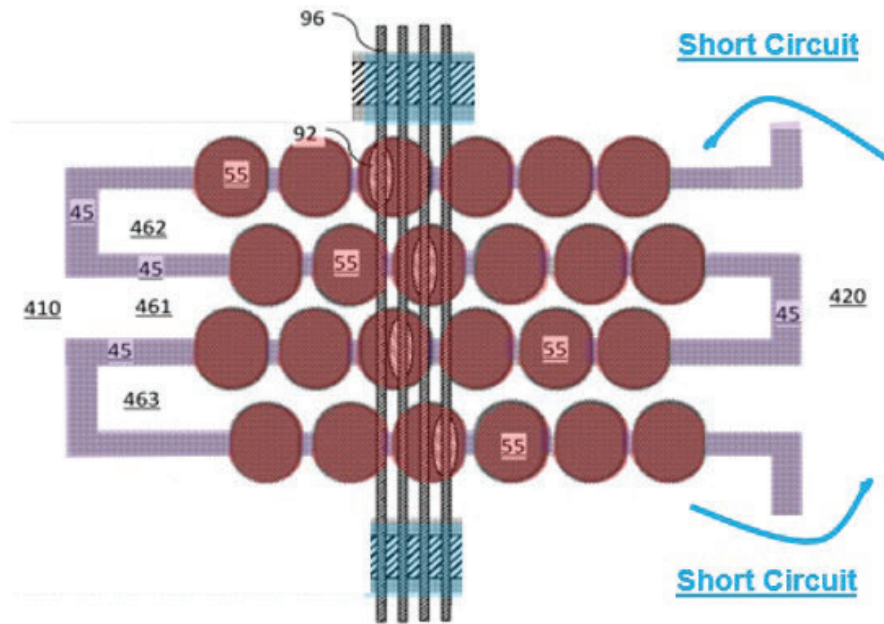
Nishikawa, Fig. 14 (annotated)

54. Specifically, the right word line WLR/420 (red) acts as gates for different memory cells than the left word line WLL/410 (green). If these two word lines are shorted together (as shown in the below annotation of Figure 14 with both word lines in red), then the separate memory cells would be driven by the same gate and would become superfluous and inoperable in the memory device. The NAND circuit structure could not perform as designed because the WLR/420 word line would be connected to the WLL/410 word line. This short circuit would result in incorrect reads and writes from every memory cell in the circuit. For example, an intended write operation using wordline WLL/410 would inadvertently overwrite data in memory cells driven by wordline WLR/420.



Nishikawa, Fig. 14 (modified to connect WLR/420 and WLL/410)

55. The trench structure helps to provide the separation between these word lines. Without the trench structure 76 to maintain the separation between the wordlines WLL/410 and WLR/420, the word lines would not be separated. For example, with a non-trench contact via 76, the two wordlines at each level would be connected at the top and bottom of Figure 16, as shown in a modified version below.



Nishikawa Fig. 16 (modified to change trench to a pillar)

56. Nishikawa2's teaching that "openings 79 can have any *suitable* shape, such as circular, rectangular or elongated trench shape" (Nishikawa2 22:38-41, emphasis added) does not show that a "circular" shape is "suitable" in Nishikawa, especially given the above problems that remain unaddressed in the Petition. To the contrary, a circular shape is *not suitable* for Nishikawa. The Petition compares embodiments of Nishikawa and Nishikawa2 that explicitly show trench structures 76. Pet. 44 (comparing Nishikawa, Fig. 16 and Nishikawa2, Fig. 17). But Nishikawa2's embodiments having a trench structure do not motivate changing Nishikawa's trench structure to a circular TAC. Figure 17 of Nishikawa2 does not motivate modification of Nishikawa to change a

trench structure with a functional purpose to a circular pillar that cannot fulfill that purpose.

VII. CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on April 29, 2025, in Arden Hills, Minnesota.

Stephen Campbell

Stephen A. Campbell