

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,  
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,  
Patent Owner.

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IPR2025-00191  
Patent 11,581,322 B2

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Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and  
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

DECISION  
Granting Institution of *Inter Partes* Review  
35 U.S.C. § 314

## I. INTRODUCTION

### A. *Background and Summary*

Micron Technology, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–20 of U.S. Patent No. 11,581,322 B2 (Ex. 1001, “the ’322 patent”). Paper 1 (“Pet.”). The Petition is supported by a Declaration from Dr. Jack C. Lee. Ex. 1003 (“Lee Declaration”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 10 (“Prelim. Resp.”). The Preliminary Response is supported by a Declaration by Dr. Stephen Campbell. Ex. 2007. On February 21, 2025, Patent Owner filed a Statutory Disclaimer of claims 1, 2, 4, 5, and 7. Ex. 2006. Thus, the non-disclaimed claims that remain challenged by the present Petition are claims 3, 6, and 8–20.

Patent Owner filed a Brief on Discretionary Denial, and Petitioner filed a brief in opposition. Papers 10 and 18. The Director considered the briefing and determined that discretionary denial was not warranted. Paper 21.

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons discussed below, we determine that Petitioner has sufficiently shown a reasonable likelihood that it will prevail as to the unpatentability of claims 8–12 and 19 of the ’322 patent but has not sufficiently shown a reasonable likelihood that it will prevail as to the unpatentability as to claims 3, 6, 13–17, and 20. Because Petitioner has sufficiently shown a reasonable likelihood that at

least one claim is unpatentable, we institute an *inter partes* review of claims 3, 6, and 8–20, which are all of the remaining non-disclaimed claims of the ’322 patent challenged in this proceeding.

*B. Patent Owner’s Disclaimer of Claims 1, 2, 4, 5, and 7*

As indicated above, Patent Owner filed a statutory disclaimer of claims 1, 2, 4, 5, and 7 of the ’322 patent. *See* Ex. 2006. In view of Patent Owner’s statutory disclaimer, we treat claims 1, 2, 4, 5, and 7 as having never been part of the ’322 patent. *See Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1383 (Fed. Cir. 1998) (“This court has interpreted the term ‘considered as part of the original patent’ in [35 U.S.C.] § 253 to mean that the patent is treated as though the disclaimed claims never existed.”). Because *inter partes* review cannot be instituted based on disclaimed claims, claims 1, 2, 4, 5, and 7 are outside the scope of this proceeding. 37 C.F.R. § 42.107(e) (“No *inter partes* review will be instituted based on disclaimed claims.”); *General Elec. Co. v. United Techs. Corp.*, IPR2017-00491, Paper 9 (PTAB July 6, 2017) (precedential) (denying institution in view of a statutory disclaimer of all the challenged claims). Thus, we confine our analysis in this Decision to claims 3, 6, and 8–20, the challenged claims that have not been disclaimed.

*C. Real Parties-in-Interest*

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as real parties-in-interest. Pet. 6. Patent Owner identifies itself as the real party-in-interest. Paper 5, 1.

*D. Related Matters*

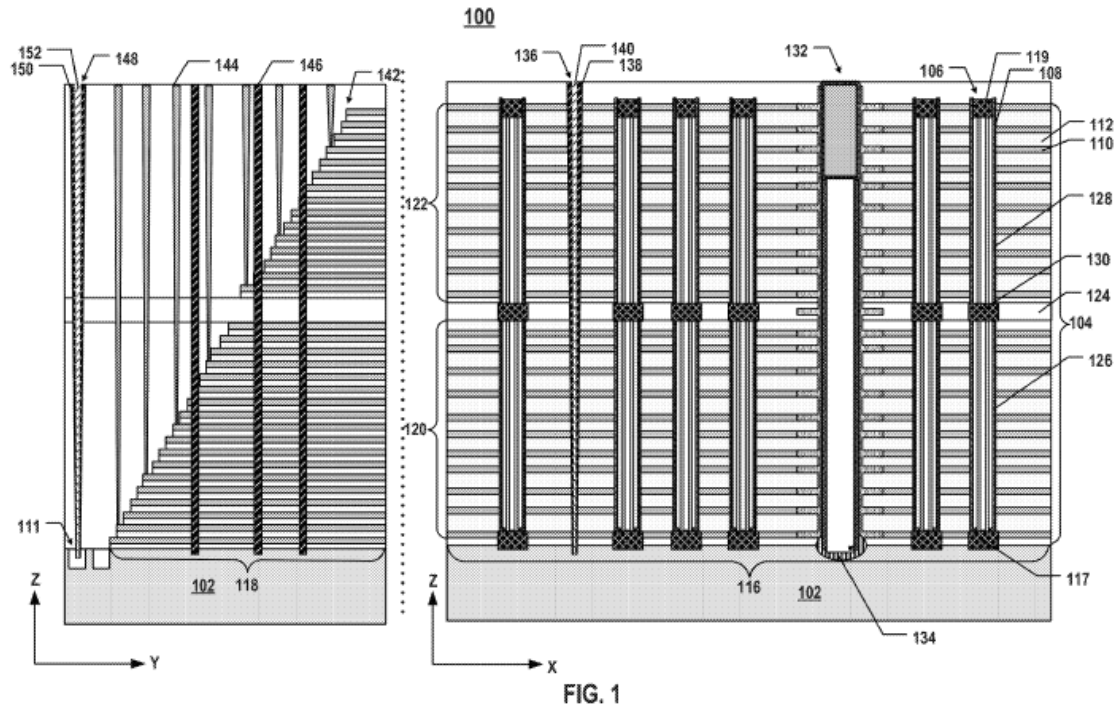
The parties represent that the ’322 patent is involved in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL

(N.D. Cal., filed November 9, 2023). Paper 5, 1; Pet. 6–7. Petitioner also filed twenty three IPRs challenging each patent asserted in the district court case. Pet. 7–8.

*E. The '322 Patent*

The '322 patent is titled “Three-Dimensional Memory Devices Having Through Array Contacts and Methods for Forming the Same.” Ex. 1001, code (54). The '322 patent issued on February 14, 2023, from application No. 17/100,847, filed on November 21, 2020, and is a division of application No. 16/745,342, now U.S. Patent 11,049,866, which is a division of U.S. Application Number 16/149,103, filed on October 1, 2018, which is now U.S. Patent 10,566,336, which in turn is a continuation of Application Number PCT/CN2018/101482, filed on August 21, 2018. *Id.* at codes (21), (22), (63).

The '322 patent relates to a staircase structure for a 3D memory device including a dielectric stack, including a plurality of dielectric/conductor layer pairs, having a channel structure extending vertically therethrough. *Id.* at code (57). A dummy channel structure filled with a dielectric layer is formed vertically in an opening in the dielectric stack. *Id.* Figure 1 of the '322 patent illustrates the structure:



Ex. 1001, Fig. 1. Figure 1 depicts memory device 100 having memory stack 104 including interleaved conductor layers 110 and dielectric layers 112, which includes channel structure 108 filled with semiconductor, and dummy channel structure 146 that is either filled with the same materials as those in channel structure 108 but lacking a connective contact, or is filled with dielectric materials. *Id.* at 5:23–7:4, 9:29–9:40.

#### F. Illustrative Claim

Claims 1 (disclaimed), 8, and 14 are independent. Claim 14 is illustrative because it contains each of the limitations disputed by Patent Owner, and recites as follows:<sup>1</sup>

[14.PRE] A three-dimensional (3D) memory device, comprising:

[14.A] a substrate;

[14.B] a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;

<sup>1</sup> Bracketed organization added as per the Petition. Pet. xvii–xviii.

[14.C] a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;

[14.D] a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a substantially circular section; and

[14.E] a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,

[14.F] wherein: a first diameter of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs; and

[14.G] a peripheral contact is arranged outside the memory stack and in contact with a peripheral device on the substrate.

*G. Evidence*

Petitioner relies on the following patent document evidence.

| <b>Name</b>                                       | <b>Patent Document</b> | <b>Exhibit</b> |
|---------------------------------------------------|------------------------|----------------|
| Nishikawa et al.<br>“Nishikawa”                   | US 9,837,431 B2        | 1005           |
| Lu et al (“Lu”)                                   | US 9,853,046 B2        | 1006           |
| Nishikawa et al.<br>(“Nishikawa123”) <sup>2</sup> | US 9,935,123 B2        | 1046           |

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<sup>2</sup> The parties refer to this reference as “Nishikawa2.”

*H. Prior Art and Asserted Grounds*

Petitioner asserts that claims 3, 6, 8–15, 17, 18, and 20 would have been unpatentable on the following grounds:<sup>3</sup>

| <b>Claim(s) Challenged</b> | <b>35 U.S.C. §</b> | <b>Reference(s)/Basis</b>   |
|----------------------------|--------------------|-----------------------------|
| 3, 6, 8–10, 13–16, 19–20   | 103 <sup>4</sup>   | Nishikawa                   |
| 11, 12, 17, 18             | 103                | Nishikawa, Lu               |
| 3, 6, 8–10, 13–16, 19–20   | 103                | Nishikawa, Nishikawa123     |
| 11, 12, 17, 18             | 103                | Nishikawa, Nishikawa123, Lu |

Pet. 10.

**II. DISCUSSION**

*A. Legal Standards*

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” 35 U.S.C. § 103; *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and

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<sup>3</sup> Although Petitioner challenged claims 1–20, this proceeding does not include disclaimed claims 1, 2, 4, 5, and 7.

<sup>4</sup> We apply AIA 35 U.S.C. § 103 to the ’322 patent because it was filed after, and never claimed the benefit of an effective filing date before, March 16, 2013. Ex. 1001, codes (22), (63); Pet. 6.

(4) objective evidence of non-obviousness.<sup>5</sup> *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

*B. Level of Ordinary Skill in the Art*

Petitioner asserts that a person of ordinary skill in the art (“POSITA”) at the critical time “would have had a Bachelor of Science degree in electrical engineering or a similar discipline, along with 2–3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 27 (citing Ex. 1003 ¶¶ 34–38). Petitioner further asserts that a POSITA “would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts.” *Id.* Patent Owner does not provide any such assessment in its Preliminary Response. Prelim. Resp. 8; Ex. 2007 ¶ 22 (reserving the right to opine as to an alternative level of a POSITA). For purposes of this Decision, we adopt Petitioner’s proposed level of ordinary skill, as it appears to be consistent with the specification of the ’322 patent and the prior art of record.

*C. Claim Construction*

Neither party proposes any express claim construction. Pet. 27 (stating claims should receive their “plain and ordinary meaning”); Prelim. Resp. 7 (stating that Petitioner’s challenges fail “under any reasonable construction”). In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the

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<sup>5</sup> Neither party presents evidence or arguments regarding objective evidence of non-obviousness. Pet. 100; Prelim. Resp.

claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). We determine no terms require express construction for purposes of this Decision.

*D. Nishikawa*

Nishikawa is titled, “3D Semicircular Vertical NAND String With Recessed Inactive Semiconductor Channel Sections.” Ex. 1005, code (54). Nishikawa describes a vertical memory device having dielectric separator structures protruding into a facing pair of sidewalls of a memory stack structure within a memory opening. *Id.* at code (57). Figure 1 is illustrative:

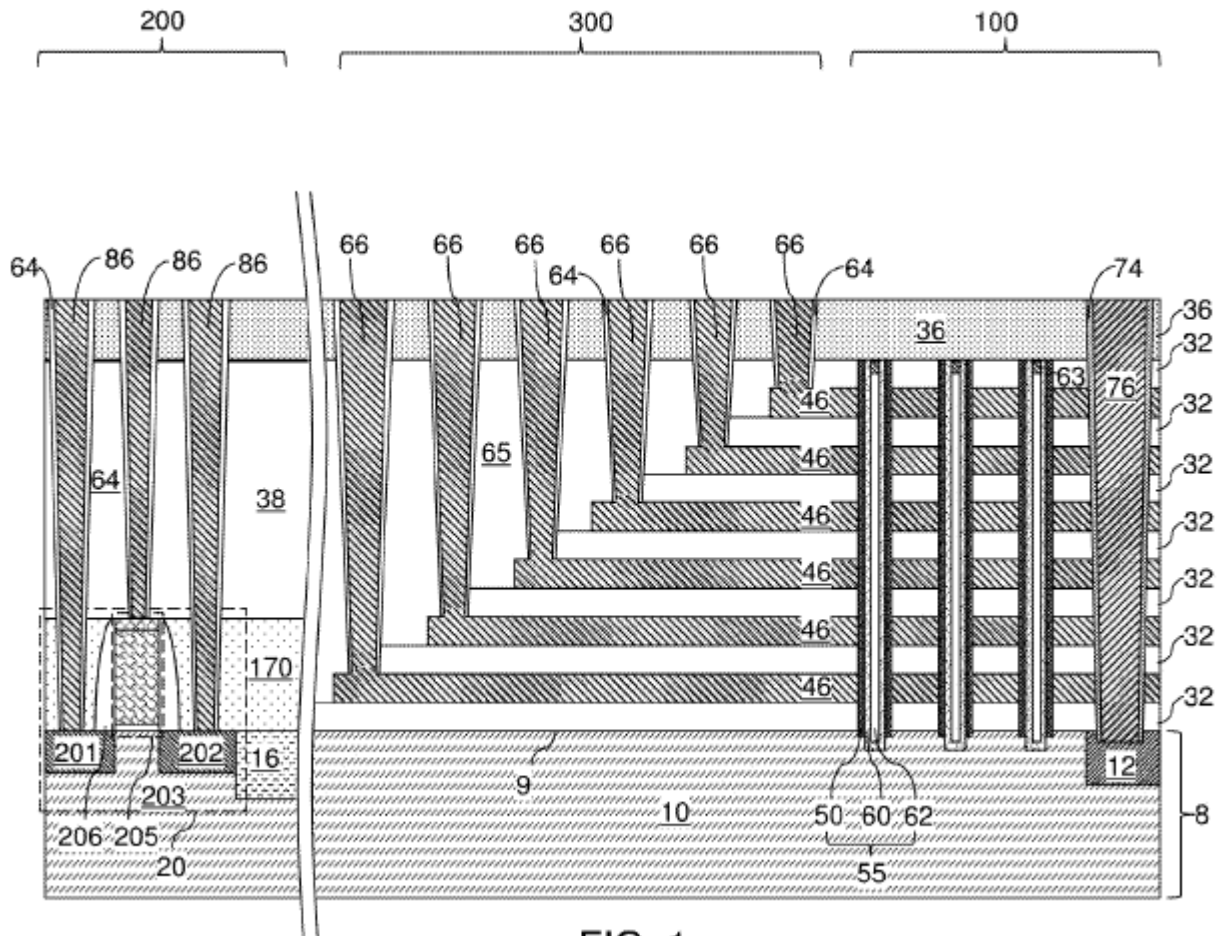


FIG. 1

Figure 1 depicts a 3D NAND stacked memory device having memory stack structures 55 (including memory film 50, semiconductor channel 60, and optionally a dielectric core 62) extending through an alternating stack of insulating layers 32 and conductive (optionally, sacrificial) layers 46, and backside contact via structure 76 providing electrical contact to source region 12. Ex. 1005, 4:22–6:57. Prior to the formation of backside contact via structure 76, etchant is introduced through a contact via stack at the backside contact regions to remove sacrificial material layers 42, which will be replaced with electrically conductive layers 46. *Id.* at 6:29–39.

*E. Nishikawa123*

Nishikawa123 is titled, “Within Array Replacement Openings for a Three-Dimensional Memory Device.” Ex. 1046, code (54). Nishikawa123 describes reduction of backside trenches by using a subset of openings, which are otherwise employed as memory stack structures, to introduce etchant in a process of removing sacrificial material layers in an alternating stack of sacrificial and dielectric layers. *Id.* at code (57). Figure 16 is illustrative:

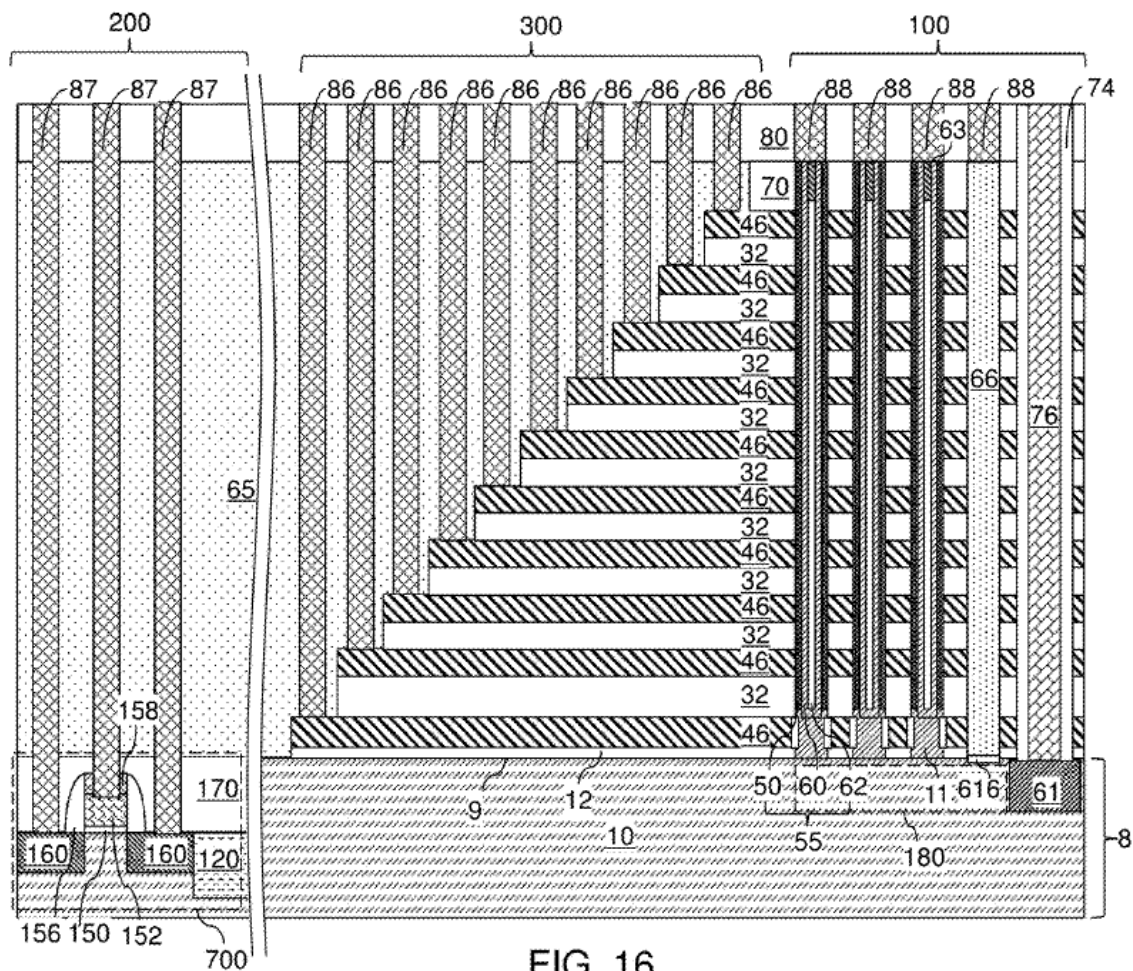


FIG. 16

Figure 16 depicts a 3D memory device including an alternating stack of insulating (23) and conductive (46) layers, memory stack structures 55,

dielectric pillar 66, and backside contact via structure 76. Ex. 1046, 25:55–26:17. Figure 17 provides a top-down view:

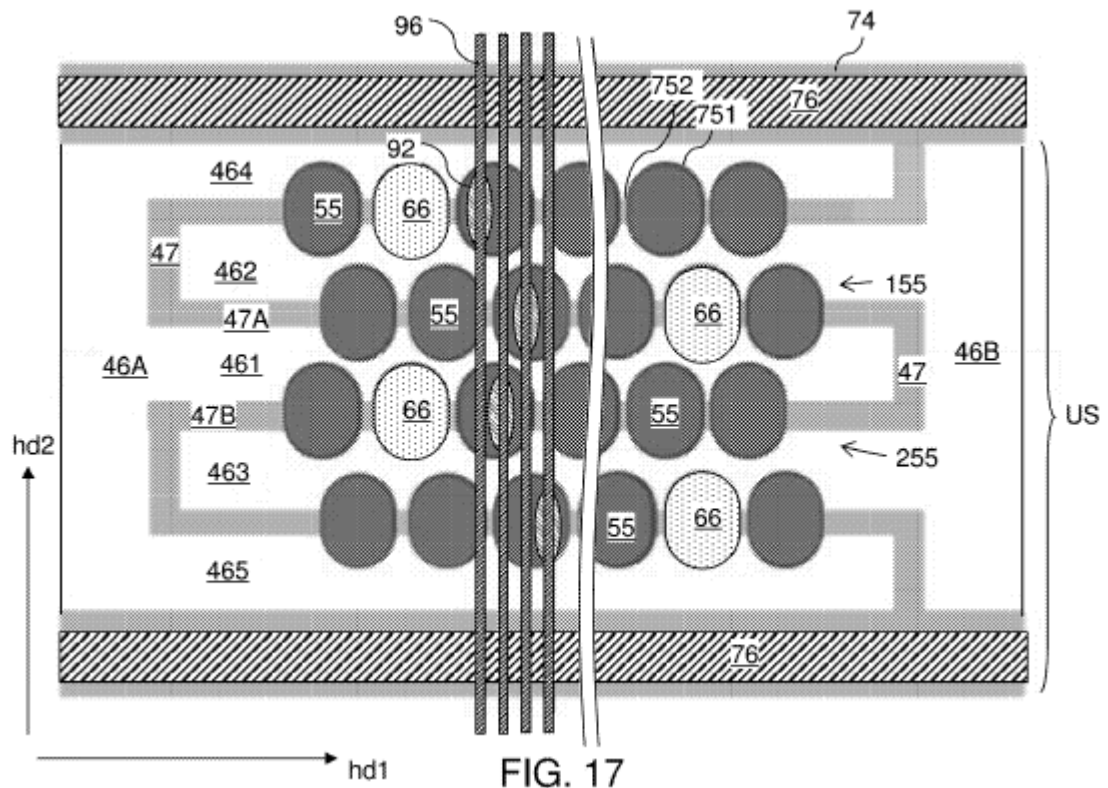


Figure 17 depicts backside contact via structures 76, dielectric pillars 76, memory stack structures 55, and insulator structures 47, 47A, 47B which separate two sets of interdigitated conductive portions 46A, 46B. *Id.* at 26:7–54.

#### *F. Analysis*

Petitioner asserts Nishikawa alone or in combination with Nishikawa123 renders obvious claims 3, 8–10, 13–16, and 19–20 and that Lu teaches the “multi-deck” limitations in dependent claims 11, 12, 17, and 18. Pet. 10, 84–98.

Patent Owner asserts Petitioner has not shown that the asserted art teaches all of the limitations of the challenged claims. In particular, Patent

Owner contests Petitioner's assertions for the limitations of a TAC having a substantially circular section, a limitation present in claims 8–20, and of a dummy channel structure, a limitation present in claims 3, 6, 14–18, and 20. Prelim. Resp. 7–30. Additionally, we address Petitioner's contentions regarding the different lateral dimensions of conductor/dielectric pairs, a limitation present in claims 13–18 and 20.<sup>6</sup>

Because claim 14 includes each of these limitations, we present our discussions relative to claim 14 and explain their impact on the remaining asserted claims. Further, Petitioner relies on Nishikawa123 in all grounds, either explicitly in the ground (Grounds 2 and 4) or as representative of the knowledge in the art (Grounds 1 and 3). Patent Owner addresses Petitioner's Ground 1 and 3 arguments together, and we follow that structure in the following analysis.

*1. “substantially circular section” (claims 8–20)*

With respect to the TAC comprising “a substantially circular section” as recited in limitation 14.D, Petitioner asserts that it would have been obvious to replace Nishikawa's trench-shaped backside contact via structure with a circular-shaped backside via structure. Pet. 43. Petitioner asserts that Nishikawa123 states that its backside trench may have a circular shape, and that Nishikawa123's TACs provide the same structure as Nishikawa's TACs. *Id.* (citing Ex. 1005, Figs. 1, 16; Ex. 1046, Figs. 16, 17; Ex. 1003 ¶ 115). Petitioner points to other prior art demonstrating the well-known nature of circular TACs, including their use in a gate replacement process.

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<sup>6</sup> Petitioner bears the burden of making its obviousness case for institution regardless of whether Patent Owner contests its assertions. 35 U.S.C. § 312(a)(3); *Harmonic Inc. v. Avid Technology, Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016).

*Id.* at 44–50. Petitioner asserts that such prior art teachings demonstrate that replacing a backside contact with a circular TAC was a known technique that would be a suitable option for Nishikawa’s trench and trench contact.

*Id.* at 50–51. Petitioner further provides advantages of a circular TAC to replace the trench in Nishikawa: (1) the smaller footprint frees space for other components, and (2) multiple individual TACs may be spread through the array to provide closer contact points. *Id.* at 51–52.

Patent Owner argues that Petitioner has not provided sufficient motivation to modify Nishikawa’s trench to a circular shape. First, with respect to Ground 1 relying on Nishikawa<sup>123</sup> as representative of the general knowledge in the art, Patent Owner argues that Petitioner’s reliance on “general knowledge” to supply the missing limitations directed to a TAC having a “substantially circular section” is in error because TAC construction is not a “particularly straightforward technology.” Prelim. Resp. 23 (citing *DSS Tech. Mgmt. v. Apple*, 885 F.3d 1367, 1374 (Fed. Cir. 2018)). Patent Owner argues that construction of a TAC involves complex semiconductor processes and multiple etching and filling steps to form. *Id.* (citing Ex. 1001, 15:44-17:8, Figs. 4A–4C, 8; Ex. 2007 ¶ 50).

We disagree with Patent Owner. In *DSS Tech.*, the Federal Circuit held that reliance on “‘ordinary creativity’ ‘as a wholesale substitute for reasoned analysis and evidence support’” without providing “a reasoned explanation that avoids conclusory generalizations” is not sufficient “when dealing with a limitation missing from the prior art references.” 885 F.3d at 1376. There, the Federal Circuit explained that the Board did not identify any evidence to support its reliance on the ordinary creativity of the skilled artisan to supply the missing limitation. *See id.* at 1375; *see also id.* at 1376 (stating that to the extent the Board relies on declarant testimony, such

“conclusory statements and unspecific expert testimony” are insufficient to support the Board’s findings). Unlike the situation presented in *DSS Tech*, the Petitioner here provides sufficient evidence at this stage of the proceeding to support its contention implementing Nishikawa’s backside contact via cylindrical TACs was a suitable, well known option. *See e.g.*, Ex. 1003 ¶¶ 113–128 (citing, *inter alia*, Ex. 1005; Ex. 1010; Exs. 1020–1023; Ex. 1046).

Moreover, *DSS Tech* permits reliance on general knowledge where the missing limitation is “unusually simple.” 885 F.3d at 1374. Here, the missing limitation is the circular shape of the TAC. At this stage of the proceeding, we understand that change of shape of a TAC to a circle is simple, as evidenced by Nishikawa123’s statement that its trench may be in multiple different shapes, including a circle. Ex. 1046, 22:38–39. Although Patent Owner points to the complexity of forming TACs, neither Patent Owner nor Dr. Campbell assert any complexity in changing the shape of a TAC. Prelim. Resp. 23 (citing Ex. 2007 ¶ 50). That is, Dr. Campbell attests that forming any TAC may involve “complex semiconductor manufacturing processes and multiple etching and filling steps,” but does not attest that performing such steps to result in the same structure, but in a different shape, is a matter of complexity. Ex. 2007 ¶ 50. Thus, the current record does not show any particular complexity in changing the shape of a semiconductor TAC feature.

With respect to Ground 3, where Petitioner relies on Nishikawa123 for teaching the circular TAC, Patent Owner asserts a POSITA would not have combined the references because they were filed only 5 days apart. Prelim. Resp. 23. Patent Owner argues that despite the common architecture and named inventor in Nishikawa and Nishikawa123, the omission of a

circular shape from Nishikawa indicates that “the Nishikawa inventors showed that they did not view a circular TAC to apply to the design in the Nishikawa patent.” Prelim. Resp. 23–24. However, obviousness is determined from the standpoint of one of ordinary skill in the art, not from the perspective of the inventors of a particular reference. Patent Owner’s argument goes to what the inventors considered their invention, rather than what one having ordinary skill in the art would recognize as being taught by the references. Thus, Patent Owner’s argument is unavailing at this stage of the proceeding against the obviousness rejection at issue.

With respect to Patent Owner further argues that a POSITA would not have been motivated to modify Nishikawa to use Nishikawa123’s circular TAC because altering Nishikawa’s trench to a circular form “destroys its key function”; i.e., electrically separating its word lines. Prelim. Resp. 24–27. Patent Owner asserts that trench 76 (i.e., the TAC) together with the “separator dielectric structures 45” perform such separation. *Id.* (citing Ex. 1005, 17:14–23; Fig. 16). Patent Owner asserts that Nishikawa123 is only operable if it does not use a circular TAC, and thus, a person having ordinary skill in the art would not be motivated to use Nishikawa123’s circular TAC in Nishikawa. *Id.* at 26–30 (citing Ex. 1046, Fig. 17).

Patent Owner essentially asks that we disregard Nishikawa123’s clear statement that a circular shaped TAC may be used as a TAC. Ex. 1046, 22:38–39 (“The openings 79 can have any suitable shape, such as circular, rectangular, or elongated trench shape.”). Patent Owner argues that a circular shape is not “suitable” (Prelim Resp. 29), but that is incorrect because a circular shape is listed as an example of a “suitable” shape. Ex. 1046, 22:38–39. Patent Owner relies on the Figure 17 embodiment of Nishikawa123 as evidence that a trench, not a circular structure, is required.

Prelim. Resp. 29–30. But Figure 17 portrays only a single embodiment, not the entirety, of Nishikawa123’s disclosure. *Id.* at 3:66–4:2. Petitioner’s reliance on the broader circular shape TAC teaching of Nishikawa123 contradicts Patent Owner’s argument that Petitioner relies only on Nishikawa123’s trench structure. Prelim. Resp. 29–30. Moreover, Patent Owner does not argue that a circular TAC is inoperable in Nishikawa123 which has a “relative similarity” to Nishikawa. *Id.* at 23–24, 29–30. Consequently, Patent Owner has not shown that the trench structure of Figure 17 of Nishikawa123 precludes one having ordinary skill in the art from recognizing and applying Nishikawa123’s teachings relating to non-trench embodiments, including circular TAC teachings.

Additionally, Patent Owner points to the “separator dielectric structures 45” of Nishikawa as contributing to the electric separation of word lines. Prelim. Resp. 25. Patent Owner asserts that dielectric structures 45, not conductive trench 76, perform the electric separation of word lines. *Id.* at 26 (citing annotated Nishikawa Fig. 16, in which the word lines are bounded by dielectric structures 45); Ex. 1005, 6:57–69 (“A dielectric spacer 74 can be employed to provide electrical isolation for the backside contact via structure 76”). Although Patent Owner and Dr. Campbell hypothesize that removal of portions of the conductive trench 76 would necessitate removal of dielectric structures 45 in a manner to short circuit the neighboring word lines, Petitioner has not proposed any removal of separating dielectric structures in its change of shape of trench 76 to a circular shape. *See* Pet. 43–53. Nor does Dr. Campbell explain why altering TAC trench 76 would necessitate altering dielectric structures needed to prevent a short circuit. Ex. 2007 ¶¶ 51–56. For this additional reason,

Patent Owner's argument that the combination would be inoperable is not supported by the current record.

Consequently, we determine that Petitioner has sufficiently shown at this stage of the proceeding its contentions for Grounds 1 and 3 that Nishikawa alone, or in combination with Nishikawa123, teaches or suggests the “substantially circular section” recited in claim 14. For the same reasons, Petitioner has also sufficiently shown that the “substantially circular section” recited in claims 8, and 19, and incorporated through dependency in claims 9–13, 15–18, and 20, would have been obvious over Nishikawa alone, or in combination with Nishikawa123.

2. *“dummy channel structure” (claims 3, 6, 14–18, 20)*

Claims 3, 6, 14–18, and 20 each require a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack. With respect to the dummy channels as recited in limitation 14.E, Petitioner asserts that Nishikawa teaches channel structures and that a person having ordinary skill in the art would have been motivated to include dummy channels, of either the same materials or with a solid dielectric fill, in Nishikawa's memory stack. *See, e.g.*, Pet. 59–64, 82. Petitioner asserts that it was well known to a person having ordinary skill in the art to include dummy channels. *Id.* at 59, 63.<sup>7</sup> Petitioner asserts that a POSITA would have been motivated to add dummy channels to Nishikawa. In particular, Petitioner asserts that adding dummy channels would (1) reduce the likelihood of defective bits on the edge of the memory cell region; (2) result in a more uniform feature pattern

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<sup>7</sup> As acknowledged by Patent Owner, Petitioner does not rely on Nishikawa123 for teaching dummy channels. Prelim. Resp. 8.

so as to reduce processing issues; (3) provide structure support in a gate replacement process; and (4) free space above the structures while serving as support structures, made by the same process and at the same time as active channels. *Id.* at 59–63.

Patent Owner argues against these asserted benefits. Prelim. Resp. 7–22. Patent Owner argues that Petitioner insufficiently supports advantages (1), that dummy channels would reduce the likelihood of defective bits on the edge of the memory cell region and increase the uniformity of the feature pattern and thereby reduce processing issues, and (2), that the additional dummy structures would be placed at “the edge of the memory cell region” to extend the memory cell pattern in such a manner as to “result in an overall more uniform feature pattern.” Pet. 59–60.

We agree with Patent Owner. Although Dr. Lee attests that “it is common to refrain from using the cells at the array edge,” which are “sometimes referred to as dummy cells,” due to “processing variations,” this does not show an advantage to adding dummy channels. Ex. 1003 ¶ 141 (quoting Ex. 1024, 8:47–53). To the extent that Dr. Lee states that dummy channels should be added, Dr. Lee attests that such a dummy region at the edge of the array is “later sacrificed in processing,” which would not result in the claimed limitation of a “dummy channel structure . . . in the memory stack.” *Id.* (citing Ex. 1025, 2:20–43).

We also agree with Patent Owner’s argument for point (3), that Nishikawa already discloses structures for providing structural support. Prelim. Resp. 9–10 (citing Ex. 1005, 10:10–12 (“Separator dielectric structures can provide structural support to the insulating layers 32 after formation of the interlayer cavities”)). We agree with Patent Owner that Petitioner does not address the support provided by these structures in

Nishikawa, which is for the same purpose as Petitioner's added dummy channels; i.e., to support recesses caused by loss of sacrificial material during the gate replacement process. Prelim. Resp. 9–11; Pet. 60–63. To the extent that Petitioner's addition of dummy structures would result in additional structural support to Nishikawa's existing separator dielectric structures, Petitioner has not explained how such additional support beyond what Nishikawa discloses, in view of any tradeoffs with additional processing needed to create additional dummy channels, would be viewed as desirable by a person having ordinary skill in the art. Consequently, the record does not support Petitioner's reason to combine dummy channels as known in the art with the teachings of Nishikawa. We further agree with Patent Owner that to the extent Petitioner's advantage (4) is similarly premised on providing additional support, it are unpersuasive on the current record. Prelim. Resp. 20–21.

Because Petitioner has not shown the combined references to teach the claimed dummy channels of claim 14, Petitioner has not shown, by a reasonable likelihood, that claim 14 would have been obvious over Nishikawa or Nishikawa and Nishikawa123. Claims 3, 6, 15–18, and 20 also contain a “dummy channel” limitation. Consequently, we determine that Petitioner has not met its burden for claims 3, 6, 14–18, and 20.

3. *Different lateral dimensions of layer pairs (claims 13–18, 20)*

Claim element 14.F requires a “first diameter of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs.” Petitioner relies upon the general knowledge in the art to teach a lateral dimension (diameter) of the conductive/dielectric layer pairs being larger than a second lateral

dimension of the conductive/dielectric pairs. Pet. 75 (citing Ex. 1037 (“Cui”); Ex. 1027 (“Kai”); Ex. 1003 ¶¶ 172–175), 82. Petitioner asserts that it would have been obvious for Nishikawa’s TAC to have a ribbed shape, that is, forming recesses in one of the stack layers because it was known in the art to create recesses in conductor/dielectric layers to form a ribbed via cavity. *Id.* (citing Ex. 1031 (“Cui”), Fig. 16A, 26:23–33). Petitioner further asserts that such a ribbed via cavity is advantageous because it creates additional area for the dielectric liner (spacer). *Id.* at 76 (citing Ex. 1003 ¶ 129). However, neither Petitioner nor Dr. Lee explain why this additional area is advantageous, except that it serves the same purpose as the lateral recesses in the ’322 patent. Ex. 1003 ¶ 173. But a reason to combine should not be obtained solely from the challenged patent. *KSR*, 550 U.S. at 421 (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”); *Metalcraft of Mayville, Inc. v. Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) (“[W]e cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention.”).

Similarly, Petitioner’s alternate assertion that typical prior art etches would result in such lateral recesses (Pet. 74–75) does not show that a person of ordinary skill in the art would find such to be a desirable combination. Petitioner asserts that typical prior art etches for creating holes in a stack “were also known to result in lateral recesses in either the dielectric spacers or sacrificial layers.” *Id.* (citing Ex. 1039 (U.S. Pat. 11,075,084)). Petitioner asserts that unintentional recesses are formed during etching because “it is a challenge to find an etch gas . . . in terms of getting a smooth sidewall of high aspect ratio holes in 3D NAND memory.” *Id.* at 74 (quoting Ex. 1039, 2:59–67); Ex. 1003 ¶ 170. However, Petitioner

admits that same reference states that “it is important to have an etching gas which can etch both . . . layers without selectivity” to result in “a smooth sidewall.” Pet. 74 (quoting Ex. 1039, 59–67). Thus, Petitioner’s assertion that a person having ordinary skill in the art would seek to use etches that would result in the claimed first and second diameters is insufficiently supported.

Because Petitioner has not shown the combined references to teach the claimed diameters of claim 14, Petitioner has not shown, by a reasonable likelihood, that claim 14 would have been obvious over Nishikawa or Nishikawa and Nishikawa123. Claims 15–18 and 20 also contain a “dummy channel” limitation. Consequently, we determine that Petitioner has not met its burden for claims 13–18 and 20.

*4. Conclusion Claims 3, 6, 13–18, and 20*

As explained above, Petitioner has not sufficiently shown that the asserted art teaches or suggests the dummy channel structure required by claims 3, 6, 14–18, and 20, or the different lateral dimensions/diameters of layer pairs required by claims 13–18 and 20. As such, Petitioner has not shown a reasonable likelihood that it would prevail in showing the unpatentability of these claims, i.e., claims 3, 6, 13–18, and 20.

*5. Claims 8–12, and 19*

We further determine that Petitioner has sufficiently shown that Nishikawa discloses the remaining limitations of claims 8–10 and 19, which contain the “substantially circular” but not the “dummy channel” or two lateral dimensions limitations. To the extent limiting, Nishikawa describes a three-dimensional memory device as set forth in limitations 1.PRE<sup>8</sup> and

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<sup>8</sup> Claim 19 depends from claim 1.

8.PRE. Ex. 1005, 2:3–3:41; Pet. 34. Nishikawa describes a memory stack comprising alternating conductor/dielectric layers (layers 46 and 32) on substrate 8, as set forth in limitations 1.A/B and 8.A/B. Ex. 1005, Fig. 1, 4:43–56, 6:4–5; Pet. 35–36. Nishikawa further describes a channel structure (memory stack structure 55) extending vertically through the paired layers in the memory stack, as set forth in limitations 1.C and 8.C. Ex. 1005, Fig. 1, 11:33–39; Pet. 36–38. Nishikawa further describes a through array contact (backside contact via structure 76) extending vertically through the conductor/dielectric pairs 46/32 and buried into substrate 8, as set forth in limitations 1.D and 8.D. Ex. 1005, Fig. 1 ; Pet. 39–40; Ex. 1003, 110–11; *see* Prelim. Resp. 22 n.5 (“Patent Owner does not challenge Petitioner’s characterization of Nishikawa’s trench 76 as a TAC”). Nishikawa further describes a slit structure, separator dielectric 45, as set forth in limitation 1.E.

Nishikawa further describes peripheral contact via structures 86 (peripheral contact) arranged outside the memory stack and in contact with a peripheral device 20 on the substrate, as set forth in limitation 9.A. Ex. 1005, Fig. 1, 4:36–39, 5:30–45, 6:52–54. These elements are shown in Figure 1 of Nishikawa:



We also determine that Petitioner has met its burden for institution to show the obviousness of the thickness and material limitations 9.B and 10. Pet. 79–81.

We further determine that Petitioner has met its burden for institution for limitations 11 and 12 to show the obviousness of the upper and lower memory decks (decks 401, 402), the upper and lower channel structures (channel materials 424, 434), an inter-deck plug (material 437) in view of Lu's teachings. Pet. 79–81, 84–97.

Thus, we determine that Petitioner has shown a reasonable likelihood of prevailing on its assertions for six claims (8–12 and 19) out of a total of 15 challenged claims.

### III. CONCLUSION

Based on the foregoing, we determine that Petitioner establishes a reasonable likelihood that it will prevail on its challenge to at least one claim of the '322 patent. Our determination at this stage of the proceeding is based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which an *inter partes* review has been instituted. Our final decision will be based on the full record developed during trial.

Accordingly, we institute an *inter partes* review of all the challenged, non-disclaimed claims on all the challenged grounds; i.e.:

| Claim(s) Challenged      | 35 U.S.C. § | Reference(s)/Basis          |
|--------------------------|-------------|-----------------------------|
| 3, 6, 8–10, 13–16, 19–20 | 103         | Nishikawa                   |
| 11, 12, 17, 18           | 103         | Nishikawa, Lu               |
| 3, 6, 8–10, 13–16, 19–20 | 103         | Nishikawa, Nishikawa123     |
| 11, 12, 17, 18           | 103         | Nishikawa, Nishikawa123, Lu |

### I. ORDER

For the foregoing reasons, it is:

ORDERED that an *inter partes* review is instituted with respect to all of the grounds asserted in the Petition with respect to the non-disclaimed challenged claims; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

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Patent 11,581,322 B2

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