

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00191
Patent 11,581,322

**DECLARATION OF STEPHEN CAMPBELL
IN SUPPORT OF
PATENT OWNER'S RESPONSE**

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I. Introduction

1. I have been retained by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) to provide my opinion concerning the validity of U.S. Patent No. 11,581,322 (Ex. 1001, “’322 Patent”). I have been asked to consider the scope and content of the prior art, and respond to certain allegations regarding the prior art, presented by Micron Technology, Inc. (“Petitioner”) in its petition for *inter partes* review of the ’322 Patent (“Petition”) and the December 2, 2024, Declaration of Dr. Jack Lee (Ex. 1003, “Lee Decl.”). The arguments raised in Dr. Lee’s declaration are similar to those raised in the Petition. Unless otherwise noted, my opinions with respect to the Petition also apply to the corresponding section of Dr. Lee’s declaration, and vice versa. As explained below (discussing the Grounds raised in the Petition), the invalidity arguments raised in the Petition do not show the prior art in view of the knowledge of a person of ordinary skill in the art (“POSITA”) renders obvious any of the Challenged Claims, and the arguments raised in Dr. Lee’s declaration are insufficient for similar reasons.

2. I have previously rendered my opinion in support of the Patent Owner’s Preliminary Responses. While I believe that declaration is accurate in all respects, **this new Declaration represents my considered opinion and supersedes my previous Declaration.** There are no substantive differences

between the two, but any ambiguities should be resolved in favor of this declaration.

3. Where possible, I have used the exhibit numbers connected to the Petition for *Inter Partes* Review of the '322 Patent (IPR2025-00191).

4. I am being compensated for my time at my usual consulting rate of \$450 per hour, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with Patent Owner ("PO") in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

5. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

II. Qualifications

6. My qualifications, including cases in which I was an expert, are stated more fully in my curriculum vitae which has been provided as Exhibit 2008. Here, I provide a brief summary of my qualifications.

7. I received my Bachelor's degree in Physics from the University of St. Thomas (St. Paul, Minnesota) in 1975, and my M.S. and Ph.D. in Physics from Northwestern University (Evanston, Illinois) in 1978 and 1981, respectively. I then

joined Sperry, now called Unisys, in 1981 as a CMOS process development engineer. In 1982, I was assigned, the lead engineer for the 1.2 μm technology process development effort. In 1984 I was promoted to head of silicon research for the company. This involved a wide variety of process technologies for submicron CMOS.

8. In 1986, I joined the University of Minnesota as an Assistant Professor in the Electrical Engineering Department. My research at the University involved semiconductor processing, materials, and device structures. I raised more than \$100M in various grants and successful submissions to companies and industry consortiums such as the Semiconductor Research Association, as well as State and US government agencies including DARPA and the National Science Foundation. The first ten years of my career at the University concentrated on the development of rapid thermal annealing for 200 mm wafers, particle control in CVD systems, and the development of high uniformity rapid wafer annealing systems. The next ten years were dedicated to the invention and development of high permittivity (aka high-k) films for use as gate insulators. This is necessary to allow the development of deeply scaled CMOS devices. This technology has been widely adopted for nanoscale CMOS devices. In the last fifteen years at the University, my work involved the development of low-cost tandem photovoltaics and micro electromechanical systems (MEMS). The latter included a chronic deep

brain sense/stimulation system and very high-speed mechanical switches. Finally, I developed processes for the fabrication of novel 2D materials such as black arsenic, and fabricated transistors using these materials. I retired from the University in 2021.

9. A brief summary of my work at the University would include:

- Approximately 200 publications
- The leading textbook on semiconductor technology. Currently in its fourth edition, Fabrication Engineering at the Micro and Nanoscale (Oxford 1996, 2000, 2008, 2013) is the dominant text on the topic.
- Honors from outside the University such as being named a Presidential Young Investigator by the National Science Foundation and a Life Fellow by the Institute of Electrical and Electronics Engineers (IEEE).
- Honors within the University including outstanding service and outstanding teaching.
- As the Director of the University's Nanofabrication Center, I increased lab usage from 30 to more than 300 users, enabling millions of dollars research awards annually by Minnesota faculty,

and leading to the construction of a new \$80M building with an expansive cleanroom facility.

10. Since retiring from the University, I have consulted with semiconductor companies, including regarding patent litigation.

11. Additional information regarding my education, technical experience and publications, including a list of the U.S. patents of which I am an inventor/coinventor, is included in my *Curriculum Vitae* (Exhibit 2008).

III. Understanding of Legal Standards

12. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

13. My understanding of the pertinent law is outlined below and is the result of explanations provided by counsel. I have applied this understanding in my analysis.

A. Interpreting Claims in an *Inter Partes* Review Proceeding (Claim Construction)

14. I understand that an *Inter Partes* Review is a proceeding before the United States Patent & Trademark Office (“USPTO”) for evaluating the validity of one or more claims of an issued patent.

15. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary.

16. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the USPTO. I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Invalidity by Obviousness

17. I understand that a patent claim is unpatentable if it is obvious in view of the prior art. I further understand that a claim is unpatentable if it is obvious from the perspective of a person of ordinary skill in the relevant art (“POSITA”), at the time the invention was made.

18. It is my understanding that a claimed invention is unpatentable as obvious under 35 U.S.C. § 103 if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

19. I have been informed that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of the claimed subject matter. I understand that several of these rationales are: 1) combining prior art elements according to known methods to yield predictable results; 2) simple substitution of one known element for another to obtain

predictable results; 3) use of a known technique to improve a similar device (method or product) in the same way; 4) applying a known technique to a known device (method or product) ready for improvement to yield predictable results; 5) choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success, 6) and some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. Such a teaching, suggestion, or motivation to combine the prior art references may be explicit or implicit in the prior art, or may be found in other evidence of the level of skill and knowledge of the ordinary artisan.

20. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by

Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

21. I have also been informed by Counsel that a patent claim may have been invalid as obvious where a limitation is undisclosed but inherently present in the prior art, but that the limitation is only inherently present if it is necessarily present or the natural result of the combination.

22. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

23. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the

invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form of hindsight. A motivation to combine based on the teachings of the challenged patent is also an impermissible form of hindsight bias. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

24. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated to make a combination includes whether he/she would select particular references in order to combine their elements.

25. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as

inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

26. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, knowledge of a POSITA can only be used to supply a limitation missing from the prior art where the recited limitation is unusually simple and the relevant technology particularly straightforward.

27. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be

taken into account in determining obviousness. I have also been informed by Counsel that where a prior art reference contains an error that is obvious to a POSITA, that reference cannot be said to describe or suggest the information subject to the error. That is, if a prior art document contains an error that would be immediately apparent to a POSITA, and the correct information is also readily apparent, that erroneous information is not considered part of the prior art that can be used to invalidate a patent.

IV. Summary Of Materials Reviewed And Considered

28. I have been asked to provide analysis and explain the subject matter of the '322 Patent, including the state of the art when the application underlying the '322 Patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '322 Patent including how that art relates to claims 3, 6, 8-20 (which I refer to as the “challenged claims”) of the '322 Patent and to provide my opinions regarding whether that art invalidates the challenged claims. I understand that the Petition challenged more than the challenged claims, but Patent Owner disclaimed a portion of the originally challenged claims.

29. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the challenged claims of the '322 Patent. Therefore, the fact that I do not address a particular point

should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

30. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '322 Patent.

31. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor design and fabrication, I reviewed the following documents:

Ex.	Description
1001	U.S. Patent No. 11,581,322 to Guo et al. ("the '322 Patent")
1003	Declaration of Dr. Jack C. Lee ("Lee Decl.")
1005	U.S. Patent No. 9,837,431 to Nishikawa et al. ("Nishikawa")
1006	U.S. Patent No. 9,853,046 to Lu et al. ("Lu")
1009	U.S. Patent No. 10,777,501 to Nakajima et al. ("Nakajima")
1010	Micheloni, "3D Flash Memories" (2016)
1012	U.S. Patent No. 10,354,980 to Mushiga et al. ("Mushiga")
1020	U.S. Patent Publication No. 2018/0301374A1 to Masamori et al. ("Masamori")
1024	U.S. Patent No. 5,945,717 to Chevallier
1025	U.S. Patent No. 10,347,487 to Lee et al.

Ex.	Description
1026	Ronse, “Optical lithography—a historical perspective,” C. R. Physique 7 (2006) (“Ronse”)
1027	U.S. Patent No. 10,290,643 to Kai et al. (“Kai”)
1028	U.S. Patent No. 9,859,297 to Park et al. (“Park297”)
1029	U.S. Patent Publication No. 2018/0308559 to Kim et al. (“Kim”)
1030	U.S. Patent No. 8,945,996 to Tang et al.
1036	U.S. Patent Publ. No. 2019/0081061 to Tessariol et al.
1037	U.S. Patent No. 10,304,852 to Cui et al. (“Cui”)
1039	U.S. Patent No. 11,075,084 to Shen et al.
1046	U.S. Patent No. 9,935,123 to Nishikawa (“Nishikawa123”)
2001	Defendants’ Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)
2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
2004	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 14, 2025), ECF No. 243

Ex.	Description
2005	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending Inter Partes Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2006	Disclaimer in Patent Under 37 C.F.R. § 1.321(a)
2007	Declaration of Dr. Stephen A. Campbell ("Campbell")
2008	<i>Curriculum Vitae</i> of Dr. Stephen A. Campbell
2009	<i>Inside Solid State Drives (SSDs)</i> (Rino Micheloni et al. eds., 2d ed. 2018)
2018	Order Granting Motion to Consolidate, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Aug. 21, 2024), ECF No. 106
2020	U.S. Patent Application Publication No. 2007/0358593 A1, Published Dec. 14, 2017
2022	Transcript of the Deposition of Jack C. Lee, Ph.D., taken July 30, 2025, <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00034 ("Lee '254 Dep.")
2023	Harmeet Singh, <i>Overcoming Challenges in 3D NAND Volume Manufacturing</i> , 60 Solid State Technology 18 (July 2017)
2024	Thermo Fisher Scientific, <i>White Paper: The Challenge of Measuring Buried Critical Dimensions in High-Aspect-Ratio Structures: How Busy Fab Process Owners Can Reduce Time-to-Data in 3D NAND Metrology</i> , https://assets.thermofisher.com/TFS-Assets/MSD/Reference-Materials/helios-5-pxl-3d-nand-whitepaper-wp0025.pdf (last visited Aug. 5, 2025)
2025	Mark Lapedus, <i>What's Next for NAND?: Vendors Pin Hopes on 3D Memory, Raising Specter of 2D NAND Shortages; Other Memory Types Add to Uncertainty</i> , Semiconductor Eng'g (May 19, 2016), https://web.archive.org/web/20161127122539/https://semiengineering.com/whats-next-for-nand/ (last visited Aug. 15, 2025)

Ex.	Description
2026	Mark Lapedus, <i>3D NAND Flash Wars Begin: Market Overcrowding, More Efficient Manufacturing, and Growing List of Scaling Issues Create a Challenging Competitive Landscape</i> , Semiconductor Eng'g (Aug. 20, 2018), https://web.archive.org/web/20180822030129/https://semiengineering.com/3d-nand-flash-wars-begin/ (last visited Aug. 15, 2025)
2027	Mark Shirey & Janay Camp, <i>Digging Deep Into High Aspect Ratio Process Control for Memory Technology</i> , Semiconductor Eng'g (Oct. 18, 2018), https://web.archive.org/web/20250621011306/https://semiengineering.com/digging-deep-into-high-aspect-ratio-process-control-for-memory-technology/ (last visited Aug. 15, 2025)
2028	Mark Lapedus, <i>3D NAND Metrology Challenges Growing: Rising Costs and Gaps in Equipment Emerge as Technology Scales; New Tools Under Development</i> , Semiconductor Eng'g (Apr. 9, 2019), https://semiengineering.com/3d-nand-metrology-challenges-growing/
2029	Mark Lapedus, <i>3D NAND's Vertical Scaling Race: More Competition, Business Uncertainty, and Much More Difficult Manufacturing Processes</i> , Semiconductor Eng'g (Dec. 17, 2020), https://semiengineering.com/3d-nands-vertical-scaling-race/
2030	Yongsik Yu, <i>Tech Brief: Memory "Grows Up" with 3D NAND</i> , Lam Rsch. Newsroom (Apr. 11, 2016), https://newsroom.lamresearch.com/Tech-Brief-Memory-Grows-Up-with-3D-NAND (last visited Aug. 5, 2025)
2031	Mark Lapedus, <i>NAND Market Hits Speed Bump: Transition from Planar to 3D NAND is Harder and More Time-Consuming Than Expected</i> , Semiconductor Eng'g (June 21, 2017), https://web.archive.org/web/20180625071314/https://semiengineering.com/nand-market-hits-speed-bump/ (last visited Aug. 15, 2025)

Ex.	Description
2032	Mark Lapedus, <i>3D NAND Race Faces Huge Tech and Cost Challenges: Shakeout Looms as Vendors Struggle to Find Ways to Add More Layers and Increase Density</i> , Semiconductor Eng'g (May 23, 2019), https://web.archive.org/web/20190619034609/https://semiengineering.com/3d-nand-race-faces-huge-tech-and-cost-challenges/ (last visited Aug. 15, 2025)
2033	Mark Lapedus, <i>How to Make 3D NAND: Foundries Progress With Complex Combination of High-Aspect Ratio Etch, Metal Deposition and String Stacking</i> , Semiconductor Eng'g (May 23, 2016), https://semiengineering.com/how-to-make-3d-nand/ (last visited Aug. 15, 2025)
2034	Timothy Yang, <i>Creating Higher Density 3D NAND Structures: Identify the Manufacturing Issues Associated With Increased 3D NAND Density to Make the Best Tradeoffs and Avoid Structural Collapse</i> , Semiconductor Eng'g (Feb. 21, 2019), https://semiengineering.com/creating-higher-density-3d-nand-structures/ (last visited Aug. 15, 2025)
2035	Seong Jae Yoo et al., <i>Highly Selective Etching of SiN_x Over SiO₂ Using ClF₃/Cl₂ Remote Plasma</i> , 34 Nanotechnology 465302 (2023)
2036	Entegris, <i>White Paper: Considerations for Improving 3D NAND Performance, Reliability, and Yield</i> , https://www.entegris.com/content/dam/web/resources/white-papers/whitepaper-improving-3d-nand-performance-8443.pdf (last visited Aug. 5, 2025)
2038	Transcript of the Deposition of Jack C. Lee, Ph.D., taken October 23, 2025, <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00191 (“Lee Dep.”)

32. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the '322

Patent at the time of the alleged invention, which I have been asked to assume is August 21, 2018.

V. Level of Ordinary Skill in the Art

33. I understand that certain issues relating to validity must be judged from the perspective of a person of ordinary skill in the relevant art at the time of the invention, which I have been told is August 21, 2018.

34. Petitioner defines a POSITA as a person having “a Bachelor of Science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts.” Pet. 27.

35. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art, except that to the extent Petitioner asserts “designing” includes circuit design. It is my opinion that circuit design is not relevant to the ’322 Patent. A POSITA in the subject matter of the ’322 Patent—3D NAND structures—does not include 2-3 years of professional experience in circuit design. In view of my educational background and work

experience, I was at least a POSITA under Dr. Lee's definition, and was so before August 21, 2018. Regardless of the precise definition of a POSITA, Grounds 1-4 of the Petition do not show the challenged claims obvious.

VI. Claim Construction

36. Petitioner alleges in its claim construction section that “the terms of the '322 Patent's claims do not require further construction and should receive their plain and ordinary meaning.” Pet. 27. Dr. Lee similarly states that “the challenged claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.” Lee Decl., ¶ 80.

37. However, when Petitioner and Dr. Lee analyze the '322 Patent claims reciting the “a lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs” (“ribbed via cavity”), they allege that Nishikawa (Ex. 1005) and the knowledge of a POSITA render obvious these limitations under two different claim constructions: (1) by inherent “unintentional recesses” formed by the typical etching process (Pet. 74-75; Lee Decl., ¶171), and (2) by an “intentional etch that forms actual recesses” (Pet. 75-77; Lee Decl., ¶¶ 172-175). Pet. 74-75 (describing the first claim construction as “PO's Incorrect Claim

Interpretation” and the second claim construction as “The Correct Claim Interpretation”); Lee Decl., ¶¶ 169-172.

38. The prior art relied on in the Petition fails to disclose the subject matter of the remaining challenged claims under any reasonable construction, including their plain and ordinary meaning. It is my opinion that no claim construction is necessary to determine that the challenged claims are valid in this proceeding.

VII. Background

A. Only Claims 3, 6, and 8-20 are at Issue

39. I understand that Micron challenged claims 1-20 of the '322 Patent on four grounds, all of which rely on Nishikawa. Pet. 10. I have been informed by counsel that on February 21, 2025, YMTC disclaimed claims 1-2, 4-5, and 7 before the Board's institution decision. ID, 2, 7 n.3. I understand only claims 3, 6, 8-20 are at issue in this proceeding and that the Board found Micron only met its burden for institution for claims 8-12 and 19. ID, 2.

B. 3D NAND Memory Technology

40. 3D NAND memory devices are a type of non-volatile flash memory that stacks memory cells vertically in multiple layers, unlike traditional 2D NAND which lays them out horizontally. Memory cells can be written or read by applying a voltage to corresponding conductors that run horizontally across the memory array, called “wordlines.” 3D NAND offers fast read and write speeds due to

shorter connection paths between layers, leading to reduced latency and increased performance. As seen below in Figure 5.20 of Exhibit 2009, an exemplary 3D NAND memory depicts a series of vertically stacked memory cells, each controlled by a “Control Gate” (the wordline) shown in red as “CG0” through “CG3.” Ex. 2009, 134. The ends of the “Control Gates” are staggered to form a staircase that allows vertical vias to access and contact each wordline (CG0 to CG3) and connect them to peripheral devices.

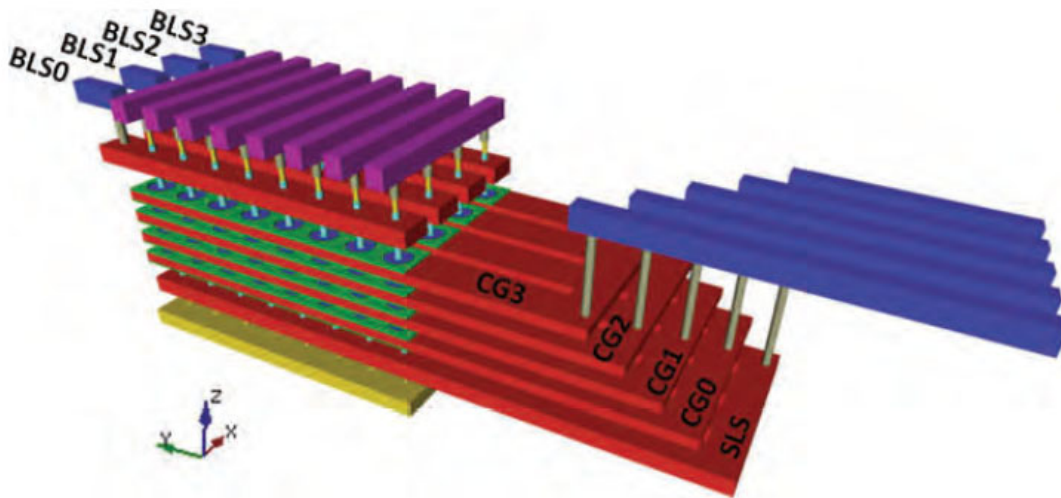


Fig. 5.20 C-FG NAND Flash array with fan-out

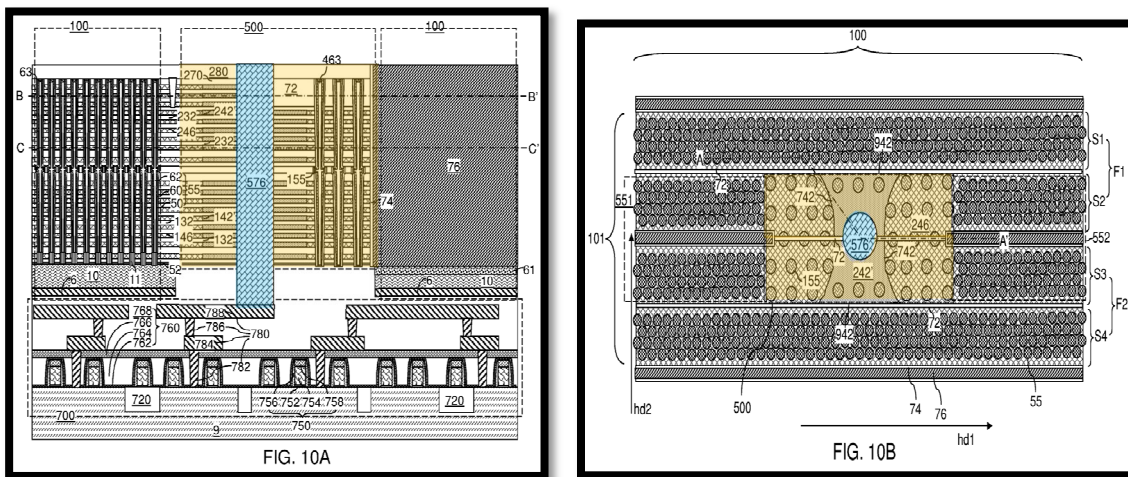
Ex. 2009, 134 (Fig. 5.20).

A. Overview of the '322 Patent (Ex. 1001)

41. The '322 Patent teaches that 3D memory devices require contacts that go vertically through the memory stack called “through array contacts” or “TACs” for “providing vertical interconnects between the stacked memory array device and peripheral device (e.g., for power bus and metal routing).” '322 Patent, 4:58-62.

Conventionally, TACs were formed within a “barrier structure” preserving a “dielectric stack region within a memory stack.” *Id.*, 4:62-65. Barrier structures had shortcomings, including that “the regions enclosed by the barrier structures take up large area in the core array region where memory strings can be formed.” *Id.* at 4:62-5:1.

42. An example TAC (blue) formed within a barrier structure (gold) is shown below in Figures 10A and 10B (annotated) from U.S. Patent Application Publication 2017/0358593 (Ex. 2020), “Yu”). Here, the TAC and barrier structure are formed in a region 500 “in which through-memory-level via structures that extend vertically through a memory-level assembly are subsequently formed.” Yu [0051].



TACs within a barrier structure “also have a negative impact on the resistance of word lines.” ‘322 Patent, 4:62-5:1. “Moreover, the existing fabrication processes for forming the barrier structures become more challenging for the next generation

3D memory devices” which “have less process margin” (i.e., room for error). *Id.*, 5:2-5.

43. The '322 Patent discloses a unique “3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures.” *Id.*, 5:6-9. The '322 Patent explains that “by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost.” *Id.*, 5:9-12. In addition, “[m]ore process margin”—i.e., room for error—“may be obtained due to the elimination of etching and alignment steps for making the barrier structures.” *Id.*, 5:13-18. To “further simplify the fabrication flow and reduce process cost,” the '322 Patent teaches that the non-barrier structure TACs can be “formed in the same fabrication process(es) for making other structures” such as “peripheral contacts” outside of the memory stack. *Id.*, 5:17-23. As a result, the non-barrier structure TACs 416 can have the same shape as the peripheral contact 420, including a “substantially circular shape in the plan view,” as shown in Figure 4C below where the circular cross-section of the TAC (green box) matches the circular cross-section of the peripheral contact (blue box). *Id.* 8:56-57. The '322 Patent also discloses “dummy channel structures 146 can provide mechanical support to the memory array structures, e.g., memory stack 104.” *Id.*

9:41-43. The dummy channels supplement the support function the omitted barrier structure would have.

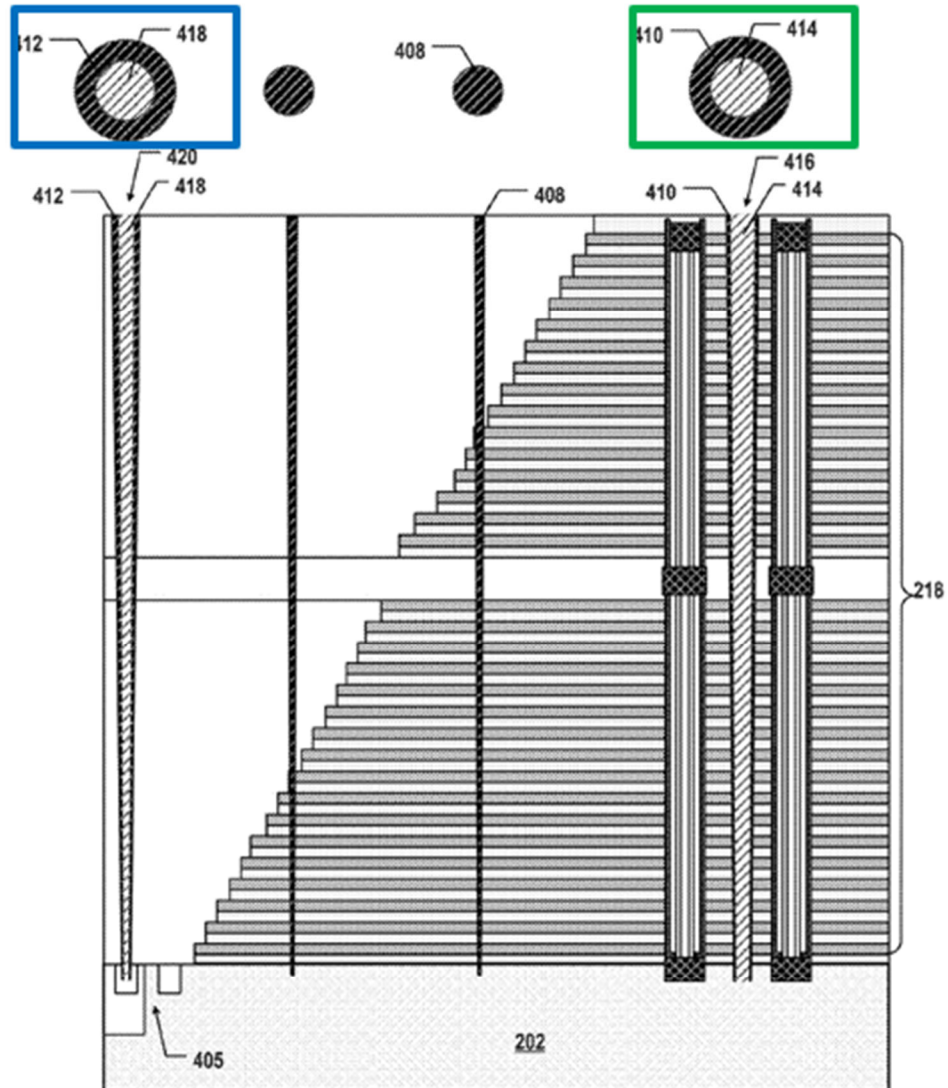
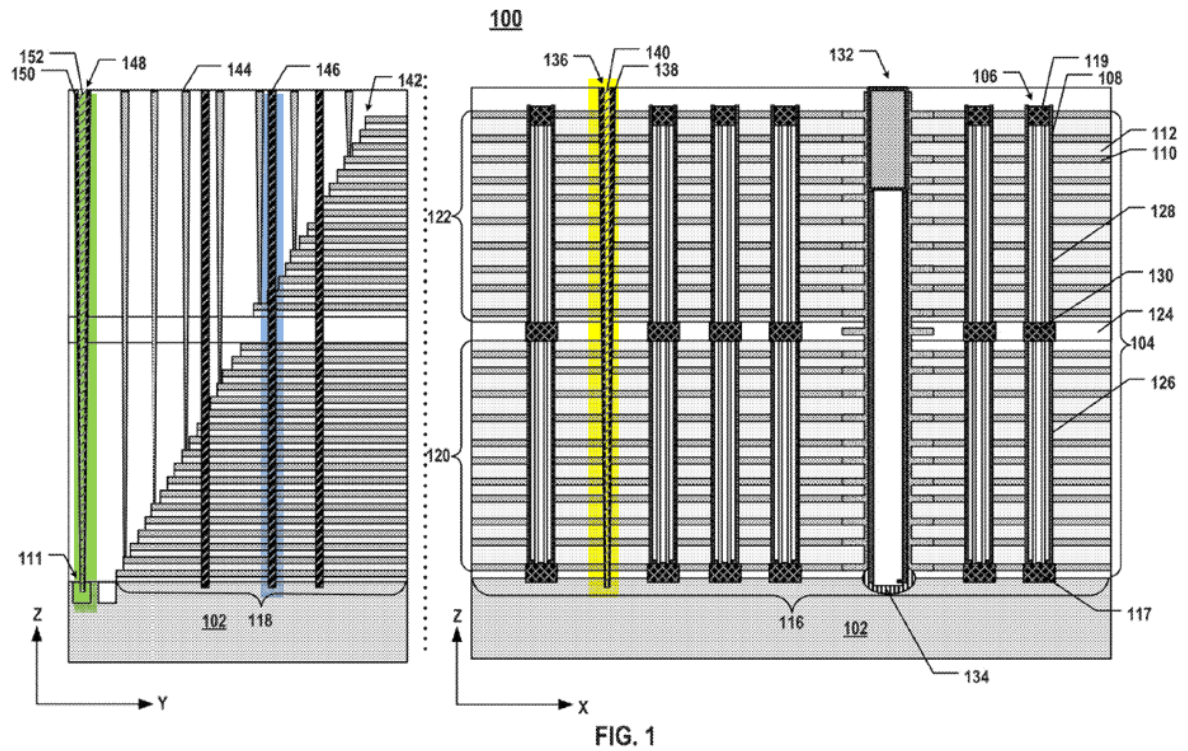


FIG. 4C

'322 Patent Fig. 4C (annotated)

44. Figure 1, reproduced below, illustrates a cross-section of an embodiment of a “memory stack 104” and a “staircase structure” 142. *Id.*, 8:63-65. As shown below in Figure 1 of the '322 Patent, the memory device 100 includes a TAC 136 (yellow) that extends vertically through the stack to carry electrical signals to/from the memory device 100. *Id.*, 8:30-46. Unlike the prior art, TAC 136 is not “enclosed by barrier structures.” *Id.*, 5:6-22. This allows the TACs to be “formed in the same fabrication process(es) for making other structures,” including those *outside* the memory array such as “peripheral contact” 148 (green). *Id.*, 5:6-22; 12:28-49. In addition, “dummy channel structures 146” (blue) are “disposed in the outer region 118 of memory stack 104 as shown in Fig. 1” to “provide mechanical support to the memory array structures, e.g., memory stack 104.” *Id.*, 9:41-51.



Id., Fig. 1 (annotated).

45. The '322 Patent also teaches TACs that may have “spacer[s]” lining the sidewalls of the TAC. '322 Patent 13:38-40. In one example, the spacers may be formed in an opening for the TAC where the opening contains a “plurality of recesses” formed by “removing parts of the sacrificial layers abutting the sidewall of the first opening.” '322 Patent 13:42-45, 14:1-5, Figs. 3D, 7B (showing a process for forming recesses). As shown below in Figure 3D, the TAC may be formed into these recesses where the sacrificial layers were removed.

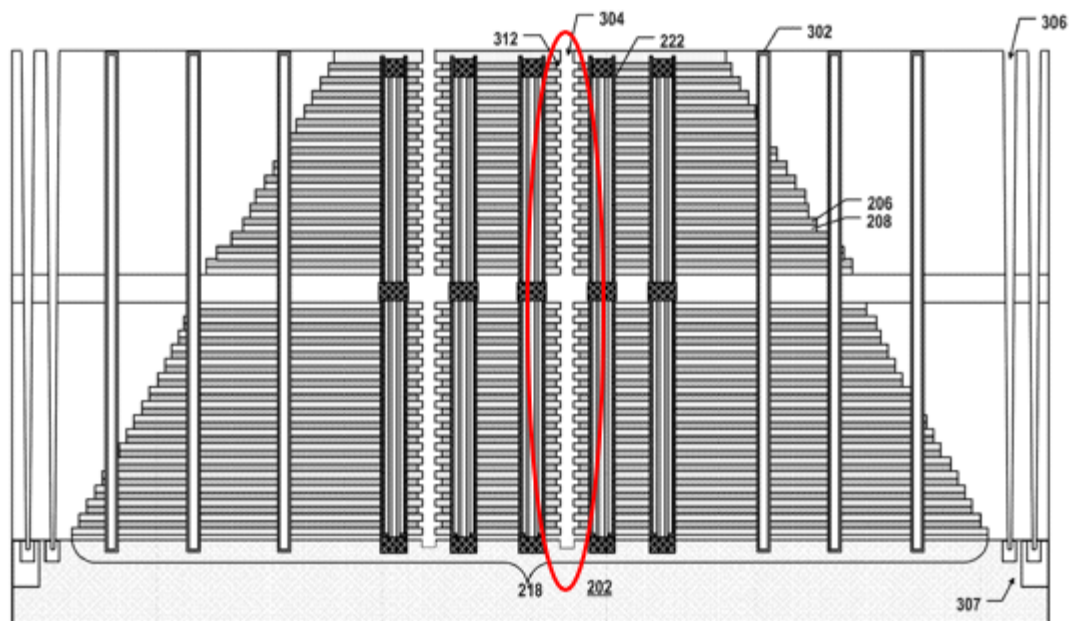


FIG. 3D

'322 Patent, Fig. 3D (annotated); *see id.* 3E.

VIII. Nishikawa and a POSITA's knowledge, alone or with Nishikawa123, do not render obvious a TAC with "a substantially circular section" (Claims 6, 8-20)

A. Petitioner fails to establish that a POSITA would have had a reasonable expectation of success or been motivated to modify Nishikawa's trench-shaped backside contact via to be a circular TAC

46. Claims 8 and 14 and claim 19 recite a TAC with "a substantially circular section" and "extending vertically through the conductor/dielectric layer pairs in the memory stack." Claim 8 adds that the TAC "compris[es] a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate." Claims 9-13 and 15-20 depend from claims 8 and 14, respectively, and thus also include this limitation.

47. Nishikawa does not disclose a TAC comprising a substantially circular section as required in claims 8, 14, and 19. Petitioner and Dr. Lee acknowledge that Nishikawa does not disclose a TAC with a substantially circular section. *See* Pet. 43, 78 ("Specifically, as that analysis demonstrates, it would have been obvious to implement Nishikawa's TAC 76 as a circular TAC (including its spacer and conductive fill therein that fills and contacts the spacer)."); Lee Decl., ¶ 180 ("Specifically, it would have been obvious to implement Nishikawa's TAC 76 as circular TAC, wherein a conformal spacer and conductive also assume circular shapes."). Petitioner argues instead only that "it would have been obvious to implement Nishikawa's structure 76 as a circular TAC," relying on a POSITA's

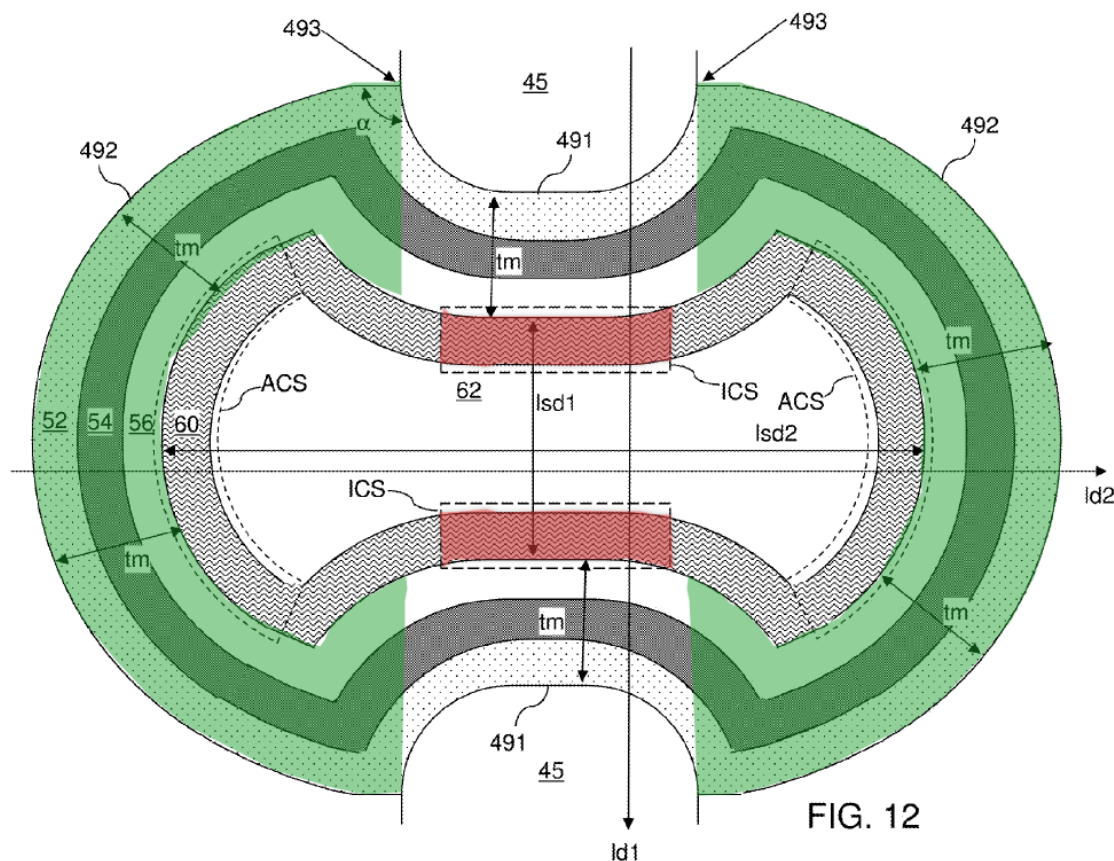
knowledge (Ground 1) and in a combination with Nishikawa123 (Ex. 1046) (Ground 3). Pet. 43-50, 78, 82-83 (Ground 1), 98-99 (Ground 3); *see* Lee Decl., ¶¶ 113-128, 180 (claim 8), 193 (claim 14), 201 (claim 19), 238 (Ground 3). Specifically, Petitioner and Dr. Lee argue it would have been obvious and that a POSITA would have been motivated (with a reasonable expectation of success) to “modify the trench-shaped common source contact (74, 76)” to “remov[e] the trench structure” and “implement Nishikawa’s TAC 76 as a circular TAC (including its spacer and conductive fill therein that fills and contacts the spacer).” Pet. 51, 78, 82, 98-99 (stating Ground 3 has “same claim mapping” as Ground 1); *see* Lee Decl., ¶ 180 (same).

48. I disagree that either ground renders this limitation obvious.

1. A circular TAC would defeat Nishikawa’s purpose and render it inoperable

49. In my opinion a POSITA would not have been motivated to modify Nishikawa to have a circular TAC because it would nullify Nishikawa’s stated purpose and render Nishikawa inoperable. Nor would a POSITA have had a reasonable expectation of success in doing so. Nishikawa’s invention is a “vertical memory device including dual memory cells per level” enabled by “separate control gate electrodes in the same horizontal device level.” Nishikawa, Abstract, 15:27-30; *see id.* 17:58-61. Nishikawa achieves this with the example arrangement described below.

50. Nishikawa's "memory stack structures" 55 include a "first portion 50A" of "the memory film (52, 54, 56)" and a "second portion 50B" of "the memory film (52, 54,56)" (green) divided by active and inactive (red) portions of the memory stack structure's "vertical semiconductor channel 60" on each side of the separator dielectric structures 45, as shown below:



Nishikawa Fig. 12 (annotated)

Nishikawa, 14:33-46, 14:60-15:2.

51. As shown below in Figure 14, the first memory cell portion 50A (yellow) is "located adjacent to" a "first control gate electrode 461," and a second

memory cell portion 50B is “located adjacent to a “second gate electrode 462” (purple). Nishikawa, 14:60-15:1.

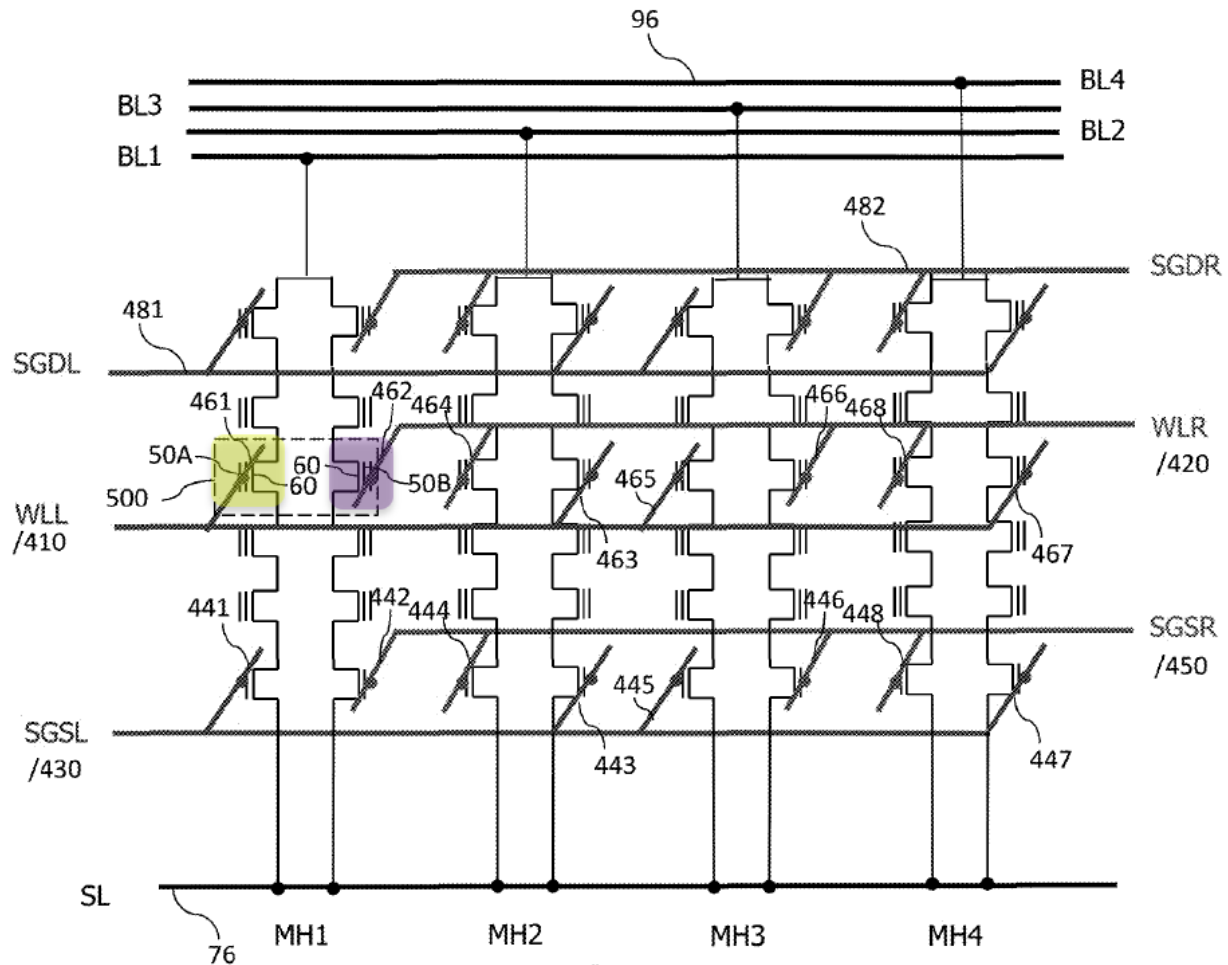
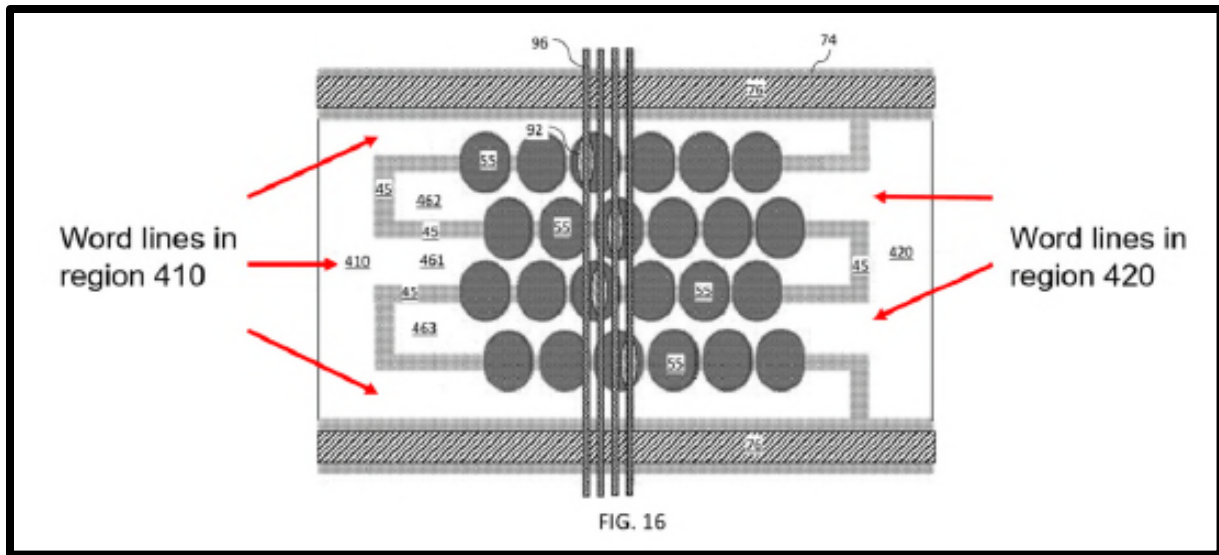


FIG. 14

Nishikawa, Fig. 14 (annotated). As a result of the memory cell portions 50A/B and the separator dielectric structure 45, the first and second gate electrodes 461/462 are “electrically insulated.” Nishikawa, 14:60-15:4.

52. Each level of control gate electrodes includes a first wordline 410 and a second wordline 420. These wordlines and corresponding gate electrodes are shown below in Petitioner’s annotation of Nishikawa’s Figure 16:



Pet. 57 (annotating Nishikawa Fig. 16)

53. The first wordline 410 is connected to a plurality of gate electrodes, for example, control gate electrode 461, that extend from the stepped contact portion into the “device region.” Nishikawa, 15:31-37. The second wordline 420 also is connected to a plurality of gate electrodes, such as control gate electrode 462. Nishikawa, 15:37-42. The wordlines 410/420 in Nishikawa are electrically isolated—i.e., enabling dual memory cells and separate control gate electrodes in the same level in each opening—by the (1) backside contact via structure 76 and its dielectric spacer lining 74 surrounding the trench structure 76; and (2) the separator dielectric structures 45. Nishikawa, Abstract, 6:57-59, 15:31-32, Fig. 16. Nishikawa discloses the dielectric spacer lining 74 “provide[s] electrical isolation for the backside contact via structure 76.” Nishikawa, 6:57-59. And the dielectric separator structures 45 “laterally separate the control gate electrodes 46” at each

level. Nishikawa, 17:16-18. Nishikawa's backside contact via structure 76 and dielectric spacer liner 74 are formed "through the alternative stack (32, 46)" and are thus surrounded by the conductive layers 46—the conductive layer forming, e.g., "the first control gate electrode 461." Nishikawa, 6:65-57, 14:60-62; *see* Pet. 39. Thus, the backside contact via structure 76 and dielectric spacer lining 74, with the separator dielectric structures 45, electrically isolate the two separate wordlines, 410 and 420, at every level of the stack, as shown below. *See* Nishikawa 17:14-23.

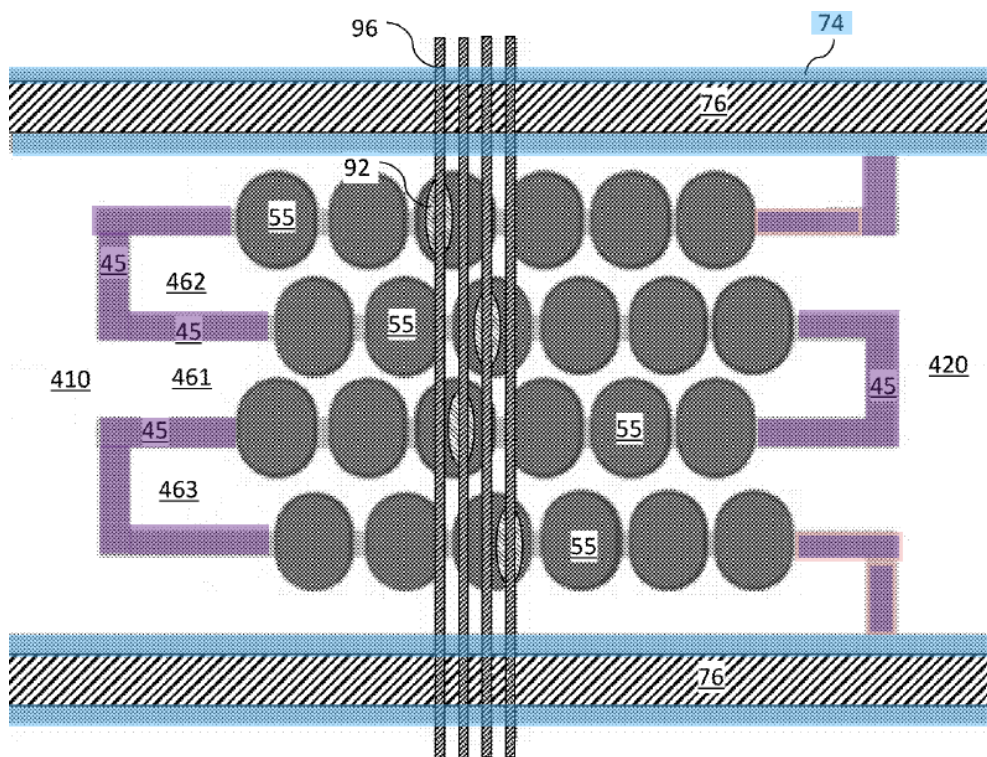


FIG. 16

Nishikawa Fig. 16 (annotated)

54. That isolation is crucial to the structure of Nishikawa's device and its purpose described above. The electrical separation allows for two wordlines at each level, WLL/410 (green) and WLR/420 (red), to be individually connected to their respective gate electrodes (461/462) and each memory region (50A/B), as shown in Figure 14, below:

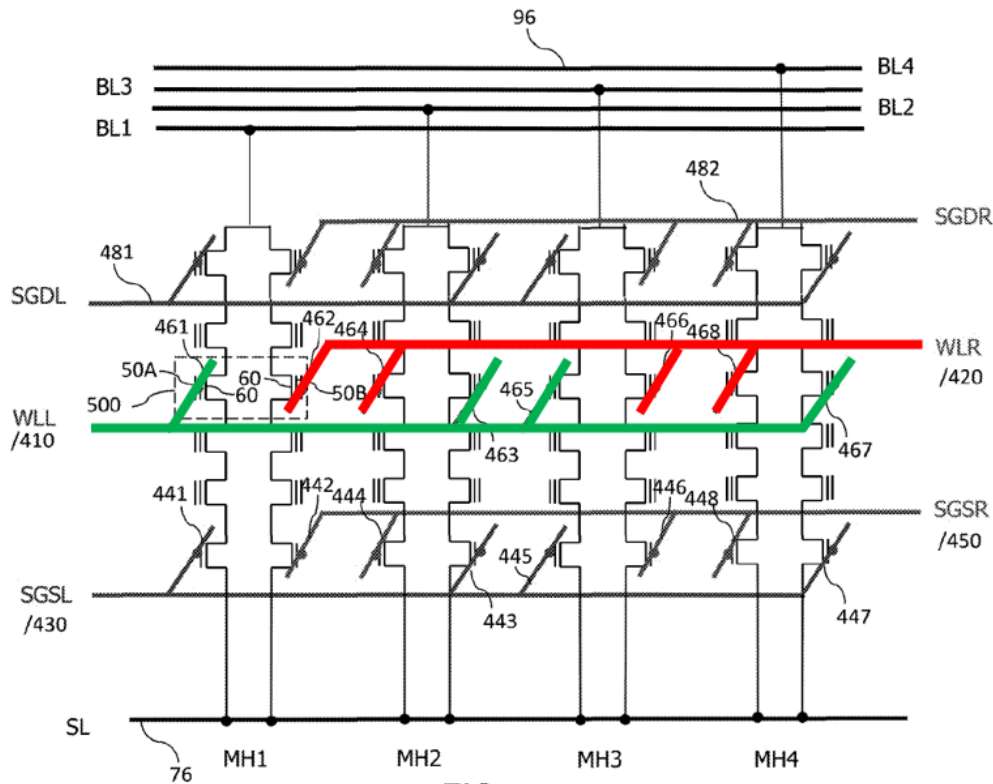


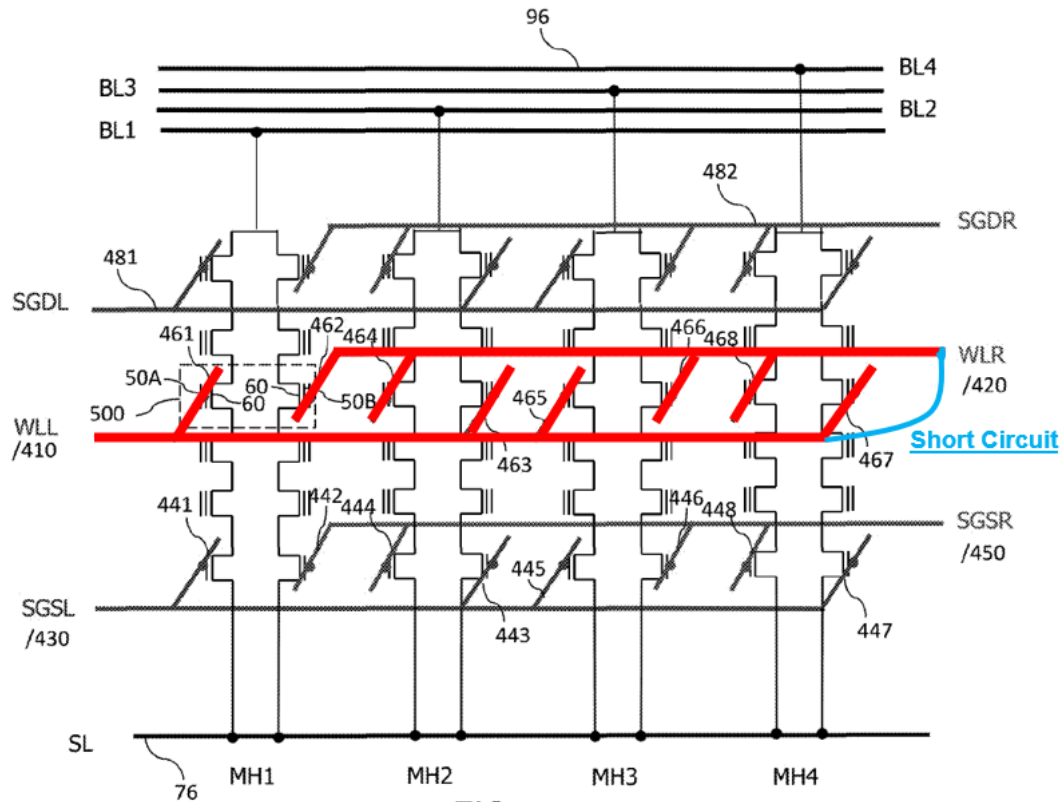
FIG. 14

Nishikawa Fig. 14 (annotated)

Nishikawa, 15:25-30, Figs. 14, 16.

55. Without this isolation the conductive path (shown below) between the WLR/420 and the WLL/410 wordlines would cause incorrect reads and writes from every memory cell in the circuit—meaning that Nishikawa's device would

not function to have dual memory cells at each level. Nishikawa, 16:13-47 (describing selectively applying voltage to each gate electrode in different wordlines for read/write operations).



Nishikawa Fig. 14 (annotated)

For example, an intended write operation using wordline WLL/410 would inadvertently overwrite data in memory cells driven by wordline WLR/420 if the separate wordlines are short-circuited. *See id.*

56. Petitioner argues a POSITA would have been motivated to modify Nishikawa to remove its trench structure and implement a circular TAC and spacer that, in my opinion, would nullify Nishikawa's primary function and render it

inoperable for the reasons I discuss above. *See* Pet. 51, 78, 82, 98-99; Lee Decl., ¶ 180 (same). Modifying Nishikawa's trench-shaped backside contact via structure 76/spacer lining 74 to be circular would cause an isolation gap between the circular backside contact via structure 76 and the separator dielectric structure 45, electrically connecting the conductive layers 46—i.e., the two wordlines 410/420 and their respective gate electrodes (e.g., 461/462) and memory regions at each level. Petitioner's proposed modification is shown below:

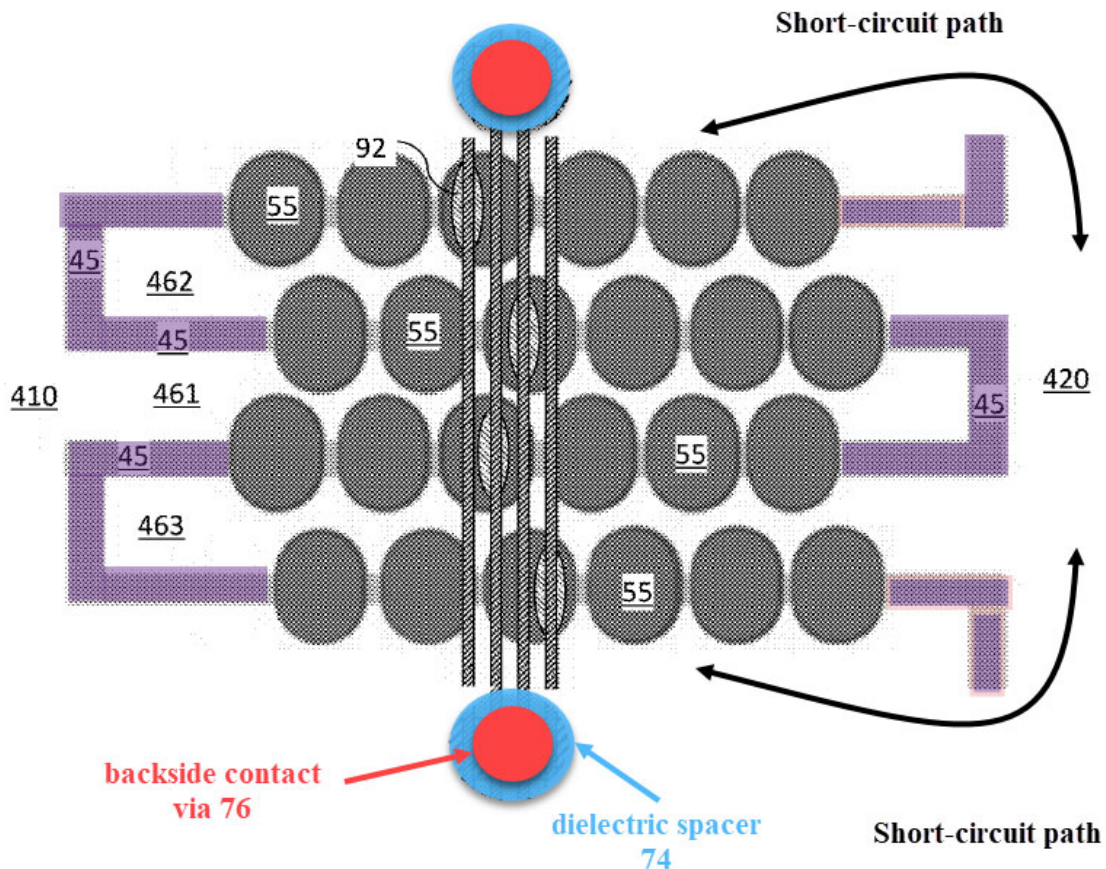


FIG. 16

Nishikawa Fig. 16 (annotated)

57. And Petitioner's modification eliminating the electrical isolation would defeat the purpose of Nishikawa's device—having dual memory cells with separate gate electrodes in each memory opening—because it would create a short circuit between the wordlines at every level. Nishikawa, Abstract. As I describe above, Nishikawa discloses its backside contact via 76 and dielectric spacer liner 74 are formed through the conductive layer 46 forming the separated gate electrodes (e.g., 461, 462, 463) and, as a result, the space in the short-circuit path indicated above is the conductive material creating a conductive path between the wordlines 410/420. *See* Pet. 39 (describing Nishikawa's TAC extending through conductor layers 46). And a voltage applied to one wordline (and thus the gate electrodes) would be applied to the other. Nishikawa, 16:13-47 (describing selectively applying voltage to each gate electrode in different wordlines).

58. A POSITA would have recognized that modifying Nishikawa's trench-shaped cavity containing both the backside contact via 76 and the dielectric liner 74 to be circular as Petitioner proposes would have eliminated the physical contact between the dielectric liner 74 and the dielectric separator structures 45, as exists in Nishikawa's Figure 16 below:

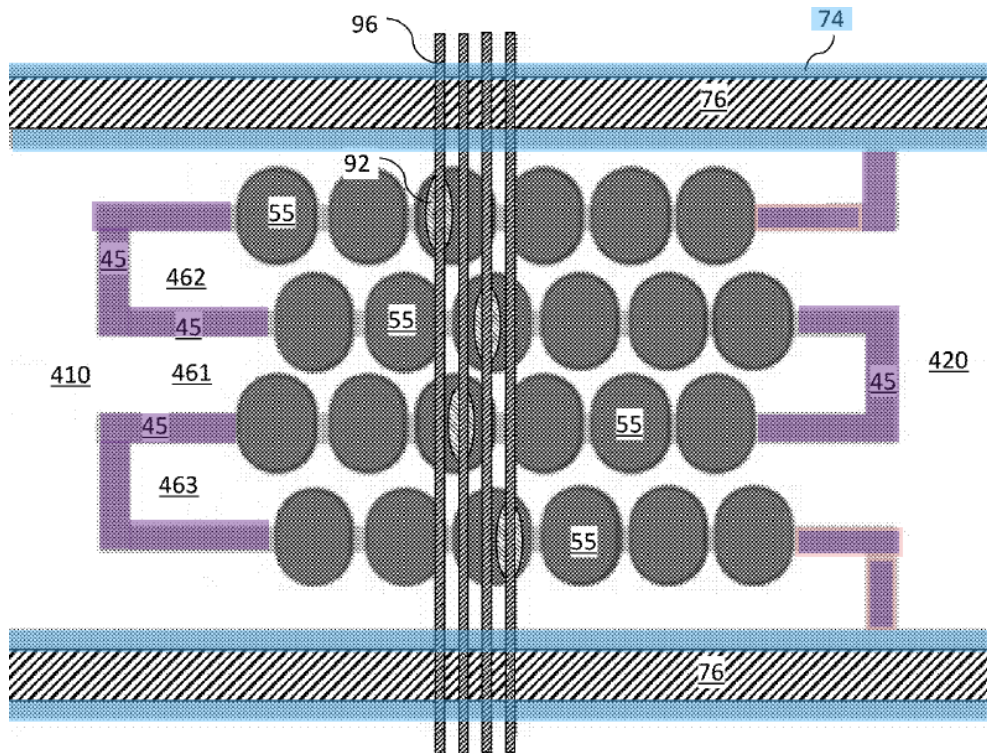


FIG. 16

Nishikawa Fig. 16 (annotated)

Figure 16 teaches that the dielectric spacer lining 74 surrounds all sides of the trench-shaped backside contact via structure 76, and the dielectric separator structures 45 terminate where they meet the dielectric spacer lining. A POSITA would have understood Nishikawa's disclosure that the dielectric separator structures 45 "laterally separate the control gate electrodes 46," e.g., first gate electrode 461 and second gate electrode 462, to mean that the dielectric separator structures 45 serve the purpose of defining the boundary between the gate electrodes and providing electrical isolation in conjunction with the dielectric liner

74 surrounding the trench-shaped via contact 76. *See* Nishikawa, 15:31-32, 17:14-23.

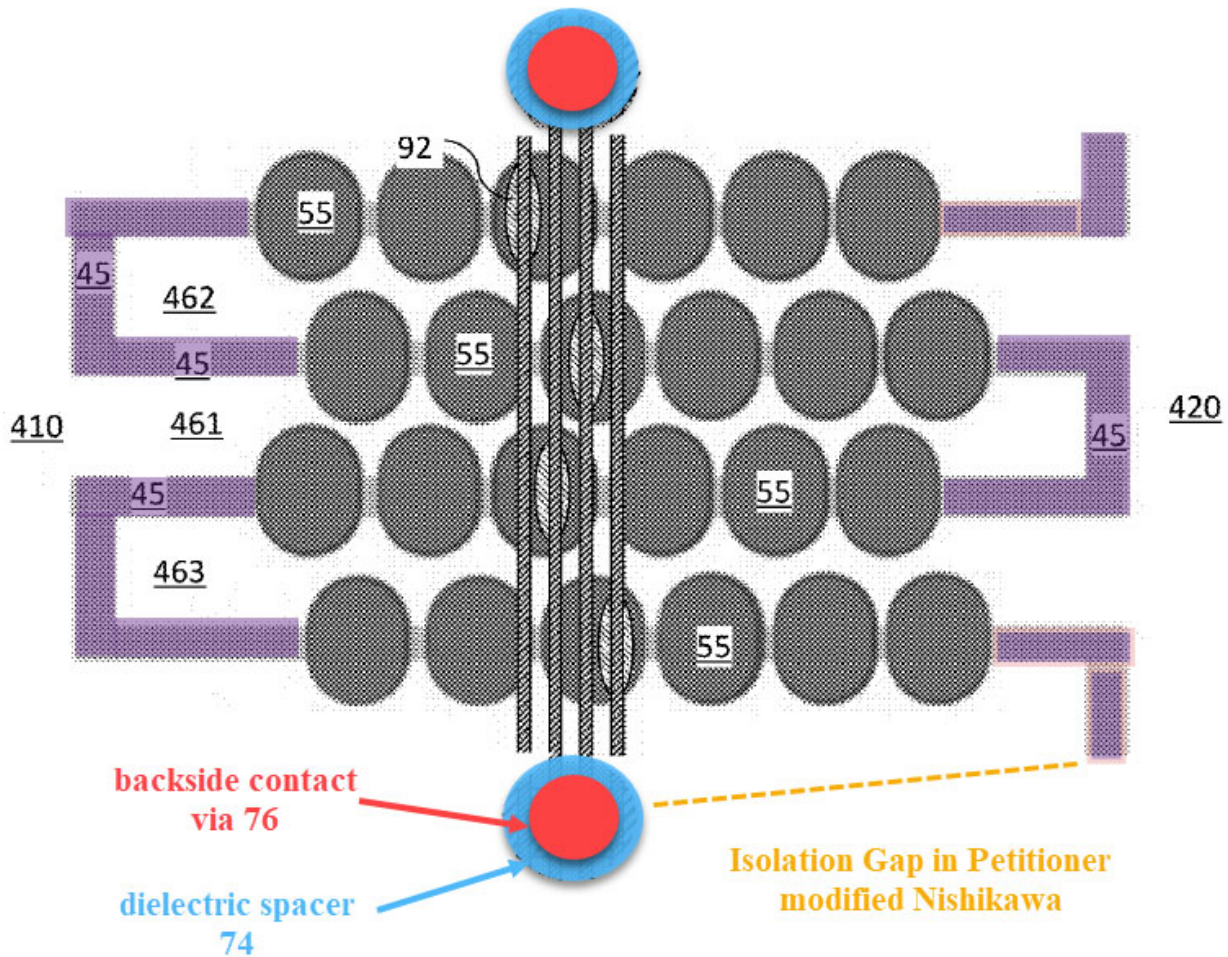


FIG. 16

Nishikawa Fig. 16 (annotated)

59. A POSITA would have understood that in Petitioner's proposed modification, it would have been necessary to modify Nishikawa's separator dielectric structures 45 to maintain electric isolation between each wordline in the

same level. Neither the Petition nor Dr. Lee proposes such a modification. *See* Pet. 39-53, 78, 98-88; Lee Decl., ¶¶ 113-128, 180, 238-240.

60. Even if a circular TAC was physically connected at the end of the separator dielectric structure 45 to cure isolation deficiencies, such a configuration is not suitable. For example, the TAC's diameter would have to be large enough to contact the side of the device to maintain the isolation, which would require a larger footprint than a rectangular trench, as shown below (red circle):

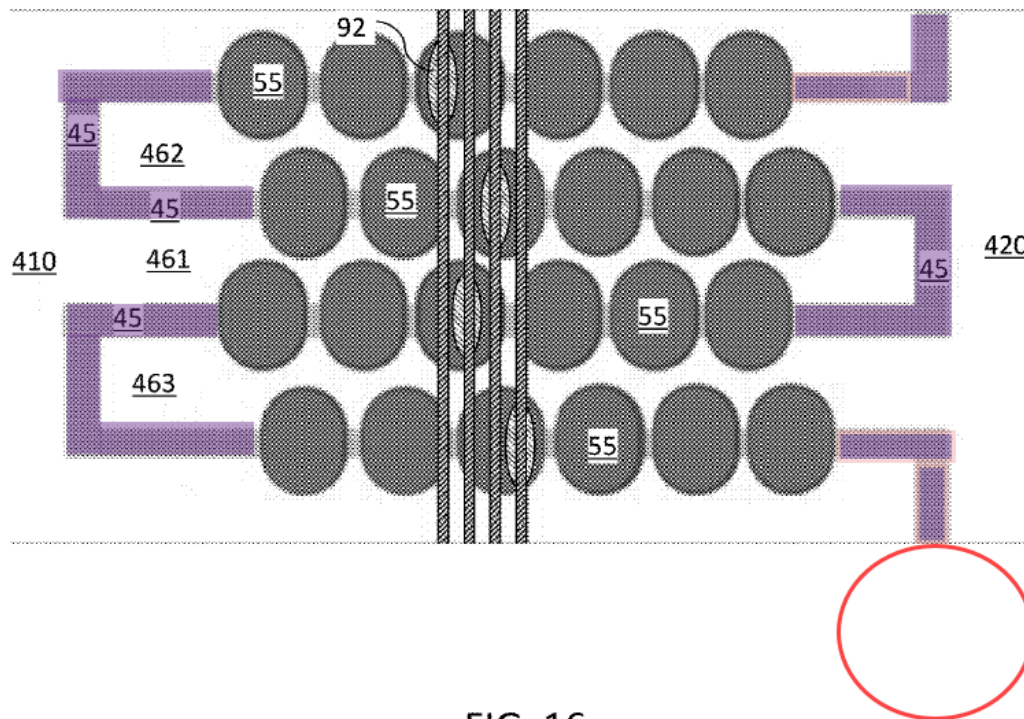


FIG. 16

Nishikawa Fig. 16 (annotated)

61. Dr. Lee correctly admits that a POSITA would not have desired an increased footprint. Lee Decl., ¶ 123; *see* Pet. 51, 99. Nor would a POSITA have replaced Nishikawa's trench-shape structure with contiguous, physically

connected circular TACs for several reasons. Doing so would push the limits of manufacturing tolerances leading to defects, such as short circuiting between densely-packed TACs. Placing TACs with dielectric liners so close that they are in contact increases the risk that etching variations cause a short circuit between the contacts, introducing mechanical stress leading to cracks in the TAC. Forming such densely-packed contact holes introduces challenges with the resolution limits of the lithography equipment—even minor variations would cause the contacts to be out of specification and could lead to the holes having tilting, non-uniform bottom and sidewalls, or failure to etch to the intended depth. Further, this channel non-uniformity would create problems with filling the hole with a contact conductor, such as voids that introduce increased contact resistance and open circuits.

62. And such densely packed TACs push the limits of physics because of parasitic capacitance—an undesired but unavoidable feature when conductive materials are in close proximity and separated by nonconductive materials—which would affect device performance.

63. Further, even though neither Petitioner nor Dr. Lee proposes modifying Nishikawa's trench structure so that it contains a circular contact via structure 76 and/or a dielectric liner 74 surrounded by a trench-shaped dielectric material to preserve electrical isolation, that modification would lack a TAC

“extending vertically through the conductor/dielectric layer pairs in the memory stack.” ’322 Patent, cls. 8, 14, 19. Instead, the TAC would extend through the dielectric material, not the memory stack.

64. Thus, it is my opinion that Petitioner’s modification would nullify the key purpose of Nishikawa’s device and cause a short-circuiting problem in Nishikawa, dissuading a POSITA from making such a combination. For the same reasons, a POSITA would not have had a reasonable expectation of success in modifying Nishikawa as Petitioner proposes.

2. A POSITA would not have been motivated to combine Nishikawa and Nishikawa123 or have had a reasonable expectation of successfully doing so

65. Petitioner asserts in Ground 3 that a POSITA would have been motivated to combine Nishikawa and Nishikawa123 because they “present the same memory architecture and key components.” Pet. 99 (citing *id.*, 27-32 (Description of Prior Art)). Petitioner asserts that both Nishikawa and Nishikawa123 disclose TACs, and that Nishikawa123 teaches that the “openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape.” Pet. 31 (citing Nishikawa123, 22:38-41, Fig. 17; Nishikawa, Fig. 16), 98-99. Petitioner further argues the memory architecture of Nishikawa123’s Figure 17 and Nishikawa’s Figure 16 are the “same.” Pet. 31, 99. In my opinion, a POSITA

would not have been motivated to apply Nishikawa123's teachings that its opening 79 can have any suitable shape, such as circular, to Nishikawa.

66. A POSITA would have understood that Nishikawa123's disclosure that the "openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape" does **not** apply to Nishikawa123's Figure 17, which, like Nishikawa Figure 16, teaches separate, electrically isolated wordlines connected to separate gate electrodes forming dual memory cells at each level. That is because Nishikawa123's Figure 17 depicts a specific embodiment adding an optional first "comb shaped word line 46A" and a second "comb shaped word line 46B," where each comb shaped wordline is connected control gate electrodes (e.g., 461/464 and 462/463), as shown below:

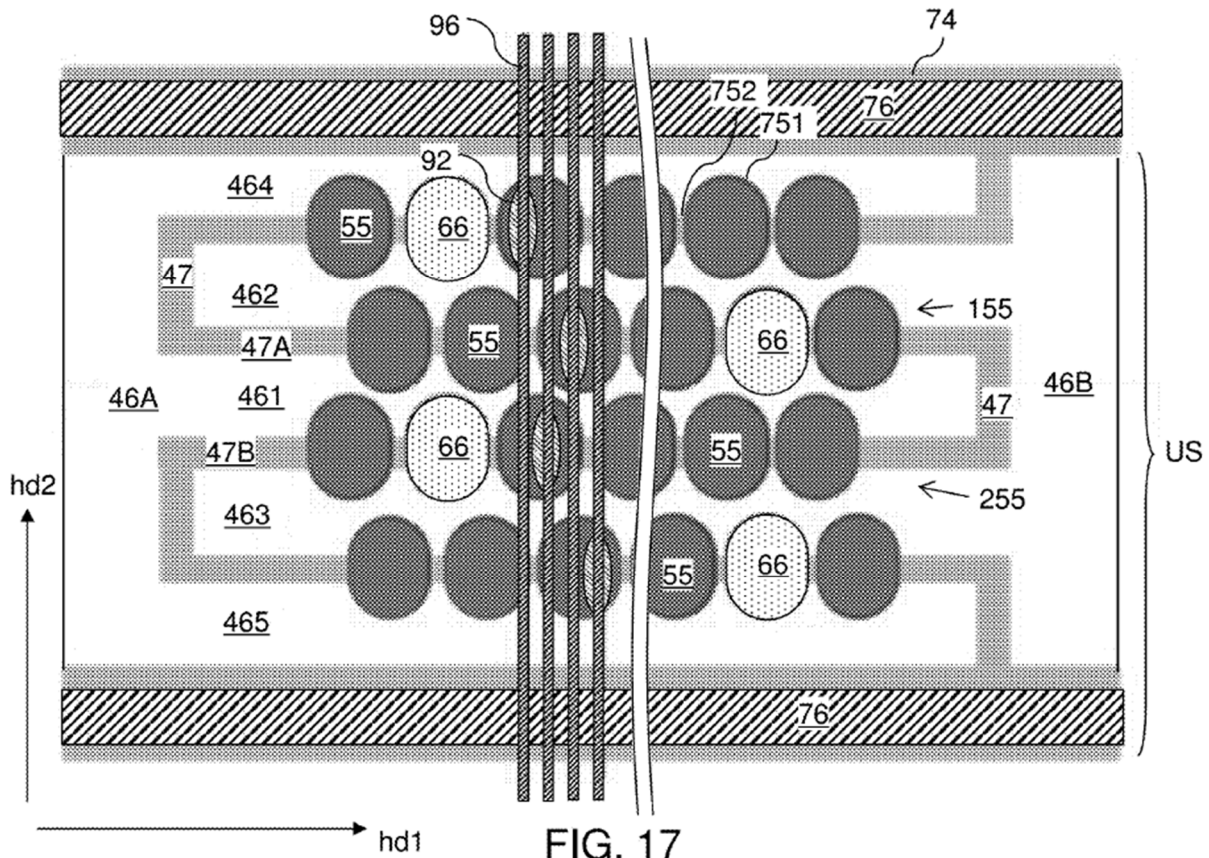


FIG. 17

Nishikawa123, 25:32-35, Fig. 17. For the reasons discussed above regarding Nishikawa's isolated wordline structures, these additional elements in Nishikawa123's Figure 17 require a trench-shaped opening 79 (and thus a backside contact via structure 76 and dielectric liner 74). Thus, a POSITA would have understood that Nishikawa123's disclosure that the opening 79 could be "any *suitable* shape," including a circular one, does not apply to Nishikawa123's Figure 17's embodiment for the reasons discussed above regarding Nishikawa.

67. Moreover, a POSITA would have recognized that Figure 17, like Nishikawa 16, explicitly teaches a trench-shaped backside contact via 76 and a

dielectric liner 74. Figure 17's embodiment may have the separated comb shaped wordlines 46A/B, where the backside contact via 76 is trench-shaped and provides the necessary electrical isolation: "Each electrically conductive layer 46 (i.e., each of the word-line-level electrically conductive layers 46) formed within the alternating stack (32, 46) includes two physically disjointed portions (46A, 46B) between each optional neighboring pair of backside trenches (which are filled with the insulating spacers 74 and the backside contact structures 76)." Nishikawa123, 25:39-49. Nishikawa's Figure 16 also shows trench-shaped backside contact vias 76 and electrically isolated wordlines at the same level provided by the trench-shaped structure disclosed in Nishikawa123. *Compare* Nishikawa, Fig. 16, *with* Nishikawa123, Fig. 17.

68. In sum, it is my opinion that, based on Nishikawa and Nishikawa123's separate teachings as a whole (each with distinct teachings), a POSITA would not have been motivated by Nishikawa123's disclosures, including its teaching regarding the "suitable shape" for an opening that Petitioner relies on as disclosing a circular TAC, to modify Nishikawa to have a circular TAC and corresponding dielectric liner. That combination would defeat Nishikawa's purpose of creating a memory device with dual memory cells per level and render it inoperable—two things a POSITA would not desire. Also for those reasons, a POSITA would not

have a reasonable expectation of success in modifying Nishikawa as Petitioner proposes.

3. A POSITA would not have been motivated by other purported benefits

69. Petitioner and Dr. Lee also argue a POSITA would have been motivated to modify Nishikawa's trench-shaped TAC because other references disclose a circular TAC as generally an option, a circular TAC "can increase memory capacity by removing the trench structure" and to "spread out source contacts." Pet. 43-52, 99; Lee Decl., ¶¶ 116-120, 123-127, 240. In my opinion, a POSITA would not have been motivated for those reasons because, as I describe above, a circular TAC would defeat the purpose of Nishikawa's device and render it inoperable, a tradeoff a POSITA would not have made. Also for those reasons, a POSITA would not have a reasonable expectation of success in modifying Nishikawa as Petitioner proposes.

B. 3D NAND is complex technology.

70. A POSITA would understand that 3D NAND technology—the technology relevant to the '322 Patent—including manufacturing relevant components, is not particularly straightforward. Instead, a POSITA would understand that 3D NAND is described as "**very complex**" and includes "complex device structures" and equally complex fabrication processes required to produce 3D NAND devices. Ex. 1010, 293; Ex. 2023, 3; Ex. 1010, 212 ("3D NAND

architectures need to be proven cost effective in terms of process costs and product yield because the process complexity is not trivial if compared to 2D NAND.”); Ex. 2023, 4 (“[T]he overall complexity and capital intensity of 3D NAND manufacturing add significantly to the challenges fabs are facing in terms of process control, yield, and economics.”); *see also* Ex. 2024, 5 (“With each generation, the fabrication of 3D NAND becomes more complex.”); ‘322 Patent, 5:2-5 (describing the link between device design and manufacturing difficulties); Lee Dep. (Ex 2038) 22:18-24:14 (agreeing “fabrication processes” and “design” are constraints on memory density”).

71. In my opinion, a POSITA would also understand that the design and fabrication of 3D NAND “involves a number of new and ***complex process steps***.” Ex. 2025, 4; Ex. 2026, 8 (describing removal of nitride layers and forming a wordline as a “complex process”); Ex. 2023, 4-5 (recognizing “[a]n incredible level of precision and repetition is required in defining complex 3D structures with extremely high aspect ratio (HAR) features,” including “alternating film deposition” and formation of “staircase,” “wordline,” “contact,” and “channel” features), Fig. 1; Ex. 2027, 1 (3D NAND has led to complex deposition and etch “with angstrom-level requirements for precision”); Ex. 2028, 8 (describing removal of nitride layers and forming a wordline as a “complex process”); *see also id.*, 3 (“[M]aking 3D NAND is a complex process” that requires “using a

deposition tool” to deposit layers of material on a substrate); *id.*, 2 (“The big challenge is to characterize the inner portions of a 3D NAND device, which consists of complex materials, multiple layers and tiny channel holes.”); Ex. 2029, 5 (“3D NAND is a complex technology”); *id.*, 5 (“In all cases, the 3D NAND process flow is complex.”).

72. Thus, 3D NAND structures, like the '322 Patent, involve concepts of chemical, mechanical, and electrical engineering on a microscopic scale and are not particularly straightforward technology. That 3D NAND structures are not particularly straightforward technology is applicable to all claim limitation I discuss herein.

C. The recited “substantially circular” TAC is not “unusually simple”

73. Designing and fabricating a 3D NAND device to include a substantially circular TAC, including changing the shape of a TAC, is complex, not unusually simple. Dr. Lee ignored that changing the shape of the TAC requires creating a new mask for lithography, which is far from a simple process. *See* Lee Decl., ¶ 128 (omitting discussion of the mask making process when discussing etching). And changing the mask to create circular features (i.e., change the shape of the TAC) requires time consuming, specialized processes, which are complicated when forming circular as opposed to angular features.

74. The forming of circular features itself is also not simple. A circular TAC, which would have a higher aspect ratio than Nishikawa's trench-shaped TAC, is complex because it is hard to maintain a continuous etch rate. When forming cylindrical channels for a TAC, unwanted variations can occur, such as bowing or twisting within the TAC, an incomplete etch, or variation between the top and bottom of the TAC. Bowing and twisting are particular problems since the etch may miss the position of the bottom contact leaving an open circuit.

75. It is increasingly complex to achieve consistent etch profiles at the top and bottom of the holes in a memory array as the height of 3D NAND increases. And the choice of material for both the target and non-target layers must be highly compatible with the selective etch chemistry because any incompatibility could lead to non-uniform etching, structural defects, or failure to form the intended structure.

76. In addition, as Dr. Lee correctly admitted, changing the shape of the TAC openings—which would increase the aspect ratio of the TAC—would introduce higher risks of undesirable tapering in the channel hole. Lee Dep., 25:9-17, 29:17-30:1, 30:13-31:3. Tapering leads to defects, such as inconsistent channel depth and defective TACs causing short circuits. Thus, forming and designing TACs with a substantially circular section is not “unusually simple,” especially as compared to other geometries such as trenches.

IX. Nishikawa and a POSITA's knowledge, alone or with Nishikawa123, do not render obvious a "dummy channel structure ... extending vertically through the conductor/dielectric layer pairs in the memory stack" (claims 3, 6, 14-18, 20)

A. A POSITA would not have been motivated or have had a reasonable expectation of success to add dummy channels to Nishikawa's memory stack

77. Claim 3 recites "a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack." '322 Patent, cl. 3. Claims 6 and 14 recite the same limitation. *Id.*, cls. 6, 14. Claims 15-18 and 20 depend from claim 14. *Id.*, cls. 15-18, 20.

78. Dr. Lee opines that a "POSITA would have been motivated, with a reasonable expectation of success, to include dummy channels ... in Nishikawa's memory stack for several reasons," namely processing and structural reasons. Lee Dec., ¶ 140. He does not opine that Nishikawa discloses a dummy channel structure. *Id.* As Dr. Lee admitted in deposition, "Nishikawa Exhibit 1005 does not explicitly or expressly disclose dummy channel structure." Lee Dep., 44:1-3. Instead, Dr. Lee asserts that the use dummy channels was known to a POSITA (Lee Decl., ¶¶ 141-144) and disclosed in other patent literature (*id.* ¶¶ 144-147). As the Board recognized, Petitioner asserts that Nishikawa discloses forming channel structures, i.e., memory stack structures 55, but does not assert that Nishikawa discloses dummy channel structures. ID, 18; *see* Pet. 59, 82.

79. The Petition also does not cite to any passage of Nishikawa as disclosing a dummy channel structure. Pet. 59-64. Rather, the Petition states that “in view of the knowledge of a POSITA, a POSITA would have been motivated, with a reasonable expectation of success, to include dummy channels ... in Nishikawa’s memory stack.” Pet. 59.

80. Based on the above, I understand the Petition to be proposing a modification of Nishikawa to “include dummy channels ... in Nishikawa’s memory stack” based on the supposed “knowledge of a POSITA.” Pet. 59.

81. In my opinion, the Petition’s and Dr. Lee’s reasons for why a POSITA would have modified Nishikawa to include dummy channels in the memory stack fail—they would not have motivated a POSITA to do so or have had a reasonable expectation of success in doing so.

1. Nishikawa’s separator dielectric structures already provide structural support, rendering dummy channels redundant

82. Petitioner asserts that a POSITA would have been motivated to add dummy channels to Nishikawa to provide structural support during “the gate replacement process.” *Cf. id.* 63. And Dr. Lee asserts that “[i]f using the gate replacement process with Nishikawa, additional motivations exist. Dummy channels provide structural support, which is important during the gate line replacement process.... As a result, ‘support pillars’ are necessary to support the stack during this process.” Lee Decl., ¶ 143 (quoting Ex. 1030 5:64-6:2, 7:19-23).

In my opinion, a POSITA would not have been motivated to include dummy channels in Nishikawa's memory stack because Nishikawa's device already has structural support.

83. Specifically, Nishikawa teaches its memory stack includes “separator dielectric structures 45” that “provide structural support to the insulating layers 32 after formation of the interlayer cavities 43,” i.e., gate replacement. Nishikawa 10:10-12. Neither the Petition nor Dr. Lee address Nishikawa's structural support provided by the separator dielectric structures. Pet. 59-64; Lee Decl., ¶¶ 140-148; *see* ID, 19-20 (“We agree with Patent Owner that Petitioner does not address the support provided by [the separator dielectric structures 45] in Nishikawa, which is for the same purpose as Petitioner's added dummy channels; i.e., to support recesses caused by loss of sacrificial material during the gate replacement process.”).

84. Nishikawa teaches its dielectric separator structures 45 provide structural support during the gate replacement process. The gate replacement process in Nishikawa involves removing the “sacrificial material layers 42” are removed, resulting in the interlayer cavities (i.e., “recess 43”). ‘322 Patent, 9:58-61, 10:8-10. The recesses are then filled with metal conductor layers (i.e., gates). Nishikawa, 10:18-27, Figs. 8A-8C. As shown below in Nishikawa's annotated Figures 6B (before gate replacement) and 7B (during gate replacement), Nishikawa

discloses forming its recess 43 (yellow) created in the space where the “sacrificial material layers 42” (green) were prior to removal. Nishikawa, 9:25-29, 9:58-61, 10:8-10.

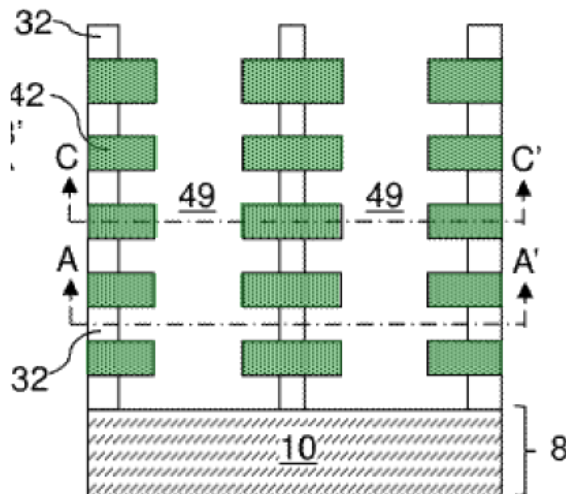


FIG. 6B

Before Gate Replacement

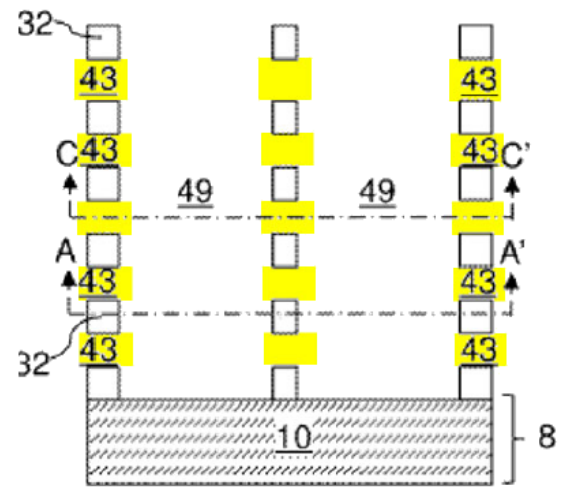
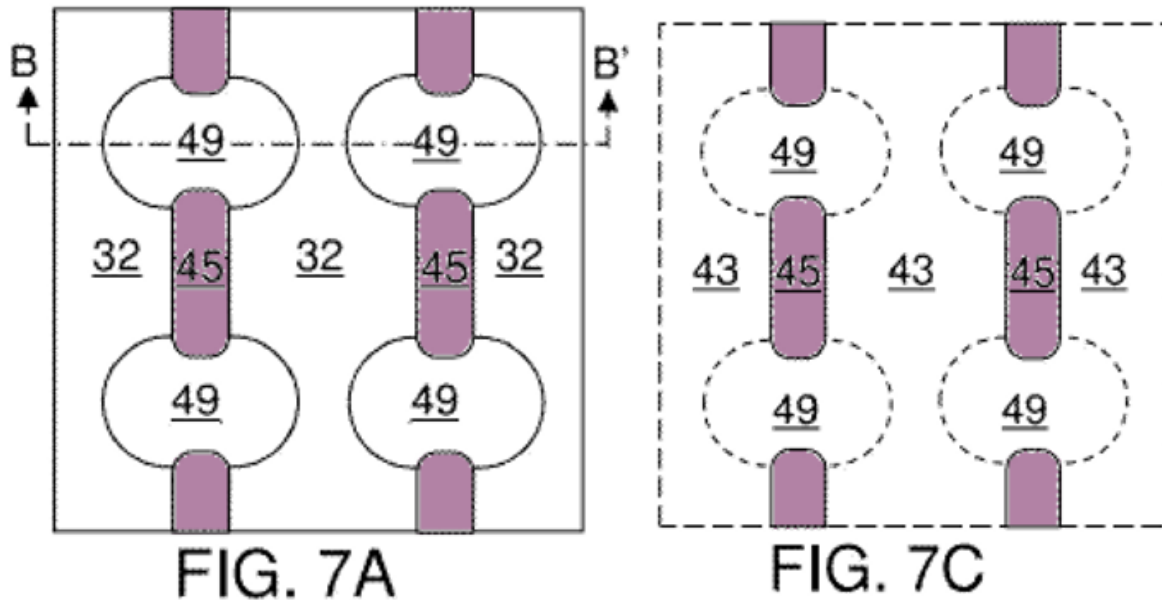


FIG. 7B

During Gate Replacement

Id. Fig. 6B, 7B (annotated).

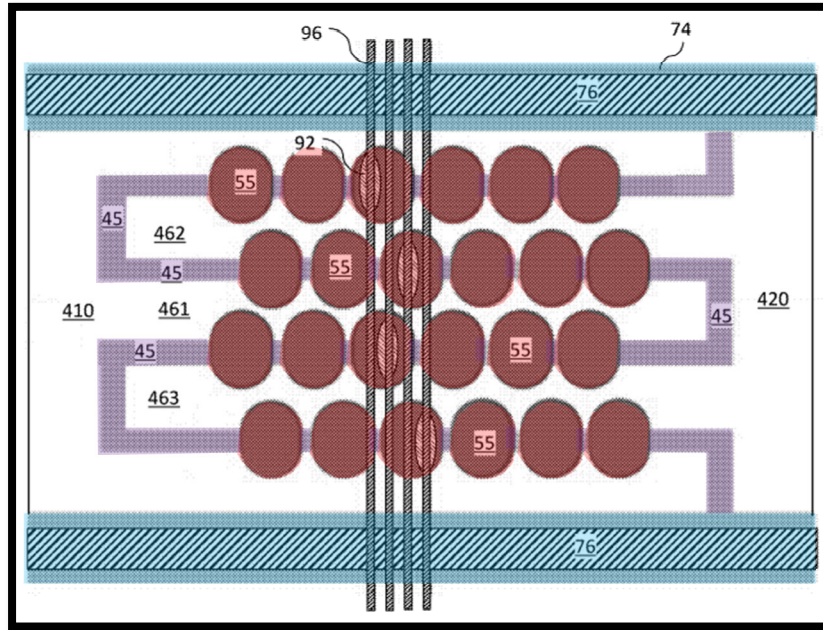
85. Nishikawa's annotated Figures 7A and 7C below are top-views of the device shown above in Figures 6B and 7B before and after the removal of the sacrificial layers 42. Nishikawa, 2:37-45.



86. Nishikawa, Figs. 7A, 7C (annotated). These figures demonstrate the separator dielectric structures 45 (purple) “provid[ing] structural support to the insulating layers 32 after formation of the interlayer cavities 43.” Nishikawa, 10:10-12. These figures show the separator dielectric structures 45 connecting to the insulating layers 32 (Fig. 7A) to provide structural support and maintain the recesses 43 (Fig. 7C). If they did not, the insulating layers 32 would collapse into the recesses 43 below and the Figure 7B structure above could not exist.

87. As shown in Figure 16, below, the separator dielectric structures 45 (purple) in the final memory device are disposed throughout the device and are therefore able to provide sufficient structural support during the gate replacement process. *See* Nishikawa, 17:14-18 (“The separator dielectric structures 45 extend through the stack, contact portions of outer sidewalls of the memory stack

structures 55, and laterally separate the control gate electrodes 46 of the plurality of charge storage elements.”).



Ex. 1005, Fig. 16. Thus, Nishikawa’s dielectric separators 45 provide structural support during the gate replacement process.

88. Dr. Lee does not assert any need for additional support during gate replacement, and does not assert that the separator dielectric structures are unable to provide sufficient structural support (which would be contrary to Nishikawa’s explicit disclosure). *See* Lee Decl., ¶¶ 140-148. Thus, a POSITA would have understood there is no need for dummy channels in Nishikawa, as they would serve no purpose. A POSITA would not have been motivated to add dummy channels that are redundant because they serve no additional support purpose.

89. Dr. Lee also opines that “[t]he dummy channels, however, typically will not include interconnects to upper-level elements, because the structures do not store data. Thus, dummy channels do not consume space above the structures, but still function as support members.” Lee Decl., ¶ 147. Dr. Lee is wrong because a POSITA would not be motivated by the fact that dummy channels do not consume space above the structures for the purpose of acting as support structures because, for the same reason stated above, Nishikawa already contains structural support. Further, regardless of whether the dummy channels consume space above the structures, they would still occupy space in Nishikawa’s memory stack, reducing memory density, as described below.

2. Adding dummy channels does not have processing benefits

90. Petitioner also asserts that a POSITA would have been motivated to add dummy channels for “processing reasons.” Pet. 59. It is my opinion that none of Petitioner’s processing-related benefits would have motivated a POSITA to add dummy channel structures to Nishikawa.

91. **First**, Petitioner argues a POSITA would have been motivated to add dummy channels in Nishikawa’s memory stack to “reduce the likelihood of defective bits on the edge of the memory cell region, because the additional rows of dummy channel structures extend the memory cell pattern to include the dummy region on the edges.” Pet. 59 (citing Lee Decl., ¶ 41, Ex. 1024, 8:47-53, Ex. 1025,

2:20-43, Ex. 1026, 11). Dr. Lee similarly opines that the “one normally employs dummy channel structures at the edge of the array. Otherwise, these channel structures may be defective, and not properly store data.” Lee Decl., ¶ 141.

92. Neither Petitioner nor Dr. Lee argues that Nishikawa’s device would suffer from “defective bits,” on the edge of the memory cell region or otherwise. *See* Pet. 59-60; Lee Decl., ¶ 141. Dr. Lee relies on two references to support his opinion a POSITA would have been motivated to include dummy channels in Nishikawa to reduce the risk of defects. Lee Decl., ¶ 141. But the references Dr. Lee relies on do not support that “edge of the array” issues are a concern in 3D NAND, let alone Nishikawa, or that adding dummy channels would resolve such issues. *See, e.g.*, Ex. 1024, 8:47-53 (patent filed in 1998 referring to a “typical flash cell array” at that time, not 3D NAND); Ex. 1025, 2:20-43 (indicating edge of array issues “*may* typically occur at the boundary ... an abnormal edge pattern at the edge of array *may* be controlled by adding a dummy pattern region”); Ex. 2025, 3-4 (discussing 3D NAND technology being “introduced in 2007” and commercialized in 2013). Dr. Lee attests that “it is common to refrain from using the cells at the array edge,” which are “sometimes referred to as dummy cells,” due to “processing variations.” Lee Decl., ¶ 141 (citing Ex. 1024). But Refraining from placing cells at the array edge does not show an advantage to *adding* dummy

channels that would have motivated a POSITA to add them to Nishikawa, especially where Nishikawa already has structural support as described above.

93. Moreover, Dr. Lee recognized that any dummy regions existing at the edge of the array would be “later sacrificed in processing.” Lee Decl., ¶ 141 (citing Ex. 1025, 2:20-43). For dummy channels formed at the edge of the array, a POSITA would not have added a “dummy channel structure” only to have it later sacrificed during processing. *See* ‘322 Patent, cl. 3. And a device with dummy structures added but later sacrificed in processing would not provide any additional support, as Petitioner asserts would have motivated a POSITA to include dummy channels in Nishikawa. *See* Pet. 63 (citing e.g., Ex. 1027, 16:28-38, Fig. 6A).

94. Petitioners cited references do not support that a POSITA would have added additional rows of dummy channels to extend the memory cell pattern. Petitioner cites nothing in Kai, Kim, Park297, or anything else that teaches “additional rows” that “extend the memory cell pattern.” Pet. 59. To the contrary, as discussed below, those references do not disclose dummy structures in the memory cell area at all. *See infra* Section IV.B. In fact, Kim and Park disclose that the dummy channels ***should not*** be within the memory cell array. Kim (Ex. 1029) [0047]; Park297 (Ex. 1028) Fig. 1, 7:38-42; *see* Pet. 62 (citing Park297, 7:45-51 as disclosing dummy channels). Petitioner also ignores that adding “additional rows” in the “memory cell pattern” will increase device size and reduce memory

density, which a POSITA would understand is not desirable. *See infra* Section IX.A.3.

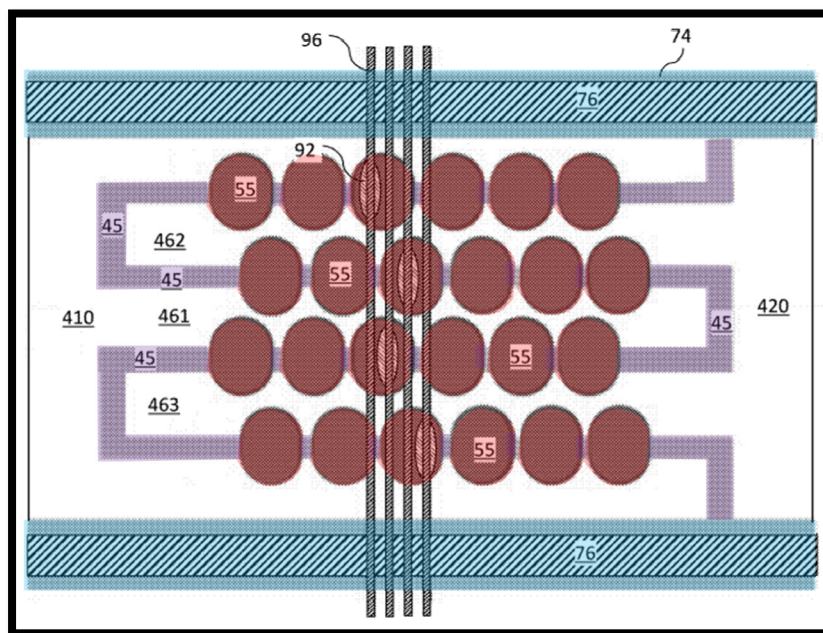
95. **Second**, Petitioner argues “adding dummy structures would result in an overall more uniform feature pattern, which reduces processing issues.” Pet. 60. Neither Petitioner nor Dr. Lee argue that Nishikawa’s device would suffer from a lack of uniformity or that including a “uniform feature pattern” would have been motivated to have such a feature in Nishikawa. *See* Pet. 59-60; Lee Decl., ¶ 142.

96. Dr. Lee cites a single reference, Ronse (Ex. 1026), for support that “adding dummy channels such that the overall pattern is more consistent was well known for decades.” Lee Decl., ¶ 142 (quoting *id.*, 11 (“As a result, this technique is particularly useful in regular patterns like memories, and much less in random logic designs where features can be completely irregular.”)). But Ronse does not provide support for Dr. Lee’s conclusion or Petitioner’s argument. For one, Ronse does not mention dummy channels at all. *See* Ronse. And the “technique” Dr. Lee cites is “[q]uadrupole illumination,” which is irrelevant to the benefits of adding dummy channels. Ronse, 11. And Ronse was published on November 22, 2006, before the creation of 3D NAND and long before its market entrance in 2013, the relevant technology of the ’322 Patent and Nishikawa. Ronse, 1; Ex. 2025, 3-4 (discussing 3D NAND technology being “introduced in 2007” and commercialized in 2013); *see* Pet. 27-28 (“Nishikawa is directed to 3D NAND”); ’322 at Abstract

(“Embodiments of three-dimensional (3D) memory devices ... are disclosed.”).

Thus, Ronse does not disclose any processing issue that is related to adding dummy channels to a device like Nishikawa's and would not have motivated a POSITA to add dummy channels to Nishikawa.

97. Further, Petitioner does not explain where or how dummy channels would be placed “in the memory stack,” including to extend the memory cell pattern in such a manner as to “result in an overall more uniform feature pattern.” Pet. 59-60. There is no room in Nishikawa's device to add dummy channels in the memory stack. Nishikawa's memory stack already is densely occupied by memory cells (55), electrical connection (66, 410, 420, 76), and structural support (45), as shown below:



Nishikawa Fig. 16 (annotated)

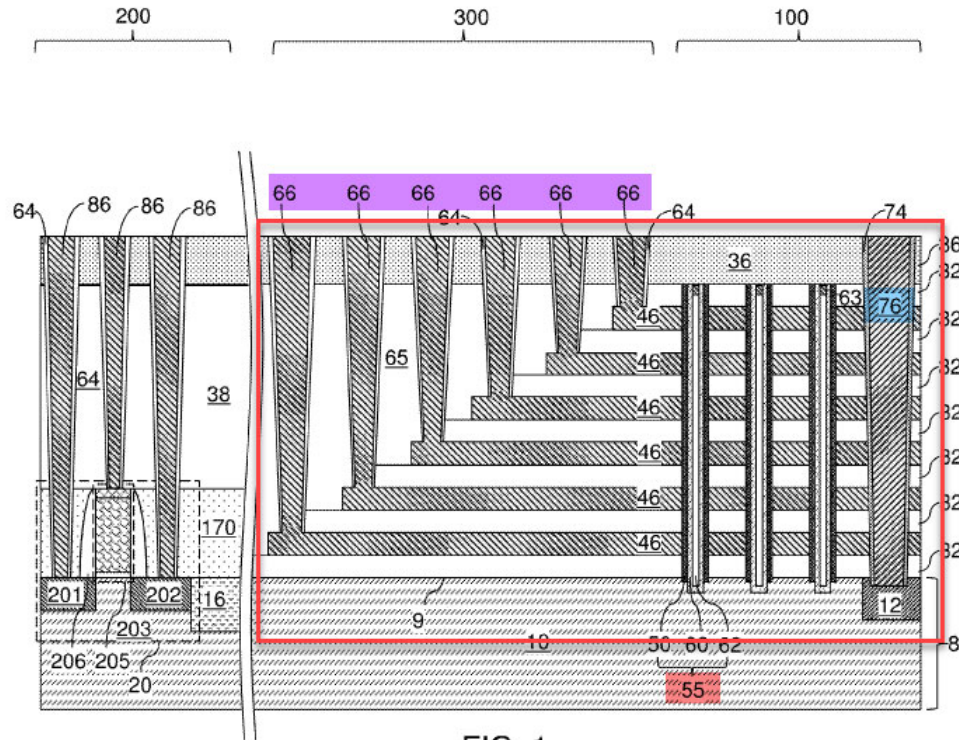


FIG. 1

Nishikawa Fig. 1 (annotated)

Indeed, as shown above, Nishikawa's staircase already contains support structures, electrical connections, and memory cells across and throughout the staircase, including those mentioned above. Nishikawa, Figs. 1, 4B, 16; *id.* 17:14-18. A POSITA would have recognized there is not physical space for a dummy structure in Nishikawa's memory stack. For this reason, a POSITA would not have been motivated to add dummy channels through Nishikawa's stack nor would have had a reasonable expectation of success in doing so.

98. **Third**, Petitioner asserts that dummy channels "can be made by the same process and at the same time as the active channels." *See* Pet. 63. This

shows, at best, that a POSITA could have made dummy channels, not that a POSITA would have been motivated to modify Nishikawa, as proposed by Petitioner. To the contrary, for the reasons stated in this declaration, a POSITA would not have been motivated to add dummy channels to Nishikawa's device, where there are no benefits and significant drawbacks a POSITA would have recognized by adding dummy channels.

3. Petitioner's proposed modification of Nishikawa would introduce performance, cost, and processing disadvantages to Nishikawa's device

99. In addition to the lack of structural benefits and processing benefits, a POSITA would have recognized that Petitioner's proposed modification has significant drawbacks, including decreased memory density, increased costs, and additional processing risks. It is my opinion that these drawbacks, in the absence of advantages as discussed above, would have dissuaded a POSITA from adding dummy channels to Nishikawa's device for the reasons discussed below.

100. *First*, Petitioner's proposed addition of dummy channels would reduce Nishikawa's memory storage capacity by reducing memory density (i.e., integration density). Memory storage capacity is a key performance metric for 3D NAND devices. A key aspect of the storage capacity of a device is the amount of bits that can be stored per unit area on a 3D NAND chip. In other words, the memory density. Active channels store data in memory cells, and dummy channels

do not. If there are more memory cells in a given space, the memory density increases. As described above, a POSITA would have recognized there is no room in Nishikawa's memory stack to add a dummy channel structure. *Supra* Section IX.A.2. To add a dummy channel structure through Nishikawa's stack, a POSITA would have to do one of two things: either (1) increase the size of the stack to create space for a dummy structure or (2) decrease Nishikawa's storage capacity by replacing functional "memory stack structures 55" (which serve as channels for the memory cells (Nishikawa, 4:28-32)) or "contact via structures 66" (which provide external access to the wordlines (*id.*, 6:45-47)) with non-functional dummy channels. Petitioner does not argue a POSITA would have replaced Nishikawa's existing memory stack structures 55; it argues a POSITA would have "include[d]" dummy channels. Pet. 59.

101. Either way, both increasing the size of the stack or replacing active channels with dummy channels would decrease the memory density of Nishikawa's device. In the first instance, increasing the size of the stack, such a modification would increase the size of the memory array without adding additional active memory capacity capable of storing data. That modification would lower Nishikawa's memory density. In the second instance, which Petitioner does not propose here (Pet. 59), replacing functional memory stack structures would replace structures capable of storing data with non-functional

dummy channels, effectively reducing the space available for active memory units.

As a result, the memory density of Nishikawa's device would be reduced.

102. POSITAs would have understood that a 3D NAND chip with a higher memory integration density, i.e., without dummy channels, could store more data in the same physical space compared to a chip with lower memory integration density. *See* Kim, [0003] (“Semiconductor devices have been highly integrated for satisfying high performance and low manufacture costs which are desired by users.”). A prominent goal in designing a 3D NAND device is having a high memory density. Dr. Lee testified that “[memory] density is *one of the most important aspect[s] in designing memory*,” and that “we always want to have as high density as possible; for lower cost, higher yield, and ... a lot more money per chip.” Lee '254 Dep. (Ex. 2022), 44:8-11, 48:1-6; *see* Lee Decl., ¶ 165 (“The driving force in manufacturing memory is to create as dense as an array as possible ... memory capacity is obvious[ly] a key element of a memory.”), ¶ 205 (“[M]emory designs typically attempt to achieve a very dense memory array”).

103. A POSITA would have recognized that Petitioner's modification of Nishikawa to add dummy channels to the memory stack would reduce the space per unit area for active channels that can store data (i.e., memory) and be counterproductive to the preeminent goal of achieving higher density in 3D NAND structures. Thus, a POSITA would not have been motivated to reduce memory

density, and therefore would not have added dummy channels to the memory stack of Nishikawa. *See, e.g.*, Ex. 2030, 3 (recognizing that 3D NAND design is “all in pursuit of higher memory density”); Ex. 2029, 5 (“In 3D NAND, the ultimate goal is to stack more layers on a substrate, enabling more density.”).

104. ***Second***, decreasing memory density makes a device less cost effective. A POSITA would have recognized that Petitioner’s modification that decreases Nishikawa’s memory density is less cost effective. Dr. Lee agrees, admitting “[a]s density increases, the memory design becomes more cost effective.” Lee Decl., ¶ 165. Specifically, as Dr. Lee recognizes, the less dense the memory array, the more silicon is needed to create a given memory size. Ex. Lee ’254 Dep., 48:18-49:2; Lee Decl., ¶ 165 (“[T]he denser the array, the less silicon is necessary to create a given memory size. ***As density increases, the memory design becomes more cost effective.***”). This is because fewer raw materials are needed to create a device, reducing the material input costs. *See* Ex. Lee ’254 Dep., 48:18-49:2; Lee Decl., ¶ 165. A POSITA would not have motivated to add dummy channels with no discernable benefits in a manner that increases costs.

105. ***Third***, adding dummy channels would have introduced processing risks. A POSITA would have considered Nishikawa’s structure, with or without additional dummy channels, to be dense and require high aspect ratio features

through the memory stack. In striving to increase memory density, POSITAs would have recognized that forming dense arrays via high-aspect ratios is a difficult task that leads to tapering in the channel. Tapering occurs where the sidewalls in a channel narrow toward the bottom of the channel. As a result, when the channel narrows, the etch-rate would slow, causing the channels to not penetrate all layers in a stack. Dr. Lee also recognizes that tapering is “undesirable” and admitted that forming “the dense array via high-aspect ratios” is “difficult” and can lead to “tapering.” Lee Decl., ¶¶ 205, 212; Lee Dep., 25:9-17.

106. A POSITA would have recognized that adding additional channels increases the risk that tapering occurs in the memory array and would not have a reasonable expectation of success in adding additional dummy channel structures to Nishikawa’s already dense array. Indeed, in Ground 4, Petitioner argues a POSITA would have been motivated to combine Lu’s multideck memory stack with Nishikawa’s device because “driving motivation for multideck structures is the difficulty in etching high aspect ratio channel holes.” Pet. 84. Petitioner undermines any expectation of success in adding dummy channels by the same process. And a POSITA would not have been motivated to add processing risk with no additional benefits, as discussed above.

107. In sum, a POSITA would not have been motivated to add dummy channels to Nishikawa's structure in light of these disadvantages without any additional advantages, which are not present, as discussed above.

B. Petitioner's cited references do not render obvious adding dummy channels "in the memory stack"

108. The Petition cites five references to "confirm[] the knowledge of a POSITA" that it was "well known to include dummy channel structures to provide structural support": Nishikawa123, Masamori, Kai, Park297, and Kim. Pet. 60. Regardless of whether those references disclose the knowledge of a POSITA, none would have motivated a POSITA to add dummy channel structures to Nishikawa.

109. Dr. Lee quotes Nishikawa123 as "recogniz[ing] th[e] known need" for support pillars during the gate replacement process. Lee Decl., ¶ 143 (citing Nishikawa123, 9:63-67 ("At least one dielectric pillar structure (not shown) can be formed through the entire set of the spacer material layers 42 and the insulating layers 32....")). But the cited passage merely describes the formation of a "not shown" dielectric pillar structure and says nothing about a "need" for support structures. Nor does it provide any reason to add support structures. Further, the Petition does not even assert that Nishikawa123 discloses dummy channels. Pet. 60.

110. As another example, Dr. Lee cites to Masamori's disclosure of "conductive support structures." Masamori (Ex. 1020), Cover (Title); *see* Lee

Decl., ¶ 146. Unlike Nishikawa, Masamori's design does not include separator dielectric structures that provide structural support during the gate replacement process.

111. Masamori devotes most of its "contact via region" (yellow) (most of contact regions 200A, 200B) adjacent to its "memory array region 100" to its conductive support structures, as shown in Figure 20B, annotated below, unlike Nishikawa that does not have a region to accommodate dummy channels. *See* Masamori, [0050], [0109], [0135], [0136], [0150], Fig. 20.

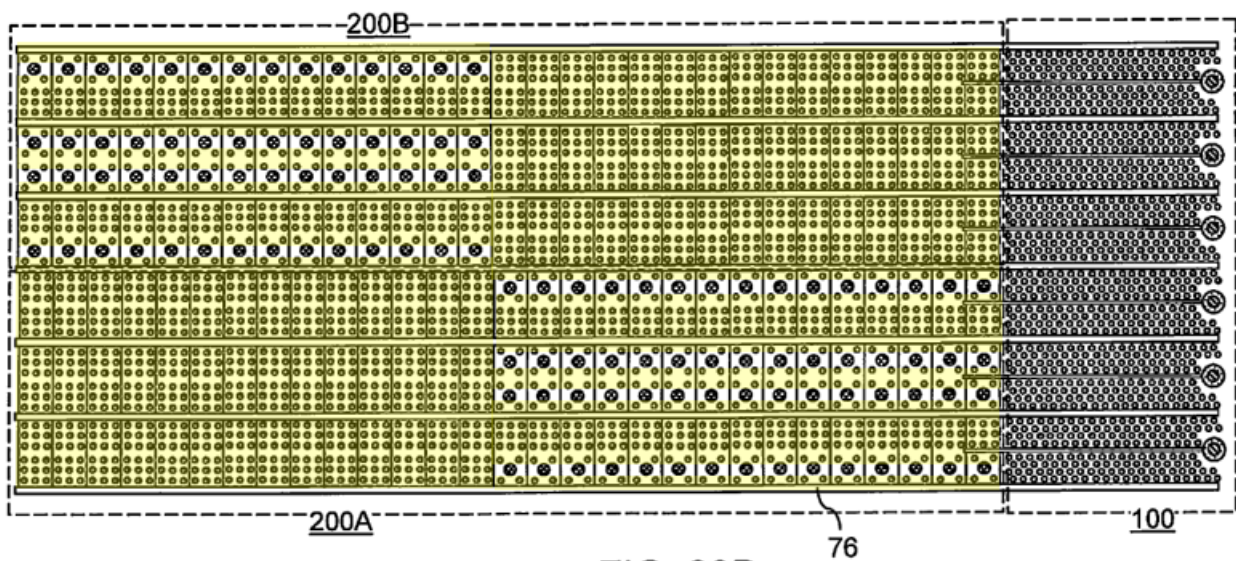
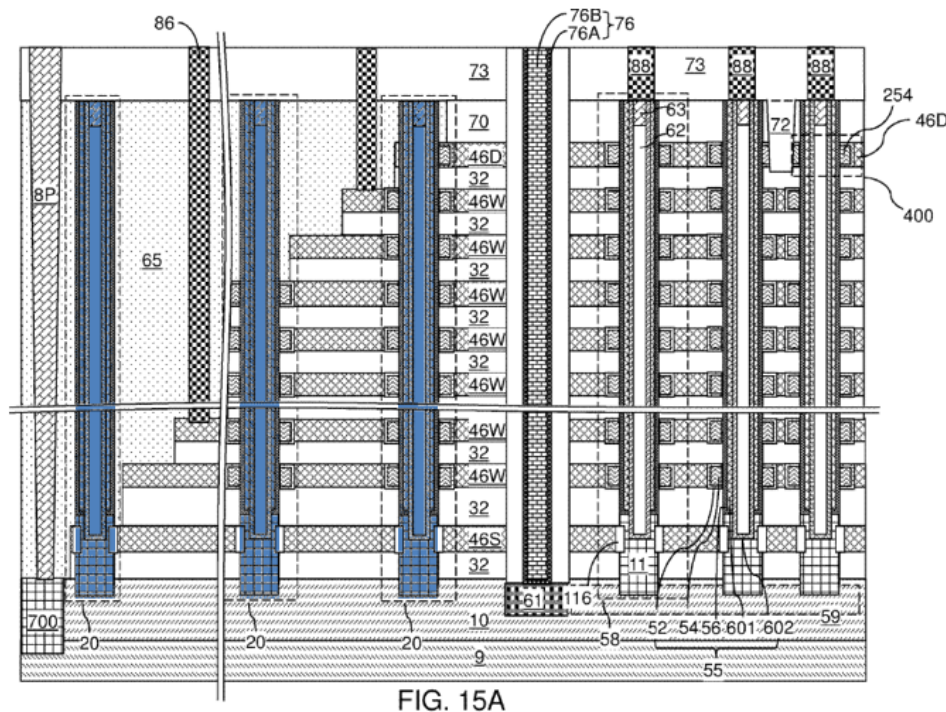


FIG. 20B

Masamori Fig. 20B (annotated)

112. Masamori's disclosure of support structures would not have motivated a POSITA to modify Nishikawa because Nishikawa has a different design that includes separator dielectric structures 45 that already provide the structural support Petitioner asserts is needed for gate replacement.

113. Dr. Lee cites to Kai as demonstrating it was “well known to include dummy support members that extend through the entire stack or partially through the stack.” Lee Decl., ¶ 143.



Kai Fig. 15A (annotated)

114. But Kai discloses “support pillar structure[s] 20” taking up significant area in a “contact region 300” in a device that, unlike Nishikawa, (1) includes no separator dielectric structures supporting the other structures during gate replacement, and (2) has a different layout than Nishikawa. Kai (Ex. 1027), Fig. 6A, 6:2-5, 16:28-31; *see also id.*, Fig. 15A (above) (showing “support pillar structure 20” (blue) only in the contact region). As shown above, Kai’s support pillar structures are in a contact region designed to accommodate dummy

structures, unlike Nishikawa. Kai would not have motivated a POSITA to add dummy channels to Nishikawa, which already has support structures.

115. Finally, Dr. Lee cites Park297 (Ex. 1028) and Kim (Ex. 1029) as disclosing “dummy, supporting channels.” Lee Decl., ¶ 145. Neither Park297 nor Kim have dielectric separator structures, like Nishikawa. Nor do they lack a region for dummy channels like Nishikawa. *See* Park297, Abstract (disclosing separate “cell and dummy regions”); Kim, [0047] (“The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region STR”), [0070] (“On the connection region CTR, a plurality of dummy holes DH may be formed.”). In fact, Kim and Park297 disclose that the dummy channels *should not* be within the memory cell array. Kim, [0047]; Park297, Fig. 1, 7:38-42; *see* Pet. 62 (citing Park297, 7:45-51 as disclosing dummy channels).

116. In sum, none of the above references disclose adding dummy channels to support a system like Nishikawa’s that already has a separator dielectric structure as an existing support structure and no region to accommodate dummy structures. Thus, none would have motivated a POSITA to modify Nishikawa as Petitioner proposes.

C. Dummy Channels are complex

117. In my opinion, adding a “dummy channel structure” in Nishikawa is not unusually simple. To the contrary, it is exceedingly complex. As described

above, one of the driving goals of creating a memory structure is to increase the memory density of the device. As more features are added to a device in an attempt to increase density, it becomes more difficult to form devices with those features—which become increasingly smaller and each perform a particular function but are structurally interrelated—to a device at the nano scale that, together, form a functioning memory device. This is true of adding dummy channel structures to a device, which must occupy valuable space in the memory stack, among other features, such as active channels, dielectric materials, and interlayer connections. Ex. 2028, 2 (“The big challenge is to characterize the inner portions of a 3D NAND device, which consists of complex materials, multiple layers and tiny channel holes.”). Indeed, a POSITA would have understood that the space available for making such structures is measured in nanometers and angstroms, not inches, feet, or millimeters. *See* Ex. 2027 1 (stating 3D NAND “channels” have “unique process control requirements” because of “angstrom-level precision requirements.”).

118. A POSITA would have recognized adding memory device features in a dense array—such as dummy channels—is inherently related to and limited by the fabrication methods and techniques available. *See* ‘322 Patent, 5:9-22 (describing the relationship between processing and design); Ex. 2036, 3 (stating “optimiz[ing] manufacturing processes” “result[s] in better performance, increased yield, and reduced costs”). This is also true of 3D NAND structures. Creating a

3D NAND device with the claimed features requires being able to etch various features in the structure along with depositing various materials. Etching is the most difficult step in 3D NAND and includes creating more than a trillion holes with a high aspect ratio with virtually no lateral variation in order to make contact with the landing pad deep in the structure. Ex. 2028, 4 (describing the etching process as “the most difficult step in 3D NAND”); Ex. 2032, 6 (describing the etching process as “the hardest part of the flow” because “the etch tool must drill tiny circular holes or channels from the top of the device stack to the bottom substrate”—“[e]ach channel must be parallel and uniform”); Ex. 2023, 6 (“More than a trillion holes must be etched simultaneously and uniformly on every wafer, each with an aspect ratio of more than 40:1.”); *id.*, 4-5 (“An incredible level of precision and repetition is required in defining complex 3D structures with extremely high aspect ratio (HAR) features.”); Ex. 1010 218 (“One of the issues is related to yield loss derived from complexity of vertical trench or hole etching with many layers.”). In other words, there is close to no room for error.

119. Etching is also necessary to add the claimed dummy channel to Nishikawa because it is the process by which channels are formed through a memory stack, and successfully doing so is central to achieving a cost-effective device. *See* Ex. 2023, 6 (stating the etching process is “the most critical and challenging step in 3D NAND because it is key to achieving uniform hole size

through multiple layers to define the channel of memory cells”); Ex. 1010, 218 (“One of the issues is related to yield loss derived from complexity of vertical trench or hole etching with many layers.”); Ex. 2026, 6 (describing importance of HAR channel etch in 3D NAND); Ex. 2028, 4 (describing the etching process as “the most difficult step in 3D NAND”).

120. The claimed dummy channel structure extends completely through the memory stack, which is a complex feature. '322 Patent, cl. 3. A POSITA would have recognized that forming the claimed dummy channel structure through the memory stack involves various steps of complex semiconductor manufacturing processes, including “etching an opening through dielectric stack 218 and/or one or more dielectric layers using wet etching, and/or dry etching, such as DRIE” and “thin film deposition processes, such as ALD, CVD, [and] PVD.” '322 Patent, 12:16-23. Forming these channels through the entire memory stack is not simple. As described above, 3D NAND structures are formed at the microscopic scale. The features, including dummy channels, have feature sizes and tolerances down to the angstrom. *See also* Ex. 2032, 7 (recognizing “[t]he memory hole etch is probably the most difficult step in 3D NAND manufacturing” because “[y]ou need to etch many microns deep and you need to be able to tightly maintain the profiles to very specific dimensions”). Further, a POSITA would have recognized creating a uniform dummy channel to avoid defects, such as the tapering issue described

above, pushes the limits of physics. Ex. 2023, 6 (“[d]eep etch[ing] on these multilayer stacks can push the limits of physics to achieve uniformity from top to bottom”); Ex. 2033, 4 (“This etch is really complex.”); Ex. 2026, 6 (describing HAR etching as the “hardest part of the flow” and “very difficult and very time-consuming”); Ex. 2023, 4 (Figure 1 depicting a “3D NAND architecture showing some of the most challenging and critical deposition and etch processes”); Ex. 2024, 2 (“The etch process to create these channels is also one of the main challenges for current and future 3D NAND designs” because “variations in the channel holes can have drastic effects on the performance of 3D NAND devices.”).

121. The deeper the etch, the harder it is to maintain a continuous etch rate. And unwanted variations can occur, such as tapering, bowing, or twisting within the channel, an incomplete etch, or variation between the top and bottom of the channel. Ex. 2023, 6, Fig. 3; *id.* (“channel hole etching becomes increasingly challenging due to higher aspect ratios”); Ex. 2031, 6-7, Fig. 7; Ex. 2030, 3 (“The channel hole etch is one of the most challenging processes” because “[t]ight control is needed to minimize bowing and twisting of the channel, which could lead to shorts or interference between neighboring memory strings.”); *see also* Ex. 2024, 2-3 (“[T]he channel hole HAR etch is arguably the most difficult step and adds considerable challenges ... [a]ny variations in channel hole width from top to bottom need to be characterized, and problems such as bow CD, twist, and tilt need

to be identified. To further complicate this process, as the etch depth increases, etch rates tend to decrease, which can exacerbate these problems.”).

122. While some of the above references discuss forming memory channels, they equally apply to etching dummy channels through the stack, which are sometimes formed by the same process as memory channels. *See, e.g.*, ‘322 Patent, 12:23-27 (“In some embodiments, dummy channel structures 302 are formed simultaneously with channel structures 222 in the same fabrication steps, such that the opening of each dummy channel structure 302 is filled with at least some of the materials filling in channel structures 222.”); Kim, [0071] (“The channel holes CH and the dummy holes DH may be formed at the same time.”).

123. Dummy channels also vary in their structures and materials. They range in size, location, and materials. For example, dummy channels may be formed of the same materials as channel structures, but also may be “fully filled with dielectric materials” like “silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.” ‘322 Patent, 9:27-37; *see* Kai, 16:23-27 (teaching its “support pillar structure 20” is a combination of at least “a memory film 50, a vertical semiconductor channel 60, a dielectric core 62, and a drain region 63 within each support opening 19”).

124. Petitioner’s cited prior art confirms the design and fabrication of a dummy channel structure is complex, not unusually simple. For example, the Kai

reference describes the process of forming a support pillar structure 20 (Petitioner's "dummy channel" (Pet. 62)) in support opening 19 by referencing Figures 5A-5L. Kai, 10:20-26 ("FIGS. 5A-5L illustrate structural changes during formation of a memory stack structure, an optional dielectric core, and a drain region in a memory opening, ... [t]he same structural change occurs simultaneously in each of the other memory openings 49 and in each support opening 19."), 16:28-31 (support pillar structure 20 formed in support opening 19), Figs. 5A-5L, 6A, 6B. Kai describes at least seven distinct processing steps for forming a support pillar structure 20 (Petitioner's "dummy channel") (Pet. 62) in a particular arrangement. Specifically, Kai describes the process to form a support pillar structure 20 (i.e., dummy channel) includes at least forming a recess (Kai, 10:27-42, Fig. 5A), laterally recessing sidewalls of sacrificial material by isotropic etching (*id.*, 11:9-34, Fig. 5C), depositing and etching a blocking dielectric layer 52L on exposed surfaces of the support openings 19 to form blocking dielectric 52 (*id.*, 11:35-53, Fig. 5D), depositing and etching a floating gate material layer 54L in the annular recesses formed in the sidewalls to form a vertical stack of floating gate electrodes 54 (*id.*, 12:20-13:47, Figs. 5E, 5F), depositing a tunneling dielectric layer 56 and optional first semiconductor channel layer 601 before performing another anisotropic etch (*id.*, 13:48-14:64, Figs. 5G, 5H), depositing a second semiconductor channel layer 602 (*id.*, 14:65-15:26, Fig. 5I), depositing and etching dielectric core layer 62L to

form a dielectric core 62 (*id.*, 15:27-59, Figs. 5J, 5K), and depositing a doped semiconductor material to form a drain region 63 (*id.*, 15:60-16:12, Fig. 5L).

125. Kim similarly demonstrates the complexity of a dummy channel and its component parts. Kim discloses forming a dummy structure within dummy holes by making a lower semiconductor pattern by an epitaxial growth process, covering an inner sidewall with a vertical insulation layer and an upper semiconductor pattern using atomic layer deposition or chemical vapor deposition, filling the dummy hole with a buried insulation pattern, and forming a pad on the upper portion of the dummy structure. Kim, [0047], [0073]-[0074]. Kim teaches that each of its dummy holes may have a diameter that “gradually increases” with increasing depth. Kim, [0070].

126. As another example, Park describes another structure and processes for dummy channels (second channel structure 120b according to Petitioner (Pet. 62 (citing Park, 7:45-51))). Park describes forming channel holes (Park, 11:47-58, 10:11-61), performing a silicon epitaxial growth process to form semiconductor patterns 110 (*id.*, 10:62-67), forming a dielectric layer structure 112 on the sidewalls of the channel holes (*id.*, 11:1-23), forming a channel layer 114 on top of dielectric layer structure 112 as well as forming a filling pattern 116 within the channel layer 114 (*id.*, 11:24-33), and forming a pad 118 disposed on top of etched-

back portions of dielectric layer 112, channel layer 114, and filling pattern 116 (*id.*, 11:34-46). *See also id.* at 11:46-51, 6:19-26, Fig. 6.

127. Given the complexities described above, including those highlighted in Petitioner's references, adding a dummy channel structure is not unusually simple.

X. Nishikawa and a POSITA's knowledge, alone or with Nishikawa¹²³, do not render obvious "a first diameter [or lateral dimension] of the TAC corresponding to each conductive layer ... is larger than a second diameter [or lateral dimension] of the TAC corresponding to each dielectric layer" (claims 13-18, 20)

128. Claim 13 depends from claim 8 and recites "a lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs" ("ribbed via cavity"). '322 Patent cl. 13. Claim 14, instead of reciting a "diameter," it recites a "lateral dimension." And claims 15-18 and 20 depend from claim 14. The "first diameter[/lateral dimension]" of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs being larger than the "second diameter[/lateral dimension]" of the TAC corresponding to each dielectric layer of the conductor/dielectric layers pairs is the result of forming a "plurality of recesses" by "removing parts of the sacrificial layers abutting the sidewall of the first opening" that is then filled in with the TAC. '322 Patent 13:42-45, Fig. 3D.

129. Petitioner alleges that Nishikawa and the knowledge of a POSITA render obvious the recited first and second diameter/lateral dimensions under two different claim interpretations: (1) by inherent “undetectable and unintentional alleged recesses” formed by the typical etching process resulting in the first and second diameters/lateral dimensions defining the TAC’s geometry (Pet. 73-75), and (2) by an “intentional etch that forms actual recesses” for the same TAC geometry (*id.* 73-77). In my opinion, Petitioner fails to render obvious the ribbed via cavity limitations under either interpretation.

A. Petitioner’s arguments fail under its first claim construction that requires “undetectable and unintentional recesses”

130. Petitioner and Dr. Lee assert that the ’322 Patent does not support that the claims cover unintentional recesses, but “makes clear that these limitations relate to an intentional etch that forms actual recesses in the sacrificial layers.” Pet. 73 (citing ’322 Patent, 13:47-61, Fig. 3D); Lee Decl., ¶ 170 (citing same). Petitioner and its expert do not cite anywhere else in the intrinsic evidence to support that the ’322 Patent’s ribbed via cavity limitations require an intentional etch that forms actual recesses in the sacrificial layers. It is my opinion that a POSITA would not have understood the ribbed via cavities are met only by intentional etches. *See* ’322 Patent, cls. 13 and 14, 13:52-65, Fig. 3D.

131. In my opinion, Petitioner’s arguments under this construction fail on the merits. Petitioner asserts that “a typical etch through a stack of silicon oxide

and silicon nitride layers does not have the exact same selectivity towards each of silicon oxide and silicon nitride, and will result in uneven sidewalls, such that there are recesses in either the oxide layers or the sacrificial layers.” Pet. 74-75. Petitioner further asserts that, as a result, “Nishikawa renders this limitation obvious ... because such unintentional recesses would naturally occur.” *Id.* 75. Unintentional recesses would not naturally occur or necessarily present in Nishikawa’s contact via structure. As shown below in Figure 15, Nishikawa’s backside contact via structure 76 and accompanying dielectric spacer 74 has a consistent diameter/lateral dimension throughout:

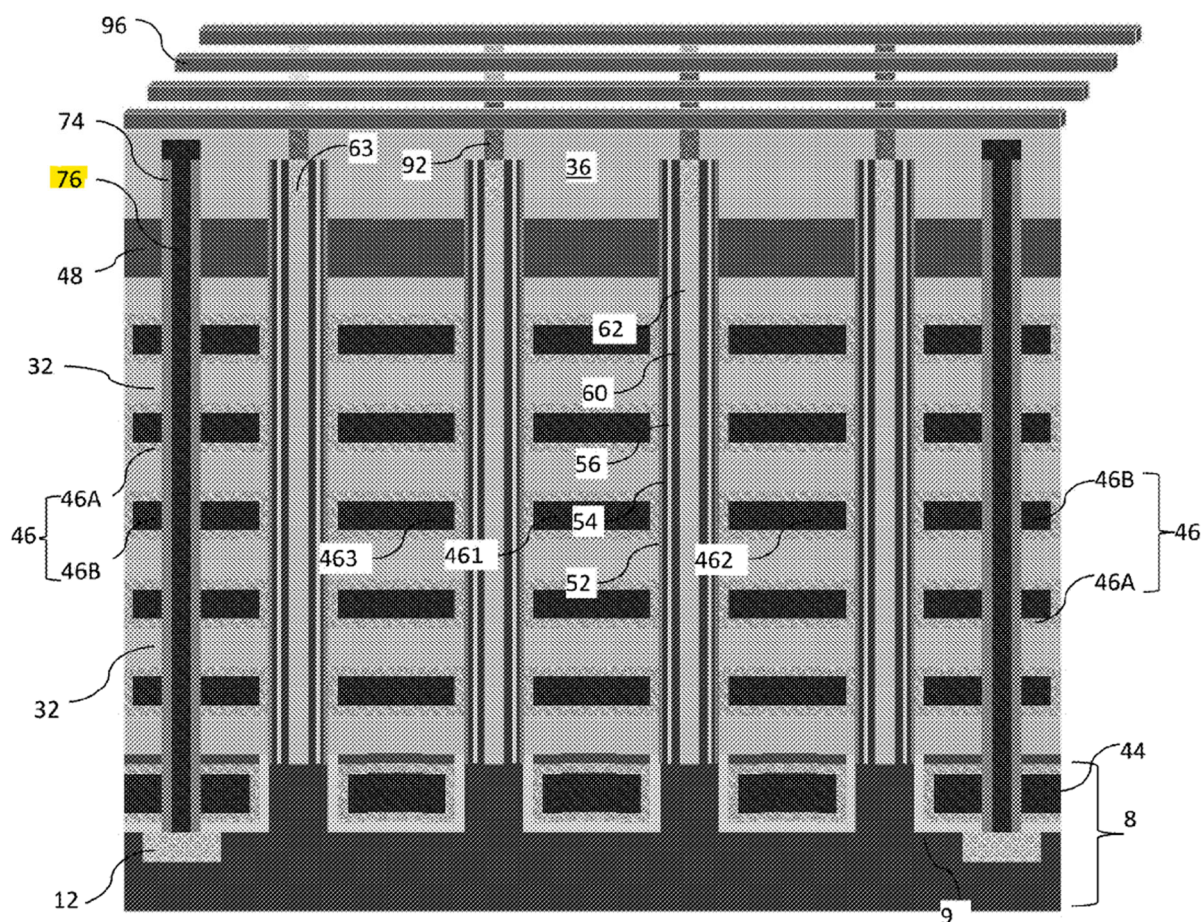


FIG. 15

Nishikawa Fig. 15 (annotated)

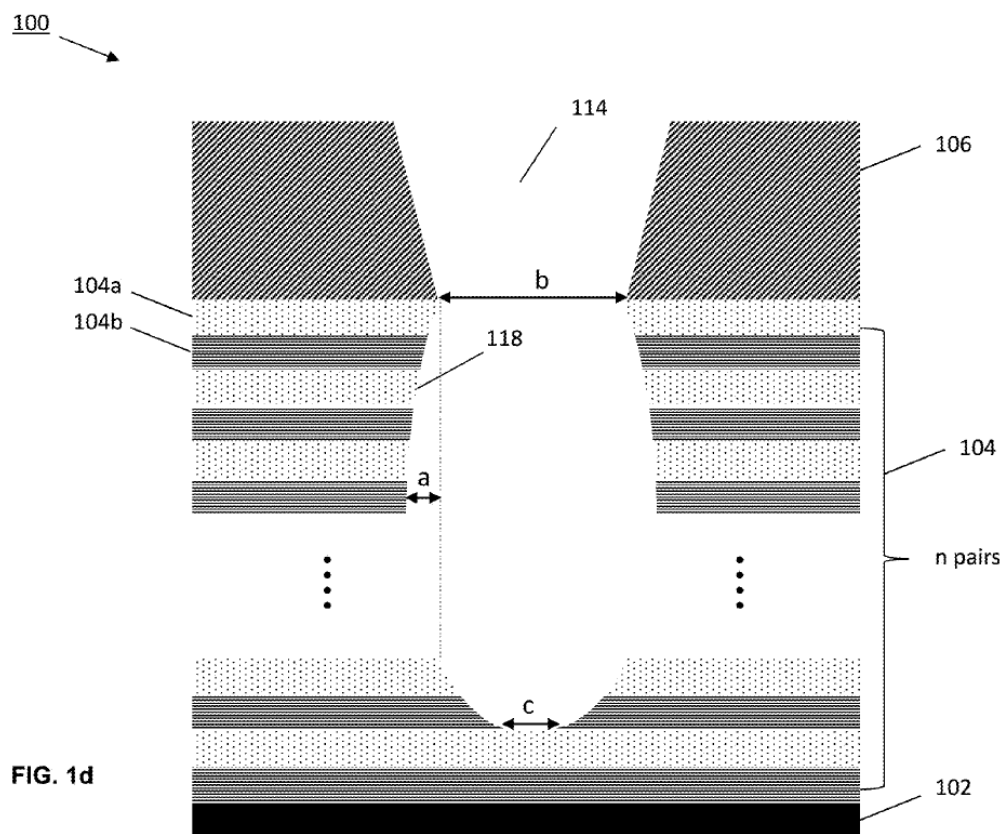
As discussed above, Nishikawa provides for etching recesses in forming the active channels during the gate replacement process, but it does not do so for forming TACs. *See supra* Section IX.A.1. It is my opinion that Nishikawa does not render obvious that a TAC would inherently have non-smooth sidewalls.

132. Further, in my opinion, Petitioner fails to provide any evidence that Nishikawa uses a “typical etch” that allegedly inherently forms “unintentional

recesses ... causing the claimed differences in width” in Nishikawa’s backside contact via structure 76. *See* Pet. 74-75. Petitioner only identifies Nishikawa’s disclosure that its “insulating layers 32” can be made of silicon oxide and its “sacrificial material layers 42” can be made of silicon nitride. *Id.* at 74 (quoting Nishikawa 7:3-11). Petitioner argues because “a typical etch” through those layers does not have the same selectivity, the TAC in Nishikawa would have uneven sidewalls. *Id.* 73-74. As discussed above, unintentional recesses would not have been the natural result of forming Nishikawa’s structure. Nor would a POSITA have been motivated to use such processes.

133. In support of Dr. Lee’s opinion that “typical prior art etches that effectively create a hole through the stack result in very small lateral recesses in either the dielectric spacers or sacrificial layers,” Lee Decl., ¶ 171, he cites Exhibit 1039. The cited passage of Ex. 1039 says no such thing. Rather, the passage describes that “[a]lthough there are numbers of prior arts for SiO₂ etching with high selectivity to SiN, for certain applications, it is important to have an etching gas which can etch both SiO₂ and SiN layers...without selectivity.” Ex. 1039 2:59-63. A POSITA would understand that etching gases “without selectivity” etch the layer stack evenly resulting in smooth vertical sidewalls—without recesses. This passage describes that it is important to have an etching gas without selectivity (which etches the layers evenly), and the patent itself purports to provide a solution.

As Exhibit 1039 further explains, its proposed solution mitigates against sidewall bowing or barreling as depicted in Figure 1d, below. Ex. 1039, 18:38-63. Exhibit 1039 further describes bowing as undesirable, and does not motivate or inform a POSITA that such a pattern would be formed in Nishikawa. Ex. 1039 18:42-44. Nor does it suggest forming a ribbed via cavity.



Ex. 1039, Fig. 1d.

134. This demonstrates that a POSITA would have been discouraged from using an etch process that produces recesses forming the ribbed via cavity. As such,

etching would not inherently produce the claimed ribbed via cavity under Petitioner's "undetectable and unintentional recesses" construction. Pet. 73.

135. Petitioner and Dr. Lee also assert Nishikawa renders obvious unintentional recesses because "it is a challenge to find" a gas that can etch "without selectivity." Pet. 74; Lee Decl., ¶ 170. But as demonstrated above, it is my opinion that a POSITA would have been motivated to, and could have, found a gas that etches without selectivity. *See, e.g.*, Ex. 1039, 24:34-37 (disclosing "hydrofluorocarbon etching gases provide etching through SiN and SiO₂ layers in a single etching process without selectivity"). Nor would a POSITA have understood Nishikawa's to be etched with a gas without selectivity that forms a ribbed cavity.

136. Thus, even under Petitioner's "undetectable and unintentional recesses" construction, etching would not inherently produce the claimed first and second TAC diameters/lateral dimensions.

B. Petitioner's arguments fail under its second claim construction that requires "intentional" formation of "actual recesses"

137. Petitioner next argues this limitation would have been obvious under Petitioner's second "interpretation" of the claim that requires the "intentional" forming of "actual recesses." Pet. 75-77. Neither Petitioner nor Dr. Lee argue that Nishikawa discloses this limitation but assert that it would have been obvious

based on a POSITA's general knowledge. *Id.* 75-76; Lee Decl., ¶¶ 169,172-173.¹

Petitioner and Dr. Lee further assert that POSITAs would have been motivated to modify Nishikawa to include a ribbed via cavity because doing so would have “serve[d] the same purpose as the '322 Patent, namely, providing additional area for the dielectric liner.” *Id.* 76.

138. Petitioner and Dr. Lee cite only the '322 Patent's statement that the “partial removal process can provide space for a thicker dielectric layer deposition in the next step” in support of its argument a POSITA would have been motivated to include a ribbed via cavity in Nishikawa. Pet. 77 (citing '322 Patent, 13:38-51); Lee Decl., ¶ 173 (same). Indeed, Petitioner and Dr. Lee argue “The ribbed via cavity serves the same purpose as the '322 Patent, namely, providing additional area for the dielectric liner.” Pet. 77 (citing '322 Patent, 13:38-51); Lee Decl., ¶ 173 (same). The Petition concludes in the next sentence: “Accordingly, in view of the knowledge of a POSITA, it would have been obvious, and a POSITA would have been motivated to, create a ribbed via cavity in Nishikawa's through-array via holes.”

¹ Dr. Lee states “Nakajima renders this limitation obvious under PO's incorrect interpretation and under the correct interpretation.” Lee Decl., ¶ 98. I understand Petitioner's ground to be based on Nishikawa, not Nakajima, and understand Dr. Lee's use of Nakajima to be a typographical error. *See id.* ¶ 75 (Summary of Grounds for Invalidity: Nishikawa Grounds).

139. Neither Petitioner nor Dr. Lee explains why the hindsight motivation of “providing additional area for the dielectric liner” is advantageous, only that it creates a longer spacer, as the ’322 Patent recites. *See* Pet. 77; Lee. Decl., ¶¶ 173-174; ’322 Patent, 13:38-51. As explained above, Counsel has informed me that a motivation to combine based on the teachings of the challenged patent is also an impermissible form of hindsight bias. Petitioner and Dr. Lee’s purported motivation relying on the ’322 Patent’s teachings would not have motivated a POSITA to modify Nishikawa based on the teachings of the ’322 Patent.

140. Petitioner and Dr. Lee further point to Kai and Cui to show it was “well known” to have a ribbed-shaped opening, Pet. 75-76; Lee Decl., ¶¶ 173-174. Neither would have motivated a POSITA to modify Nishikawa to include a ribbed via cavity. As an initial matter, a POSITA would not be motivated to modify Nishikawa only because other references disclose ribbed via cavities. Regarding Cui, Dr. Lee argues that Cui’s recesses “create[] additional space,” the same motivation from the ’322 Patent that the Petition relies on in modifying Nishikawa. Lee Decl., ¶ 173 (citing Cui (Ex. 1037)). Petitioner cites Kai for disclosure of forming “lateral[] recesses[s].” Pet. 75 (citing Kai, 11:9-34). Petitioner does not argue that Kai forms recesses in the “sacrificial layers” of an alternating stack of dielectric and sacrificial layers for openings associated with a TAC, as claimed. Rather, the “lateral[] recesses[s] do not disclose a “ribbed via cavity” that provides

“additional area for the dielectric liner” (Pet. 77) and thus does not support Petitioner’s motivation to combine. *See* Pet. 75; *see* Lee Decl., ¶¶ 173-174. Rather, Kai discloses that the recesses are filled with blocking dielectric 52 and a floating gate electrode 54 before tunneling dielectric layer 56 is deposited, not a spacer in a TAC. Ex. 1027, 11:35-39, 12:20-23, 12:47-49, 12:56-61, 13:48-51, Figs. 5C-5G.

141. In sum, Petitioner provides no reason besides hindsight based on the ’322 Patent why a POSITA would implement the claimed first and second TAC diameters/lateral dimensions formed by forming “rib regions” in Nishikawa’s backside contact via structures 76. Thus, it is my opinion that a POSITA would not be motivated to implement ribbed via cavities in Nishikawa.

C. A TAC with ribbed via cavities is complex

142. Forming a ribbed via cavity producing the claimed TAC dimensions/diameters is complex. Petitioner cites evidence that producing a particular profile of a TAC sidewall is “a challenge.” Pet. 74 (quoting Ex. 1039, 2:59-67). Dr. Lee also attempts to put the etching process into “simple terms” to explain the etching processes required to form a particular profile. Lee Decl., ¶ 170.

143. Forming a TAC with the ribbed via cavity is controlled by the etching rate and etching time. ’322 Patent, 13:61-63. Defining the claimed diameters by etching one material (e.g., Nishikawa’s sacrificial layers 42) is a challenging

endeavor. Ex. 2034, 2 (“An additional challenge is posed by the removal, in certain types of 3D NAND, of sacrificial layers in between the ‘steps’ of the staircase.”); Ex. 2029, 5-6 (describing the removal of nitride layers as part of a “complex” process); Ex. 2035, 1 (“because of miniaturization and complexity of structures,” 3D NAND “fabrication requires various highly selective etch processes not only for anisotropic etching but also for isotropic etching”).

144. In my opinion, a POSITA would understand that adding a ribbed via cavity—where the dimension/diameter corresponding to “each conductive layer” is greater than the dimension/diameter corresponding to “each dielectric layer, i.e. throughout the TAC—to a TAC cannot be simplified to etchant selection because control of the etchant chemistry, surrounding material, the uniform transport of etchant gasses and the etch byproducts through a HAR geometry, and complex process conditions are all key. *See, e.g.*, Mushiga, 1:17-28 (describing the high density and multi-tier 3D NAND flash memory structures “increase[] the complexity of the etch process for forming memory openings and the metal replacement process employed to form the word lines”), 6:10-13 (reaching depth uniformity using reactive ion etching (RIE) “increases process complexity”); Ex. 2026, 8-9 (describing removal of nitride layers in the stack and forming wordlines as “a complex process”); Ex. 2023, 6 (describing forming wordlines as “particularly challenging because of the need to achieve void-free fill of complex,

narrow, lateral structures with minimal stress on the memory stack”). Because of the isotropic nature of the etch (i.e., etching in all directions unlike an anisotropic (directional) etch), controlling the lateral recess distance required to form the claimed dimensions/diameter is critical because over-etching could compromise the structural integrity of the device, while under-etching would fail to effectively create the claimed ribbed via cavity. Ex. 2030, 3 (describing replacement-gate schemes as “particularly challenging because of the complex geometries involved”).

145. Further, a POSITA would understand that it is increasingly complex and challenging to achieve consistent etch profiles at the top and bottom of the holes in a memory array as the height of 3D NAND increases, especially when trying to reach a depth that creates the claimed diameters/dimensions without over etching. Ex. 2036, 3-4, Fig. 3. Also, the choice of material for both the target and non-target layers must be highly compatible with the selective etch chemistry because any incompatibility could lead to non-uniform etching, structural defects, or failure to form the intended structure. *See, e.g.*, Kai, 11:16-20 (“For example, if the sacrificial material layers 42 include silicon nitride, the insulating layers 32 include silicon oxide, and the epitaxial channel portions 11 include silicon, the isotropic etch process can include a wet etch process employing hot phosphoric acid as an etchant.”).

XI. Nishikawa and a POSITA's knowledge, alone or with Nishikawa123, do not render obvious a "diameter of the TAC is at least equal to a diameter of the peripheral contact" (claims 6, 9-10, 15-16)

146. Claims 6 and 15 recite "a diameter of the TAC is at least equal to a diameter of the peripheral contact." '322 Patent, cls. 6, 15. Claim 16 depends from claim 15. *Id.* cl. 16. The claimed TAC extends through the memory stack, while the peripheral contact is outside the memory stack. *Id.* cls. 1, 6, 14.

147. Petitioner argues "it would have been obvious to implement Nishikawa's TAC as a cylindrical contact with a diameter" and that a POSITA would have been motivated "to make the TAC and peripheral contacts the same size." Pet. 67, 69. Petitioner does not argue that Nishikawa discloses its trench-shaped backside contact via structures 76 (i.e., TAC) are at least equal in diameter to the contact via structures 86 (i.e., peripheral contacts). *See id.*, 67-79. Nishikawa's TAC is not circular shaped, it is a trench shape and does not have a diameter. *See* Nishikawa, Fig. 16.

148. Petitioner asserts that a POSITA would have been motivated to modify Nishikawa because it was "common" to have the peripheral contacts and the TACs the same diameter. Pet. 68. But a POSITA would not have made Nishikawa's TAC (even if circular) the same diameter as the peripheral contacts merely because some devices disclose it.

149. Petitioner and Dr. Lee also assert that a POSITA would have been motivated to form the peripheral contacts and TAC with “the same size to employ a common process (including the hole size in masking steps) when forming the contacts” to save “process time.” Pet. 68-69; Lee Decl., ¶¶ 160-162. Petitioner and Dr. Lee rely on Mushiga, Tessariol, and Nakajima to show the general knowledge of a POSITA includes forming peripheral contacts and TACs at the same time. Pet. 68-69. None of those references teaches what Petitioner asserts, let alone would have motivated a POSITA to form the claimed diameters.

150. For example, Petitioner asserts Mushiga’s TACs 588—inside and outside the stack—are formed at the same time “use[] the same processing steps.” Pet. 68; *see* Lee Decl., ¶ 160. Mushiga does not disclose the timing of forming the cavities that become structures 588. Mushiga (Ex. 1012), Fig. 5, 10:31-58). Mushiga at most discloses the timing of the formation of the cavities in relation to the formation of the conductive layers (146, 246) but this does not teach simultaneous formation of cavities both through and outside the stack. *See id.*, 10:49-57.

151. As another example, Petitioner argues “Nakajima only discloses one step for creating the H1 holes” for forming the “C4 contacts” inside and outside the stack. Pet. 69 (citing Nakajima (Ex.1009), 7:35-8:11, Fig. 2); Lee Decl., ¶ 161. In my opinion, a POSITA reasonably considering Nakajima’s entire disclosure

would have noticed an obvious error in Figure 2 (below with Petitioner’s annotations)—the component in area 100d identified as “C4” should be “C3.”

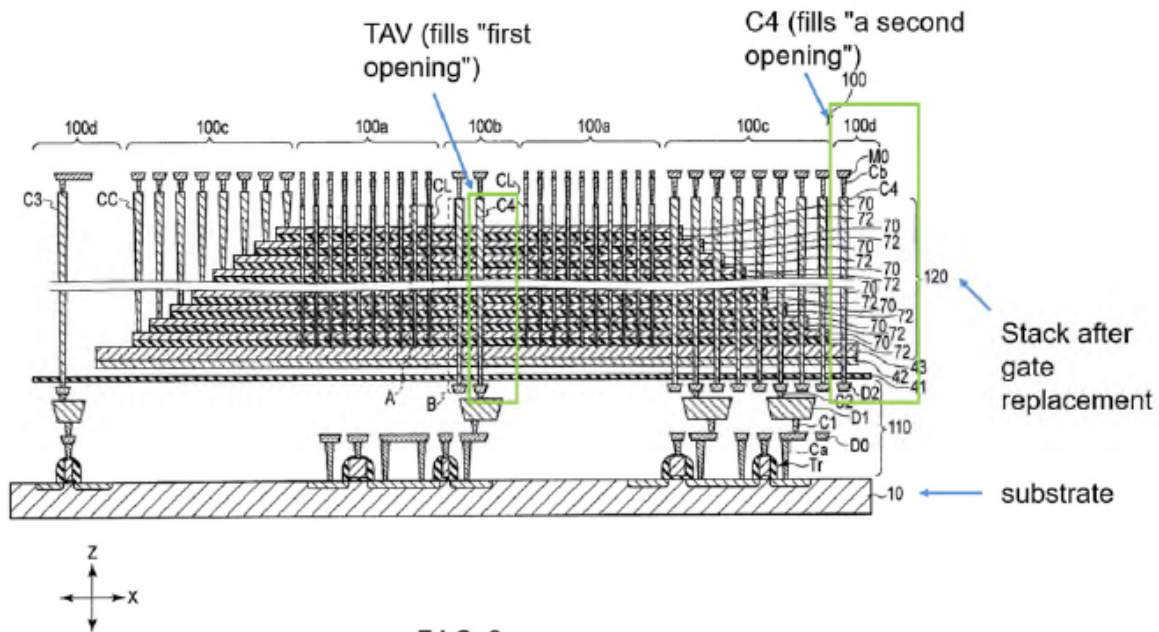
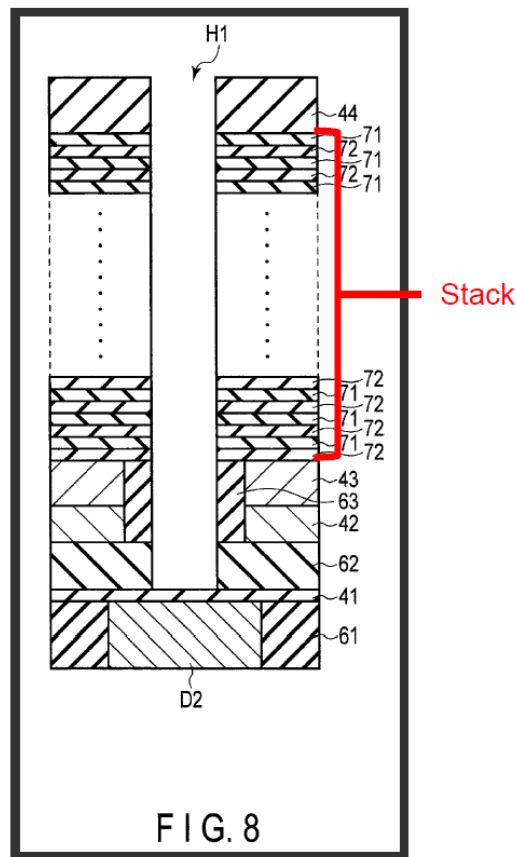


FIG. 2

Pet. 69 (annotating Nakajima Fig. 2); *see* Lee Decl., ¶ 161 (same). The component in area 100d in Nakajima Petitioner identifies as “C4” should be “C3,” which are Nakajima’s peripheral contacts. Nakajima’s disclosure regarding Figure 2 (above) states that “the contacts C3 are provided in the peripheral area 100d,” such that “[a]n upper end of a contact C3 is coupled to an interconnect M0 via a contact Cb.” Nakajima, 4:57-60; *see id.*, 3:59 (disclosing that “area 100d includes contacts C3,” not C4). Nakajima also discloses that “[t]he contacts C4 are provided in the layer stack 120 in the staircase area 100c on the other side and in the contact area 100b,” not the peripheral area 100d. Nakajima, 4:49-51, 3:23-30; *see id.*, Fig. 1. A POSITA would also recognize that there is no textual disclosure in Nakajima that

describes contacts C4 in peripheral area 100d. In view of these disclosures, in my opinion a POSITA would readily understand the “C4” component identified in area 100d of Figure 2 to be an obvious error and mentally substitute the incorrect “C4” for the correct “C3,” as supported by Nakajima’s entire disclosure.

152. Forming “hole H1”—Nakajima’s process Petitioner asserts forms both the peripheral contacts and the TACs—is “formed in the insulation layers ... and the layer stack 120 as shown in FIG. 8.” Nakajima, 7:37-39.



Nakajima, Fig. 8. The “hole H1 penetrates the insulation layers ... and the layer stack 120, to reach the silicon nitride layer 41.” *Id.*, 7:41-43. Thus, Nakajima

discloses that all H1 holes for the C4 structures are etched through the stack, not the periphery.

153. Similarly, Tessariol's disclosure Petitioner and Dr. Lee rely on merely discloses two holes for "dummy structure openings 56 and via openings 54" that are both formed "through the stack," not the claimed TAC through the stack and a peripheral contact outside the stack. Pet. 69 (citing Ex. 1036, [0037], Fig. 9); Lee Decl., ¶ 162 (same). As seen below in Figure 9, Petitioner pointed to the dummy-structure openings 56 (blue) and via openings 54 (green) that are both formed through the stack (red box):

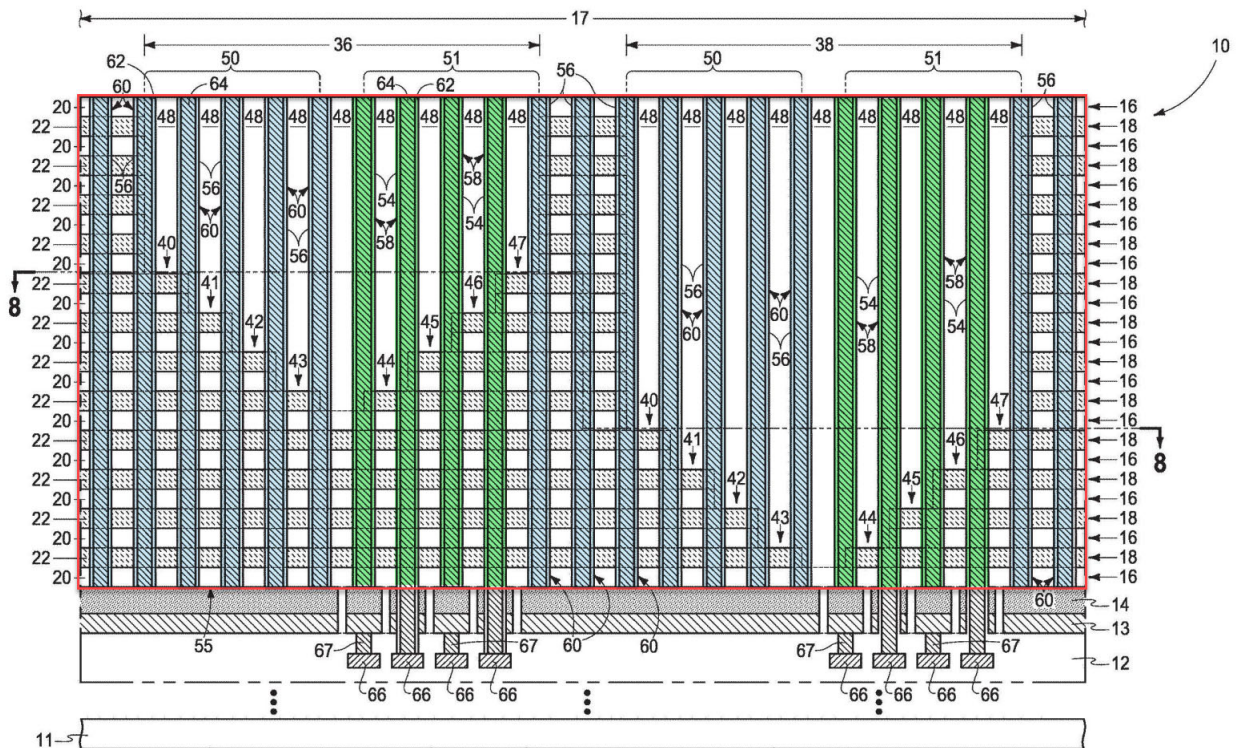
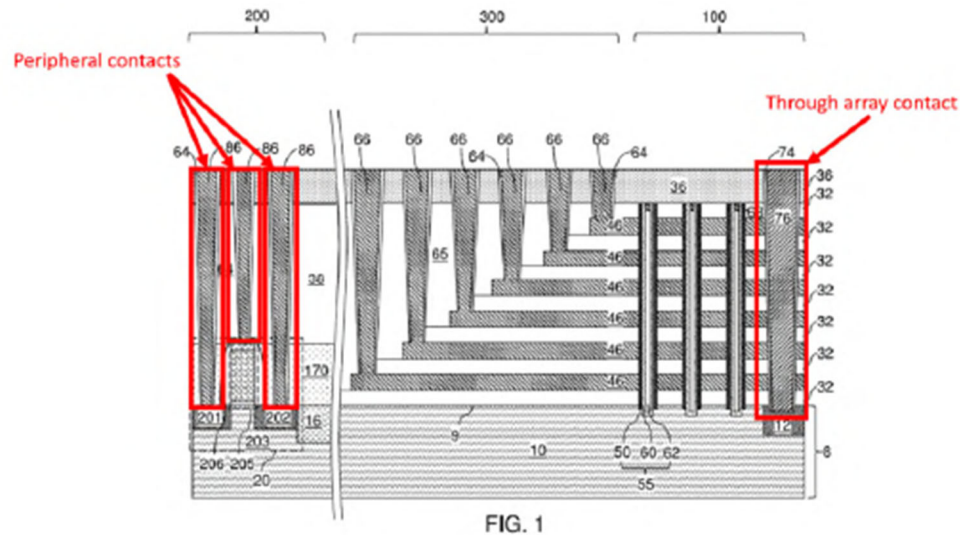


FIG. 9

Ex. 1036, Fig. 9 (annotated); see Pet. 69-70 (citing Ex. 1036, [0037], Fig. 9).

154. Thus, these figures do not establish that a POSITA would have been motivated to form peripheral contacts and TAC with “the same size to employ a common process (including the hole size in masking steps) when forming the contacts” to save “process time.” Pet. 68-70.

155. Dr. Lee argues a “POSITA would have been motivated to make the TAC and peripheral contacts the same size to employ a common process (including the hole size in masking steps)” because this “can save considerable process time because it involves simply employ[ing] a common size for the holes in a pattern.” Lee Decl., ¶ 162. In my opinion, a POSITA would not have used a “common process” (and thus would not save processing time) for forming Nishikawa’s TAC (even if circular) and its peripheral contacts because of structural differences in the regions for forming Nishikawa’s peripheral contacts and TAC. In Nishikawa, the backside contact via contacts 76 (TAC) and the contact via structures 86 (peripheral contacts) are in different regions of the memory device and etch through different structures.



Pet. 67 (annotating Nishikawa, Fig. 1). The contact via structures 86 are formed by etching the dielectric material 38 and planarization dielectric layer 170, while the contact via structures are formed in openings that etch through the stack of alternating, varying materials. *See* Nishikawa, 6:8-28 (dielectric materials), 7:4-15 (describing different materials for insulating layers 32 and sacrificial material layers 42). Even if the peripheral contact and TAC had the same diameter, etching processes generally etch different materials at different rates. Because Nishikawa's TAC and peripheral contacts form in spaces etched through different materials, a POSITA would not have used a common process, including etching forming the openings at the same time, as Petitioner argues. *See* Pet. 70. Nor would a POSITA have used the same etch chemistries, as Petitioner asserts. *See id.*

156. It is my opinion that forming TACs and peripheral contacts of the same diameter (i.e., a circular feature) in different parts of a stack is complex, not

unusually simple. As discussed above, the processes for forming openings in a stack, including TACs are complex because it is harder to maintain a continuous etch rate and a consistent profile in the channel hole, which directly implicates controlling for the claimed diameters. *See supra* ¶¶ 71-73. This is especially true when trying to control etching through different materials—one through the stack and one outside the stack. Ex. 2023, 4, Figure 1 (describing contacts etched outside of the stack as part of “some of the most challenging and critical deposition and etch processes”); *id.*, 6 (stating “[d]eep etch[ing] on these multilayer stacks can push the limits of physics to achieve uniformity from top to bottom.”).

XII. CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on November 17, 2025 in Arden Hills, Minnesota.

Stephen Campbell

Stephen Campbell