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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

- - - - - x

MICRON TECHNOLOGY, INC.

Case IPR2025-00034

v. :

YANGTZE MEMORY TECHNOLOGIES : U.S. Patent No.

COMPANY, LTD., : 10,879,254

Patent Owner. :

- - - - - X

Deposition of JACK C. LEE, Ph.D.

Conducted Virtually

Wednesday, July 30, 2025

10:01 a.m. EDT

Job No.: 591824

Pages 1 - 75

Reported by: Debra A. Whitehead

1 Deposition of JACK C. LEE, Ph.D., conducted
2 virtually.

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5 Pursuant to notice, before Debra Ann Whitehead,
6 E-Notary Public in and for the Commonwealth of
7 Virginia.

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A P P E A R A N C E S

ON BEHALF OF PETITIONER:

JING LUO, ESQUIRE

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Menlo Park, California 94025-1015

(650) 614-7400

ON BEHALF OF PATENT OWNER:

RICHARD LOWRY, ESQUIRE

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Washington, DC 20004

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ALSO PRESENT:

STEVE CAMPBELL

DAVID MIELCAREK, A/V Technician

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C O N T E N T S

EXAMINATION OF JACK C. LEE, Ph.D.	PAGE
By Mr. Lowry	5

EXHIBITS MARKED IN TODAY'S SESSION

(None marked)

EXHIBITS MARKED IN PRIOR SESSIONS

(Not attached)

DEPOSITION EXHIBIT	PAGE
Exhibit 1003	12
Exhibit 1005	32

1 P R O C E E D I N G S

2 JACK C. LEE, Ph.D.,

3 having been duly sworn, testified as follows:

4 EXAMINATION BY COUNSEL FOR PATENT OWNER

5 BY MR. LOWRY:

6 Q Good morning, Dr. Lee. My name is Rich
7 Lowry. Very nice to meet you. Thank you for
8 being here today.

9 A Nice meeting you.

10 Q Can you please state your full name, for
11 the record.

12 A Yes. Jack C. Lee.

13 Q And can you please state your home
14 address, for the record.

15 A Yes. It is 5803 West Loop Cove, Austin,
16 Texas, 78731.

17 Q And where are you right now?

18 A I am at that address.

19 Q And my understanding is you have been
20 deposed multiple times.

21 Is that right?

22 A Yes.

1 Q And in this case today you are being
2 deposed because you gave a declaration in an IPR
3 proceeding.

4 Is that correct?

5 A Yes.

6 Q Now, I'm going to go over some ground
7 rules about deposition basics just to refresh your
8 recollection, if that's okay with you?

9 A Yes.

10 Q You understand that your testimony today
11 is under oath and under penalty of perjury?

12 A Yes.

13 Q You understand that you are under the
14 same obligation to tell the truth as if you were
15 testifying before a judge and jury?

16 A Yes.

17 Q We have a court reporter here, and it's
18 important that she be able to transcribe your
19 answers. So can you try to provide verbal answers
20 to my questions?

21 A Yes.

22 Q If you don't understand or are confused

1 by any questions, please let me know so I can try
2 to rephrase it. Okay?

3 A Yes.

4 Q And your attorney may state an objection
5 to the form of some questions, but unless your
6 attorney instructs you not to answer, you still
7 need to answer the question.

8 Do you understand?

9 A Yes.

10 Q And during the deposition you're not to
11 communicate with your counsel while we are on the
12 record, and this includes verbal and nonverbal
13 cues, as well as electronic messages or means
14 thereof.

15 Do you understand?

16 A Yes.

17 Q Is there any reason that you cannot
18 provide full and truthful testimony today?

19 A No.

20 Q Now, when I reference "this case" or
21 "this IPR," I'm referring to IPR2025-00034. Okay?

22 A Yes.

1 Q And when I refer to "the '254 patent," I
2 am referring to U.S. Patent Number 10,879,254 at
3 issue in this IPR. Okay?

4 A Yes.

5 Q And I'll to try to take breaks every
6 hour. But if at any time you need a break, please
7 don't hesitate to ask.

8 A Okay.

9 Q But if I have asked you a question,
10 please answer it before we take that break.

11 Is that okay?

12 A Yes.

13 Q Now, based on what I can see, it looks
14 like you don't have any materials with you today.

15 Is that correct?

16 A I have a hard copy of my declarations
17 that -- so I have that. I might refer to it.

18 This is a clean copy.

19 Q You don't have any other notes or
20 documents in front of you?

21 A No.

22 Q Do you have your phone in front of you?

1 A No.

2 Q Do you have any other applications open
3 on your computer?

4 A No.

5 Q Is there anyone else in the room with
6 you?

7 A No.

8 Q Can you agree not to take your cellphone
9 out and look at it at any time during the
10 deposition today?

11 A Yes.

12 Q And can you also agree not to open any
13 document or file on your computer during your
14 deposition, aside from those provided through the
15 Zoom software?

16 A Yes.

17 Q And can you also agree not to access the
18 internet during the deposition?

19 A Yes.

20 Q Great. Now, what did you do to prepare
21 for your deposition today?

22 A I reviewed my declaration, the file

1 histories of the '254 patent, the '254 patent, and
2 all the prior art that I cited in my declaration.
3 And I also discussed with my counsel.

4 Q And who did you meet with when you refer
5 to "my counsel"?

6 A Jing Luo here with us and another
7 attorney Jason -- I -- let's see. Sorry.

8 Q Was it another attorney at Orrick?

9 A Yeah. Is --

10 Q Okay.

11 A It will come to me. Jason Lang, sorry.

12 Q And how long were the meetings?

13 A How long was?

14 Q How long were the meetings?

15 A I don't recall. We have several meetings
16 in the last couple of weeks.

17 Q And were those meetings in person, video,
18 or by phone?

19 A Videos, Zoom call.

20 Q Were in-house lawyers from Micron
21 present?

22 A No.

1 Q Was anyone who isn't a lawyer at the
2 meeting?

3 A No; just those two attorneys that I
4 mentioned.

5 Q Besides those attorneys, have you
6 discussed this case with anyone else?

7 A No.

8 Q Since you signed your declaration that
9 you submitted in this IPR, have you changed any of
10 your opinions?

11 A Yes.

12 Q Can you explain which opinions you've
13 changed?

14 A Yes. May I have my declaration or may I
15 refer to my declaration here? Can you upload the
16 declaration?

17 Q Yes. I'll do that right now. And you
18 can refer to your clean copy that's in front of
19 you.

20 A Uh-huh.

21 Q And it looks like Zoom is being
22 challenged. There it goes.

1 A Oh, I see it now.

2 Q So I'll just repeat the question. Can
3 you explain which opinions you've changed?

4 A Yeah, I'm going to open --

5 Q Okay.

6 A -- the declaration, your electronic copy
7 as well.

8 (Exhibit 1003, previously marked, not
9 attached.)

10 A Okay. On Page 69 of my declaration
11 regarding Claim 8, I found a typographical error
12 in Paragraph 135. In my first sentence.

13 I first note that the '254 patent
14 described using isotropic etch. Sorry. An
15 isotropic etch because the dielectric material on
16 the bottom will be thicker than on the side wall.
17 And the typographical error is that the bottom
18 dielectric liner should have been -- the correct
19 word is thinner than the side wall liner.

20 And I also corrected this error in my
21 second declaration for the same patent, for the
22 '254 patent.

1 Q Anything else?

2 A That's the only one I like to point out.

3 There's one other one, but that's not --
4 that's not critical.

5 Q Okay. What's the other thing in your
6 declaration that you'd like to change?

7 A On Page 43, on the top of that page is
8 Figure 7 from Exhibit 1005. There is a side
9 saying point to Region 120, and it says, Stack
10 after gate-replacement.

11 Do you see that?

12 Q Yes.

13 A And let's see. And it should have
14 been -- it should have been said, Stack before
15 gate-replacement.

16 So those are the two typographical error
17 that I found so far in my declaration. It does
18 not -- these typographical error does not change
19 my opinion.

20 Q Can you explain on Page 43 of your
21 declaration why "stack after gate-replacement" is
22 incorrect and should be changed to "stack before

1 gate-replacement"?

2 A Yes.

3 You notice that the layers are 71 and 72.

4 In the previous page it says that 71 is

5 sacrificial layers, and 72 are insulating layer.

6 Okay? Then sacrificial layers are removed during

7 the gate-replacement process and replace it with

8 conductive layer 70. Okay?

9 And the fact that in Figure 7 you still

10 have the sacrificial layer means that the

11 gate-replacement process had not been done.

12 Q Dr. Lee, how much time have you put into
13 this IPR so far?

14 A I don't -- I have not counted the number
15 of hours.

16 Q Can you give a ballpark estimate?

17 A Not really, because we spent -- I spent a
18 lot of time working with counsel to discuss the
19 arguments formed for the IPR. That was back in
20 September, October time frame of 2024.

21 So, and then my counsel and I together
22 draft the report, the declaration. So I don't

1 know how many hours -- I don't recall how many
2 hours that I spent on writing the declarations.

3 And then in preparation for the
4 depositions, I also review, as I mentioned to you,
5 reviewed the declarations, the patent, the file
6 histories, and all the prior arts and other
7 exhibits listed in my declarations.

8 So I don't recall how many hours total.
9 If you ask me to ballpark, I will say probably
10 close to, if not more than, hundred hours. I
11 don't know.

12 Q And who initially drafted the text of
13 your declaration?

14 A I will say that all of the counsel and I
15 work on it together. I provide certain part of
16 the declarations for the first draft, and counsel
17 provide some other parts.

18 Of course I'm not a lawyer, and this is a
19 legal document. And so a lot of the legal
20 arguments I would need the help from counsel to
21 write those sections. But much of the technical
22 issues, technical arguments, I -- first of all,

1 like I said, we discuss that prior to the first
2 draft, and we work on the first draft together.

3 Q You said that you provided certain parts
4 of the declarations for the first draft. Which
5 parts did you write for the first draft?

6 A I don't recall exactly, but a lot of the
7 technology description, for example, technology
8 background section and state of the art, I
9 provided that.

10 Now, of course prior to that there are
11 other IPRs related to this case that I worked on.
12 So much of the technology background sections I
13 wrote previously and I imported into this IPR.
14 But so that sections I probably -- I'm the one
15 that developed that sections.

16 And my qualification, of course, I
17 provide that. And within the analysis I provide
18 some sentences to describe some of the technology,
19 description of the technology; for example, what
20 is isotropic etch, what is anisotropic etch, what
21 is -- I believe there's a section on some
22 description on ALD, atomic layer deposition. So I

1 describe, I provide that section.

2 So there's various -- it's hard to say
3 which part it is, because in each section there's
4 some technology highly -- some technology
5 descriptions, so I provide sentences describing
6 that.

7 Q And when did you first start working with
8 Micron on these series of IPRs?

9 MS. LUO: Objection. Form.

10 A Could you clarify the question? I'm
11 sorry.

12 Q Well, yes. You said that you have been
13 working with Micron on this IPR and before this,
14 other IPRs related to this case.

15 And I'm asking you when did you begin to
16 work with Micron on these series of IPRs?

17 MS. LUO: Objection. Form.

18 A I was engaged on this case in January
19 2024.

20 Q And can you confirm that the declaration
21 I uploaded is correct for this proceeding?

22 A It appears to be. At least the number of

1 pages, and the last page seems to be, and the
2 first page are correct.

3 Q Let's go to Section 3 of your
4 declaration, which is on Page 7.

5 Please let me know when you're there.

6 A Page 7? Yes.

7 Q Your declaration cites many exhibits in
8 Paragraph 17. Right?

9 A Yes.

10 Q Did you review all these exhibits before
11 your deposition?

12 A Yes. As much as I can.

13 Q Did you review any other documents to
14 refresh your recollection about this declaration,
15 besides the ones listed in the chart on Pages 8
16 through 10 of your declaration?

17 A I don't think so.

18 Q And did you consider any other materials
19 in formulating your opinions that are not provided
20 in the chart of Paragraph 17?

21 A Well, in Paragraph 17, in addition to the
22 chart, as I indicated in the beginning of the

1 Paragraph 17, Exhibit 1001, which is the patent,
2 the '254 patent; and the prosecution history,
3 which is the Exhibit 10 -- 1002, so those are the
4 two additional document that I review, in addition
5 to what's listed in that chart.

6 Q And who provided the prior art for your
7 analysis in your declaration?

8 A When we -- when counsel and I discussed
9 this IPR, we work together to find -- to find
10 these -- these prior art. And some of the
11 documents, for example Exhibit 1008, Exhibit 1014,
12 are ones -- are the ones that have been cited in
13 other IPR.

14 And I know that -- I believe those are
15 the ones that I found, because I have access to
16 the library at the university. And, but that was
17 some time back.

18 But to answer your question, both counsel
19 and I find these prior arts together.

20 Q Let's talk about your background for a
21 minute.

22 You've taught classes relating to 3D NAND

1 technology.

2 Is that correct?

3 A Yes.

4 Q And which classes?

5 A I have a -- I teach -- I have taught a
6 graduate class on semiconductor device fabrication
7 and design. Actually, I touch on those also in my
8 undergraduate level class.

9 I also taught and still teaching short
10 courses in industry, and those are the courses
11 that focus on semiconductor devices and
12 technology, and fabrication and design.

13 And in those courses I covered, among
14 other things, 3D NAND technologies.

15 Q And you've also encountered 3D NAND
16 memory in your research.

17 Is that right?

18 A That's right.

19 Q And can you explain which research you
20 conducted that involved 3D NAND memory?

21 A Well, we have -- you know, I work with my
22 student who are my research assistant, and we look

1 at specific issues related to 3D NAND; for
2 example, etching technology, deposit of
3 dielectric, dielectric interface with conductors.
4 So various different issues related to 3D NAND
5 flash memory have been researched in my group
6 together with my graduate students who are my
7 research assistant.

8 Q I don't have a background in that
9 technology, but it sounds complicated.

10 A I don't know what you mean by
11 "complicated." The 3D NAND process have been
12 around for many years and have been routinely
13 fabricated by many companies. And so I don't --
14 you know, obviously it requires a team effort to
15 fabricate the entire chip.

16 But just like, you know, from my point of
17 view I look at what you guys do, I thought that
18 that's very complicated, being a lawyer, have to
19 learn all those legal procedures.

20 So perhaps for you it might be -- it
21 might seem complicated, but for a person of
22 ordinary skill in the art at the time of the

1 alleged invention, you know, it's not -- I don't
2 think they would view that as complicated.

3 Q Now, how long does it take to develop a
4 new 3D NAND product?

5 MS. LUO: Object to form.

6 A I don't know what you mean by "new 3D
7 NAND product."

8 Obviously, 3D NAND has been around for
9 many -- for many years. And so in general there
10 is technology advances, the dimension becomes
11 smaller. And so, you know, it's basically -- it's
12 not, like, completely new concept.

13 So I'm not sure if I understand your
14 question.

15 Q Well, have you followed the history --
16 let me strike that.

17 Are you familiar with the history of 3D
18 NAND development?

19 A Yes, I have discussed -- I mean, I had
20 taught how -- in my course how 3D NAND, how the 3D
21 NAND works. So, but that is not something
22 specifically I prepared to testify in terms of,

1 you know, how long does it take and -- but, so --
2 sorry.

3 Q Well, my question is, from one generation
4 of 3D NAND technology to the next generation of 3D
5 NAND technology, about how long does that take to
6 develop the new generation?

7 MS. LUO: Objection. Form.

8 A So I don't -- you know, I work with -- I
9 know a lot of people to -- in the industry. And
10 so I -- but, you know, these are -- these
11 information are proprietary. How long it takes, I
12 don't think they disclose -- disclose that.

13 In general, you know, it varies from one
14 company to another, so. But I don't recall how
15 many -- how many months. And it -- you know, it
16 depends on the technology. It depends on whether
17 it was a one first generation or second
18 generation. So, but, you know, it's not -- these
19 are all well-planned. So --

20 Q Sitting here today -- sorry. I didn't
21 mean to interrupt. Go ahead.

22 A No. You're -- again, these are not --

1 for a person of ordinary skill in the art,
2 understanding these technology and working in this
3 technology is not as complicated as you might
4 think.

5 Q So that's your testimony sitting here
6 today, that the research you've conducted
7 regarding 3D NAND technology and the courses you
8 teach regarding 3D NAND technology, and the
9 development of these generations of technology is,
10 quote, "not as complicated as you might think."

11 Is that right?

12 MS. LUO: Objection. Form.

13 A Again, is what -- how complicated it is,
14 is depending on the perspective. Right?

15 For someone who's not in the field of
16 semiconductor, they might think that it is very
17 complicated. For someone who's in the
18 semiconductor, it might be easier. For someone
19 who's right in the field of NAND technology, 3D
20 NAND technology, you know, is probably they
21 wouldn't view that as complicated. And so for
22 somebody -- someone as I describe, a person of

1 ordinary skill in the art, would see that.

2 Of course, these are not, you know, as
3 simple as baking a cake, but it's not as
4 complicated as you make it sound like.

5 Q So if I went and pulled a textbook that
6 covered 3D NAND, it would describe the technology
7 as not very complicated.

8 Is that accurate?

9 MS. LUO: Objection. Form.

10 A I don't know which textbook are you
11 referring to. And so I -- it's not something
12 that -- you know, that's for me to answer your
13 hypothetical question. And it's not something
14 specifically I prepared to testify about, you
15 know, what textbook would say.

16 But again, depending on who you talk to,
17 the complexity may seem a lot for one person who
18 is outside the field, and is not so much for a
19 person of ordinary skill in the art, especially
20 those working in 3D NAND technology.

21 Q So sitting here today, is it your
22 testimony that it's not possible for a POSITA to

1 characterize 3D NAND technology as complicated?

2 MS. LUO: Objection. Form.

3 A I'm not sure -- can you repeat that
4 again?

5 Q Yes. Sitting here today, is it your
6 testimony that it's not possible for a
7 POSITA to characterize 3D NAND technology as
8 complicated?

9 MS. LUO: Objection. Form.

10 A Well, I think that a lot of the
11 technologies, processes involved in 3D NAND, for
12 example forming the dummy gates and the recesses
13 that discuss in the patent and in my IPR, have
14 been well-known for a long time. So I wouldn't
15 for -- I wouldn't characterize that those
16 processes are complicated.

17 Q All right. So, Dr. Lee, that's not
18 responsive to my question. I think I'm going to
19 repeat my question and ask you to answer it
20 directly.

21 A Okay. Sorry about that.

22 Q That's okay.

1 A I apologize.

2 Q Sitting here today, is it your testimony
3 that it's not possible for a POSITA to
4 characterize 3D NAND technology as complicated?

5 MS. LUO: Objection. Form.

6 A You are saying that is it possible for a
7 POSITA to characterize the 3D NAND processes as
8 complicated. Or conversely, that it is not
9 possible for a POSITA to characterize 3D NAND
10 technology as complicated.

11 Is that what you mean?

12 Q Yes, you can answer that question.

13 A Let me -- in one section I describe what
14 a POSITA is. Right? And that is in Page 14, on
15 Paragraph 34 to 38.

16 To answer your question, I would think
17 that a person with the level of skill in the art
18 that I describe in those paragraphs would not
19 viewed 3D NAND processes as complicated. Now, I'm
20 not sure how to answer -- you know, obviously if
21 you ask a hundred people with those
22 qualifications, is it possible that one person

1 might feel that, Oh, it is complicated, I don't
2 know. I don't know how, you know -- perhaps you
3 have asked someone with those skills and you say,
4 Hey, is this complicated? I don't know, I can't
5 guarantee what the guy would say.

6 But in my mind, in my opinion, a person
7 with such level of skill in the art as described
8 in that Section 5 of my IPR, that person, that
9 POSITA, would not have viewed 3D NAND as
10 complicated, in your -- in your word.

11 And I can't guarantee that if you ask --
12 you know, I don't know who you ask, whether that
13 person would say that it is complicated or not
14 complicated.

15 But in my opinion, that person of
16 ordinary skill in the art with the skill described
17 in Section 5 of my IPR, would not view 3D NAND
18 technology and 3D NAND processes, such as forming
19 dummy gates and forming recesses, as complicated,
20 because it has been -- those processes have been
21 well-known for a long time.

22 Q Let's turn to Page 40 of your

1 declaration.

2 Let me know when you're there.

3 A Okay.

4 Q You see the heading B, which states,
5 "Ground 1: Nakajima In View of the Knowledge of a
6 POSITA Render Obvious Claims 1 Through 15, 17
7 through 18, and 20"?

8 A Yes.

9 Q So you rely on either Nakajima or the
10 knowledge of a POSITA to disclose every limitation
11 of those identified claims.

12 Is that right?

13 A I don't think what you said characterized
14 the heading and what my opinion is in Section B.

15 You said that I relied on Nakajima or the
16 knowledge of the POSITA in rendering obvious in
17 the claims listed in the heading. That's not what
18 I said, and that's not my opinion.

19 My opinion is that for Section B, which
20 is Ground 1 -- I think that's the only ground --
21 that Nakajima in view of the knowledge of a POSITA
22 renders obvious Claims 1 through 15, 17 through

1 18, and Claim 20.

2 Q I think -- let me try to restate the
3 question.

4 You relied on Nakajima to allege that the
5 challenged claims are obvious. Right?

6 A I relied on Nakajima in view of the
7 knowledge of a POSITA in rendering obvious in the
8 challenged claim -- claims.

9 Q And you haven't offered an opinion that
10 these claims of the '254 patent are anticipated by
11 the prior art. Right?

12 A I don't think so.

13 Q And you don't have any obviousness
14 allegations that are based solely on prior art
15 patents or publications. Right?

16 MS. LUO: Object to form.

17 A Can you repeat that question, please?

18 Q Sure. You don't have any obviousness
19 allegations that are based solely on prior art
20 patents or publications. Right?

21 MS. LUO: Object to form.

22 A Again, my arguments in my IPR is that

1 these claims are rendered obvious based on
2 Nakajima prior art in view of the knowledge of a
3 POSITA.

4 I have not offered an opinion that these
5 claims are rendered obvious solely on a prior art,
6 if that is your question.

7 Q Yeah, I mean, a simple yes or no will do,
8 Dr. Lee.

9 The question is, you don't have any
10 obviousness allegations that are based solely on
11 prior art patents or publications. Right?

12 MS. LUO: Object to form.

13 A No, I have not offered an opinion
14 regarding obviousness solely on a certain prior
15 art.

16 Q Okay. Can we go to Page 40 of your
17 declaration, please.

18 A It's the same page that you --

19 Q Sorry, 46. I apologize.

20 A Forty-six.

21 Q And I'm uploading Exhibit 1005 to this
22 proceeding, which is Nakajima.

1 (Exhibit 1005, previously marked, not
2 attached.)

3 MR. LOWRY: Could we go off the record
4 for a second, Debbie, please.

5 (A recess was taken.)

6 BY MR. LOWRY:

7 Q Dr. Lee, please turn to Page 46 of your
8 declaration.

9 A Forty-six.

10 Q And you can see I've uploaded Exhibit
11 1005, which is the Nakajima reference.

12 A Yes.

13 Q Are you familiar with this reference?

14 A Yes.

15 Q Do you see Limitation 1 C on Page 46 of
16 your declaration?

17 A Yes.

18 Q And this limitation recites, "Forming a
19 first opening extending vertically through the
20 stack."

21 Right?

22 A Yes.

1 Q And to address this limitation, you refer
2 to Nakajima's disclosure regarding contact C4.

3 Right?

4 A Where are you reading?

5 Q Paragraph 88, for example, says, "As seen
6 in the final memory device (Figure 2), Nakajima
7 discloses Contact C4."

8 A Yes.

9 Q So to address this limitation, you refer
10 to Nakajima's disclosure regarding Contact C4.

11 Right?

12 A That is correct.

13 Q And are you familiar with how Nakajima's
14 Contact C4 is formed?

15 A Yes.

16 Q Can you explain it, please.

17 A Well, as I describe in Paragraph 89, To
18 form C4, Nakajima first etched -- etches a first
19 opening, what he calls Hole H1, capital H one,
20 extending vertically through the stack (120). And
21 I cited a section in Nakajima in quotations in 89.

22 Do you want me to read that?

1 Q That's not necessary.

2 A Okay.

3 Q Nakajima discloses that Hole H1 is formed
4 by reactive ion etching, or RIE. Right?

5 A Yes.

6 Q And what is reactive ion etching?

7 A And I think -- okay. I thought I
8 have ...

9 As I discuss in my declaration at several
10 places, a reactive ion etch is considered to be an
11 anisotropic etch, which is meaning that it's a
12 directional etch. It is a very common etch that's
13 been around for many years. It require a
14 low-pressure plasma, and reactive species are
15 injected into this chamber of reactive -- of --
16 with the low -- in general low-pressure plasma.

17 And the etching occurs when you have
18 chemical reaction; for example, fluorine coming
19 from some gas, CF₄ or SF₄, or SF₆, that the
20 fluorine in those gas will react with silicon on
21 the substrate, for example, to form silicon
22 tetrafluoride, SF₄.

1 And in addition to the chemical reaction,
2 there's also a physical sputtering effect, meaning
3 there's an ion bombardment. And the volatile
4 byproduct of this reaction is pumped away.

5 So in essence, that's what reactive ion
6 etch is. Of course, there's a lot more detail
7 that I skip in some. In short, it's a etching
8 process that etches certain structure in the wafer
9 under low-pressure plasma using reactive ion etch.
10 And the chamber is bias in such a way that it also
11 involve ion bombardment. And it is due to this
12 ion bombardment that generally reactive ion etch
13 is considered what is called the anisotropic etch,
14 meaning that it is a directional etch.

15 Again, this is a very brief description.
16 And, you know, in my class I spend half an hour to
17 45 minutes to discuss the details of reactive ion
18 etch.

19 Q Okay. And the formation of Hole 1, or
20 Hole H1, is shown in Figure 8 of Nakajima. Right?

21 A This is -- I'm going back to -- is it
22 Page 46? Right?

1 Q Yes, that's correct, 46 of your
2 declaration, or Nakajima at Figure 8.

3 A Yes. So you're asking -- your question
4 is whether the hole -- can you repeat the question
5 please?

6 Q Sure. The formation of Hole H1 is shown
7 in Figure 8 of Nakajima. Right?

8 A That's correct.

9 Q So what happens next in the Nakajima
10 process, after Hole H1 is formed?

11 A After the Hole H1 is formed, as I
12 describe in Paragraph 91, that the silicon oxide
13 layer 81 as described and shown in Figure 9 is
14 formed on the inner surface of the layer stack
15 120, and the isolation layers 46 -- 44, 62, and 63
16 in Hole H1 and on the silicon layer -- silicon
17 nitride layer 41 as shown in Figure 9.

18 So in short, that after the Hole H1 is
19 etched, a silicon oxide layer 81 is conformably
20 formed along the bottom and the side surface of
21 the Hole H1.

22 Q What does Nakajima show for the next step

1 in Figure 10?

2 A So in Figure 10 shows that metal -- so
3 first of all, Nakajima -- hold on. Let me see.
4 Sorry.

5 So in Figure 10 Nakajima first removes
6 the bottom portion of the spacers, which is
7 relating -- which relates to the subsequent
8 dependent claims. In other words, that the bottom
9 part of the silicon oxide layer 81 has to be
10 removed in order for the subsequent conductive
11 layer to be connected to the underlying regions D2
12 as shown in Figure 11.

13 Q And the bottom portion of silicon oxide
14 layer 81 is removed by reactive ion etching.

15 Right?

16 A I believe so, yes.

17 Q And I believe you said this earlier, but
18 I'm just trying to understand this. Is reactive
19 ion etching is anisotropic. Right?

20 A Is anisotropic in general.

21 Q Okay.

22 A Anisotropic meaning directional etch, as

1 opposed to isotropic, which is nondirectional, it
2 etches in all directions.

3 Q And after the bottom portion of the
4 dielectric is removed by reactive ion etching, the
5 resulting sidewalls of silicon oxide layer 81 are
6 flat and vertical. Right?

7 A So 81 was deposit as shown in Figure 9 on
8 the side wall, as well as on the bottom of that
9 Hole H1.

10 And the subsequent etching removes the
11 bottom portion only of the layer 81 on the bottom
12 of the Hole H1. So what you have left is
13 so-called the dielectric spacer, meaning is
14 silicon oxide layer on the side wall of the Hole
15 H1.

16 Q Okay. Dr. Lee, I don't think that
17 answered my question. I'll just repeat the
18 question. Please answer it directly.

19 After the bottom portion of the
20 dielectric is removed by reactive ion etching as
21 shown in Figure 10 of Nakajima, the resulting
22 sidewalls of silicon oxide layer 81 are flat and

1 vertical. Correct?

2 MS. LUO: Object to form.

3 A I don't know what you mean by "flat and
4 vertical." But the remaining SiO₂ layer, silicon
5 oxide layer 81, is on the side wall of the Hole
6 H1. So the side wall is -- of the hole is,
7 indeed, vertical. When you say "flat," do you
8 mean with the same thickness along the side wall?
9 If that's the case, in general yes.

10 Q And what happens next in Figure 11 after
11 removal of the bottom portion of the dielectric?

12 A After the removal of the dielectric, that
13 Nakajima discloses forming a through array
14 contact, capital A, capital -- sorry, TAC, capital
15 T, capital A, capital C. And what Nakajima
16 referred to as C4, that extend vertically through
17 the stack by depositing a conductive layer, what
18 Nakajima label as metal layer 82, over the spacer
19 oxide layer 81 in the first opening, what Nakajima
20 refer to as Hole H1.

21 Q Okay. So I'm looking at Figure 11 on
22 Page 50 of your declaration.

1 Do you see that?

2 A Yes.

3 Q Okay. Now, the sides of metal layer 82
4 are formed such that they touch silicon oxide
5 layer 81. Right?

6 A You mean the side of 82 -- the 82, the
7 metal layer, is touching the side of the side wall
8 oxide layer 81.

9 Is that what you're saying?

10 Q Yes, that's all I'm asking.

11 A Yeah. Yes, as shown in Figure 11.

12 Q Okay.

13 A Eighty-two is in contact with 81.

14 Q And the sides of metal layer 82 in Figure
15 11 are -- they're vertical. Right?

16 MS. LUO: Object to form.

17 A I don't know -- well, are you saying 82?
18 Right?

19 Q Yeah, metal layer 82. Yes, sir.

20 A Yeah, the metal layer 82 is the through
21 array contact, the TAC, region. And it is, as I
22 discuss and describe in my declaration in

1 Paragraph 92, is extended vertically through the
2 stack.

3 Q Okay. Now, the bottom of metal layer 82,
4 that's formed on top -- on the top surface of
5 interconnect D2. Right?

6 A That is -- that is correct. D2 is an
7 interconnect conductor.

8 Q The bottom of metal layer 82 is
9 horizontal, too. Right?

10 MS. LUO: Object to form.

11 A In Figure 11, it shows the axis. X is
12 going from east to west. It is -- you can call
13 that horizontal. And Z is vertical, going from
14 north to south.

15 So as shown in Figure 11, the bottom of
16 82 is parallel to the X axis. So if you call that
17 X axis as horizontal, then the answer to your
18 question is yes, the bottom of 82 is horizontal.

19 Q Now, the top of metal layer 82 touches
20 insulation layer 64, which is formed above it.

21 Right?

22 A Yes, the insulation layer 64, silicon

1 oxide layer.

2 Q And the insulation layer 64 insulates the
3 top surface of the metal layer 82. Right?

4 A At that point as shown in Figure 2 --
5 Figure 11, insulating layer insulate the metal
6 layer 82 from what's above it at this point.

7 Q And the top of metal layer 82 is also
8 horizontal along the X axis. Right?

9 A The layer 82, as I describe in Paragraph
10 92, is the -- is the TAC region C4 is extended
11 vertically through the stack. And so the top is
12 parallel to the X axis. The top of the conductive
13 layer 82 is parallel to the X axis. And if you
14 call X axis is a horizontal, then, yes, the answer
15 to your question is the top of the conductive
16 layer 82 is horizontal.

17 Q Let's turn to your declaration at Page
18 16, specifically at Paragraph 42.

19 Let me know when you're there, please.

20 A Page 16?

21 Q Yes, that's correct, sir.

22 A Yes.

1 Q In that paragraph you state, The other
2 most important -- sorry, "The other most common
3 type of flash memory is NOR flash, but NAND offers
4 a higher integration density and occupies a larger
5 market than NOR flash."

6 Do you see that?

7 A The last sentence. Is that right? Of
8 Paragraph 82?

9 Q That's correct.

10 A Forty-two, I'm sorry.

11 Q Yes, the last paragraph -- sorry, we
12 cannot get this right. The last sentence of
13 Paragraph 42, that's right.

14 A Yes, that's what it says.

15 Q What did you mean here by "higher
16 integration density"?

17 A Well, NAND flash in general is
18 organizing -- organized, you can think of it, that
19 there are many -- in series, what the person of
20 ordinary skill in the art will call their cell
21 connection as series, meaning that there are many
22 cells per string. Whereas NOR flash, the cell

1 connections are in parallel, that in -- such that
2 the NAND flash provide much higher integration
3 density. Meaning that per unit area of the chip,
4 per unit -- some people call that the per unit
5 area of the real estate, there are many more
6 memory cells in NAND flash compared to the NOR
7 flash, which is a lower density architecture.

8 Q Is density an important aspect of
9 designing memory devices?

10 A Yes, density is one of the most important
11 aspect in designing memory, memory devices.

12 Q Can you tell me what affects integration
13 density in memory devices?

14 MS. LUO: Object to form.

15 A Well, there are many factors. Can you
16 repeat the question? What -- what affect the
17 density of the memory device?

18 Q Yeah. So let me just clarify it.

19 Can you tell me what factors impact --
20 impact integration density in memory devices?

21 A Well, there are many factors.

22 First, as I mentioned, what architecture

1 you use, whether it's NAND flash or NOR flash, and
2 since we're talking about 3D NAND here, let's
3 focus on that. Probably the most important
4 determination factor is how many layers of word
5 lines you have. The higher the number of word
6 lines you have, the number of bits per string
7 increases. Right?

8 And -- so number of cell increases when
9 you increase the number of layers in the stack.
10 But in addition, each memory cell can have either
11 1 bit, 2 bit, 4 bits, and 3 bits of memory. So
12 the number of bits per cell also is another factor
13 that affect the overall density.

14 Obviously that over the years the
15 lithography resolution increases. Meaning that
16 what is the smallest line you can resolve on the
17 chip, that dimension decreases dramatically over
18 the years. And so that's called the pitch
19 scaling. So that's -- that also -- that's why we
20 spend so much cost to have a very high resolution
21 for the lithography equipment.

22 In fact, photolithography steps is

1 probably the most expensive steps among the
2 processes. So, of course, the staircase footprint
3 is important. And -- and then you have the CMOS
4 peripheral circuit. Right? Those are the circuit
5 that control the memory informations from the 3D
6 NAND memory array to the outside world. And how
7 that integrate on the chip is important.

8 If the CMOS peripheral circuit is
9 integrated on the side of the array, that's a
10 simpler but less density, because it occupy larger
11 area. Whereas, some technology the CMOS logic
12 circuit is under the array, and so you can see
13 that for a particular chip size. Right? That
14 having the CMOS rather than on the side, that's
15 underneath, that also increases your packing
16 density.

17 So those are the -- some of the factors
18 that affect the density of the -- of the chip.
19 The reason why you want high density is because if
20 there's a low-density chip, it means that for a
21 particular memory size, the chip size will be much
22 larger. And large chip is undesirable because on

1 a given wafer size, let's say a 12-inch wafer, if
2 the -- if the chip size is very large, the number
3 of chips you can put in a wafer is -- would be
4 much less. So the average cost for the chip would
5 be much higher.

6 What's even worse is that even though
7 the -- we spend a lot of money to have avoid
8 contamination and particles inside the clean room
9 and inside the manufacture equipment, it cannot be
10 avoided that you would have some particles.

11 So imagine that the chip size is very
12 small compared with the chip size very large. If
13 you think about it, the number of particles
14 contamination is fixed, even though it's very
15 small.

16 It's like you have a wafer, you throw a
17 bunch of bits up in the air and let it fall down,
18 and each bit, you know, represent -- each particle
19 represent a defect. One defect essentially will
20 kill the chip. So if you have a large -- large
21 chip, the probability of that -- of one particle
22 fall on that chip will be much larger.

1 So that's the reason why we -- that's
2 another reason why we always want to have as high
3 density as possible; for lower cost, higher yield,
4 and at the end, you know, with lower cost per bit,
5 higher yield, the company would -- would make a
6 lot more money per chip.

7 So to -- I'm sorry, that's a long, long
8 answer. It's basically those are the key factors
9 that affect the density of a memory chip.

10 Q Dr. Lee, and you'd agree that 3D NAND
11 memory designs attempt to achieve a very dense
12 memory array. Right?

13 MS. LUO: Object to form.

14 A I believe I -- my previous -- my answer
15 to your question right before that is that, yeah,
16 one of the goal of designing 3D NAND is to achieve
17 high density.

18 Q And another reason for creating a dense
19 memory array is because the denser the array, the
20 less silicon you need to create a given memory
21 size.

22 Isn't that fair?

1 A Yes. I think that's what I said before
2 too.

3 Q And you agree with the statement that a
4 large focus of design efforts for memory resolves
5 around fabricating a dense array. Right?

6 MS. LUO: Object to form.

7 A Can you repeat the question, please.

8 Q Sure. You'd agree that a large focus of
9 design efforts for memory revolves around
10 fabricating a dense array. Right?

11 MS. LUO: Object to form.

12 A That is one of the -- one of the goals of
13 designing a memory chip, is to achieve higher
14 density.

15 Q Okay. Let's go to Page 10 of your
16 declaration, please.

17 A Hold on.

18 Yes.

19 Q Do you see the section 4 titled,
20 Understanding of the Law?

21 A Yes.

22 Q In this section, which extends from Page

1 10 to Page 14, you describe your understanding of
2 obviousness. Right?

3 A Are you referring to Paragraph 20?

4 Q So I'll just repeat it just for clarity.

5 In Section 4, titled, Understanding the
6 Law, which extends from Paragraph 18 to Paragraph
7 33 of your declaration, within that section you
8 describe your understanding of obviousness.

9 Right?

10 A Yes.

11 Q Now, Dr. Lee, there is no paragraph
12 describing when is proper to rely on the knowledge
13 of a POSITA for obviousness in this section, is
14 there?

15 MS. LUO: Object to form.

16 MR. LOWRY: Counsel, what's your
17 objection based on?

18 MS. LUO: Your question is, there's no
19 paragraph describing when it is proper. I don't
20 understand what you mean by proper to rely on the
21 knowledge of a POSITA. There are -- I don't want
22 to testify, but there are obviously paragraphs

1 here that explain how a POSITA would view prior
2 art in the obviousness standard.

3 MR. LOWRY: Sure. I'll rephrase the
4 question.

5 Q Dr. Lee, there's no paragraph in this
6 section that sets forth the legal standard for
7 relying on the knowledge of a POSITA as part of a
8 ground for obviousness. Right?

9 MS. LUO: I'm still going to object to
10 form on that one.

11 A I'm not a lawyer. So my understanding is
12 that the prior art, a collection of prior art or
13 even a single prior art, in view of a POSITA's
14 knowledge can render the claims obvious.

15 In -- perhaps in that section I might not
16 have explicitly indicating -- well, actually, I
17 take that back. In Paragraph 19 I cited that how
18 a person of ordinary skill in the art, meaning
19 that a POSITA's knowledge, would understand the
20 challenged claims of the alleged invention.

21 And in Paragraph 20 I also mention that a
22 patent claims is unpatentable and invalid as

1 obvious if the subject matter of the claim as a
2 whole would have been obviously to a POSITA,
3 meaning that in view of the POSITA's knowledge of
4 the claimed subject matter at the time of the
5 alleged invention at issue.

6 So in Paragraph 22 there I also said that
7 in determining whether an invention that is in
8 combination of known elements would be obvious to
9 a POSITA, meaning that in view of the POSITA's
10 knowledge at the time of the alleged invention.

11 So in that section I have said that prior
12 arts, or even a single prior art in view of a
13 POSITA's knowledge, can render the claims obvious.

14 Q For that last statement, Dr. Lee, when
15 you said that prior arts, or even a single prior
16 art in view of a POSITA's knowledge can render the
17 claims obvious, which paragraph are you referring
18 to in your declaration?

19 A Well, all the paragraph that I describe
20 in my answer right before this answer; Paragraph
21 19, Paragraph 20, Paragraph 21 -- 22, and so on.

22 Q So you can't point to a specific

1 paragraph that stands for that proposition?

2 A No; I point to all three paragraphs,
3 three or four paragraphs.

4 Q So you alleged one ground for obviousness
5 in your declaration. Right?

6 A Ground 1, yes, it is right.

7 Q And Ground 1 is based on Nakajima in view
8 of the knowledge of a person of ordinary skill in
9 the art. Right?

10 A That is correct, Ground 1 is Nakajima in
11 view of the knowledge of a POSITA render obvious
12 claims that I list in 1 through 15, 17 through 18,
13 and 20.

14 Q And there's no paragraph in your
15 Understanding of the Law section, where you
16 describe when it's proper to rely on the knowledge
17 of a POSITA to supply a missing limitation in an
18 allegation of obviousness, is there?

19 MS. LUO: Object to form.

20 A You said there's no paragraph in Section
21 4, the Understanding of the Law, that describe
22 when to apply a prior art in view of POSITA's

1 knowledge to render the claims obvious?

2 Is that what you said?

3 Q No, that's not what I said.

4 I said, in this Understanding of the Law
5 section, there's no sentence that describes when
6 it's proper to rely on the knowledge of a POSITA,
7 as you do in Ground 1, to supply a missing
8 limitation for an allegation of obviousness.

9 Isn't that right?

10 MS. LUO: Object to form.

11 A Again, I'm not a lawyer. But the way I
12 read the paragraph that I cited, Paragraph 19,
13 Paragraph 20, Paragraph 21, 22, all indicate to me
14 that a missing element, missing limitations, can
15 be relied on by a POSITA, and in view of the
16 POSITA's knowledge, to render the claims obvious.

17 I mean, if you wanted an explicit
18 sentence, I think that a person of ordinary skill
19 in the art, reading that section, would have
20 understood that a set of prior art or even a
21 single prior art in view of the POSITA's
22 knowledge, can render the claims obvious. And any

1 missing limitation can be relied on by a POSITA's
2 knowledge, or in other words in view of the
3 POSITA's knowledge, to render the claims obvious.

4 Q Right. And what I'm asking you is, you
5 say it's there, but can you point to me where it
6 is? Because I don't see it.

7 And I'm just asking please show me in
8 your declaration where it is in this section.

9 A In Paragraph 19 I state, I address how a
10 person of ordinary skill in the art, a POSITA,
11 would have understood the challenged claim of the
12 alleged invention in Section 8 and Section 9.

13 And Paragraph 20, that I stated that I
14 have been further instructed and understand that a
15 patent claim is unpatentable and invalid as
16 obvious if the subject matter of the claim as a
17 whole would be -- would have been obvious to a
18 person of the ordinary skill in the art of the
19 claimed subject matter at the time of the
20 invention at issue.

21 In other words, that seems to me that
22 indicating that the prior art or a set of prior

1 art in view of POSITA's knowledge, can render the
2 claim obvious, and any missing limitation can be
3 relied on by -- on a POSITA's knowledge to render
4 the claims obvious.

5 And Paragraph 21, I also said that for
6 the claimed subject matter to be obvious over
7 multiple -- sorry, no. Claim -- sorry, Paragraph
8 22, that an invention that is in combination of
9 known element would be -- would have been obvious
10 to a person of ordinary skill in the art at the
11 time of the invention.

12 So all these various sentences suggest to
13 a reader, even though I'm not -- a person of
14 ordinary skill in the art might not be an
15 attorney, and certainly I'm not an attorney, that
16 all these sentences and paragraphs indicate that a
17 set of prior arts or a single prior art in view of
18 POSITA knowledge, can render the claims obvious.
19 The missing limitations in the prior art can be
20 relied on by a POSITA, in other words, in view of
21 a POSITA's knowledge, to render the claims
22 obvious.

1 So that's how I read the section in
2 Section 4. Again, I'm not an attorney, so I've
3 been instructed by counsel about all this. That's
4 how -- that's how I would understand what is
5 written in Paragraph 18 to Paragraph 33.

6 Q Dr. Lee, very simple question.

7 In Paragraphs 18 to Paragraph 33 of your
8 declaration, is the phrase "knowledge of a POSITA"
9 used once?

10 A Although the phrase "knowledge of a
11 POSITA," the exact phrase is not mentioned in
12 Section 4, but a person of ordinary skill in the
13 art or any person reading Section 4, which is
14 Understanding of the Law, even though a person of
15 ordinary skill in the art might not be attorney or
16 for sure I'm not an attorney, as I stated in
17 Paragraph 18, that is what those paragraph means,
18 that a prior art in view of POSITA's knowledge can
19 render the claims obvious.

20 Q Dr. Lee, just another simple yes-or-no
21 question. In Paragraphs 18 to Paragraph 33 of
22 your declaration, is the phrase "POSITA's

1 knowledge" used at all?

2 A And I believe I just answered your
3 question that --

4 Q But --

5 A Can I finish my answer? You asked --

6 Q Yes, please.

7 A Please. Thank you, sir.

8 I did answer your question. I said, no,
9 it has not been expressed explicitly in that
10 phrase. However, reading that section, a person
11 of ordinary skill in the art would have understood
12 that what that means is that a set of prior art or
13 a single prior art in view of POSITA's knowledge,
14 can render the claims obvious.

15 Q Dr. Lee, just to clarify, my previous
16 question asked you whether the phrase "knowledge
17 of a POSITA" was used. And my subsequent question
18 asked whether the phrase "POSITA's knowledge" was
19 used. So just to clarify.

20 Are the phrases "knowledge of a POSITA"
21 or "POSITA's knowledge" used in Paragraphs 18 to
22 33 of your declaration?

1 A In paragraph --

2 MS. LUO: Objection. Form.

3 THE WITNESS: Sorry.

4 A In Paragraph 18 to 33, the phrase
5 "knowledge of a POSITA" or "POSITA's knowledge"
6 was not explicitly disclosed, but implicitly
7 disclosed.

8 Q Let's turn to Page 53 of your
9 declaration.

10 Actually, Dr. Lee, would you like to take
11 a break or would you like to keep going?

12 A Let's, perhaps, a five minutes break.

13 MR. LOWRY: Sounds good. We'll come back
14 on the record at 12:09. Thank you.

15 THE WITNESS: Thank you, sir.

16 (A recess was taken.)

17 BY MR. LOWRY:

18 Q Let's go to Page 53 of your declaration,
19 please, Dr. Lee.

20 A Yes, I've got it.

21 Q Do you see Claim 2?

22 A Claim 2, yes.

1 Q Now, Claim 2 recites in part, "forming a
2 dummy channel structure extending vertically
3 through the stack." Right?

4 A Yes.

5 Q And in Paragraph 100 of your declaration,
6 you state that Nakajima, in view of the knowledge
7 of a POSITA, render this limitation obvious.

8 Right?

9 A Yes.

10 Q Here you're relying on the knowledge of a
11 POSITA to provide the recited dummy channels.

12 Right?

13 A Yes.

14 Q And Nakajima by itself does not disclose
15 dummy channels, does it?

16 A As I describe in Paragraph 101, that
17 Nakajima already formed the channel, the active
18 channel, before the TACs. And that it would be
19 understood and certainly obvious to a person of
20 ordinary skill in the art to form dummy channels
21 at the same time as the active channel CL, capital
22 C, capital L, as I listed several reasons in the

1 subsequent paragraphs.

2 Q And I see that, Dr. Lee. My question is
3 just generally simple. Just Nakajima by itself
4 doesn't disclose dummy channels, does it?

5 A So you're saying Nakajima does not by
6 itself discloses dummy channel.

7 Is that right?

8 Q That's correct.

9 A Yeah, as I describe in Paragraph 101,
10 that a POSITA would have been motivated and would
11 have been obvious to have Nakajima form dummy
12 channel, even though dummy -- dummy channel was
13 not explicitly disclosed in Nakajima.

14 Q Let's go to Page 65 of your declaration,
15 please.

16 A Sixty-five, yes.

17 Q Let me know when you're there.

18 A I'm there.

19 Q Do you see Claim 7?

20 A Yes.

21 Q Claim 7 recites, "forming a plurality of
22 shallow recesses." Right?

1 A Yes.

2 Q And if we scroll down to Paragraph 128 of
3 your declaration, you discuss the correct claim
4 interpretation regarding shallow recesses, the
5 shallow recesses limitation. Right?

6 A Sorry, what paragraph?

7 Q It's right above 128. I can repeat the
8 question if it's helpful.

9 A Right above Paragraph 128. So Paragraph
10 127?

11 Q I guess technically there's just a bold
12 heading between Paragraphs 127 and 128.

13 A Oh, okay. Yeah.

14 Q Okay. So in Paragraph 128 of your
15 declaration is where you discuss the correct claim
16 interpretation, as the heading states, regarding
17 the shallow recesses limitation. Right?

18 A That's right. The title above 128,
19 Paragraph 128, is, The Correct Claim
20 Interpretation.

21 Q And under this, quote/unquote, correct
22 claim interpretation, you're relying on the

1 knowledge of a POSITA to provide the recited
2 shallow recesses. Right?

3 A Yes, I -- I at least show the claim's
4 invalid, the Claim 7 are invalid, on the basis of
5 obviousness, using the correct claim
6 interpretations.

7 Q Let's look at Paragraph 20 of your
8 declaration.

9 A Sorry.

10 Q That's okay. It's on Page 10.

11 A Okay.

12 Q The first sentence of Paragraph 20
13 states, "I have been further instructed and
14 understand that a patent claim is unpatentable and
15 invalid as obvious if the subject matter of the
16 claim as a whole would have been obvious to a
17 POSITA of the claimed subject matter as of the
18 time of the invention at issue."

19 Do you see that?

20 A Yes.

21 Q What time of invention for the '254
22 patent did you consider?

1 A Priority date I believe is somewhere in
2 2018.

3 Q Do you recall the date?

4 A I'm looking it up now.

5 Okay. On Paragraph 61, My opinions in
6 this declaration were formed from the perspective
7 of a POSITA as of August 21, 2028 [sic], including
8 both the knowledge of a POSITA at the time, as
9 well as how a POSITA would understand -- would
10 have understood the '254 patent and the prior art.

11 Q Dr. Lee, and it's your opinion that the
12 challenged claims do not require any claim
13 construction. Right?

14 A So in Paragraph 70 that I stated that I
15 have been formed -- that I have been informed that
16 the words of a claim are generally given their
17 plain and ordinary meaning, that the term or
18 phrase would have to POSITA at the time of
19 invention in view of the surrounding claim
20 languages -- language, the specification, and the
21 file history, collectively the intrinsic evidence
22 or intrinsic record.

1 So to answer your question, that I don't
2 think either side had offer claim construction,
3 but given -- generally given the plain and
4 ordinary meaning.

5 Q And, Dr. Lee, what's the plain and
6 ordinary meaning of "shallow recesses"?

7 A So first of all, I have reviewed the
8 patent, patent '254, exhibit, let's see, 1001 I
9 believe. Yes. And there's no definitions of what
10 "shallow" is. You know, as we all know, "shallow"
11 is a relative term.

12 For example, shallow trench isolation,
13 right, that isolation is shallow in -- in relation
14 to the depth of the substrate. So shallow
15 recesses in a person of ordinary skill
16 perspective, would probably refer to the lateral
17 width of the recess in relationship to the length
18 of the sacrificial layer or eventually the
19 conductive layer the word lines.

20 But what is considered shallow, whether
21 it's 10 percent, 1 percent, or 50 percent of the
22 ratio, is not defined in paragraph -- in the '254

1 patent.

2 However, I think '254 clearly teaches
3 that these recesses are intentional as opposed to
4 unintentional. In other words, it's deliberate.

5 Q Dr. Lee, what part of the '254 patent
6 teaches that recesses are intentional?

7 A I believe that -- let's see.

8 So in Paragraph 126 I stated, The '254
9 patent discloses an etch that intentionally forms
10 recesses in the sacrificial layer. That is in the
11 '254 patent, Exhibit 1001, Column 13, Row 47 to
12 61, as well as in Figure 3D.

13 Q Dr. Lee, can you go to Paragraph 4 of
14 your declaration?

15 A Paragraph 4. What page?

16 Q Page 4.

17 A Oh, Page 4.

18 Q And Paragraph 4.

19 A Yeah. Yes. About my compensation?

20 Q Yes. You state that you're being
21 compensated at a rate of \$680 per hour. Right?

22 A That's right.

1 Q Do you have any stock in Micron?

2 A No, not that I know of. I don't invest
3 in individual stocks.

4 Q Do you receive any bonuses tied to how
5 well Micron does as a company?

6 A Absolutely not.

7 Q Have you received any compensation for
8 your inventions from Micron?

9 A I don't think so.

10 Q Now, you've worked as an expert for
11 Micron before. Right?

12 A Other than this case?

13 Q Uh-huh.

14 A I don't -- I don't recall.

15 I know in this case obviously I have.

16 Q By "this case" are you referring to this
17 IPR proceeding or the numerous IPR proceedings --

18 A The numerous IPR -- the numerous IPR.
19 Sorry to interrupt. The numerous IPR of IMTC
20 versus Micron. And yes, I have previously work in
21 a case -- in one other case on the side of Micron.

22 Q And, Dr. Lee, would a person in a CMOS

1 fab -- excuse me. Or strike that.

2 Would a person working in a CMOS fab for
3 three years qualify as a POSITA?

4 MS. LUO: Object to form.

5 A In Paragraph -- in Section 5 I listed
6 what is -- what qualify a POSITA, specifically in
7 Paragraph 35. Would you like me to read that?

8 Q No. And let me just rephrase the
9 question.

10 Would a person working in a CMOS fab,
11 referring to complementary
12 metal-oxide-semiconductor, for three years, would
13 they qualify as a POSITA?

14 MS. LUO: Object to form.

15 A Well, with that alone, I would say
16 that -- I would say that not, because you didn't
17 give me the additional background whether he has a
18 bachelor degree of science in electrical
19 engineering or similar discipline; whether he has
20 two to three years of professional experience in
21 NAND flash memory device. And so with that alone,
22 without additional further information, you know,

1 I would say by that alone I wouldn't call that a
2 POSITA, based on my opinion disclosed in Section 5
3 of my declaration.

4 Q And would someone who has a degree, a
5 bachelor's degree in electrical engineering and
6 has been working in a CMOS fab for three years,
7 would they qualify as a POSITA?

8 MS. LUO: Object to form.

9 A In my opinion, as stated in Paragraph 36,
10 that in addition to at least a Bachelor Degree of
11 Science in Electrical Engineering or similar
12 discipline, along with two to three years of
13 professional experience working with either in
14 design, research, or teaching, NAND flash memory
15 devices or equivalent level of skill, knowledge,
16 and experience.

17 So, in other words, that with a general
18 CMOS experience -- with experience in general CMOS
19 technology, which many, many CMOS technology does
20 not -- do not include 3D NAND, so in my mind
21 that -- that it is probably not considered a
22 POSITA. However, it helps having some -- having

1 the bachelor degree and knowledge of CMOS
2 technology definitely help to understand 3D NAND
3 technology.

4 But it will be to me a person of ordinary
5 skill in the art in the field of '254 patent, to
6 me would have to have what is described in
7 Paragraph 36.

8 Q Would your answer change if the person
9 working in the CMOS fab was focused on 3D NAND
10 technology?

11 MS. LUO: Object to form.

12 A Are you saying that if a person of
13 ordinary skill in the art has three years of
14 professional experience working with 3D NAND, as
15 well as having a degree of science in electrical
16 engineering or similar discipline, would they
17 consider a POSITA? That's the question?

18 Q That's not my question.

19 My question is, if a person has a degree
20 of science in electrical engineering and three
21 years of professional experience working in a CMOS
22 fab on 3D NAND technology, would that person be

1 considered a POSITA?

2 MS. LUO: Object to form.

3 A Well, obviously what that means is that
4 that person had three years of professional
5 experience working with 3D NAND flash memory. And
6 I don't know what you mean by CMOS lab. Are you
7 talking about a fab that fabricates CMOS devices
8 as well as 3D NAND flash memory. Because 3D flash
9 memory, as you know, not only consider -- contain
10 memory devices, but also CMOS peripheral circuits.

11 So to answer your question, it sounded
12 like that person have a bachelor degree in
13 electrical engineering and three years of
14 experience working with 3D NAND fab flash memory
15 devices. And in my opinion, that would qualify --
16 according to Paragraph 36, that would qualify to
17 be a POSITA.

18 Now, of course in Paragraph 37 and 38 I
19 also say that the POSITA would also -- should be
20 aware of the general knowledge of semiconductor
21 manufacturing and 3D NAND structure, how it
22 operates, how it control, and so on and so forth.

1 MR. LOWRY: Okay. No further questions.
2 I'll pass the witness.

3 MS. LUO: Richard, do you mind if we take
4 a ten-minute break?

5 MR. LOWRY: Sure.

6 (A recess was taken.)

7 MS. LUO: Dr. Lee, I just wanted to thank
8 you for your time today. I have no further
9 questions.

10 THE WITNESS: Thank you.

11 MR. LOWRY: Thank you, Dr. Lee.

12 THE WITNESS: Thank you, Richard.

13 (Off the record at 12:54 p.m. EDT.)
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ACKNOWLEDGMENT OF DEPONENT

I, JACK C. LEE, Ph.D., do hereby
acknowledge that I have read and examined the
foregoing testimony, and the same is a true,
correct and complete transcription of the
testimony given by me, and any corrections appear
on the attached Errata sheet signed by me.

(DATE)

(SIGNATURE)

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C E R T I F I C A T E

I, Debra Ann Whitehead, E-Notary Public in and for
the Commonwealth of Virginia, do hereby certify:

That JACK C. LEE, Ph.D., the witness whose
deposition is hereinbefore set forth, was duly sworn
by me before the commencement of such deposition and
that such deposition was taken virtually and is a
true record of the testimony given by such witness.

I further certify that the adverse party,
MICRON TECHNOLOGY, INC., was represented by counsel
at the deposition.

I further certify that the deposition of
JACK C. LEE, Ph.D., occurred virtually, on
Wednesday, July 30th, 2025, from 10:01 a.m. to 12:54
p.m. EDT.

1 I further certify that I am not related to
2 any of the parties to this action by blood or
3 marriage, I am not employed by or an attorney to any
4 of the parties to this action, and that I am in no
5 way interested, financially or otherwise, in the
6 outcome of this matter.

7

8 IN WITNESS WHEREOF, I have hereunto set my
9 hand this 30th day of July, 2025.

10

11 My commission expires:

12 October 31, 2027

13

14 *Debra Ann Whitehead*

15

16 -----

17 E-NOTARY PUBLIC IN AND FOR THE

18 COMMONWEALTH OF VIRGINIA

19

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