

Solid State TECHNOLOGY

Insights for Electronics Manufacturing

**Overcoming Challenges
in 3D NAND Volume
Manufacturing**

P. 18

**In-line Metrology for
Characterization of
Bonded Wafers**

P. 22

**The Pervasiveness of
ASICs in the IoT Era**

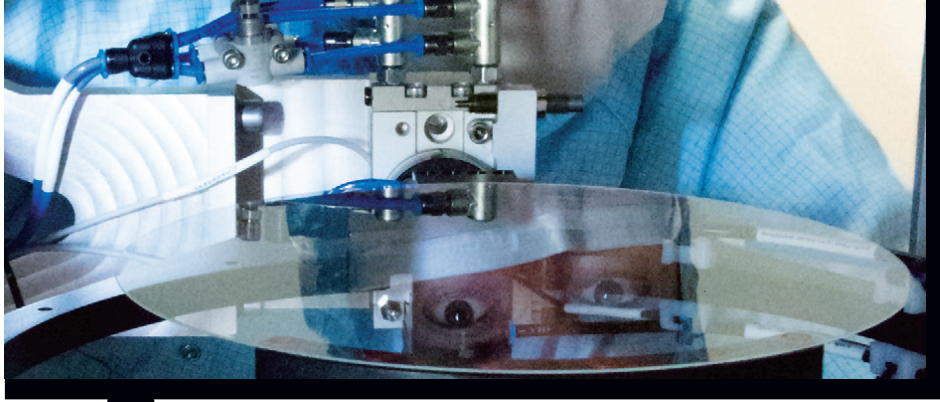
P. 36

Laser Debonding for Ultrathin and Stacked Fan Out

P.12

www.solid-state.com

Extension
MEDIA



Solid State TECHNOLOGY®

JULY 2017 VOL. 60 NO. 5

Solid-state UV laser debonding utilizing temporary glass carriers enables cost-effective high-volume-manufacturing (HVM) processing of ultra-thin stacked fan-out packages.

COVER

FEATURES

12

ADVANCED PACKAGING | Laser debonding for ultrathin and stacked fan out packages

UV laser debonding solutions combine the advantages of the solid-state laser with low maintenance, low consumables costs and high pulse frequencies combined with high spatial control due to the special beam shaping optics.

Elisabeth Brandl, Thomas Uhrmann and Martin Eibelhuber, EV Group, St. Florian, Austria

18

3D NAND | Overcoming challenges in 3D NAND volume manufacturing

As 3D NAND becomes the mainstream technology, its challenging roadmap poses opportunities for continued innovation.

Harmeet Singh, Lam Research, Fremont, CA

22

METROLOGY | In-line metrology for characterization and control of extreme wafer thinning of bonded wafers

In-line metrology methods used during extreme wafer thinning process pathfinding and development are introduced.

M. Liebens, A. Jourdain, J. De Vos, T. Vandeweyer, A. Miller, E. Beyne, imec, Leuven, Belgium, and S. Li, G. Bast, M. Stoerring, S. Hiebert, A. Cross, KLA-Tencor Corporation, Milpitas, California

30

VACUUM TECH | Enhanced vacuum security using advanced sub-fab monitoring and data analytics

Sub-Fab Fault Detection and Classification (FDC) software platforms collect, integrate and analyse operational data.

Erik Collart, Edwards, Sanborn, NY

36

IOT | The pervasiveness of ASICs in the IoT era

For an increasing number of designs, companies are finding it beneficial to design their own ASICs with system-on-a-chip (SoC) complexity.

41

METROLOGY | NASA's new vacuum-channel nanoelectronics rely on Park Systems AFM

Using scanning capacitance microscopy with a Park Systems atomic force microscope a team at NASA successfully characterized both the spatial variations in capacitance as well as the topography of vacuum-channel nanoelectronic transistors.

Mark Andrews, Park Systems, Santa Clara, CA

COLUMNS

- 2 **Editorial** | What's next in leading edge semiconductor manufacturing?
Pete Singer, Editor-in-Chief
- 10 **Packaging** | 450mm equipment for WLCSPs?
Phil Garrou, Contributing Editor
- 11 **Semiconductors** | PCM + ReRAM = OUM as XPoint,
Ed Korczynski, Sr. Technical Editor

DEPARTMENTS

- 4 Web Exclusives
- 4 News
- 47 Ad Index



What's next in leading edge semiconductor manufacturing?

Do you know what's coming? The semiconductor industry is evolving rapidly, driven by new demands from an increasingly diverse array of applications, including the IoT, 5G telecommunication, autonomous driving, virtual and augmented reality, and artificial intelligence/deep learning. Solid State Technology will be conducting a new survey that will take aim at understanding what this evolution means to the semiconductor manufacturing industry supply chain in terms of the technology that will be needed.

IoT alone is expected to drive not only a huge demand for sensors, but a far more sophisticated cloud computing infrastructure that will employ the most advanced logic and memory chips available, including 7 and 5nm logic devices and 3D NAND. The survey will provide answer to questions such as:

- What new materials are going into volume production and what kind of challenges do they create in terms of availability, handling and disposal?
- How are fabs dealing with more complex devices structures such as FinFETs and 3D NAND which can create new pressures on process control, yield, and economics?

- EUV lithography is expected to be in volume production for the 5nm node, if not sooner. What new opportunities and challenges will this create in the supply chain for process equipment, materials and inspection tools?
- 200mm fabs are seeing a resurgence, in part due to the booming market for IoT devices and sensors. How will this impact the leading edge?
- What kind of new challenges and opportunities exist in heterogeneous integration and advanced packaging?

The survey will be conducted across the entire Solid State Technology audience, which includes more than 180,000 engineering and management professionals in 181 countries. The report will be compiled by Solid State Technology editors, who will add valuable insights and interpretations based on decades of experience.

Stay tuned for the survey – we welcome your input!

—Pete Singer, Editor-in-Chief

Solid State TECHNOLOGY®

Pete Singer, Editor-in-Chief
Ph: 978.470.1806,
psinger@extensionmedia.com

Shannon Davis, Editor, Digital Media
Ph: 603.547.5309
sdavis@extensionmedia.com

Ed Korczynski, Senior Technical Editor,
edk@extensionmedia.com

Dave Lammers, Contributing Editor

Phil Garrou, Contributing Editor

Dick James, Contributing Editor

Vivek Bakshi, Contributing Editor

CREATIVE/PRODUCTION/ONLINE

Marjorie Sharp, Production Traffic
Coordinator

Nicky Jacobson, Senior Graphic Designer

Simone Bradley, Graphic Designer

Slava Dotsenko, Senior Web Developer

MARKETING/CIRCULATION

Jenna Johnson,
jjohnson@extensionmedia.com

CORPORATE OFFICERS

Extension Media, LLC

Vince Ridley, President and Publisher
vridley@extensionmedia.com

Clair Bright, Vice President and Publisher
Embedded Electronics Media Group
cbright@extensionmedia.com

For subscription inquiries:

Tel: 847.559.7500; Fax: 847.291.4816;
Customer Service e-mail: sst@omedia.com;
Subscribe: www.sst-subscribe.com

Solid State Technology is published eight times a year by Extension Media LLC, 1786 Street, San Francisco, CA 94107. Copyright © 2017 by Extension Media LLC. All rights reserved. Printed in the U.S.

Extension
MEDIA

1786 18th Street
San Francisco, CA 94107

June 2017 VOL. 60 NO. 5 • **Solid State Technology** ©2017 (ISSN 0038-111X) **Subscriptions:** Domestic: one year: \$258.00, two years: \$413.00; one year Canada/Mexico: \$360.00, two years: \$573.00; one-year international airmail: \$434.00, two years: \$691.00; Single copy price: \$15.00 in the US, and \$20.00 elsewhere. Digital distribution: \$130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including change of address) to: *Solid State Technology*, 1786 18th Street, San Francisco, CA 94107-2343, (8 am – 5 pm, PST).

Overcoming challenges in 3D NAND volume manufacturing

HARMEET SINGH, Lam Research Corp., Fremont, CA

As 3D NAND becomes the mainstream technology, its challenging roadmap poses opportunities for continued innovation.

Since its introduction several years ago, 3D NAND has become a mainstream technology because of its ability to increase bit density in memory devices. Its adoption has been accelerated by advances in the underlying manufacturing processes that are enabling 3D architectures and lowering the cost per bit. With all its advantages, however, the overall complexity and capital intensity of 3D NAND manufacturing add significantly to the challenges fabs are facing in terms of process control, yield, and economics.

Market and technology drivers for 3D NAND

The main impetus for 3D NAND was the recognition that planar technology was approaching the end of its physical limits to deliver higher densities and a lower cost-per-bit. Past advances in conventional planar NAND technology have primarily been driven by physical scaling, where lithography capabilities determined just how many memory cells could fit within a given die size. Using multiple levels of charge within each cell by going from single- to multi-level cell designs has also enabled increased bit densities. However, these improvements typically have come at the expense of speed because of the need to differentiate between the multiple levels of charge. In addition, since the individual memory cells for these designs lie in a horizontal plane, scaling is still ultimately limited by lithography. Other challenges in scaling 2D NAND beyond the 15 nm node include cell-to-cell interference, unscalable dielectrics, and electron leakage [1].

To address these issues, 3D NAND fundamentally changes the scaling paradigm. Instead of traditional X-Y scaling in a horizontal plane, 3D NAND scales in the Z-direction by stacking multiple layers of NAND gates vertically. This allows more cells to be packed into the same X-Y space (planar area) on the die without shrinking dimensions horizontally. By easing cell size requirements, triple- and even quadruple-level cell designs are possible. As such, 3D NAND offers a significant increase in bit density over planar NAND.

Unlike planar NAND, where scaling is primarily driven by lithography, 3D NAND scaling is enabled by advances in deposition and etch processes. An incredible level of precision and repetition is required in defining complex

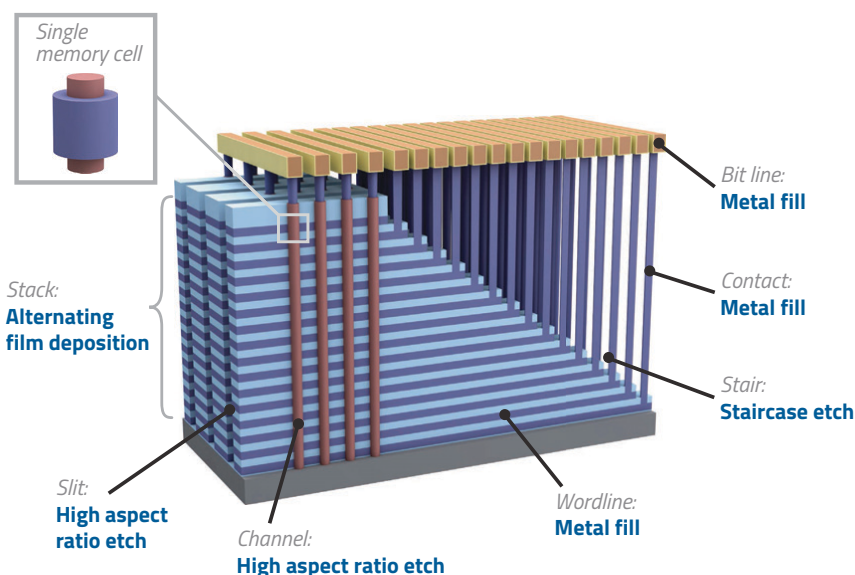


FIGURE 1. 3D NAND architecture showing some of the most challenging and critical deposition and etch processes.

HARMEET SINGH is Vice President, Etch Products, Lam Research Corp., Fremont, CA

3D structures with extremely high aspect ratio (HAR) features. Achieving success with 3D NAND requires innovative deposition and etch solutions that minimize variability.

Overview of critical 3D NAND processes

The 3D NAND architecture requires advanced capabilities enabling HAR and complex structures (**FIGURE 1**). Critical processes involved include multilayer stack deposition, HAR channel etch, wordline metallization, staircase etch, HAR slit etch, and stair contacts formation. The following sections look at some of these areas in more depth and describe the most critical process parameters that must be controlled.

Film deposition

Creating stacked memory cells starts with depositing alternating layers of thin films. Unlike planar NAND, where cell pitch is defined by lithography, pitch in 3D NAND is determined by the film thickness. As such, precise control of layer-to-layer deposition uniformity is extremely important. Currently, commercial 3D NAND products in high-volume manufacturing have layers ranging from 32 to 48 pairs, while next-generation products with more than 60 pairs are now beginning high-volume ramps.

Critical requirements for depositing stacked films are the stress and uniformity of the individual layers within the overall stack. These requirements become more stringent and increasingly more challenging to meet as the number of layers grows. Wafer bow and local film stress (**FIGURE 2**) directly impact the ability to achieve precise lithography overlay. Film thickness and repeatability affects the active area of cell and consistency of the litho/etch performance. As a result, both film stress control and

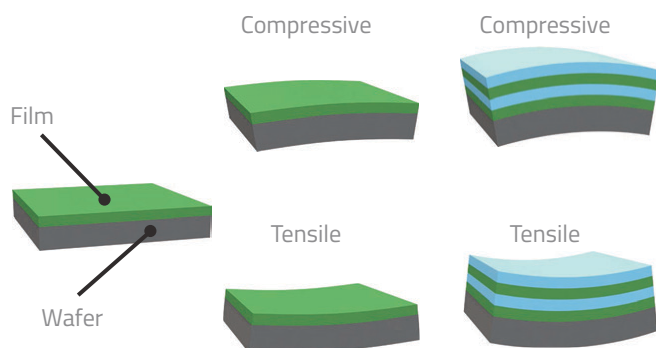


FIGURE 2. As the number of layers increases in the 3D NAND device, the effect of film stress can become magnified.



© 2017 Brewer Science, Inc.

OptiStack[®] Systems

Advanced Multilayer Lithography

OptiStack[®] multilayer lithography systems are designed for the most advanced high-volume semiconductor manufacturing processes in the world. Our versatile OptiStack[®] material set is designed to be used in combination with our proprietary optical modeling to achieve the finest resolutions possible.

Brewer Science[®] OptiStack[®] system offers:

- Lithography modeling service
- Materials with customizable n and k optics
- Process compatibility for any application: FEOL or BEOL, PTD or NTD, ArF or KrF
- Process and cost-of-ownership advantages
- Universal substrate
- Lithography tool extension
- Industry-recognized expertise and support

www.brewerscience.com






excellent uniformity are critical to wafer yields. To address these concerns, careful management of stress by tuning deposition conditions and optimizing integration is needed not only for the film stack deposition, but also throughout 3D NAND manufacturing.

High aspect ratio channel etching

HAR channel etch is the most critical and challenging step in 3D NAND because it is key to achieving uniform hole size through multiple layers to define the channel of memory cells. More than a trillion holes must be etched simultaneously and uniformly on every wafer, each with an aspect ratio of more than 40:1. For comparison, the highest aspect ratio structure that is etched in planar NAND is less than 15:1.

Deep etch on these multilayer stacks can push the limits of physics to achieve uniformity from top to bottom. As shown in **FIGURE 3**, the high aspect ratio of this etch leads to transport limitation challenges that can generate a range of problems. These include incomplete etch wherein some holes don't reach the bottom, bowing, twisting, and CD variation between the top and bottom of the stack. Such defects can lead to shorts, interference between neighboring memory strings, and other performance issues. Solving these HAR-related transport issues requires precise control of high-energy ions during the etch process. Technologies that help deliver this capability include a symmetric chamber design for intrinsic uniformity, a proprietary high ion energy source with advanced plasma confinement and modulation, and orthogonal (independent) uniformity tuning knobs, such as multi-zone gas delivery and temperature control to achieve required uniformity across the wafer.

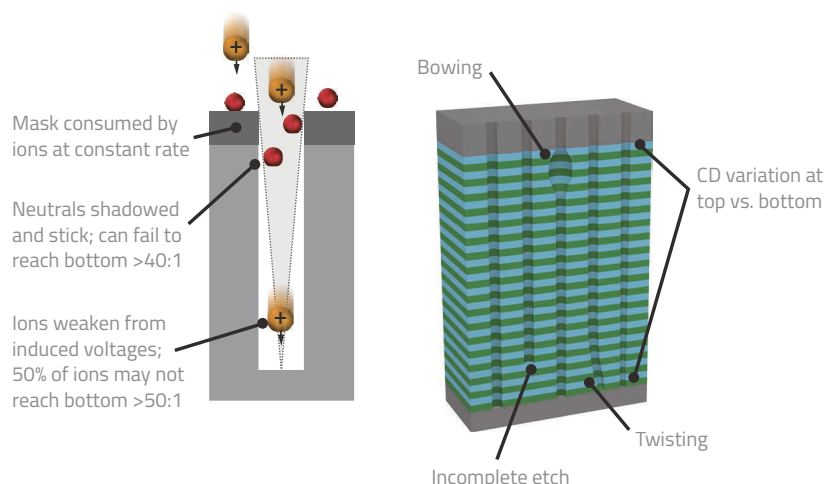


FIGURE 3. Transport limitation can lead to distortion (bowing and twisting), CD variation, and incomplete etch during channel formation.

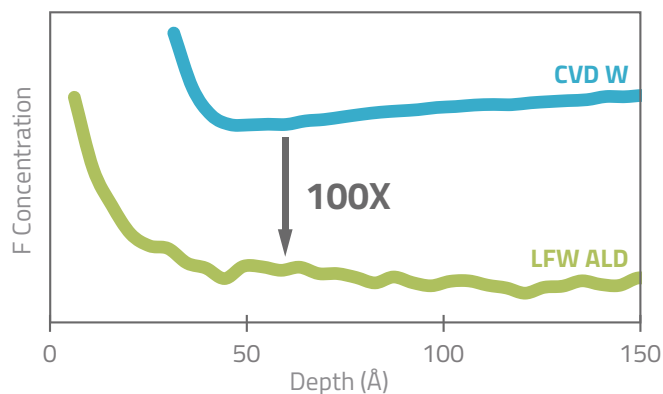


FIGURE 4. Low-fluorine tungsten ALD has demonstrated 100x lower fluorine versus CVD tungsten.

As the 3D NAND roadmap adds more layers to achieve higher bit density, channel hole etching becomes increasingly challenging due to higher aspect ratios. Managing the fundamental trade-offs among profile, selectivity, and CD requires continuous equipment innovation, not only to deliver HAR etching capabilities for more than 100 pairs, but also to do this at the productivity needed for volume manufacturing.

Wordline tungsten metal fill

For replacement-gate 3D NAND schemes, wordline tungsten fill provides the critical conductive links between individual memory cells within layers. This process is particularly challenging because of the need to achieve void-free fill of complex, narrow, lateral structures with minimal stress on the memory stack.

Due to the structural complexity, atomic-scale engineering is required for wordline fill. Traditional CVD tungsten films have inherent characteristics that limit capability for 3D NAND wordline fill. High tensile stress in CVD tungsten can lead to wafer bow, and fluorine in the process has been known to diffuse into adjacent layers where it can create yield-limiting defects. In addition, resistivity limits scaling: making each layer thinner would allow for more layers (more storage bits), but would also make wordline resistance too high. One approach to address these concerns is the use of a low-fluorine tungsten (LFW) ALD process. This has the ability to provide a smoother morphology that conforms better with the surface in each fill layer, thereby minimizing stress induced by the deposition process. Stress reduction by more than an order of magnitude has been demonstrated with LFW ALD technology. This

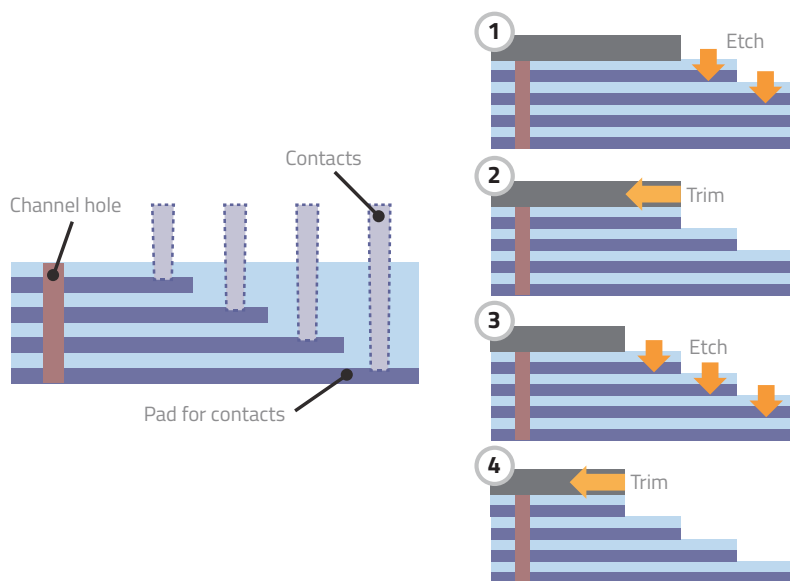


FIGURE 5. Staircase etch uses repeated vertical etch and lateral trim etch passes to define the contact pads.

approach has also been shown to lower fluorine content by up to 100x (**FIGURE 4**) and reduce resistivity by over 30% compared to conventional CVD tungsten.

Staircase etch

The staircase etch step creates the individual contact pads for each memory cell within the layers. A highly controlled etch process is used to define the size of each contact pad. To reduce the cost associated with lithography and improve productivity, repeated vertical etch and lateral trim etch processes are adopted to form the staircase instead of using numerous lithography steps. For each lithography pass, multiple staircase levels can be created by etching and trimming, as shown in **FIGURE 5**. The number of stairs that can be formed by this process is determined by the lateral-to-vertical (L/V) etch rate. Improving L/V etch selectivity can reduce the number of lithography steps needed.

Extreme accuracy is required to maintain the stair CD, thus avoiding misaligned contacts. If the CD for a pad is off by a few percent, that error will propagate through subsequent pads defined within the same lithography pass. Current technology can deliver uniform and repeatable stair CD precision of 1% (3-sigma) after more than five L/V trim processes. This is a critical factor for achieving high productivity and being able to scale to higher stacks with more layers economically.

Summary

Traditional planar scaling to increase NAND density is approaching its limits due to lithography and performance challenges. As 3D NAND becomes the mainstream

technology, its challenging roadmap poses opportunities for continued innovation. Stress management throughout wafer processing is crucial, and significant innovations in both deposition and etch processes are essential in forming the HAR features that dominate 3D NAND architectures. Finally, reducing variability in every critical step is a must to meet performance, yield, reliability, and cost requirements.

3D NAND completely changes the scaling paradigm by going vertical. No longer limited by lithography capabilities, 3D NAND can achieve greater levels of integrity, performance, and reliability – while building vertically for higher bit density and a lower cost-per-bit – through relying on advances in deposition

and etch processes.

References

1. Y.W. Park, Flash Memory, IEDM short course, 2015 ◀



TDK Self-Circulating Nitrogen EFEM Will Support FAB Yield Improvement

Self-circulating Nitrogen EFEM
CAVS-NE



Live Demo at
SEMICON West

- N₂ sealed bottom purge Load Ports installed on sealed N₂ EFEM module
- Low N₂ consumption by TDK Self-circulating N₂ EFEM purge system
- Inert Wafer FOUP environment controlled by TDK bottom purge sealed Load Port
- Wafers are never exposed to atmosphere between FOUP and load lock
- O₂ level <100ppm and humidity control to minimize water oxidation defects

Visit TDK Booth 5228, North Hall

For more information contact: phil.couts@us.tdk.com