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3D NAND's Vertical Scaling Race

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Shares*More competition, business uncertainty, and much more difficult manufacturing processes.*DECEMBER 17TH, 2020 - BY: **MARK LAPEDUS** (HTTPS://SEMIENGINEERING.COM/AUTHOR/MARK-LAPEDUS/)

3D NAND suppliers are accelerating their efforts to move to the next technology nodes in a race against growing competition, but all of these vendors are facing an assortment of new business, manufacturing, and cost challenges.

Two suppliers, Micron and SK Hynix, recently leapfrogged the competition and have taken the scaling race lead in 3D NAND. But Samsung and the Kioxia-Western Digital (WD) duo are readying their next 3D NAND products, as well. (Kioxia is the NAND spinoff of Toshiba.)

On the business front, meanwhile, the industry is undergoing some turbulence. There is a potential oversupply heading into 2021. In addition, after a period of losses in the memory sector, Intel recently exited the 3D NAND market, selling the business to SK Hynix for \$9 billion. And finally, China's Yangtze Memory Technologies Co. (YMTC), the newcomer in 3D NAND, is hoping to keep pace. But YMTC's parent company, Tsinghua Unigroup, has defaulted on its bond payments, leaving a cloud over the company.

[3D NAND](https://semiengineering.com/knowledge_centers/memory/non-volatile-memory-nvm/flash-memory/3d-nand/) (https://semiengineering.com/knowledge_centers/memory/non-volatile-memory-nvm/flash-memory/3d-nand/) is the successor to today's planar NAND [flash memory](https://semiengineering.com/knowledge_centers/memory/non-volatile-memory-nvm/flash-memory/). (https://semiengineering.com/knowledge_centers/memory/non-volatile-memory-nvm/flash-memory/). It is used for storage applications such as smartphones and solid-state storage drives (SSDs). Unlike planar NAND, which is a 2D structure, 3D NAND resembles a vertical skyscraper in which horizontal layers of memory cells are stacked and then connected using tiny vertical channels.

3D NAND is quantified by the number of layers stacked in a device. As more layers are added, the bit density increases, enabling products with more storage capacity. In 2013, Samsung shipped the world's first 3D NAND, a 24-layer 128Gbit device. Today, suppliers are shipping 64- and 96-layer 3D NAND devices and are now racing each other to ramp up products at the next technology generations, with 128 and 176 layers.

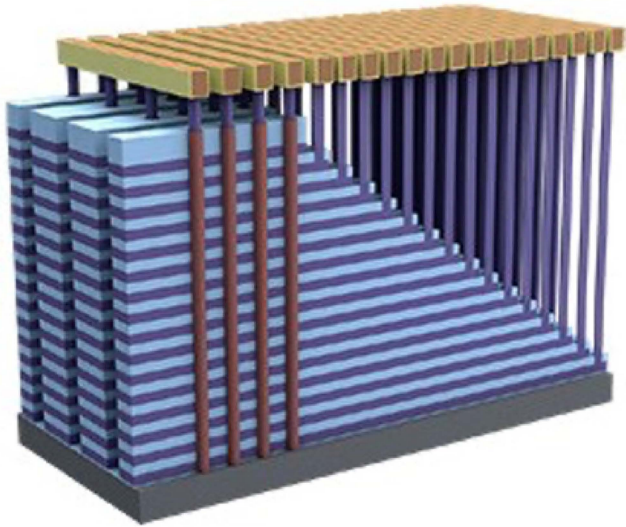


Fig. 1: 3D NAND device. Source: Lam Research

In R&D, meanwhile, vendors are working on 256-layer products and beyond. It's unclear how far 3D NAND will extend, but each technology migration is more difficult than the previous one. As vendors add more layers, the manufacturing challenges increase with higher costs.

On average, vendors are adding 30% to 50% more layers for each 3D NAND generation, according to Mark Webb, principal at MKW Ventures Consulting. "In reality, we have typically added 10% to 15% to wafer cost for each new generation, depending the inputs from tool vendors," Webb said in a recent presentation.

On the bright side, the 3D NAND market continues to grow, and the technology is becoming more efficient to manufacture at each generation over time. "The cost reduction for NAND is 20% per year on average," Webb said. "Bit costs will drop 20% per year on average."

To be sure, the 3D NAND market remains dynamic with various trends and events taking place in the arena. Among them:

- **More layers.** Micron and SK Hynix took the technology lead by moving from 128- to 176-layer 3D NAND products. Others are working on similar products.
- **More stacking.** The ability to stack all 3D NAND layers on the same die is running out of steam, forcing some to take new stacking approaches.
- **New architectures.** Vendors are developing new gate and die schemes to enable faster and smaller chips.

Why 3D NAND?

Today's systems incorporate a multitude of chips, such as CPUs, memory, and storage. CPUs handle the processing tasks, while memory and storage are designed to store data.

Memory and storage come in different forms and are arranged in a hierarchy in systems. In the first tier of the hierarchy, [SRAM](https://semiengineering.com/knowledge_centers/memory/volatile-memory/static-random-access-memory/) (https://semiengineering.com/knowledge_centers/memory/volatile-memory/static-random-access-memory/) is a memory type that's integrated into the processor to enable fast data access. [DRAM](https://semiengineering.com/knowledge_centers/memory/volatile-memory/dynamic-random-access-memory/) (https://semiengineering.com/knowledge_centers/memory/volatile-memory/dynamic-random-access-memory/), the next tier, is used for main memory. Disk drives and NAND-based SSDs are used for storage.

In total, the overall NAND market is expected to reach \$57 billion in terms of sales in 2021, up 12% over 2020, according to Risto Puhakka, president of VLSI Research. That compares to 25% growth in 2020 over 2019, according to the firm. It also sees some ominous signs in the market heading into 2021. "Companies are adding capacity. Whe'

the 'alpha' company adds capacity, which it's already doing, the followers need to do the same. Otherwise, they lose market share. Given another year or two, they all have too much capacity," Puhakka said.

NAND flash memory is a non-volatile technology that can be electrically erased and reprogrammed. In NAND, data is stored a memory cell and is represented by either a '0' or '1'. A cell can store 1 bit per cell (0, 1) as well as 2, 3, and 4 bits per cell. In all cases, the data remains stored even after the power is turned off in systems.

For years, the industry used planar NAND technology. In planar NAND, a series of memory cells are connected in series along a horizontal string.

A traditional flash memory cell involves a planar transistor structure with a control gate and a floating gate. Electrons are stored and removed from the floating gate by applying a voltage to the cell.

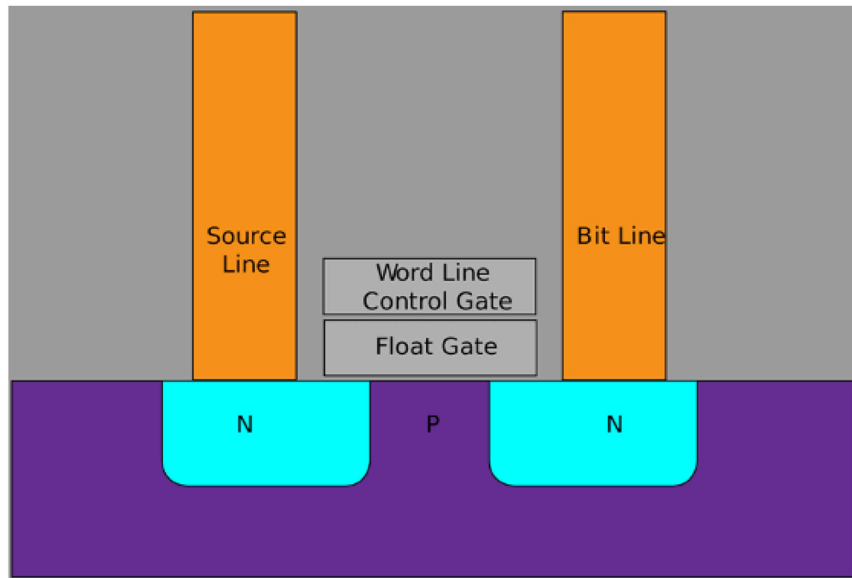


Fig. 2: Planar NAND memory cell Source: Wikipedia

Over the years, vendors scaled the cell size in planar NAND from 120nm to the 1xnm node, enabling 100 times more capacity. Recently, though, the cell size reached the limit at 14nm, meaning the technology can no longer scale.

That's where 3D NAND fits in. "3D NAND flash memory has enabled a new generation of non-volatile solid-state storage useful in nearly every electronic device imaginable," said Timothy Yang, a software applications engineer at [Coventor, a Lam Research Company](https://semiengineering.com/entities/coventor-inc/) (<https://semiengineering.com/entities/coventor-inc/>). "3D NAND can achieve data densities exceeding those of 2D NAND structures, even when fabricated on later generation technology nodes."

As stated, planar NAND consists of a horizontal string with memory cells. In 3D NAND, the memory cell string is stretched, folded over, and stood up vertically in a "U shape" structure. In effect, the cells are stacked in a vertical fashion to scale the density.

So there are multiple levels of memory cells. On one level, the cells reside on a horizontal plate, which consists of a layer of materials. 3D NAND has multiple layers.

"The layers describe the number of wordlines that are stacked up on top of each other," explained Mark Helm, a senior fellow at Micron. "We cut a vertical pillar through those wordline layers. And where we have an intersection of that pillar with each of those wordlines, that represents a single physical cell. That cell is formed at that intersection."

Each 3D NAND memory cell resembles a tiny cylinder-like structure. The tiny cell consists of a vertical channel in the middle, followed by a charge layer inside the structure. A gate wraps around the structure. "By applying a voltage, electrons are taken in and out of the insulating charge-storage film and signals are read," according to Kioxia.

Unlike planar NAND, which reduced the cell size at each node, 3D NAND uses a more relaxed process, somewhere between 30nm to 50nm. "Scaling in 3D NAND memory capacity is achieved in a different way: by adding vertical layers," said Nerissa Draeger, director of university engagements at [Lam Research](https://semiengineering.com/entities/lam-research/) (<https://semiengineering.com/entities/lam-research/>). "In this memory structure, cell density increases directly with the number of layers in the stack."

Then, at a one- to two-year cadence, vendors migrate from one technology generation to the next. "Early 3D NAND structures were made using 24 layer pairs. Today, chips with 96-layer structures are in volume production, and even taller stacks are on the horizon," Draeger said.

So the direction for 3D NAND is clear. "We need to continue stacking more and more layers of 3D NAND on top of each other as well as bringing in multi-level cell technologies that enable us to continue the bit scaling per square unit area," said Robert Clark, senior member of the technical staff at TEL, in a presentation.

Most vendors currently are in production at the 64- and 96-layer technology generations, which enables 256-Gbit and 512-Gbit 3D NAND devices, respectively.

Recently, Samsung and others introduced 128-layer 3D NAND devices, which represents the next node. Seeking to get a jump on the market, Micron and SK Hynix moved from the 128- to the 176-layer generation. Others are working on 176-layer and related products.

Micron's 176-layer 3D NAND technology incorporates a triple-level cell (TLC) scheme. "Now, we have 176 wordlines stacked up. Then, on each pillar, we have 176 physical cells associated with that pillar," Micron's Helm said. "For a 512Gbit TLC device, we have over a billion pillars in that particular die."

The device also has a 30% smaller die size than other chips. To accomplish this feat, Micron pioneered a concept called CMOS-under-array, where it stacks the 3D NAND array over the peripheral logic.

Others have different approaches. Some develop separate memory array and logic dies, which are situated next to each other. Going forward, though, most are moving toward the CMOS-under-array concept to reduce the die sizes. "One easily overlooked characteristic of 3D flash is that it boosted the write performance of NAND up by a factor of ~three compared to 2D flash," said Johann Alsmeier, a senior director at Western Digital, in a presentation at IEDM. "The main reason is the simpler program methods possible due to the complete screening of the NAND channels in the gate-all-around structure and the larger cell geometry with lower programming noise. Even higher parallelism can be achieved with multi-plane CUA (CMOS-under-array) architectures, of four or more partly independent planes for read and write. However, the CUA process is more costly if used for very low number of WLs."

Nonetheless, 128- and 176-layer 3D NAND won't become the mainstream technologies for some time. "64-layer 3D NAND is still ramping," said Jim Handy, an analyst with Objective Analysis. "2021 will be the year of 96 layers for most makers. Micron says they are shipping 176. SK Hynix' announcement is a response to Micron's, and that it may be some months before a chip is sighted in the marketplace."

3D NAND process flow

Suppliers have developed their own 3D NAND architectures, which are all slightly different. For example, Samsung's technology is called TCAT, while the Kioxia-WD duo uses the term BiCS.

In 3D NAND, the ultimate goal is to stack more layers on a substrate, enabling more density. Generally, there are two approaches to stack the layers — single deck or double deck.

Then, there are several ways to implement the gate structure, such as gate-first or gate-last. Suppliers are mainly embracing the gate-last approach. In addition, vendors are implementing two types of storage media — charge-trap and floating gate. Charge-trap is the dominant type.

All told, 3D NAND is a complex technology that presents some major challenging in the fab. According to TechInsights, some of the manufacturing challenges for current and future 3D NAND are:

- High-aspect ratio (HAR) etch processes to enable tiny vertical channels.
- Obtaining enough drive current between the memory cells.
- Logic die design optimization for CMOS-under-array.
- Wafer warpage.

“Cell current and wafer warpage are the top most concerns,” said Jeongdong Choe, a senior technical fellow at TechInsights. “Throughput of the production process is another one.”

To make 3D NAND, suppliers have several architecture options, material types, and process flows. One of the first manufacturing decisions is to determine which scaling approach is the best path. There are two approaches — single deck or double deck.

Traditionally, Samsung has taken the single-deck approach. For example, Samsung’s 92-layer 3D NAND device stacks all 92 layers on the same die. Samsung’s latest 128-layer technology stacks 128 layers on the same chip.

By stacking all of the required layers on one die, vendors can reduce costs and development time. But the single-deck approach apparently has reached its limit. “128 layers will be the last one for single deck,” Choe said.

The challenge here is the HAR etch process step. In 3D NAND, you need to etch through a stack of layers in one shot. It’s possible to etch through a stack of 128 layers in one single shot, but beyond that, it becomes difficult.

That’s where the double-deck approach fits in. Many suppliers already have implemented this approach. For example, in a 96-layer device, some are stacking two 48-layer structures on top of each other. In the latest example, Micron is stacking two 88-layer structures on each other, resulting in a 176-layer device.

So beyond 128-layer devices, the double-deck approach will become the norm. This approach is somewhat easier to implement. In simple terms, it’s easier to perform the HAR etch step with less layers. But all this adds more steps and cost to the equation. Instead of a monolithic die, vendors are basically developing two separate structures and stacking them.

In all cases, the 3D NAND process flow is complex.

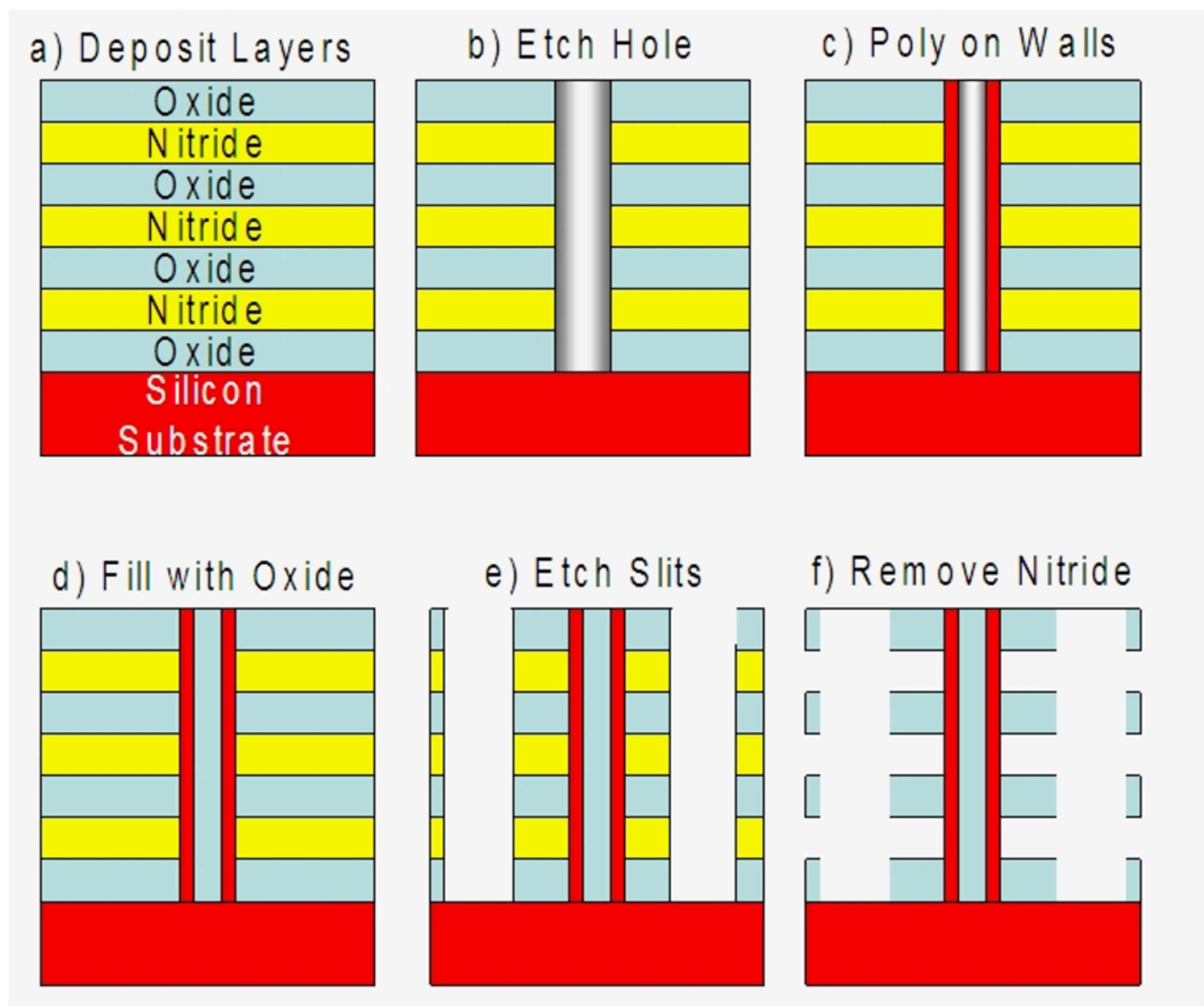


Fig. 3: 3D NAND process flow. Source: Jim Handy, The Memory Guy

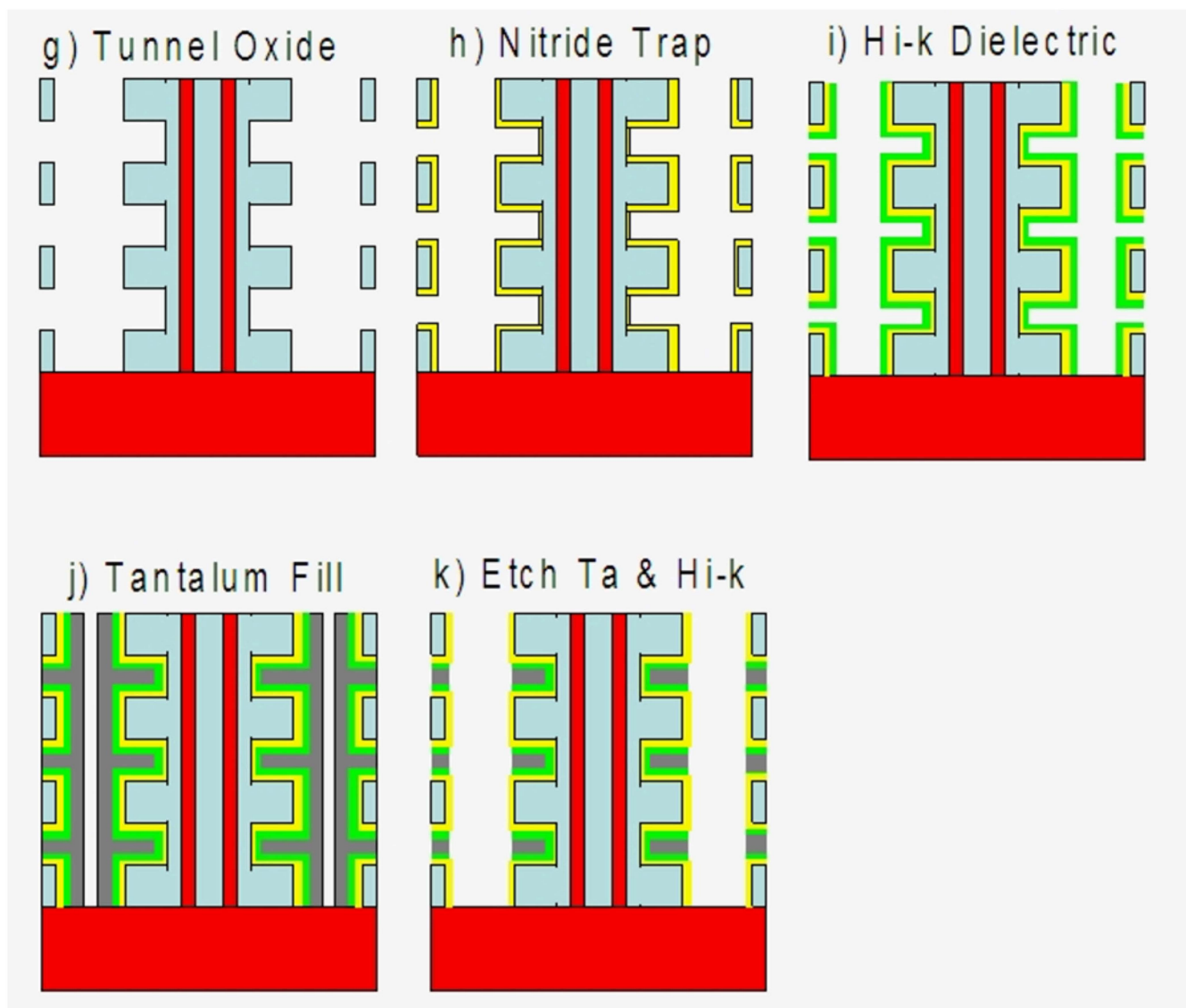


Fig. 4: 3D NAND process flow. Source: Jim Handy, The Memory Guy

The process starts with a substrate. Then, vendors undergo the first challenge in the flow — alternating stack deposition. Using [chemical vapor deposition](https://semiengineering.com/knowledge_centers/manufacturing/process/deposition/chemical-vapor-deposition/) (CVD), alternating stack deposition involves a process of depositing and stacking thin layers on the substrate.

First, a layer of material is deposited on the substrate, followed by another layer on top. The process is repeated several times until a given device has the desired number of layers.

Each vendor uses a different set of materials to create a stack of layers. For example, in Samsung's 3D NAND technology, the company deposits alternating layers of silicon nitride and silicon dioxide on the substrate.

In theory, suppliers can stack an unlimited number of layers. But as more layers are added, the challenge is to stack the layers with the exact thickness and good uniformities. There are other major challenges, as well.

"One is the stress in the films that builds up as you deposit more and more layers, which can warp the wafer and distort the patterns. So when you go double deck or triple deck, alignment becomes a bigger challenge," said Rick Gottscho, CTO of Lam Research.

There are solutions on the process control side. “As the number of 3D NAND layers increases to 176 and higher, there are many process control challenges,” said Masami Aoki, Asia region director for process control solutions at KLA. “As the film stacks grow higher, they induce stress on the wafer, ultimately distorting the surface planarity of the wafer. These warped wafers impact the uniformity of downstream processes and patterning integrity, ultimately affecting final yield. For 3D NAND, as the number of layers increases, the extent of potential wafer warpage also increases. KLA’s new patterned wafer geometry system has wider warp dynamic range in order to characterize these high stack wafers and provide fab engineers with the information needed to inform process decisions.”

Following this step, meanwhile, is the hardest part of the flow — HAR etch. For this, the etch tool must drill tiny circular holes or channels from the top of the device stack to the bottom substrate. The channels enable the cells to connect with one another in the vertical stack.

In this process, a carbon-based material is first deposited on the stack. That material becomes a hard mask. The next step is to pattern holes on the top of the hard mask.

Then, the HAR etch tool drills tiny vertical channels in the die at aspect ratios of 70:1. “You are using different chemistries. You’re going after certain etch profiles, especially for high-aspect ratio etching. That’s becoming extremely critical,” said Ben Rathack, vice president and deputy general manager for [TEL](https://semiengineering.com/entities/tel/) (<https://semiengineering.com/entities/tel/>).

This is a difficult process. A device may have millions of tiny channels in the same chip. Each channel must be parallel and uniform. And as the etch process penetrates deeper into the channels, the etch rates tend to decrease. CD variations may also occur in the holes.

“As in the case of etching, we’re working on different approaches to increase the inherent etch rate so that you don’t have such a falloff as you increase the aspect ratio,” Lam’s Gottscho said.

There are other challenges. “For 176 and higher layer 3D NAND devices, memory manufacturers are implementing a two-tier structure,” KLA’s Aoki said. “The difficulty lies in lining up the channel holes from tier to tier so that electrons can flow unimpeded. Physical stress from the higher film stack creates lithography challenges, while thermal stress during upper deck film deposition can result in lower channel dislocation. Not only is overlay control critical, but also monitoring for wafer warp and channel hole etch profile variability.”

The other difficult part is to measure the uniformities and profiles inside the individual channels. The challenge is to determine where the variations are located and to make the measurements using an assortment of metrology tools.

“Higher-aspect ratio structures will bring new and thicker hard masks and wider pitch wordlines, further challenging traditional metrology capability,” said Scott Hoover, senior director of strategic product marketing at [Onto Innovation](https://semiengineering.com/entities/onto-innovation/) (<https://semiengineering.com/entities/onto-innovation/>). “Higher-aspect ratio channel hole and wordline isolation further erodes the correlation between scribe line targets and device structures. [Metrology](https://semiengineering.com/knowledge_centers/manufacturing/process/metrology/) (https://semiengineering.com/knowledge_centers/manufacturing/process/metrology/) for these applications will need to move to in-die, on-device, and in doing so in concert with higher-aspect ratio structures.”

Following that step, the tiny vertical channels are lined with a polysilicon material, and the channels are then filled with oxide. As the vertical channels become taller with more layers, there are more challenges, namely channel mobility. “Channel mobility is a critical challenge to continue WL stacking,” said Naga Chandrasekaran, senior vice president of technology development at Micron, in a paper at IEDM. “Polysilicon channel mobility and variability are

highly dependent on grain size and trap density. Although several materials have been considered for alternative channel materials like SiGe, Ge, metal induced lateral crystallized silicon, III-V, the current industry standard of engineered polycrystalline silicon is still the best-known material for this application.”

At this point, the gate is formed, along with the storage media for the memory cells. For the storage media, most vendors have implemented a charge-trap flash technology. Charge-trap stores the electric charges in the insulators.

For years, Micron and Intel develop 3D NAND based on the rival floating-gate architecture. Floating gate stores the electric charge in the conductors of the cell. Starting at 128 layers and continuing with 176 layers, Micron moved from floating gate to charge trap. Under the auspices of SK Hynix, Intel will continue to develop 3D NAND with floating gate.

To develop the gate and charge-trap technology, most vendors use a replacement gate or gate-last process. On each side of the tiny vertical channels, two vertical columns are formed, which extend from the top to the bottom of the device.

Then, in Samsung’s TCAT flow, the original nitride layer is removed from the structure. “The entire tower is then coated with a silicon dioxide tunnel dielectric layer, followed by a silicon nitride charge trap, and then the alumina high-k gate dielectric,” Objective Analysis’ Handy said in a blog.

The remaining gaps in the structure are filled with the tantalum nitride control gate material. The resulting structure is a vertical NAND string of TANOS (tantalum-alumina-nitride-oxide-silicon) transistors, according to Handy.

At that point, the device is filled with a tungsten conductive metal gate material. Finally, the peripheral logic is connected to the control gates. “3D NAND array is built with a gate-all-around (GAA) cell architecture. 3D NAND cells are ~20x larger in cell area and ~8x more electrons per 1V Vt shift compared to the scaled planar NAND cells (<20nm). This larger area results in improved reliability, improved Vt distribution and reduced interference,” Micron’s Chandrasekaran said.

Other approaches

Others are moving towards different approaches. In early 2020, Kioxia and WD rolled out its latest 3D NAND technology, a 112-layer device.

Then, in 2021, Kioxia and WD are expected to move to a 160-layer technology based on a new split-gate architecture. The new device will likely stack two 80-layer structures on top of each other, forming a 160-layer device.

In split-gate, circular-shaped control gates are formed, which are then split into two smaller semicircular gates. By splitting the gate into two parts, the cell size is reduced by half, thereby increasing the capacity.

“The circle-shaped control gate provides a larger program window with relaxed saturation problems because of the curvature effect, where carrier injection through the tunnel dielectric is enhanced while electron leakage to the block dielectric is lowered,” said Makoto Fujiwara, a researcher at Kioxia, in a paper at IEDM in 2019. “In this split-gate cell design, the circular control gate is symmetrically divided into two semicircular gates to take advantage of the strong improvement in the program/erase dynamics.”

To make a semicircular 3D NAND memory cell, a vendor stacks alternating layers of silicon oxide and silicon nitride on a substrate. Vertical channels are formed, followed by the formation of the cell stack films. The sacrificial silicon nitride layer is stripped and replaced by a control gate metal, according to Kioxia.

Meanwhile, China's YMTC, the wild card in 3D NAND, last year shipped its first product, a 64-layer 3D NAND device. YMTC skipped the 96-layer generation and is moving to 128-layer technology. The company is sampling 128-layer parts.

YMTC takes a different approach than others. It processes the periphery circuits and memory array on two separate wafers. Then, it stacks and joins them using a copper hybrid bonding technique. The periphery circuits are above the memory, enabling higher bit density. But this bonding technique is still expensive.

YMTC is still a small player in the market, but it potentially could disrupt the status quo. YMTC's chips are being incorporated in USB cards and SSDs from China-based companies. If Chinese OEMs adopt YMTC's technology, "it could become a disruptive situation in NAND market share," TechInsights' Choe said.

Conclusion

Clearly, the 3D NAND market is dynamic. Many players are competing in a tough but large market. Today, prices are under pressure, which impacts margins.

But amid an explosion of data in the market, there is always a need for more memory and storage in systems. "We are optimistic about the long-term demand for NAND flash memory," said Amy Leong, senior vice president at [FormFactor](https://semiengineering.com/entities/formfactor/) (<https://semiengineering.com/entities/formfactor/>).

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