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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

- - - - - x
MICRON TECHNOLOGY, INC. :
Petitioner, : Case IPR2025-00191
v. :
YANGTZE MEMORY TECHNOLOGIES : U.S. Patent No.
COMPANY, LTD., : 11,581,322
Patent Owner. :
- - - - - X

Deposition of JACK C. LEE, Ph.D.
Conducted Virtually
Thursday, October 23, 2025
10:08 a.m. EDT

Job No.: 601327
Pages 1 - 68
Reported by: Debra A. Whitehead

1 Deposition of JACK C. LEE, Ph.D., conducted
2 virtually.

3
4
5 Pursuant to notice, before Debra Ann Whitehead,
6 E-Notary Public in and for the Commonwealth of
7 Virginia.

1 A P P E A R A N C E S

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1 A P P E A R A N C E S C O N T I N U E D

2 ALSO PRESENT:

3 SUE PYBAS, A/V Technician

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C O N T E N T S

EXAMINATION OF JACK C. LEE, Ph.D.	PAGE
By Mr. Grabowski	6

EXHIBITS MARKED IN TODAY'S SESSION

(Attached to the Transcript)

LEE DEPOSITION EXHIBIT	PAGE
Exhibit A Transcript of 1/30/25 Deposition of Jack Lee, Ph.D.	61
Exhibit B Transcript of 7/30/25 Deposition of Jack Lee, Ph.D.	62

EXHIBITS MARKED IN PRIOR SESSIONS

(Not attached)

DEPOSITION EXHIBIT	PAGE
Exhibit 1003	13
Exhibit 1005	42

1 P R O C E E D I N G S

2 JACK C. LEE, Ph.D.,

3 having been duly sworn, testified as follows:

4 EXAMINATION BY COUNSEL FOR PATENT OWNER

5 BY MR. GRABOWSKI:

6 Q Dr. Lee, my name is Alex Grabowski. I am
7 here on behalf of the patent owner. With me is
8 Bobby Dunteman. We're from the law firm of Latham
9 & Watkins.

10 If you wouldn't mind while we start off
11 just stating your name and business address, for
12 the record.

13 MR. LANG: I should just state my name,
14 for the record. Jason Lang, from Orrick,
15 Herrington, on behalf of Micron and Dr. Lee.

16 Q All right. And with that, Dr. Lee, if
17 you wouldn't mind stating your name and business
18 address, for the record.

19 A My name is Jack Lee. And I'm residing in
20 Austin, Texas. My address is 5803 West Loop Cove,
21 Austin, Texas, 78731.

22 Q All right. And have you ever been

1 deposed before?

2 A Yes.

3 Q About how many times?

4 A I don't recall. Maybe 30 times.

5 Q All right. Well, then I'll just give you
6 a quick refresher on the rules so we're all on the
7 same page.

8 I'm going to ask questions, and you will
9 give answers.

10 Is that all right?

11 A Yes.

12 Q And it will help if they are verbal
13 answers, not nodding or shaking your head, so the
14 court reporter can get them down.

15 Is that okay?

16 A Yes.

17 Q By that same token I'll try not to talk
18 over you, and I would ask you to do the same so we
19 can get a clear record, if that works?

20 A Yes.

21 Q All right. If you don't understand any
22 of my questions, I'm happy to clarify them if you

1 ask, otherwise I will assume you've understood
2 them.

3 Is that fair?

4 A Yes.

5 Q All right. From time to time your lawyer
6 may make objections. You understand that if he
7 doesn't instruct you not to answer, you still have
8 to answer the question. Right?

9 A Yes.

10 Q We'll have an opportunity to take breaks
11 probably every hour or so. If you need a break
12 that I'm not calling for, feel free to ask for
13 one. The only thing I ask is that you answer any
14 pending question before we go on a break.

15 Is that all right?

16 A Yes.

17 Q Then just a couple of questions I have to
18 ask everyone. Are you taking any medications that
19 may impact your ability to give truthful,
20 complete, and accurate testimony today?

21 A No.

22 Q Are there any other reasons you cannot

1 give truthful, complete, and accurate testimony
2 today?

3 A No.

4 Q All right. Then because this is a remote
5 deposition, I just have a few questions about your
6 setup.

7 Is there anyone else in the room with
8 you?

9 A No.

10 Q Do you have any notes in front of you?

11 A No.

12 Q Do you have any documents in front of
13 you?

14 A No.

15 Q Other than the computer you're using to
16 connect to the Zoom, do you have any other
17 computers, phones, or devices in front of you?

18 A No.

19 Q Other than this Zoom, are there any
20 applications open on your computer?

21 A No.

22 Q Your prior depositions, were you acting

1 as an expert witness in all of them?

2 A I believe so.

3 Q What did you do to prepare for your
4 deposition today?

5 A I have reviewed my declarations, my --
6 yeah, my declaration. I reviewed all the
7 documents listed in the -- in my declaration.
8 There's a table that listed all the exhibits. I
9 reviewed the '322 patent. I also reviewed any
10 document that's -- I think that's mainly it.

11 And then I obviously have worked with my
12 counsel to discuss about --

13 MR. LANG: I'll just -- I'll just counsel
14 the witness, or instruct the witness, not to
15 disclose communications that you had with counsel.
16 But as far as, you know, the fact that you may
17 have met with counsel or for how long, you can
18 disclose that.

19 A Yeah, I met with the counsel in
20 preparation.

21 Q And how many meetings with counsel were
22 there?

1 A I don't recall. The last couple of weeks
2 we have met at least a few times.

3 Q Were all those meetings specifically to
4 prepare for this deposition?

5 A Yes.

6 Q Was Mr. Lang at those meetings?

7 A Yes.

8 Q Any other lawyers?

9 A No.

10 Q Anyone other than Mr. Lang?

11 A No.

12 Q About how long in total did you spend in
13 these meetings?

14 A I don't -- I have not taken the
15 accounting of that. A few hours each meeting. I
16 don't -- I don't recall exact time that we spent
17 each time.

18 Q Separate from those meetings, did you
19 speak to anyone other than Mr. Lang to prepare for
20 this deposition?

21 A No.

22 Q When were you first contacted about these

1 proceedings?

2 MR. LANG: Objection. Form.

3 A I'm not sure what you mean by that. Do
4 you mean by the proceeding of this particular IPR
5 or in general the case? Because there are many
6 other patent and many other IPR in this case.

7 Q Yes. So I guess this set of IPRs in the
8 case generally, let's start there.

9 A I don't recall exactly. Yeah, some time
10 last year maybe. Yeah, I don't -- I don't recall
11 exactly when, when it was that I started working
12 on this case.

13 Yeah, I think it's early last year.
14 2024, I'm sorry.

15 Q Do you recall when you were specifically
16 contacted first about this IPR?

17 A It must -- it must have been some time in
18 the October, November -- somewhere around there,
19 time frame. I don't recall exactly the time.

20 MR. GRABOWSKI: Could we please bring up
21 Exhibit 1003, which should be Dr. Lee's
22 declaration.

1 (Exhibit 1003, previously marked, not
2 attached.)

3 A Are you uploading that to the Chat?

4 A/V TECHNICIAN: It should be in the chat
5 right now. It may take a second to upload.

6 A I've got it. Okay.

7 Q All right. Were you able to access it?

8 A Yes.

9 Q All right. And you see it on the screen
10 as well?

11 A Yes.

12 Q Perfect.

13 You recognize Exhibit 1003 as the
14 declaration you submitted in connection with this
15 IPR?

16 A Yes.

17 Q And this declaration contains your
18 complete opinions on U.S. Patent Number
19 11,581,322. Correct?

20 MR. LANG: Objection to form.

21 A Can you repeat the question, please.

22 Q This declaration contains your complete

1 opinions concerning U.S. Patent Number 11,581,322?

2 MR. LANG: Same objections.

3 A As of this -- as of this point I believe
4 my opinion is included in this declaration.

5 Q And if I refer to that patent as the '322
6 patent, you'll know what I mean. Right?

7 A Yes.

8 Q As you sit here today, are there any
9 mistakes you're aware of in this declaration?

10 A I don't -- there might have been. There
11 might have been some typo, but I don't recall any
12 substantive mistake.

13 Q Who wrote this declaration?

14 A Well, it is a collaboration with counsel
15 in writing this IPR declaration. Obviously I'm
16 not a lawyer, so -- and this is a legal document
17 that I would rely on counsel in taking -- showing
18 the particularly related to the law.

19 Q And how long did you spend preparing this
20 declaration?

21 A You mean in terms of preparing the
22 writing of the declaration plus the forming my

1 opinion in the declaration?

2 Q Yeah. Everything that went into it; the
3 research, the writing, the revisions, discussions
4 with counsel.

5 A I don't recall exactly. Because as you
6 know, there are many -- there are quite a few IPR
7 in this case, and so I -- and many issues are very
8 similar. So there is some issues and the
9 write-up, you know, can be -- can be used at --
10 for more than one IPR.

11 So it's hard to -- hard to tell how many
12 hours in total that I prepared for this
13 declarations. But it must be, you know, quite a
14 few number of hours.

15 Q Do you have a ballpark sense of what you
16 mean by "quite a few"?

17 A I don't recall exactly, but I would say
18 at least 30, 40, 50 hours.

19 Q And your declaration concerns a number of
20 references involved in obviousness combinations.

21 Right?

22 A Yes.

1 Q Who provided those references for the
2 declaration?

3 A Some of them I provided, and some of them
4 are provided by -- by counsel. And, again, some
5 of the -- there are many IPRs. Some of them are
6 used in multiple IPR.

7 So with -- when there are so many
8 exhibits and prior art, I lose -- I lost count of
9 how many I provided and how many are provided by
10 counsel, including Jason and other folks in the
11 firm.

12 Q All right. We can talk about that more
13 when we get to specific references.

14 For now, did you talk to any nonlawyers
15 to prepare your declaration?

16 A No.

17 Q You understand your declaration relates
18 to the concept of obviousness in patent law.

19 Right?

20 A Yes.

21 Q Do you have an understanding of what
22 obviousness means in the context of patent law?

1 A I'm not a lawyer. But my understanding
2 of the law related to -- related to this IPR is
3 described in Section 4 of my declaration.

4 MR. GRABOWSKI: Could we go to PDF Page
5 12, please.

6 Q And is this Section 4 here starting on
7 Page 12 what you're referring to?

8 A Yes.

9 Q Your opinion relates to four grounds of
10 invalidity. Right?

11 A Yes.

12 Q Is it your understanding that all four of
13 those grounds are based on obviousness?

14 A Yes.

15 Q And all four of those grounds rely on
16 the -- well, strike that.

17 Are you familiar with the concept of a
18 person of ordinary skill in the art?

19 A Yes.

20 Q And all four of the obviousness grounds
21 in your opinion rely on the knowledge of a person
22 of ordinary skill in the art as part of their

1 combinations. Right?

2 A Yes. In addition, in Ground 2, 3, and 4,
3 in addition to relying on the knowledge of a
4 POSITA, also rely on more than one prior art.

5 Q And Ground 1 relies on a single prior art
6 reference and the knowledge of a POSITA. Correct?

7 A Ground 1 relies on Nishikawa in view of
8 the knowledge of a POSITA.

9 Q Have you ever heard the term
10 "anticipation" in the context of patent law?

11 A Yes.

12 Q Do you have an understanding what that
13 term means?

14 A I don't have it with me. I don't
15 believe -- hold on one second. Let me search.

16 I don't -- because in this IPR, as I
17 mentioned, all four grounds are relying on
18 obviousness argument. So in Section 4 I did not
19 offer my understanding of what is anticipation.

20 Hello? Okay.

21 But if I recall, I believe that
22 anticipation means that there's a single prior art

1 reference that disclose every limitation of the
2 claim, a challenged claim.

3 Q So -- oh, I apologize.

4 A Either expressively -- expressly, sorry,
5 or inherently. That's my understanding. I might
6 be totally wrong. I'm not a lawyer. You are a
7 lawyer, so you can tell me what I have said wrong.

8 Q I'll try and short-circuit the need for
9 that.

10 You're not offering the opinion in your
11 declaration that any claims of the '322 patent are
12 anticipated. Right?

13 A No. I think all four ground, as I
14 mentioned, my opinion based on obviousness
15 argument.

16 Q Perfect. Then we can get out of the law
17 and into something where you're the expert. I
18 want to talk a little bit about the design and
19 manufacturing of 3D NAND.

20 Fair to say that's something you're
21 familiar with?

22 A Yes.

1 Q And would you agree that as a general
2 matter, designing and manufacturing 3D NAND memory
3 devices is a complex process?

4 A Well, it really depends on who you talk
5 to.

6 If you talk to somebody who is not in the
7 area of -- in the area of engineering, let's say,
8 you know, a lawyer. I'm sorry.

9 Q That's okay.

10 A And, you know, it might be very
11 complicated. But if you're talking to somebody
12 who has experience, professional experience
13 working with NAND flash memory, then it is not too
14 complicated.

15 Q Fair to say it's something that requires
16 a deal of specialized knowledge?

17 A Well --

18 MR. LANG: Objection to form.

19 A -- I don't know what you mean by
20 "specialized."

21 Q I guess I'm just trying to understand
22 your answer, which -- and I'm not trying to put

1 words in your mouth. But it sounds like what you
2 said, it's not complex as long as you have a Ph.D.
3 in doing it?

4 MR. LANG: Objection. Mischaracterizes
5 the testimony.

6 A I didn't say a Ph.D.

7 As I describe in my declaration, what a
8 POSITA -- the qualification of a POSITA, which is
9 a bachelor degree in electrical engineering or
10 similar discipline, along with two to three year
11 of professional experience working with NAND flash
12 memory devices or equivalent of -- level of skill,
13 "working with" meaning, researching, designing, or
14 teaching.

15 And this -- and this also depending on
16 the experience, for example, advanced degree might
17 replace some of the professional experience.

18 So this is all described in Section 5 of
19 my declaration.

20 Q All right. Are you familiar with the
21 term "memory density" in the context of 3D NAND
22 memory?

1 A I believe that -- let me take a look at
2 my declaration. I believe I said that in my
3 declaration.

4 So 3D, I did not -- I don't think I have
5 this specifically gave a definition of what is a
6 memory density. But in 3D NAND, memory density in
7 general refers to how many data storage, or how
8 much data storage can be packed in a given area.
9 In general, measure as the number of gigabits per
10 square millimeter or bits per wafer.

11 So, obviously, that the higher the memory
12 density, the better it is in terms of cost, in
13 terms of yield, and so on and so forth.

14 Q And would you agree that memory density
15 is limited by fabrication processes?

16 MR. LANG: Objection to form.

17 A Can you repeat that again?

18 Q Would you agree that memory density is
19 limited by fabrication processes?

20 MR. LANG: Same objection.

21 A Well, the memory density is affected by
22 many factors. For example, number of layers,

1 and -- on the chip. The more layer, the more bit
2 per unit area you can have. Number of bits per
3 cells. And whether you have 2 bit per cell, 3 bit
4 per cell, or 4 bit per cell. The larger the
5 number of bits per cell increase -- increase the
6 density per physical cells.

7 So that's not really a -- that's not only
8 depending on the manufacturing process, but also
9 determined by the circuit designed. And it also
10 depends on the peripheral circuit, where they are
11 placed, whether it's placed on the side or on --
12 on the -- if it is under the array, then it would
13 increase the effective density.

14 And it also -- the memory density also
15 depend on, you know, how much -- how many stack
16 you have, how much the -- whether it is a --
17 whether structures are in the form of trench or
18 circular geometry.

19 So that's the only depends on -- that's
20 not depending on the fabrication process but
21 rather than -- rather depend on the layout. And
22 the peripheral circuit also depends on the circuit

1 design, and the layout itself.

2 So I think it's too simplistic to say
3 that the memory density depends on the
4 manufacturing process.

5 Q So I didn't mean to imply that the memory
6 density was solely dependent on the manufacturing
7 process.

8 A I'm sorry. I misunderstood.

9 Q No. It was a bad question. I just want
10 to make sure.

11 Can we agree that fabrication processes
12 are one of the constraints on memory density?

13 A In addition to other consideration; for
14 example, the list that I mentioned.

15 Q And could we go to Paragraph 205 of your
16 report. It is PDF Page 109.

17 A Paragraph 209?

18 Q Paragraph 205, Page 109.

19 A Right.

20 Q And do you see the last two sentences
21 there that start, "In 3D NAND, this requires"?

22 A Yes.

1 Q And it's talking about forming
2 high-aspect ratio holes through the stack. Right?

3 A Right.

4 Q And you say that those high-aspect holes
5 became a limiting factor to memory density?

6 Do you see that?

7 A Yes.

8 Q Oh, what did you mean by that?

9 A Well, one of the problem associated with
10 high aspect ratio geometry is that when you etch a
11 very deep high-aspect ratio hole in a memory
12 stack, because of the nature of the etching, it
13 will cause what is called a tapering of the hole.
14 That is that the hole will start out with pretty
15 wide. As it go down to a deeper region it becomes
16 narrower and narrower. Obviously that is
17 undesirable, and that would limit your -- what did
18 I say? It will limit the limiting factor to
19 memory density.

20 Q What causes that tapering?

21 MR. LANG: Objection to form.

22 A I believe I describe that in my

1 declaration. Let me find that. Hold on one
2 second.

3 I know -- hold on.

4 Sorry, I thought I describe directly of
5 what the cause of the tapering, but not directly.

6 So in general when you -- sorry. When
7 you etch an high-aspect ratio hole, like memory
8 hole or channel hole in the 3D NAND stack,
9 tapering means, like I said, the hole become
10 narrower at the bottom compared to the top. And
11 the reason is that -- that when you do a etching,
12 that the reactive species, whether it's ion or
13 radicals from the plasma have harder time to reach
14 the bottom. Right?

15 And meanwhile, the byproduct of the
16 etching and the neutral byproducts have difficulty
17 of escaping. And which it's in a sense kind of
18 block the opening and block the reactive ion going
19 in there. And so that's one reason.

20 Another reason is that when you have
21 plasma, the ions loses energy as it go into the
22 hole when it collide with the side wall or the

1 neutral byproduct accumulating near the top before
2 reaching the bottom.

3 So -- so when you -- when the ion have
4 less energy, then it reducing -- it reduces the
5 bombardment effect at the bottom, and that the
6 etching rate would become slower.

7 So those are just -- there are many
8 other, many other factors, and you can look up in
9 textbook. That's, you know, an entire section, so
10 multiple pages describe this tapering effect. But
11 that's just two of those reason why we have
12 tapering.

13 Unless you want me to, if you want me to,
14 I can go into even more detail about other effect.

15 Q I actually would be curious to hear,
16 yeah, what else causes tapering. Or what other
17 effects are playing a role, I guess I should say.

18 A Okay. So I was talking about, like, you
19 know, it have the two -- two effect, energy loss,
20 and also harder time for ion to reach the bottom.

21 And then there's also polymer depositions
22 when you have the etching, the plasma etching

1 that, for example, that uses CF₄ or CHF₃ or --
2 CHF₃, yeah. That creates some polymer and can
3 deposit on the side wall, and therefore lower the
4 diameter as you go deeper and deeper.

5 What else? When you etch -- in general,
6 for example, when you etch TAC, through-array
7 contact, you're etching a insulating material.
8 And as you know, insulating material can have
9 charging effect, static charge. Any time you have
10 a charging in the insulator, that can deflect the
11 incoming ion, and which basically create an effect
12 which even instead of going straight down, it
13 basically bouncing back and forth due to this
14 charging effect.

15 And then there's also pressure effect.
16 Let me see. If you have -- in general you want to
17 have more ion. Right? You want to have more ion
18 to have a faster etch rate to improve the
19 throughput. But when you have higher pressure,
20 you also create what is called a scattering
21 effect. In other words, that ions tend to bounce,
22 collide with each other.

1 And at higher pressure, so call a mean
2 free path between collisions becomes smaller and
3 smaller. It collide more frequently. And that
4 lead to poor directionality.

5 In other words, what you'd like to do is
6 have the ion to have more vertical etch in a very
7 high aspect ratio etching. So you have more
8 directional etch. But here you have, due to
9 scattering, you have the directionality become
10 less. So that also cause limited gas diffusion
11 into the deeper region.

12 I think those are the ones that -- those
13 are some of the effect that come to my mind. I'm
14 sure that I have missed a few others.

15 Q Understood. It certainly sounds like
16 there's a lot at play.

17 You had mentioned in your answer etching
18 a TAC.

19 Would these effects be more prevalent the
20 smaller the TAC opening is?

21 A Well, obviously the higher the aspect
22 ratio, the more tapering you have in this -- in

1 the etching.

2 So when you say the TAC is larger, that
3 really depends on -- when you say the TAC has a
4 larger diameter, does the height remain -- the
5 depth remain the same, or is it also
6 correspondingly deeper.

7 So it's not -- it's not just the diameter
8 of the hole but also the depth of the hole that's
9 important.

10 Q So --

11 A Does that make sense?

12 Q That makes sense.

13 So two holes of equal depth, the one with
14 the smaller diameter is going to experience more
15 pronounced versions of these effects?

16 Is that right?

17 A Yeah. Two holes with -- of the same
18 depth, the narrower the hole means that it's a
19 higher aspect ratio.

20 So the -- all these problem is related to
21 etching high -- higher aspect ratio hole. So,
22 therefore, you're right that for the same depth,

1 smaller diameter means higher aspect ratio, and
2 therefore, there's tapering effect become more
3 pronounced.

4 Q And were these known issues that a
5 skilled artisan would have been considering at the
6 time of the priority date when designing these
7 sorts of 3D NAND devices?

8 MR. LANG: Objection to form.

9 A As I describe in Ground 2, I list a
10 number of prior art, including Lu, L-U, which
11 is -- I am going to try to find the exhibit
12 number. Including Lu. Tessariol,
13 T-E-S-S-A-R-I-O-L, which is Exhibit 136. Exhibit
14 1040 by Goda, G-O-D-A. Exhibit 1020 by Masamori,
15 M-A-S-A-M-O-R-I. And even -- even textbook,
16 Exhibit 1010 by Micheloni, M-I-C-H-E-L-O-N-I. All
17 these are prior art that addresses -- that address
18 these issues of etching a high aspect ratio hole.

19 So to answer your question, yes, this is
20 well-known way before the priority date of the
21 '322 patent.

22 I might have missed a few prior art that

1 I mention in the section related to Ground 2,
2 which is in the topic of the etching a high aspect
3 ratio and the use of multi-deck 3D NAND stack.

4 Q Okay. Those are helpful.

5 Have you -- strike that.

6 Are you familiar with the process for
7 designing a method of manufacturing a new 3D NAND
8 device?

9 MR. LANG: Objection to form.

10 A Process of designing and manufacturing?

11 Q Designing the method of manufacturing.

12 So once you have the design for the
13 device itself, designing the way of making the
14 device.

15 MR. LANG: Objection to form.

16 A You're asking me something that I am not
17 sure if I address it in my declaration. If I
18 have, can you point to where in my declaration I
19 address that?

20 Q I don't have a specific spot in mind. I
21 am not sure you don't, but I'm not aware of
22 anywhere where you do.

1 I'm just trying to understand your
2 familiarity with the process for designing these
3 methods of manufacturing these devices.

4 MR. LANG: Objection to form.

5 A Well, I don't think -- I'm not sure if I
6 addressed that in my declaration.

7 But in general, I think you first have to
8 establish what kind of 3D NAND structure that you
9 are building, what is the cell type that you are
10 doing, whether it's floating gate or charge trap
11 flash; what is the array architecture. There are
12 many architecture, whether it's circular, vertical
13 channel, or so-called U-shape. How many bits per
14 cell. How many blocks there are. How many
15 wordlines per stack. How do you integrate the
16 peripheral circuit, whether it is on the side or
17 underneath the array, and what is the target
18 performance in terms of endurance, retention, and
19 the bottom line how much the cost that you are
20 targeting.

21 Then when you design the process flow,
22 there's a lot of -- there's some considerations;

1 what starting wafer that you're using, what is
2 the -- we talked about this, the aspect ratio of
3 each hole; whether you use gate replacement
4 process or not. So how do you etch the device,
5 what is the cleaning process. Then you have to
6 usually do some simulations and experimental
7 process.

8 So the question that you have is
9 essentially the same when you try to develop a
10 process not just for 3D NAND but also for a
11 microprocessor or a memory chip such as DRAM.

12 So a person of ordinary skill in the art
13 would understand that it's not such a complicated
14 issues, that these process steps of designing the
15 method of manufacturing a particular chip is
16 well-known in industry. A person of ordinary
17 skill in the art would understand that quite
18 clearly.

19 Q You referred to doing some simulations
20 and experimental work in your answer.

21 What did you mean by that?

22 A Well, the -- in general you like to --

1 there's a lot of tools, so-called computer-aided
2 design tools, that one can use to understand what
3 the electrical behavior is of the device; such as
4 what is a threshold voltage, what is the expected
5 reliability, retention, and endurance.

6 And then typically after the simulation,
7 you would have some experiment. For example, if
8 you want to etch a certain aspect ratio or deposit
9 a certain material, then you would do some
10 experiment to test out those ideas.

11 Again -- and then you would do a
12 cross-sectional TEM or SEM to try to find out
13 whether certain etch is better than -- certain --
14 than other etches.

15 So, again, these are a very standard
16 process in designing the method of manufacturing
17 any chips, whether it's CMOS chips, logic chip,
18 analog chip, or memory chip such as 3D NAND. And
19 it is something that a person of ordinary skill in
20 the art in the field of electrical engineering,
21 particularly, for example, related to '322 patent,
22 would understand very careful -- pretty clearly.

1 Q You mentioned TEM and SEM.

2 Can you just say what those stand for?

3 A TEM stand for transmission electron
4 microscopy. SEM stand for scanning electron
5 microscopy.

6 Q As part of this process for designing 3D
7 NAND memory chips is there any work -- strike
8 that.

9 As part of this process for designing the
10 manufacturing method for 3D NAND memory chips, is
11 there any work that has to be done to sort of
12 qualify or validate that the manufacturing method
13 is actually going to produce a working chip that
14 matches the design?

15 MR. LANG: Objection to form.

16 A I'm not sure I understand your question.

17 Q Yeah. So you -- you had talked about,
18 for instance, testing different etches to see
19 which one was preferable.

20 Did I understand that correctly?

21 A That's an example, yeah.

22 Q And so you're going to have to design a

1 whole manufacturing process from start to finish
2 that builds one of these 3D NAND memory chips.

3 Right?

4 MR. LANG: Objection to form.

5 A Say that again? I'm sorry.

6 Q You're going to have to design a
7 manufacturing process that, start to finish,
8 builds one of these 3D NAND memory chips. Right?

9 A Yeah, eventually.

10 Q Is there -- strike that.

11 As part of that process of coming to a
12 final manufacturing process, is there a
13 qualification or validation that has to be done to
14 show that this manufacturing process will actually
15 build working 3D NAND memory chips that are --
16 that match the design?

17 A Yeah --

18 MR. LANG: Objection. Objection to form.

19 THE WITNESS: Sorry, Jason.

20 A If I understand your question correctly,
21 in semiconducting -- semiconductor process
22 development, there's always validations and

1 verification.

2 Validation means that it's a process that
3 makes sure that the process and design have been
4 implemented correctly according to the
5 specification; in other words, whether we build a
6 process correctly.

7 Validation means that is a process in
8 which we ensure that the final product meet the
9 performance and reliability requirement.

10 So, yeah, whether it's 3D NAND, CMOS,
11 logic CMOS, analog design devices, memory device
12 such as DRAM, mixed signal design or as, you know,
13 AI chips, they all have to go through verification
14 and validations process.

15 And that is something a POSITA would
16 understand and would have understand the detail of
17 verifications and validation.

18 Q I'm sorry, Doctor, I just want to make
19 sure you understand. Because you said I think
20 "validation" twice in that answer. There's --

21 A Last sentence I said?

22 Q No. So you had said, Validation means

1 that it is a process that makes sure the process
2 inside of is implemented correctly. And then you
3 also said, Validation is the process that ensures
4 the final product meets performance and
5 reliability. I just wanted to check if one of
6 those should be verification.

7 A No. The first one is verification.

8 Q Okay. So --

9 A Verification -- verification is a process
10 which you make sure that the process and design
11 are implemented correctly according to the
12 specification.

13 So, and then validation is the testing to
14 make sure that the final product of the chip meets
15 the performance and reliability and functional
16 requirements.

17 Q Have you ever been involved in a
18 validation and verification process for a 3D NAND
19 memory chip?

20 A I have in do consulting in this -- in
21 this area. Not just 3D NAND, but also CMOS chips.
22 And I don't recall exactly whether I have involved

1 in consulting verifications or validations. But
2 I'm sure that I have talked to many engineers
3 about the -- the process of and the
4 implementations of verification and validation
5 procedures.

6 Q Have you ever been involved in changing
7 the design of a 3D NAND memory chip?

8 A I have been teaching at the University of
9 Texas in Austin and work with many outstanding
10 researchers in the area of nonvolatile memory.
11 And specifically we look at how changing the
12 material, changing the process, how that affect
13 the particular metric of the memory devices.

14 So, yes, in my research I have looked at
15 how changing either the design or the process
16 recipe or the process flow, how that change, how
17 those changes affect the final outcomes.

18 And in addition, as I also mentioned, in
19 addition to my research in -- at UT Austin -- by
20 the way, I've graduated more than 40 Ph.D.
21 students and published more than 600 journal
22 papers and conference proceedings. And you can --

1 you can look at it. Many of the papers are
2 related to nonvolatile memory and 3D NAND.

3 And in addition to all the work related
4 to the university, I also do consulting in
5 industry regarding to these processes.

6 MR. GRABOWSKI: All right. We've been
7 going about an hour and ten minutes. This might
8 not be a bad spot to take a break, if that works
9 for you.

10 THE WITNESS: Sounds good.

11 (A recess was taken.)

12 BY MR. GRABOWSKI:

13 Q Dr. Lee, are you familiar with the term
14 "dummy channels"?

15 A Yes.

16 Q What's your understanding of the term
17 "dummy channel"?

18 A Oh, I believe I describe that in my
19 declaration. Let me get there.

20 Okay. In Paragraph 61. In short, dummy
21 channel structures are inactive memory strings.

22 Q So dummy channels don't have memory

1 capacity.

2 Is that right?

3 MR. LANG: Objection to form.

4 A Dummy channel does not serve the purpose
5 of memory functions, that's why it's called the
6 inactive memory string, or dummy channel.

7 MR. GRABOWSKI: Could we please have
8 Exhibit 1005.

9 (Exhibit 1005, previously marked, not
10 attached.)

11 Q Do you recognize Exhibit 1005?

12 A Yes.

13 Q This is the Nishikawa reference you
14 relied on in forming some of your opinions in this
15 case. Correct?

16 A Yes.

17 Q Now, Nishikawa 1005 here doesn't disclose
18 the use of dummy channels. Right?

19 MR. LANG: Objection to form.

20 A As I discuss --

21 THE WITNESS: Sorry, Jason.

22 MR. LANG: Objection to form.

1 A As I discuss in Paragraph 140, Nishikawa
2 discusses channel structures, that is the memory
3 stack structure 55. And a POSITA would have been
4 motivated with reasonable expectation of success
5 to include dummy channel of either the same
6 material or with a solid dielectric field in
7 Nishikawa's memory stack. And I listed a number
8 of reasons for it.

9 And furthermore, as I describe in
10 Paragraph 43, Nishikawa also published -- also
11 issue another patent, which I call Nishikawa2, in
12 Exhibit 1046 that Nishikawa2 recognizes the need
13 of adding dummy channel, what they call -- what he
14 call support pillars, dielectric support
15 structure.

16 Q So I appreciate that it's your opinion
17 that a POSA would add dummy channels to Nishikawa.
18 I'm just trying to understand sort of the
19 predicate point.

20 So can we agree that the Nishikawa
21 reference itself doesn't have dummy channels?

22 MR. LANG: Objection to form.

1 A Nishikawa Exhibit 1005 does not
2 explicitly or expressly disclose dummy channel
3 structure.

4 Q Okay. But it's your opinion that a POSA,
5 based on their general knowledge or based on
6 Nishikawa2, would add dummy channels to
7 Nishikawa's memory array?

8 Is that right?

9 MR. LANG: Objection to form.

10 A A POSITA would have been motivated to add
11 dummy channel to Nishikawa, especially considering
12 that the same inventor recognized the need of
13 adding dummy channel and show embodiment and
14 examples of adding these dummy channel.

15 Q And in your opinion, would the POSITA add
16 those dummy channels to the memory array in
17 Nishikawa?

18 MR. LANG: Objection to form.

19 A In general the dummy channel can be added
20 around the perimeter or the edge of the memory
21 array or in the staircase region as I describe,
22 let me see, in Paragraph 143. And I showed a lot

1 of examples, and including Exhibit 1027 by Kai,
2 K-A-I.

3 So in Paragraph 89 I also showed an
4 example in Figure 17 of Nishikawa2 in which
5 Nishikawa add dummy structure, which is Number 66,
6 next to the regular -- next to the rail channel
7 structure. And it does not reduce the storage
8 density by adding the dummy channel.

9 What I mean is by -- in answering your
10 question, depending on how the memory array is
11 designed, one can add dummy channel in the memory
12 array.

13 But in general the dummy channel added to
14 the perimeter on the edge of the memory array
15 and/or in the staircase region, and such that they
16 do not cause an effect or reduction of the memory
17 density.

18 Q So I'm looking at Paragraph 89. Am I
19 correct that in these figures here for Nishikawa
20 and Nishikawa2, Element 55 is the actual memory
21 channel and Element 66 is the dummy -- this is
22 Exhibit 1003. It's on PDF Page 45.

1 A Yeah, if you look at Nishikawa2, which is
2 Exhibit 1046, in Column 22, it says, Dielectric
3 pillar structure 66. So that is what Nishikawa
4 call as their dummy channel. And in the same
5 column it describe Element 55 as the memory stack
6 structure, which is the memory channel.

7 Q Okay. Then looking at Paragraph 89 of
8 Exhibit 1003, which is your declaration, you've
9 got figures for Nishikawa and Nishikawa2.

10 Correct?

11 A That is correct.

12 Q And both of them show four rows of six
13 channels?

14 Is that right?

15 A You can say that, yes.

16 Q And in the Nishikawa diagram on the left
17 without dummy channels, that's four rows of six
18 channels, all of which are active. Right?

19 A Right.

20 Q And in the Nishikawa2 diagram on the
21 right, one channel in each row is replaced with a
22 dummy channel. Right?

1 A Well, that figure is just an example. As
2 you can see, that there are more rooms to add more
3 channel or dummy channel. Considerably a person
4 of ordinary skill in the art, Nishikawa, could add
5 more -- Nishikawa2 can add or to place the dummy
6 channel on the edge of the row of six memory
7 channels.

8 So it is just show, this is just an
9 illustration of adding dummy channel within the
10 array, not for the purpose of what you just did,
11 is comparing Figure 16 from Nishikawa and Figure
12 17 in Nishikawa2. And it's not the purpose to
13 saying that, Look, adding a dummy channel would
14 reduce the memory density; it's the opposite.

15 It's basically saying that, Look, you can
16 add dummy channel within the array or at the edge
17 or the perimeter or the -- even in the staircase
18 of the array. And either cases -- either case it
19 would not change the memory density.

20 So I think it is inappropriate to compare
21 the two figures and concluded that the number of
22 memory channel is reduced from one to another.

1 Q So, Dr. Lee, am I correct that you
2 selected these two figures for side-by-side
3 inclusion in your declaration?

4 MR. LANG: Objection to form.

5 A What I select those two is to show that,
6 as I mentioned in the sentence in Paragraph 89, to
7 show that Nishikawa2 relate to the same memory
8 architecture of Nishikawa.

9 It is not the purpose of counting the
10 number of black dots versus the number of white
11 dots, 55 versus 66, and for the comparison between
12 Nishikawa and Nishikawa2. That was not the
13 purpose of selecting those two figures. And no
14 one of POSITA would read the declaration or to
15 read Nishikawa and Nishikawa2 to conclude that
16 adding dummy channel would change the memory
17 density.

18 In fact, the conclusion of reading the
19 two Nishikawa, Nishikawa and Nishikawa2, a person
20 of ordinary skill in the art would conclude that
21 adding a dummy channel would not change the memory
22 density. At the same time, would have added

1 benefits, as I discuss in my declaration between
2 Paragraph 140 and 149, I believe.

3 Q We can agree, though, that at a minimum a
4 dummy channel would take up space in the lateral
5 direction of the staircase. Right?

6 A I'm not sure what you mean by "take up
7 space."

8 Obviously that adding a dummy channel in
9 the staircase region would -- is a -- one element
10 added to that region. But the bottom line is
11 that, as we mentioned before, memory density is an
12 important parameters in 3D NAND. The important
13 point is that adding dummy channel in the
14 perimeter or the edge of the memory array or in
15 the staircase region, do not change -- does not
16 change and does not reduce the memory density.

17 Q And looking back, I think you also said
18 that you could see there was still space in these
19 figures in Paragraph 89 of your report to add
20 additional dummy channels?

21 Did I get that right?

22 A Yeah. For -- so -- yes. For example,

1 the -- what Nishikawa does is insert the dummy
2 channel, in fact the channel -- the memory
3 channel, into the -- what he called the separator
4 dielectric structure, which is labeled as 45 and
5 47.

6 So as you can see, that there are space
7 to the left of the row of -- of each row of the
8 memory cells that Nishikawa or a person of
9 ordinary skill in the art could see that you can
10 add dummy structure in -- in that space.

11 So, for example, if you look at the top
12 row of Nishikawa, between the left-most Element 55
13 and where it's turned the corner in Element 45,
14 there are spaces there. There are space that one
15 can add the dummy structure 66 there.

16 And similarly, to the far right of the
17 top row, which before the separator dielectric
18 structure 45 turn upward, one can also add dummy
19 structure there.

20 And furthermore, one can add dummy
21 channel even in the region of 410 or 420, or
22 further to the left or to the right in the

1 staircase region.

2 So there are ample opportunity for adding
3 dummy structure, which a person of ordinary skill
4 in the art would understand has a lot of benefits.
5 Not only provide additional mechanical support,
6 but also solve some of the fabrication issues that
7 I mention -- that I discuss in my declaration.

8 And one more thing is that you can see
9 that in Figure 17 in Nishikawa2 that even with the
10 separator dielectric structure 47 which provide
11 mechanical support, Nishikawa2 still add dummy
12 channel 66 for additional support.

13 So it is incorrect to say that there's
14 already a separator dielectric structure 47 that
15 provide mechanical support. It is not reasonable.
16 One might argue that why would you even add any
17 more dummy channel? Well, as you can see, that
18 Nishikawa2 has just done that.

19 Q Could we go back to Exhibit 1005, please.

20 A Yes.

21 Q All right. We've already talked about
22 this feature some. But you're familiar with the

1 term "through-array contact." Right?

2 A Through-array contact, you mean TAC,
3 T-A-C.

4 Q Yes. Perfect.

5 And what is a TAC?

6 A I believe I discuss --

7 MR. LANG: Objection to the form.

8 A I believe I discuss that -- sorry, I know
9 I have discussed that. I want to go to where I
10 discuss that. Okay?

11 So through-array contact is, you can
12 think of it as a vertical conductive vias. And
13 sometimes, in fact in Paragraph 57, sometimes it's
14 called the via structures or through-silicon vias,
15 TSV, or through-array contact. Those are vertical
16 conductive element that extent through the entire
17 memory stack.

18 And in Paragraph 57, the function of that
19 is to provide connections between different chips
20 in the stack. And I have provide some example in
21 my -- in the section of technology background.

22 Q And how is a TAC formed in a 3D NAND

1 device?

2 A Okay. Let me -- I'm searching for -- so
3 in Paragraph 109, I said that TAC can include a
4 vertical opening through a memory stack and is
5 filled with filling material.

6 So in general, the steps are, basically
7 fill a form the through stack openings, okay, and
8 across the alternating dielectric conductive
9 layers. And those opening are then, depending
10 on -- depending on what gate-replacement process
11 you are doing, but eventually you would deposit a
12 dielectric spacer, which means is a liner, along
13 the side wall of the through-stack opening that I
14 just discussed.

15 And that is used to isolate electrically
16 to the subsequent metal contact from the adjacent
17 wordlines, wordline layers.

18 And then, finally, you would deposit a
19 conductive layer, such as tungsten, into the
20 opening that is lined with dielectric spacers.

21 And then at the end you would do a
22 planarization to the top surface. And that's

1 basically the overview of the steps described in
2 Nishikawa2 and Nishikawa.

3 Q And I want to talk more about the
4 through-stack opening.

5 Is that a hole that's made by etching?

6 A Yes.

7 Q Is the process for etching a
8 through-stack opening with a circular
9 cross-section the same as etching one with an
10 angular cross-section?

11 MR. LANG: Objection to form.

12 A What do you mean, "angular"?

13 Q Noncircular, let's call it.

14 MR. LANG: Objection to form.

15 A What do you mean by "same"? Are you --
16 same recipe, same time, same layout? I'm not sure
17 what you mean by "same."

18 Q I guess I mean same across all of those
19 things.

20 I'm trying to understand, in your
21 opinion, what would have to change about an etch
22 process to etch a circular TAC, as opposed to a

1 noncircular one, if anything?

2 MR. LANG: Objection to form.

3 A Well, broadly speaking, etching a
4 through-stack opening in the 3D NAND, whether it's
5 a circular cross-section or noncircular
6 cross-section, such as a slot or elliptical, is
7 still used a similar reactive ion etch principles.

8 So in that respect is the same. Is the
9 same etch recipe, the same etch part -- part RIE
10 process.

11 In fact, in general, etching a circular
12 structure typically is more straightforward than
13 etching a noncircular structure because of the
14 distortions aspect in processing and maintaining
15 the design shape.

16 But overall, they're very similar.

17 Q What determines the shape of the
18 through-stack opening?

19 A What do you mean? It's a design.

20 Q Yeah, that was a bad question.

21 In -- during the manufacturing process,
22 how do you control the shape of the through-stack

1 opening?

2 A Well, it is the design of the layout, by
3 the layout person. I'm not sure what you mean by,
4 What determine the shape.

5 Of course, the etching got to be done
6 correctly to maintain the shape.

7 Q I'm trying to ask about masks for the
8 etching, essentially.

9 Is that what determines the shape?

10 A Yeah, that's basically -- basically it.
11 That whether you want a slot or a circular
12 structure is up to the designer.

13 Q Would -- strike that.

14 Do you have an understanding of whether
15 changing the shape of the TAC would change the
16 number of masks required for the etching?

17 A I --

18 MR. LANG: Objection to form.

19 Q I apologize, Doctor, I didn't catch that.

20 MR. LANG: And I had objected to form.

21 And I didn't -- couldn't hear what Dr. Lee said as
22 well. So if you could kindly reask the question?

1 MR. GRABOWSKI: Sure.

2 Q Do you have an understanding of whether
3 changing the shape of the TAC would change the
4 number of masks required for the etching?

5 MR. LANG: Objection to form.

6 A No, it shouldn't. To the first order, it
7 shouldn't. But, you know, your question is kind
8 of vague. You know, if there is other -- other
9 aspect to it. I don't know what you mean by -- by
10 your question, actually.

11 Q That's fine. We can move on.

12 Let's look briefly at your report. I'm
13 looking at Paragraph 108.

14 In it you talk about -- it's PDF Page 54.

15 A Hold on. Let me get there.

16 Okay.

17 Q And at the very bottom of the page you
18 talk about how Nishikawa discloses a through-array
19 contact, and then you identify two structures
20 there, the backside contact via structure and the
21 dielectric spacer.

22 Do you see that?

1 A You mean 76 and 74?

2 Q Yes.

3 A Yeah.

4 Q All right. What purpose -- I think --
5 strike that, because I think we may have discussed
6 this before.

7 Do you have an understanding of the
8 purpose that the dielectric spacer 74 serves?

9 A As I described earlier, that you need to
10 add a dielectric spacer, what some other -- some
11 people called it a liner -- along the side wall of
12 the -- of the two stack opening. And that serve
13 the purpose of electrically isolate the subsequent
14 metal contact, which is the through-array contact,
15 from the eventual adjacent wordline layer.

16 Without the spacer, dielectric spacer,
17 the through-array contact will be shorted to the
18 wordline, and therefore will make the chips
19 nonfunctioned.

20 In fact, followup to this point, that's
21 why that a lot of people added what is called the
22 level recess. The purpose of that is that the

1 liner, right, when you -- when you etch the hole,
2 you want to make sure that the side wall liner,
3 the dielectric spacer 74, is sufficient to avoid a
4 shorting between the through-array contact and the
5 wordline.

6 And the level recesses that discuss in
7 various prior art, such as Cui, C-U-I, and in my
8 declaration, I think later on in my declaration,
9 the purpose of that is simply to make the
10 isolation spacer wider in the layer between the
11 conductive layer. And so, therefore, basically
12 added a -- an insurance such that when you etch
13 the hole, you don't accidentally etch the
14 perimeters, the dielectric liner spacers between
15 the TAC, T-A-C, and the wordline.

16 And so to answer your question, the
17 dielectric spacer, the function of the dielectric
18 spacer 74, is to make sure that the TAC does not
19 short to the wordline.

20 And incidentally, the purpose of the
21 level recesses that discuss in Cui and in my
22 declaration is to give an extra assurance that the

1 shorting between the TAC and the wordline will not
2 happen.

3 Did I answer your question?

4 Q I think so. Let me just make sure I
5 understand one piece of vocabulary.

6 When you say "make sure the TAC doesn't
7 short," in Nishikawa's labeling system do you mean
8 backside contact structure via 76?

9 A Yes.

10 Q Okay.

11 A Yeah. In fact, in Paragraph 108 I put a
12 parentheses that's a TAC. So, yeah, the purpose
13 of dielectric spacer 74 is to make sure that the
14 TAC, the backside contact via structure 76, does
15 not short to the subsequent wordlines.

16 And with the additional precaution we
17 even make the -- the spacer to have different
18 length between the conductive layer and dielectric
19 layer just to have the additional assurance to
20 avoid accidental shorting between the TAC and the
21 wordline.

22 Q All right.

1 MR. GRABOWSKI: Could we please have one
2 of the unmarked exhibits, this is the Lee '806
3 deposition that I guess we'll call Lee Exhibit A.

4 (Lee Deposition Exhibit A marked for
5 identification and is attached to the transcript.)

6 A I'm sorry?

7 Q It will get pulled down for you.

8 MR. LANG: I'll, just to start, formulate
9 or state an objection to the use of this exhibit
10 as relating to what I understand to be a different
11 IPR proceeding relating to a different unrelated
12 patent.

13 Q Dr. Lee, do you recognize Lee Exhibit A
14 here?

15 A I -- it appears to be, if I read the
16 first page, it appears to be the two IPR. On Page
17 2, if you can scroll down, ending with 00791 and
18 00911.

19 Q And am I correct that this is a
20 transcript of a deposition that you gave in IPR
21 2024-00791?

22 A Yeah, it appears to be, but I have to

1 look through it to make sure that's the case.

2 Q Please take your time to review it. I
3 want to make sure you're comfortable with it.

4 A Yeah, according to the -- to this page it
5 appears to be the one that -- that I was deposed
6 in January 30th, 2025.

7 Q And like I said, take all the time you
8 need to look at it, if you want to confirm the
9 accuracy of it.

10 A No. Go ahead.

11 Q All right. The only question I have for
12 you is, you were under oath when you provided the
13 testimony you gave at this deposition. Correct?

14 A Of course.

15 Q All right.

16 MR. GRABOWSKI: Could we now have the Lee
17 254 deposition, which is going to be Lee B.

18 (Lee Deposition Exhibit B marked for
19 identification and is attached to the transcript.)

20 Q And, again, take all the time you need to
21 look at it. But does Lee Exhibit B appear to be
22 an accurate transcript of the dep that you gave in

1 IPR2025-34?

2 MR. LANG: I will again object to the use
3 of Exhibit -- did you mark this as an exhibit?
4 I'm sorry.

5 MR. GRABOWSKI: It's Lee Exhibit B, just
6 so we have it for purposes of the record. It's
7 not otherwise marked.

8 MR. LANG: Okay. I'll object to the Lee
9 Exhibit B or what looks to be like a deposition
10 transcript from a different -- a proceeding
11 relating to a different patent.

12 Q Dr. Lee, let me know if you'd like the
13 question again.

14 A Yeah, it appears to be a deposition
15 transcript that related to the '254 patent,
16 conducted in July 30th, 2024.

17 Q And does it appear to be an accurate
18 transcript of the deposition you gave specifically
19 in IPR2025-34?

20 A I don't know. I don't know whether it's
21 the E-transcript or a version of the transcript.
22 I have no idea.

1 Q You're welcome to take the time to
2 review.

3 A It would take me two hours, three hours
4 to make sure that it is the -- it is the depo that
5 I did. I simply -- you just show me this document
6 that I have not seen for many months, or weeks at
7 least, and ask me whether this is the accurate
8 document.

9 I don't know how to answer that.

10 Q Fair enough.

11 Do you recall being deposed on the '254
12 patent?

13 A Yes.

14 Q All right. And you were under oath when
15 you gave that deposition?

16 Is that right?

17 A Yes.

18 Q All right.

19 MR. GRABOWSKI: We've been going close to
20 another hour, and this is probably a good spot for
21 a break. Why don't we take five or ten minutes
22 and come back, if that works for you.

1 MR. LANG: Yeah, let's take ten.

2 (A recess was taken.)

3 MR. GRABOWSKI: Thank you, Dr. Lee. I
4 don't have any further questions.

5 I'll pass the witness.

6 THE WITNESS: Thank you.

7 MR. LANG: Yeah, I don't have any further
8 questions.

9 But I just did want to make clear for the
10 record our objections to whatever is going to be
11 marked as, you know, the Lee '806 deposition, the
12 Lee '254 deposition, for being, you know,
13 irrelevant to this proceeding and how are they
14 going to be used. We may have further objections.
15 But just wanted to ensure that our objections are
16 timely to those.

17 But with that, I have no further
18 questions.

19 (Off the record at 12:36 p.m. EDT.)

20

21

22

ACKNOWLEDGMENT OF DEPONENT

I, JACK C. LEE, Ph.D., do hereby
acknowledge that I have read and examined the
foregoing testimony, and the same is a true,
correct and complete transcription of the
testimony given by me, and any corrections appear
on the attached Errata sheet signed by me.

(DATE)

(SIGNATURE)

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C E R T I F I C A T E

I, Debra Ann Whitehead, E-Notary Public in and for
the Commonwealth of Virginia, do hereby certify:

That JACK C. LEE, Ph.D., the witness whose
deposition is hereinbefore set forth, was duly sworn
by me before the commencement of such deposition and
that such deposition was taken virtually and is a
true record of the testimony given by such witness.

I further certify that the adverse party,
MICRON TECHNOLOGY, INC., was represented by counsel
at the deposition.

I further certify that the deposition of
JACK C. LEE, Ph.D., occurred virtually, on Thursday,
October 23, 2025 from 10:08 a.m. to 12:36 p.m. EDT.

1 I further certify that I am not related to
2 any of the parties to this action by blood or
3 marriage, I am not employed by or an attorney to any
4 of the parties to this action, and that I am in no
5 way interested, financially or otherwise, in the
6 outcome of this matter.

7

8 IN WITNESS WHEREOF, I have hereunto set my
9 hand this 28th day of October, 2025.

10

11 My commission expires:

12 October 31, 2027

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E-NOTARY PUBLIC IN AND FOR THE

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COMMONWEALTH OF VIRGINIA

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A			
ability	45:20	affect	23:8, 23:9,
8:19	actually	40:12, 40:17	23:14, 23:22,
able	27:15, 36:13,	affected	27:20, 27:21,
13:7	37:14, 57:10	22:21	28:15, 28:20,
about	add	after	29:10, 30:5,
7:3, 9:5,	43:17, 44:6,	35:6	30:8, 34:10,
10:12, 11:12,	44:10, 44:15,	again	39:3, 39:21,
11:22, 12:16,	45:5, 45:11,	16:4, 22:17,	40:18, 41:4,
16:12, 19:18,	47:2, 47:4,	35:11, 35:15,	43:10, 45:3,
25:1, 27:14,	47:5, 47:16,	37:5, 62:20,	49:17, 50:18,
27:18, 34:2,	49:19, 50:10,	63:2, 63:13	51:6
36:17, 40:3,	50:15, 50:18,	agree	alternating
41:7, 51:21,	50:20, 51:11,	20:1, 22:14,	53:8
54:3, 54:21,	51:16, 58:10	22:18, 24:11,	always
56:7, 57:14,	added	43:20, 49:3	37:22
57:18	44:19, 45:13,	ahead	ample
access	48:22, 49:10,	62:10	51:2
13:7	58:21, 59:12	ai	analog
accidental	adding	38:13	35:18, 38:11
60:20	43:13, 44:13,	alex	angular
accidentally	44:14, 45:8,	3:10, 6:6	54:10, 54:12
59:13	47:9, 47:13,	all	ann
according	48:16, 48:21,	6:16, 6:22,	2:5, 67:2
38:4, 39:11,	49:8, 49:13,	7:5, 7:6, 7:10,	another
62:4	51:2	7:21, 8:5, 8:15,	26:20, 43:11,
accounting	addition	9:4, 10:1, 10:6,	47:22, 64:20
11:15	18:2, 18:3,	10:8, 11:3,	answer
accumulating	24:13, 40:18,	13:7, 13:9,	8:7, 8:8, 8:13,
27:1	40:19, 41:3	16:12, 17:12,	20:22, 29:17,
accuracy	additional	17:15, 17:20,	31:19, 34:20,
62:9	49:20, 51:5,	18:17, 19:13,	38:20, 59:16,
accurate	51:12, 60:16,	21:18, 21:20,	60:3, 64:9
8:20, 9:1,	60:19	30:20, 31:16,	answering
62:22, 63:17,	address	38:13, 41:3,	45:9
64:7	6:11, 6:18,	41:6, 46:18,	answers
acknowledge	6:20, 31:17,	51:21, 54:18,	7:9, 7:13
66:3	32:17, 32:19	58:4, 60:22,	anticipated
acknowledgment	addressed	62:7, 62:11,	19:12
66:1	33:6	62:15, 62:20,	anticipation
across	addresses	64:14, 64:18	18:10, 18:19,
53:8, 54:18	31:17	along	18:22
acting	adjacent	21:10, 53:12,	any
9:22	53:16, 58:15	58:11	7:21, 8:13,
action	advanced	already	8:18, 8:22,
68:2, 68:4	21:16	51:14, 51:21	9:10, 9:12,
active	adverse	also	9:16, 9:19,
46:18	67:11	4:2, 10:9,	10:9, 11:8,
		18:4, 21:15,	14:8, 14:11,

16:14, 19:11, 28:9, 35:17, 36:7, 36:11, 51:16, 65:4, 65:7, 66:6, 68:2, 68:3 anyone 9:7, 11:10, 11:19 anything 55:1 anywhere 32:22 apologize 19:3, 56:19 appeal 1:2 appear 62:21, 63:17, 66:6 appears 61:15, 61:16, 61:22, 62:5, 63:14 applications 9:20 appreciate 43:16 architecture 33:11, 33:12, 48:8 area 20:7, 22:8, 23:2, 39:21, 40:10 argue 51:16 argument 18:18, 19:15 around 12:18, 44:20 array 23:12, 33:11, 33:17, 44:7, 44:16, 44:21, 45:10, 45:12, 45:14, 47:10, 47:16, 47:18,	49:14 art 16:8, 17:18, 17:22, 18:4, 18:5, 18:22, 31:10, 31:17, 31:22, 34:12, 34:17, 35:20, 47:4, 48:20, 50:9, 51:4, 59:7 artisan 31:5 asking 32:16 aspect 25:10, 29:7, 29:21, 30:19, 30:21, 31:1, 31:18, 32:2, 34:2, 35:8, 55:14, 57:9 associated 25:9 assume 8:1 assurance 59:22, 60:19 attached 5:6, 5:14, 13:2, 42:10, 61:5, 62:19, 66:7 attorney 68:3 austin 6:20, 6:21, 40:9, 40:19 avenue 3:12 avoid 59:3, 60:20 aware 14:9, 32:21 B bachelor 21:9 back 28:13, 49:17,	51:19, 64:22 background 52:21 backside 57:20, 60:8, 60:14 bad 24:9, 41:8, 55:20 ballpark 15:15 based 17:13, 19:14, 44:5 basically 28:11, 28:13, 47:15, 53:6, 54:1, 56:10, 59:11 became 25:5 because 9:4, 12:5, 15:5, 18:16, 25:12, 38:19, 55:13, 58:5 become 26:9, 27:6, 29:9, 31:2 becomes 25:15, 29:2 been 6:3, 6:22, 12:17, 14:10, 14:11, 31:5, 38:3, 39:17, 40:6, 40:8, 41:6, 43:3, 44:10, 64:19 before 1:2, 2:5, 7:1, 8:14, 27:1, 31:20, 49:11, 50:17, 58:6, 67:7 behalf 3:2, 3:9, 6:7, 6:15	behavior 35:3 being 64:11, 65:12 believe 10:2, 14:3, 18:15, 18:21, 22:1, 22:2, 25:22, 41:18, 49:2, 52:6, 52:8 benefits 49:1, 51:4 better 22:12, 35:13 between 29:2, 48:11, 49:1, 50:12, 52:19, 59:4, 59:10, 59:14, 60:1, 60:18, 60:20 bit 19:18, 23:1, 23:3, 23:4 bits 22:10, 23:2, 23:5, 33:13 black 48:10 blake 3:17 block 26:18 blocks 33:14 blood 68:2 board 1:2 bobby 6:8 bombardment 27:5 both 46:12 bottom 26:10, 26:14, 27:2, 27:5,
---	--	---	--

27:20, 33:19, 49:10, 57:17 bounce 28:21 bouncing 28:13 break 8:11, 8:14, 41:8, 64:21 breaks 8:10 briefly 57:12 bring 12:20 broadly 55:3 build 37:15, 38:5 building 33:9 builds 37:2, 37:8 business 6:11, 6:17 byproduct 26:15, 27:1 byproducts 26:16	capacity 42:1 careful 35:22 case 1:5, 12:5, 12:6, 12:8, 12:12, 15:7, 42:15, 47:18, 62:1 cases 47:18 catch 56:19 cause 25:13, 26:5, 29:10, 45:16 causes 25:20, 27:16 cell 23:3, 23:4, 23:5, 33:9, 33:14 cells 23:3, 23:6, 50:8 certain 35:8, 35:9, 35:13 certainly 29:15 certify 67:3, 67:11, 67:15, 68:1 cf4 28:1 challenged 19:2 change 40:16, 47:19, 48:16, 48:21, 49:15, 49:16, 54:21, 56:15, 57:3 changes 40:17 changing 40:6, 40:11,	40:12, 40:15, 56:15, 57:3 channel 26:8, 33:13, 41:17, 41:21, 42:4, 42:6, 43:2, 43:5, 43:13, 44:2, 44:11, 44:13, 44:14, 44:19, 45:6, 45:8, 45:11, 45:13, 45:21, 46:4, 46:6, 46:21, 46:22, 47:3, 47:6, 47:9, 47:13, 47:16, 47:22, 48:16, 48:21, 49:4, 49:8, 49:13, 50:2, 50:3, 50:21, 51:12, 51:17 channels 41:14, 41:22, 42:18, 43:17, 43:21, 44:6, 44:16, 46:13, 46:17, 46:18, 47:7, 49:20 charge 28:9, 33:10 charging 28:9, 28:10, 28:14 chat 13:3, 13:4 check 39:5 chf3 28:1, 28:2 chicago 3:14 chip 23:1, 34:11, 34:15, 35:17, 35:18, 36:13, 39:14, 39:19,	40:7 chips 35:17, 36:7, 36:10, 37:2, 37:8, 37:15, 38:13, 39:21, 52:19, 58:18 circuit 23:9, 23:10, 23:22, 33:16 circular 23:18, 33:12, 54:8, 54:22, 55:5, 55:11, 56:11 claim 19:2 claims 19:11 clarify 7:22 cleaning 34:5 clear 7:19, 65:9 clearly 34:18, 35:22 close 64:19 cmos 35:17, 38:10, 38:11, 39:21 collaboration 14:14 collide 26:22, 28:22, 29:3 collisions 29:2 column 46:2, 46:5 combinations 15:20, 18:1 come 29:13, 64:22 comfortable 62:3 coming 37:11
C			
c-u-i 59:7 california 3:6 call 29:1, 43:11, 43:13, 43:14, 46:4, 54:13, 61:3 called 25:13, 28:20, 42:5, 50:3, 52:14, 58:11, 58:21 calling 8:12 cannot 8:22			

commencement 67:7 commission 68:11 commonwealth 2:6, 67:3, 68:17 communications 10:15 company 1:8 compare 47:20 compared 26:10 comparing 47:11 comparison 48:11 complete 8:20, 9:1, 13:18, 13:22, 66:5 complex 20:3, 21:2 complicated 20:11, 20:14, 34:13 computer 9:15, 9:20 computer-aided 35:1 computers 9:17 concept 16:18, 17:17 concerning 14:1 concerns 15:19 conclude 48:15, 48:20 concluded 47:21 conclusion 48:18 conducted 1:14, 2:1,	63:16 conductive 52:12, 52:16, 53:8, 53:19, 59:11, 60:18 conference 40:22 confirm 62:8 connect 9:16 connection 13:14 connections 52:19 considerably 47:3 consideration 24:13 considerations 33:22 considering 31:5, 44:11 constraints 24:12 consulting 39:20, 40:1, 41:4 contact 28:7, 52:1, 52:2, 52:11, 52:15, 53:16, 57:19, 57:20, 58:14, 58:17, 59:4, 60:8, 60:14 contacted 11:22, 12:16 contains 13:17, 13:22 context 16:22, 18:10, 21:21 control 55:22 corner 50:13 correct 13:19, 18:6,	42:15, 45:19, 46:10, 46:11, 48:1, 61:19, 62:13, 66:5 corrections 66:6 correctly 36:20, 37:20, 38:4, 38:6, 39:2, 39:11, 56:6 correspondingly 30:6 cost 22:12, 33:19 could 12:20, 17:4, 24:15, 42:7, 47:4, 49:18, 50:9, 51:19, 56:22, 61:1, 62:16 couldn't 56:21 counsel 6:4, 10:12, 10:13, 10:15, 10:17, 10:19, 10:21, 14:14, 14:17, 15:4, 16:4, 16:10, 67:12 count 16:8 counting 48:9 couple 8:17, 11:1 course 56:5, 62:14 court 7:14 cove 6:20 create 28:11, 28:20 creates 28:2	cross-section 54:9, 54:10, 55:5, 55:6 cross-sectional 35:12 cui 59:7, 59:21 curious 27:15 D data 22:7, 22:8 date 31:6, 31:20, 66:10 day 68:9 dc 3:20 deal 20:16 debra 1:22, 2:5, 67:2 declaration 10:6, 10:7, 12:22, 13:14, 13:17, 13:22, 14:4, 14:9, 14:13, 14:15, 14:20, 14:22, 15:1, 15:19, 16:2, 16:15, 16:17, 17:3, 19:11, 21:7, 21:19, 22:2, 22:3, 26:1, 32:17, 32:18, 33:6, 41:19, 46:8, 48:3, 48:14, 49:1, 51:7, 59:8, 59:22 declarations 10:5, 15:13 deep 25:11 deeper 25:15, 28:4,
---	---	--	--

29:11, 30:6 definition 22:5 deflect 28:10 degree 21:9, 21:16 density 21:21, 22:6, 22:12, 22:14, 22:18, 22:21, 23:6, 23:13, 23:14, 24:3, 24:6, 24:12, 25:5, 25:19, 45:8, 45:17, 47:14, 47:19, 48:17, 48:22, 49:11, 49:16 dep 62:22 depend 23:15, 23:21 dependent 24:6 depending 21:15, 23:8, 23:20, 45:10, 53:9, 53:10 depends 20:4, 23:10, 23:19, 23:22, 24:3, 30:3 depo 64:4 deponent 66:1 deposed 7:1, 62:5, 64:11 deposit 28:3, 35:8, 53:11, 53:18 deposition 1:13, 2:1, 5:7, 5:8, 5:10, 5:15, 9:5, 10:4, 11:4, 11:20, 61:3,	61:4, 61:20, 62:13, 62:17, 62:18, 63:9, 63:14, 63:18, 64:15, 65:11, 65:12, 67:6, 67:7, 67:8, 67:13, 67:15 depositions 9:22, 27:21 depth 30:5, 30:8, 30:13, 30:18, 30:22 describe 21:7, 25:22, 26:4, 27:10, 31:9, 41:18, 43:9, 44:21, 46:5 described 17:3, 21:18, 54:1, 58:9 design 19:18, 24:1, 32:12, 33:21, 35:2, 36:14, 36:22, 37:6, 37:16, 38:3, 38:11, 38:12, 39:10, 40:7, 40:15, 55:15, 55:19, 56:2 designed 23:9, 45:11 designer 56:12 designing 20:2, 21:13, 31:6, 32:7, 32:10, 32:11, 32:13, 33:2, 34:14, 35:16, 36:6, 36:9 detail 27:14, 38:16 determine 56:4	determined 23:9 determines 55:17, 56:9 develop 34:9 development 37:22 device 32:8, 32:13, 32:14, 34:4, 35:3, 38:11, 53:1 devices 9:17, 20:3, 21:12, 31:7, 33:3, 38:11, 40:13 diagram 46:16, 46:20 diameter 28:4, 30:4, 30:7, 30:14, 31:1 dielectric 43:6, 43:14, 46:2, 50:4, 50:17, 51:10, 51:14, 53:8, 53:12, 53:20, 57:21, 58:8, 58:10, 58:16, 59:3, 59:14, 59:17, 60:13, 60:18 different 36:18, 52:19, 60:17, 61:10, 61:11, 63:10, 63:11 difficulty 26:16 diffusion 29:10 direction 49:5 directional 29:8	directionality 29:4, 29:9 directly 26:4, 26:5 discipline 21:10 disclose 10:15, 10:18, 19:1, 42:17, 44:2 discloses 57:18 discuss 10:12, 42:20, 43:1, 49:1, 51:7, 52:6, 52:8, 52:10, 59:6, 59:21 discussed 52:9, 53:14, 58:5 discusses 43:2 discussions 15:3 distortions 55:14 doctor 38:18, 56:19 document 10:10, 14:16, 64:5, 64:8 documents 9:12, 10:7 doing 21:3, 33:10, 34:19, 53:11 done 36:11, 37:13, 51:18, 56:5 dots 48:10, 48:11 down 7:14, 25:15, 28:12, 61:7, 61:17 dr 6:6, 6:15,
--	--	---	--

6:16, 12:21, 41:13, 48:1, 56:21, 61:13, 63:12, 65:3 dram 34:11, 38:12 due 28:13, 29:8 duly 6:3, 67:6 dummy 41:14, 41:17, 41:20, 41:22, 42:4, 42:6, 42:18, 43:5, 43:13, 43:17, 43:21, 44:2, 44:6, 44:11, 44:13, 44:14, 44:16, 44:19, 45:5, 45:8, 45:11, 45:13, 45:21, 46:4, 46:17, 46:22, 47:3, 47:5, 47:9, 47:13, 47:16, 48:16, 48:21, 49:4, 49:8, 49:13, 49:20, 50:1, 50:10, 50:15, 50:18, 50:20, 51:3, 51:11, 51:17 dunteman 3:17, 6:8 during 55:21 E e-notary 2:6, 67:2, 68:16 e-transcript 63:21 each 11:15, 11:17, 28:22, 34:3,	46:21, 50:7 earlier 58:9 early 12:13 edge 44:20, 45:14, 47:6, 47:16, 49:14 edt 1:16, 65:19, 67:17 effect 27:5, 27:10, 27:14, 27:19, 28:9, 28:11, 28:14, 28:15, 28:21, 29:13, 31:2, 45:16 effective 23:13 effects 27:17, 29:19, 30:15 either 19:4, 40:15, 43:5, 47:18 electrical 21:9, 35:3, 35:20 electrically 53:15, 58:13 electron 36:3, 36:4 element 45:20, 45:21, 46:5, 49:9, 50:12, 50:13, 52:16 eleventh 3:19 elliptical 55:6 else 9:7, 27:16, 28:5 embodiment 44:13	employed 68:3 end 53:21 ending 61:17 endurance 33:18, 35:5 energy 26:21, 27:4, 27:19 engineering 20:7, 21:9, 35:20 engineers 40:2 enough 64:10 ensure 38:8, 65:15 ensures 39:3 entire 27:9, 52:16 equal 30:13 equivalent 21:12 errata 66:7 escaping 26:17 especially 44:11 esquire 3:3, 3:10, 3:17 essentially 34:9, 56:8 establish 33:8 etch 25:10, 26:7, 28:5, 28:6, 28:18, 29:6, 29:8, 34:4, 35:8, 35:13, 54:21, 54:22, 55:7, 55:9,	59:1, 59:12, 59:13 etches 35:14, 36:18 etching 25:12, 26:11, 26:16, 27:6, 27:22, 28:7, 29:7, 29:17, 30:1, 30:21, 31:18, 32:2, 54:5, 54:7, 54:9, 55:3, 55:11, 55:13, 56:5, 56:8, 56:16, 57:4 even 27:14, 28:12, 31:15, 47:17, 50:21, 51:9, 51:16, 60:17 eventual 58:15 eventually 37:9, 53:11 ever 6:22, 18:9, 39:17, 40:6 every 8:11, 19:1 everyone 8:18 everything 15:2 exact 11:16 exactly 12:9, 12:11, 12:19, 15:5, 15:17, 39:22 examination 5:2, 6:4 examined 66:3 example 21:16, 22:22, 24:14, 28:1, 28:6, 35:7,
---	---	---	--

35:21, 36:21, 45:4, 47:1, 49:22, 50:11, 52:20 examples 44:14, 45:1 exhibit 5:7, 5:8, 5:10, 5:15, 5:16, 5:17, 12:21, 13:1, 13:13, 31:11, 31:13, 31:14, 31:16, 42:8, 42:9, 42:11, 43:12, 44:1, 45:1, 45:22, 46:2, 46:8, 51:19, 61:3, 61:4, 61:9, 61:13, 62:18, 62:21, 63:3, 63:5, 63:9 exhibits 5:5, 5:13, 10:8, 16:8, 61:2 expectation 43:4 expected 35:4 experience 20:12, 21:11, 21:16, 21:17, 30:14 experiment 35:7, 35:10 experimental 34:6, 34:20 expert 10:1, 19:17 expires 68:11 explicitly 44:2 expressively 19:4 expressly 19:4, 44:2 extent 52:16	extra 59:22 F fabrication 22:15, 22:19, 23:20, 24:11, 51:6 fact 10:16, 48:18, 50:2, 52:13, 55:11, 58:20, 60:11 factor 25:5, 25:18 factors 22:22, 27:8 fair 8:3, 19:20, 20:15, 64:10 familiar 17:17, 19:21, 21:20, 32:6, 41:13, 51:22 familiarity 33:2 far 10:16, 50:16 faster 28:18 feature 51:22 feel 8:12 few 9:5, 11:2, 11:15, 15:6, 15:14, 15:16, 29:14, 31:22 field 35:20, 43:6 figure 45:4, 47:1, 47:11, 51:9 figures 45:19, 46:9, 47:21, 48:2, 48:13, 49:19	fill 53:7 filled 53:5 filling 53:5 final 37:12, 38:8, 39:4, 39:14, 40:17 finally 53:18 financially 68:5 find 26:1, 31:11, 35:12 fine 57:11 finish 37:1, 37:7 firm 6:8, 16:11 first 11:22, 12:16, 33:7, 39:7, 57:6, 61:16 five 64:21 flash 20:13, 21:11, 33:11 floating 33:10 flow 33:21, 40:16 folks 16:10 follows 6:3 followup 58:20 foregoing 66:4 form 12:2, 13:20, 20:18, 22:16, 23:17, 25:21,	31:8, 32:9, 32:15, 33:4, 36:15, 37:4, 37:18, 42:3, 42:19, 42:22, 43:22, 44:9, 44:18, 48:4, 52:7, 53:7, 54:11, 54:14, 55:2, 56:18, 56:20, 57:5 formed 52:22 forming 14:22, 25:1, 42:14 formulate 61:8 forth 22:13, 28:13, 67:6 four 17:9, 17:12, 17:15, 17:20, 18:17, 19:13, 46:12, 46:17 frame 12:19 free 8:12, 29:2 frequently 29:3 front 9:10, 9:12, 9:17 function 52:18, 59:17 functional 39:15 functions 42:5 further 50:22, 65:4, 65:7, 65:14, 65:17, 67:11, 67:15, 68:1 furthermore 43:9, 50:20
--	--	---	--

G g-o-d-a 31:14 gas 29:10 gate 33:10, 34:3 gate-replacement 53:10 gave 22:5, 61:20, 62:13, 62:22, 63:18, 64:15 general 12:5, 20:1, 22:7, 22:9, 26:6, 28:5, 28:16, 33:7, 34:22, 44:5, 44:19, 45:13, 53:6, 55:11 generally 12:8 geometry 23:18, 25:10 gigabits 22:9 give 7:5, 7:9, 8:19, 9:1, 59:22 given 22:8, 66:6, 67:9 go 8:14, 17:4, 24:15, 25:15, 26:21, 27:14, 28:4, 38:13, 51:19, 52:9, 62:10 goda 31:14 going 7:8, 26:18, 28:12, 30:14, 31:11, 36:13, 36:22, 37:6,	41:7, 62:17, 64:19, 65:10, 65:14 good 41:10, 64:20 grabowski 3:10, 5:3, 6:5, 6:6, 12:20, 17:4, 41:6, 41:12, 42:7, 57:1, 61:1, 62:16, 63:5, 64:19, 65:3 graduated 40:20 ground 18:2, 18:5, 18:7, 19:13, 31:9, 32:1 grounds 17:9, 17:13, 17:15, 17:20, 18:17 guess 12:7, 20:21, 27:17, 54:18, 61:3 H hand 68:9 happen 60:2 happy 7:22 hard 15:11 harder 26:13, 27:20 head 7:13 hear 27:15, 56:21 heard 18:9 height 30:4 hello 18:20	help 7:12 helpful 32:4 here 6:7, 14:8, 17:6, 29:8, 42:17, 45:19, 61:14 hereby 66:2, 67:3 hereinbefore 67:6 hereunto 68:8 herrington 3:4, 6:15 high 25:10, 29:7, 30:21, 31:18, 32:2 high-aspect 25:2, 25:4, 25:11, 26:7 higher 22:11, 28:19, 29:1, 29:21, 30:19, 30:21, 31:1 hold 18:15, 26:1, 26:3, 26:7, 57:15 hole 25:11, 25:13, 25:14, 26:8, 26:9, 26:22, 30:8, 30:18, 30:21, 31:18, 34:3, 54:5, 59:1, 59:13 holes 25:2, 25:4, 30:13, 30:17 hour 8:11, 41:7, 64:20 hours 11:15, 15:12,	15:14, 15:18, 64:3 I idea 63:22 ideas 35:10 identification 61:5, 62:19 identify 57:19 illinois 3:14 illustration 47:9 impact 8:19 implementations 40:4 implemented 38:4, 39:2, 39:11 imply 24:5 important 30:9, 49:12 improve 28:18 inactive 41:21, 42:6 inappropriate 47:20 inc 1:4, 67:12 incidentally 59:20 include 43:5, 53:3 included 14:4 including 16:10, 31:10, 31:12, 45:1 inclusion 48:3 incoming 28:11
---	--	---	--

incorrect 51:13 increase 23:5, 23:13 industry 34:16, 41:5 inherently 19:5 insert 50:1 inside 39:2 instance 36:18 instead 28:12 instruct 8:7, 10:14 insulating 28:7, 28:8 insulator 28:10 insurance 59:12 integrate 33:15 interested 68:5 invalidity 17:10 inventor 44:12 involved 15:20, 39:17, 39:22, 40:6 ion 26:12, 26:18, 27:3, 27:20, 28:11, 28:17, 29:6, 55:7 ions 26:21, 28:21 ipr 1:5, 12:4, 12:6, 12:16, 13:15, 14:15, 15:6, 15:10, 16:6, 17:2,	18:16, 61:11, 61:16, 61:20, 63:1, 63:19 iprs 12:7, 16:5 irrelevant 65:13 isolate 53:15, 58:13 isolation 59:10 issue 43:11 issues 15:7, 15:8, 31:4, 31:18, 34:14, 51:6 itself 24:1, 32:13, 43:21 J jack 1:13, 2:1, 5:2, 5:9, 5:11, 6:2, 6:19, 66:2, 67:5, 67:16 january 62:6 jason 3:3, 6:14, 16:10, 37:19, 42:21 job 1:20 journal 40:21 july 63:16 K k-a-i 45:2 kai 45:1 kind 26:17, 33:8, 57:7	kindly 56:22 know 10:16, 14:6, 15:6, 15:9, 15:13, 20:8, 20:10, 20:19, 23:15, 26:3, 27:9, 27:19, 28:8, 38:12, 52:8, 57:7, 57:8, 57:9, 63:12, 63:20, 64:9, 65:11, 65:12 knowledge 17:21, 18:3, 18:6, 18:8, 20:16, 44:5 known 31:4 L l-u 31:10 labeled 50:4 labeling 60:7 lang 3:3, 6:13, 6:14, 10:13, 11:6, 11:10, 11:19, 12:2, 13:20, 14:2, 20:18, 21:4, 22:16, 22:20, 25:21, 31:8, 32:9, 32:15, 33:4, 36:15, 37:4, 37:18, 42:3, 42:19, 42:22, 43:22, 44:9, 44:18, 48:4, 52:7, 54:11, 54:14, 55:2, 56:18, 56:20, 57:5,	61:8, 63:2, 63:8, 65:1, 65:7 larger 23:4, 30:2, 30:4 last 11:1, 12:10, 12:13, 24:20, 38:21 later 59:8 lateral 49:4 latham 3:11, 3:18, 6:8 law 6:8, 14:18, 16:18, 16:22, 17:2, 18:10, 19:16 lawyer 8:5, 14:16, 17:1, 19:6, 19:7, 20:8 lawyers 11:8 layer 23:1, 53:19, 58:15, 59:10, 59:11, 60:18, 60:19 layers 22:22, 53:9, 53:17 layout 23:21, 24:1, 54:16, 56:2, 56:3 lead 29:4 least 11:2, 15:18, 64:7 lee 1:13, 2:1, 5:2, 5:7, 5:9, 5:11, 6:2, 6:6, 6:15, 6:16, 6:19,
---	--	---	---

41:13, 48:1, 56:21, 61:2, 61:3, 61:4, 61:13, 62:16, 62:17, 62:18, 62:21, 63:5, 63:8, 63:12, 65:3, 65:11, 65:12, 66:2, 67:5, 67:16 lee's 12:21 left 46:16, 50:7, 50:22 left-most 50:12 legal 14:16 length 60:18 less 27:4, 29:10 let's 12:8, 20:7, 54:13, 57:12, 65:1 level 21:12, 58:22, 59:6, 59:21 limit 25:17, 25:18 limitation 19:1 limited 22:15, 22:19, 29:10 limiting 25:5, 25:18 line 33:19, 49:10 lined 53:20 liner 53:12, 58:11, 59:1, 59:2, 59:14 list 24:14, 31:9	listed 10:7, 10:8, 43:7 little 19:18 llp 3:4, 3:11, 3:18 logic 35:17, 38:11 long 10:17, 11:12, 14:19, 21:2 look 22:1, 27:8, 40:11, 41:1, 46:1, 47:13, 47:15, 50:11, 57:12, 62:1, 62:8, 62:21 looked 40:14 looking 45:18, 46:7, 49:17, 57:13 looks 63:9 loop 6:20 lose 16:8 loses 26:21 loss 27:19 lost 16:8 lot 29:16, 33:22, 35:1, 44:22, 51:4, 58:21 lower 28:3 lu 31:10, 31:12	m-i-c-h-e-l-o-n-i 31:16 made 54:5 mainly 10:10 maintain 56:6 maintaining 55:14 make 8:6, 24:10, 30:11, 38:18, 39:10, 39:14, 58:18, 59:2, 59:9, 59:18, 60:4, 60:6, 60:13, 60:17, 62:1, 62:3, 64:4, 65:9 makes 30:12, 38:3, 39:1 making 32:13 manufacturing 19:19, 20:2, 23:8, 24:4, 24:6, 32:7, 32:10, 32:11, 33:3, 34:15, 35:16, 36:10, 36:12, 37:1, 37:7, 37:12, 37:14, 55:21 many 7:3, 10:21, 12:5, 12:6, 15:6, 15:7, 15:11, 16:5, 16:7, 16:9, 22:7, 22:22, 23:15, 27:7, 27:8, 33:12, 33:13, 33:14, 40:2, 40:9, 41:1, 64:6 mark 63:3	marked 5:5, 5:13, 13:1, 42:9, 61:4, 62:18, 63:7, 65:11 marriage 68:3 marsh 3:5 masamori 31:14 masks 56:7, 56:16, 57:4 match 37:16 matches 36:14 material 28:7, 28:8, 35:9, 40:12, 43:6, 53:5 matter 20:2, 68:6 maybe 7:4, 12:10 mean 12:3, 12:4, 14:6, 14:21, 15:16, 20:19, 24:5, 25:8, 29:1, 34:21, 45:9, 49:6, 52:2, 54:12, 54:15, 54:17, 54:18, 55:19, 56:3, 57:9, 58:1, 60:7 meaning 21:13 means 16:22, 18:13, 18:22, 26:9, 30:18, 31:1, 38:2, 38:7, 38:22, 53:12 meanwhile 26:15
---	---	---	--

measure 22:9 mechanical 51:5, 51:11, 51:15 medications 8:18 meet 38:8 meeting 11:15 meetings 10:21, 11:3, 11:6, 11:13, 11:18 meets 39:4, 39:14 memory 1:7, 20:2, 20:13, 21:12, 21:21, 21:22, 22:6, 22:11, 22:14, 22:18, 22:21, 23:14, 24:3, 24:5, 24:12, 25:5, 25:11, 25:19, 26:7, 34:11, 35:18, 36:7, 36:10, 37:2, 37:8, 37:15, 38:11, 39:19, 40:7, 40:10, 40:13, 41:2, 41:21, 41:22, 42:5, 42:6, 43:2, 43:7, 44:7, 44:16, 44:20, 45:10, 45:11, 45:14, 45:16, 45:20, 46:5, 46:6, 47:6, 47:14, 47:19, 47:22, 48:7, 48:16, 48:21, 49:11, 49:14, 49:16, 50:2, 50:8,	52:17, 53:4 menlo 3:6 mention 32:1, 51:7 mentioned 18:17, 19:14, 24:14, 29:17, 36:1, 40:18, 48:6, 49:11 met 10:17, 10:19, 11:2 metal 53:16, 58:14 method 32:7, 32:11, 34:15, 35:16, 36:10, 36:12 methods 33:3 metric 40:13 miceloni 31:16 micron 1:4, 6:15, 67:12 microprocessor 34:11 microscopy 36:4, 36:5 might 14:10, 14:11, 19:5, 20:10, 21:16, 31:22, 41:7, 51:16 millimeter 22:10 mind 6:10, 6:17, 29:13, 32:20 minimum 49:3 minutes 41:7, 64:21 mischaracterizes 21:4	missed 29:14, 31:22 mistake 14:12 mistakes 14:9 misunderstood 24:8 mixed 38:12 months 64:6 more 15:10, 16:12, 18:4, 23:1, 27:14, 28:17, 29:3, 29:6, 29:7, 29:19, 29:22, 30:14, 31:2, 40:20, 40:21, 47:2, 47:5, 51:8, 51:17, 54:3, 55:12 motivated 43:4, 44:10 mouth 21:1 move 57:11 much 22:8, 23:15, 23:16, 33:19 multi-deck 32:3 multiple 16:6, 27:10 must 12:17, 15:13 N name 6:6, 6:11, 6:13, 6:17, 6:19 nand 19:19, 20:2, 20:13, 21:11, 21:21, 22:6,	24:21, 26:8, 31:7, 32:3, 32:7, 33:8, 34:10, 35:18, 36:7, 36:10, 37:2, 37:8, 37:15, 38:10, 39:18, 39:21, 40:7, 41:2, 49:12, 52:22, 55:4 narrower 25:16, 26:10, 30:18 nature 25:12 near 27:1 need 8:11, 19:8, 43:12, 44:12, 58:9, 62:8, 62:20 neutral 26:16, 27:1 new 32:7 next 45:6 nishikawa 18:7, 42:13, 42:17, 43:1, 43:10, 43:17, 43:20, 44:1, 44:11, 44:17, 45:5, 45:19, 46:3, 46:9, 46:16, 47:4, 47:11, 48:8, 48:12, 48:15, 48:19, 50:1, 50:8, 50:12, 54:2, 57:18 nishikawa's 43:7, 44:7, 60:7 nishikawa2 43:11, 43:12,
--	--	--	---

Transcript of Jack C. Lee, Ph.D.
Conducted on October 23, 2025

80

44:6, 45:4, 45:20, 46:1, 46:9, 46:20, 47:5, 47:12, 48:7, 48:12, 48:15, 48:19, 51:9, 51:11, 51:18, 54:2 nodding 7:13 noncircular 54:13, 55:1, 55:5, 55:13 nonfunctioned 58:19 nonlawyers 16:14 nonvolatile 40:10, 41:2 north 3:12 notes 9:10 notice 2:5 november 12:18 number 13:18, 14:1, 15:14, 15:19, 22:9, 22:22, 23:2, 23:5, 31:10, 31:12, 43:7, 45:5, 47:21, 48:10, 56:16, 57:4 nw 3:19 O oath 62:12, 64:14 object 63:2, 63:8 objected 56:20 objection 12:2, 13:20,	20:18, 21:4, 22:16, 22:20, 25:21, 31:8, 32:9, 32:15, 33:4, 36:15, 37:4, 37:18, 42:3, 42:19, 42:22, 43:22, 44:9, 44:18, 48:4, 52:7, 54:11, 54:14, 55:2, 56:18, 57:5, 61:9 objections 8:6, 14:2, 65:10, 65:14, 65:15 obviously 10:11, 14:15, 22:11, 25:16, 29:21, 49:8 obviousness 15:20, 16:18, 16:22, 17:13, 17:20, 18:18, 19:14 occurred 67:16 october 1:15, 12:18, 67:17, 68:9, 68:12 offer 18:19 offering 19:10 office 1:1 oh 19:3, 25:8, 41:18 okay 7:15, 13:6, 18:20, 20:9, 27:18, 32:4, 39:8, 41:20, 44:4, 46:7, 52:10, 53:2,	53:7, 57:16, 60:10, 63:8 once 32:12 one 8:13, 15:10, 18:4, 18:15, 24:12, 25:9, 26:1, 26:19, 30:13, 35:2, 36:19, 37:2, 37:8, 39:5, 39:7, 45:11, 46:21, 47:22, 48:14, 49:9, 50:14, 50:18, 50:20, 51:8, 51:16, 54:9, 55:1, 60:5, 61:1, 62:5 ones 29:12 only 8:13, 23:7, 23:19, 51:5, 62:11 open 9:20 opening 26:18, 29:20, 53:4, 53:9, 53:13, 53:20, 54:4, 54:8, 55:4, 55:18, 56:1, 58:12 openings 53:7 opinion 14:4, 15:1, 17:9, 17:21, 19:10, 19:14, 43:16, 44:4, 44:15, 54:21 opinions 13:18, 14:1, 42:14 opportunity 8:10, 51:2	opposed 54:22 opposite 47:14 order 57:6 ordinary 17:18, 17:22, 34:12, 34:16, 35:19, 47:4, 48:20, 50:9, 51:3 orrick 3:4, 6:14 other 8:22, 9:15, 9:16, 9:19, 11:8, 11:10, 11:19, 12:6, 16:10, 24:13, 27:8, 27:14, 27:16, 28:21, 28:22, 29:5, 35:14, 38:5, 57:8, 58:10 others 29:14 otherwise 8:1, 63:7, 68:5 out 19:16, 25:14, 35:10, 35:12 outcome 68:6 outcomes 40:17 outstanding 40:9 over 7:18 overall 55:16 overview 54:1 owner 1:9, 3:9, 6:4, 6:7 P packed 22:8
--	--	---	--

page 5:2, 5:7, 5:15, 7:7, 17:4, 17:7, 24:16, 24:18, 45:22, 57:14, 57:17, 61:16, 62:4 pages 1:21, 27:10 papers 40:22, 41:1 paragraph 24:15, 24:17, 24:18, 41:20, 43:1, 43:10, 44:22, 45:3, 45:18, 46:7, 48:6, 49:2, 49:19, 52:13, 52:18, 53:3, 57:13, 60:11 parameters 49:12 parentheses 60:12 park 3:6 part 17:22, 36:6, 36:9, 37:11, 55:9 particular 12:4, 34:15, 40:13 particularly 14:18, 35:21 parties 68:2, 68:4 party 67:11 pass 65:5 patent 1:1, 1:2, 1:7, 1:9, 3:9, 6:4, 6:7, 10:9, 12:6, 13:18, 14:1, 14:5, 14:6,	16:18, 16:22, 18:10, 19:11, 31:21, 35:21, 43:11, 61:12, 63:11, 63:15, 64:12 path 29:2 pdf 17:4, 24:16, 45:22, 57:14 pending 8:14 people 58:11, 58:21 perfect 13:12, 19:16, 52:4 performance 33:18, 38:9, 39:4, 39:15 perimeter 44:20, 45:14, 47:17, 49:14 perimeters 59:14 peripheral 23:10, 23:22, 33:16 person 17:18, 17:21, 34:12, 34:16, 35:19, 47:3, 48:19, 50:8, 51:3, 56:3 petitioner 1:5, 3:2 ph 1:13, 2:1, 5:2, 5:9, 5:11, 6:2, 21:2, 21:6, 40:20, 66:2, 67:5, 67:16 phones 9:17 physical 23:6 piece 60:5	pillar 46:3 pillars 43:14 place 47:5 placed 23:11 planarization 53:22 plasma 26:13, 26:21, 27:22 play 29:16 playing 27:17 please 12:20, 13:21, 17:5, 42:7, 51:19, 61:1, 62:2 plus 14:22 point 14:3, 32:18, 43:19, 49:13, 58:20 polymer 27:21, 28:2 poor 29:4 posa 43:17, 44:4 posita 18:4, 18:6, 18:8, 21:8, 38:15, 43:3, 44:10, 44:15, 48:14 precaution 60:16 predicate 43:19 preferable 36:19 preparation 10:20	prepare 10:3, 11:4, 11:19, 16:15 prepared 15:12 preparing 14:19, 14:21 present 4:2 pressure 28:15, 28:19, 29:1 pretty 25:14, 35:22 prevalent 29:19 previously 13:1, 42:9 principles 55:7 prior 5:13, 9:22, 16:8, 18:4, 18:5, 18:22, 31:10, 31:17, 31:22, 59:7 priority 31:6, 31:20 probably 8:11, 64:20 problem 25:9, 30:20 procedures 40:5 proceeding 12:4, 61:11, 63:10, 65:13 proceedings 12:1, 40:22 process 20:3, 23:8, 23:20, 24:4, 24:7, 32:6, 32:10, 33:2, 33:21, 34:4, 34:5, 34:7, 34:10, 34:14, 35:16, 36:6,
--	---	---	--

36:9, 37:1, 37:7, 37:11, 37:12, 37:14, 37:21, 38:2, 38:3, 38:6, 38:7, 38:14, 39:1, 39:3, 39:9, 39:10, 39:18, 40:3, 40:12, 40:15, 40:16, 53:10, 54:7, 54:22, 55:10, 55:21 processes 22:15, 22:19, 24:11, 41:5 processing 55:14 produce 36:13 product 38:8, 39:4, 39:14 professional 20:12, 21:11, 21:17 pronounced 30:15, 31:3 provide 51:5, 51:10, 51:15, 52:19, 52:20 provided 16:1, 16:3, 16:4, 16:9, 62:12 public 2:6, 67:2, 68:16 published 40:21, 43:10 pulled 61:7 purpose 42:4, 47:10, 47:12, 48:9, 48:13, 58:4, 58:8, 58:13,	58:22, 59:9, 59:20, 60:12 purposes 63:6 pursuant 2:5 put 20:22, 60:11 pybas 4:3 Q qualification 21:8, 37:13 qualify 36:12 question 8:8, 8:14, 13:21, 24:9, 31:19, 34:8, 36:16, 37:20, 45:10, 55:20, 56:22, 57:7, 57:10, 59:16, 60:3, 62:11, 63:13 questions 7:8, 7:22, 8:17, 9:5, 65:4, 65:8, 65:18 quick 7:6 quite 15:6, 15:13, 15:16, 34:17 R radicals 26:13 rail 45:6 rate 27:6, 28:18 rather 23:21 ratio 25:2, 25:10, 25:11, 26:7,	29:7, 29:22, 30:19, 30:21, 31:1, 31:18, 32:3, 34:2, 35:8 reach 26:13, 27:20 reaching 27:2 reactive 26:12, 26:18, 55:7 read 48:14, 48:15, 61:15, 66:3 reading 48:18 really 20:4, 23:7, 30:3 reask 56:22 reason 26:11, 26:19, 26:20, 27:11 reasonable 43:4, 51:15 reasons 8:22, 43:8 recall 7:4, 11:1, 11:16, 12:9, 12:10, 12:15, 12:19, 14:11, 15:5, 15:17, 18:21, 39:22, 64:11 recess 41:11, 58:22, 65:2 recesses 59:6, 59:21 recipe 40:16, 54:16, 55:9 recognize 13:13, 42:11, 61:13 recognized 44:12	recognizes 43:12 record 6:12, 6:14, 6:18, 7:19, 63:6, 65:10, 65:19, 67:9 reduce 45:7, 47:14, 49:16 reduced 47:22 reduces 27:4 reducing 27:4 reduction 45:16 refer 14:5 reference 18:6, 19:1, 42:13, 43:21 references 15:20, 16:1, 16:13 referred 34:19 referring 17:7 refers 22:7 refresher 7:6 regarding 41:5 region 25:15, 29:11, 44:21, 45:15, 49:9, 49:10, 49:15, 50:21, 51:1 regular 45:6 relate 48:7 related 14:18, 17:2,
---	--	---	---

30:20, 32:1, 35:21, 41:2, 41:3, 63:15, 68:1 relates 16:17, 17:9 relating 61:10, 61:11, 63:11 reliability 35:5, 38:9, 39:5, 39:15 relied 42:14 relies 18:5, 18:7 rely 14:17, 17:15, 17:21, 18:4 relying 18:3, 18:17 remain 30:4, 30:5 remote 9:4 repeat 13:21, 22:17 replace 21:17 replaced 46:21 replacement 34:3 report 24:16, 49:19, 57:12 reported 1:22 reporter 7:14 represented 67:12 required 56:16, 57:4 requirement 38:9 requirements 39:16	requires 20:15, 24:21 research 15:3, 40:14, 40:19 researchers 40:10 researching 21:13 residing 6:19 respect 55:8 retention 33:18, 35:5 review 62:2, 64:2 reviewed 10:5, 10:6, 10:9 revisions 15:3 rie 55:9 right 6:16, 6:22, 7:5, 7:10, 7:21, 8:5, 8:8, 8:15, 9:4, 13:5, 13:7, 13:9, 14:6, 15:21, 16:12, 16:19, 17:10, 18:1, 19:12, 21:20, 24:19, 25:2, 25:3, 26:14, 28:17, 30:16, 30:22, 37:3, 37:8, 41:6, 42:2, 42:18, 44:8, 46:14, 46:18, 46:19, 46:21, 46:22, 49:5, 49:21, 50:16, 50:22, 51:21, 52:1, 58:4, 59:1, 60:22, 62:11, 62:15,	64:14, 64:16, 64:18 road 3:5 robert 3:17 role 27:17 room 9:7 rooms 47:2 row 46:21, 47:6, 50:7, 50:12, 50:17 rows 46:12, 46:17 rules 7:6 S said 19:7, 21:2, 22:2, 26:9, 38:19, 38:21, 38:22, 39:3, 49:17, 53:3, 56:21, 62:7 same 7:7, 7:17, 7:18, 14:2, 22:20, 30:5, 30:17, 30:22, 34:9, 43:5, 44:12, 46:4, 48:7, 48:22, 54:9, 54:15, 54:16, 54:17, 54:18, 55:8, 55:9, 66:4 say 15:17, 19:20, 20:7, 20:15, 21:6, 24:2, 25:4, 25:18, 27:17, 30:2, 30:3, 36:2,	37:5, 46:15, 51:13, 60:6 saying 47:13, 47:15 says 46:2 scanning 36:4 scattering 28:20, 29:9 screen 13:9 scroll 61:17 search 18:15 searching 53:2 second 13:5, 18:15, 26:2 section 17:3, 17:6, 18:18, 21:18, 27:9, 32:1, 52:21 see 13:9, 24:20, 25:6, 28:16, 36:18, 44:22, 47:2, 49:18, 50:6, 50:9, 51:8, 51:17, 57:22 seen 64:6 select 48:5 selected 48:2 selecting 48:13 sem 35:12, 36:1, 36:4 semiconducting 37:21 semiconductor 37:21
--	---	--	--

sense 15:15, 26:17, 30:11, 30:12 sentence 38:21, 48:6 sentences 24:20 separate 11:18 separator 50:3, 50:17, 51:10, 51:14 serve 42:4, 58:12 serves 58:8 session 5:5 sessions 5:13 set 12:7, 67:6, 68:8 setup 9:6 shaking 7:13 shape 55:15, 55:17, 55:22, 56:4, 56:6, 56:9, 56:15, 57:3 sheet 66:7 short 41:20, 59:19, 60:7, 60:15 short-circuit 19:8 shorted 58:17 shorting 59:4, 60:1, 60:20 should 6:13, 12:21, 13:4, 27:17, 39:6	shouldn't 57:6, 57:7 show 37:14, 44:13, 46:12, 47:8, 48:5, 48:7, 64:5 showed 44:22, 45:3 showing 14:17 side 23:11, 26:22, 28:3, 33:16, 53:13, 58:11, 59:2 side-by-side 48:2 signal 38:12 signature 66:10 signature-plkal 68:13 signed 66:7 similar 15:8, 21:10, 55:7, 55:16 similarly 50:16 simplistic 24:2 simply 59:9, 64:5 simulation 35:6 simulations 34:6, 34:19 single 18:5, 18:22 sit 14:8 six 46:12, 46:17, 47:6 skill 17:18, 17:22, 21:12, 34:12,	34:17, 35:19, 47:4, 48:20, 50:9, 51:3 skilled 31:5 slot 55:6, 56:11 slower 27:6 smaller 29:2, 29:3, 29:20, 30:14, 31:1 so-called 33:13, 35:1 solely 24:6 solid 43:6 solve 51:6 some 12:9, 12:17, 14:11, 15:8, 16:3, 16:4, 16:5, 21:17, 28:2, 29:13, 33:22, 34:6, 34:19, 35:7, 35:9, 42:14, 51:6, 51:22, 52:20, 58:10 somebody 20:6, 20:11 something 19:17, 19:20, 20:15, 32:16, 35:19, 38:15 sometimes 52:13 somewhere 12:18 sorry 12:14, 19:4, 20:8, 24:8, 26:4, 26:6, 37:5, 37:19, 38:18, 42:21,	52:8, 61:6, 63:4 sort 36:11, 43:18 sorts 31:7 sounds 21:1, 29:15, 41:10 space 49:4, 49:7, 49:18, 50:6, 50:10, 50:14 spacer 53:12, 57:21, 58:8, 58:10, 58:16, 59:3, 59:10, 59:17, 59:18, 60:13, 60:17 spacers 53:20, 59:14 spaces 50:14 speak 11:19 speaking 55:3 specialized 20:16, 20:20 species 26:12 specific 16:13, 32:20 specifically 11:3, 12:15, 22:5, 40:11, 63:18 specification 38:5, 39:12 spend 11:12, 14:19 spent 11:16 spot 32:20, 41:8, 64:20 square 22:10
--	--	---	---

stack 23:15, 25:2, 25:12, 26:8, 32:3, 33:15, 43:3, 43:7, 46:5, 52:17, 52:20, 53:4, 53:7, 58:12 staircase 44:21, 45:15, 47:17, 49:5, 49:9, 49:15, 51:1 stand 36:2, 36:3, 36:4 standard 35:15 start 6:10, 12:8, 24:21, 25:14, 37:1, 37:7, 61:8 started 12:11 starting 17:6, 34:1 state 6:13, 61:9 states 1:1 static 28:9 stating 6:11, 6:17 steps 34:14, 53:6, 54:1 still 8:7, 49:18, 51:11, 55:7 storage 22:7, 22:8, 45:7 straight 28:12 straightforward 55:12 street 3:19	strike 17:16, 32:5, 36:7, 37:10, 56:13, 58:5 string 42:6 strings 41:21 structure 33:8, 43:3, 43:15, 44:3, 45:5, 45:7, 46:3, 46:6, 50:4, 50:10, 50:15, 50:18, 50:19, 51:3, 51:10, 51:14, 55:12, 55:13, 56:12, 57:20, 60:8, 60:14 structures 23:17, 41:21, 43:2, 52:14, 57:19 students 40:21 submitted 13:14 subsequent 53:16, 58:13, 60:15 substantive 14:12 success 43:4 sue 4:3 sufficient 59:3 suite 3:13, 3:19 support 43:14, 51:5, 51:11, 51:12, 51:15 sure 12:3, 24:10, 29:14, 32:17,	32:21, 33:5, 36:16, 38:3, 38:19, 39:1, 39:10, 39:14, 40:2, 49:6, 54:16, 56:3, 57:1, 59:2, 59:18, 60:4, 60:6, 60:13, 62:1, 62:3, 64:4 surface 53:22 sutcliffe 3:4 sworn 6:3, 67:6 system 60:7 T t-a-c 52:3, 59:15 t-e-s-s-a-r-i-o-l 31:13 table 10:8 tac 28:6, 29:18, 29:20, 30:2, 30:3, 52:2, 52:5, 52:22, 53:3, 54:22, 56:15, 57:3, 59:15, 59:18, 60:1, 60:6, 60:12, 60:14, 60:20 take 8:10, 13:5, 22:1, 41:8, 49:4, 49:6, 62:2, 62:7, 62:20, 64:1, 64:3, 64:21, 65:1 taken 11:14, 41:11, 65:2, 67:8	taking 8:18, 14:17 talk 7:17, 16:12, 16:14, 19:18, 20:4, 20:6, 54:3, 57:14, 57:18 talked 34:2, 36:17, 40:2, 51:21 talking 20:11, 25:1, 27:18 tapering 25:13, 25:20, 26:5, 26:9, 27:10, 27:12, 27:16, 29:22, 31:2 target 33:17 targeting 33:20 teaching 21:14, 40:8 technician 4:3, 13:4 technologies 1:7 technology 1:4, 52:21, 67:12 tell 15:11, 19:7 tem 35:12, 36:1, 36:3 ten 41:7, 64:21, 65:1 tend 28:21 term 18:9, 18:13, 21:21, 41:13, 41:16, 52:1 terms 14:21, 22:12,
---	--	---	---

22:13, 33:18 tessariol 31:12 test 35:10 testified 6:3 testimony 8:20, 9:1, 21:5, 62:13, 66:4, 66:6, 67:9 testing 36:18, 39:13 texas 6:20, 6:21, 40:9 textbook 27:9, 31:15 th 62:6, 63:16, 68:9 thank 65:3, 65:6 therefore 28:3, 30:22, 31:2, 58:18, 59:11 thing 8:13, 51:8 things 54:19 think 10:10, 12:13, 19:13, 22:4, 24:2, 29:12, 33:5, 33:7, 38:19, 47:20, 49:17, 52:12, 58:4, 58:5, 59:8, 60:4 thought 26:4 three 21:10, 64:3 threshold 35:4 through 25:2, 38:13,	52:16, 53:4, 53:7, 62:1 through-array 28:6, 52:1, 52:2, 52:11, 52:15, 57:18, 58:14, 58:17, 59:4 through-silicon 52:14 through-stack 53:13, 54:4, 54:8, 55:4, 55:18, 55:22 throughput 28:19 thursday 1:15, 67:16 time 8:5, 11:16, 11:17, 12:9, 12:17, 12:19, 26:13, 27:20, 28:9, 31:6, 48:22, 54:16, 62:2, 62:7, 62:20, 64:1 timely 65:16 times 7:3, 7:4, 11:2 today 8:20, 9:2, 10:4, 14:8 today's 5:5 token 7:17 tools 35:1, 35:2 top 26:10, 27:1, 50:11, 50:17, 53:22 topic 32:2 total 11:12, 15:12	totally 19:6 trademark 1:1 transcript 5:6, 5:8, 5:10, 61:5, 61:20, 62:19, 62:22, 63:10, 63:15, 63:18, 63:21 transcription 66:5 transmission 36:3 trap 33:10 trench 23:17 trial 1:2 true 66:4, 67:9 truthful 8:19, 9:1 try 7:17, 19:8, 31:11, 34:9, 35:12 trying 20:21, 20:22, 33:1, 43:18, 54:20, 56:7 tsv 52:15 tungsten 53:19 turn 50:18 turned 50:13 twice 38:20 two 21:10, 24:20, 27:11, 27:19, 30:13, 30:17, 47:21, 48:2, 48:5, 48:13,	48:19, 57:19, 58:12, 61:16, 64:3 type 33:9 typically 35:6, 55:12 typo 14:11 U u-shape 33:13 under 23:12, 62:12, 64:14 underneath 33:17 understand 7:21, 8:6, 16:17, 20:21, 33:1, 34:13, 34:17, 35:2, 35:22, 36:16, 36:20, 37:20, 38:16, 38:19, 43:18, 51:4, 54:20, 60:5, 61:10 understanding 16:21, 17:1, 17:12, 18:12, 18:19, 19:5, 41:16, 56:14, 57:2, 58:7 understood 8:1, 29:15 undesirable 25:17 unit 23:2 united 1:1 university 40:8, 41:4 unless 27:13 unmarked 61:2
---	--	--	---

unrelated 61:11 upload 13:5 uploading 13:3 upward 50:18 use 32:3, 34:3, 35:2, 42:18, 61:9, 63:2 uses 28:1 using 9:15, 34:1 usually 34:6 ut 40:19 V vague 57:8 validate 36:12 validation 37:13, 38:2, 38:7, 38:17, 38:20, 38:22, 39:3, 39:13, 39:18, 40:4 validations 37:22, 38:14, 40:1 various 59:7 verbal 7:12 verification 38:1, 38:13, 39:6, 39:7, 39:9, 39:18, 40:4 verifications 38:17, 40:1 version 63:21	versions 30:15 versus 48:10, 48:11 vertical 29:6, 33:12, 52:12, 52:15, 53:4 via 52:14, 57:20, 60:8, 60:14 vias 52:12, 52:14 view 18:7 virginia 2:7, 67:3, 68:17 virtually 1:14, 2:2, 67:8, 67:16 vocabulary 60:5 voltage 35:4 W wabash 3:12 wafer 22:10, 34:1 wall 26:22, 28:3, 53:13, 58:11, 59:2 want 19:18, 24:9, 27:13, 28:16, 28:17, 35:8, 38:18, 52:9, 54:3, 56:11, 59:2, 62:3, 62:8, 65:9 wanted 39:5, 65:15 washington 3:20 watkins 3:11, 3:18, 6:9	way 31:20, 32:13, 40:20, 68:5 we'll 8:10, 61:3 we're 6:8, 7:6 we've 41:6, 51:21, 64:19 weeks 11:1, 64:6 welcome 64:1 well-known 31:20, 34:16 went 15:2 west 6:20 whatever 65:10 whereof 68:8 whether 23:3, 23:11, 23:16, 23:17, 26:12, 33:10, 33:12, 33:16, 34:3, 35:13, 35:17, 38:5, 38:10, 39:22, 55:4, 56:11, 56:14, 57:2, 63:20, 64:7 white 48:10 whitehead 1:22, 2:5, 67:2 whole 37:1 wide 25:15 wider 59:10 within 47:9, 47:16 without 46:17, 58:16	witness 3:2, 10:1, 10:14, 37:19, 41:10, 42:21, 65:5, 65:6, 67:5, 67:9, 68:8 wordline 53:17, 58:15, 58:18, 59:5, 59:15, 59:19, 60:1, 60:21 wordlines 33:15, 53:17, 60:15 words 21:1, 28:21, 29:5, 38:5 work 34:20, 36:7, 36:11, 40:9, 41:3 worked 10:11 working 12:11, 20:13, 21:11, 21:13, 36:13, 37:15 works 7:19, 41:8, 64:22 wouldn't 6:10, 6:17 write-up 15:9 writing 14:15, 14:22, 15:3 wrong 19:6, 19:7 wrote 14:13 Y yangtze 1:7 yeah 10:6, 10:19, 12:9, 12:10,
---	--	--	--

12:13, 15:2, 27:16, 28:2, 30:17, 36:17, 36:21, 37:9, 37:17, 38:10, 46:1, 49:22, 55:20, 56:10, 58:3, 60:11, 60:12, 61:22, 62:4, 63:14, 65:1, 65:7 year 12:10, 12:13, 21:10 yield 22:13	1020 31:14 1027 45:1 1040 31:14 1046 43:12, 46:2 108 57:13, 60:11 109 24:16, 24:18, 53:3 11,581,322 1:8, 13:19, 14:1 12 17:5, 17:7, 65:19, 67:17 13 5:16 136 31:13 140 43:1, 49:2 143 44:22 149 49:2 16 47:11 17 45:4, 47:12, 51:9	2027 68:12 205 24:15, 24:18 209 24:17 22 46:2 2200 3:21 23 1:15, 67:17 25 5:8, 5:10 254 62:17, 63:15, 64:11, 65:12 28 68:9 2800 3:13	35:18, 36:6, 36:10, 37:2, 37:8, 37:15, 38:10, 39:18, 39:21, 40:7, 41:2, 49:12, 52:22, 55:4
z			4
zoom 9:16, 9:19			40 15:18, 40:20 410 50:21 42 5:17 420 50:21 43 43:10 45 45:22, 50:4, 50:13, 50:18 47 50:5, 51:10, 51:14
0			5
00191 1:5 00791 61:17, 61:21 00911 61:18 08 1:16, 67:17			50 15:18 54 57:14 55 43:3, 45:20, 46:5, 48:11, 50:12 555 3:19 57 52:13, 52:18 5803 6:20
1			6
10 1:16, 67:17 1000 3:5, 3:19 1003 5:16, 12:21, 13:1, 13:13, 45:22, 46:8 1005 5:17, 42:8, 42:9, 42:11, 42:17, 44:1, 51:19 1010 31:16 1015 3:6	2 20004 3:20 202 3:21 2024 12:14, 61:21, 63:16 2025 1:5, 1:15, 62:6, 63:1, 63:19, 67:17, 68:9	3 30 5:8, 5:10, 7:4, 15:18, 62:6, 63:16 31 68:12 312 3:15 322 10:9, 14:5, 19:11, 31:21, 35:21 330 3:12 34 63:1, 63:19 36 65:19, 67:17 3d 19:19, 20:2, 21:21, 22:4, 22:6, 24:21, 26:8, 31:7, 32:3, 32:7, 33:8, 34:10,	600 40:21 601327 1:20 60611 3:14

61
5:8, 41:20
614
3:7
62
5:10
637
3:21
650
3:7
66
45:5, 45:21,
46:3, 48:11,
50:15, 51:12
68
1:21

7

74
58:1, 58:8,
59:3, 59:18,
60:13
7400
3:7
76
58:1, 60:8,
60:14
7700
3:15
78731
6:21

8

806
61:2, 65:11
876
3:15
89
45:3, 45:18,
46:7, 48:6,
49:19

9

94025
3:6