

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: November 17, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00191
Patent 11,581,322

PATENT OWNER'S RESPONSE

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2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
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2006	Disclaimer in Patent Under 37 C.F.R. § 1.321(a)
2007	Declaration of Dr. Stephen A. Campbell ("Campbell")
2008	<i>Curriculum Vitae</i> of Dr. Stephen A. Campbell
2009	<i>Inside Solid State Drives (SSDs)</i> (Rino Micheloni et al. eds., 2d ed. 2018)

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2010	RESERVED
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2021	Declaration of Stephen Campbell in Support of Patent Owner's Response ("Campbell2")
2022	Transcript of the Deposition of Jack C. Lee, Ph.D., taken July 30, 2025, <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00034 ("Lee '254 Dep.")
2023	Harmeet Singh, <i>Overcoming Challenges in 3D NAND Volume Manufacturing</i> , 60 Solid State Technology 18 (July 2017)

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2025	Mark Lapedus, <i>What's Next for NAND?: Vendors Pin Hopes on 3D Memory, Raising Specter of 2D NAND Shortages; Other Memory Types Add to Uncertainty</i> , Semiconductor Eng'g (May 19, 2016), https://web.archive.org/web/20161127122539/https://semiengineering.com/whats-next-for-nand/ (last visited Aug. 15, 2025)
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2031	Mark Lapedus, <i>NAND Market Hits Speed Bump: Transition from Planar to 3D NAND is Harder and More Time-Consuming Than Expected</i> , Semiconductor Eng'g (June 21, 2017), https://web.archive.org/web/20180625071314/https://semiengineering.com/nand-market-hits-speed-bump/ (last visited Aug. 15, 2025)
2032	Mark Lapedus, <i>3D NAND Race Faces Huge Tech and Cost Challenges: Shakeout Looms as Vendors Struggle to Find Ways to Add More Layers and Increase Density</i> , Semiconductor Eng'g (May 23, 2019), https://web.archive.org/web/20190619034609/https://semiengineering.com/3d-nand-race-faces-huge-tech-and-cost-challenges/ (last visited Aug. 15, 2025)
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2034	Timothy Yang, <i>Creating Higher Density 3D NAND Structures: Identify the Manufacturing Issues Associated With Increased 3D NAND Density to Make the Best Tradeoffs and Avoid Structural Collapse</i> , Semiconductor Eng'g (Feb. 21, 2019), https://semiengineering.com/creating-higher-density-3d-nand-structures/ (last visited Aug. 15, 2025)
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2037	RESERVED
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I. Introduction

Patent Owner Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) submits this Patent Owner’s Response in the *inter partes* review of U.S. Patent No. 11,581,322 (“the ’322 Patent,” Ex.1001). As explained below, Petitioner has not met its burden to show that any of the challenged claims are unpatentable.

The ’322 Patent describes and claims innovative methods for forming 3D memory structures with a vertical “through array contact,” or “TAC,” with a “first lateral dimension [or diameter] of the TAC ... larger than a second lateral dimension [or diameter] of the TAC” and “a dummy channel structure” that extends through a stack of dielectric and sacrificial layers. ’322 Patent 1:51-54, 1:64-65, 5:6-9, 13:40-65, cls. 13-14. The ’322 Patent claims such memory structures with (i) “dummy channel[s]” and (ii) a TAC having “a substantially circular section.” *See id.* cls. 3, 6, 8-10, 13-16, 19-20.

Petitioner asserts that the challenged claims are invalid based on Nishikawa, alone or in combination with Nishikawa¹²³ and/or Lu. But each of Petitioner’s grounds does not disclose several key claim limitations, including: (1) the use of dummy channels, (2) the “first lateral dimension [or diameter] of the TAC ... larger than a second lateral dimension [or diameter] of the TAC,” or (3) a “substantially circular” TAC. Petitioner instead seeks to supply these missing limitations by

invoking the “general knowledge” of a POSITA, but Petitioner’s attempt to back-fill limitations to argue the claims of the ’322 Patent were obvious fails.

First, Petitioner’s assertion that a POSITA would have been motivated to modify Nishikawa’s trench-shaped backside contact 76 to be substantially circular is incorrect. Indeed, POSITAs would have understood that making this change would defeat Nishikawa’s stated purpose of having dual memory cells on each level of the memory stack and render Nishikawa’s system inoperable for its intended purpose because a circular TAC in Nishikawa would cause short circuiting in Nishikawa’s device. A combination that interferes with a reference’s stated purpose or renders the combined device inoperable would not have been obvious. *Medtronic, Inc. v. Teleflex Innovations S.a.r.l.*, 69 F.4th 1341, 1349-50 (Fed. Cir. 2023) (“[I]t was error for the Board to ignore evidence that a proposed modification would interfere with a reference’s stated purpose.”); *In re Fritch*, 972 F.2d 1260, 1265 n.12 (Fed. Cir. 1992) (“[A] proposed modification [is] inappropriate for an obviousness inquiry when the modification render[s] the prior art reference inoperable for its intended purpose.”).¹

¹ All emphases are added and internal quotation marks and citations omitted unless otherwise noted.

Second, as the Board correctly found in its institution decision, Petitioner failed to establish that it would have been obvious to modify Nishikawa to add dummy channels, as recited in claims 3, 6, 14-18, and 20. To the contrary, POSITAs would not have been motivated to add dummy channels to Nishikawa's memory stack for structural support because Nishikawa already has *other* support structures to perform that function, and adding dummy channels would have reduced storage capacity, increased costs, and increased the risk of defects.

Third, as the Board correctly found in its institution decision, Petitioner's obviousness position for the first and second lateral dimensions/diameters of the TAC, as recited in claims 13-18 and 20, fails under either of Petitioner's proposed claim constructions. Petitioner engaged in blatant hindsight, arguing the '322 Patent's stated purpose would have motivated a POSITA to modify Nishikawa to include the claimed lateral dimensions/diameters. And Petitioner's evidence establishes that a POSITA would *not* have been motivated to form a TAC with the claimed dimensions/diameters.

Finally, Petitioner relies on a POSITA's general knowledge to fill in for these missing limitations, but that reliance is misplaced. General knowledge can be invoked to fill in a missing limitation *only* if the limitation in question is "unusually simple and the technology particularly straightforward." *DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018). Petitioner has failed to present any

evidence that any of the missing limitations are unusually simple or that 3D NAND structures are particularly straightforward. Nor can it, as 3D NAND is far from straightforward. And the limitations missing in Nishikawa are complex, not unusually simple. All of the Petition's grounds fail on this basis alone. Further, Petitioner's use of general knowledge fails to comply with 35 U.S.C. § 311(b) and 37 C.F.R. § 42.104(b)(4) because it does not ground its obviousness inquiry in only "prior art consisting of patents or printed publications."

Thus, the Board should find that Petitioner failed to prove any claim of the '322 Patent would have been obvious.

II. Background

A. Only Claims 3, 6, and 8-20 are at Issue

Micron challenged claims 1-20 of the '322 Patent on four grounds, all of which rely on Nishikawa. Pet. 10. On April 28, 2025, YMTC disclaimed claims 1-2, 4-5, and 7 before the Board's institution decision. Ex.2006; ID (Paper 22) 2, 7 n.3. Therefore only claims 3, 6, 8-20 are at issue in this proceeding. Of those claims, the Board found Micron did not meet its burden for institution with regard to claims 3, 6, 13-18, and 20, but only for claims 8-12 and 19. ID 2.

B. 3D NAND Memory Technology

3D NAND memory devices are "memory arrays" with memory cells stacked vertically. Memory cells can be written or read by applying a voltage to corresponding conductors that run horizontally across the memory array, called

“wordlines.” Ex.2021 (“Campbell2”) ¶40. An exemplary 3D NAND memory is shown in Figure 5.20 of Exhibit 2009, reproduced below, which depicts a series of vertically stacked memory cells, each controlled by a “Control Gate” (the wordline) shown in red as “CG0” through “CG3.” *Id.*; Ex.2009 134. The ends of the “Control Gates” are staggered to form a staircase that allows vertical vias to access and contact each wordline (CG0 to CG3) and connect them to peripheral devices. Campbell2 ¶40.

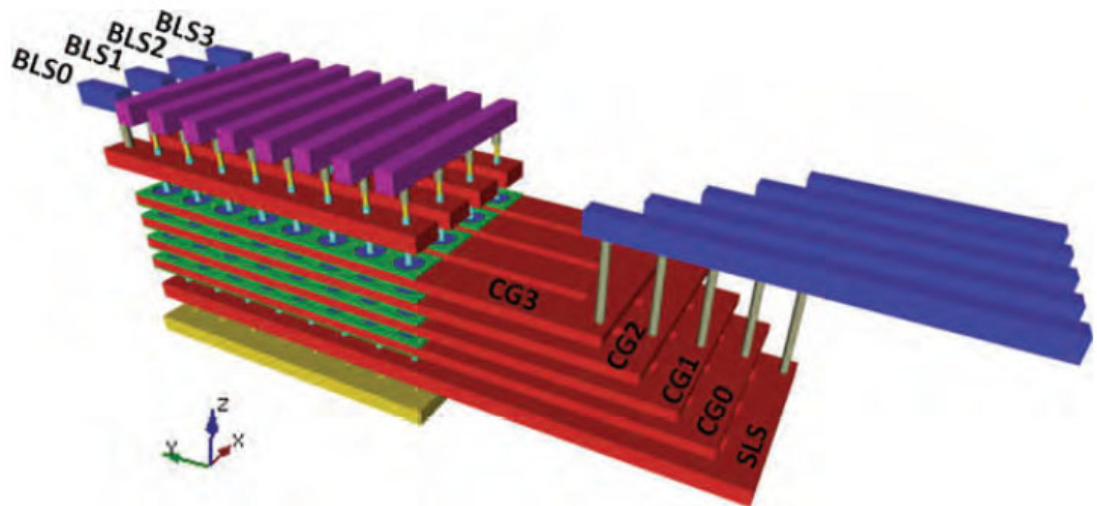


Fig. 5.20 C-FG NAND Flash array with fan-out

C. The '322 Patent

The '322 Patent recognized that 3D memory devices require TACs for “providing vertical interconnects between the stacked memory array device and peripheral device (e.g., for power bus and metal routing).” '322 Patent 4:58-62. Previously, TACs were formed within “barrier structures” to “preserve[] a dielectric

stack region within a memory stack for ease of etching the openings of the TACs.” *Id.* 4:62-65. A drawback of a “barrier structure[]” is that “the regions enclosed by a barrier structure take up large area in the core array region where memory strings can be formed.” *Id.* 4:62-5:1; Campbell2 ¶¶41-42 (discussing prior art example of barrier structures). TACs within a barrier structure “also have a negative impact on the resistance of word lines.” ’322 Patent 4:62-5:1; Campbell2 ¶42. “Moreover, the existing fabrication processes for forming the barrier structures become more challenging for the next-generation 3D memory devices,” which “have less process margin” (*i.e.*, room for error). ’322 Patent 5:2-5; Campbell2 ¶42.

The ’322 Patent discloses a novel “3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures.” ’322 Patent 5:6-9. It explains that, “by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost.” ’322 Patent 5:9-12; Campbell2 ¶43. In addition, “[m]ore process margin” may “be obtained due to the elimination of etching and alignment steps for making the barrier structures.” ’322 Patent 5:13-18; Campbell2 ¶43.

To “further simplify the fabrication flow and reduce process cost,” the ’322 Patent teaches its TACs can be “formed in the same fabrication process(es) for making other structures” such as “peripheral contacts” outside of the memory stack.

'322 Patent 5:17-23; Campbell2 ¶43. As a result, TACs 416 not enclosed by barrier structures can have the same shape as the peripheral contact 420, including a “substantially circular shape in the plan view,” as shown in Figure 4C below where the circular cross section of the TAC (green box) matches the circular cross section of the peripheral contact (blue box). '322 Patent 8:56-57; Campbell2 ¶43.

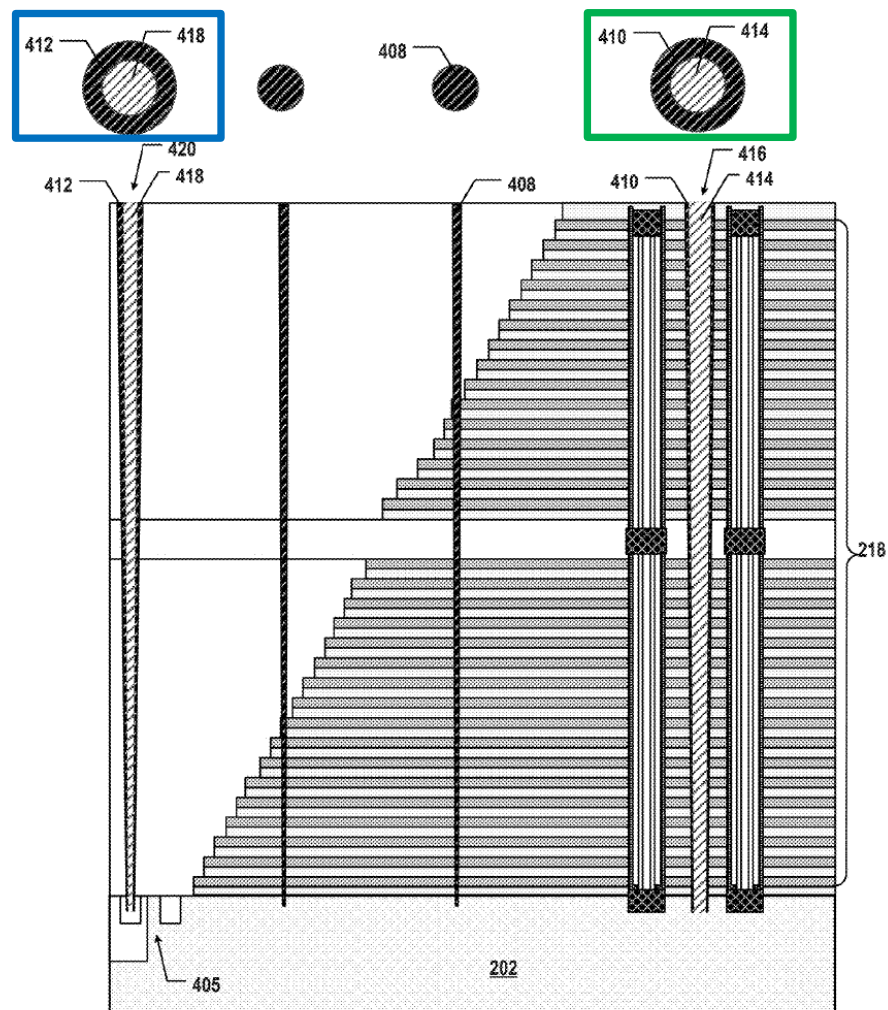
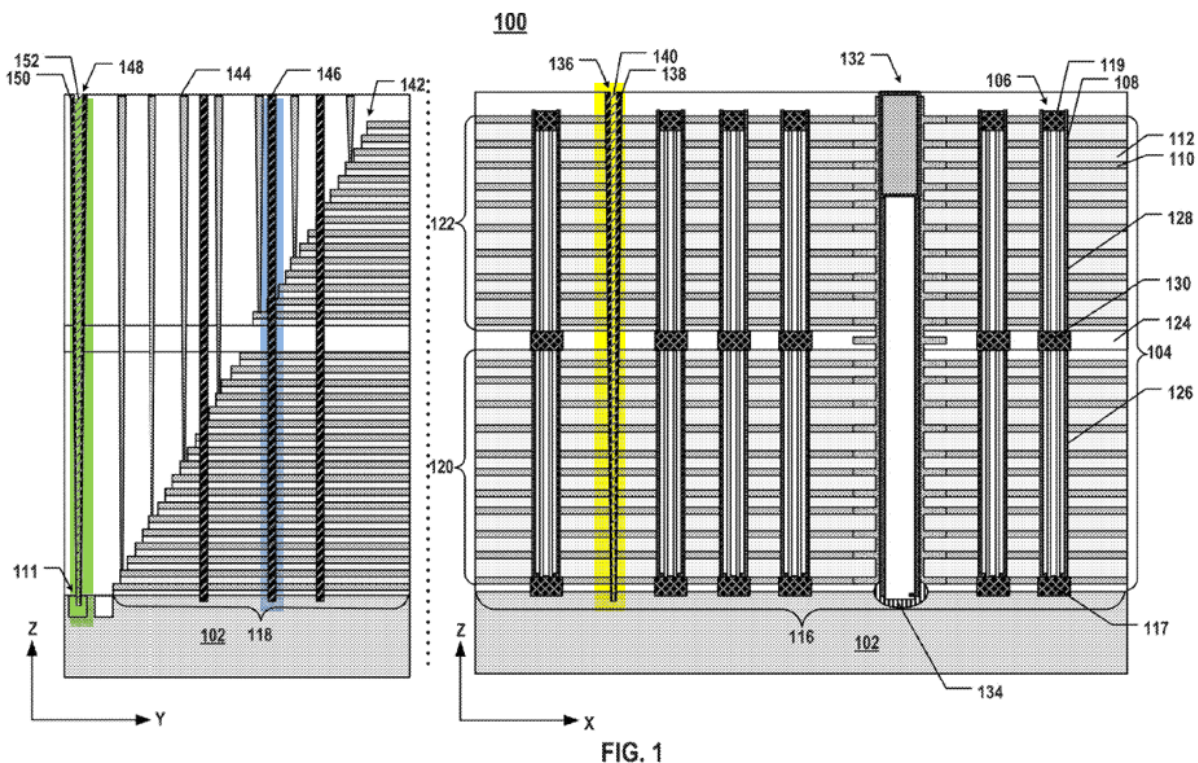


FIG. 4C

'322 Patent Fig. 4C (annotated)

Figure 1, reproduced below, illustrates a cross-section of an embodiment of a “memory stack 104” and a “staircase structure” 142. *Id.* 8:63-65. As shown below, the memory device 100 includes a TAC 136 (yellow) that extends vertically through the stack to carry electrical signals to/from the memory device 100. *Id.* 8:30-46. Unlike the prior art, TAC 136 is not “enclosed by barrier structures.” *Id.* 5:6-22. This allows the TACs to be “formed in the same fabrication process(es) for making other structures,” including those *outside* the memory array such as “peripheral contact” 148 (green). *Id.* 5:6-22; 12:28-49. In addition, “dummy channel structures 146” (blue) are “disposed in the outer region 118 of memory stack 104 as shown in Fig. 1” to “provide mechanical support to the memory array structures, e.g., memory stack 104.” *Id.* 9:41-51.



The '322 Patent also teaches TACs that can have “spacer[s]” lining the sidewalls of the TAC. '322 Patent 13:38-40. In one example, the spacers may be formed in an opening for the TAC where the opening contains a “plurality of recesses” formed by “removing parts of the sacrificial layers abutting the sidewall of the first opening.” *Id.* 13:42-45, 14:1-5, Figs. 3D, 7B (showing a process for forming recesses); Campbell2 ¶45. As a result, as shown below in Figure 3D, the TAC may be formed into these recesses where the sacrificial layers were removed.

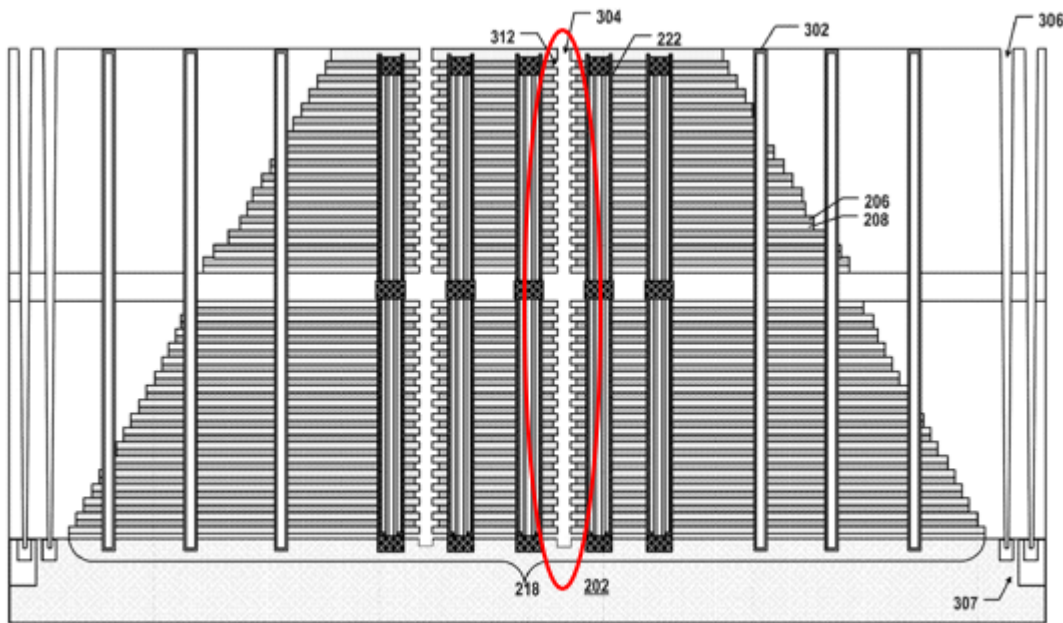


FIG. 3D

'322 Patent Fig. 3D (annotated); *see id.* Fig. 3E.

D. Person of Ordinary Skill in the Art

For purposes of this proceeding only, Patent Owner does not object to the definition of a POSITA proffered by Petitioner and adopted by the Board at institution, except as indicated in Dr. Campbell's declaration. Pet. 27; ID 8;

Campbell2 ¶35. The remaining challenged claims are valid regardless of the precise definition used for a POSITA. Campbell2 ¶35.

E. Claim Construction

The prior art relied on in the Petition fails to disclose the subject matter of the challenged claims under any reasonable construction, including their plain meaning.

Id. ¶38.

III. Nishikawa and a POSITA's knowledge, alone or with Nishikawa123, do not render obvious a TAC with "a substantially circular section" (Claims 6, 8-20).

A. Petitioner fails to establish that a POSITA would have had a reasonable expectation of success or been motivated to modify Nishikawa's trench-shaped backside contact via to be a circular TAC.

Claims 8 and 14 (independent) and claim 19 (dependent) recite a TAC with "a substantially circular section" and "extending vertically through the conductor/dielectric layer pairs in the memory stack." Claim 8 adds that the TAC "compris[es] a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate." Claims 9-13 and 15-20 depend from claims 8 and 14, respectively.

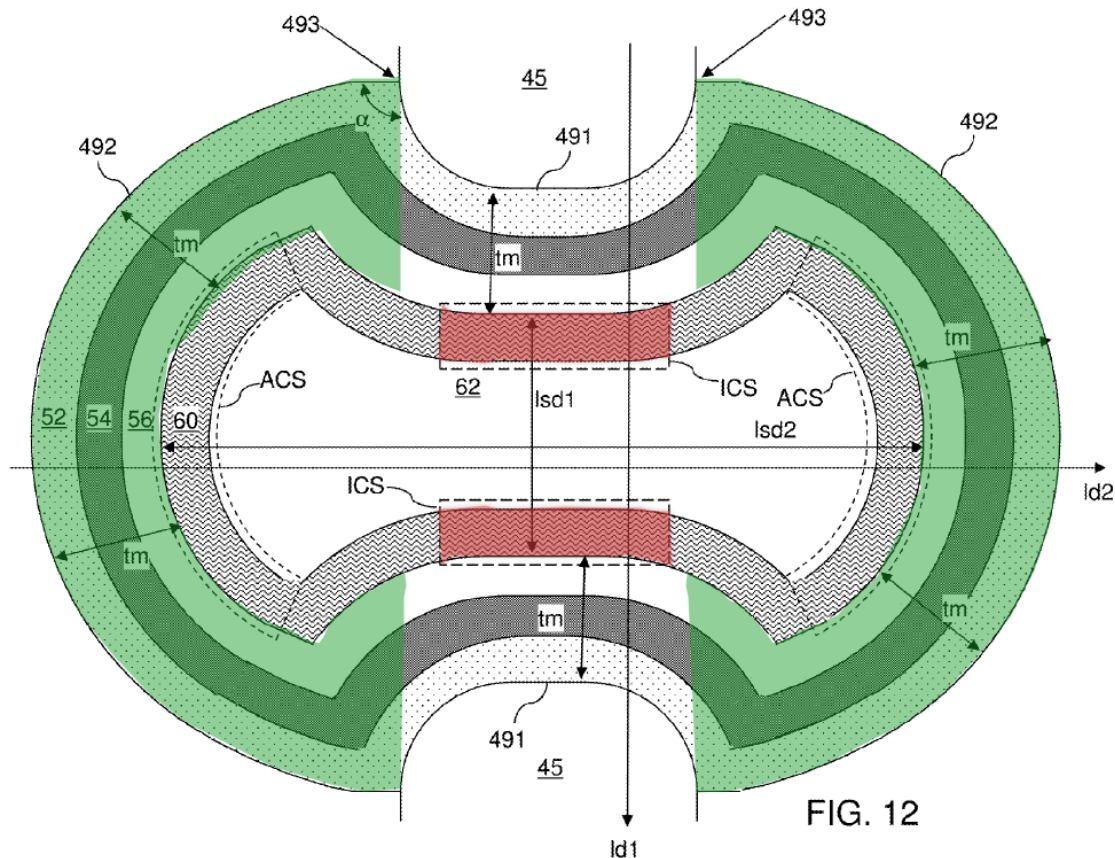
Petitioner acknowledges that Nishikawa (Ex.1005) does not disclose a TAC with a substantially circular section. Pet. 43, 78; *see* Ex.1003 ¶180. Petitioner argues instead only that "it would have been obvious to implement Nishikawa's structure 76 as a circular TAC," relying a POSITA's knowledge (Ground 1) and in

combination with Nishikawa123 (Ex.1046) (Ground 3). Pet. 43-50, 78, 82-83, 98-99; *see* Ex.1003 ¶¶113-128, 180, 193, 201, 238. Both grounds fail.

1. A circular TAC would defeat Nishikawa's purpose and render it inoperable.

Petitioner asserts that a POSITA would have been motivated to include a circular TAC in Nishikawa instead of a trench-shaped backside contact in view of the knowledge of a POSITA, which Petitioner asserts includes Nishikawa123, because they have “the same structure.” Pet. 43-44. To the contrary, a POSITA would not have modified Nishikawa as such because it would nullify Nishikawa's stated purpose and render Nishikawa inoperable. Campbell2 ¶49; *Medtronic*, 69 F.4th at 1349-50; *Fritch*, 972 F.2d at 1265 n.12.

Nishikawa's invention is a “vertical memory device including dual memory cells per level” enabled by “separate control gate electrodes in the same horizontal device level.” Ex.1005 Abstract, 15:27-30; *see id.* 17:58-61; Campbell2 ¶49. Nishikawa's “memory stack structures” 55 include a “first portion 50A” of “the memory film (52, 54, 56)” and a “second portion 50B” of “the memory film (52, 54, 56)” (green) divided by active and inactive (red) portions of the memory stack structure's “vertical semiconductor channel 60” on each side of the separator dielectric structures 45, as shown below in Figure 12 below:



Nishikawa Fig. 12 (annotated)

Nishikawa 14:33-46, 14:60-15:2; Campbell2 ¶50. As shown below in Figure 14, the first memory cell portion 50A (yellow) is “located adjacent to” a “first control gate electrode 461,” and a second memory cell portion 50B is “located adjacent to a “second gate electrode 462” (purple). Nishikawa 14:60-15:1; Campbell2 ¶51.

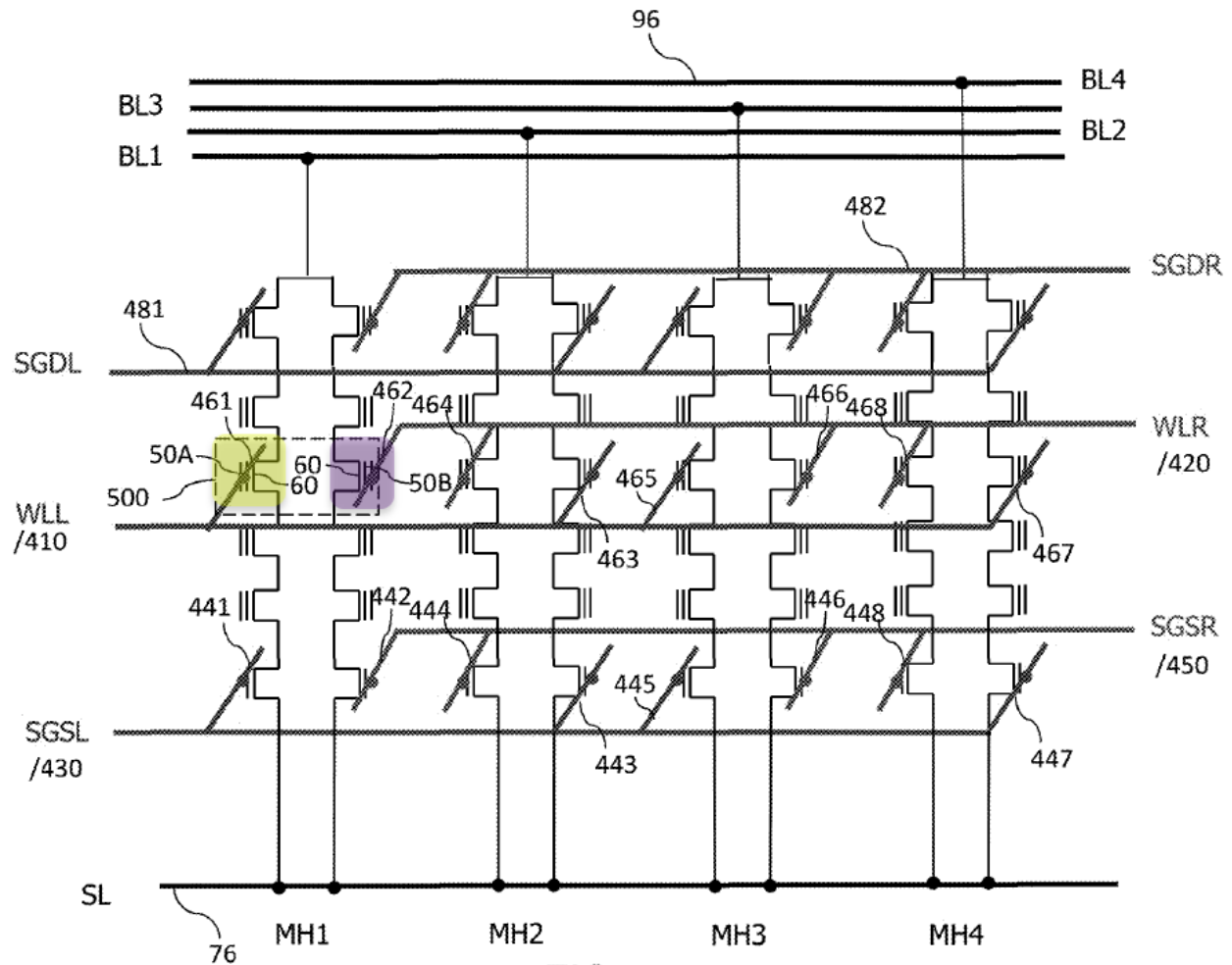
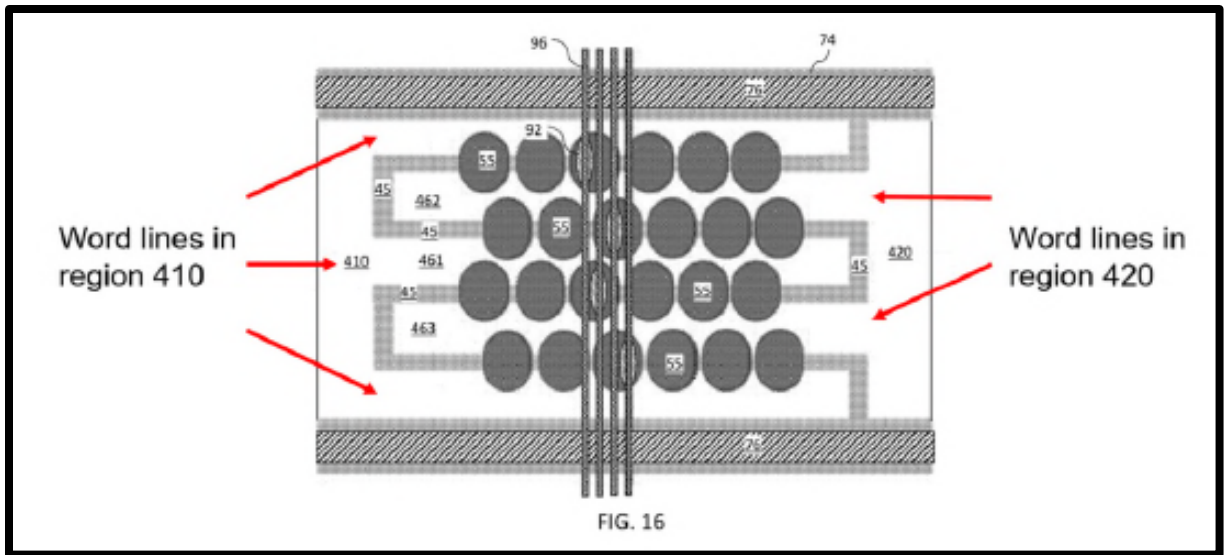


FIG. 14

Nishikawa Fig. 14 (annotated)

As a result of the memory cell portions 50A/B and the separator dielectric structure 45, the first and second gate electrodes 461/462 are “electrically insulated.” Nishikawa 14:60-15:4; Campbell2 ¶51.

Moreover, each level of control gate electrodes includes a first wordline 410 and a second wordline 420. Campbell2 ¶52. These wordlines and their corresponding gate electrodes are shown below:



Pet. 57 (annotating Nishikawa Fig. 16)

The first wordline 410 is connected to a plurality of gate electrodes, e.g., 461, that extend from the stepped contact portion into the “device region.” Nishikawa 15:31-37; Campbell2 ¶53. The second wordline 420 also is connected to a plurality of gate electrodes, such as 462. Nishikawa 15:37-42; Campbell2 ¶53. Importantly, the wordlines 410/420 are electrically isolated—*i.e.*, enabling dual memory cells and separate control gate electrodes in the same level in each opening—by the (1) backside contact via structure 76 and its dielectric spacer lining 74 surrounding the trench structure 76; and (2) the separator dielectric structures 45. Campbell2 ¶53; Nishikawa Abstract, 6:57-59, 15:31-32, Fig. 16. Indeed, Nishikawa’s dielectric spacer lining 74 “provide[s] electrical isolation for the backside contact via structure 76.” Nishikawa 6:57-59; Campbell2 ¶53. And the dielectric separator structures 45 “laterally separate the control gate electrodes 46” at each level. Ex. 1005 17:16-18;

Campbell2 ¶53. Nishikawa's backside contact via structure 76 and dielectric spacer 74 are formed "through the alternating stack (32, 46)" and are thus surrounded by the conductive layers 46—the conductive layer forming, e.g., "the first control gate electrode 461." Nishikawa 6:54-57, 14:60-62; Campbell2 ¶53; *see* Pet. 39. Thus, the backside contact via structure 76 and dielectric spacer lining 74, with the separator dielectric structures 45, electrically isolate the two separate wordlines, 410 and 420, at every level of the stack, as shown below. *See* Nishikawa 17:14-23; Campbell2 ¶53.

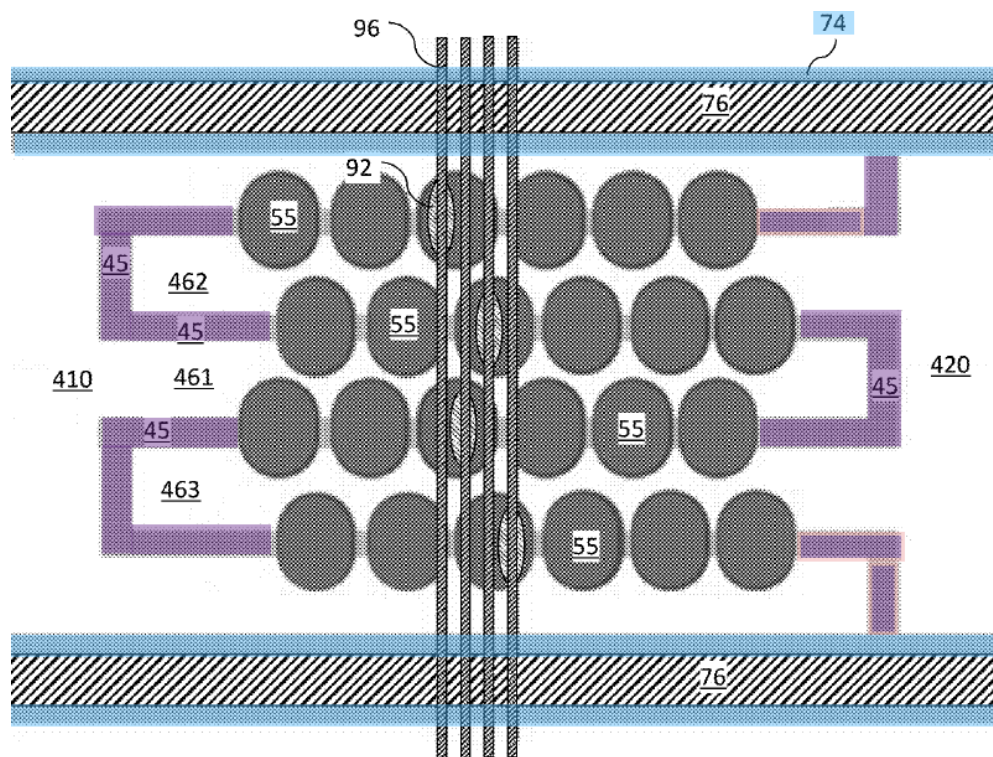
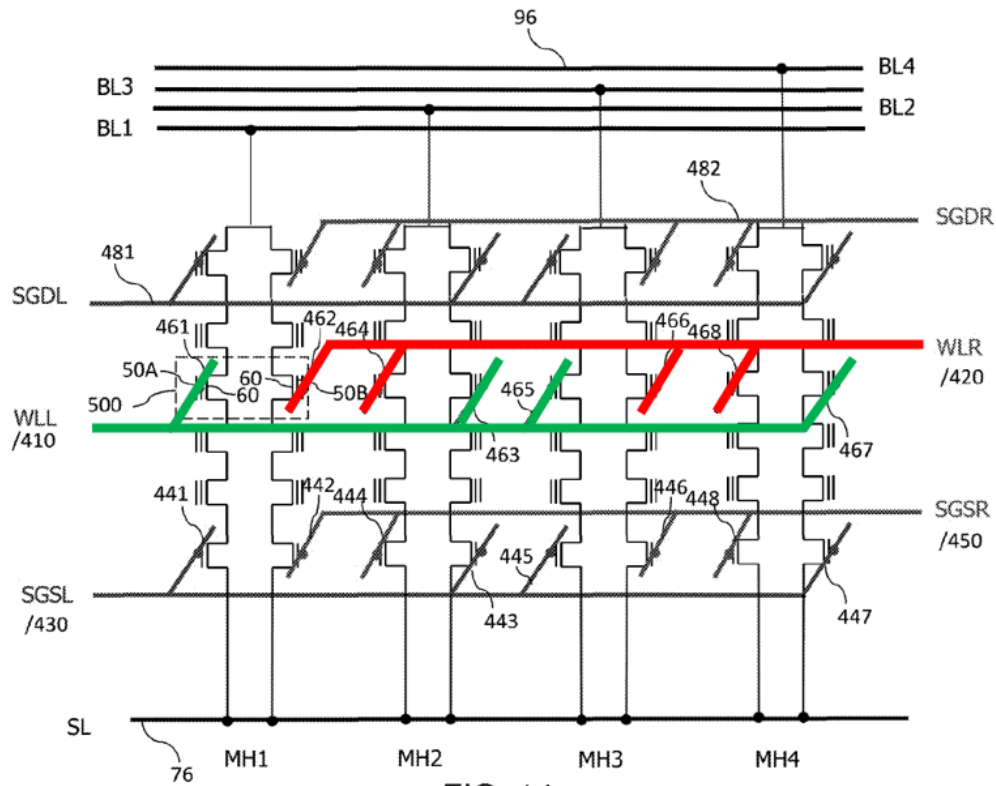


FIG. 16

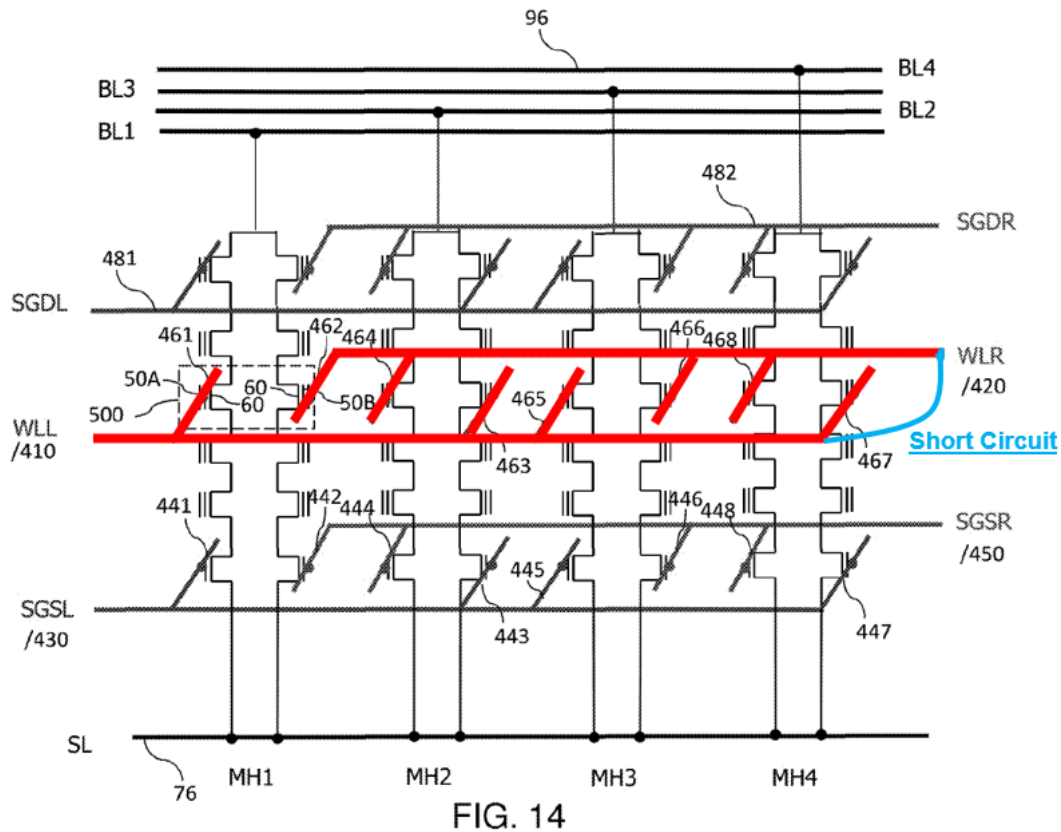
Nishikawa Fig. 16 (annotated)

This separation is crucial to Nishikawa's device. Campbell ¶54. The electrical separation allows for two wordlines at each level, WLL/410 (green) and WLR/420 (red), to be individually connected to their respective gate electrodes (461/462) and each memory region (50A/B), as shown in Figure 14:



Nishikawa Fig. 14 (annotated)

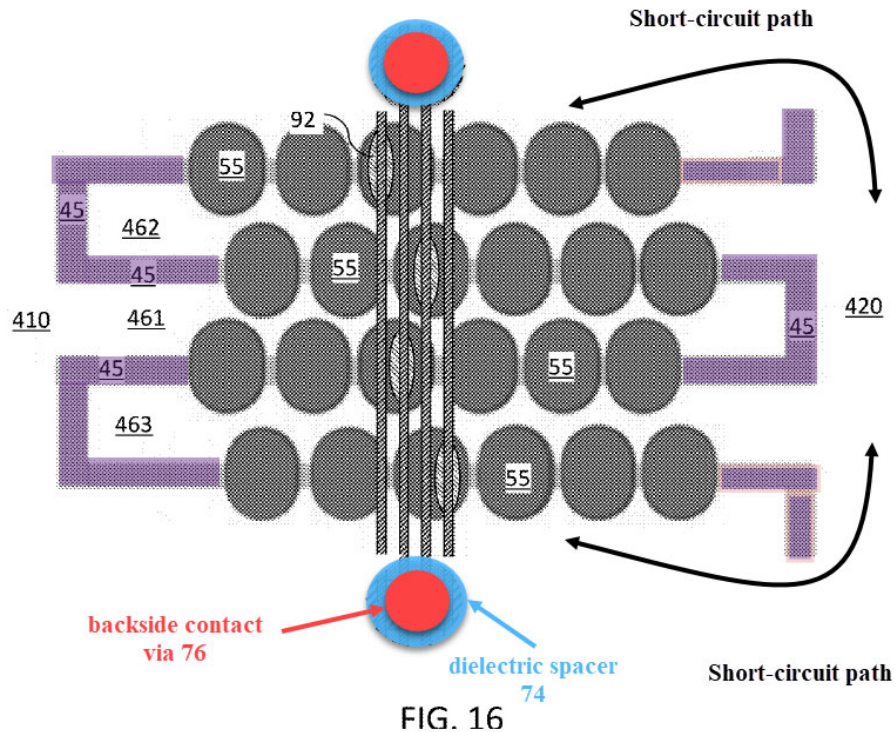
Nishikawa 15:25-30, Figs. 14, 16; Campbell2 ¶54. Without this isolation, as shown in Figure 14 below, the conductive path between the WLR/420 and the WLL/410 wordlines would cause incorrect reads and writes from every memory cell—meaning that Nishikawa’s device would not function to have dual memory cells at each level. Campbell2 ¶55.



Nishikawa Fig. 14 (annotated)

That is precisely what Petitioner's proposed modification would do. Campbell2 ¶¶56-58. Petitioner argues a POSITA would have been motivated to “modify the trench-shaped common source contact (74, 76)” to “remov[e] the trench structure” and “implement Nishikawa's TAC 76 as a circular TAC (including its spacer...)” Pet. 51, 78, 82, 98-99 (stating Ground 3 has “same claim mapping” as Ground 1); see Ex.1003 ¶180. That modification of Nishikawa's trench-shaped backside contact via structure 76/spacer lining 74 would cause a gap in the isolation between the circular backside contact via structure 76 and the separator dielectric structure 45, electrically connecting the conductive layers 46—*i.e.*, the two

wordlines 410/420 and their respective gate electrodes (e.g., 461/462) and memory regions at each level, as shown in a modified Figure 16 below. Campbell2 ¶56.



Nishikawa Fig. 16 (modified)

And Petitioner's modification eliminating the electrical isolation would defeat the purpose of Nishikawa's device—having dual memory cells with separate gate electrodes in each memory opening—because it would create a short circuit between the wordlines at every level. Nishikawa Abstract; Campbell2 ¶57. Indeed, as described above, Nishikawa discloses its backside contact via 76 and dielectric spacer 74 are formed through the conductive layer 46 forming the separated gate electrodes (e.g., 461, 462, 463)—as such, the space in the short-circuit path indicated above is the conductive material creating a conductive path between the wordlines

410/420. Campbell2 ¶57; *see* Pet. 39 (describing Nishikawa's TAC extending through conductor layers 46). And a voltage applied to one wordline (and thus the gate electrodes) would be applied to the other. Campbell2 ¶57; Nishikawa 16:13-47 (describing selectively applying voltage to each gate electrode in different wordlines).

Further, the Board understood Patent Owner to argue in its preliminary response "that dielectric structures 45, not conductive trench 76, perform the electric separation of word lines." ID 17. That is not Patent Owner's position. As stated above, both the trench-shaped backside contact via structure 76/dielectric spacer 74 and the separator dielectric structures 45 provide the necessary electrical isolation between the wordlines 410/420. *See* Nishikawa 15:31-32, Fig. 16; Campbell2 ¶58. Indeed, the dielectric spacer 74 surrounds all sides of the trench-shaped backside contact via structure 76, and the dielectric separator structures 45 terminate where they meet the dielectric spacer lining, as shown below in Nishikawa's Figure 16. Campbell2 ¶58. This is because the dielectric separator structures 45 "laterally separate the control gate electrodes 46," e.g., first gate electrode 461 and second gate electrode 462, as shown below. Nishikawa 17:14-23. Campbell2 ¶58.

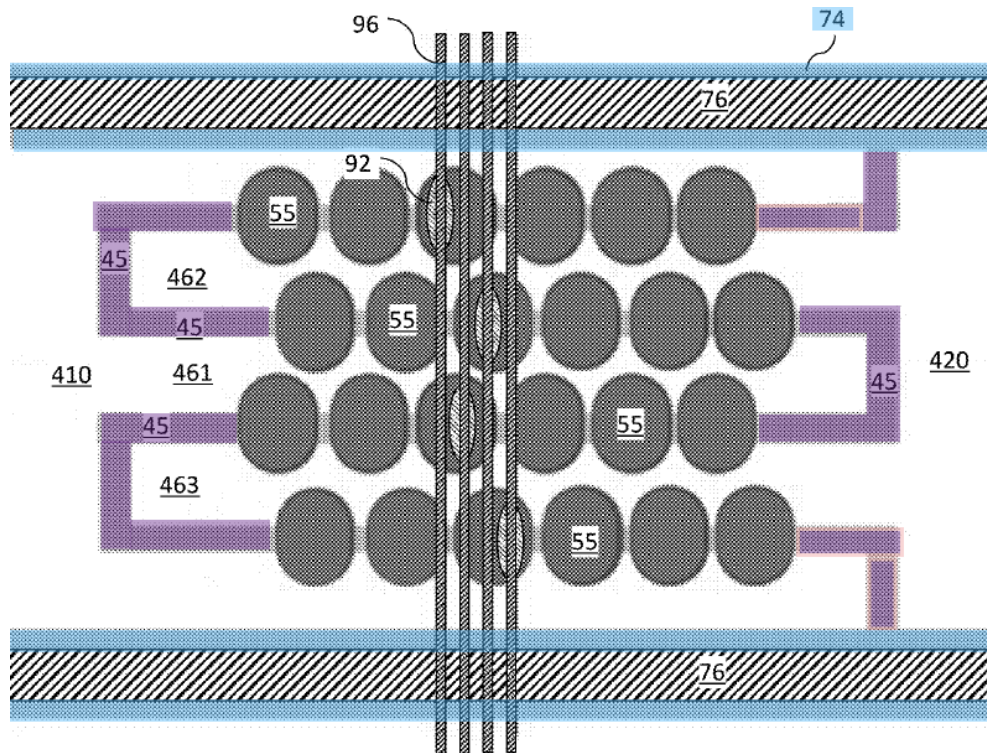


FIG. 16

Nishikawa Fig. 16 (annotated)

But in Petitioner's modification—which does not modify the separator dielectric structures 45—there is no longer the physical and electrical isolation provided by the separator dielectric structures 45 and the trench-shaped backside contact via 76/dielectric spacer 74 because they are not in contact with each other and do not separate the conductive layer the TAC extends through:

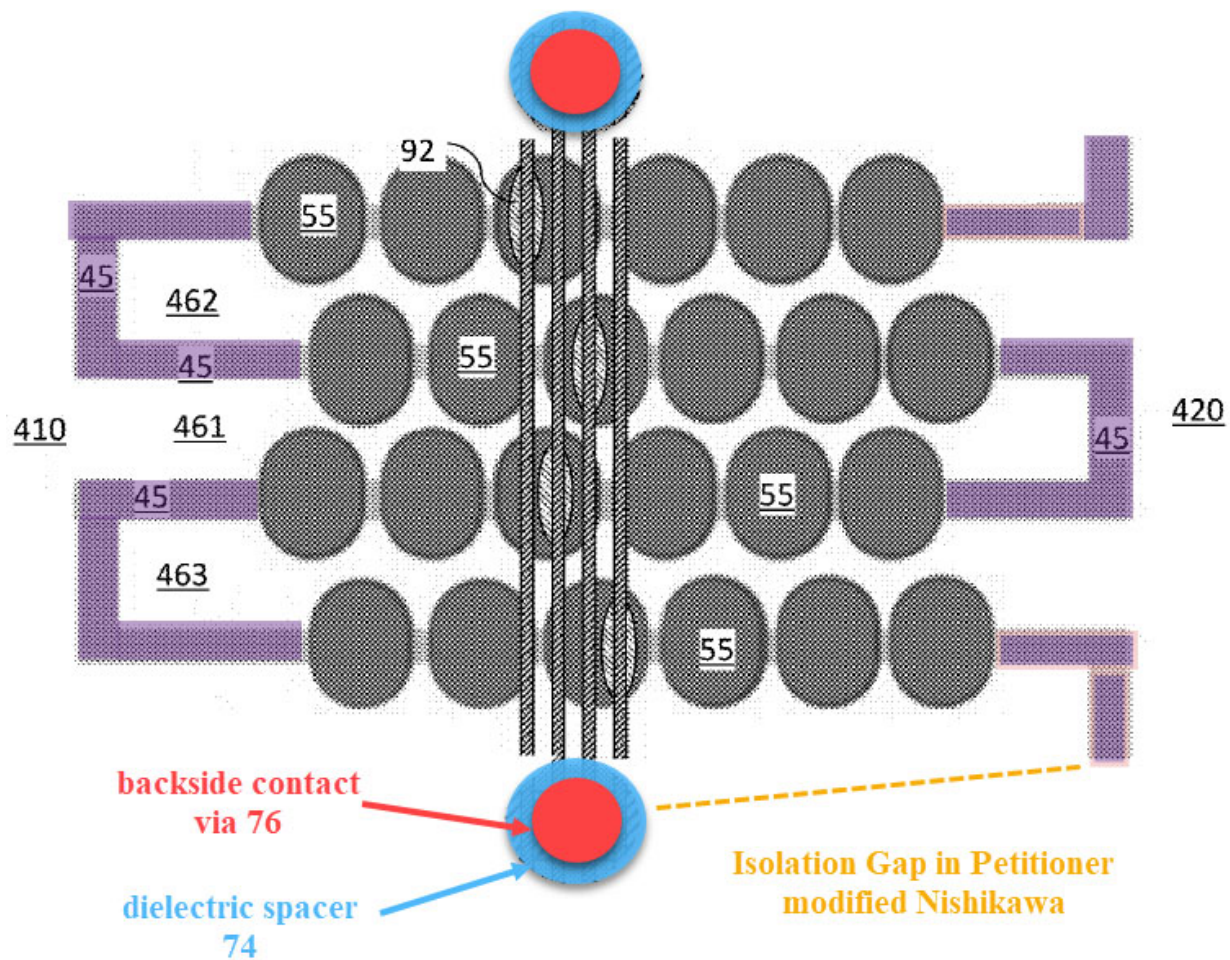


FIG. 16

Nishikawa Fig. 16 (annotated)

Campbell2 ¶¶56, 58. Thus, without modifying Nishikawa's separator dielectric structures 45—which is the case in Petitioner's proposal—Petitioner's modification would nullify the key purpose of Nishikawa's device and cause a short-circuiting problem in Nishikawa, dissuading a POSITA from making such a combination. Campbell2 ¶59; Nishikawa Abstract (“Control of the threshold voltage of such a vertical memory device can be enhanced because of the dielectric separator

dielectric structures.”); *see Medtronic*, 69 F.4th at 1349-50; *Fritch*, 972 F.2d at 1265 n.12.

If Petitioner were to assert its obviousness argument permits a circular TAC to be physically connected at the end of the separator dielectric structure 45 to cure isolation deficiencies (it did not), a POSITA would have recognized such a configuration is not suitable. Campbell2 ¶60. For example, a POSITA would have recognized that the TAC's diameter would have to be large enough to contact the side of the device to maintain the isolation, which would require a larger footprint than a rectangular trench, as shown below (red circle). *Id.*

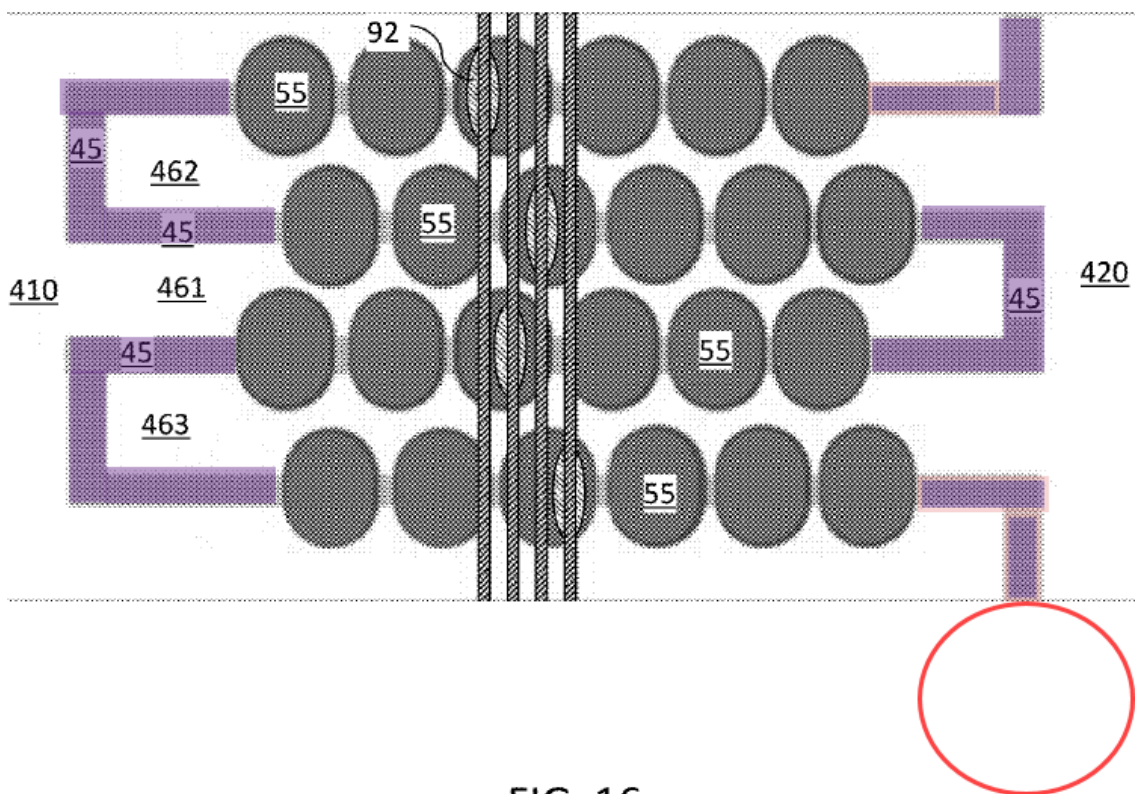


FIG. 16

Nishikawa Fig. 16 (modified)

Indeed, Petitioner admits a POSITA would not have desired an increased footprint. *See* Pet. 51, 99; Ex.1003 ¶123; Campbell2 ¶61. As another example, a POSITA would not have replaced Nishikawa's trench-shape structure with contiguous, physically connected circular TACs. Campbell2 ¶¶61-62. Doing so would push the limits of manufacturing tolerances leading to defects, such as short circuiting between densely-packed TACs and incomplete or deformed channel holes. *Id.* ¶61. And such densely packed TACs push the limits of physics because of parasitic capacitance, which would affect device performance. *Id.* ¶62.

Further, even if Petitioner argues (which it did not) a POSITA would have modified Nishikawa's trench structure so that it contains a circular contact via structure 76 and/or a dielectric spacer 74 surrounded by a trench-shaped dielectric material to preserve electrical isolation, that modification would fail because it would not meet the claims' requirement that the TAC "extend[s] vertically through the conductor/dielectric layer pairs in the memory stack."² '322 Patent cls. 8, 14, 19.

² The Petition does not propose these modifications, as described above. Pet. 51, 78, 82, 98-99; *see* Ex.1003 ¶180. Thus, Petitioner has waived such an argument. *Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1286 (Fed. Cir. 2017) (argument pointing to newly-raised modification of prior art reference "foreclosed by statute, our precedent, and Board guidelines").

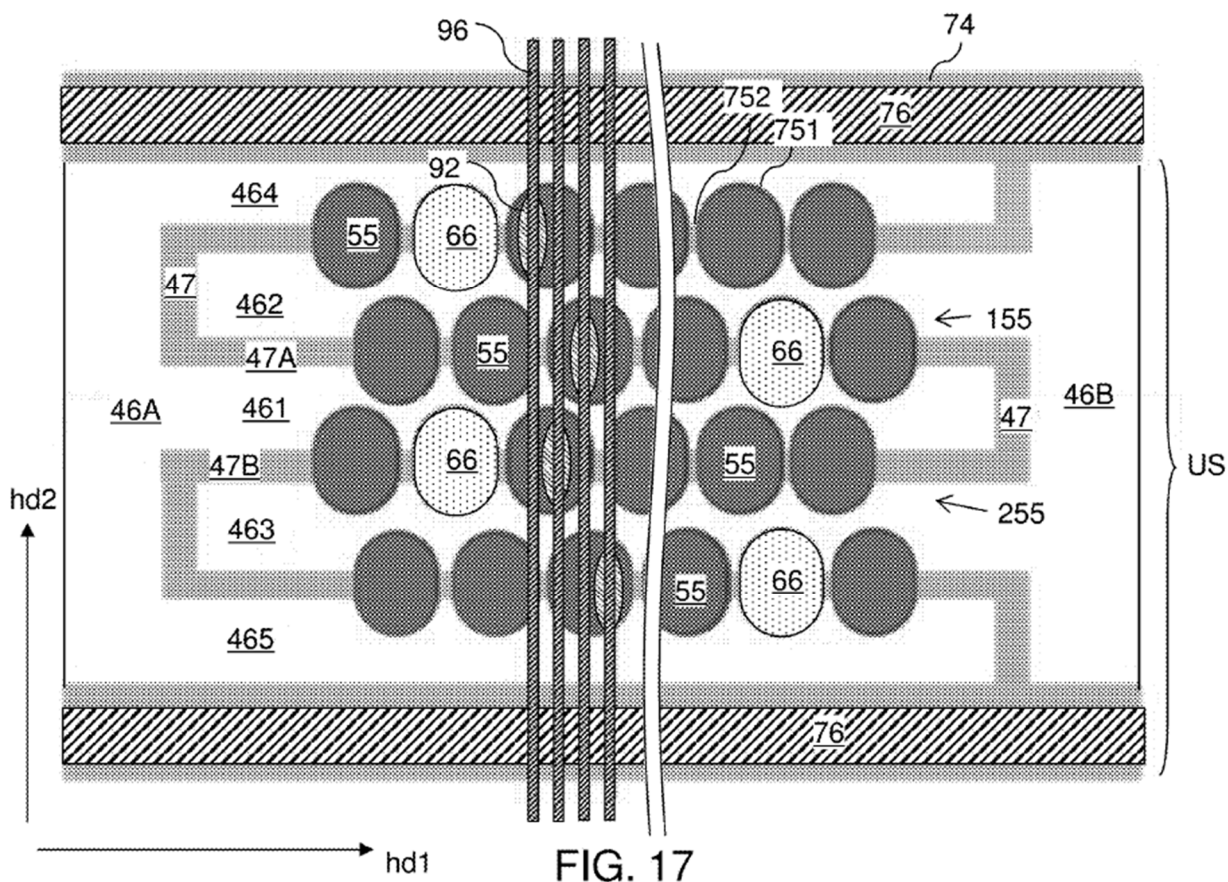
Rather, the TAC would extend through the dielectric material, not the memory stack as claimed. Campbell2 ¶63. Thus, a POSITA would not have been motivated to modify Nishikawa to have a circular TAC and would not have had a reasonable expectation of success in doing so. *Id.* ¶64.

2. A POSITA would not have been motivated to combine Nishikawa and Nishikawa123 or have had a reasonable expectation of successfully doing so.

In Ground 3, Petitioner argues a POSITA would have been motivated to combine Nishikawa and Nishikawa123 because they “present the same memory architecture and key components.” Pet. 99 (citing *id.* 27-32 (Description of Prior Art)). In describing these similarities, Petitioner argues that both Nishikawa and Nishikawa123 disclose TACs, and that Nishikawa123 teaches that the “openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape.” *Id.* 31-32 (citing Nishikawa123 22:38-41, Fig. 17; Nishikawa Fig. 16), 98-99. Petitioner further argues the architecture of Nishikawa123's Figure 17 and Nishikawa's Figure 16 are the “same.” *Id.* 31, 99.

Petitioner is wrong that a POSITA would have been motivated to apply Nishikawa123's teaching that an opening for forming a TAC could be circular to Nishikawa's device—that teaching does not apply to Nishikawa123's Figure 17 embodiment. Campbell2 ¶66; *see* Pet. 43, 98-99; Nishikawa123 22:34-41. Nishikawa123's teaching that the shape of an opening can be a “suitable shape, such

as circular” does *not* apply to Nishikawa123's Figure 17, which, like Nishikawa Figure 16, teaches separate, electrically isolated wordlines connected to separate gate electrodes forming dual memory cells at each level. Campbell2 ¶66. Indeed, Nishikawa123's embodiment in Figure 17 depicts a specific embodiment adding an optional first “comb shaped word line 46A” and a second “comb shaped word line 46B,” where each comb shaped wordline is connected control gate electrodes (e.g., 461/464 and 462/463), as shown below:



Nishikawa123 25:32-35, Fig. 17. For the reasons discussed above, these additional elements in Figure 17 require a trench-shaped opening 79 (and thus a backside

contact via structure 76 and dielectric spacer 74) or else the dual-cell configuration will not be able to function as intended. Campbell2 ¶66. Thus, a POSITA would have understood that Nishikawa123's disclosure that the opening 79 could be "any *suitable* shape," including a circular one, does not apply to Figure 17's embodiment for the reasons discussed above regarding Nishikawa. *Id.*

Moreover, Figure 17 teaches only a trench-shaped backside contact via contact 76/dielectric spacer 74. *Id.* ¶67. A POSITA would have understood Figure 17's embodiment may have the separated comb shaped wordlines 46A/B where the backside contact via contact 76 is trench-shaped and provides the necessary electrical isolation: "Each electrically conductive layer 46 (*i.e.*, each of the word-line-level electrically conductive layers 46) formed within the alternating stack (32, 46) includes two physically disjointed portions (46A, 46B) *between each optional neighboring pair of backside trenches (which are filled with the insulating spacers 74 and the backside contact structures 76).*" Nishikawa123 25:36-49; Campbell2 ¶67. Indeed, Petitioner compares Figure 17 to Nishikawa, both of which explicitly show *trench-shaped* backside contact vias 76 and electrically isolated wordlines at the same level provided by the trench-shaped structure disclosed in Nishikawa123. Pet. 31 (comparing Nishikawa, Fig. 16 and Nishikawa123 Fig. 17), 99; Campbell2 ¶67. In any event, Petitioner has failed to propose a single application of a circular TAC in either Nishikawa or Nishikawa123 that could preserve the isolation of the

dual-cell configuration. This failure of proof is fatal to Petitioner's proposed modification, which suffers from a lack of motivation to combine and a reasonable expectation of success. Campbell2 ¶¶64, 68.

Thus, Nishikawa123's teaching regarding the "suitable shape" for an opening that Petitioner relies on as disclosing a circular TAC would not have motivated a POSITA to modify Nishikawa to have a circular TAC and corresponding dielectric spacer, as Petitioner proposes. *Id.* ¶68.

3. Petitioner improperly relies on the common inventorship of Nishikawa and Nishikawa123.

Petitioner also incorrectly argues a POSITA would have combined Nishikawa and Nishikawa123 because they were filed by the "same inventor" "only 5 days apart" and have the same "architecture." Pet. 99. When viewing both in light of their full disclosures, a POSITA would have understood the inventor filed two patents for two distinct devices that could not be combined as Petitioner asserts. *See* Section III.A.2; Campbell2 ¶68.

Petitioner also improperly asserts that a POSITA would combine Nishikawa and Nishikawa123 because a POSITA "would have considered potential improvements in Nishikawa[123] [over Nishikawa] given that its provisional was filed 5 days later" and by the same inventor. Pet. 99. What matters, as the Board

recognized, is the “standpoint of one of ordinary skill in the art,” not “the perspective of the inventors of a particular reference.”³ ID 16.

4. Petitioner's other arguments fail.

Petitioner asserts a POSITA would have modified Nishikawa's trench-shaped backside contact via structure 76 to be a circular TAC because background references demonstrate that circular TACs were generally known to a POSITA and a “suitable option.” Pet. 43-50. Petitioner also asserts a circular TAC would increase “memory capacity.” *Id.* 99. But Petitioner misses the point: a POSITA would not have modified Nishikawa based on just any general disclosures by other references if doing so would defeat Nishikawa's stated purpose or render it inoperable, especially when the alleged benefits are marginal. *See* Section III.A.1; Campbell² ¶¶69; *Arctic Cat Inc. v. Polaris Indus., Inc.*, 795 F. App'x 827, 833 (Fed. Cir. 2019) (“The Board must weigh the benefits and drawbacks of the modification

³ Patent Owner agrees, and clarifies here, that it was not arguing that the obviousness analysis should only be looked at through the lens of the inventor as opposed to a POSITA. Rather, Patent Owner argues a POSITA would have understood Nishikawa and Nishikawa¹²³ are distinct devices with different requirements, components, and compatibilities. *See* Campbell² ¶¶65-68.

against each other, to determine whether there would be a motivation to combine.”); *Medtronic*, 69 F.4th at 1349-50; *Fritch*, 972 F.2d at 1265 n.12.

Thus, Petitioner did not meet its burden of proving Nishikawa and the knowledge of a POSITA, alone or with Nishikawa123, renders the circular TAC limitation obvious.

B. Petitioner improperly supplies missing limitations by relying on additional background references and invoking a POSITA's knowledge.

1. Petitioner's use of a POSITA's general knowledge and background references is impermissible under statute, regulation, and obviousness law.

Faced with Nishikawa's deficient disclosures, Petitioner improperly relies on a POSITA's knowledge to supplement the missing circular TAC limitation. *See, e.g.*, Pet. 59-60. But Petitioner's grounds are based on Nishikawa and knowledge of a POSITA and fail to satisfy 35 U.S.C. § 311(b), which requires *inter partes* review be requested “only on the basis of prior art consisting of patents or printed publications.” *See Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1373-75 (Fed. Cir. 2022) (stating that the “basis of a ground” must be “contained in a document that is a prior art patent or prior art printed publication”). Petitioner's grounds similarly fail under the then-Acting Director's clarification of 37 C.F.R. § 42.104(b)(4)'s requirement to “specify where each element of the claim is found *in the prior art patents or printed publications relied upon.*” Reference to a POSITA's general

knowledge does not meet this standard, according to that clarification of § 42.104(b)(4), and Petitioner is not entitled to rely on it to supply missing limitations.⁴

Even in the context of invalidity broadly, Petitioners can invoke a POSITA's knowledge to supply a missing limitation *only* if the record establishes the missing limitation is “*unusually simple*” and the “technology particularly *straightforward*.” *DSS Tech.*, 885 F.3d at 1374; *Motorola Mobility LLC v. Largan Precision Co.*,

⁴ Then Acting Director of the USPTO issued a memorandum effective for petitions filed in September 2025 clarifying as much, explaining that “enforcement of Rule 104(b)(4) means that applicant admitted prior art (AAPA), expert testimony, common sense, and other evidence that is not ‘prior art consisting of patents or printed publications’ (collectively ‘general knowledge’) may not be used to supply a missing claim limitation.” See USPTO Memorandum, Enforcement and Non-Waiver of 37 C.F.R. § 42.104(b)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews at 1 (July 31, 2025). While this Petition was filed before September 1, 2025, the Board should reject Petitioner's effort to use “common knowledge” to fill in missing claim limitations here because, as the Director stated, “enforcement of Rule 104(b)(4) means that ... ‘general knowledge’ may not be used to supply a missing claim limitation.” *Id.*

IPR2024-00688, Paper 7 at 29 (Oct. 28, 2024) (finding that a recited etching process for a light blocking sheet was not “unusually simple” nor the technology “particularly straightforward”). “Failure to prove the matter *as required by the applicable standard* means that the party with the burden of persuasion,” *i.e.*, Petitioner “loses.” *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378-79 (Fed. Cir. 2015); *Motorola Mobility, LLC v. Int’l Trade Comm’n*, 737 F.3d 1345, 1350 (Fed. Cir. 2013) (“At all times, the burden of persuasion rests on the party challenging the patent.”). Thus, the burden of showing a limitation is unusually simple and the technology straightforward falls on *Petitioner*.

Here, Petitioner provides no argument that the substantially circular TAC limitation (or any limitation) it supplies based on a POSITA’s general knowledge⁵

⁵ To the extent Petitioner argues that it relied on background references such as Nishikawa and pieces of other prior art references (*e.g.*, Nakajima (Ex.1009) (Pet. 43-50)), such an argument is equally improper. Petitioner is not entitled to make an end-run around establishing a motivation to combine and reasonable expectation of success for these references by not including them in the relevant ground, but still using them to supply a missing limitation. If Petitioner intended to rely on these other references to supply a missing limitation, it was required to make them part of

is unusually simple or that 3D NAND technology is particularly straightforward. *See* Pet. 59-64. Further, that a POSITA would be “generally knowledgeable about 3D NAND’s structure [and] how it is manufactured” is of no moment. *See* ID 8. If it were, a Petitioner could supply any missing limitation so long as a POSITA was “generally knowledgeable” about it. That is not the test. A missing limitation can be supplied by a POSITA’s knowledge only when the missing limitation is “unusually simple” **and** the technology is “particularly straightforward.” *See DSS Tech.*, 885 F.3d at 1373-74 (rejecting Board’s reliance on “common knowledge” to “supply a missing claim limitation” because wireless communications are not “particularly straightforward” technology). Therefore, all four grounds fail on that basis alone.

a. 3D NAND technology is complex.

Highly technical electronic inventions, such as the 3D NAND devices of the ’322 Patent, are not “particularly straightforward.”⁶ *See id.*; Pet. 14-20; ’322 Patent 4:58-5:22 (describing features of the device, its design benefits, and fabrication

the applicable obviousness combination and conduct the proper analysis. It failed to do so here.

⁶ Even though whether the limitation is “unusually simple” may be different for each limitation, the “technology” applicable to all grounds is 3D NAND and applies to all limitations. *Campbell* 2 ¶72.

complexities associated with 3D NAND); Campbell2 ¶70. Instead, 3D NAND is “**very complex**” and includes “complex device structures” linked with the equally complex fabrication processes required to produce such devices. *Id.* (citing, e.g., Ex.2023 4; Ex.2024 5; Ex.1010 212); Ex.1010 293; Ex.2023 3; *see* ’322 Patent 5:2-5 (describing the link between device design and manufacturing difficulties); Ex.2038 22:18-24:14 (agreeing “fabrication processes” and “design” are constraints on “memory density”).

Forming 3D NAND structures “involve[] a number of new and **complex process steps**.” Campbell2 ¶71 (citing e.g., Ex.2028 2-3, 8; Ex.2029 5); Ex.2025 4; Ex.2026 8; *see* Ex.2023 4-5 (recognizing “[a]n incredible level of precision and repetition is required in defining complex 3D structures with extremely high aspect ratio (HAR) features”), Fig. 1; Ex.2027 1 (stating 3D NAND “channels” have “unique process control requirements” because of “angstrom-level precision requirements”). Thus, 3D NAND structures involve concepts of chemical, mechanical, and electrical engineering on a microscopic scale and is not “particularly straightforward” technology. Campbell2 ¶72.

As every ground relies on the knowledge of a POSITA to supply missing limitations in the not particularly straightforward 3D NAND technology, the Petition fails to prove any claim at issue is invalid.

b. The recited “substantially circular” TAC is not “unusually simple.”

Forming a 3D NAND device to include a substantially circular TAC—including changing the shape of a TAC—is complex, not unusually simple. *Id.* ¶¶73-76. The lithography process for forming holes requires creating a mask. *Id.* ¶73. To change the shape of a feature, a POSITA must redesign the etching mask. *Id.* But changing the mask to create circular features (*i.e.*, change the shape of the TAC) requires time consuming, specialized processes, which are complicated when forming circular as opposed to angular features. *Id.*

Besides the mask-making process, making a circular TAC, which is a higher aspect ratio than Nishikawa's trench-shaped TAC, is complex because it is harder to maintain a continuous etch rate. *Id.* ¶74. In Petitioner's proposed modifications, unwanted variations can occur, such as bowing or twisting within the TAC, an incomplete etch, or variation between the top and bottom of the TAC. *Id.*

Further, it is increasingly complex to achieve consistent etch profiles at the top and bottom of the holes in a memory array as the height of 3D NAND increases. *Id.* ¶75. And the choice of material for both the target and non-target layers must be highly compatible with the selective etch chemistry because any incompatibility could lead to non-uniform etching, structural defects, or failure to form the intended structure. *Id.* These issues demonstrate the complexity of creating TACs of the claimed geometry. *Id.* ¶¶73-75.

In addition, as Petitioner's expert Dr. Lee admitted, changing the shape of the TAC openings—which would increase the aspect ratio of the TAC—would introduce higher risks of undesirable tapering in the channel hole that can lead to inconsistent channel depth and defective TACs causing short circuits. *Id.* ¶76; Ex.2038 25:9-17, 29:17-30:1, 30:13-31:3. Forming a circular TAC as opposed to non-circular shape *does* increase the complexity compared to the “same structure, but in a different shape.” *See* ID 15; Campbell2 ¶76. Thus, forming and designing TACs with a substantially circular section is not “unusually simple.” Campbell2 ¶76.

IV. Nishikawa and a POSITA's knowledge, alone or with Nishikawa¹²³, do not render obvious a “dummy channel structure ... extending vertically through the conductor/dielectric layer pairs in the memory stack” (claims 3, 6, 14-18, 20).

Claim 3 recites “a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack.” '322 Patent cl. 3. Claims 6 and 14 recite the same limitation. *Id.* cls. 6, 14. Claims 15-18 and 20 depend from claim 14. *Id.* cls. 15-18, 20.

As the Board correctly stated, neither Petitioner nor its expert asserts that Nishikawa discloses a dummy channel structure. ID 18; Pet. 59, 82; Campbell2 ¶¶78-79; Ex.1003 ¶140 (stating “[a] POSITA would have been motivated ... *to include dummy channels*”). Instead, for Grounds 1 and 3, Petitioner relies entirely on the “knowledge of a POSITA” to supply the missing dummy channel limitation, arguing “a POSITA would have been motivated, with a reasonable expectation of

success, to include dummy channels ... in Nishikawa's memory stack.”⁷ Pet. 59; Campbell2 ¶80. Petitioner's modification of Nishikawa fails for both grounds. Campbell2 ¶81.

A. A POSITA would not have been motivated or have had a reasonable expectation of success to add dummy channels to Nishikawa's memory stack.

Petitioner asserts it would have been obvious to “include dummy channels ... in Nishikawa's memory stack” for “structural support” and “processing reasons.” Pet. 59-60. But, as the Board correctly found, the “record does not support Petitioner's reason to combine dummy channels as known in the art with the teachings of Nishikawa” for either reason. ID 20; *see* Campbell2 ¶¶78, 81.

1. Nishikawa's separator dielectric structures already provide structural support, rendering dummy channels redundant.

Petitioner asserts that a POSITA would have been motivated to add dummy channels to Nishikawa to provide structural support during “the gate replacement process.” Pet. 60; Campbell2 ¶82. But Nishikawa *already* provides structural support for its gate replacement process. *Cf.* Pet. 63 (identifying as an alleged motivation “support during the gate replacement process”); Campbell2 ¶¶82-83.

⁷As the Board recognized, Petitioner does not rely on Nishikawa¹²³ for teaching dummy channels. ID 18, n.7; *see* Pet. 98. Thus, Petitioner's arguments for Grounds 1 and 3 fall together.

Nishikawa's memory stack includes "separator dielectric structures 45" that "provide *structural* support to the insulating layers 32 after formation of the interlayer cavities 43," *i.e.*, gate replacement. Nishikawa 10:10-12; Campbell2 ¶83. As the Board recognized, Petitioner failed to "address the support provided by" Nishikawa's separator dielectric structures. ID 19-20. POSITAs would have understood there was no reason to add dummy channels to perform a function already accomplished by Nishikawa's existing structures. Campbell2 ¶¶82-83, 88.

Indeed, adding dummy channels to Nishikawa would provide no additional structural support benefit. *Id.* ¶¶83, 88. The "gate replacement" process in Nishikawa involves removing the "sacrificial material layers 42" and creating the interlayer cavities (*i.e.*, "recess 43") prior to filling the interlayer cavities with metal conductor layers (*i.e.*, gates). *Id.* ¶84. As shown below in Figures 6B (before gate replacement) and 7B (during gate replacement), Nishikawa teaches forming its recess 43 (yellow) created in the space where the "sacrificial material layers 42" (green) were prior to removal.

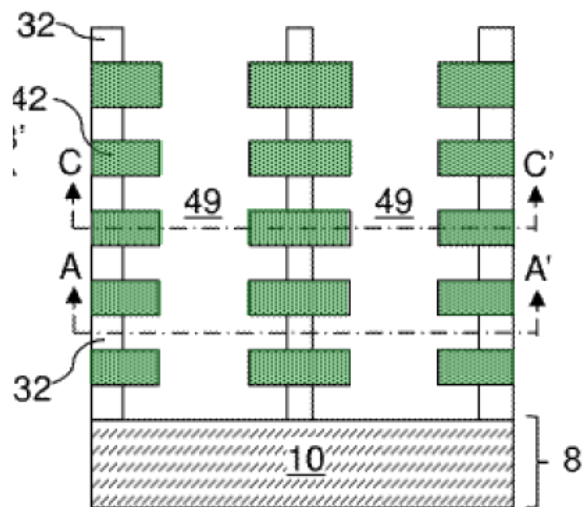


FIG. 6B

Before Gate Replacement

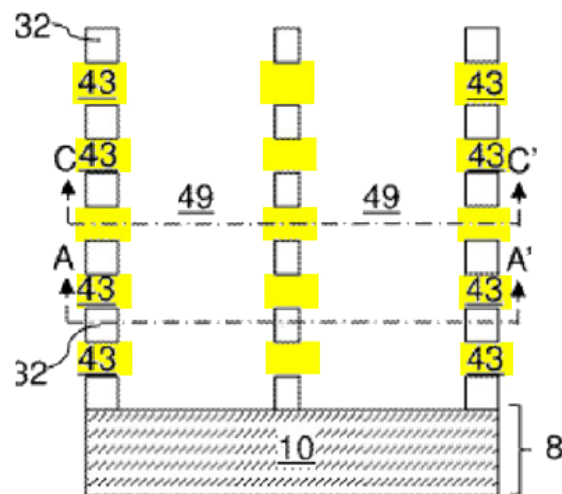
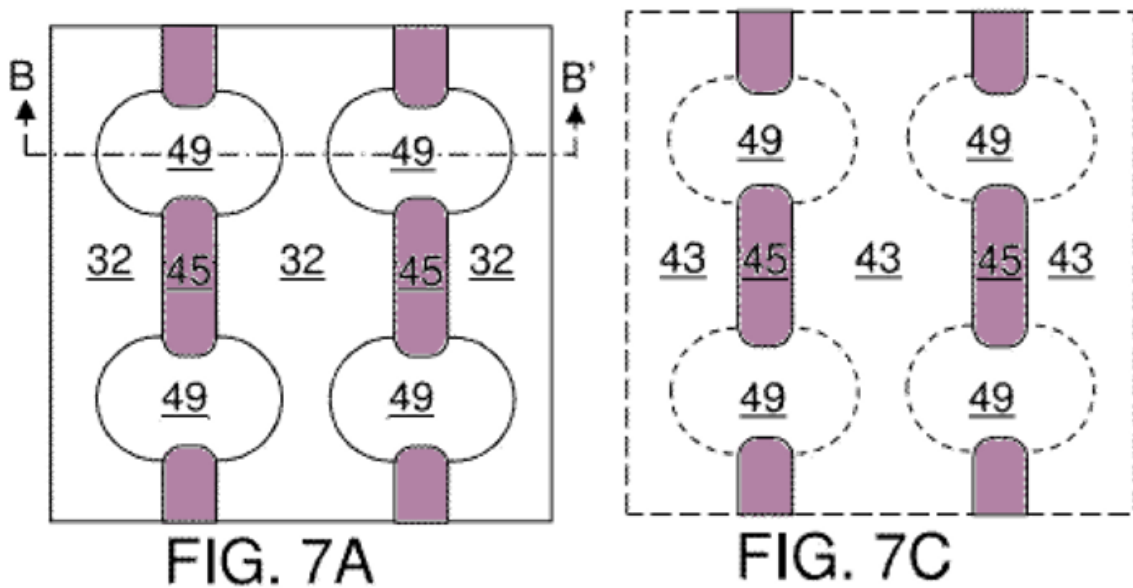


FIG. 7B

During Gate Replacement

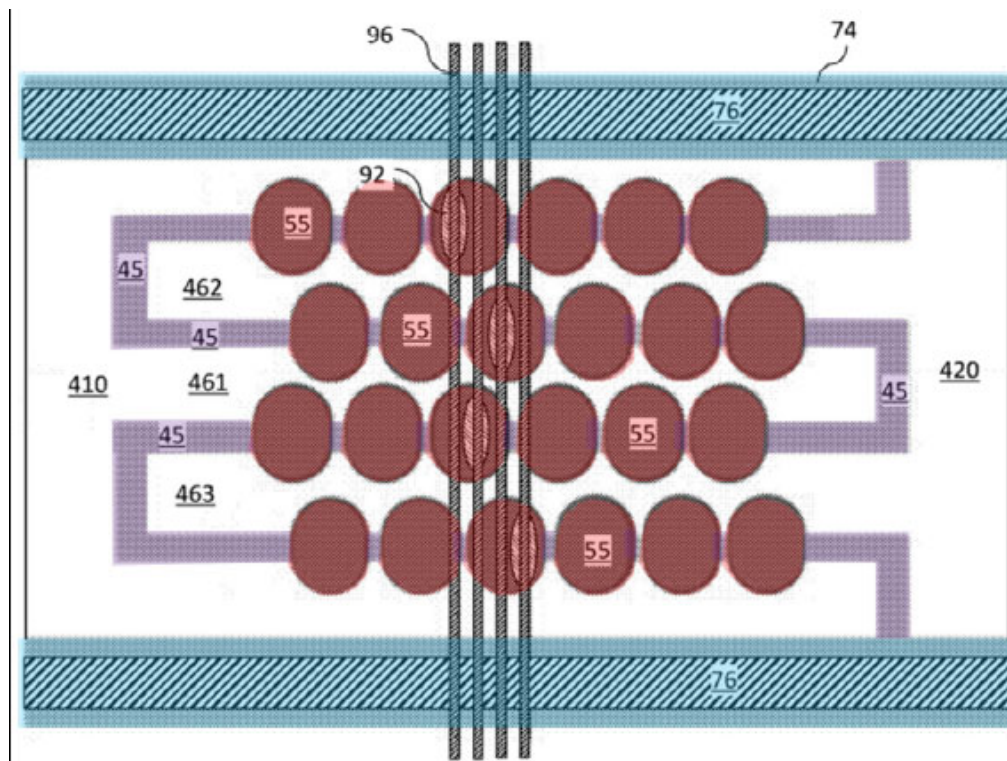
Id. ¶¶84-85; Nishikawa 10:8-10, Figs. 6B, 7B (annotated).

Figures 7A and 7C below—which are top-views of the device shown above in Figures 6B and 7B—show the separator dielectric structures 45 (purple) “provid[ing] *structural* support to the insulating layers 32 after formation of the interlayer cavities 43,” preventing the insulating layers 32 from collapsing into the recesses and not forming a functioning device. Nishikawa 10:10-12; Campbell2 ¶¶85-86.



Nishikawa Figs. 7A, 7C (annotated)

Nishikawa also discloses the separator dielectric structures 45 are disposed *throughout* Nishikawa's memory stack and therefore provide structural support to the device during the gate replacement process, as shown below in annotated Figure 16. *Id.* ¶87.



Id.; Nishikawa Fig. 16 (annotated), 17:14-18 (“The separator dielectric structures 45 [purple] extend through the stack.”).

Petitioner’s remaining support-related arguments also fail. Petitioner argues that dummy channels are suitable and “do not require connections to the upper-level devices, thereby not consuming space above the structures while also serving as support structures.” Pet. 63. Those arguments simply restate that dummy channels add structural support—support that a POSITA would recognize Nishikawa already

provides.⁸ *See* ID 20 (noting Petitioner's argument is "premised on providing additional support"); Campbell2 ¶¶89. Nor is there evidence that dummy channels would be necessary or helpful to Nishikawa's device already containing support structures. Petitioner does not argue that Nishikawa's existing support structures inadequately provide such support. *See* Pet. 59-64. To the contrary, a POSITA would have understood that such dummy channels were redundant and unnecessary. Campbell2 ¶¶88-89; *see S.-Tek Sys., LLC v. Engineered Corrosion Sols., LLC*, 748 F. App'x 1003, 1007 (Fed. Cir. 2018) (affirming finding that a POSITA would not be motivated to add a "drain" to a reference where it already taught a "drum drip that serves [the same] purpose" and would be "redundant").

2. Adding dummy channels does not have processing benefits.

Petitioner also asserts that a POSITA would have been motivated to add dummy channels for "processing reasons." Pet. 59. None of Petitioner's processing-related arguments would have motivated a POSITA to add dummy channel structures to Nishikawa. Campbell2 ¶¶90-97.

⁸ Even if the channels are not consuming space above the structures, they would consume space in Nishikawa's memory stack, reducing memory density. Campbell2 ¶¶83, 100-103; *see* Section IV.A.3.

First, Petitioner argues a POSITA would have been motivated to add dummy channels in Nishikawa's memory stack to "reduce the likelihood of defective bits on the edge of the memory cell region, because the additional rows of dummy channel structures extend the memory cell pattern to include the dummy region on the edges." Pet. 59.

But Petitioner fails to show that Nishikawa's device would suffer from a "likelihood of defective bits on the edge of the memory cell region." *Id.* 59-60; Campbell2 ¶92. Indeed, the references Dr. Lee identifies do not show that "edge of the array" issues are a concern in 3D NAND generally or that adding dummy channels would resolve such concerns, let alone address any concerns with Nishikawa. Campbell2 ¶92; *see, e.g.*, Ex.1024 8:47-53 (referring to a "typical flash cell array" in 1998, not 3D NAND); Ex.1025 2:20-43 (indicating edge of array issues "**may** typically occur at the boundary ... an abnormal edge pattern at the edge of array **may** be controlled by adding a dummy pattern region"). And although Dr. Lee attests that "it is common to refrain from using the cells at the array edge," which are "sometimes referred to as dummy cells," due to "processing variations" (Ex.1003 ¶141 (quoting Ex.1024 8:47-53)), this does not show an advantage to **adding** dummy channels that would have motivated a POSITA to add them to Nishikawa, especially where Nishikawa already has structural support. Campbell2 ¶92.

Regardless, the Board correctly noted that Dr. Lee recognizes that any dummy regions existing at the edge of the array would be “later sacrificed in processing.” *Id.* ¶93; Ex.1003 ¶141 (quoting Ex.1025 2:20-43); ID 19. To the extent Petitioner argues dummy channels would be formed at the edge of the memory cell, Pet. 60, a POSITA would not have added a “dummy channel structure” simply to have it later sacrificed during processing. ’322 Patent cl. 3; Campbell2 ¶93; *see* ID 19. And dummy structures added but later sacrificed in processing would not meet the claim limitation nor would they provide any additional support. Pet. 63 (citing, *e.g.*, Kai (Ex.1027) Fig. 6A); ID 19; Campbell2 ¶93.

Further, Petitioner cites nothing in Kai, Kim, Park297, or anything else that teaches “additional rows of dummy channel structures” that “extend the memory cell pattern.” Pet. 59. To the contrary, as discussed below, those references do not disclose dummy structures in the memory cell area at all. *See* Section IV.B; Campbell2 ¶94. In fact, Kim and Park297 disclose that the dummy channels ***should not*** be within the memory cell array. Kim (Ex.1029) [0047]; Park297 (Ex.1028) Fig. 1, 7:38-42; Campbell2 ¶94; *see* Pet. 62 (citing Park297 7:45-51 as disclosing dummy channels). Petitioner also ignores that adding “additional rows” in the “memory cell pattern” will increase device size and reduce memory density, which a POSITA would understand is not desirable. Campbell2 ¶94; *see* Section IV.A.3.

Second, Petitioner argues “adding dummy structures would result in an overall more uniform feature pattern, which reduces processing issues.” Pet. 60. But Petitioner fails to show that Nishikawa’s structure would not be uniform or that such a “uniform feature pattern” was well known in the art such that it would be implemented in Nishikawa. *Id.*; Campbell2 ¶95; see *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (Petitioner bears “the burden from the onset to show with particularity why the patent it challenges is unpatentable.”).

Indeed, Dr. Lee relies only on Ronse (Ex.1026), which was published prior to the invention of 3D NAND. Campbell2 ¶96. And the “technique” Dr. Lee cites in Ronse to support his conclusion that adding dummy channels creates uniform feature patterns discusses “[q]uadrupole illumination,” which is irrelevant to the benefits of adding dummy channels.⁹ *Id.*; see Ex.1003 ¶142 (citing Ronse 11). But even if it was

⁹ Petitioner asserted Ronse in support of a similar argument in *Micron Tech., Inc. v. YMTC*, IPR2025-00034 for the related U.S. Patent No. 10,879,254 (“’254 Patent”). Paper 1 at 41 (Oct. 11, 2024). The Board correctly noted there that Ronse merely “discusses advantages of quadrupole illumination for photolithography, lacks an explanation of its connection to the [dummy] channels ..., and therefore does not meaningfully support Petitioner’s obviousness assertion.” *Id.* Paper 19 at 18 n.9 (May 16, 2025).

relevant, it does not describe how adding dummy channels would improve Nishikawa. Campbell2 ¶96.

Further, Petitioner does not explain where or how dummy channels would be placed “in the memory stack,” including to extend the memory cell pattern in such a manner as to “result in an overall more uniform feature pattern,” Pet. 59-60, which is particularly problematic because there is no room in Nishikawa’s device to add redundant dummy structures to space already occupied by memory cells (55), electrical connection (66, 410, 420, 76), and structural support (45). Campbell2 ¶97. Thus, a POSITA would not have been motivated to add dummy channels through Nishikawa’s stack nor would have had a reasonable expectation of success. Further, as described below, expanding the size of the stack to accommodate dummy channels or replacing active channels with dummy channels would introduce density, performance, and cost disadvantages with no benefit. *Id.* ¶¶99-107; *See* Section IV.A.3; Ex.1003 ¶141.

At bottom, Petitioner’s argument to include “dummy channels” in Nishikawa’s device is nothing more than hindsight reconstruction of the claimed invention. *In re Entresto*, 125 F.4th 1090, 1100 (Fed. Cir. 2025) (affirming claims as non-obviousness because there was no motivation to combine the separate elements and challenger “impermissibly use[d] [the claimed combination] as a starting point and ‘retrace[d] the path of the inventor with hindsight’”).

Third, Petitioner's remaining processing-related argument also fails. Petitioner's assertion that dummy channels "can be made by the same process and at the same time as the active channels" does not suggest that a POSITA would have been motivated to do so. *See* Pet. 63; Campbell2 ¶98. Nishikawa already discloses that its separator dielectric structures 45 provide structural support for the memory array during the gate replacement process. *See* Section IV.A.1. Petitioner does not—and cannot—argue that those separator dielectric structures 45 do not serve that purpose. *See id.*

3. Petitioner's proposed modification of Nishikawa would introduce performance, cost, and processing disadvantages to Nishikawa's device.

The Board correctly recognized that Petitioner had not explained why any additional support provided by dummy structures would have been necessary, particularly "in view of any tradeoffs with additional processing needed to create additional dummy channels," nor why such tradeoffs "would be viewed as desirable" by a POSITA. ID 20; *see Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (Fed. Cir. 2000) ("Instead, the benefits, both lost and gained, should be weighed against one another."). In fact, POSITAs would be dissuaded from adding dummy channels because doing so would introduce significant device performance, cost, and processing disadvantages without offering any advantages. Campbell2 ¶99; Kim [0003] ("Semiconductor devices have been highly integrated for satisfying high

performance and low manufacture costs which are desired by users.”); *see Arctic Cat*, 795 F. App'x at 833.

First, adding dummy channels would reduce Nishikawa's memory storage capacity, negatively impacting device performance. Campbell2 ¶100. To add a dummy channel structure through Nishikawa's stack, Pet. 59, a POSITA would have to either (1) increase the size of stack to create space for a dummy structure or (2) decrease Nishikawa's storage capacity by replacing functional “memory stack structures 55” (which serve as channels for the memory cells (Nishikawa 4:28-32)) or “contact via structures 66” (which provide external access to the wordlines (*id.* 6:45-47)) with non-functional dummy channels.¹⁰ Campbell2 ¶100; *see* Section IV.B.2 (arguing there is no room in Nishikawa's memory stack). Either way, adding inactive dummy channels in Nishikawa's memory stack reduces the space available for active memory units and/or increases the array size without adding memory capacity, reducing Nishikawa's memory density. Pet. 59-60 (noting a technique for

¹⁰ Petitioner asserts in its petition challenging the related '254 Patent that “it would have been obvious to implement some of [the prior art reference]'s channels as dummy channels.” *Micron Tech.*, IPR2025-00034, Paper 1 at 39. Here, Petitioner does not propose modifying any existing structures to be “dummy channels” and instead asserts only that a POSITA would “include dummy channels.” Pet. 59.

adding dummy channels includes “expanding the channel structure region”); Campbell2 ¶101.

POSITAs would have understood that a 3D NAND chip with a higher memory integration density, *i.e.*, without dummy channels, could store more data in the same physical space compared to a chip with lower memory integration density. Campbell2 ¶102; *see* Kim [0003] (“Semiconductor devices have been highly integrated for satisfying high performance and low manufacture costs which are desired by users.”). Even Petitioner’s expert admitted here and in an *inter partes* review for the related ’254 Patent that “[memory] density is ***one of the most important aspect[s] in designing memory***,” and that “we always want to have as high density as possible; for lower cost, higher yield, and ... a lot more money per chip.” Ex.2022 44:8-11, 48:1-6; *see* Ex.1003 ¶165 (“The driving force in manufacturing memory is to create as dense as an array as possible ... memory capacity is obvious[ly] a key element of a memory.”), ¶205 (“[M]emory designs typically attempt to achieve a very dense memory array”). Adding dummy channels to Nishikawa’s memory stack reduces the space available for active channels (*i.e.*, memory) and would be antithetical to “achiev[ing] higher density,” which is “one of the goal[s] of designing 3D NAND” and “designing a memory chip.” Ex.2022 48:10-17, 49:8-14; Campbell2 ¶103.

Thus, a POSITA would not have been motivated to reduce memory density, and therefore would not have added dummy channels to the memory stack of Nishikawa. Campbell2 ¶103 (citing Ex.2030 3, Ex.2029 5).

Second, POSITAs would have also recognized that decreasing memory density would make the memory less cost effective, as Dr. Lee admitted. Ex.1003 ¶165 (“As density increases, the memory design becomes more cost effective”); Kim [0003] (“Semiconductor devices have been highly integrated for satisfying high performance and low manufacture costs which are desired by users.”); Campbell2 ¶104. Dr. Lee further admitted that the less dense the memory array, the more silicon is needed to create a given memory size, reducing cost effectiveness. Ex.2022 48:18-49:2; Ex.1003 ¶165 (“[T]he denser the array, the less silicon is necessary to create a given memory size. *As density increases, the memory design becomes more cost effective.*”); Campbell2 ¶104. POSITAs would not have been motivated to decrease memory density, thereby increasing cost. Campbell2 ¶104.

Third, POSITAs would have also recognized adding dummy channels would have introduced processing risks. Specifically, in striving to increase memory density, POSITAs would have recognized that forming “the dense array via high-aspect ratios” is “difficult” and can lead to “taper[ing],” where the sidewalls in a channel narrow toward the bottom of the channel. *Id.* ¶105; Pet. 84-85, 88; Ex.1003

¶¶205, 212; Ex.2038 25:9-17.¹¹ Petitioner's expert admitted tapering is “undesirable,” and POSITAs would have recognized tapering can lead to channels that do not penetrate all layers in a stack because the etch-rate will slow as the channel tapers. Campbell2 ¶105. A POSITA would have recognized that adding dummy channel structures to an already-dense memory array adds *more* processing risks to the formation of channels, without any additional benefits as discussed above. *Id.* ¶106.

Thus, a POSITA would not have been motivated to modify Nishikawa to introduce these disadvantages for the sake of introducing redundant dummy channel structures. *Id.* ¶107. Petitioner also fails to show a POSITA would have had a reasonable expectation of success in adding dummy channels to Nishikawa. *Id.* ¶106.

B. Petitioner's cited references do not render obvious adding dummy channels “in the memory stack.”

Petitioner relies on five references to purportedly “confirm[] the knowledge of a POSITA” that it was “well known to include dummy channel structures to

¹¹ Petitioner's Ground 4—which argues a POSITA would have been motivated to combine Lu's multideck memory stack with Nishikawa's device because “driving motivation for multi-deck structures is the difficulty in etching high aspect ratio channel holes,” Pet. 84—undermines any expectation of success in adding dummy channels by the same process. Campbell2 ¶106.

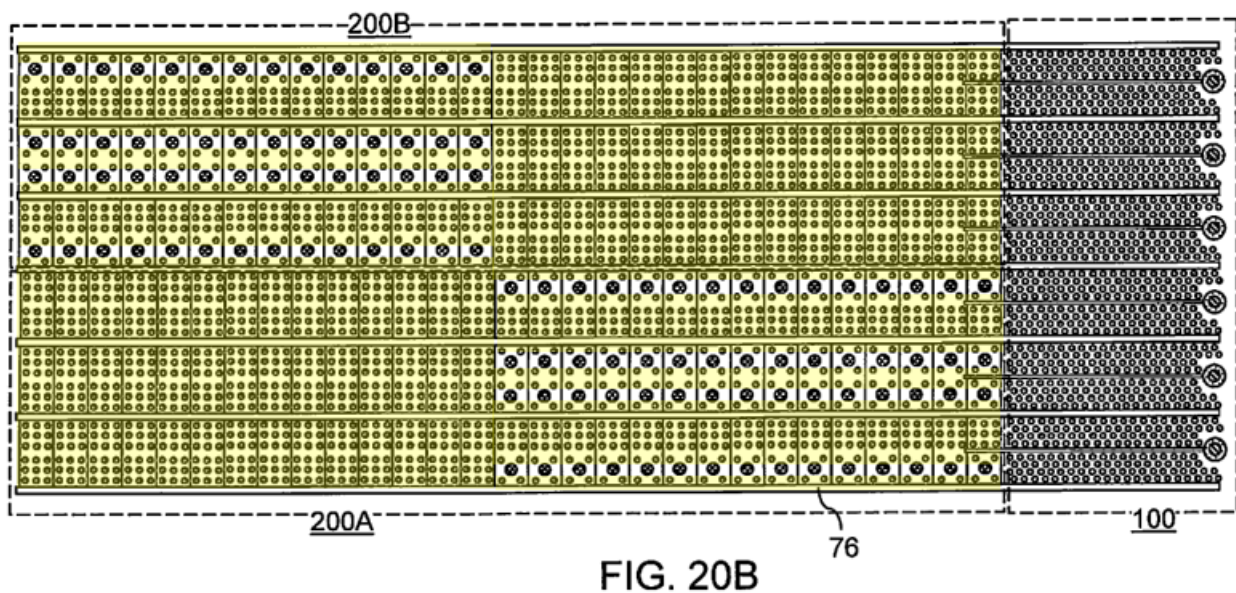
provide structural support”: Nishikawa123, Masamori, Kai, Park297, and Kim. Pet. 60, 62. But just because dummy channels were purportedly “well known” does not mean a POSITA “would have been motivated to make the combinations or modifications” of adding a dummy channel structure to Nishikawa—especially when Nishikawa already has other structures that provide structural support. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”); *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993-94 (Fed. Cir. 2017).

Regardless, those references do disclose dummy structures with structural differences compared to Nishikawa that would not have motivated a POSITA to modify Nishikawa. Campbell2 ¶¶108-116; Pet. 59-60. Thus, they do not establish that a POSITA would have been motivated to add dummy channels in Nishikawa’s memory stack. Campbell2 ¶¶108-116.

For example, Petitioner quotes Nishikawa123 as “recogniz[ing] the need for support structures.” Pet. 60. Petitioner is incorrect. In fact, the passage Petitioner cites merely describes the formation of a “not shown” dielectric pillar structure and says nothing about a “need” for support structures, let alone describe any motivation to add support structures in Nishikawa, which already has existing support

structures. Campbell2 ¶109. Further, the Petition does not even assert that Nishikawa123 discloses dummy channels. *Id.*; Pet. 60.

Next, Petitioner cites to Masamori, which discloses “conductive support structures.” Masamori (Ex.1020), Cover (Title). But unlike Nishikawa, Masamori’s design does not include separator dielectric structures that provide structural support during the gate replacement process and devotes most of its “contact via region” (yellow) (most of contact regions 200A, 200B) to its conductive support structures, as shown in Figure 20B, annotated below. Campbell2 ¶110 (citing Masamori);

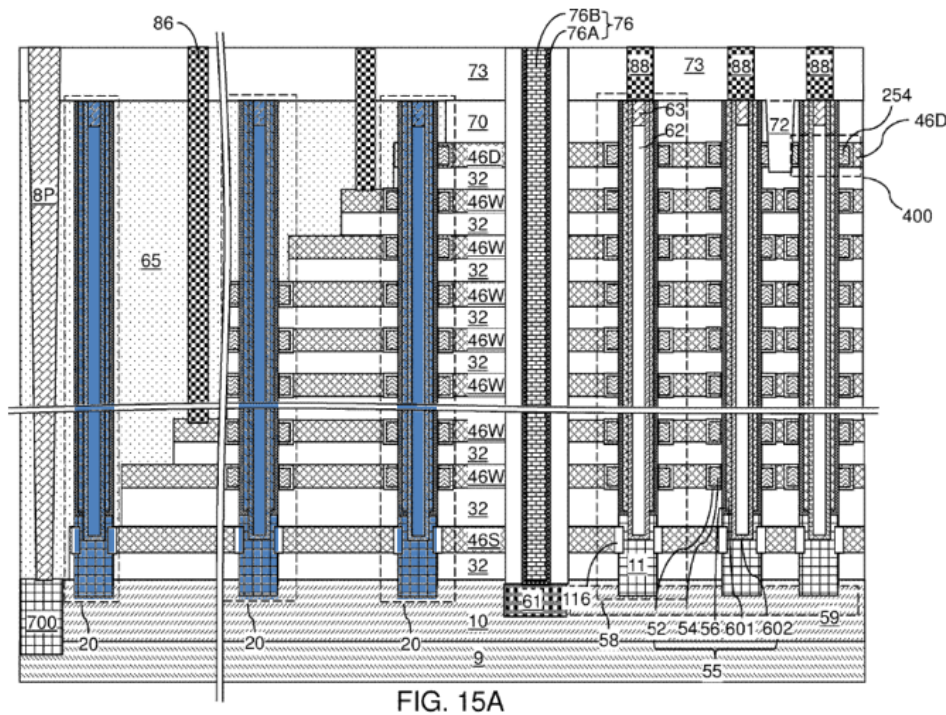


Masamori Fig. 20B (annotated)

Unlike Masamori, Nishikawa does not have a region to accommodate dummy channels. Campbell2 ¶111. Masamori’s disclosure of support structures does not motivate modifying Nishikawa—a different design with separator dielectric

structures 45 that already provide the structural support Petitioner asserts is needed for gate replacement. *Id.*

Petitioner's reliance on Kai's disclosure of dummy channels likewise fails. Kai discloses "support pillar structure[s] 20" taking up significant area in a "contact region 300" in a device that, unlike Nishikawa, (1) includes no separator dielectric structures supporting the other structures during gate replacement, and (2) has a different layout than Nishikawa. Kai Fig. 6A, 6:2-5, 16:28-31; *see also id.* Fig. 15A (below) (showing "support pillar structure 20" (blue) only in the contact region); Campbell² ¶114. Kai would not have motivated a POSITA to add dummy channels to Nishikawa, which already includes support structures. *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1369 (Fed. Cir. 2012) ("Because each device independently operates effectively, a [POSITA], who was merely seeking to create a better device to drain fluids from a wound, would have no reason to combine the features of both devices into a single device."); Campbell² ¶114.



Kai Fig. 15A (annotated)

Finally, Petitioner cites to Kim and Park²⁹⁷, neither of which provide the missing motivation to modify Nishikawa to add redundant support. Pet. 62. Neither Kim nor Park²⁹⁷ disclose adding dummy channels to a device, like Nishikawa, that does not have a region for dummy channels and already contains a dielectric separator structure that provides support throughout the active region of Nishikawa's device. Campbell² ¶115.

Thus, none of Petitioner's cited references disclose adding dummy channels to support a system like Nishikawa's that already has a separator dielectric structure as an existing support structures and no region to accommodate dummy structures;

these references would not have motivated a POSITA to modify Nishikawa. *Id.* ¶116.

C. Petitioner improperly supplies missing limitations using a POSITA's knowledge.

Faced with Nishikawa's deficient disclosures, Petitioner improperly relies on a POSITA's knowledge to gap-fill the missing dummy channel limitations. Petitioner's arguments fail for the reasons described in Section III.B.1.

To the extent Petitioner argues it relied on background references such as Nishikawa¹²³, Masamori, Kai, Park²⁹⁷, or Kim (*see, e.g.*, Pet. 59-64), this argument is improper for the reasons described in Section III.B.1. Further, as discussed above, 3D NAND technology is not "particularly straightforward." *See* Section III.B.1.a

Nor is adding a "dummy channel structure" "unusually simple" such that a Petitioner may rely on a POSITA's knowledge. Campbell² ¶117. As described above and admitted by Petitioner's expert, "[memory] density is *one of the most important aspect[s] in designing memory*," and that "we always want to have as high density as possible; for lower cost, higher yield, and at the end, you know, with lower cost per bit, higher yield, [a] company would ... make a lot more money per chip." Ex.2022 44:8-11, 48:1-6; *see* Ex.1003 ¶¶165, 205; Campbell² ¶102. In other words, real estate in 3D NAND devices is scarce and at a premium. *See* Campbell² ¶117. Thus, it is exceedingly difficult to add features to a device containing

arrangements of distinct but interrelated features at the microscopic scale that, together, form a functioning memory device. *Id.*

The design of 3D NAND features in a dense array—such as dummy channels—is inherently related to the fabrication of 3D NAND. *Id.* ¶118; *see* '322 Patent 5:9-22 (describing the relationship between processing and design); Ex.2036 3 (stating “optimiz[ing] manufacturing processes” “result[s] in better performance, increased yield, and reduced costs”). Creating a 3D NAND device with the claimed features requires being able to etch various features in the structure—which is “the most difficult step in 3D NAND”—along with depositing various materials. Ex.2028 4; Campbell2 ¶118. Indeed, this etching process is “the most critical and challenging step in 3D NAND because it is key to achieving uniform hole size through multiple layers to define the channel of memory cells,” as well as dummy channels. Ex.2023 6; *see* Campbell2 ¶118-19 (citing, e.g., Ex.2032 6; Ex.1010 218 (“One of the issues is related to yield loss derived from complexity of vertical trench or hole etching with many layers.”)); Ex.2031 6. “More than a trillion holes must be etched simultaneously and uniformly on every wafer, each with an aspect ratio of more than 40:1” and virtually no lateral variation to make contact with a landing pad deep in the structure. Ex.2023 6; *id.* 4-5 (“An incredible level of precision and repetition is required in defining complex 3D structures with extremely high aspect ratio (HAR) features.”); Campbell2 ¶118. There is close to no room for error. Campbell2 ¶¶118.

The claimed dummy channel structure extends completely through the memory stack. '322 Patent cl. 3. Forming the claimed dummy channel structure through the memory stack involves various steps of complex semiconductor manufacturing processes. '322 Patent 12:16-23; Campbell2 ¶120. And forming these channels through the entire memory stack is not simple—“[d]eep etch[ing] on these multilayer stacks can *push the limits of physics* to achieve uniformity from top to bottom.” Ex.2023 6; Campbell2 ¶120 (citing, *e.g.*, Ex.2026 6; Ex.2032 7; Ex.2024 2). Indeed, the deeper the etch, the harder it is to maintain a continuous etch rate and unwanted variations can occur, such as tapering, bowing, or twisting within the channel, an incomplete etch, or variation between the top and bottom of the channel. Campbell2 ¶121 (citing *e.g.*, Ex.2030 3; Ex.2031 6-7, Fig. 7).

While some of the above statements refer to memory channels, a POSITA would understand that they equally apply to etching dummy channels through the stack, which is necessary to forming dummy channels and sometimes formed by the same process as memory channels. Campbell2 ¶122; *See, e.g.*, '322 Patent 12:23-27 (“[D]ummy channel structures 302 are formed simultaneously with channel structures 222 in the same fabrication steps.”); Kim [0071] (“The channel holes CH and the dummy holes DH may be formed at the same time.”).

Moreover, dummy channels do not have a standard, predictable structure, instead ranging from containing the same materials as channel structures to being

“fully filled with dielectric materials” like “silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.” ’322 Patent 9:27-37; Campbell2 ¶123.

Petitioner’s cited prior art confirms making a dummy channel structure is not “unusually simple.” Campbell2 ¶124. For example, Kai describes at least seven distinct processing steps for forming a support pillar structure 20 (Petitioner’s “dummy channel”) (Pet. 62) in a particular arrangement. *Id.* (citing Kai). And Park and Kim describe an entirely different method to form a “dummy channel,” further confirming that forming a dummy channel structure is not “unusually simple.” *Id.* ¶¶125-126 (citing Kim, Park297).

Thus, the forming the dummy channel structure missing in Nishikawa is not “unusually simple” and plays a “major role in the claimed subject matter” in providing support in the absence of the barrier structure. *Id.* ¶127; ’322 Patent 4:63-65 (stating barrier structure “preserves a dielectric stack region within a memory stack”), 9:41-43 (“Instead, dummy channel structures 146 can provide mechanical support to the memory array structures, e.g., memory stack 104.”); *see DSS Tech.*, 885 F.3d at 1373-75 (finding limitation for supplying “low duty cycle RF bursts” in telecommunications technology that was “critical” to patent’s goal could not be supplied by knowledge of a POSITA). Petitioner’s reliance on a POSITA’s “general knowledge” to supply the missing “dummy channel” limitation is thus legal error. Petitioner’s arguments as to this limitation fail for this reason alone.

V. Nishikawa and a POSITA's knowledge, alone or with Nishikawa¹²³, do not render obvious “a first diameter [or lateral dimension] of the TAC corresponding to each conductive layer ... is larger than a second diameter [or lateral dimension] of the TAC corresponding to each dielectric layer” (claims 13-18, 20).

Claim 13, which depends from claim 8, recites a “lateral dimension of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second lateral dimension of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs” (*i.e.*, “ribbed via cavity”). ’322 Patent cl. 13. Claim 14 has a nearly identical limitation, except instead of reciting a “lateral dimension,” it recites a “diameter.”¹² *Id.* cl. 14. Claims 15-18 and 20 depend from claim 14. A POSITA would have understood the “first diameter [or lateral dimension]” of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs being larger than the “second diameter [or lateral dimension]” of the TAC corresponding to each dielectric layer of the conductor/dielectric layers pairs is the result of forming a “plurality of ... recesses” by “removing parts of the sacrificial layers abutting the sidewall of the first opening” that is then filled in with the TAC. ’322 Patent 13:42-45, Fig. 3D; Campbell² ¶128.

¹² Petitioner treats the analysis for claims 13 and 14 the same for this limitation. *See* Pet. 75-77, 81-82 (relying on analysis from claim 7). Thus, Petitioner's argument regarding these limitations falls together.

Petitioner asserts that Nishikawa and the knowledge of a POSITA—alone or in combination with Nishikawa¹²³—render obvious the recited ribbed via cavity under two interpretations: (1) by inherent “undetectable and unintentional alleged recesses” formed by the typical etching process resulting in the first and second diameters/lateral dimensions defining the TACs geometry (Pet. 73-75 (citing Ex.1038 (Ex.B-1, YMTC’s Contentions, 11, 28)), and (2) by an “intentional etch that forms actual recesses” for the same TAC geometry (*id.* 73-77). Petitioner’s arguments fail under either construction.¹³ Campbell² ¶129.

A. Petitioner’s arguments fail under its first claim construction that requires “undetectable and unintentional recesses.”

Petitioner argues that Nishikawa renders obvious this limitation “under PO’s incorrect interpretation” that the claim requires “largely undetectable and unintentional alleged recesses.” Pet. 73-75. Patent Owner never set forth such a construction, and YMTC’s infringement contentions say nothing about “undetectable and unintentional” ribbed via cavities. *See* Ex.1038.

To begin with, Petitioner cannot meet its burden under a construction that it asserts is wrong. *See Samsung Elecs. Am., Inc. v. UNILOC 2017 LLC*, IPR2020-

¹³ As the Board recognized, “Petitioner relies upon the general knowledge in the art” to supply this limitation. ID 20-21 (citing Pet. 75). Thus, the analysis for this limitation applies equally to Grounds 1 and 3.

00046, Paper 6 at 7-8 (Apr. 1, 2020) (declining to address grounds based on constructions Petitioner asserted were wrong). Petitioner and Dr. Lee assert that the '322 Patent does not support that the claims cover unintentional recesses because the '322 Patent “makes clear that these limitations relate to an intentional etch that forms actual recesses in the sacrificial layers.” Pet. 73 (citing '322 Patent 13:52-65, Fig. 3D); Ex.1003 ¶170 (citing same). Petitioner does not argue its construction is supported by the plain language of claims 13 and 14—which only recite the diameter/lateral dimensions—or any other intrinsic evidence. *See* Pet. 73-74. Accordingly, Petitioner's arguments under this construction must fail. *See* Campbell2 ¶¶131-136.

Petitioner's arguments under this construction also fail on the merits. Petitioner asserts that “a typical etch through a stack of silicon oxide and silicon nitride layers does not have the exact same selectivity towards each of silicon oxide and silicon nitride, and will result in uneven sidewalls, such that there are recesses in either the oxide layers or the sacrificial layers.” Pet. 74-75. According to Petitioner, as a result “Nishikawa renders this limitation obvious ... because such unintentional recesses would naturally result.” *Id.* 75.

But Petitioner improperly invokes the doctrine of inherency, which requires the limitation be “necessarily ... present[] or the natural result.” *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1195 (Fed. Cir. 2014). Unintentional recesses

are neither the natural result nor necessarily present in Nishikawa. Figure 15 shows Nishikawa's backside contact via structure 76 and accompanying dielectric spacer 74 have a consistent diameter/lateral dimension throughout:

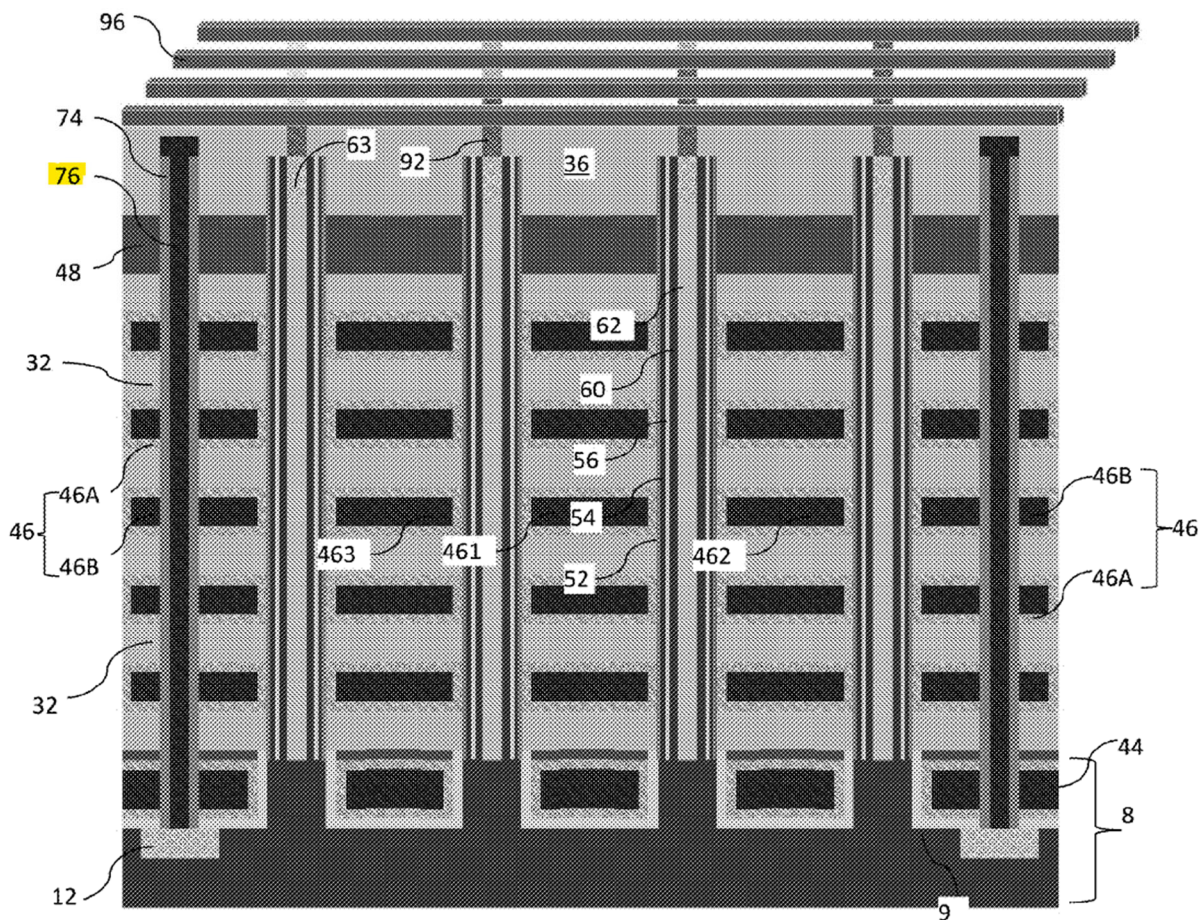


FIG. 15

Nishikawa Fig. 15 (annotated)

Campbell2 ¶131. Indeed, as discussed above, Nishikawa provides for etching recesses in forming the active channels during the gate replacement process, but it does not do so for forming TACs. *Id.*; see Section IV.A.1. Thus, Petitioner failed to

meet its burden to show that Nishikawa renders obvious a ribbed via cavity. Campbell2 ¶131.

Petitioner ignores that Nishikawa teaches a smooth TAC sidewall and instead only points to Nishikawa's disclosure that its "insulating layers 32" can be made of "silicon oxide" and its "sacrificial material layers 42" can be made of "silicon nitride." Pet. 74 (quoting Nishikawa 7:3-11). It argues because "a typical etch" through those layers does not have the same selectivity, the TAC in Nishikawa would have uneven sidewalls. Petitioner is wrong. Unintentional recesses would not have been obvious as the natural result of forming Nishikawa's structure (or would have motivated a POSITA to use such processes). Campbell2 ¶132. Indeed Petitioner's own evidence establishes a POSITA would have been *discouraged* from using an etch process that forms a ribbed via cavity, whether they are intentional or not: "In '3D NAND memory, *it is important to have an etching gas* which can etch both SiO₂ and SiN layers ... *without selectivity*'" to produce "a smooth sidewall." Pet. 74 (quoting Ex.1039 2:59-67); see Campbell2 ¶¶133-134.

Petitioner also asserts Nishikawa renders obvious unintentional recesses because "it is a challenge to find" a gas that can etch "without selectivity." Pet. 74. But that does not mean a POSITA would have understood Nishikawa to use an etch gas *with* selectivity that would result in unintentional recesses that form the claimed ribbed via cavity (let alone would have motivated a POSITA to use such an etch).

Campbell2 ¶134. The opposite is true: A POSITA would have sought and used gases that can etch without selectivity. *Id.* ¶¶134-135; *see, e.g.*, Ex.1039 18:42-44, 24:34-37 (disclosing “hydrofluorocarbon etching gases provide etching through SiN and SiO₂ layers in a single etching process without selectivity”). Thus, as the Board correctly found, “Petitioner’s assertion that a person having ordinary skill in the art would seek to use etches that would result in the claimed first and second diameters is insufficiently supported.” ID 22; *see* Campbell2 ¶133-135. Accordingly, Petitioner failed to prove it would have been obvious to produce the claimed ribbed via cavity even under Petitioner’s “undetectable and unintentional recesses” construction. Campbell2 ¶136.

B. Petitioner’s arguments fail under its second claim construction that requires “intentional” formation of “actual recesses.”

Petitioner next argues this limitation would have been obvious under Petitioner’s second “interpretation” of the claim that requires the “intentional” forming of “actual recesses.” Pet. 73, 75-77. Petitioner concedes that Nishikawa does not disclose this limitation but asserts that it would have been obvious based on a POSITA’s general knowledge. *Id.* Petitioner further asserts that POSITAs would have been motivated to modify Nishikawa to include a ribbed via cavity because doing so would have “serve[d] the same purpose as the ’322 Patent, namely, providing additional area for the dielectric liner.” *Id.* 77. Petitioner is wrong on both counts.

First, as the Board properly found, Petitioner has failed to provide a sufficient motivation to modify Nishikawa to include a ribbed via cavity according to the knowledge of a POSITA. ID 20; *see* Pet. 77. Instead, Petitioner relies entirely on the '322 Patent itself to assert that its proposed modification of Nishikawa would “serve the same purpose as the '322 Patent.” Pet. 77 (citing Cui (Ex.1037) 27:54-28:8). But as the Board explained, “a reason to combine should not be obtained solely from the challenged patent.” ID 21. Doing so is the epitome of hindsight bias. *Millennium Pharms., Inc. v. Sandoz Inc.*, 862 F.3d 1356, 1367 (Fed. Cir. 2017) (“[T]he inventor’s own path itself never leads to a conclusion of obviousness; that is hindsight.”).

As the Board noted, neither Petitioner nor Dr. Lee explain why the hindsight motivation of providing “additional area for the dielectric liner” is advantageous, only that it creates a longer spacer—the same purpose of the lateral recesses in the '322 Patent. ID 21; *see also* Pet. 77; Ex.1003 ¶173; Campbell2 ¶¶138-140. Petitioner’s improper reliance on the '322 Patent is underscored by its admission that the '322 Patent “provides virtually no explanation on creating these known rib regions.” Pet. 77. In sum, Petitioner’s motivation to combine fails and is derived solely from the '322 Patent, which is insufficient; Petitioner has not shown claims 13 and 14 are obvious. *Millennium*, 862 F.3d at 1367; Campbell2 ¶139. Petitioner’s

assertions as to claims 15-18, and 20 likewise fail by relying on the same assertions as claims 14 and 13.

Second, Petitioner points to background references to show it was “well known” to have a ribbed-shaped opening, Pet. 75-76, but this shows, at best, that a POSITA “*could have made*” a ribbed opening, not that a POSITA “*would have been motivated to make*” one. *Belden Inc.*, 805 F.3d at 1073; Campbell2 ¶140. Regardless, Kai, for example, does not support Petitioner’s argument. Petitioner cites Kai for disclosure of forming “lateral[] recesses[s].” Pet. 75 (citing Kai 11:9-34). But Petitioner does not assert—nor can it—that those lateral recesses in the “sacrificial layers” of an alternating stack of dielectric and sacrificial layers produce openings associated with a TAC, as claimed. Campbell2 ¶140. Indeed, Kai does not disclose a “ribbed via cavity” that provides “additional area for the dielectric liner” (Pet. 77)—the foundation of Petitioner’s argument. *Id.*; see Pet. 77. Instead, Kai discloses that the recesses are filled with blocking dielectric 52 and a floating gate electrode 54 before tunneling dielectric layer 56 is deposited, not a spacer in a TAC. Kai 11:35-39, 12:20-23, 12:47-49, 12:56-61, 13:48-51, Figs. 5C-5G; Campbell2 ¶140.

Petitioner provides no reason—other than hindsight bias based on the ’322 Patent—why a POSITA would implement the claimed ribbed via cavity in

Nishikawa's backside contact via structures 76. Pet. 75; Campbell2 ¶141. Thus, Petitioner's arguments fail under this construction.

C. Petitioner improperly supplies a missing limitation using a POSITA's knowledge.

Faced with Nishikawa's deficient disclosures, Petitioner improperly relies on a POSITA's knowledge to gap-fill the missing ribbed cavity via limitation. Petitioner's arguments fail for the reasons described in Section III.B.1. To the extent Petitioner argues it relied on background references, such as Kai (*see, e.g.*, Pet. 75-76), this argument is improper for the reasons described in Section III.B.1. Further, as discussed above, 3D NAND technology is not "particularly straightforward." *See* Section III.B.1.a.

Petitioner also failed to demonstrate or support that modifying Nishikawa to include TAC's with the recited lateral dimensions/diameters is "*unusually simple*." Indeed, Petitioner's own evidence confirms that creating etch recipes to produce a desired profile of a TAC's sidewall is "a challenge," Pet. 74 (quoting Ex.1039 2:59-67), and Dr. Lee had to put the etching process into "simple terms" in attempting to explain it, Ex.1003 ¶170. Campbell2 ¶142.

Forming a TAC with the ribbed via cavity requires, among other things, that "the lateral dimension" be "controlled by the etching rate and/or etching time," which is a challenge. '322 Patent 13:61-63; Campbell2 ¶143 (citing Ex.2034 2; Ex.2029 5-6; Ex.2035 1). Forming recesses to define the diameter of the TAC cannot

be simplified to etchant selection because control of the etchant chemistry, hole geometry, surrounding material, and complex process conditions are all key. Campbell2 ¶144 (citing, *e.g.*, Ex.1012 1:17-28, 6:10-13; Ex.2026 8-9).

It is increasingly complex and challenging to achieve consistent etch profiles throughout the holes in a memory array as the height of 3D NAND increases, especially when trying to reach a certain depth. *Id.* ¶145; Ex.2036 3-4, Fig. 3; *see Motorola*, IPR2024-00688, Paper 7 at 29 (ruling process “Petitioner proposes to arrive at the structure of limitation” that recites a light blocking sheet with particular diameters was not “unusually simple,” reasoning Petitioner failed to “indicate how much time beyond CN182’s stated range of 3 to 5 hours would be required” for the etching to reach the recited depth required by the claimed structure). Moreover, the choice of material for both the target and non-target layers must be highly compatible with the selective etch chemistry because any incompatibility could lead to non-uniform etching, structural defects, or failure to form the intended structure. Campbell2 ¶145; *see, e.g.*, Kai 11:16-20. Petitioner thus cannot rely on a POSITA’s general knowledge to supply the missing ribbed via cavity.

VI. Nishikawa and a POSITA’s knowledge, alone or with Nishikawa123, do not render obvious a “diameter of the TAC is at least equal to a diameter of the peripheral contact” (claims 6, 9-10, 15-16).

Claims 6 and 15 recite “a diameter of the TAC is at least equal to a diameter of the peripheral contact.” ’322 Patent cls. 6, 15. Claim 16 depends from claim 15.

Id. cl. 16. The claimed TAC extends through the memory stack, while the peripheral contact is outside the memory stack. *Id.* cls. 1, 6, 14.

Petitioner argues “it would have been obvious to implement Nishikawa’s TAC as a cylindrical contact with a diameter” and that a POSITA would have been motivated “to make the TAC and peripheral contacts the same size.” Pet. 67, 69. Petitioner does not argue that Nishikawa discloses its trench-shaped backside contact via structures 76 (*i.e.*, TAC) are at least equal in diameter to the contact via structures 86 (*i.e.*, peripheral contacts). *See id.* 67-70. Nor could it—as discussed above, Nishikawa’s backside contact via contact structure 76 is not circular (and therefore does not have a diameter). *See* Section III.A.; Campbell2 ¶147. Because a POSITA would not have modified Nishikawa to have a substantially circular TAC, Petitioner fails to prove claims 6 and 15 obvious. *See* Section III. Nonetheless, Petitioner argues a POSITA would have been motivated to implement the claimed diameters because it was “well known” to do so and “saves ... process time.” Pet. 68-70. Petitioner’s arguments fail.

First, Petitioner asserts that Nakajima and Mushiga disclose TACs and peripheral contacts with the same diameters by comparing what appear to be their relative sizes in figures without dimensions. *Id.* 68-69. But “arguments based on drawings not explicitly made to scale in issued patents are unavailing.” *Nystrom v. TREX Co.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005); *see* Mushiga (Ex.1012) 6:30 (“The

drawings are not drawn to scale.”); Nakajima (not disclosing drawings are to scale). Thus, Nakajima and Mushiga do not support Petitioner's obviousness argument.¹⁴

Second, Petitioner asserts that a POSITA would have been motivated to modify Nishikawa because it was “common” to have the peripheral contacts and the TACs the same diameter. Pet. 68-69. But this shows, at best, that a POSITA “*could have made*” dummy channels, not that a POSITA “*would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc.*, 805 F.3d at 1073; Campbell2 ¶148.

Third, Petitioner asserts a POSITA would have been motivated to form the peripheral contacts and TAC with “the same size to employ a common process (including the hole size in masking steps) when forming the contacts” to save “process time.” Pet. 68-69. Petitioner relies on Mushiga, Tessariol, and Nakajima to show the general knowledge of a POSITA includes forming peripheral contacts and TACs at the same time. *Id.* None of those references teach what Petitioner asserts,

¹⁴ Petitioner makes the same mistake by arguing Cui demonstrates the knowledge of a POSITA renders obvious that the diameter of a dummy channel is smaller than the TAC and peripheral contact, as recited in claim 6.D. *See* Pet. 71 (citing Cui Fig. 25B).

let alone would have motivated a POSITA to form the claimed diameters.¹⁵ Campbell2 ¶149.

Petitioner asserts Mushiga's TACs 588—inside and outside the stack—are formed at the same time and “use[] the same processing steps.” Pet. 68. Mushiga does not disclose anything about the timing of forming the cavities that become structures 588. *See id.* (citing Mushiga Fig. 5, 10:31-58); Campbell2 ¶150. Mushiga at most discloses the timing of the formation of the cavities in relation to the formation of the conductive layers 146, 246, but this does not teach simultaneous formation of cavities both through and outside the stack. Campbell2 ¶150; Mushiga 10:49-57.

Petitioner's reliance on Nakajima is similarly flawed because it relies on disclosures relating only to forming contacts in Nakajima's stack. Campbell2 ¶¶151-152. Petitioner argues “Nakajima only discloses one step for creating the H1 holes” for forming the “C4 contacts” inside and outside the stack. Pet. 69 (citing Nakajima

¹⁵ For claim 9, Petitioner relies on its argument regarding limitation 6.C, including Mushiga and Nakajima, to argue it would have been obvious “a thickness of the spacer in the TAC is nominally identical to a thickness of a spacer in the peripheral contact.” Pet. 79-80. For the reasons discussed regarding claim 6, Petitioner's arguments regarding claims 9 and 10 also fail.

7:35-8:11, Fig. 2). But the component in area 100d in Nakajima Petitioner identifies as “C4” should be “C3,” which are Nakajima’s peripheral contacts. Campbell2 ¶151. When describing Figure 2, Nakajima states that “the contacts C3 are provided in the peripheral area 100d,” such that “[a]n upper end of a contact C3 is coupled to an interconnect M0 via a contact Cb.” *Id.*; Nakajima 4:57-60; *see* Nakajima 3:59 (disclosing that “area 100d includes contacts C3,” not C4). Moreover, Nakajima discloses that “[t]he contacts C4 are provided in the layer stack 120 in the staircase area 100c on the other side and in the contact area 100b,” not the peripheral area 100d. Nakajima 4:49-51, 3:23-30; *see id.* Fig. 1; Campbell2 ¶151. In fact, there is no textual disclosure in Nakajima that describes contacts C4 in peripheral area 100d. Campbell2 ¶151.

As a result, Petitioner’s reliance on Nakajima’s disclosures regarding “C4” (Pet. 69 (citing Nakajima 7:5-8:11)) should be ignored: Where a prior art reference contains “an error obvious to one of ordinary skill in the art, it cannot be said to describe or suggest” the errant information. *In re Yale*, 434 F.2d 666, 668-69 (C.C.P.A. 1970) (describing that a POSITA “would readily recognize” an internal inconsistency within a reference as signifying error); *LG Elecs. Inc. v. ImmerVision, Inc.*, 39 F.4th 1364, 1372 (Fed. Cir. 2022) (affirming finding that a prior art table included an obvious error that would have been apparent to a POSITA, eliminating the erroneous portion as prior art).

Moreover, forming “hole H1”—the process Petitioner asserts forms both the peripheral contacts and the TACs—is “formed in the insulation layers ... and the layer stack 120 as shown in FIG. 8.” Nakajima 7:37-39; Campbell2 ¶152. The “hole H1 penetrates the insulation layers ... and the layer stack 120, to reach the silicon nitride layer 41.” Nakajima 7:41-43; Campbell2 ¶152. Thus, a POSITA would have understood Nakajima discloses that all H1 holes for the C4 structures—which are in the stack, not the periphery—are etched *through the stack*. Campbell2 ¶152.

Tessariol's disclosure Petitioner relies on—like Nakajima's—merely discloses two holes that are both formed through the stack, not the claimed TAC through the stack and a peripheral contact outside the stack. Tessariol (Ex.1036) [0037]; Campbell2 ¶153. In particular, as seen below in Figure 9, Petitioner pointed to the dummy-structure openings 56 (blue) and via openings 54 (green) that are both formed *through the stack* (red box):

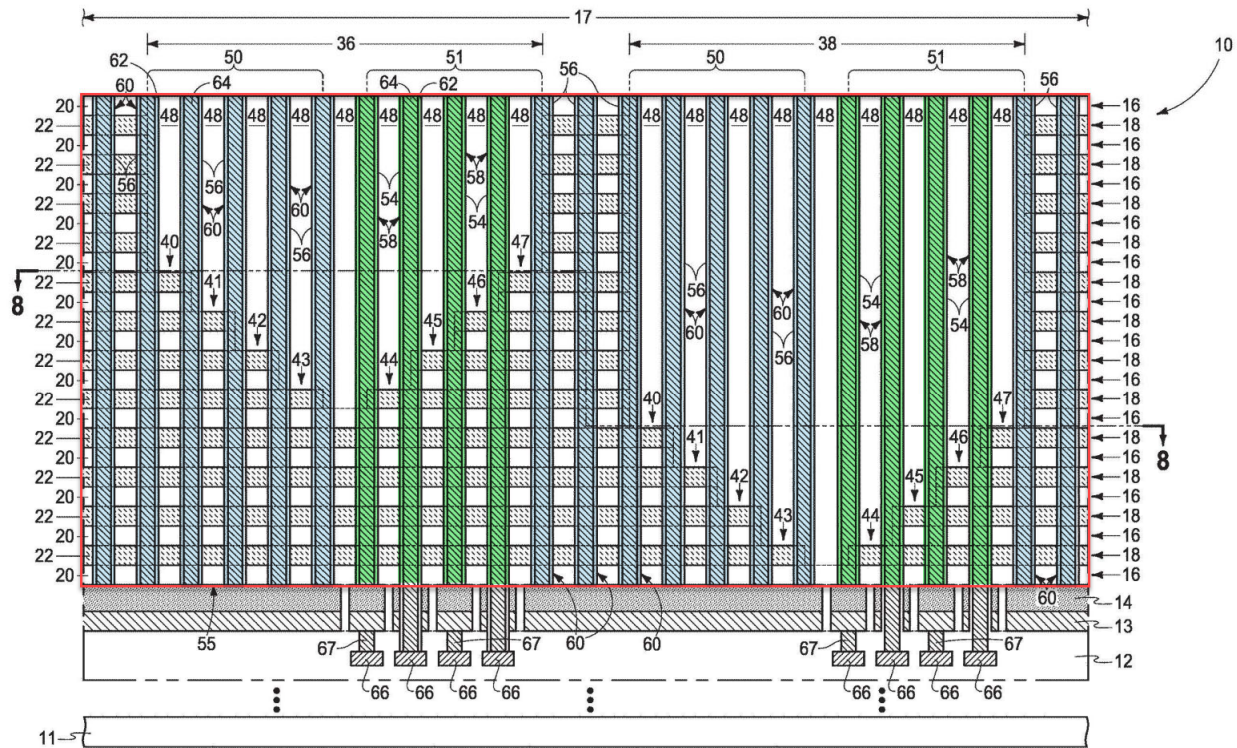
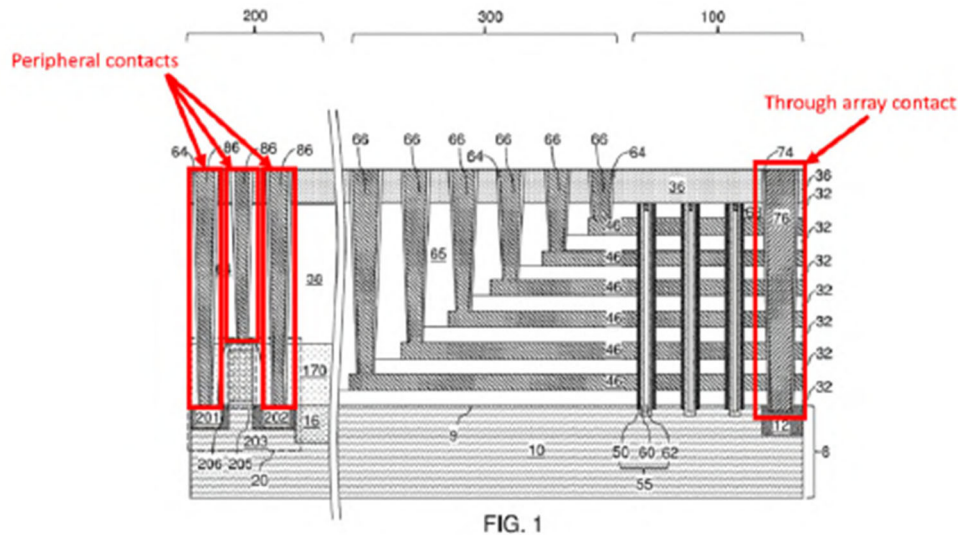


FIG. 9

Tessariol Fig. 9 (annotated); *see* Pet. 69-70 (citing Tessariol [0037], Fig. 9).

Regardless, Petitioner's motivation to combine fails because a POSITA would not have used a "common process" to form Nishikawa's TAC and peripheral contacts, as Petitioner proposes, and thus would not save processing time. Rather, a POSITA would have used different etch chemistries for etching the TAC openings and peripheral contact openings. Campbell2 ¶155; *see* Pet. 68-69. In Nishikawa, the backside contact via contacts 76 (TAC) and the contact via structures 86 (peripheral contacts) are in different regions of the memory device and etch through different structures. Campbell2 ¶155.



Pet. 67 (annotating Nishikawa Fig. 1). Indeed, the contact via structures 86 are formed by etching the dielectric material 38 and planarization dielectric layer 170, while the contact via structures are formed in openings that etch through the stack of alternating, sacrificial and insulating layers. See Nishikawa 6:8-28 (dielectric materials), 7:4-15 (describing different materials for insulating layers 32 and sacrificial material layers 42); Campbell2 ¶155. Even if the peripheral contact and TAC had the same diameter, etching processes generally etch different materials at different rates. Campbell2 ¶155. Because Nishikawa's TAC and peripheral contacts form in spaces etched through different materials, a POSITA would not have used a "common process," including etching forming the openings at the same time, as Petitioner argues. *Id.* Nor would a POSITA have used the same etch chemistries, as Petitioner asserts. *Id.*; see Pet. 70.

Fourth, as explained throughout, Petitioner repeats legal errors. Petitioner improperly relies on the knowledge of a POSITA and disclosures from references not in these grounds to supply missing limitations. *See* Section III.B.1. Regardless, forming TACs and etching contact holes are not unusually simple, and 3D NAND is not a particularly straightforward technology. *See id.* This limitation is no different. Campbell2 ¶156.

Thus, Petitioner fails to render obvious claims 6 and 15-16.

VII. Claims 11-12 and 17-18 are not obvious over Nishikawa in view of the knowledge of a POSITA, Nishikawa123, and/or Lu.

Petitioner's challenge of dependent claims 11-12 and 17-18 in Grounds 2 and 4 relies on the failed Grounds 1 and 3 arguments for claims 8 and 14, respectively. Pet. 96-98, 100. Petitioner does not rely on Lu to teach any claim limitation in claims 8 and 14. Pet. 84-98, 100. Accordingly, Petitioner has not proven claims 11-12, and 17-18 would have been obvious in Grounds 2 and 4 for the same reasons as discussed above for Grounds 1 and 3.

VIII. Conclusion

For the reasons set forth above, the Board should deny the Petition for Inter Partes Review.

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(2) because the Patent Owner's Response contains a total of 13,938 words, which is the sum of 13,885 words calculated by Microsoft Word's word-count feature and 53 words hand counted in the figures. This total excludes the cover page, signature block, and the parts of the Patent Owner's Response exempted by 37 C.F.R. § 42.24(b)(2).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 17th day of November, 2025, a true and correct copy of the foregoing **Patent Owner's Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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