

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00191
U.S. Patent No. 11,581,322

PETITIONER'S REPLY BRIEF

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LISTING OF EXHIBITS

Exhibit.	Description
1001	U.S. Patent No. 11,581,322 to Guo et al. (“322 patent”)
1002	File History of U.S. Patent No. 11,581,322 (“322 FH”)
1003	Declaration of Dr. Jack C. Lee (“Lee”)
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent No. 9,837,431 to Nishikawa et al. (“Nishikawa”)
1006	U.S. Patent No. 9,853,046 to Lu et al. (“Lu”)
1007	U.S. Patent No. 10,658,378 to Tao et al.
1008	U.S. Patent Publication No. 2019/0229125A1 to Zhou et al.
1009	U.S. Patent No. 10,777,501 to Nakajima et al. (“Nakajima”)
1010	Micheloni, “3D Flash Memories” (2016)
1011	U.S. Patent Publication No. 2017/0179026 A1 to Toyama et al.
1012	U.S. Patent No. 10,354,980 to Mushiga et al. (“Mushiga”)
1013	PCT Publication No. WO 2019/042103A1 to Dai et al.
1014	U.S. Patent No.10,679,721 to Kim et al.
1015	Aritome, “NAND Flash Memory Technologies” (“Aritome”)
1016	File History for U.S. Patent Application No. 16/745,342
1017	U.S. Patent Publication No. 2012/0280304A1 to Lee et al. (“Lee304”)
1018	U.S. Patent Publication No. 2017/0125430A1 to Nishikawa et al. (“Nishikawa430”)
1019	U.S. Patent Publication No. 2015/0348987A1 to Lee et al. (“Lee987”)

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1020	U.S. Patent Publication No. 2018/0301374A1 to Masamori et al. (“Masamori”)
1021	U.S. Patent No. 8,107,292 to Maejima
1022	U.S. Patent No. 10,347,654 to Iwai et al. (“Iwai”)
1023	U.S. Patent No. 10,559,583 to Park et al.
1024	U.S. Patent No. 5,945,717 to Chevallier
1025	U.S. Patent No. 10,347,487 to Lee et al.
1026	Ronse, “Optical lithography—a historical perspective,” C. R. Physique 7 (2006) (“Ronse”)
1027	U.S. Patent No. 10,290,643 to Kai et al. (“Kai”)
1028	U.S. Patent No. 9,859,297 to Park et al. (“Park297”)
1029	U.S. Patent Publication No. 2018/0308559 to Kim et al. (“Kim559”)
1030	U.S. Patent No. 8,945,996 to Tang et al.
1031	U.S. Patent No. 10,115,632 to Masamori et al. (“Masamori632”)
1032	U.S. Patent No. 10,879,254 to Guo et al.
1033	U.S. Patent No. 9,793,139 to Sharangpani et al.
1034	Wolf, “Silicon Processing for the VLSI Era, Volume 1-Process Technology,” Lattice Press (1986) (“Wolf Vol. 1”)
1035	Wolf, “Silicon Processing for the VLSI Era, Volume 2-Process Integration,” Lattice Press (1990) (“Wolf Vol. 2”)
1036	U.S. Patent Publ. No. 2019/0081061 to Tessariol et al. (“Tessariol”)
1037	U.S. Patent No. 10,304,852 to Cui et al. (“Cui”)

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1038	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,879,254 (Ex. B-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) (“Ex. B-1, YMTC’s Contentions”) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1039	U.S. Patent No. 11,075,084 to Shen et al.
1040	U.S. Patent No. 10,504,596 to Goda et al.
1041	U.S. Patent No. 10,381,369 to Kim et al. (“Kim369”)
1042	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1043	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1044	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.’s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1045	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL
1046	U.S. Patent No. 9,935,123 to Nishikawa (“Nishikawa2”)
1047	Printout, 11/26/2024, Britannica (https://www.britannica.com/science/geometry) (ellipse)
1048	Declaration of Jared Bobrow in Support of Petitioner’s Motion for Admission <i>Pro Hac Vice</i>
1049	<i>Intentionally Omitted</i>
1050	<i>Intentionally Omitted</i>

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1051	Press Release, Micron, Micron and Intel Unveil New 3D NAND Flash Memory (Mar. 26, 2015) (“Micron ‘3D NAND Flash Memory’ Press Release”)
1052	Press Release, Micron, <i>Micron and WekaIO Win Best of Show Award at the Flash Memory Summit 2019</i> (Aug. 29, 2019) (“Micron ‘Best of Show Award’”)
1053	Micron Technology, Inc., Annual Report (Form 10-K) (Oct. 4, 2024)
1054	Ministry of Industry and Information Technology, <i>The Ministry of Industry and Information Technology Officially Announced the “National Integrated Circuit Industry Development Promotion Outline”</i> (Jun. 26, 2014) (https://www.cac.gov.cn/2014-06/26/c_1111325916.htm) (“National IC Development Promotion Outline”)
1055	Certified English Translation of EX1054 (National IC Development Promotion Outline)
1056	Karen M. Sutter et al., Cong. Rsch. Serv., R47558, <i>Semiconductors and the CHIPS Act: The Global Context</i> (2023)
1057	Alex He, <i>Case Study: From Paper Tiger to Real Tiger? The Development of China’s Semiconductor Industry</i> , CENTRE FOR INT’L GOVERNANCE INNOVATION 14 (2021)
1058	State-Owned Assets Supervision and Administration Commission of the State Council (SASAC), <i>Definition of “State-Owned Enterprise”</i> (July 4, 2019) (https://www.sasac.gov.cn/n2588040/n2590387/n9854212/c11647665/content.html) (“SASAC Definition”)
1059	Certified English Translation of EX1058 (SASAC Definition)
1060	China’s State Council, <i>Notice of the State Council on Issuing “Made in China 2025”</i> (May 19, 2015) (https://www.gov.cn/zhengce/content/2015-05/19/content_9784.htm) (“Made in China 2025”)
1061	Certified English Translation of EX1060 (Made in China 2025)
1062	Karen M. Sutter, Cong. Rsch. Serv., R46767, <i>China’s New Semiconductor Policies: Issues for Congress</i> (2021)

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1063	Liu Yuanchun et al., <i>Accelerating the Realization of High-Level Scientific and Technological Self-Reliance</i> , PEOPLE (July 15, 2024) (http://paper.people.com.cn/zgjzk/html/2024-07/15/nw.zgjzk_20240715_1-05.htm) (“ <i>People’s Paper Article</i> ”)
1064	Certified English Translation of EX1063 (<i>People’s Paper Article</i>)
1065	YMTC, <i>Yangtze Memory Technologies Co. Ltd. Officially Established</i> (Aug. 1, 2016) (https://www.ymtc.com/cn/news/28.html) (“YMTC Press Release”)
1066	Certified English Translation of EX1065 (YMTC Press Release)
1067	Testimony of Stephen Ezell (VP, Global Innovation Policy – Information Technology & Innovation Foundation) Before the U.S.-China Economic and Security Review Commission (Apr. 14, 2022)
1068	Yahoo! Finance, South China Morning Post, Tech War: China’s Top Memory Chip Maker YMTC Gets US\$7 Billion From State-Backed Investors (Mar. 2, 2023) (“ <i>Yahoo! Article</i> ”)
1069	Baidu, <i>Yangtze Memory Increases Capital and Expands Capacity to RMB 100 Billion, Big Fund Phase II Forms a Partnership with Local Hubei State-owned Assets</i> (Mar. 2, 2023) (https://baijiahao.baidu.com/s?id=1759256650733024656&wfr=spider&for=pc) (“ <i>Baidu Article</i> ”)
1070	Certified English Translation of EX1069 (<i>Baidu Article</i>)
1071	YMTC’s Rule 7.1 Corporate Disclosure Statement, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , Case No. 5:23-cv-05792-VKD (N.D. Cal. Nov. 9, 2023)
1072	Lianhe Credit Rating Co., Ltd., Wuhan Optics Valley Financial Holding Group Co., Ltd., 2024 Tracking Rating Report (Jun. 28, 2024) (“ <i>2024 Tracking Rating Report</i> ”)
1073	Certified English Translation of EX1072 (2024 Tracking Rating Report)

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1074	State-Owned Assets Supervision and Administration Commission of the State Council (SASAC), <i>Focusing on Key Points and Making Breakthroughs in Innovation, Hubei Solidly Promotes the Deepening and Improvement Actions to Go Deeper and More Concrete</i> (Mar. 25, 2024) (www.sasac.gov.cn/n4470048/n29955503/n30329277/n30329358/c30380577/content.html) (“Statement of China’s State Council”)
1075	Certified English Translation of EX1074 (Statement of China’s State Council)
1076	Sina Finance, <i>Yangtze Memory’s “Double 11 Performance” Surpassed Samsung’s for the First Time</i> (Nov. 12, 2024) (https://finance.sina.com.cn/roll/2024-11-12/doc-incvupap6483110.shtml) (“Sina Finance Article”)
1077	Certified English Translation of EX1076 (<i>Sina Finance</i> Article)
1078	Southeast University, <i>Yangtze Memory Technologies Co., Ltd. 2024 Campus Recruitment</i> (Mar. 13, 2024) (https://seu.91job.org.cn/substation/lectureDetail?xjhid=1000000000301932&xxdm=10286) (“Southeast Univ., YMTC 2024 Campus Recruitment”)
1079	Certified English Translation of EX1078 (Southeast Univ., YMTC 2024 Campus Recruitment)
1080	Wuhan University of Science and Technology, <i>Yangtze Memory Technologies Co., Ltd. 2020 Campus Recruitment Introduction</i> (Sept. 10, 2019) (https://wust.91wllm.cn/teachin/view/id/97310) (“Wuhan Univ. of Sci. and Tech., YMTC 2020 Campus Recruitment Introduction”)
1081	Certified English Translation of EX1080 (Wuhan Univ. of Sci. and Tech., YMTC 2020 Campus Recruitment Introduction)
1082	China University of Petroleum, <i>Yangtze Memory 2025 Campus Recruitment</i> (Feb. 20, 2025) (https://career.cup.edu.cn/job/view/id/618140) (“China Univ. Of Petroleum, YMTC 2025 Campus Recruitment”)
1083	Certified English Translation of EX1082 (China Univ. of Petroleum, YMTC 2025 Campus Recruitment)
1084	Yoko Kubota et al., <i>U.S. Chip Equipment Suppliers Suspend Business Activities at Yangtze Memory</i> , WALL STREET JOURNAL CHINA (Oct. 13, 2022) (https://cn.wsj.com/articles/美国供应商暂停在中国长江存储科技的业务活动-11665617406) (“WSJ China Article”)

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1085	Certified English Translation of EX1084 (<i>WSJ China Article</i>)
1086	Letter from Michael T. McCaul, Member of Congress, and Bill Hagerty, U.S. Senator, to the Honorable Gina Raimondo, U.S. Commerce Secretary (July 12, 2021)
1087	Demetri Sevastopulo, <i>Bipartisan Group Urges US Blacklist for “Beijing-Directed” Chipmaker</i> , FINANCIAL TIMES (Sept. 20, 2022) (https://www.ft.com/content/173eb5b7-c211-4fa8-af8e-93382ed12836) (“ <i>Financial Times Article</i> ”)
1088	U.S. Senator Charles E. Schumer, <i>With Chinese Chip Companies Threatening National Security And Jobs, Schumer Announces President Has Heeded His Call And Will Add YMTC - One Of China’s Leading Chip Makers - To A Trade Blacklist; Administration Action Will Strengthen National Security And Protect The Domestic Chip Industry</i> (Dec. 16, 2022) (“Schumer Statement”)
1089	U.S. Department of Defense, <i>DOD Releases List of People’s Republic of China (PRC) Military Companies in Accordance with Section 1260H of the National Defense Authorization Act for Fiscal Year 2021</i> (Jan. 31, 2024) (https://www.defense.gov/News/Releases/Release/article/3661985/dod-releases-list-of-peoples-republic-of-china-prc-military-companies-in-accord/)
1090	U.S. Department of Defense, <i>Entities Identified as Chinese Military Companies Operating in the United States in accordance with Section 1260H of the William M. (“Mac”) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Public Law 116-283)</i> (https://media.defense.gov/2024/Jan/31/2003384819/-1/-1/0/1260H-LIST.PDF)
1091	<i>Oversight of the USPTO: Hearing Before the Subcomm. On Intellectual Property</i> , 118th Cong. (2023) (Testimony of Katherine Vidal, Undersecretary of Commerce for IP and Director of USPTO)
1092	China’s State Council, <i>Notice of the State Council on Issuing Policies to Promote the High-quality Development of the Integrated Circuit Industry and Software Industry in the New Era</i> (Aug. 4, 2020) (https://www.gov.cn/zhengce/content/2020-08/04/content_5532370.htm) (“State Council Notice on Policies to Promote Development of IC”)

Exhibit.	Description
1093	Certified English Translation of EX1092 (State Council Notice on Policies to Promote Development of IC)
1094	Declaration of Karen Lee, Translator (Mar. 10, 2025)
1095	Declaration of Fei-Xue Qian, Translator (Mar. 10, 2025)
1096	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Techs. Co., Ltd. v. Micron Tech., Inc. et al.</i> , Case No. 3:23-cv-05792-RFL, Docket No. 243 (N.D. Cal. Mar. 14, 2025)
1097	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s Disclosure of YMTC I Asserted Claims and Infringement Contentions, <i>Yangtze Memory Techs. Co., Ltd. v. Micron Tech., Inc. et al.</i> , Case no. 23-cv-05792-RFL (N.D. Cal. May 6, 2024)
1098	Declaration of Ingrid Hsieh-Yee, Ph.D. Regarding Micron EX1010 (Michelsoni), originally filed in Case No. IPR2025-0034 (SERVICE ONLY)
1099	Entry on the Wiley Online Library for Aritome, "NAND Flash Memory Technologies," https://onlinelibrary.wiley.com/doi/book/10.1002/9781119132639 (SERVICE ONLY)
1100	U.S. Copyright Registration for Aritome, "NAND Flash Memory Technologies" (SERVICE ONLY)
1101	Library of Congress Marc Record for Aritome, "NAND Flash Memory Technologies," https://search.catalog.loc.gov/instances/f731a7af-7a75-5ccf-9aca-32cf0b662658?option=lccn&query=2016462666 (SERVICE ONLY)
1102	Declaration of Jeremy Jason Lang regarding Ronse (EX1026) (SERVICE ONLY)
1103	US Copyright Registration for Wolf & Tauber Vol. 1 (1986) (SERVICE ONLY)
1104	US Copyright Registration for Wolf & Tauber Vol. 2 (1990) (SERVICE ONLY)
1105	Reply Declaration of Dr. Jack C. Lee ("Lee2")
1106	Transcript of the Deposition of Stephen Campbell, taken January 23, 2026, Micron Tech. Inc. v. Yangtze Memory Techs. Co., IPR2025-00191

Exhibit.	Description
1107	Additional excerpts from Wolf, “Silicon Processing for the VLSI Era, Volume 1-Process Technology,” Lattice Press (1986)
1108	U.S. Patent No. 11,043,507
1109	U.S. Patent Publication No. 2015/0029775A1
1110	U.S. Patent Publication No. 2019/0027434A1
1111	U.S. Patent No. 10,115,737 (“Iwai737”)
1112	U.S. Patent No. 9,449,987 (“Miyata”)
1113	U.S. Patent No. 9,929,174 (“Mizutani”)
1114	U.S. Patent Publication No. 2019/035942A1 (“Kwon”)
1115	U.S. Patent Publication No. 2018/0190540 (“Liu”)
1116	PCT Publication No. WO 2019/066829A1

TABLE OF ABBREVIATIONS

ABBREVIATION	TERM
'322 patent	U.S. Patent No. 11,581,322 (EX1001)
Cui	U.S. Patent No. 10,304,852 (EX1037)
Iwai	U.S. Patent No. 10,347,654 (EX1022)
Iwai737	U.S. Patent No. 10,347,654 (EX1111)
Kai	U.S. Patent No. 10,290,643 (EX1027)
Kim559	U.S. Patent Publication No. 2018/0308559 (EX1029)
Kwon	U.S. Patent Publication No. 2019/035942A1 (EX1114)
Lee	Declaration of Dr. Jack C. Lee (EX1003)
Lee2	Reply Declaration of Dr. Jack C. Lee (EX1105)
Liu	U.S. Patent Publication No. 2018/0190540 (EX1115)
Masamori	U.S. Patent Publication No. 2018/0301374A1 (EX1020)
Masamori632	U.S. Patent No. 10,115,632 (EX1031)
Miyata	U.S. Patent No. 9,449,987 (EX1112)
Mizutani	U.S. Patent No. 9,929,174 (EX1113)
Mushiga	U.S. Patent No. 10,354,980 (EX1012)
Nakajima	U.S. Patent No. 10,777,501 (EX1009)
Nishikawa	U.S. Patent No. 9,837,431 (EX1005)
Nishikawa2	U.S. Patent No. 9,935,123 (EX1046)
Park297	U.S. Patent No. 9,859,297 (EX1028)
Tessariol	U.S. Patent Publication No. 2019/0081061 (EX1036)

ABBREVIATION	TERM
ID	Decision Granting Institution of <i>Inter Partes</i> Review (Paper 22)
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,581,322 (Paper 1)
Petitioner	Micron Technology, Inc.
PO or Patent Owner	Yangtze Memory Technologies Co. Ltd.
POPR	Patent Owner's Preliminary Response (Paper 12)
POR	Patent Owner's Response (Paper 34)

I. INTRODUCTION

PO raises four meritless arguments against Nishikawa and Nishikawa-Nishikawa2.

First, PO's argument that Nishikawa would be inoperable if it included a circular TAC fails, because (1) it relies on manipulating Nishikawa's structure—in ways its own expert, Dr. Campbell, said no POSITA would do—to artificially create a short circuit, and (2) Nishikawa2, which has the same architecture as Nishikawa, expressly discloses a circular TAC.

Second, PO's argument that including dummy channels in Nishikawa would not be obvious fails, because the full trial record demonstrates that to overcome edge effects and stability issues in 3D memories, dummy channels were known to provide a suitable solution. PO's arguments rely on misinterpreting Nishikawa, e.g., suggesting that Nishikawa needs no additional support structures by conveniently ignoring portions of its device (the edges and the connection region).

Third, PO's argument that a ribbed TAC would not be obvious fails, because it ignores that such TACs were known to be a suitable option to mitigate risks of short circuits and capacitive coupling.

Fourth, PO's argument that a POSITA would not implement Nishikawa with peripheral contacts and TACs having the same diameters fails, because it ignores the

record evidence that forming various contacts with the same diameter was a suitable solution to a known over-etching problem.

This is a classic case of the limitations-at-issue being well known and routine techniques to address known problems—the epitome of obvious.

II. ARGUMENT

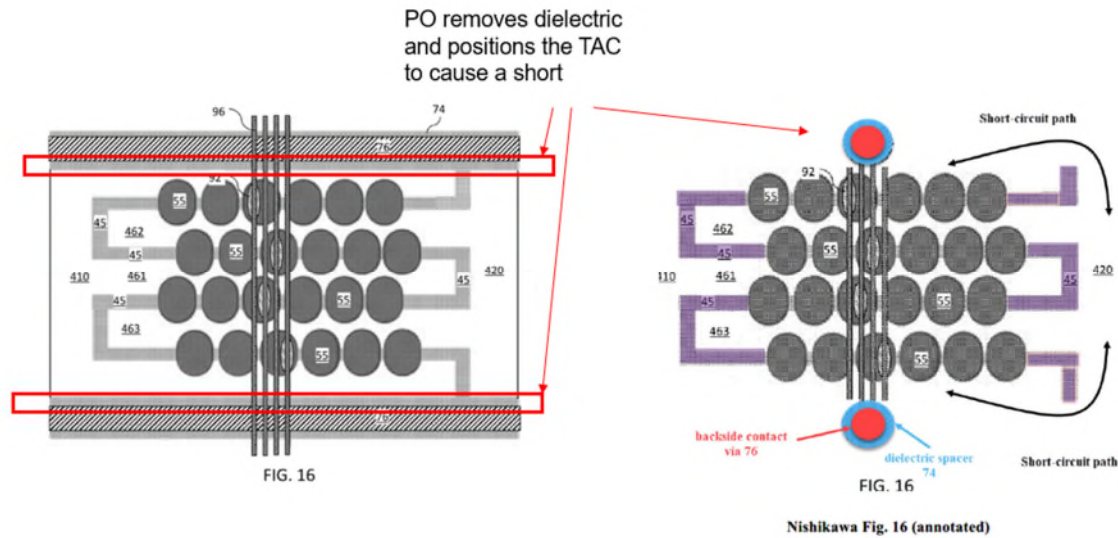
A. A Circular TAC Was Obvious

The Board correctly found, in the ID, that both Nishikawa and Nishikawa-Nishikawa2 render obvious a TAC having a “substantially circular section,” given (1) prior art teachings which demonstrate that a circular TAC was a suitable option for Nishikawa’s trench contact, and (2) Nishikawa2’s express statement that the trench contact can be “circular.” ID, 13-18.

1. A Circular TAC Would Not Render Nishikawa Inoperable

PO regurgitates its argument that a circular TAC would be inoperable in Nishikawa due to “short circuits.” POPR, 22-30; POR 11-24.

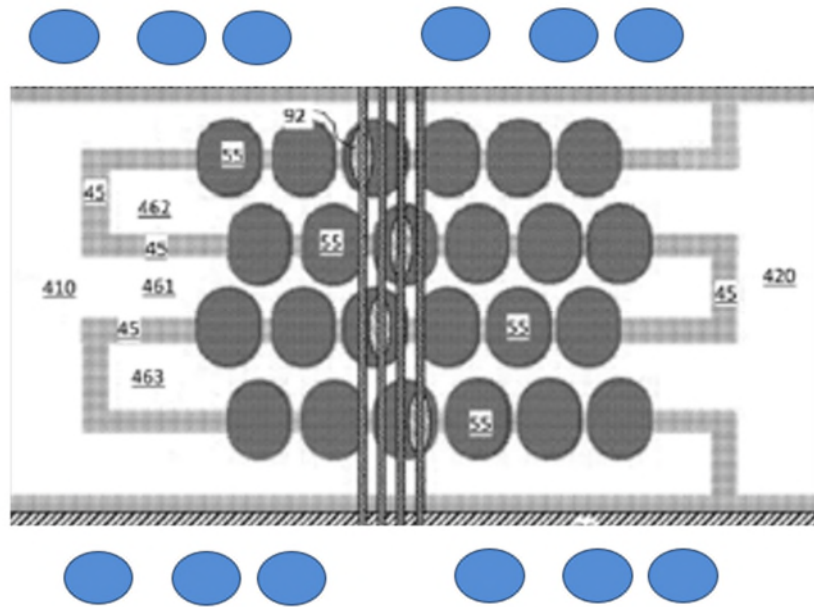
PO’s inoperability argument relies on a modification to Nishikawa (below) of its own making. The modification is not found in the Petition, and its own expert, Dr. Campbell, says “[a] POSITA would not” modify Nishikawa in this way because it would not provide “isolation between 420 and 410” (i.e., it would short them). EX1106, 73:22-74:9; POR 17-18. Thus, PO’s inoperability argument fails, because it is based on a modification to Nishikawa that its own expert confirms no POSITA would implement.



POR, 18 (right)¹; Lee2, ¶¶8-9.

The Petition advances an obviousness ground in which the separator “split[s] the memory stack into two regions (410 and 420).” Pet. 53-57. This is the function of the separator: “the separator dielectric structures 45 can laterally separate various portions of the alternating stack (32, 42).” Nishikawa, 8:33-35. Accordingly, instead of doing what Dr. Campbell concedes a POSITA would not do, the Petition shows that a POSITA would, e.g., implement the circular TACs with the separator providing the isolation:

¹ All annotation and emphasis added.



Nishikawa, Fig. 16; Lee2, ¶10.²

PO suggests that the obviousness ground cannot include horizontal separators 45 to isolate the wordline sets, because these separators are, instead, the spacers (74) for the trench (76):

² The memory device may include multiple instances of this block. *E.g.*, Nishikawa2, Fig. 14B; Lee2, ¶11.

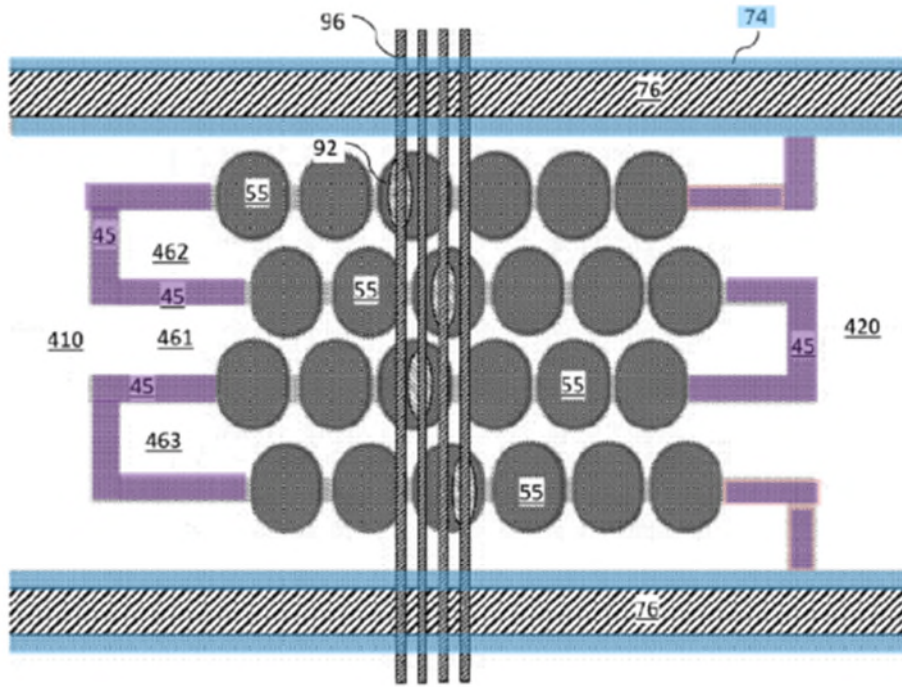
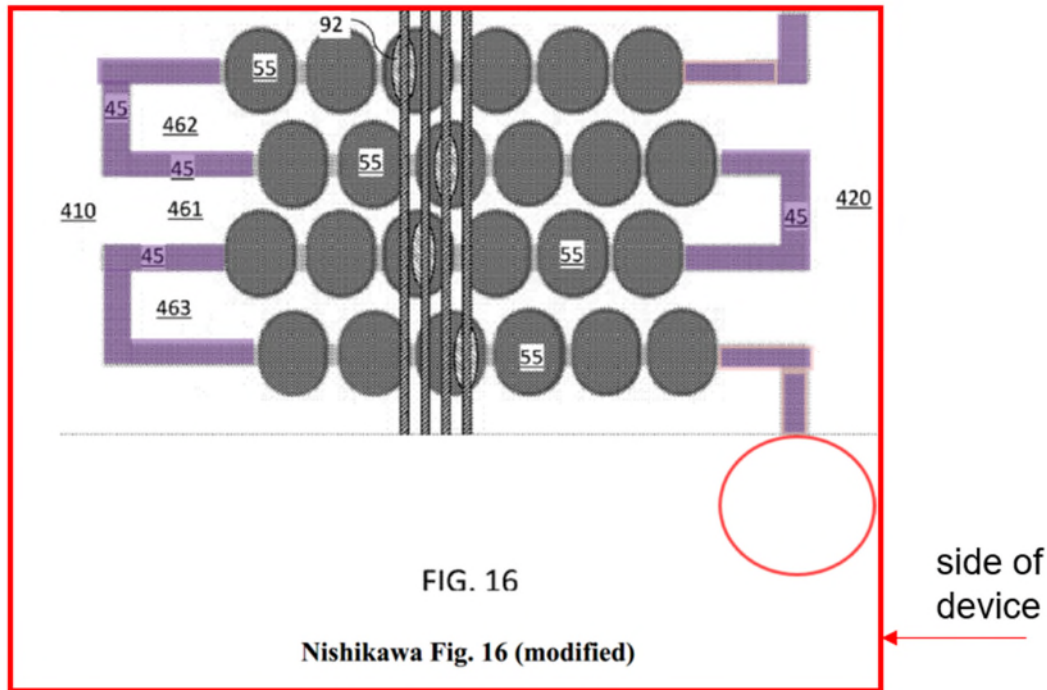


FIG. 16

Nishikawa Fig. 16 (annotated)

POR, 20. This argument misses the mark. First, PO misinterprets Nishikawa, which states that the separators 45 “laterally separate the control gates,” i.e., dielectric separators include the top and bottom portions because they laterally separate gate sets. Nishikawa, 17:14-23. Second, even if PO were correct, the argument attacks a strawman: the combination a separator that isolates, e.g., one that includes horizontal portions. Again, Nishikawa teaches separating the sets 410 and 420, and Dr. Campbell admits no POSITA would short 410 and 420 contrary to Nishikawa’s express guidance. EX1106, 73:22-74:9; Lee2, ¶12.

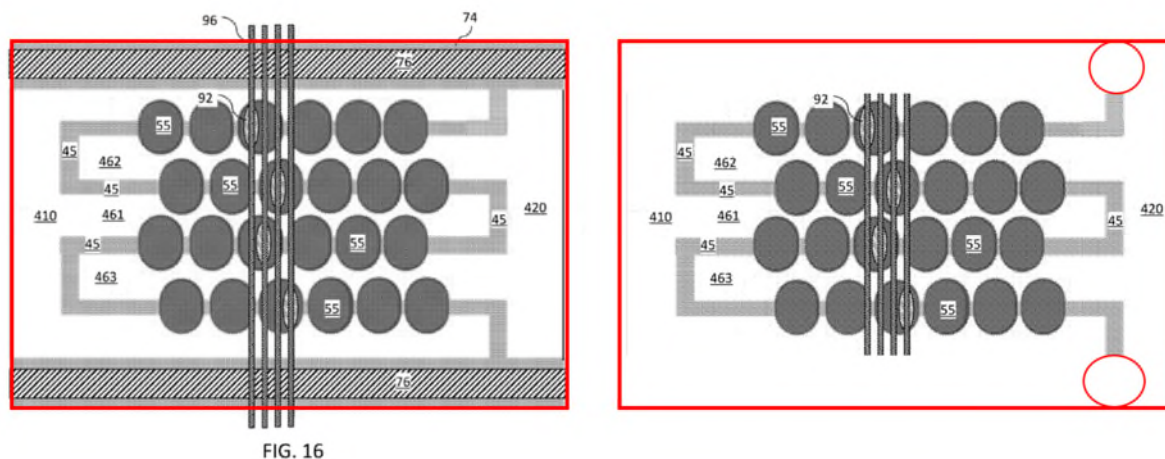
The numerous *operable* implementations of circular TACs are apparent from POR's own example that positions the circular TAC against the side of the device to isolate the gate sets:



POR 22 (with Petitioner's annotations).³ PO only argues that its footprint would be too big. *Id.*, 22-23. Dr. Campbell again would not defend PO's position, admitting

³ *Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.* is inapposite. POR, 23 n.2; 853 F.3d 1272, 1286 (Fed. Cir. 2017). There, the Reply used new references for the first time to argue that a limitation was disclosed and obvious, whereas here, the Reply rebuts inoperability arguments raised in the POR. *Idemitsu Kosan Co., Ltd. v. SFC*

that this arrangement need not increase footprint. EX1106, 74:10-17, 82:18-84:12. This is because, the circular TACs would be positioned at the edge of the device (e.g., where the trenches were) and isolate the two sides—all while *not* increasing the footprint:



Nishikawa, Fig. 16; Lee2, ¶13.

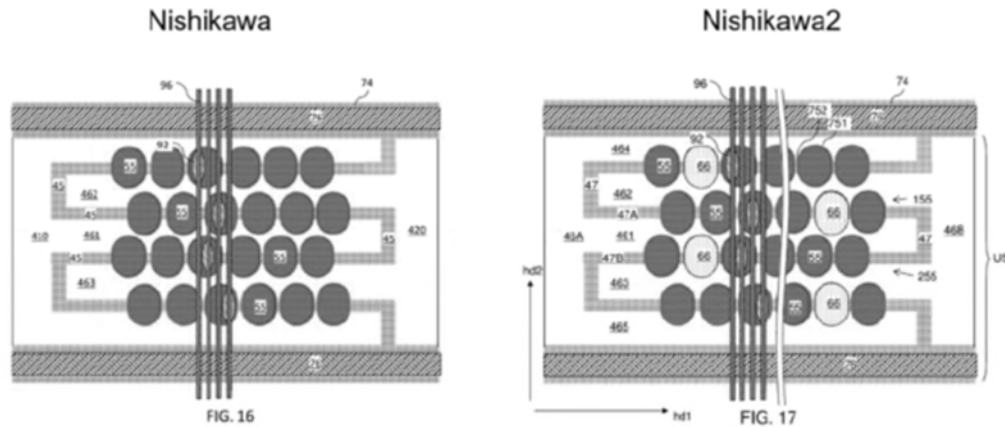
Notably, Nishikawa2’s “circular” TAC statement confirms a circular TAC does not create an inoperable device. *Infra*, §IIA.2.

2. Nishikawa2’s Circular TAC Disclosure Is Relevant to Nishikawa

The similarities in architecture between Nishikawa and Nishikawa2 would motivate a POSITA to consider Nishikawa2’s statement that the TAC “can have any

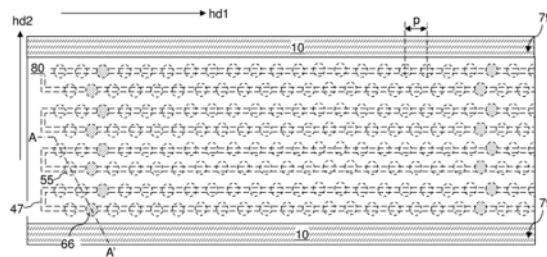
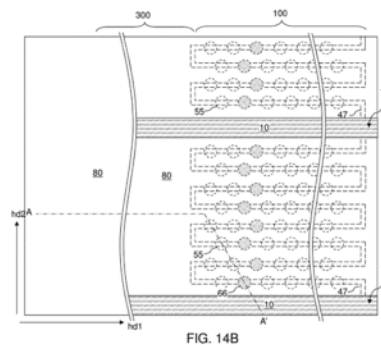
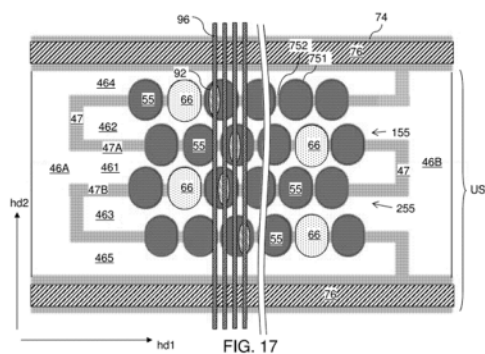
Co., Ltd., 870 F.3d 1376, 1380-81 (Fed. Cir. 2017) (petitioner may refute PO’s claims that a combination would lack a reasonable expectation of success with new argument and evidence in a reply brief).

suitable shape, such as *circular*,” to improve Nishikawa. Pet., 99 (Nishikawa2, 22:38-39).



Nishikawa, Fig. 16; Nishikawa2, Fig. 17; Lee, ¶ 115.

Pet., 44. PO argues that Nishikawa2’s circular TAC statement is not applicable to Nishikawa, apparently because (1) Nishikawa2’s statement appears in the context of its Figures 14A-C, and (2) the two sets of comb-shaped wordlines (46A and 46B) distinguish its Figure 17 from its Figure 14A-C. POR, 24-27. PO does not dispute that if the circular TAC statement is applicable to Nishikawa2’s Figure 17, then the statement would be applicable to Nishikawa. It is. As shown below, both Figure 17 and Figures 14A-C include comb-shaped sets of wordlines:



Nishikawa2, Figs. 14B-C, 17.

Notably, Dr. Campbell was unwilling to testify that Nishikawa2's Figure 17 is "a separate embodiment from Figure 14." EX1106, 100:22-101:3. Figures 14A-C focus on the device while there are trench openings 79. Nishikawa2, 22:34-23:43. Figure 15 focuses on the backside contact structures in the trench openings. *Id.*, 23:44-52. Figure 16 focuses on additional contact structures. *Id.*, 24:53-64. "Fig.17 is a see-through top-down view in which dielectric material layers overlying a topmost electrically conductive layer 46 have been omitted for clarity," focusing on how conductive layer 46 is split into the comb shapes. *Id.*, 24:65-67. Figures 14A-C, of course, include the top dielectric layers (80) and, notably, the same conductive layer 46 that Figure 17 is describing. *Id.*, 22:34-59. Put simply, Figure 17 is

describing the view under Figures 14's top dielectric layers (80). *Id.*, 24:65-67, 25:36-55. The common numerals among the figures confirm that they are referring to the same structures. 37 CFR 1.84(p)(4) ("same reference characters must never be used to designate different parts"); Lee2, ¶¶14-15.

Separately, PO argues that "trench-shaped" TACs "provide[] the necessary electrical isolation" in Figure 17. POR, 26. Nishikawa2 says such "trenches" are "optional." Nishikawa2, 25:39-49, 27:62. This is consistent with Figure 14's circular TAC statement. Lee2, ¶16.

3. PO Is Incorrect That Nishikawa and Nishikawa2 Are "Two Distinct Devices"

PO does not dispute that Nishikawa's Figure 16 and Nishikawa2's Figure 17 are the same architecture. And, as demonstrated above, PO is incorrect in asserting that Nishikawa2's Figures 14A-C represent a different architecture than Figure 17. Thus, PO's alleged "two distinct devices" argument (POR, 27-28) falls flat. Further, Dr. Campbell admits the obvious: that it is common for an author of a paper (here, Nishikawa) to write a follow-up paper (here, Nishikawa2) that "address[es] other aspects that weren't addressed in the first paper" (here, alternative shapes of Nishikawa's TAC). EX1106, 17:8-22; Lee2, ¶17.

4. PO Concedes Circular TAC Were Well Known and Suitable for Nishikawa's Trench Functions

PO does not contest that circular TACs were a well-known and suitable option for connecting structures through a memory stack. POR, 28-29; Pet., 41-52. Instead, PO raises only its failed inoperability argument against suitability. Thus, PO has no argument to rebut obviousness under the suitability precedent.

5. PO's Missing Limitation Arguments Fail

All of PO's "missing limitations" arguments fail.

First, *Qualcomm Inc. v. Apple Inc.* merely stands for the proposition that a ground must be based on prior art. 24 F.4th 1367, 1373-75 (Fed. Cir. 2022); POR, 29. The Grounds in this Petition all include at least Nishikawa.

Second, PO's citation to the September 2025 memo (POR, 29-30) fails, because it does not govern this proceeding and because it takes issue only with gap filling that does not rely on references (unlike the Petition here).

Third, there is no "missing limitation," because Nishikawa² and other references disclose a circular TAC. As the Board already held, the "missing limitation" line of cases applies "when dealing with a limitation missing from the prior art references" altogether and the petitioner is relying only on "ordinary creativity." ID., 14.

Fourth, even if there were a "missing limitation," the Petition provides thorough evidence that implementing a circular TAC was simple, had several

benefits, and was a more than suitable option. Nishikawa2’s statement that Nishikawa’s TAC could be circular, along with its limited description of that option, demonstrates that a POSITA knew how to implement it. *Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1339 (Fed. Cir. 2020) (silence about implementation shows a POSITA “was more than capable of selecting between the[se] known methods...”); *Epistar Corp. v. ITC*, 566 F.3d 1321, 1336 (Fed. Cir. 2009) (“[a] patent ... preferably omits[] what is well known in the art”). Next, the Petition discusses several references that teach circular TACs, was suitable for Nishikawa’s purposes, and had benefits. Pet., 44-52.

At bottom, PO’s arguments amount to arguing that semiconductor fabrication is complex. POR, 29-35. Yet a POSITA was already designing 3D memories and certainly would have been able to implement textbook contacts. Pet., 44-50; Lee2, ¶¶19-21.

B. The Addition of Dummy Channels In Nishikawa Was Obvious

Respectfully, the ID applies an overly restrictive obviousness standard in preliminarily finding the addition of dummy channels not obvious. ID, 18-20. “A party is not rigidly required to show an improvement or benefit in combining prior art references in a ‘categorical sense’ in order to show a motivation to combine.” *Cisco Sys., Inc. v. K.Mizra LLC*, 2024 U.S. App. LEXIS 20720, *9-10 (Fed. Cir. Aug. 16, 2024). Indeed, where there is a known problem, obviousness requires only

evidence of, e.g., a “known” or “suitable” option to address that problem. *Id.* (“known”); *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. 2023) (“suitable”). As the Petition and Reply demonstrate, it is beyond dispute that (1) Nishikawa poses edge effect and stability problems, and (2) dummy channels were both a known and suitable option for addressing these problems.

1. A Suitable Solution to Edge Effects Was Dummy Channels

The Petition cites to EX1024, which explains that “it is *common* to refrain from using the cells at the array edge” because such cells are “subject to processing variations.” Pet., 60 (citing EX1024, 8:47-53). Using these—instead of leaving them as dummy cells—risks a defective device. EX1024, 8:47-9:16; Lee2, ¶¶22-23 (citing EX1107 to describe exemplary edge effects, e.g., scattering and diffraction effects).⁴ PO arguments to the contrary all fail.

First, PO suggests that edge effects are a problem only for 2D memory devices. POR, 42. This strains credibility. For example, Lee, filed the same day as the ’322 patent, states in the *background section*—in the context of “*conventional 3D memory device structure[s]*”—that due to “*defects at the edges* of the vertical memory array (e.g., commonly referred to as ‘*array edge effects*’),” “an *array of*

⁴ Dr. Lee’s explanation of edge effects also explains the need for a consistent, uniform pattern.

‘dummy’ pillars (e.g., dielectric pillars) is *conventionally provided between the vertical memory array and the opening to set the edges of the vertical memory array* back farther from the opening and mitigate the aforementioned damage.” EX1108, 1:41-63. There can be no dispute that a suitable option for dealing with edge effects in 3D memories is thus dummy channels. EX1109, [0026] (3D memory), [0033] (“Dummy material portions ... can be utilized to reduce undesired edge array effects”); EX1110, [0004], Fig. 3B, [0045] (“The edge region MEC2 of the memory cell region MEC may include a dummy channel region DM”), Fig. 1 (“DM” region). Lee2, ¶¶24-27.

Second, PO misstates Dr. Lee’s testimony, suggesting that Dr. Lee recognizes that dummies are later sacrificed. Not so. Dr. Lee cited EX1025 to demonstrate the general principle of edge effects. Lee, ¶141. As EX1024, 8:47-53 and the above references (EX1108-EX1110) demonstrate, the typical and *suitable option* was to refrain from using the channels at the edge during operation (rendering them dummy channels). EX1111, Fig. 4B (“DUMMY MH” with no wiring); Lee2, ¶¶28-29.

Third, PO argues that Petitioner cites nothing to support using dummies on the edge of the memory cell pattern. POR, 43. Not true. The Petition cites EX1024, 8:47-53, which discloses dummies “at the array edge.” Pet., 60. EX1108-EX1111

(*supra*) further demonstrate that a known way to counter the “edge effect” was to use dummies on the “edge.”⁵

Fourth, PO incorrectly argues that there is “no room” in Nishikawa for dummy channels. POR 45. Not so. There is always room for dummies on the edge, because those dummies are created by not using them in operation. EX1024, 8:47-53. And in any event, Nishikawa’s “drawings are not drawn to scale.” EX1005 3:53. It is a conceptual drawing of a handful of memory cells out of a device that has billions of such cells. EX1106, 60:22-61:2. Further, EX1108-EX1111 (*supra*) demonstrate that 3D memory devices such Nishikawa have plenty of “room” for dummy channels. *See also* §II.B.2; Lee2, ¶30.

Fifth, PO is incorrect that Petitioner relies on hindsight, as EX1014 and EX1108-EX1111 state that employing such dummies on the edge of the array was common.

⁵ PO’s argument that Kai, Kim559, and Park297 teach not to use dummies on the edge is incorrect. POR, 43. Each teaches dummies in the connection region (and regardless, the connection region abuts the array edge). Kim559, [0045]; Park297, 7:38-42; Kai, 9:45-48.

2. Dummy Channels Do Not Provide Only Redundant Support

PO argues that Nishikawa’s separator dielectric structures “already provide structural support,” rendering additional dummy channel support unnecessary. POR 36–40. This argument fails on multiple fronts.

First, while the separators provide proximate support, the separators are only in a small portion of Nishikawa’s device. The separator is only in a portion of the array:

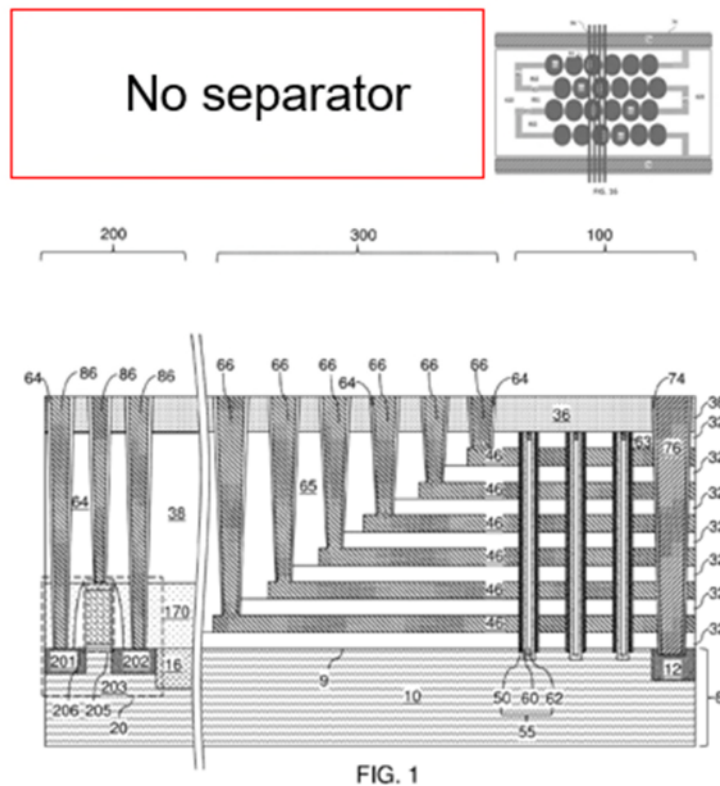


FIG. 1

Nishikawa, Figs. 1, 16. Nishikawa2 confirms the same:

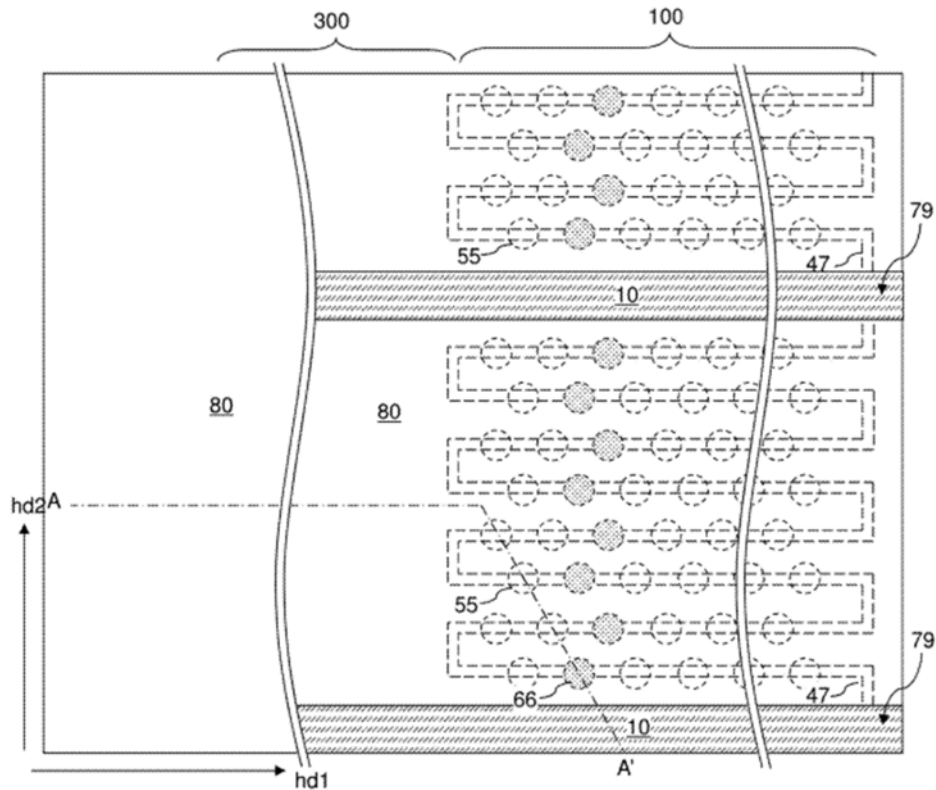
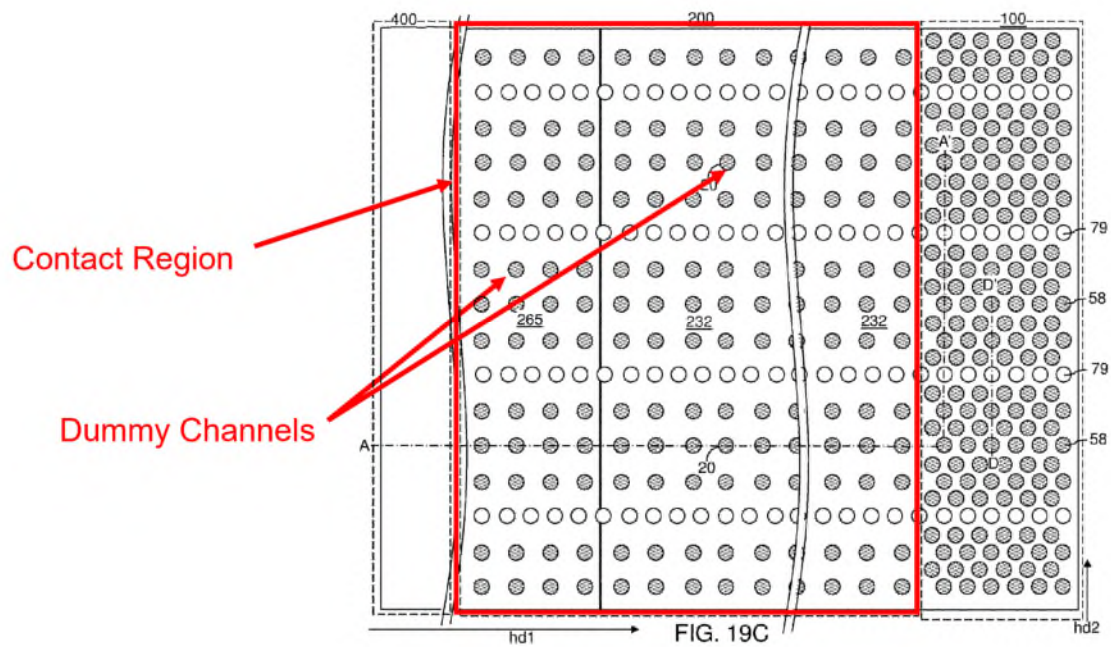


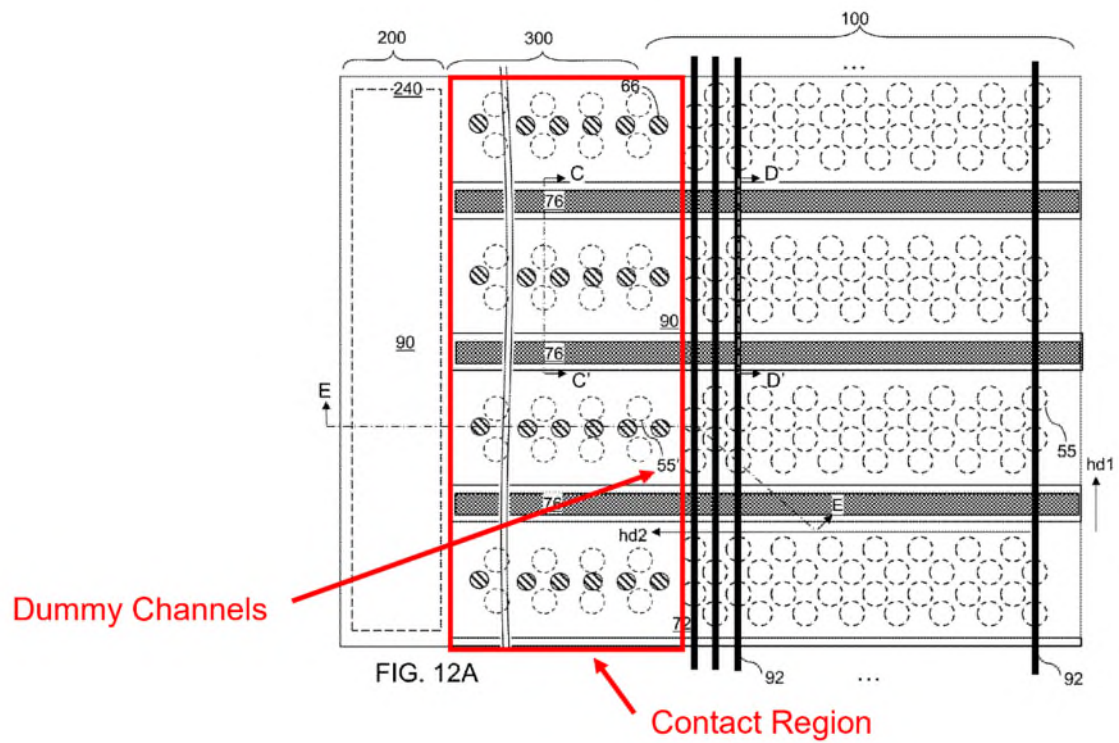
FIG. 14B

Nishikawa2, Fig. 14B; Lee2, ¶¶31-32.

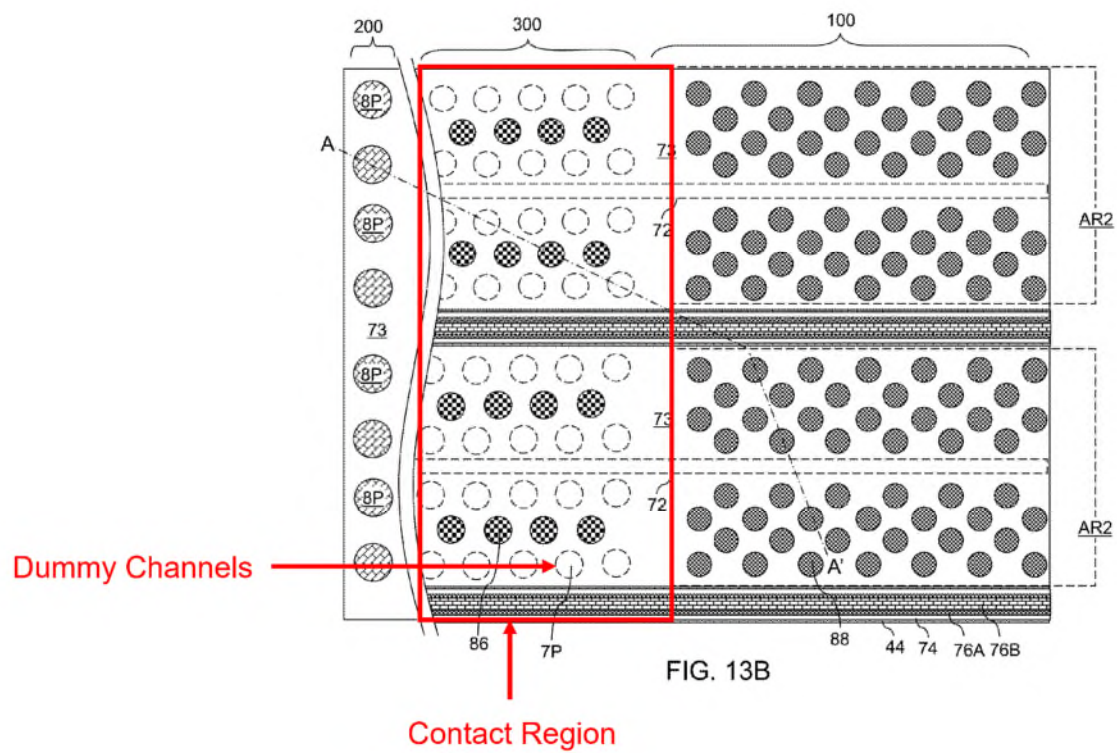
It was a conventional—and certainly a suitable—option to provide support *throughout the device* by including dummy channels from the edge of the array through the contact region to prevent collapse.



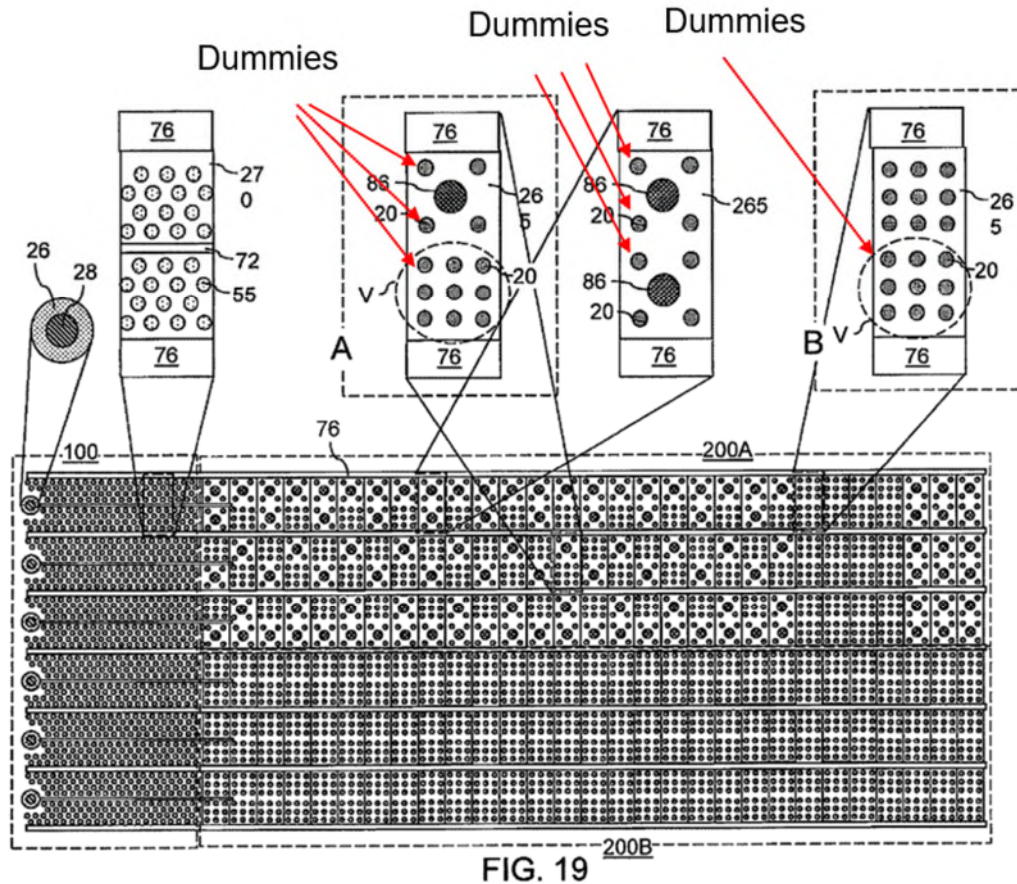
Iwai, Fig. 19C, 28:33-35.



Miyata, Fig. 12A, 44:37-40.



Mizutani, Fig. 13B, 16:38-51.



Masamori632, Fig. 19, 30:14-27. Moreover, Nishikawa was filed in 2015. As three-dimensional devices have scaled down, additional support structures were necessary to counter greater instability issues. Masamori, [0003]. Nishikawa was filed a few years after the earliest priority date of the '322 patent, and thus a POSITA also would have been motivated to include dummy channels in Nishikawa as it scaled to smaller sizes. Lee2, ¶¶36-37.

At bottom, there is nothing redundant or unnecessary about, and no serious tradeoff regarding, additional support structures (POR, 41), as dummy channels

avoid the edge effect and provide necessary support throughout the device. *See also* §II.B.4.

3. Apart from a Support Function, Dummies Improve the Gate Replacement Process

PO argues there is no reason to use dummy channels in Nishikawa. POR, 36. But PO wholly ignores the Petition's showing that aside from support, the memory holes (and dummy holes) alternatively are suitable for introducing the etchant and metal during gate replacement. Pet., 51. Nishikawa2 also expressly discloses using the dummy channel holes ("access openings")⁶ for this exact reason. Nishikawa2, 18:56-62. Further, the Petition demonstrates that it was known to include many such holes and spread them out to improve the gate replacement process. *Id.*, 51-52.

Notably, PO cannot be correct that there is no need for dummy channels when a device includes a separator, because Niskikawa2 includes both structures. Lee2, ¶¶38-39.

4. Alleged Disadvantages of Dummy Channels Do Not Render These Ubiquitous Structures Nonobvious

PO argues that adding dummy channels to Nishikawa would be nonobvious, because it would impact chip size, density, and/or cost. POR, 47-49. This argument

⁶ Nishikawa2 describes forming, e.g., dielectric pillars (66), that have the same volume as channels. Nishikawa2, 21:40-22:14, Fig. 14B.

fails, because the record demonstrates that a suitable option to mitigate edge effects and stability issues was to use dummy channels. *Supra*, §II.B.1-2. Moreover, because an array contains billions of active channels, and the edges and contact region would include but a fraction of this number. i.e., the impact is insignificant. Lee2, ¶¶41-42. In fact, PO cites Kim559 for support (POR, 48), yet Kim559 itself includes dummy channels (as PO admits elsewhere, POR, 43). Finally, Dr. Campbell admits that fabricating an operational device—a process that dummy channels facilitate by mitigating edge effects and preventing collapse—is of equal concern as density and size. EX1106, 139:18-140:19.

Next, PO argues that adding dummy channels introduces “processing risks.” POR 49-50. This argument fails, the prior art demonstrates that dummy channels were conventional and routine to fabricate (made just like regular channels) and reduce device defect risks. Lee2, ¶42.

5. Petitioner Did Not Improperly Supply Missing Limitations Using a POSITA’s Knowledge

PO argues that Petitioner improperly gap fills “missing limitations.” POR, 55-58. Again, this issue is not present here, because dummy channels were replete in the art—there is no missing limitation. Further, Petitioner’s citations are proper, because “the motivation to combine ... need not come from the references themselves.” *LKQ Corp. v. GM Glob. Tech. Operations LLC*, 102 F.4th 1280, 1299 (Fed. Cir. 2024).

PO's "general knowledge" arguments fail for two additional reasons. POR, 55-58. First, the dummy channel limitations are "peripheral limitations" to which the inquiry does not apply. *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1363 (Fed. Cir. 2016). The alleged invention is using TACs, not well known, conventional dummy channels. EX1001, 4:58-5:22. Second, PO ignores that the standard for assessing an "unusually simple" missing limitation is from a "skilled artisan[']s" perspective. *FullView, Inc. v. Polycom, Inc.*, 2024 WL 1843686, at *5 (Fed. Cir. Apr. 29, 2024). The record demonstrates that implementing dummy channels was routine—its just fabricating a channel structure and not wiring it.

Further, the '322 patent and the prior art contradict PO's arguments. The '322 patent (*e.g.*, 9:39-43) and the prior art (*supra*) do not address alleged difficulties in forming dummy channels. *Epistar*, 566 F.3d at 1336 ("[a] patent ... preferably omits[] what is well known in the art"); Lee2, ¶¶43-44.

6. The Board Should Disregard Dr. Campbell's Testimony Regarding Dummy Channels

Notably, the Board must disregard all of Dr. Campbell's testimony on issues pertaining to dummy channels. To start, Dr. Campbell admits that he has "no idea" what "edge effects" are—a conventional problem any POSITA knows. EX1106, 60:8-21, 109:23-110:15. Thus, Dr. Campbell does not have the knowledge to testify that dummy channels would or would not be suitable to address edge effects in Nishikawa, and testimony suggesting that a POSITA would not have had "edge

effects” concerns improperly contradicts the record. The Board “must disregard the testimony of an expert that is plainly inconsistent with the record.” *Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1378 (Fed. Cir. 2017).

C. A Ribbed TAC Was Obvious

Claims 13-18 and 20 (via claims 13 and 14), in effect, recite a ribbed TAC: the lateral diameter of the TAC corresponding to the conductive layers (gap 312) is wider than the lateral diameter corresponding to the dielectric layers (gap 304), forming a ribbed shape:

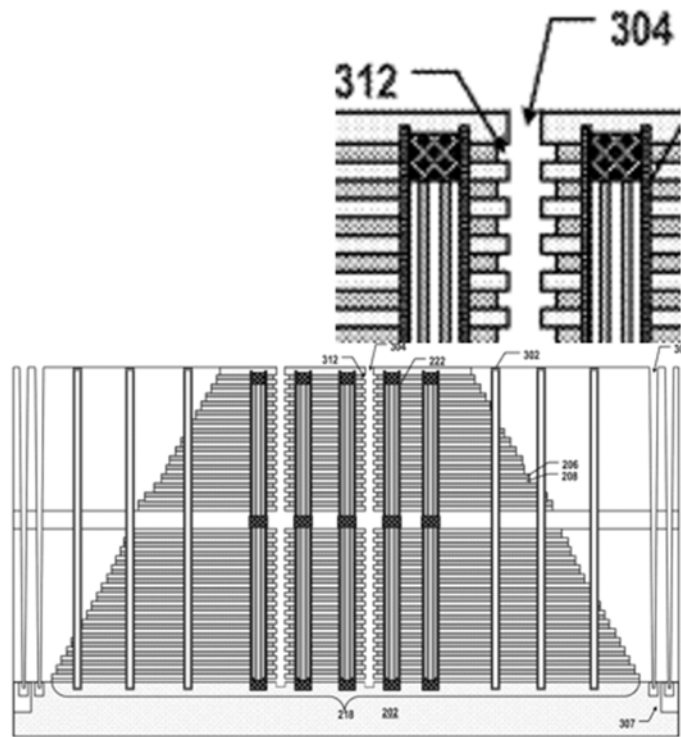


FIG. 3D

EX1001, Fig. 3D. Curiously, PO states that the relative width of these portions of the TAC would be understood to be met by a method step, namely, removing a

portion of the sacrificial layers (which become the conductive layers). POR, 59. The above figure represents the device after this removal step. PO likely advances this position to obfuscate that these lateral recesses are hardly visible in the final product due to a subsequent process step. As the '322 patent explains, after forming a spacer in the above TAC hole, a subsequent etch removes the bottom portion of the liner *and lateral portions of the spacer in the TAC hole*, leaving a largely undetectable wider lateral diameter of the TAC corresponding to the conductive layers:

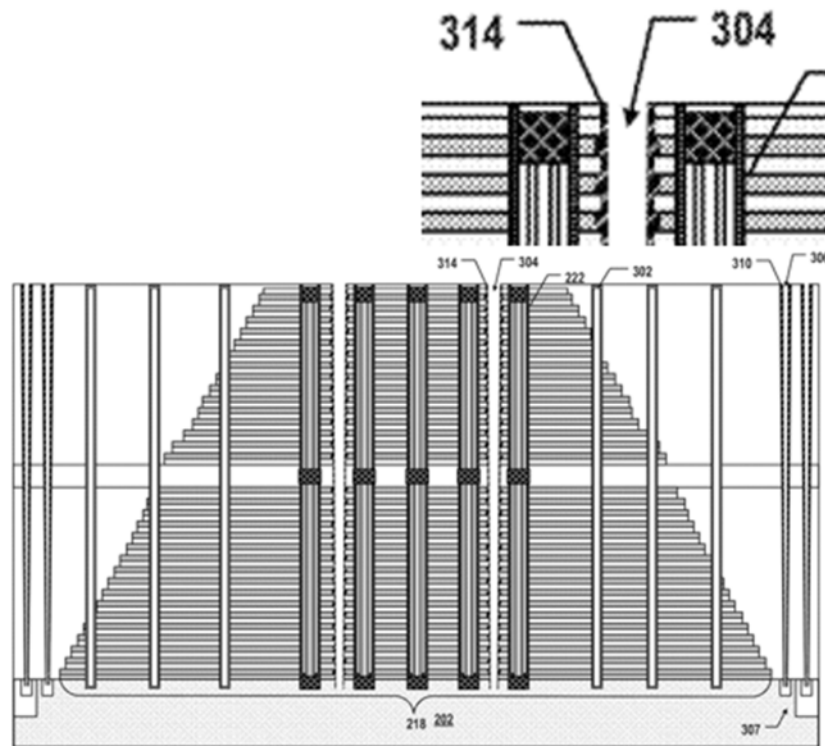


FIG. 3E

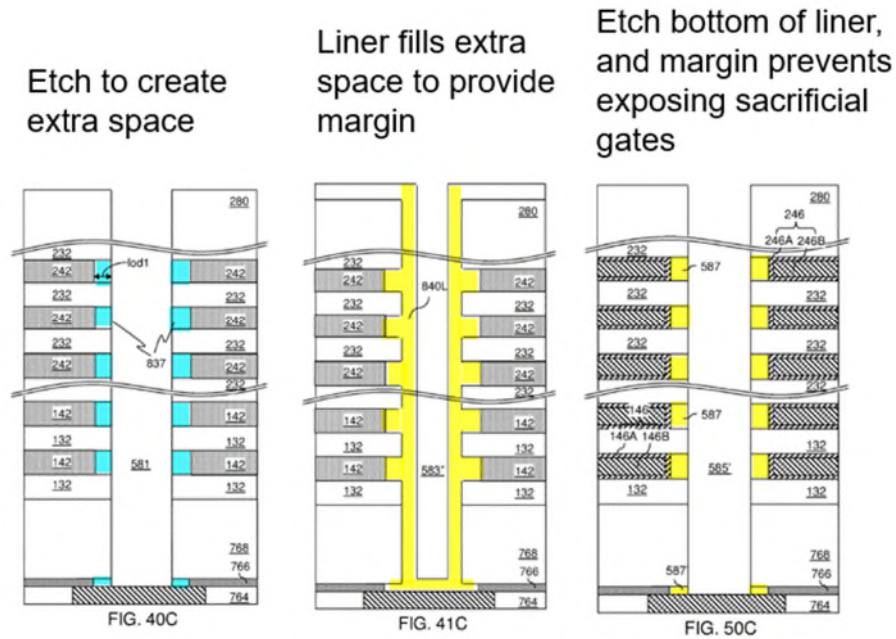
EX1001, Fig. 3D; Lee2, ¶¶45-46.

PO's omission of the full process is notable for two reasons. First, this process that creates extra room for dielectric material for the subsequent etch to avoid a short was extremely well known. Second, PO does not dispute that these limitations are met by a TAC that has a larger diameter corresponding to the conductive layers—albeit hardly detectable—than the diameter corresponding to the dielectric layers—that is, what the Petition calls PO's apparent construction. Pet., 74-75.

1. The Motivation of Providing Extra Room Was Extremely Well Known

The Petition demonstrates that under its construction (which PO does not dispute is outside the claim scope), a ribbed TAC was obvious, because the ribs create extra room for dielectric material. Pet., 75-76. PO merely feigns ignorance in stating that the Petition fails to provide a motivation, because (1) PO concedes that the Petition asserts the benefit of a ribbed TAC is providing additional room for the dielectric (POR 65-66), and (2) the Petition cites Cui's Figure 41 that demonstrates the reason for the extra room, i.e., to prevent shorting the conductive layers to the TAC (Pet., 76). Specifically, Figure 41 demonstrates that this additional room (*see* blue recesses at below-left and yellow spacer at below-middle) provides lateral margin for the etch that removes the bottom portion of the liner. Specifically, as shown below in the middle and right figures, etching the bottom portion can also etch the spacer on the side. If the recess did not have this additional dielectric, the etch could expose the sacrificial layers (which become the conductive gates),

resulting in short-circuits (because the TAC's core could then contact the conductive gates):



Cui, Figs. 40C, 41C, 50C, 44:55-45:25 (processing to form cavities), 45:46-60 (liner), 48:17-33 (etch of bottom liner). In other words, because of the margin, after filling the TAC hole, the conductive TAC core does not electrically short exposed conductive gate layers:

Lateral etching



FIG. 41C

Margin prevents exposing sacrificial gates

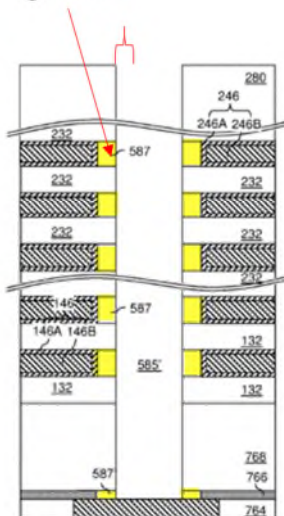


FIG. 50C

Fill 186 does not electrically connect conductive gates due to margin

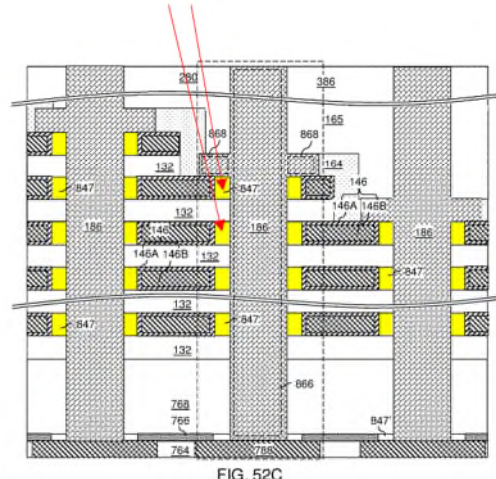


FIG. 52C

6ui, Figs. 41C, 50C, 52C, 49:16-52 (conductive fill) Lee2, ¶47. Indeed, PO does not dispute, nor can it, that ribbed TACs were extremely well-known and that Cui demonstrates why. Such recessing to avoid short circuits, or in other words, to increase leakage current suppression, was extremely well known. For example, Liu discloses recessing conductive layers to provide extra room for the dielectric liner, thereby isolating the conductive layers from the TACs and avoiding leakage current (i.e. shorting):

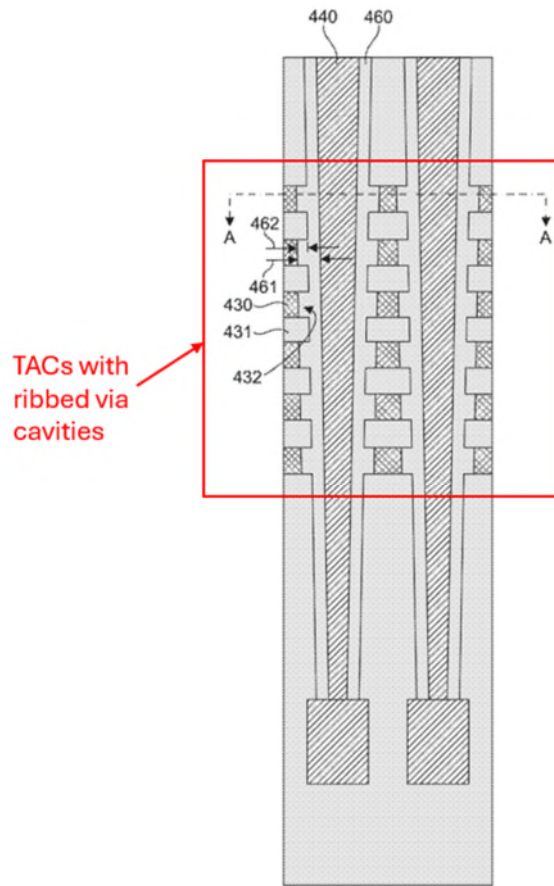


FIG. 7

Liu, [0048] (“conductive layers 430 can be recessed proximate contacts 440 such that material of insulative layers 431 is closer to the contacts 440 than the material of the conductive layers 430”). Notably, Liu discloses that “[r]ecesses can be included if additional isolation from the contacts 440 is desired” and “[i]n general, it is desirable to minimize capacitor coupling as much as possible.” *Id.* Thus, it is “desirable” to have the recess to minimize capacitor coupling. Lilak, too, recesses conductive gates to create a longer path between the vertical wordlines around the dielectric layers to avoid leakage current in a 3D memory.

Greater distance
path between
conductive wordlines

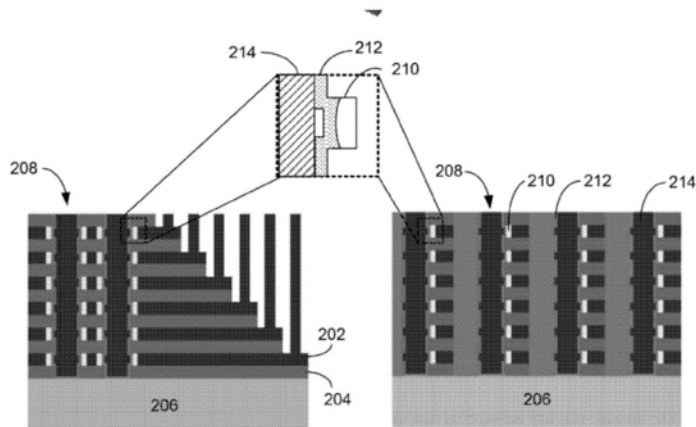
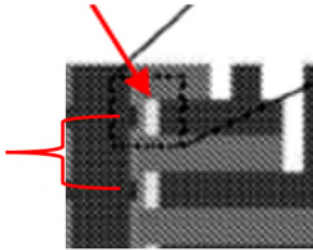


FIG. 2B

FIG. 2C

EX1116, 2B-2C, 7:12-17 (“Also, in the embodiment shown, the first conductive layers 202 are recessed from the etch pits 208 to increase leakage current suppression.”). Lee2, ¶¶48-50.

In sum, the record demonstrates that it was known that ribbed cavities create extra room to mitigate short-circuits and the capacitive coupling of conductor pairs. PO does not (and cannot) dispute that Nishikawa teaches a conductive TAC. Thus, the ribbed cavities provide a well-known technique to address a problem (possible short circuits and isolation) that Nishikawa indisputably has. As such, the ribbed cavities are obvious.

PO admits that the '322 patent fails to explain the point of the ribbed TAC. POR, 65. But PO's admission—along with Cui and the above references—proves obviousness, because the '322 patent's silence demonstrates that a POSITA “was more than capable of selecting between the[se] known methods...” *Uber Techs.*,

957 F.3d at 1339; *Epistar*, 566 F.3d at 1336 (“[a] patent ... preferably omits[] what is well known in the art”).⁷

2. A Ribbed Cavity Is Obvious Under Petitioner’s Construction

The Petition assumes that PO’s position is that unintentional recesses satisfy the claim language (Pet., 73-75), and PO did not dispute this in the POR. Thus, unless the Board reads an intent element into the limitation, unintentional recesses satisfy these limitations.⁸ This is an alternative basis to §II.C1’s basis on which to find the claims unpatentable.

PO is incorrect that Petitioner’s advances an inherency theory (POR, 61-62), admitting that Petitioner is advancing an obviousness theory elsewhere. POR, 63. Against this obviousness theory, PO’s only argument is that “[a] POSITA would have sought and used gases that can etch without selectivity” (i.e., leaving no ribs), providing one example of an etchant that allegedly accomplishes this. *Id.*, 64.

⁷ While PO downplays Kai (POR, 66), PO does not dispute that Kai teaches recessing the sacrificial gates (Kai, 11:9-14). This, in turn, demonstrates that recessing the sacrificial gates was routine.

⁸ PO cites a *Samsung* case for the proposition that the Board cannot rule under this construction. POR 60-61. That case deals with a failure to map a construction to the prior art and is thus inapposite.

Critically, PO does not dispute the Petition’s evidence that finding such an etchant was a “challenge.” Pet., 74 (citing EX1039). Thus, there is no dispute that most etchants result in unintentional recesses. Respectfully, the Board’s suggestion that Petitioner must prove a POSITA would seek this result is incorrect. Instead, the question is would using typical and obvious etchants result in unintentional recess? There is no dispute that the answer is yes, because it was a “challenge” to do the opposite. Thus, the result of forming Nishikawa’s TACs with typical and obvious etchants is unintentional recesses. Lee2, ¶51.

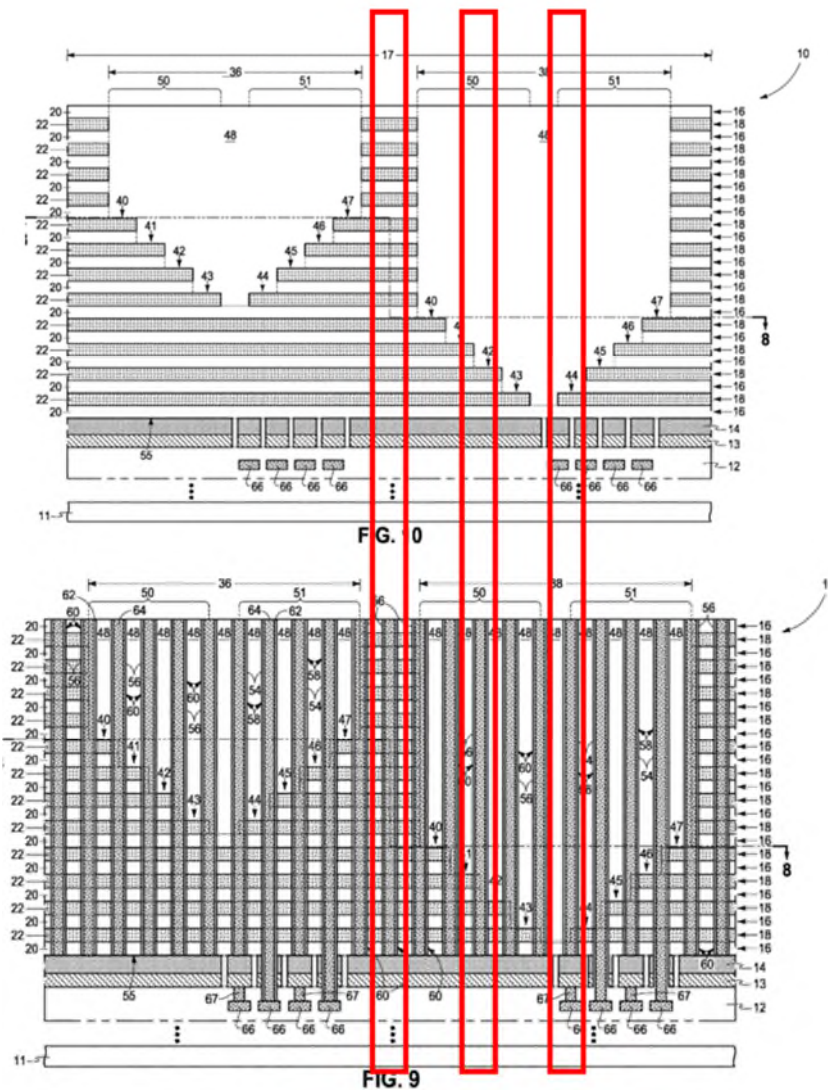
3. Petitioner Does Not Improperly Supply a Missing Limitation

PO’s “missing limitation” argument fails for the same reason as set forth in §II.A.5. POR, 67-68. There is no “missing limitation,” as, e.g., Cui discloses a ribbed TAC. Moreover, the claimed ribbed TAC is a peripheral limitation to which the inquiry does not apply. PO acknowledges the ’322 patent never mentions anything special about ribbed via cavities. POR, 65; EX1001, 13:61-63. There is nothing complex about what the ’322 patent assumes a POSITA would readily know how to implement. *FullView*, 2024 WL 1843686, at 5. Indeed, Liu describes ribbed TACs and smooth TACs side-by-side and does not describe any challenges to either. Liu, Figs. 6-7, [0047]-[0048]; Lee2, ¶¶52-53.

D. TACs And Peripheral Contacts With Equal Diameters Were Obvious

PO argues that it would not have been obvious to implement TACs with the same diameter as peripheral contacts. POR, 69-76. To start, all of PO's arguments fail, because PO ignores that it was textbook material to use the same diameters for different contacts, "overcome[ing]" the "problem" of over-etching contact holes and therefore was a "common" solution. EX1035, 33; Pet., 68. That's dispositive, because this common solution for 3D connections is necessarily obvious as a suitable and known technique. *Cisco*, 2024 U.S. App. LEXIS 20720, 9–10; *Intel*, 61 F.4th at 1381; Lee2 ¶55.

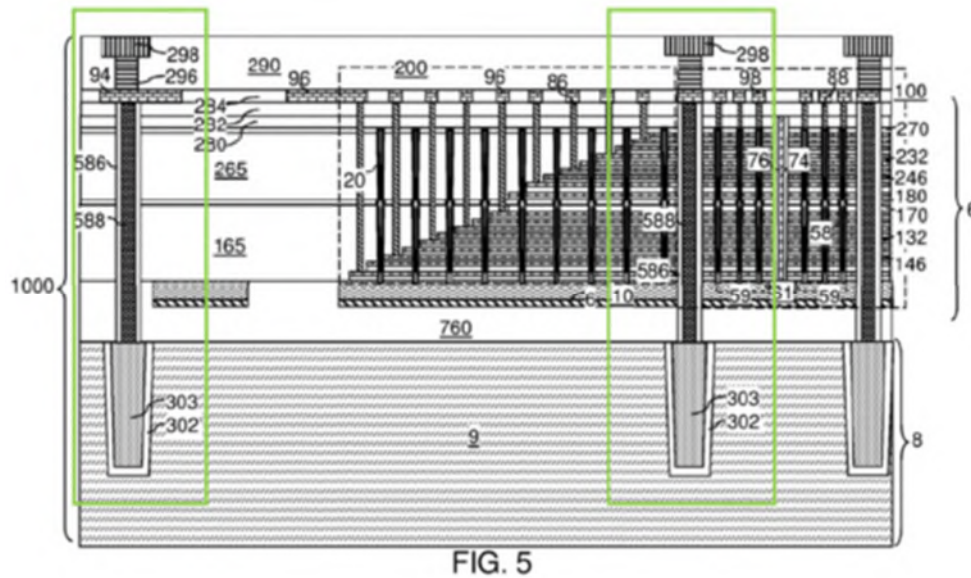
What PO does address is unavailing. Indeed, PO's arguments all suffer from a technical error that the record lays bare. PO's premise is that one cannot use a "common process" to form peripheral contacts and TACs, because the respective etches occur in different regions: *some through the stack and some through the dielectric fill*. POR, 74-75. This is incorrect. Tessariol states that the dummy and via openings are "simultaneously" formed. Tessariol, [0037]. These openings are formed *through the stack of alternating layers, through portions of the stack and portions of the dielectric fill, and through the dielectric fill* (or at best, partially through one layer of the stack), all in a single step and through this common etch:



Tessariol, Figs. 9, 10. Similarly, the contacts are “formed at the same time.” *Id.*, [0038]; Lee2, ¶56. Next, PO’s attempt to discount the relevance of figures disclosing peripheral contacts and TACs with the same diameters fails for at least three reasons. POR, 69-70. First, PO misinterprets *Nystrom*, where “[t]he Federal Circuit held that the speculative modeling premised on unstated assumptions in prior art patent drawings cannot be the basis for challenging the validity of claims *reciting*

specific dimensions not disclosed directly in such prior art.” IPR2024-00789, FWD (Paper 37) (10/23/2025) (citing *Nystrom v. TREX Co., Inc.*, 424 F.3d 1136, 1148 (Fed. Cir. 2005)). Specific dimensions, e.g., 10nm, are not at issue here. *See id.* Second, even if precise dimensions were at issue (they are not), Patent Owner provides only part of the legal rule: “[P]atent drawings do not define the precise proportions of the elements ... *if the specification is completely silent on the issue.*” *Nystrom*, 424 F.3d at 1149. Here, the written description confirms that the patent drawings in Nakajima and Mushiga disclose TACs and peripheral contacts with the same diameters. Specifically, Mushiga discloses forming its through-array contacts using the same processing steps at the same time. Mushiga, 10:31-58; *see* Lee, ¶¶160-161. Likewise, Nakajima discloses forming all of its through-array contacts via the same process. Nakajima, 7:37-8:11; Lee, ¶161. And this description is consistent with using the same diameter to avoid over-etching issues. EX1035, 33; Pet. 68. PO’s contention that Micron’s assertions rely solely on figures is incorrect. POR, 69. Instead, Micron contends that a skilled artisan would have read Mushiga and Nakajima to disclose contacts of the same size based on how the references describe those contacts as being processed. *See Paice LLC v. Ford Motor Co.*, 722 F. App’x 1015, 1022 (Fed. Cir. 2018) (affirming obviousness based on what a

“skilled artisan would understand” a figure to disclose).⁹ Third, CFR 1.84(p)(4) mandates that the same numerals in figures denote the same structures, and thus the art, e.g., Mushiga, is depicting peripheral contacts and TACs (both 586) with the same diameters:



Mushiga, Fig. 5; Lee2, ¶57.

⁹ PO again misrepresents the record when it alleges that Petitioner “makes the same mistake” in relying only on a figure for limitation 6.D (POR 70, n.14). Instead, the Petition cites EX1010 and Dr. Lee’s explanation to explain the figure. Pet., 70-71. PO appears to insinuate the same as to claims 9-10 (POR, 71, n.15), again failing to note that Dr. Lee explains that using the same process, with the same hole size, results in the same spacer thickness (Pet., 79-81).

Next, PO is incorrect that Mushiga does not form the contacts of the same size (at the same time with the same process step). POR, 71. Mushiga consistently refers to single steps in forming the contacts: “cavities can be formed,” “spacer material layer can be conformally deposited and anisotropically etched,” and “conductive material filler ... deposited in the remaining volumes to form through-memory-level via structures 588.” Mushiga, 10:31-58. And Mushiga labels both the peripheral contact and TAC with “586.” Lee2, ¶58.

Similarly, PO is incorrect that Nakajima incorrectly labels the C4 contact shown below on the right and therefore Nakajima does not disclose a C4 contact that is outside the stack (i.e., outside the gate alternating gate-dielectric layers). PO raises this alleged error to argue that Nakajima does not form contacts inside and outside the stack with the same C4 process. POR, 72-73.

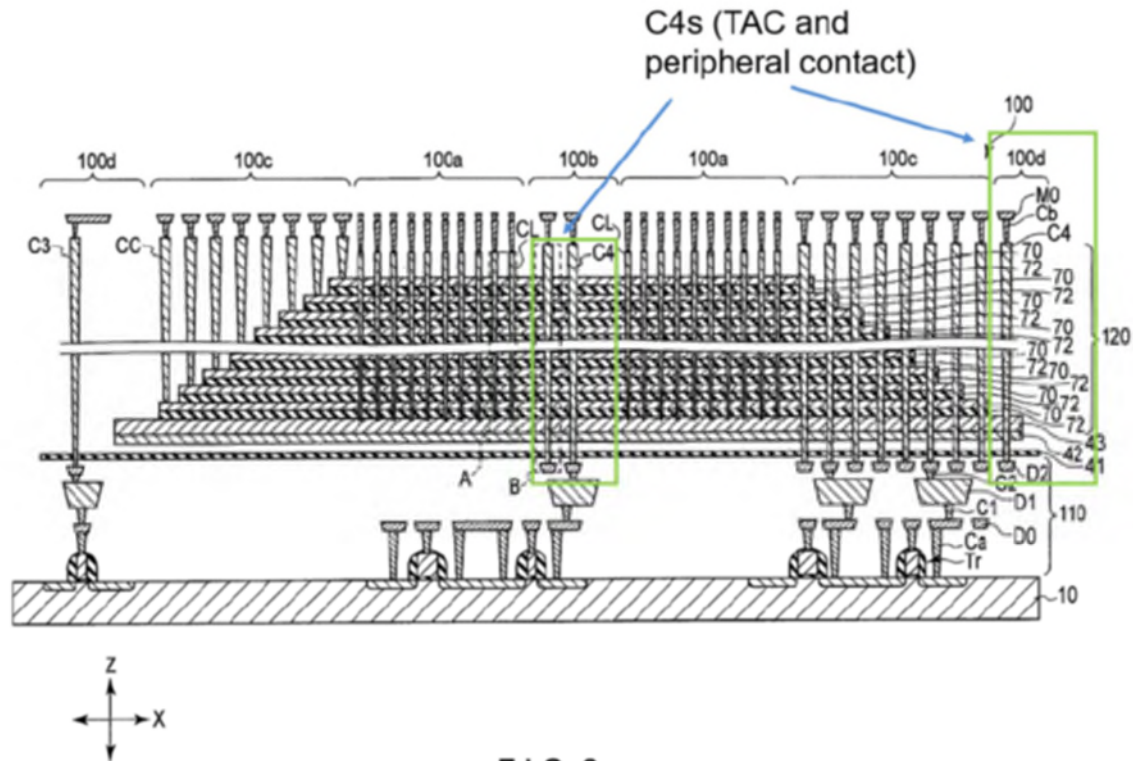


FIG. 2

Nakajima, Fig. 2. First, note that the C4 on the right extends through the substrate, like all other C4s—whereas the C3 on left does not. Thus, a POSITA would not consider the consistent labeling of these C4s to be in error. Second, PO makes much ado about the difference between C4s allegedly going through all the dielectric-gate layer pairs, while the C3s go through only the dielectric. POR, 72. This is incorrect. As shown below, some C4s extend through all the dielectric-gate pairs, some extend through dielectric and only some pairs, and some extend through only the dielectric (or at best, through one layer of the pairs):

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Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing Petitioner's Reply Brief complies with the word count limits set forth in 37 C.F.R. §42.24(a)(1)(i). Excluding the parts of the Petition exempted by 37 C.F.R. §42.24(a)(1), this Reply contains 5,526 words as determined using the word count feature in Microsoft Word, which was used to prepare this Reply.

Dated: February 9, 2026

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing paper was caused to be served on February 9, 2026 via electronic mail, upon the following attorneys of record for the Patent Owner

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