

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00191
U.S. Patent No. 11,581,322

REPLY DECLARATION OF DR. JACK C. LEE

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TABLE OF ABBREVIATIONS

ABBREVIATION	TERM
'322 patent	U.S. Patent No. 11,581,322 (EX1001)
Cui	U.S. Patent No. 10,304,852 (EX1037)
Iwai	U.S. Patent No. 10,347,654 (EX1022)
Iwai737	U.S. Patent No. 10,347,654 (EX1111)
Kai	U.S. Patent No. 10,290,643 (EX1027)
Kim559	U.S. Patent Publication No. 2018/0308559 (EX1029)
Kwon	U.S. Patent Publication No. 2019/035942A1 (EX1114)
Masamori	U.S. Patent Publication No. 2018/0301374A1 (EX1020)
Liu	U.S. Patent Publication No. 2018/0190540 (EX1115)
Masamori632	U.S. Patent No. 10,115,632 (EX1031)
Miyata	U.S. Patent No. 9,449,987 (EX1112)
Mizutani	U.S. Patent No. 9,929,174 (EX1113)
Mushiga	U.S. Patent No. 10,354,980 (EX1012)
Nakajima	U.S. Patent No. 10,777,501 (EX1009)
Nishikawa	U.S. Patent No. 9,837,431 (EX1005)
Nishikawa2	U.S. Patent No. 9,935,123 (EX1046)
Park297	U.S. Patent No. 9,859,297 (EX1028)
Tessariol	U.S. Patent Publication No. 2019/0081061 (EX1036)
ID	Decision Granting Institution of <i>Inter Partes</i> Review (Paper 22)

ABBREVIATION	TERM
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,581,322 (Paper 1)
Petitioner	Micron Technology, Inc.
PO or Patent Owner	Yangtze Memory Technologies Co. Ltd.
POPR	Patent Owner's Preliminary Response (Paper 12)
POR	Patent Owner's Response (Paper 34)

I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron” or “Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to reply to certain of the positions set forth in Patent Owner’s Response (Paper 34) and opinions in a November 17, 2025 declaration of Stephen Campbell (EX2021), submitted by Patent Owner in an *inter partes* review proceeding relating to U.S. Patent No. 11,581,322, which I refer to herein as the ’322 patent.

3. I am being compensated at my current standard consulting rate, plus reimbursement for any reasonable expenses. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

4. The prior declaration I submitted in connection with this proceeding, which I understand has been designated as Exhibit 1003, sets forth among other topics my educational background and professional experience (EX1003, ¶¶5-13

and associated Exhibit 1004), my understanding of the law (*id.*, ¶¶18-33), an overview of pertinent technical background (*id.*, ¶¶39-58), an overview of the '322 patent and its prosecution history (*id.*, ¶¶59-76), the knowledge and characteristics of a person having ordinary skill in the art (*id.*, ¶¶34-38), and certain claim construction opinions (*id.*, ¶¶77-80).

5. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, my work with those of ordinary skill at the time of the alleged invention, and my general experience in the field of art.

6. I have also reviewed and considered the materials listed in my prior declaration (EX1003, ¶17), the Board's Institution Decision (Paper 22), Patent Owner's Response (Paper 34), the transcript of my deposition in this proceeding (EX2038), the Campbell Declaration (EX2021) (and the exhibits that he discusses in his declaration), and the following materials to the extent relevant to my opinions:

Exhibit	Description
1001	U.S. Patent No. 11,581,322 to Guo et al. ("322 patent")
1002	File History of U.S. Patent No. 11,581,322 ("322 FH")
1003	Declaration of Dr. Jack C. Lee
1005	U.S. Patent No. 9,837,431 to Nishikawa et al. ("Nishikawa")
1006	U.S. Patent No. 9,853,046 to Lu et al. ("Lu")

Exhibit	Description
1007	U.S. Patent No. 10,658,378 to Tao et al.
1008	U.S. Patent Publication No. 2019/0229125A1 to Zhou et al.
1009	U.S. Patent No. 10,777,501 to Nakajima et al. (“Nakajima”)
1010	Michelsoni, “3D Flash Memories” (2016)
1011	U.S. Patent Publication No. 2017/0179026 A1 to Toyama et al.
1012	U.S. Patent No. 10,354,980 to Mushiga et al. (“Mushiga”)
1013	PCT Publication No. WO 2019/042103A1 to Dai et al.
1014	U.S. Patent No.10,679,721 to Kim et al.
1015	Aritome, “NAND Flash Memory Technologies”
1016	File History for U.S. Patent Application No. 16/745,342
1017	U.S. Patent Publication No. 2012/0280304A1 to Lee et al. (“Lee304”)
1018	U.S. Patent Publication No. 2017/0125430A1 to Nishikawa et al. (“Nishikawa430”)
1019	U.S. Patent Publication No. 2015/0348987A1 to Lee et al. (“Lee987”)
1020	U.S. Patent Publication No. 2018/0301374A1 to Masamori et al. (“Masamori”)
1021	U.S. Patent No. 8,107,292 to Maejima
1022	U.S. Patent No. 10,347,654 to Iwai et al. (“Iwai”)
1023	U.S. Patent No. 10,559,583 to Park et al.
1024	U.S. Patent No. 5,945,717 to Chevallier
1025	U.S. Patent No. 10,347,487 to Lee et al.

Exhibit	Description
1026	Ronse, “Optical lithography—a historical perspective,” C. R. Physique 7 (2006)
1027	U.S. Patent No. 10,290,643 to Kai et al. (“Kai”)
1028	U.S. Patent No. 9,859,297 to Park et al. (“Park297”)
1029	U.S. Patent Publication No. 2018/0308559 to Kim et al. (“Kim559”)
1030	U.S. Patent No. 8,945,996 to Tang et al.
1031	U.S. Patent No. 10,115,632 to Masamori et al. (“Masamori632”)
1032	U.S. Patent No. 10,879,254 to Guo et al.
1033	U.S. Patent No. 9,793,139 to Sharangpani et al.
1034	Excerpts from Wolf, “Silicon Processing for the VLSI Era, Volume 1-Process Technology,” Lattice Press (1986) (“Wolf Vol. 1”)
1035	Excerpts from Wolf, “Silicon Processing for the VLSI Era, Volume 2-Process Integration,” Lattice Press (1990) (“Wolf Vol. 2”)
1036	U.S. Patent Publication No. 2019/0081061 to Tessariol et al. (“Tessariol”)
1037	U.S. Patent No. 10,304,852 to Cui et al. (“Cui”)
1038	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,879,254 (Ex. B-1 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) (“Ex. B-1, YMTC’s Contentions”) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1039	U.S. Patent No. 11,075,084 to Shen et al.
1040	U.S. Patent No. 10,504,596 to Goda et al.

Exhibit	Description
1041	U.S. Patent No. 10,381,369 to Kim et al. (“Kim369”)
1046	U.S. Patent No. 9,935,123 to Nishikawa (“Nishikawa2”)
1047	Printout, 11/26/2024, Britannica (https://www.britannica.com/science/geometry) (ellipse)
1106	Transcript of the Deposition of Stephen Campbell, taken January 23, 2026, <i>Micron Tech. Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00191
1107	Additional excerpts from Wolf, “Silicon Processing for the VLSI Era, Volume 1-Process Technology,” Lattice Press (1986)
1108	U.S. Patent No. 11,043,507
1109	U.S. Patent Publication No. 2015/0029775A1
1110	U.S. Patent Publication No. 2019/0027434A1
1111	U.S. Patent No. 10,115,737 (“Iwai737”)
1112	U.S. Patent No. 9,449,987 (“Miyata”)
1113	U.S. Patent No. 9,929,174 (“Mizutani”)
1114	U.S. Patent Publication No. 2019/035942A1 (“Kwon”)
1115	U.S. Patent Publication No. 2018/0190540 (“Liu”)
1116	PCT Publication No. WO 2019/066829A1
2021	Declaration of Stephen Campbell in Support of Patent Owner’s Response
2030	Yongsik Yu, Tech Brief: Memory “Grows Up” with 3D NAND, Lam Rsch. Newsroom (Apr. 11, 2016), https://newsroom.lamresearch.com/Tech-Brief-Memory-Grows-Upwith-3D-NAND

Exhibit	Description
2038	Transcript of the Deposition of Jack C. Lee, Ph.D., taken October 23, 2025, <i>Micron Tech. Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00191

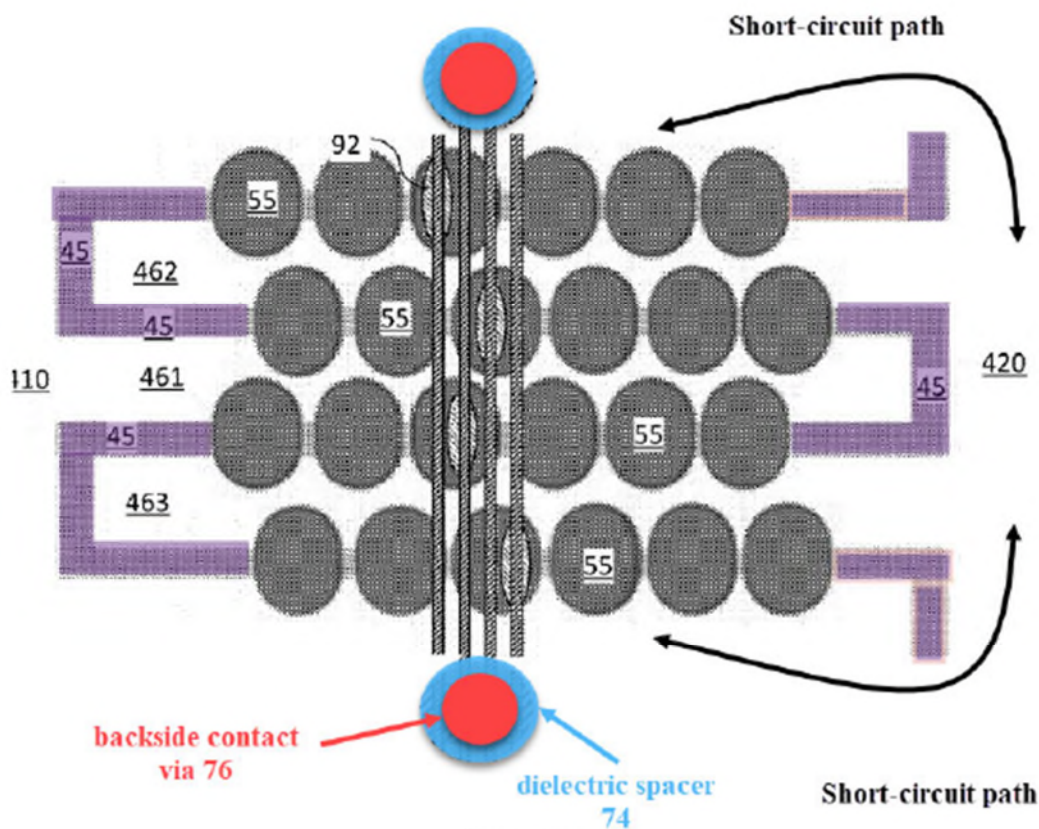
II. RESPONSE TO CERTAIN OF PATENT OWNER’S ARGUMENTS

7. The paragraphs below respond to certain of the arguments and assertions made by Patent Owner and Dr. Campbell in this proceeding. In these paragraphs, I address only a fraction of the opinions and assertions Dr. Campbell set forth in his declaration. The fact that I do not respond to any particular opinion expressed by Dr. Campbell should not be considered to indicate agreement with that opinion or as a concession of any kind.

A. A Circular TAC Was Obvious In View of Nishikawa Alone Or Additionally In View Of Nishikawa2

1. Implementing a Circular TAC Would Not Render Nishikawa Inoperable

8. I understand that PO asserts that implementing a circular TAC in Nishikawa would result in an inoperable device because the gate sets 410 and 420 would short (i.e., electrically connect). POR 11-24. Dr. Campbell, for example, states that “Petitioner’s proposed modification is shown below.” EX2021, ¶56.

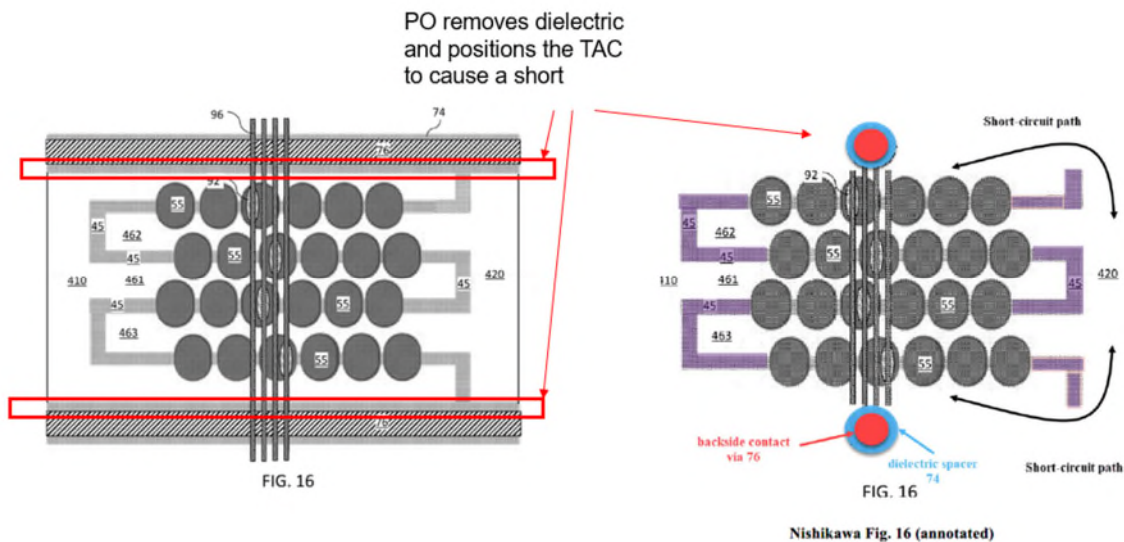


Nishikawa Fig. 16 (annotated)

EX2021, ¶56.

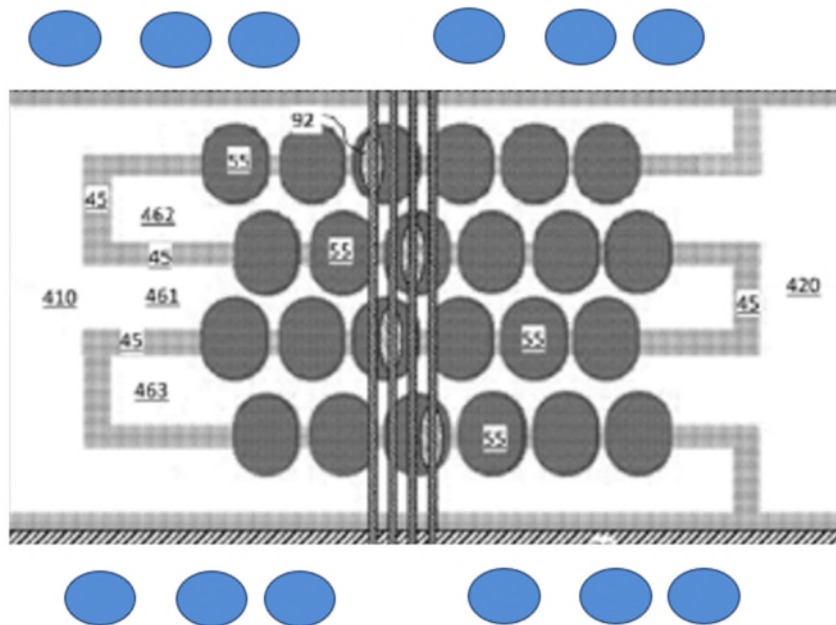
9. I understand that Dr. Campbell testified that “[a] POSITA would not” modify Nishikawa in this way. EX1106, 73:22-74:9. I agree that a POSITA would not modify Nishikawa as shown above because that depiction removes dielectric structures required to maintain electrical isolation. As shown below, this modification removes dielectric structures that are above and below the memory cells, creating an electrical path (via the gate layers) between gate sets 410 and 420.

In other words, this modification would electrically couple gate sets 410 and 420. This is what Patent Owner and Dr. Campbell refer to as a short circuit.



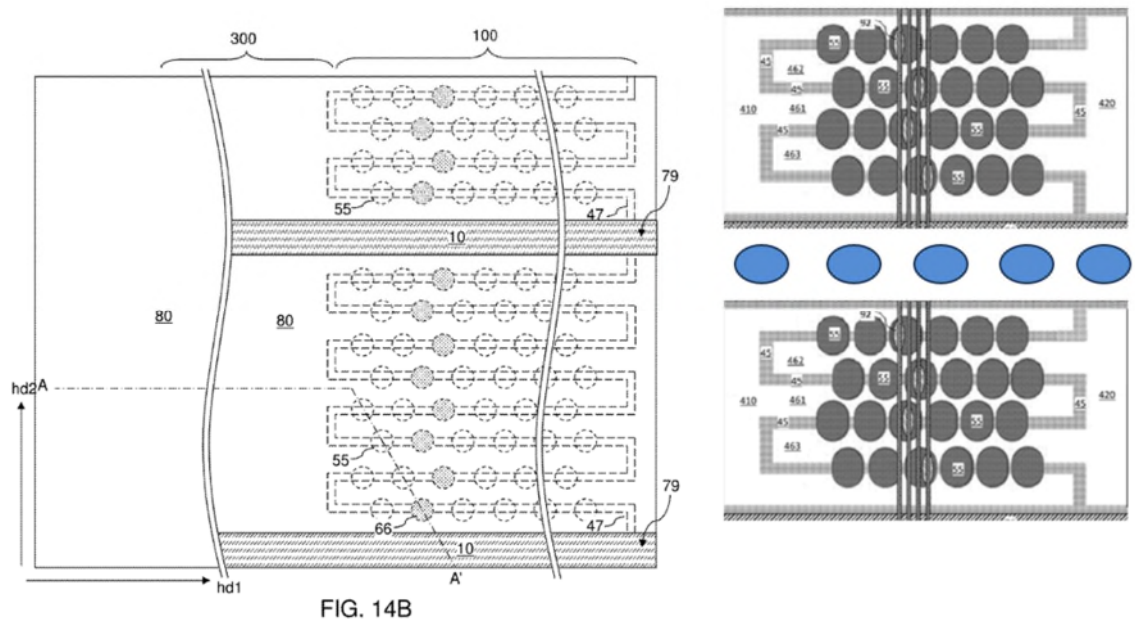
EX1005, Nishikawa, Fig. 16 (along with adding annotations onto Dr. Campbell's version of Figure 16).

10. This is not representative of the obvious circular TAC implementation that my original declaration explains. Specifically, I explain how the separator 45 splits the Nishikawa into memory zones, i.e., that gate sets 410 and 420 are separate: “The voids for the separator dielectric 45 segments the array stack into separate portions, and the insulating fill isolates those segments. In short, there are separate areas of the memory stack, such that a gate layer does not extend through the entire memory array (but only its respective memory zone).” EX1003, ¶131. Thus, the dielectric separator still separates the gate sets in the combination, as shown below:



EX1005, Nishikawa, Fig. 16 (with annotations).

11. A POSITA would have understood multiple well-known arrangements are operable with circular TACs. For example, one might repeat instances of the above unit or block. This is consistent with Nishikawa2's teaching in Figure 14B. Here, separators or circular TACs could separate the gate sets in each unit or block, as shown below:



EX1046, Nishikawa2, Fig. 14B (left), modifications to EX1005, Nishikawa, Fig. 16 (right). Similarly, with this same arrangement, one could remove the two horizontal dielectrics on both sides of the TACs, and instead, employ a single TAC that connects the bottom block's right dielectric portion to the top block's right dielectric portion (which then allows the comb-shaped dielectric structure and the TAC to completely set gate sets 410 and 420).

12. Dr. Campbell suggests that the horizontal dielectric structures above and below the memory cells are only the spacers (74) for the trench (76), not the separators (45), and thus the obviousness grounds create a short:

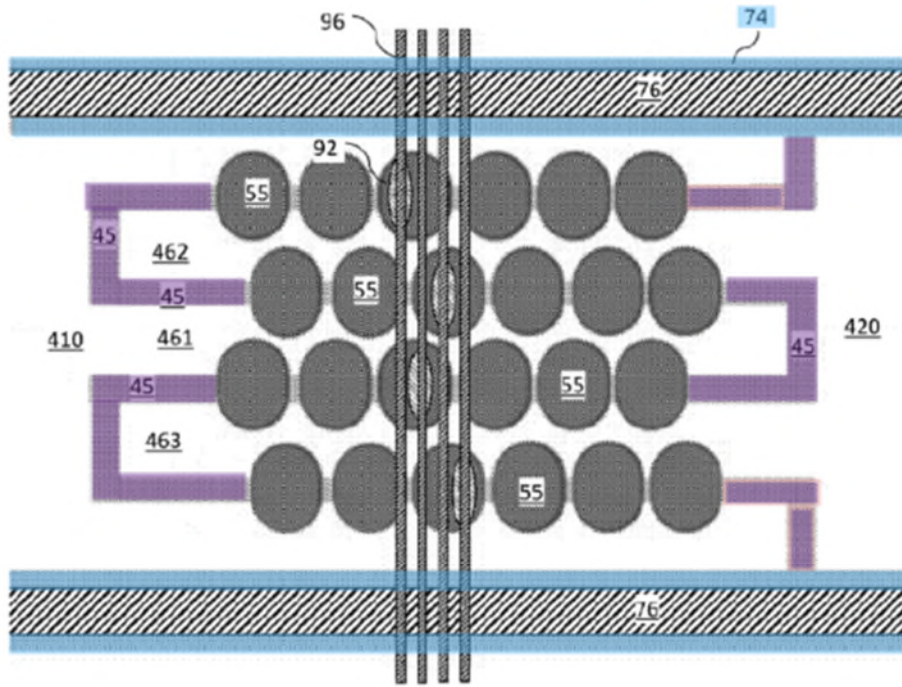
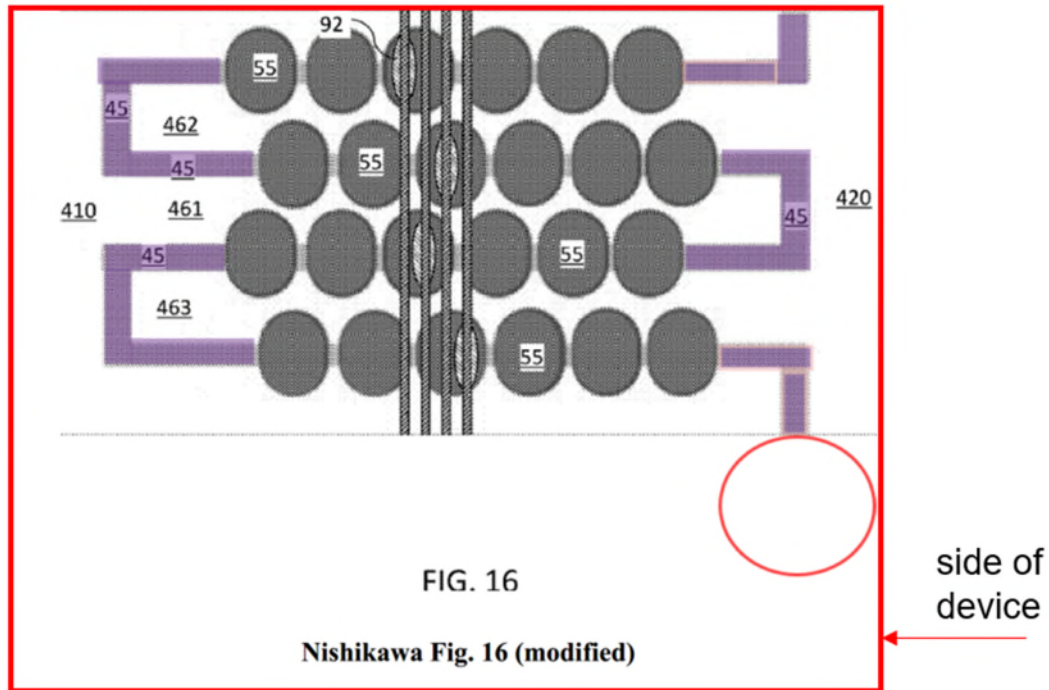


FIG. 16

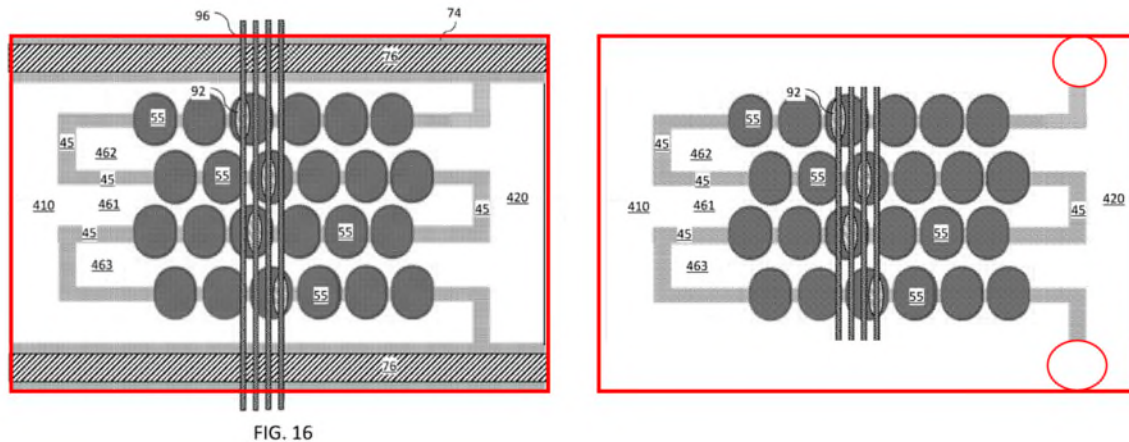
Nishikawa Fig. 16 (annotated)

EX2021, ¶58. I disagree, because Nishikawa states that the separators 45 “laterally separate the control gates,” i.e., dielectric separators include the top and bottom portions because they laterally separate gate sets 410 and 420. EX1005, Nishikawa, 17:14-23. But more importantly, as I describe above, the obviousness ground includes a separator that separates gate sets 410 and 420. In fact, Dr. Campbell opines that the “purpose” of Nishikawa is separating gate sets 410 and 420. EX2021, ¶57. Thus, consistent with this purpose, the obviousness ground includes separator structures to provide this separation.

13. Dr. Campbell provides the example below of Nishikawa with a circular TAC:



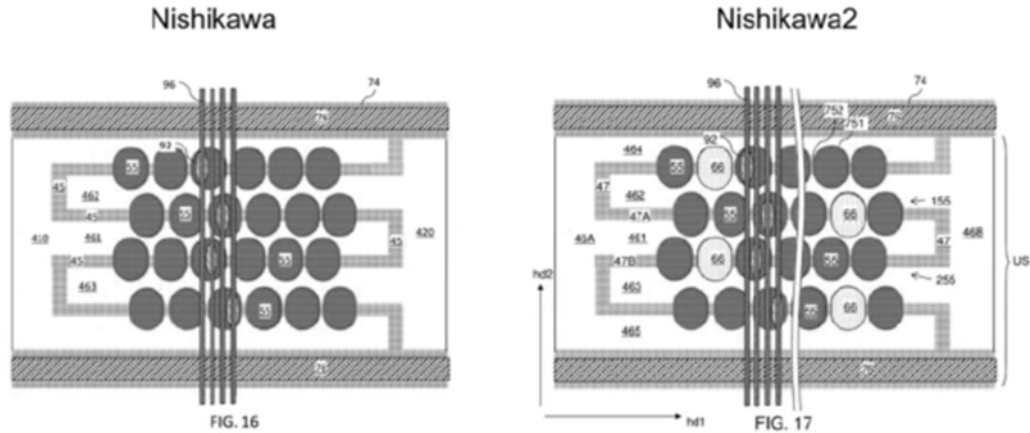
EX2021, ¶60 (along with my annotation of an outline of the possible device, excluding the connection region and peripheral region for illustration purposes). Dr. Campbell states that this example necessarily would require a larger footprint. I disagree. The circular TACs could simply replace the trenches, abutting the device edge, as shown below:



EX1005, Nishikawa, Fig. 16 (with annotations). The above depiction of the likely end of the device is consistent with Nishikawa2's Figure 14B, unlike what Dr. Campbell appears to suggest would be the end of the device in his example. In any event, in my opinion, the assumption that a circular TAC that isolates gate sets 410 and 420 would increase the footprint is incorrect.

2. **Nishikawa2's Circular TAC Disclosure Is Relevant to Nishikawa and a POSITA Would Understand the Statement Means That a Circular Shape Is Suitable for Nishikawa's Trench TAC**

14. My opening declaration explains the similarities between Nishikawa and Nishikawa2.



Nishikawa, Fig. 16; Nishikawa2, Fig. 17; Lee, ¶ 115.

EX1003, ¶115. Dr. Campbell states that this “circular” statement in Nishikawa2 would not be understood to apply Figure 17 of Nishikawa2 (and thus not Figure 16 of Nishikawa). EX2021, ¶66. I disagree. First, both Figure 17 and Figures 14A-C of Nishikawa2 include combed-shaped sets of wordlines. This is shown below.

clarity.” *Id.*, 24:65-67. With reference to Figure 14A below, one can see the dielectric layers 70 and 80 above the alternating layers. Figure 17 simply removes these so the viewer can see a top-down view of the top layer 46 below.

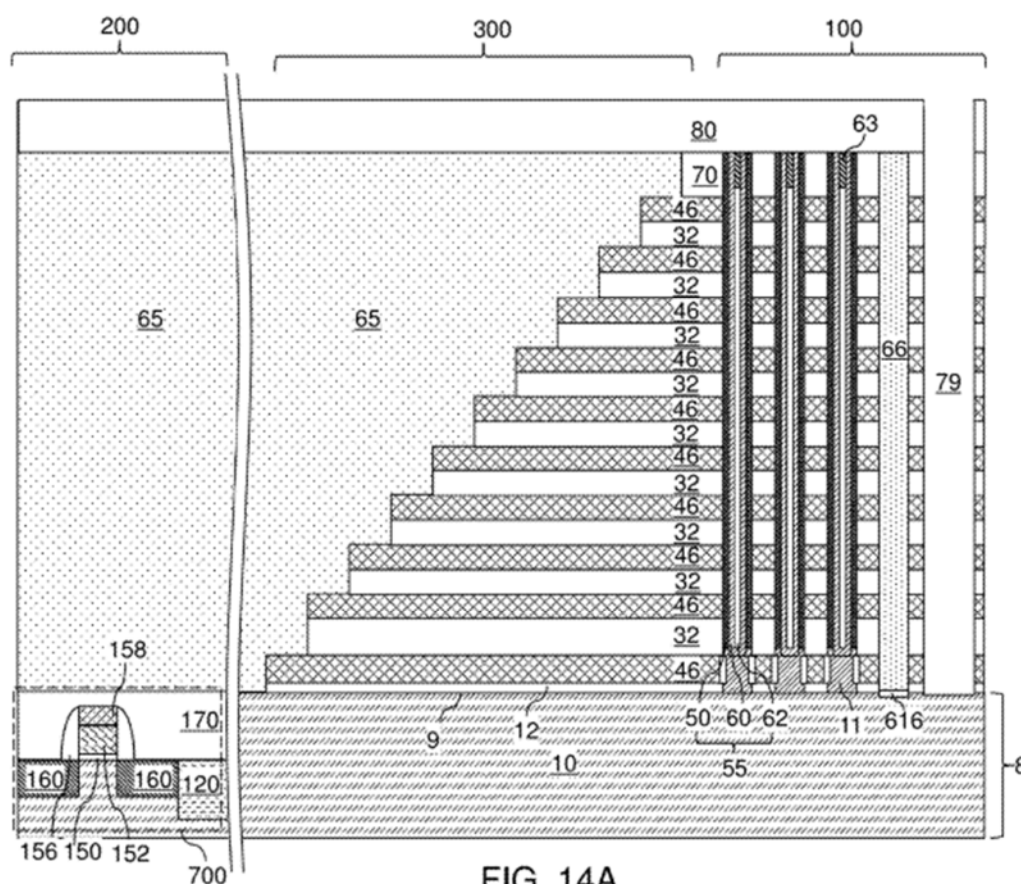


FIG. 14A

Id., Fig. 14A. Thus, the top-down view shows how the top conductive layer 46 is split (between gate sets), and the description focuses on that split and the gate sets.

15. I also note that Figures 14-17 use common numerals, *e.g.*, 46, 70, 76, 79, and 80. I understand that a patent regulation states that the “same reference characters must never be used to designate different parts.” 37 Code of Federal

Regulations 1.84(p)(4). This is consistent with how a POSITA would have understood these figures. And this is consistent with Figure 14-16 describing the device effectively in stages of manufacture, and with Figure 17 then removing the top layers to describe the gate sets (*see above*).

16. Dr. Campbell also states that “backside contact via 76 ... provides the necessary electrical isolation.” EX2021, ¶67. But Nishikawa2 refers to the trenches there and elsewhere as “optional,” which a POSITA would understand to mean that alternative shapes—including circular trenches—are suitable for performing the same function. EX1046, Nishikawa2, 25:39-49, 27:62. This is consistent with Nishikawa stating that such trenches may be in any suitable shape, such as “circular.”

3. Nishikawa and Nishikawa2 Describe the Same Architecture

17. I describe above that Figures 14-17 of Nishikawa2 describe the same embodiment. This is not surprising, because a POSITA often would describe an invention, set of inventions, or a project in multiple, serial publications or patents. I understand that Dr. Campbell testified that a POSITA would often address, in a subsequent publication, “other aspects that weren’t addressed in the first paper.” EX1106, 17:8-22. I agree with Dr. Campbell in this regard. And in my opinion, a POSITA would at once understand the applicability of Nishikawa2’s circular TAC statement to Nishikawa’s TAC.

4. Circular TACs Were Well Known and Suitable for Nishikawa's Trench Functions

18. Dr. Campbell states that a POSITA would not have been motivated, or had a reasonable expectation of success, to implement circular TACs in Nishikawa due to alleged inoperability issues. EX2021, ¶69. For the reasons that I discuss above, I disagree.

5. Circular TACs Are Not Complex to a POSITA

19. Dr. Campbell states that 3D NAND technology is not straightforward and involves complex process steps. EX2021, ¶¶70-71. This assertion lacks context because complexity must be evaluated from the perspective of a POSITA, not in the abstract. I understand that we must provide our opinions from the perspective of a POSITA. A POSITA would have already had substantial practical experience with 3D NAND fabrication. To put the TAC in context, the smallest circular etches are for the memory structures. I discuss this with citation to EX1010 in my initial declaration. EX1003, ¶165. To do this, the technique would even involve multi-deck structure, so one could etch the holes in two steps, limiting tapering. *Id.* TACs, on the other hand, are much larger in size and do not involve the relative complexity of etching channel holes. Tessariol is instructive. Tessariol describes forming the holes, and other components, of TACs through the memory stack (including through the entire stack and through mostly the dielectric fill) in simple terms. EX1036, Tessariol, [0037]-[0038], Fig. 16.; §II.D. Further, Nishikawa2's statement that

trenches “can be any suitable shape, such as circular” (EX1046, Nishikawa2, 22:38-41), without detailing the processing, e.g., mask and etch chemistries, shows that such fabrication of TACs was routine to a POSITA.

20. Dr. Campbell suggests that the change in mask would not be “unusually simple.” EX2021, ¶73. But Tessariol rejects that. Indeed, forming a mask involves photolithography to form a shape, e.g., rectangular or circular. As Nishikawa2 says, that can be any suitable shape, just like the TAC. I provide many examples of these routine steps in my opening declarations. EX1003, ¶¶117-21. These references show that any alleged complications that Dr. Campbell raises, e.g., EX2021, ¶¶74-75, are simple fabrication issues that POSITAs knew how to manage. Again, TACs were routine to implement relevant to the channel structures, which Nishikawa already fabricates. In fact, Nishikawa already fabricates circular contacts, the peripheral and staircase contacts. EX1005, Nishikawa, Fig. 1. Forming circular contacts was basic textbook material well before the ’322 patent. §II.D.

21. I discussed some of these fabrication issues during my last deposition, and Dr. Campbell cites that testimony referring to “channel holes.” EX2021, ¶76. Again, high-aspect channel holes were more difficult to etch than TAC holes, but Nishikawa already etches both holes (e.g., channel holes, staircase contacts, peripheral contacts). This demonstrates that fabricating circular TAC was routine

and well within the ordinary skill of a POSITA in the context of Nishikawa and the '322 patent.

B. A POSITA Would Have Been Motivated With A Reasonable Expectation of Success to Add Dummy Channels To Nishikawa

1. It Was Common to Include Dummy Channels on the Edge of the Array to Avoid a Defective Device

22. In my first Declaration, I discuss edge effects and cite EX1024. That reference discloses: “In a typical flash cell array, cells located at the edge of the array are much more subject to processing variations than the cells not located at the edge. Because of this, it is common to refrain from using the cells at the array edge. Such cells, which extend around the perimeter of the array, are sometimes referred to as dummy cells.” EX1024, 8:47-53. By way of one example of a “processing variation” at the edge of array, there are issues relating to “proximity effects” at the edges of “dense patterns” (e.g., a dense pattern of memory cells). EX1107, Wolfe, Volume I, p. 26 (“As described in Chap. 14, however, for small features in dense patterns, the effect of backscattering (leading to pattern distortion by proximity effects) must be accounted for in e-beam exposure.”). In short, close neighboring structures can cause scattering issues: “closely spaced patterns will receive electrons from the exposure of their neighbors.” *Id.*, p. 43. Adjustments can be made “for proximity effect corrections.” *Id.* But because the pattern changes for the edges, that is, there is not a “closely spaced pattern[]” on the other side of a respective edge,

the scattering is different at the end, and thus even with the corrections that account for the internal portion of the array, the fabrication result is different on the edges. Another process variation is that lithography at small geometries implicates diffraction effects. *Id.*, pp. 3-7. One simple way to view these mechanisms is to imagine light and small objects reflecting off surfaces; if those surfaces are a consistent pattern, corrections can be made to account for these reflections. But at the end of a pattern, those corrections do not apply, because the surrounding surfaces are different than in the middle of the pattern. Thus, this phenomenon is no different when fabricating a 2D versus 3D array of memory cells. These edge effects similarly explain that pattern distortion that my opening declaration discusses. EX1003, ¶142. Put simply, the conventional desire is to fabricate a pattern (and thus fill in empty spaces if necessary), account for issues such as proximity effects and diffraction effects, and then refrain from using the edge cells (or other structure) to avoid structural differences those edge cells (or other structures) will have (and which will likely impact those edge cells operation).

23. As a result of the above edge effects, the edge cells have structural differences from those cells in the core that lead to different electrical behavior and reduced reliability, making it common practice to designate them as dummy cells. In other words, it was common to simply not use the edge cells, not connect them to, e.g., bit lines, and hence leave them as dummy cells. EX1024, 8:47-53.

Attempting to use the edge cells may result in a defective device because the cells do not accurately read data.

24. It is also notable that on the edge, structurally speaking, there is nothing on the other side, whereas in the core, cells surround the core cells. EX1015, p. 101 (“an edge memory cell has a different condition compared with middle cells.”); *see also id.*, p. 98 (“dummy word-line (dummy cell) scheme in NAND flash memory was proposed to eliminate abnormal program disturb of edge memory cell”). For this additional reason, the edge cells operate differently. It was textbook material to use dummy edge cells to account for all these variances. *Id.*, pp. 98-103.

25. Again, edge effects are applicable to 3D memories, just like 2D memories. Lee, which was filed the same day as the ’322 patent, discloses dummy channel in view of “array edge effects”:

In a conventional 3D memory device structure, data lines (e.g., bit lines, digit lines) are electrically coupled to vertical memory strings of a vertical memory array, and an opening is provided next to edges of the vertical memory array to accommodate data line contacts for each of the data lines. The data line contacts electrically couple the data lines to control logic circuitry to facilitate operations (e.g., read operations, write operations, erase operations) on the vertical memory strings of the vertical memory array. However, providing the opening for the data line contacts next to the vertical memory array can effectuate damage to and/or defects at the edges of the vertical memory array (e.g., commonly referred to as “array edge effects”). Accordingly, an array of “dummy” pillars (e.g., dielectric pillars) is conventionally provided between the vertical memory array and the opening to set the edges of the vertical memory array back farther from the opening and mitigate the aforementioned damage to and/or defects at the edges of the vertical memory array.

EX1108, U.S. Pat. No. 11,043,507, 1:41-63. Lee's disclosure confirms that inclusion of dummy channels to mitigate edge effects was a routine and accepted design practice at the relevant time. Lee attempts to reduce the number of necessary dummy channels (*id.*, 1:64-2:2), but still includes dummy channels (*id.*, e.g., claim 1), demonstrating that dummy channels are a normal addition to account for edge effects even for POSITAs attempting to include as few as possible dummy channels.

26. By way of another example, Ravasio discloses a 3D memory. EX1109, U.S. Pat. Publ. No. 2015-0029775A1, [0026] ("a three-dimensional (3D) cross-point memory array architecture"). Ravasio also describes dummy channels in view of "edge array effects":

Dummy material portions, e.g., portions 234-1 and 234-2, can include, for instance material formed to a lower tolerance and formed external, e.g., on an outer edge, to the active array portion 252. For example, in patterning a memory cell array, outer memory cell stack structures can be deformed or marginalities can be generated, caused by an iso-dense loading effect. Dummy material portions, if electrically inactive, e.g., isolated, as compared to the rest of the array, can be utilized to reduce undesired edge array effects. In a number of embodiments of the present disclosure, dummy material portions can be inactive, e.g., be non-active, non-electrically connected portions used to reduce undesired edge array effects. In a number of embodiments, dummy material portions can be electrically inactive in cross-point memory arrays and/or three-dimensional cross-point memory arrays. In a number of embodiments, electrically inactive can include being in electrical contact with at least one of a first and second conductive material, e.g., a word line and a bit line. In various embodiments an electrically inactive stack can comprise a stack structure connected to only one of the first and second conductive materials. In a number of embodiments, electrically inactive can include electrically isolated, including from at least one of a first and second conductive material.

Id., [0033]. The iso-dense loading effect refers to that at the edge, due to a change in density of devices, etching rates and profiles will be different. Again, this is a process variation to which EX1024 refers above.

27. By way of another example, Lee discloses a 3D memory device. EX1110, U.S. Pat. Publ. No. 2019-0027434A1, [0004] (“a vertical memory device”), Fig. 3B (same). Lee attempts to minimize the number of dummy channels. Yet still, Lee recognizes the need for dummy channels:

The edge region MEC2 of the memory cell region MEC may include a dummy channel region DM disposed at a portion adjacent to the connection region CON. A plurality of dummy channel structures D180 may be disposed in the dummy channel region DM of the edge region MEC2. The plurality of dummy channel structures D180 may have substantially the same configuration as the plurality of first channel structures 180A and the plurality of second channel structures 180B. In other words, each of the plurality of dummy channel structures D180 may include the gate dielectric film 182, the channel region 184, the buried insulating film 186, and the drain region 188. As illustrated in FIG. 4, the plurality of dummy channel structures D180 may extend nonlinearly in the vertical direction (e.g., the Z direction), which is similar to the plurality of second channel structures 180B.

[0045].

28. Dr. Campbell states that I “recognized that any dummy regions existing at the edge of the array would be ‘later sacrificed in processing.’” EX2021, ¶93. I did not recognize that. I was citing EX1025 to demonstrate the general principle of edge effects. EX1003, ¶141. The “later sacrificed in processing” refers to that the dummy channels are not wired later in the process, and therefore are used as active

channels (“sacrificed”) and this occurs “later,” when the bit lines are fabricated (see *infra*, §II.B.5). The sentence after “sacrificed” refers to the dummy pattern region causing noise, so that region is still there during operation when the product is final and operation (hence there being “noise”). EX1025, 2:30-48: (“Conventionally, an abnormal edge pattern at the edge of array may be controlled by adding a dummy pattern region, which is later sacrificed in processing. However, noise associated with overlay (OVL) mark for scanner alignment or real time defect analysis (RDA) inspection can be an issue if edge pattern is abnormal, even if within a dummy pattern region.”). And as all of the above references show, it was conventional to leave the dummy edge cells.

29. I should also note that were one to remove the edge dummy region, then the edge cells would be operational. As I discuss above, a known issue, in that case, was those edge cells are different because the neighboring cells are different in number and orientation relative to the core cells. Thus, the operational characteristics are different. This was a reason, separate from the process variations, not to use the edge cells and leave them as dummy cells.

30. Dr. Campbell states that there is “no room” for memory cells in Nishikawa. EX2021, ¶97. This assertion is incorrect. First, of course, Nishikawa’s “drawings are not drawn to scale.” EX1005, Nishikawa, 3:53. 3D memories device store millions or billions of memory cells. I also discuss immediately below that Dr.

Campbell is showing a portion of the Nishikawa device here. The device includes the array region, continues to a connection region, and then continues to a peripheral region. The common approach, to avoid edge effects and provide constant support through the device, was to include dummy channel structures from the edge of the array throughout the connection (or contact) region. And there is always room for the dummy channels, because by definition, you place channels at the edge of the array (and refrain from using those, rendering the dummy channels).

2. Dummy Channels In Nishikawa Do Not Provide Only Redundant Support

31. Dr. Campbell states that “[a] POSITA would not have been motivated to add dummy channels that are redundant because they serve no additional support purpose.” EX2021, ¶88. I disagree. Recall that the gate sets are 410 and 420 below:

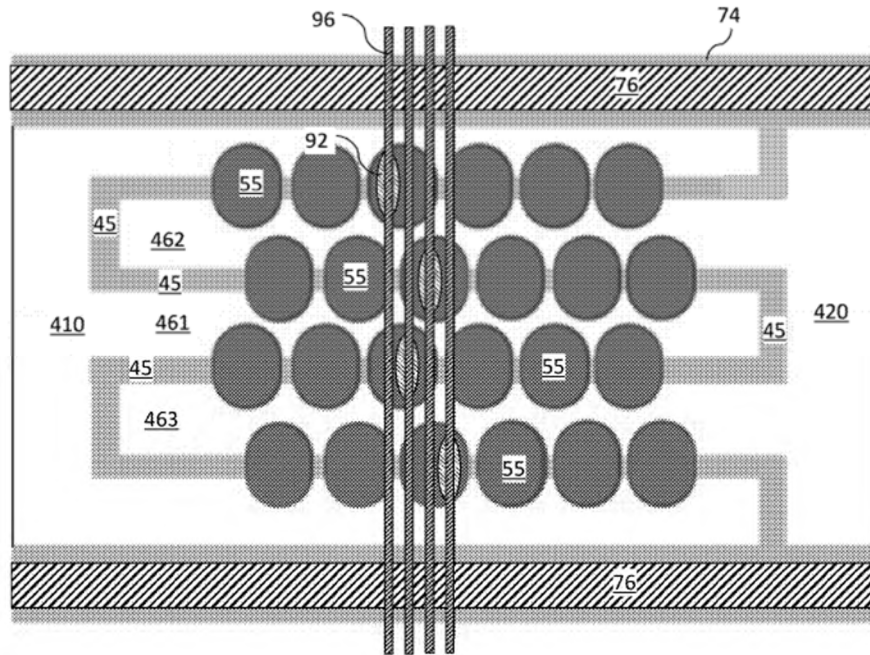
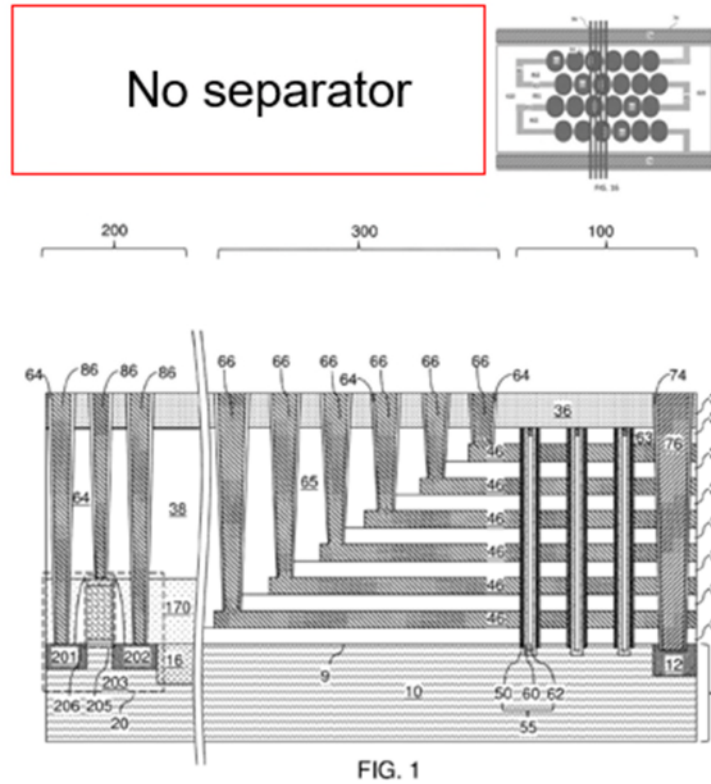


FIG. 16

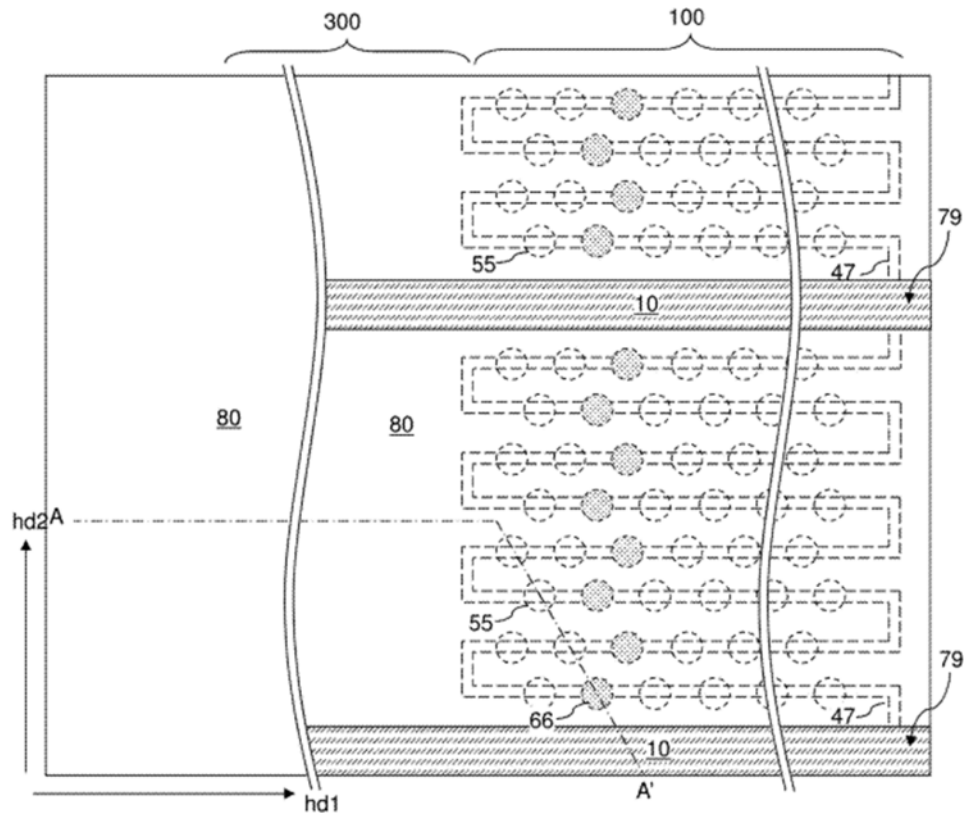
EX1005, Nishikawa, Fig. 16. During the gate replacement process, there are voids where the sacrificial gates are, because those gates are etched out. Vertical members through the stack provide support during the gate replacement process, when voids are present and the alternating layers would otherwise be prone to collapse or deformation. By analogy, imagine branches (like the dielectric layers) extending from a tree (like the vertical member). Of course, the further away from the tree, the branches start to bend down. Thus, for a proper amount of support, the device needs the support structures throughout the device wherever layers of the stack (and thus voids during the gate replacement process) are. EX1030, 7:30-35 (“In accordance with one embodiment of the invention, dummy structures in the end portion support the features (e.g., the respective ceilings and floors, or plates) from vertical

movement, for example by laterally engaging side portions of such floors/ceilings that were created where such dummy structures extend there-through.”). Otherwise, in a region in which there are no support members, the stack will collapse. This is why 3D memory design includes support members throughout the device, from the array (e.g., memory cells (if the holes are not used for the gate replacement process) or separator-like structure), the array edge, contact or connection region (staircase contact), and the peripheral region (which may need little support if it mostly comprises dielectric fill instead of layers of the alternating stack). I demonstrate this with several prior art examples below.

32. As a preliminary matter, Dr. Campbell does not even consider Nishikawa’s full device when making his “no room” assertion. Nishikawa includes an array (100), peripheral region (200), and connection region (300). There is no separator in either the peripheral or connection region:



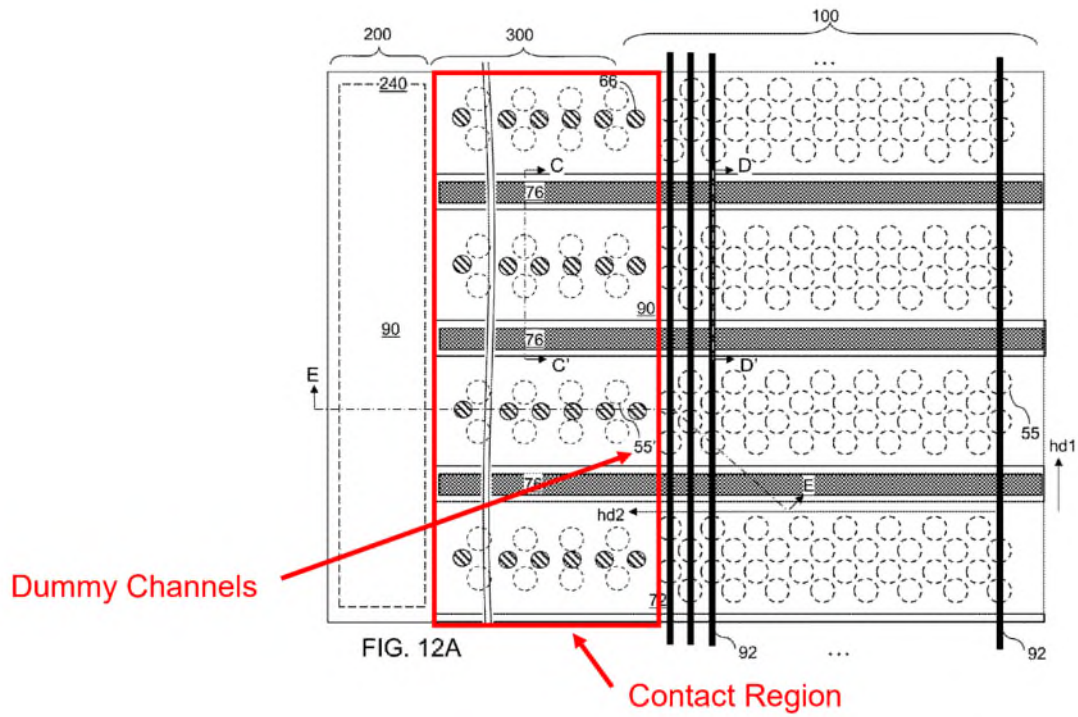
EX1005, Nishikawa, Figs. 1, 16. That there is no separator in the peripheral or connection region is consistent with Nishikawa2:



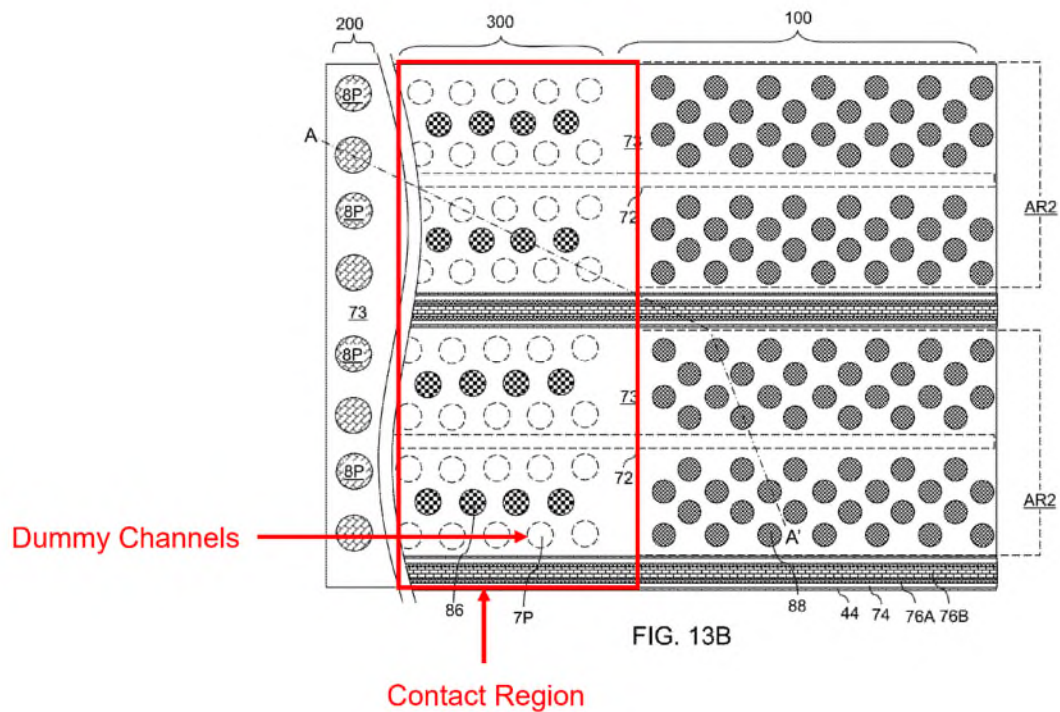
EX1046, Nishikawa2, Fig. 14B.. But, of course, there are alternating stack layers from the edge of the array through the staircase region, and thus voids during the gate replacement process and stability issues.

33. To be clear, a POSITA would have understood that while Nishikawa does not disclose support structures, such as dummy channels, in the connection region, that region must include support structures. This was known by at least 2010:

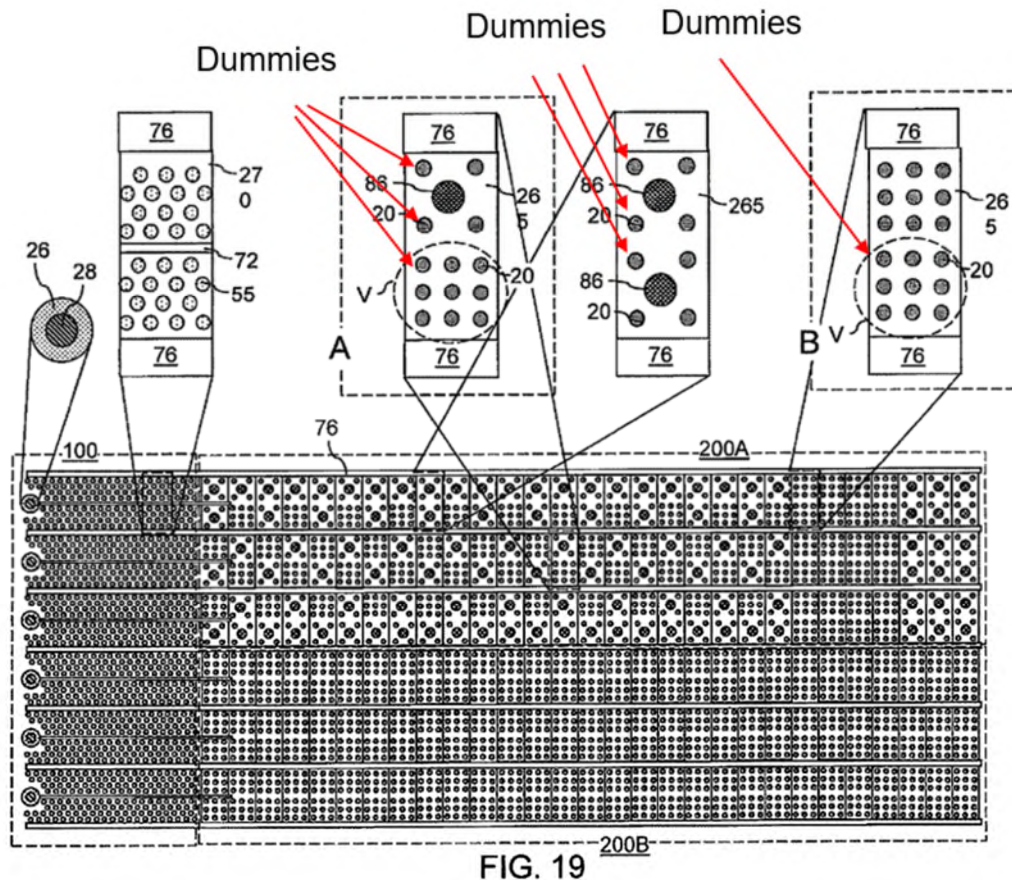
The dummy structures may support material of the features from vertical movement in the end portion while at least some of sacrificial material that is elevationally between the material of the features in the primary and end portions is removed. The processing depicted in going from that of FIGS. 5-8 to that of FIGS. 9 and 10 is but one such example processing. With respect to a prior art problem, dummy structures



EX1112, Miyata, Fig. 12A, 44:37-40.



EX1113, Mizutani, Fig. 13B, 16:38-51.



EX1031, Masamori632, Fig. 19, 30:14-27, EX1003, ¶143.

37. I also note that as devices scale, e.g., to include more layers in the alternating stack, additional support becomes necessary. As Masamori states, “enhancing structural support” becomes desirable with such scaling. EX1020, Masamori, [0003]. Nishikawa was filed a few years after the earliest priority date of the ’322 patent. Thus, when considering Nishikawa disclosure at the time of the ’322 patent’s earliest priority date, a POSITA would have been motivated to consider additional support structures, as the POSITA would assume that Nishikawa

would scale to smaller sizes. This would have further motivated the additional support structures.

3. **Dummy Channels, as an Alternative to Support, Can Be Used to Improve the Gate Replacement Process**

38. In my opening Declaration, I describe that Nishikawa can perform the gate line replacement process through the memory openings and by spreading those out through the device, this can improve the gate line replacement process, because the openings can be spread throughout the device. EX1003, ¶¶125-26.

39. Nishikawa2 similarly describes using memory openings and dummy openings for the gate line replacement process. EX1046, 18:56-62. Nishikawa2 describes forming, e.g., dielectric pillars (66) that are like the channel structures, in the access openings. *Id.*, 21:40-22:14, Fig. 14B. Therefore, if not using the dummy channel as support structures, instead, the dummy holes (which then will become dummy channels) can be used to improve the gate replacement process. Thus, dummy channels provide multiple independent benefits, including mitigating edge effects, providing mechanical support, and improving the gate replacement process.

4. **The Alleged Disadvantages of Dummy Channels Would Not Discourage a POSITA from Including Dummy Channels in Nishikawa**

40. Dr. Campbell opines that a POSITA would not be motivated to include dummy channels in Nishikawa because it would decrease memory density. EX2021, ¶¶99-103. I disagree because this is not a serious tradeoff to consider. Support is

necessary during the gate replacement process to avoid the stack from collapsing and resulting in a defective, non-sellable device. *Supra*, §II.B.1-2. Also, using the edge cells similarly risks a defective device. *Id.* Thus, it goes without saying that there is a benefit in this alleged “tradeoff,” because a functional device is better than a non-functional one with slightly more density. All of the exemplary examples demonstrate this. *Supra*, §II.B.1-2. Any marginal reduction in density would have been understood by a POSITA to be an acceptable and common tradeoff to ensure yield and functional device operation.

41. Further, memory devices include millions and usually billions of active memory cells. The percentage of dummy channels pales in comparison. Thus, the incremental cost to ensure a functional device is well worth the tradeoff.

42. Dr. Campbell alleges that the introduction of additional dummy channels creates “processing risks.” EX2021, ¶¶105-06. I disagree, because to create dummy channels, all that one does is not, for example, wire the instances of the active channels (rendering the dummy channels). *See supra*, §II.B.1, *infra*, §II.B.5. Also, this actually improves yield, because it mitigates the risk of fabricating defective devices due to the edge effect and the potential collapse of the alternating layers. *Supra*, §II.B.1-2.

5. **Dummy Channels Are Not Complex in the Context of a POSITA**

43. Dr. Campbell opines that forming dummy channels is complex. Complex is a relative term. It can be said that fabricating any semiconductor device is complex. But in the context of a POSITA, for example, fabricating a channel structure certainly is not complex, but is routine. A POSITA, of course, knows how to fabricate a memory channel, because all 3D memory devices, which a POSITA has experience designing, have memory channels. Memory channels, of course, are the “heart” or “engine” of a memory device.

44. All that fabricating dummy channels requires is forming channel structures, which Nishikawa and all the references do, and refraining from using some, e.g., the ones on the edge. EX1024, 8:47-53. This can be seen below:

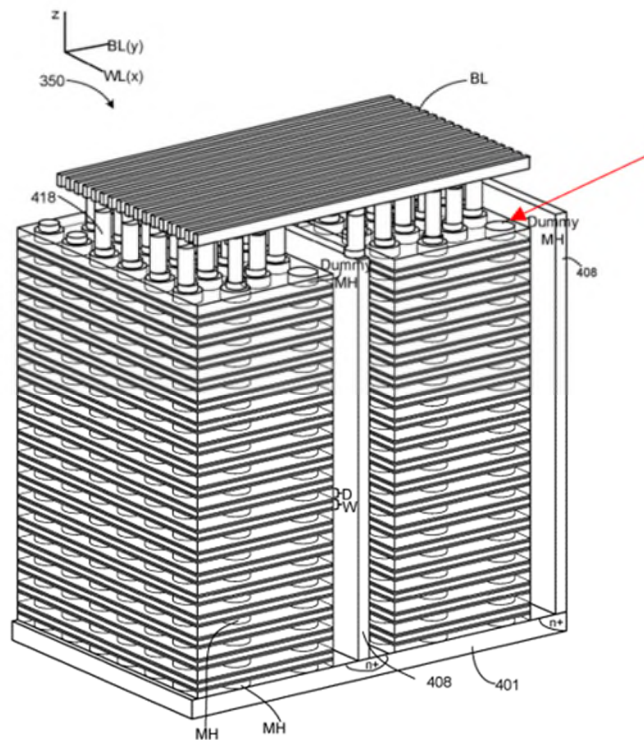


Figure 4B

EX1111, Iwai737, Fig. 4B. As can be seen above, there is simply no bit line connection to the “Dummy MH.” Typically, they are fabricated the same but not “wired,” i.e., connected to the relevant electrical paths, e.g., bit line, and thus are electrically inactive versions of memory structures (hence the name, “dummy channel”).

C. A Ribbed TAC Was Obvious

45. Claims 13-18 and 20 (via claims 13 and 14) describe a ribbed TAC. As can be seen below, the lateral diameter of the TAC corresponding to the conductive layers (gap 312) is wider than the lateral diameter corresponding to the dielectric layers (gap 304), forming a ribbed shape:

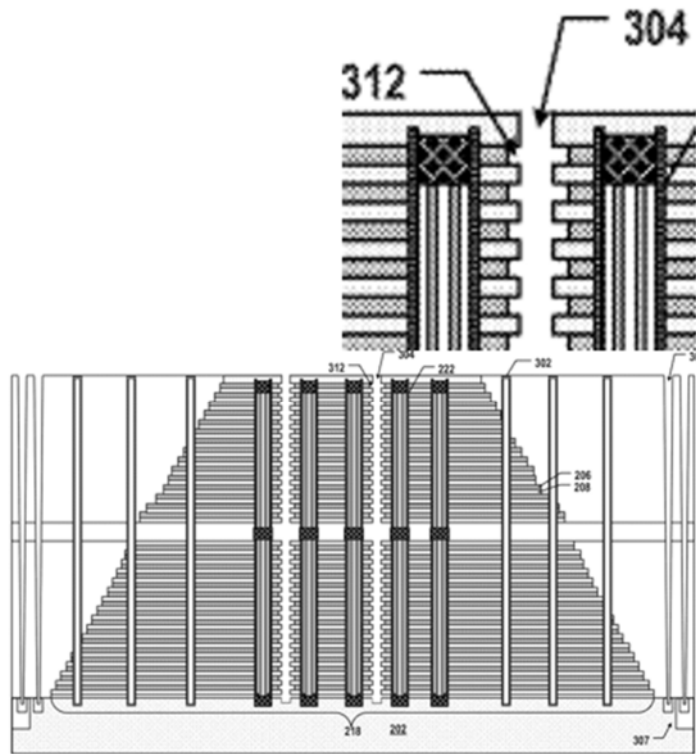


FIG. 3D

EX1001, Fig. 3D. Dr. Campbell describes this apparatus limitation by reference to a method step of removing a portion of the sacrificial layers (which become the conductive layers). EX2021, ¶128. The result after this step is shown above. However, there is an important step after this. Specifically, after forming a liner in the above TAC hole, a subsequent etch removes the bottom portion of the liner and lateral portions of the spacer in the TAC hole. The degree of lateral etching that occurs will depend on the degree to which the etch is directional, and a POSITA would expect at least some lateral recessing to occur in routine etch processes. The

etch of the bottom portion of the liner, which is necessary to connect the bottom of the TAC core to an underlying device, is shown below in the '322 patent:

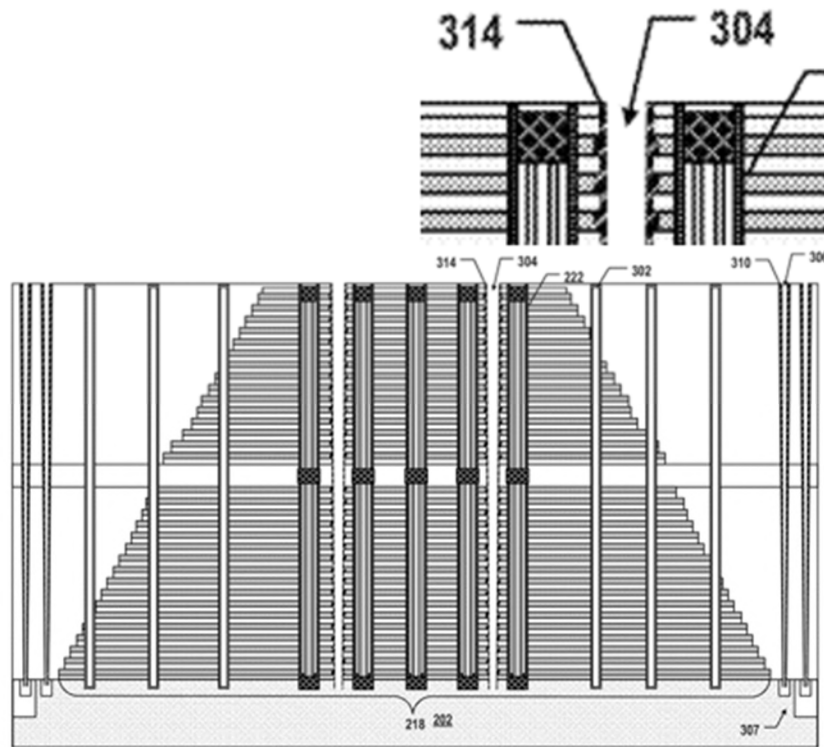


FIG. 3E

EX1001, Fig. 3D.

46. As I will describe below, the impact of this lateral etch was well known and recessing the sacrificial gates (which become conductive gates) was well known to mitigate the risk of short circuits as a result of this lateral etch occurring (and also to generally mitigate against capacitive coupling between the conductive gate and TAC core).

1. The Motivation of Providing Extra Space Was Extremely Well Known

47. I explain that recessing the sacrificial gates creates extra space for additional dielectric spacer in my opening declaration. EX1003, ¶173. This additional dielectric therefore provides additional dielectric between the TAC liner and the sacrificial gates (which become conductive gates). Cui demonstrates the import of this extra space. This additional space (*see* blue recesses at below-left and yellow spacer at below-middle) provides lateral margin for the etch that removes the bottom portion of the liner. By margin, I mean that even if the etch of the bottom liner laterally etches, there is a margin, or room for the etch to occur, before the etch would expose the sacrificial gate. As shown below in the middle and right figure, etching the bottom portion can also etch the spacer on the side. Again, the degree of the lateral etching is dependent on the degree to which the etch of the bottom liner is directional. In any event, if the recess did not have this additional dielectric, the etch could expose the sacrificial layers (which become the conductive gates), because the lateral etching would etch the spacer liner and directly expose portions of the respective sacrificial gates. Then, after forming the TAC core, there would be short circuits, because the TAC's core could then contact the conductive gates.

Etch to create
extra space



FIG. 40C

Liner fills extra
space to provide
margin

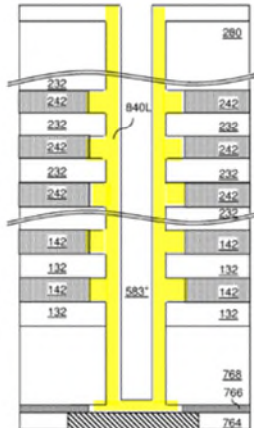


FIG. 41C

Etch bottom of liner,
and margin prevents
exposing sacrificial
gates

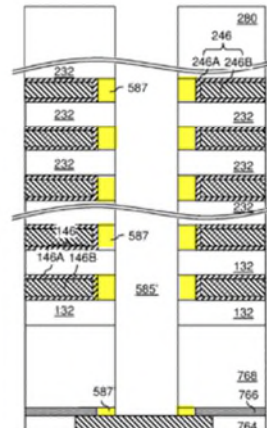
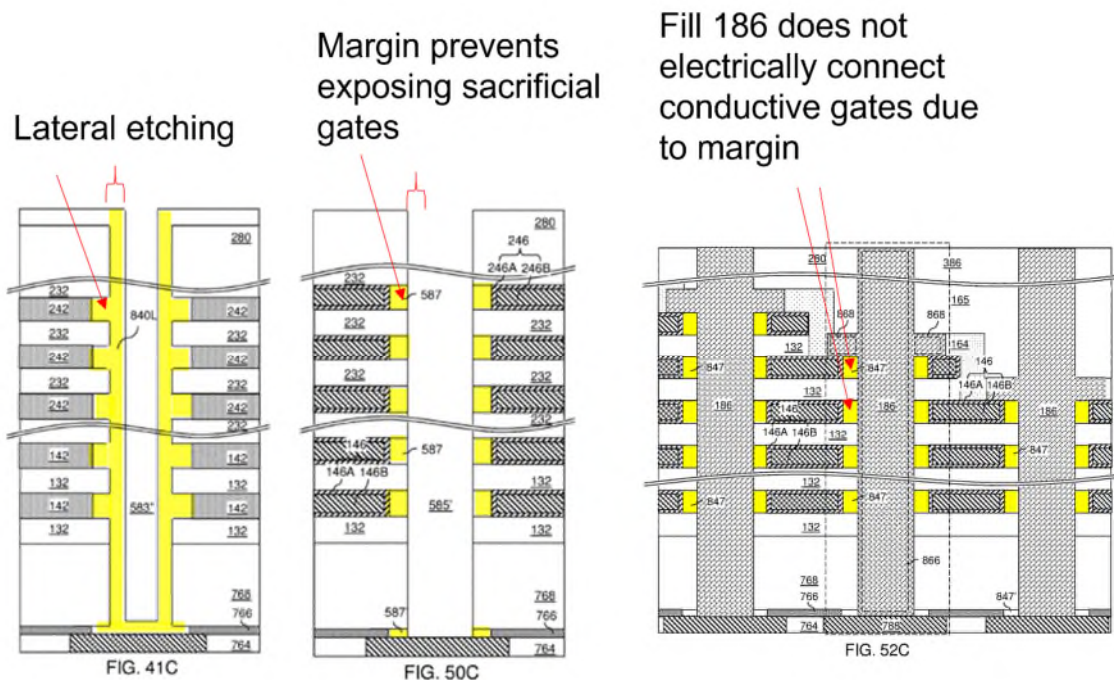


FIG. 50C

EX1037, Cui, Figs. 40C, 41C, 50C, 44:55-45:25 (processing to form cavities), 45:46-60 (liner), 48:17-33 (etch of bottom liner). As shown below, even though there is lateral etching to a degree, because of the extra space with dielectric, the TAC core does not physically contact the sacrificial gates.



Id., Figs. 41C, 50C, 52C, 49:16-52 (conductive fill).

48. Another advantage is that the extra space creates a greater amount of dielectric material between the conductive gate and the TAC core. Capacitive coupling occurs between two conductive elements with a dielectric spacer therebetween, but the thicker the space, the less coupling. This coupling, in short, creates issues such as noise that interferes with operation of the device and current leakage. Liu, for example, discloses a 3D memory with contacts (440) shown below. EX1115, Liu, [0038]. Liu, too, discloses recessing conductive layers to provide extra room for the dielectric liner, thereby isolating the conductive layers from the TACs and avoiding leakage current (i.e. shorting):

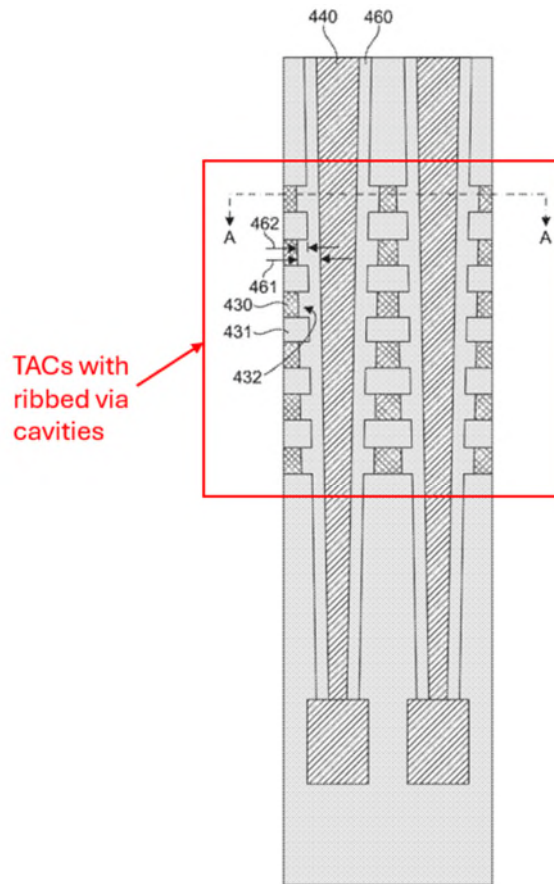
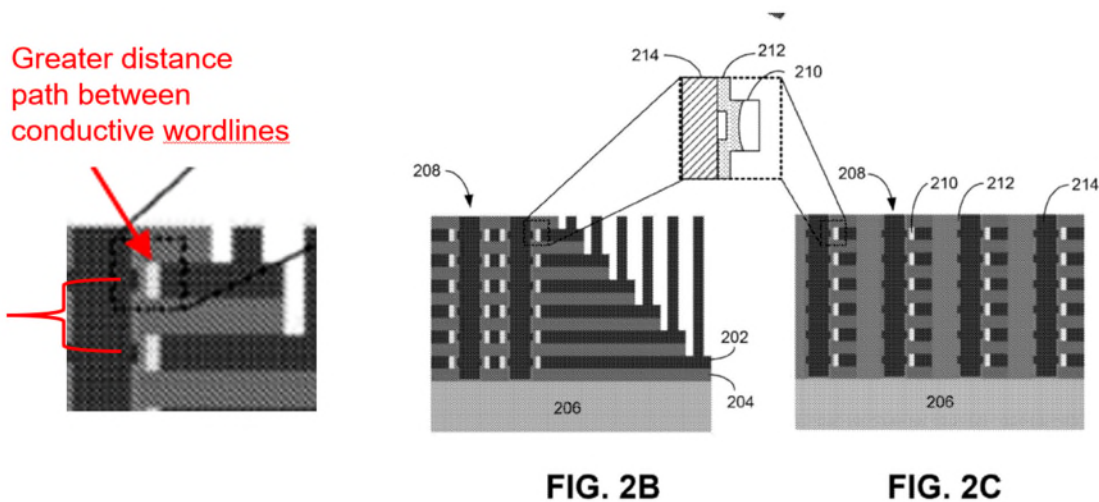


FIG. 7

Id., Fig. 7, [0038] (3D NAND memory). Liu describes that: as “illustrated in the side view of FIG. 7 and the top view of FIG. 8, conductive layers 430 can be recessed proximate contacts 440 such that material of insulative layers 431 is closer to the contacts 440 than the material of the conductive layers 430. Such recesses 432 in the conductive layers 430 can be filled with insulative material, such as that of an insulative liner 460. ***Recesses can be included if additional isolation from the contacts 440 is desired.***” *Id.*, [0048]. Liu states: “Such ***electrical isolation*** can be accomplished at least in part by separating adjacent contacts by a distance 463 of at

least about 200 nm in some embodiments. ***In general, it is desirable to minimize capacitor coupling as much as possible.*** Electrical isolation can be achieved when capacitance between adjacent contacts and between contacts and conductive layer material is acceptable for a given circuit.” *Id.* As can be seen, the additional space provides additional room for the dielectric, which increases the distance between the conductive core TAC and the conductive gate, which in turn creates the additional electrical isolation.

49. Lilak, a 3D RRAM memory, also demonstrates this benefit:



EX1116, Lilak, WO 2019/066829, 2B-2C. The wordlines are 202. As can be seen above, they are recessed back. As further seen above, the path from one conductive wordline around the respective dielectric layer is longer due to the recess. Lilak explains: “Also, in the embodiment shown, the first conductive layers 202 are recessed from the etch pits 208 to increase leakage current suppression.” *Id.*, 7:12-

17. Lilak further discloses: “The disclosed embodiments are advantageous in the sense that a self-aligned selector layer is introduced (whereas the existing approach does not) and eliminates or significantly reduces the sneak leakage problem between adjacent vertical wordlines. The disclosed embodiments also allows for increased vertical scaling as the insulating layers between the wordlines can be scaled much further as sneak leakage is not an issue.” *Id.*, 7:18-23. Here, Lilak is disclosing the coupling and leakage current that can result from the “adjacent vertical wordlines” is reduced, because the recesses space them out more.

50. Dr. Campbell takes issue with my citation to the '322 patent to demonstrate that Cui discloses the same. EX2021, ¶138. But the point is that Cui discloses the exact same purpose of the extra space as the '322 patent. And the additional references above show this was extremely well known.

2. **A Ribbed Cavity Is Obvious Under Petitioner's Construction**

51. Dr. Campbell opines that “[b]ut as demonstrated above, it is my opinion that a POSITA would have been motivated to, and could have, found a gas that etches without selectivity.” EX2021, ¶135. I agree that a POSITA perhaps could have found an etch chemistry that minimizes any recesses. But Dr. Campbell does not dispute that finding such a chemistry was a “challenge” to a POSITA. *Id.* Thus, in my opinion, the non-challenging etch chemistries used to form TAC holes would naturally and predictably result in ribbed TAC profiles, consistent with the claimed

structure. Thus, in my opinion, there would be several obvious implementations of fabricating Nishikawa that would result in a ribbed TAC.

3. Petitioner Does Not Improperly Supply a Missing Limitation

52. I disagree with Dr. Campbell that forming a ribbed TAC is complex in the context of a POSITA. EX2021, ¶¶142-45. Dr. Campbell cites that it is a “challenge” to produce a particular profile. *Id.*, ¶142. That reference (EX1039, 2:59-67) says it is a challenge not to create a ribbed profile, because most etchants are not equally selective to silicon nitride and silicon oxide. Thus, this demonstrates that most etchants will naturally provide a ribbed shape when etching a hole in an alternating stack of dielectric and silicon nitride layers.

53. I also note that Liu demonstrates, to a POSITA, ribbed TACs were routine because he describes both side-by-side in simple terms:

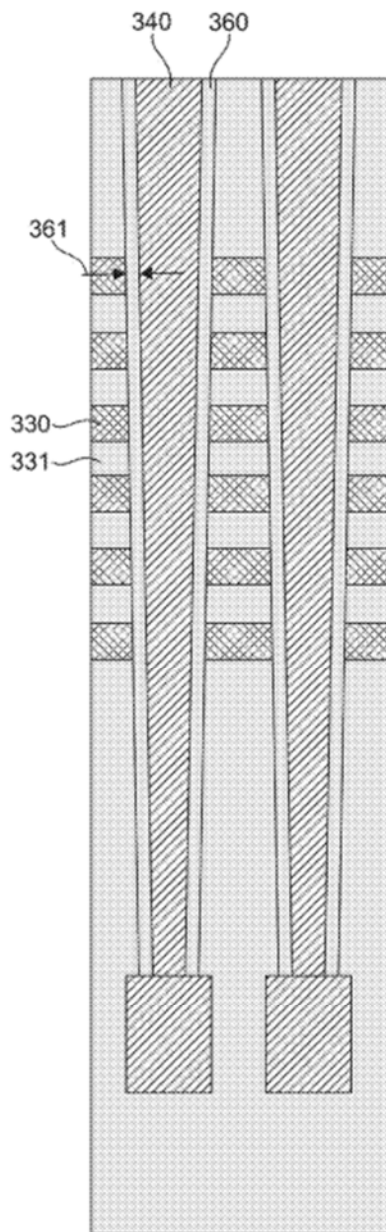


FIG. 6

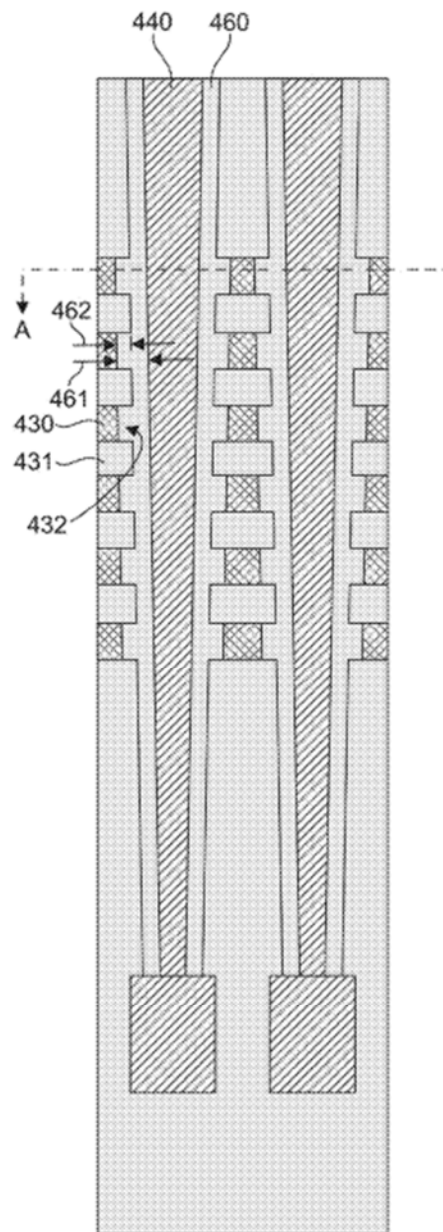


FIG. 7

EX1115, Liu, Figs. 6-7, [0047]-[0048].

54. Dr. Campbell also cites references that discuss removing the sacrificial gates, not recessing them. EX2021, ¶143. Regardless, these references assume the ability to remove the sacrificial gates as part of the gate replacement process (*supra*),

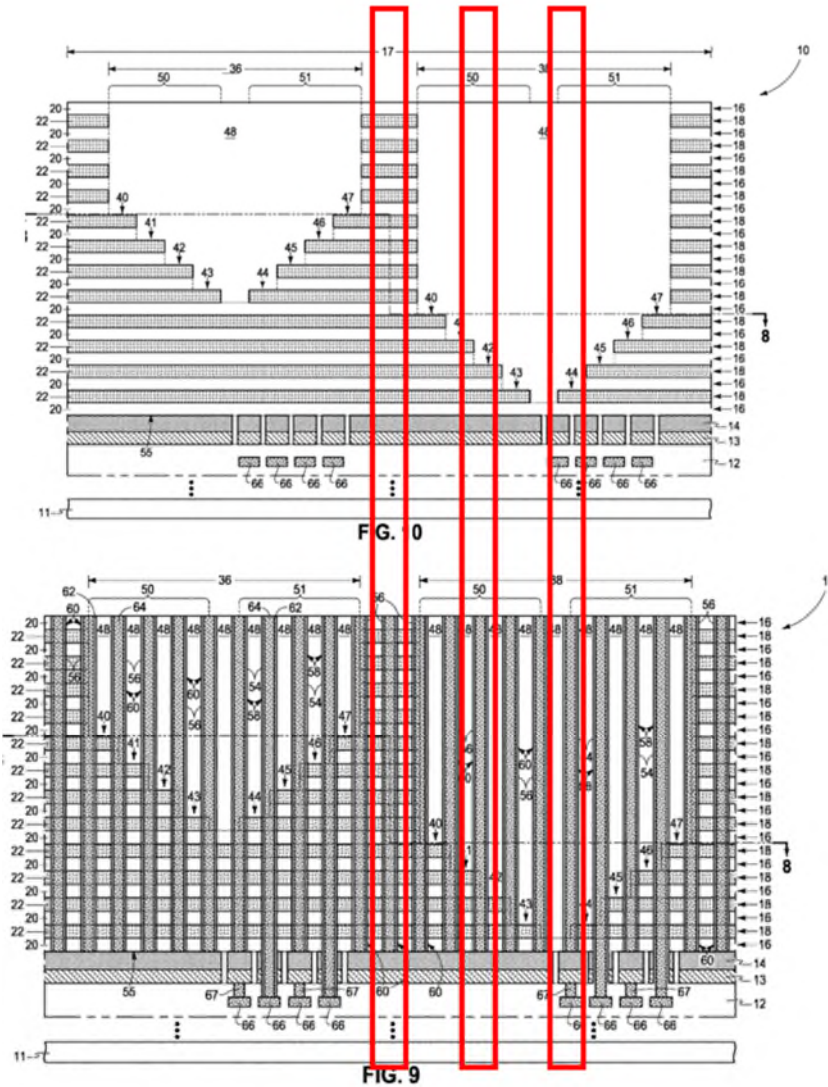
and thus a POSITA knew how to remove the gates (and simply recess them). Dr. Campbell again cites to replacement gate art in paragraphs 144 and 145 (citing EX2030). And while Dr. Campbell cites Kai (EX1027) that reference, at his own citation, provides a simple explanation of how to recess sacrificial gates. All this confirms that how to recess the sacrificial gates, e.g., an etch highly selective to etch the silicon nitride (and not much of the, e.g., silicon oxide) was routine. Again, the challenge was finding an etchant that was equally selective to both silicon nitride and silicon oxide.

D. TACs And Peripheral Contacts With Equal Diameters Were Obvious

55. I discuss that it was well known to form all contacts having the same diameter in my opening declaration. EX1003, ¶160 (citing EX1035). This solves the issue of over-etching, and as EX1035 discusses, allows for simpler etches (though solutions exist by using more complex etching options to etch at the same rate even when etching different sizes). EX1035, 33. Thus, it was “common” to fabricate contacts of all the same size (and thus same diameter size).

56. Dr. Campbell suggests that Tessariol discloses only etching holes through the “stack” at the same time. EX2021, ¶153. In my opinion, this mischaracterizes Tessariol. Tessariol discloses etching all of the contact and dummy contact holes in a single etch sequence, even though those holes extend through different combinations of dielectric fill and alternating layers. EX1036, Tessariol,

[0037]. That is, some of these holes extend through entirely alternating dielectric and sacrificial gate layers, while some extend through some of those layers and some dielectric fill, while others extend almost entirely through dielectric fill:

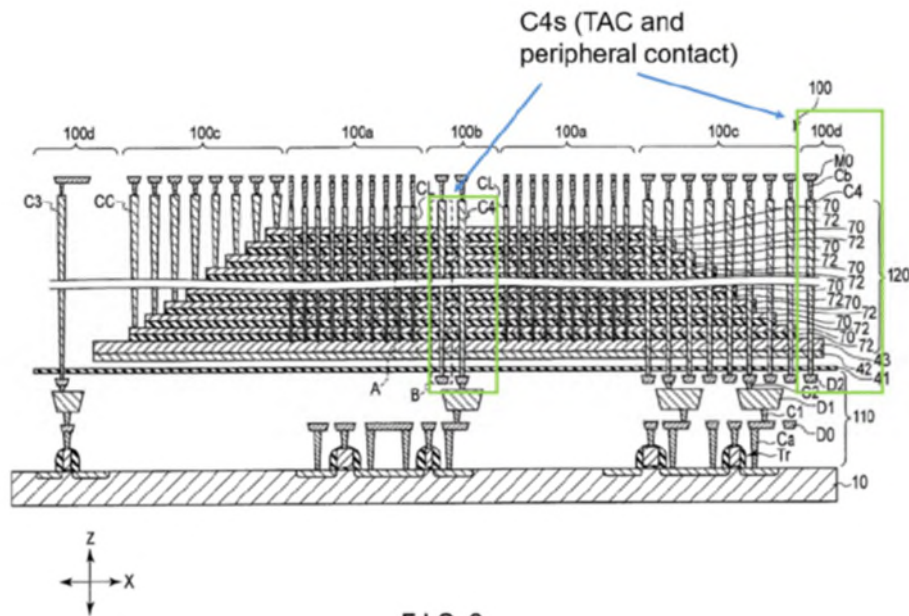


Id., Figs. 9, 10. Similarly, the contacts are “formed at the same time.” *Id.*, [0038]. Thus, that the holes are in different areas of the device, in which some areas are dielectric fill and other areas are mostly alternating stack (or all alternating layers),

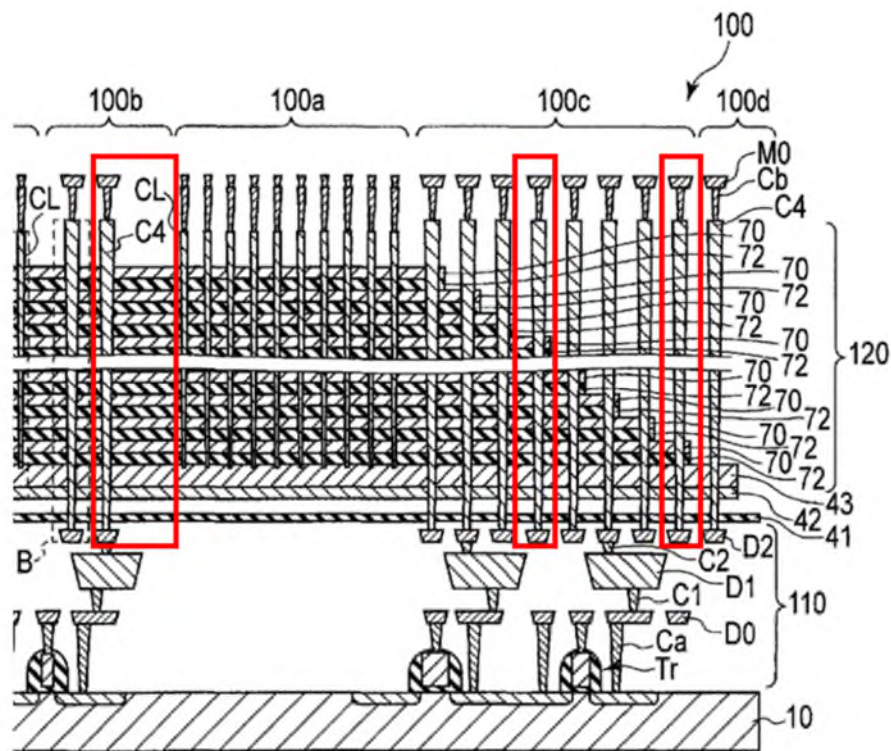
does not matter if a POSITA selects the appropriate common process. Tessariol demonstrates this. This is consistent with the '322 patent itself. EX1001, 12:28-49; EX1106, 63:9-64:3.

57. Tessariol's description is consistent with Nakajima and Mushiga. Mushiga discloses forming its through-array contacts using the same processing steps at the same time. EX1012, Mushiga, 10:31-58. Nakajima discloses forming all of its through-array contacts via the same process. EX1009, Nakajima, 7:37-8:11; EX1003, ¶161. This description is consistent with using the same diameter size to avoid etching issues. EX1035, 33; Pet. 68. And this is consistent with Tessariol expressly stating the same and showing the etches through different areas of the device. I also note that I understand that a patent rule Code of Federal Regulations 1.84(p)(4) requires the same numerals in figures denote the same structures. This is consistent with how a POSITA would have understood Mushiga, i.e., peripheral and TACs (both 586) are the same contact structure with the same diameters:

59. Dr. Campbell opines that Nakajima includes an error with respect to the C4 shown below. EX2021, ¶151. I disagree. As I explain above, a textbook (EX1035) discusses fabricating contacts of the same size and of different sizes, demonstrating that a POSITA would have understood that adjusting etch chemistry to account for such size-related variances was well known.



60. Dr. Campbell appears to attempt to draw a distinction between C3s, through only dielectric material, and C4s, allegedly through only the stack of alternating layers. This is inaccurate. As shown below, some C4s extend entirely through the dielectric-gate pairs, some extend through both dielectric fill and only some pairs, and some extend through only the dielectric (or at best, through one layer of the pairs). Thus, this alleged distinction between C3s and C4s is incorrect.

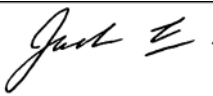


EX1009, Nakajima, Fig. 2.

61. Finally, I disagree with Dr. Campbell that in context (i.e., assuming the knowledge of a POSITA), that forming TACs and peripheral contacts with the same diameters was “complex.” These descriptions of Tessariol and Mushiga, for

example, demonstrate that a POSITA would have considered the implementation details known to a POSITA and did not feel the need to detail them in the respective disclosures. In other words, because forming such contacts using a common process was routine and well understood at the relevant time, the prior art appropriately omits detailed fabrication steps that a POSITA would have readily known how to implement.

62. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date:	<u>February 8, 2026</u>
Location:	<u>Austin TX</u>
Signature:	<u></u>
	DR. JACK C. LEE