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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

vs.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case No. IPR2025-00191
U.S. Patent No. 11,581,322

REMOTE DEPOSITION OF STEPHEN CAMPBELL

Friday, January 23, 2026

9:00 a.m. (CT)

Stenographically Reported by:

Joan Ferrara, RMR, FCRR

Job No. 2025-1008171

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January 23, 2026

9:00 a.m. (CT)

Deposition of STEPHEN CAMPBELL,
held remotely via Zoom, before Joan
Ferrara, a Registered Merit Reporter,
Certified Realtime Reporter, and
Notary Public.

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----- I N D E X -----

WITNESS	EXAMINATION BY	PAGE
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	MR. DUNTEMAN	124
	MR. JAMES	136

EXHIBITS REFERENCED	PAGE
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Exhibit 1001	61
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- - -

(REPORTER'S NOTE: All quotations
from exhibits are reflected in the manner in
which they were read into the record and do
not necessarily denote an exact quote from
the document.)

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STEPHEN CAMPBELL,
called as a witness, having been duly
sworn by a Notary Public, was examined
and testified as follows:
MR. JAMES: Thomas James, Orrick
Herrington & Sutcliffe, on behalf of
Petitioner Micron Technology Inc.
EXAMINATION BY
MR. JAMES:
Q. Good morning, Dr. Campbell.
A. Good morning.
Q. How are you doing today?
A. Trying to stay warm. Quite cold
where I am.
Q. You know, I grew up -- are you in
Minnesota?
A. Yes, minus 22 this morning.
Q. Yeah, I grew up near Grand
Rapids.
A. Oh.
Q. All right. We're here today to
discuss IPR Proceeding 2025-00191
instituted for review of United States
Patent No. 11,581,322.

1 S. CAMPBELL

2 Is that your understanding?

3 A. Yes.

4 Q. And if I refer to that patent as
5 the '322 Patent, will you understand what
6 I am referring to?

7 A. Yes.

8 Q. Can you please state your full
9 name for the record and spell it?

10 A. Stephen, S-T-E-P-H-E-N, Alan,
11 A-L-A-N, Campbell, C-A-M-P-B-E-L-L.

12 Q. You've been deposed before,
13 correct?

14 A. Yes.

15 Q. About how many times?

16 A. I think this is my fourth, might
17 be fifth.

18 Q. One of those depositions -- I'm
19 sorry, were you done?

20 A. Sorry.

21 Q. One of those depositions was for
22 IPR Proceeding 2025-00117 regarding United
23 States Patent No. 10,672,711, correct?

24 A. Yes, that's correct.

25 Q. How long ago was that?

1 S. CAMPBELL

2 A. I had two recent ones and I'm
3 just trying to remember one which is one.

4 Q. Was that one in November of 2025?

5 A. Again, I'm not sure which is
6 which. One was a week ago and one was
7 several months ago, but probably November,
8 yeah.

9 Q. Okay, excellent.

10 So I'll just run through some
11 ground rules here.

12 I'm going to ask you questions
13 and you're obligated to provide answers
14 absent instruction from your counsel not
15 to answer. Okay?

16 A. Yes.

17 Q. If you don't understand a
18 question, please let me know. Okay?

19 A. Okay.

20 Q. And if you don't, I'll assume
21 that you've understood the question.
22 Okay?

23 A. Yes.

24 Q. The court reporter is
25 transcribing our conversation, so please

1 S. CAMPBELL

2 respond to my questions verbally, not with
3 physical gestures. Okay?

4 A. Yes.

5 Q. If a question calls for a yes or
6 no answer, please answer "yes" or "no,"
7 not "uh-huh" or other such things. Okay?

8 A. Yes.

9 Q. We'll take a break about every
10 hour. Does that work for you?

11 A. Yes. If I need a break in
12 addition, I'll let you know.

13 Q. Excellent. And the only thing I
14 ask is that before you do so, you answer
15 any pending questions. Okay?

16 A. Yes.

17 Q. Is there any reason you're not
18 able to competently answer questions today
19 such as a medical condition?

20 A. No.

21 Q. Any other reason that you can't
22 give complete and accurate testimony
23 today?

24 A. No.

25 Q. Do you have any documents with

1 S. CAMPBELL

2 you?

3 A. I have a copy of my declaration.

4 That's all.

5 Q. And where are you located today?

6 A. I am in Arden Hills, Minnesota.

7 Q. And it appears you're in your
8 personal office, is that right?

9 A. That's correct.

10 Q. And that's at your home?

11 A. Yes.

12 Q. Is there anyone else in the room
13 with you today?

14 A. No.

15 Q. What did you do to prepare for
16 today's deposition?

17 MR. DUNTEMAN: One moment. I'll
18 remind the witness not to reveal any
19 confidential communications -- I'm
20 sorry, any communications with counsel
21 that would reveal privileged
22 information.

23 Q. You may answer.

24 A. And I will. Give me a moment.

25 I prepared for the deposition

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S. CAMPBELL

today by reviewing my declaration,
reviewing the patents that are --
particularly those that are mentioned in
the declaration, as well as -- I'll leave
that -- and also had a discussion with
lawyers at LW.

Q. And by LW, you mean Latham &
Watkins, is that correct?

A. Yes, that's correct.

Q. And how many attorneys did you
meet with?

A. Three.

Q. And what are their names?

A. Bobby Duntelman -- I'm sorry if I
say that wrong. Adam, and I don't
remember Adam's last name. And then there
was a third lawyer that came in and out,
was not -- was not there most of the time.

Q. And about how long did you spend
preparing for your deposition, for this
deposition?

A. Preparing total or preparing in
the meeting with the lawyers?

Q. Total first.

1 S. CAMPBELL

2 A. Total would be, I would guess
3 about 20 hours.

4 Q. And how long did you meet with
5 your attorneys for?

6 A. Five.

7 Q. Stepping back for a moment, do
8 you have any other devices with you
9 besides the laptop that you're taking this
10 deposition through?

11 A. I have a phone, but it's turned
12 off. I don't have any other devices.

13 Q. Do you have any other documents
14 or applications open on your computer?

15 A. The only applications on my
16 computer are this Zoom and Adobe which has
17 my declaration on it.

18 Q. So you have a printed version of
19 your declaration on your desk and an
20 electronic version open on your computer,
21 is that right?

22 A. That's correct.

23 Q. And are both copies of those
24 declarations clean?

25 A. Yes.

1 S. CAMPBELL

2 Q. Did you review anything not
3 submitted to the PTAB in this proceeding
4 to prepare for today's deposition?

5 MR. DUNTEMAN: I'll also again
6 instruct the witness not to reveal any
7 attorney/client communications or
8 attorney work product.

9 A. I'm not sure I understand the
10 question. Can you give me some
11 explanation on what kinds of things might
12 be in this category?

13 Q. White papers, patents, things of
14 that nature.

15 A. That were not disclosed to the
16 PTAB?

17 Q. In this proceeding, yes.

18 A. I certainly don't know of
19 anything that would be in that category.

20 Q. Besides your attorneys, did you
21 speak with anyone else in preparation for
22 this deposition?

23 A. No.

24 Q. Did your attorneys help you
25 prepare your declaration for this

1 S. CAMPBELL

2 proceeding?

3 MR. DUNTEMAN: Objection. I'll
4 instruct the witness not to reveal any
5 attorney/client communications. You
6 can talk about who is involved, but
7 nothing beyond that.

8 A. So the declaration is mine, it's
9 my name on it. However, there are parts
10 of it specifically referring to legal
11 matters that I'm not competent to draw.

12 And so yes, in areas where it was
13 primarily legal discussion, certainly I
14 had a great deal of help from lawyers.

15 Q. And were any other sections of
16 your report first drafted by someone other
17 than you?

18 MR. DUNTEMAN: I'm going to
19 object and instruct him not to answer
20 that. It's asking for attorney work
21 product.

22 Q. So regardless of authorship, you
23 adopted the opinions in your declaration
24 and you believe them to be true and
25 accurate, is that correct?

1 S. CAMPBELL

2 A. Yes.

3 Q. You submitted two declarations in
4 this proceeding, correct?

5 A. Yes.

6 Q. Do you recall when the first
7 declaration was submitted?

8 A. I do not. I'm sorry.

9 Q. Do you recall when you started
10 working on the second declaration?

11 A. I believe we started working -- I
12 started working on this in the fall, late
13 summer/early fall of 2025.

14 Q. And how much time did you spend
15 drafting your declaration?

16 A. Of course this is just an
17 estimate, it's not a hard number, but I
18 would guess it's about 50 hours total.

19 Q. I understand -- again, I
20 understand that you submitted two
21 declarations in this matter, but for the
22 remainder of this deposition when I refer
23 to your declaration, I'm referring to the
24 second declaration, unless I specifically
25 state otherwise. Okay?

1 S. CAMPBELL

2 A. I understand.

3 MR. DUNTEMAN: James -- or I'm
4 sorry, Thomas is your first name,
5 right?

6 MR. JAMES: Yes.

7 MR. DUNTEMAN: Can we just
8 clarify what exhibit number we're
9 talking about when we refer to second,
10 just to make sure we're on the same
11 page? Is that all right?

12 MR. JAMES: Mr. Duntelman, please,
13 no speaking objections. Please
14 restrict your participation to
15 objections to my questions.

16 MR. DUNTEMAN: Okay. Objection.

17 MR. JAMES: The deposition will
18 proceed and there will be clarity.
19 Thank you.

20 MR. DUNTEMAN: I'll note my
21 objection.

22 BY MR. JAMES:

23 Q. And for the record, your second
24 declaration is Exhibit 2021 to this
25 proceeding, is that correct?

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S. CAMPBELL

A. Yes, that's correct.

Q. Have you ever published more than
one paper on the same project?

MR. DUNTEMAN: Objection. Vague.

A. Yes.

Q. Have you ever read more than one
paper published on the same project?

MR. DUNTEMAN: Same objection.

A. Yes.

Q. Have you ever published an
initial paper on a project and then later
published a more detailed paper on the
same project?

MR. DUNTEMAN: Objection. Vague.

A. I'm trying to recall if I've ever
done that. Give me a moment.

Could I ask you to repeat the
question again?

Q. Have you ever published an
initial paper on a project and then
published a more detailed paper on the
same project later?

A. I probably did, yeah.

Q. And have you ever read a series

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S. CAMPBELL

of such papers published by others?

MR. DUNTEMAN: Objection. Vague.

A. Yes.

Q. So it's common for folks to
publish a series of papers on the same
project -- strike that question.

So it's common for academics to
publish a series of papers on the same
project, correct?

A. It is not unusual.

Q. And subsequent papers often
provide additional detail on that project,
isn't that right?

A. Certainly, I can't think of any
papers that I wrote that provide
additional detail. Usually, follow-up
papers address other aspects that weren't
addressed in the first paper.

Q. You've reviewed a lot of patents
and academic papers related to memory
devices, is that fair?

A. I reviewed some, yes -- well,
yeah.

What was the word that you used?

1 S. CAMPBELL

2 What was the adjective?

3 Q. You've reviewed -- excuse me.

4 I'll repeat the question.

5 You've reviewed a lot of papers

6 and -- I'll start again. I apologize.

7 You've reviewed a lot of papers

8 and academic papers related to memory

9 devices, is that fair?

10 A. Yes, I guess that's fair.

11 Q. In your experience, do patents

12 and academic papers illustrate all the

13 structures required to form a functional

14 memory device?

15 A. I guess I need to -- a bit

16 clarification on that. Are you saying do

17 these papers and patents provide

18 everything you would need to know to make

19 a device? Is that what you're asking?

20 Q. Yes.

21 A. Well, the answer is no.

22 Q. In your experience, patents and

23 academic papers are generally directed to

24 solving a specific problem for advancing a

25 novel idea, isn't that right?

1 S. CAMPBELL

2 MR. DUNTEMAN: Objection. Calls
3 for legal conclusions.

4 Q. I'll ask a different question.

5 In your experience, patents and
6 academic papers are generally directed to
7 solving a specific problem or advancing an
8 idea, isn't that right?

9 A. The way that you have phrased it,
10 it would seem all papers and patents have
11 that motivation. That isn't true, but it
12 is true for many.

13 Q. So it's true for many patents and
14 academic papers, correct?

15 A. For many, yes, correct.

16 Q. And in your experience, patents
17 and academic papers typically only
18 disclose enough context to the reader to
19 understand the problem being solved or the
20 advancement being disclosed, isn't that
21 right?

22 MR. DUNTEMAN: Objection. Form.

23 A. Could you repeat the question?

24 Q. In your experience, patents and
25 academic papers typically only disclose

1 S. CAMPBELL

2 enough context for a reader to understand
3 the problem being solved or the
4 advancement being disclosed, isn't that
5 right?

6 A. When you say "only" -- is that
7 the word I heard?

8 MR. JAMES: Court reporter, can
9 you read back my question, please?

10 (The requested portion was read
11 back by the Court Reporter.)

12 A. I guess my response is -- can you
13 reword it? Let me put it that way.

14 Q. What about the question is
15 confusing you?

16 A. The term "only."

17 Q. In your experience, patents and
18 academic papers typically disclose enough
19 context for a reader to understand the
20 problem being solved or the advancement
21 being disclosed, isn't that right?

22 A. Yes.

23 Q. And they do not typically
24 disclose more than that, is that right?

25 I'll reask the question.

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S. CAMPBELL

In those patents and --

THE COURT REPORTER: I think

Mr. James is frozen.

MR. DUNTEMAN: Yeah, it's not

just me. Can we go off the record for

a moment?

THE COURT REPORTER: Sure. We're

off the record.

(Pause.)

BY MR. JAMES:

Q. So those patents and academic
papers typically do not disclose more
context than is needed to understand the
problem being solved or the advancement
contained therein, isn't that right?

MR. DUNTEMAN: Objection. Form.

A. I can't say universally that
that's true.

Q. I asked typically.

A. Typically, oh, my apologies.

Typically, that's true.

Q. If I use the term "POSITA," do
you know what I mean?

A. Yes.

1 S. CAMPBELL

2 Q. So a POSITA would have looked to
3 related works to gain a better
4 understanding of a subject matter of a
5 given project, correct?

6 MR. DUNTEMAN: Objection. Form.

7 A. A POSITA would -- I'm sorry, I
8 didn't hear half of it. Go ahead again.

9 Q. So a POSITA would have looked to
10 related works to gain a better
11 understanding of a subject matter of a
12 given project, correct?

13 A. Yes, that's correct.

14 Q. Were the placement of dummy
15 channels a structural aspect of 3D NAND
16 memory prior to the priority date of the
17 '322 Patent?

18 MR. DUNTEMAN: Objection.

19 A. Dummy channels were known prior
20 to the patent.

21 Q. Were they a structural aspect of
22 3D NAND memory devices?

23 MR. DUNTEMAN: Objection.

24 A. They are a structural element in
25 3D NAND devices.

1 S. CAMPBELL

2 Q. Was the size of peripheral
3 contacts a structural aspect of 3D NAND
4 memory prior to the priority date of the
5 '322 Patent?

6 MR. DUNTEMAN: Objection. Vague.

7 A. You're asking are they
8 structural?

9 Q. I'm asking --

10 A. They were known.

11 Q. I'm asking if the size of the
12 contact is a structural aspect.

13 A. The size of the structure of
14 the --

15 Q. Peripheral device.

16 A. Peripheral device. Well, the
17 peripheral device is not -- contacts to a
18 peripheral device are not generally viewed
19 as structural elements. They are outside
20 the array.

21 Q. Being outside the array makes
22 something not structural?

23 A. When we talk about structural
24 elements in a 3D device, we're mainly
25 concerned with the memory array.

1 S. CAMPBELL

2 Q. So a peripheral contact is not a
3 structural device and in a 3D NAND memory?

4 A. Of course one can say that
5 anything is a structural element. What
6 I'm trying to communicate to you is that
7 that's not the primary purpose of
8 peripheral devices -- peripheral contacts,
9 sorry -- peripheral contacts.

10 Q. And the size of the peripheral
11 contact is also not a structural aspect of
12 a 3D NAND memory device?

13 A. To the extent that the peripheral
14 contact is a structural element, the size
15 would impact its ability to be -- to
16 provide structural support. The larger
17 the contact, the more structural support,
18 in principal, it would offer.

19 Q. But the size itself is
20 structural. Do you disagree?

21 MR. DUNTEMAN: Objection. Form.

22 A. You're asking me if the
23 peripheral contact, the size of the
24 peripheral contact is a structural
25 element. Didn't we just answer that?

1 S. CAMPBELL

2 Again, let's hear it again.

3 Q. I'll ask my original question.

4 Were the size of peripheral
5 contacts a structural aspect of 3D NAND
6 memory?

7 A. The size of the peripheral
8 device --

9 Q. No, no, the peripheral contact.

10 A. Peripheral contact, my
11 apologies -- the size of the peripheral
12 contact would have some effect on the
13 structural elements.

14 Q. But your testimony is that the
15 size of the peripheral contact itself
16 isn't a structure in a 3D NAND memory
17 device?

18 MR. DUNTEMAN: Objection.

19 Mischaracterizes testimony.

20 A. As I said before, the -- well,
21 okay, so let me -- the structure in a 3D
22 device that is most prone to structural
23 issues is the memory array. Full stop.

24 There are other areas where
25 structural concerns can arise and making

1 S. CAMPBELL

2 one of these could be peripheral devices
3 or contacts to peripheral devices.

4 And looking at that limited
5 scope, not the memory array, just that
6 scope, the size of the contact could
7 affect the stability.

8 Q. Were the size of through-array
9 contacts a structural aspect of 3D NAND
10 memory?

11 A. Were the size of --

12 Q. Through array-contacts.

13 A. Through array, oh.

14 Because of the -- well, I'm using
15 to calling them TACs -- because the TAC
16 goes through the array, it does have an
17 affect on structural stability of the
18 memory array.

19 Q. And the TAC itself is a structure
20 in a 3D NAND memory, correct?

21 A. Yes, that's correct.

22 Q. And a peripheral contact is a
23 structure in a 3D NAND memory device,
24 correct?

25 A. Yes.

1 S. CAMPBELL

2 Q. You have been professor at the
3 University of Minnesota since 1986, is
4 that correct?

5 A. That is correct.

6 Q. You haven't engaged in CMOS
7 fabrication technology, correct?

8 A. I haven't is what you said?

9 Q. That's correct.

10 A. No, that is not correct.

11 Q. Okay. We'll come back to that.

12 You would characterize your work
13 generally as directed to fabrication of
14 semiconductor devices and semiconductor
15 materials, correct?

16 A. Yes, that's correct.

17 Q. And your work has most
18 prominently been related to CMOS devices,
19 bio MEMS devices, solar cells, and
20 portable devices, is that correct?

21 A. Yes. In my publications,
22 that's -- that's my primary areas.

23 Q. As a consultant, but not in your
24 academic work, you worked on solid state
25 devices, is that correct?

1 S. CAMPBELL

2 A. Yes.

3 Q. And your work on solid state
4 devices occurred around 2023, is that
5 correct?

6 A. I have done -- certainly I did
7 work in 2023, that's correct. I did
8 consulting work beyond that.

9 Q. And prior to August 21, 2018, you
10 hadn't engaged in fabrication technologies
11 of 3D NAND memory devices, is that
12 correct?

13 A. That's correct.

14 MR. DUNTEMAN: Objection.

15 A. I'd like to make a -- sorry, I'd
16 like to make an addendum to my response to
17 you.

18 When you -- am I allowed to do
19 this?

20 MR. DUNTEMAN: Please proceed,
21 Dr. Campbell.

22 THE WITNESS: Very well.

23 A. When we say did you work in 3D
24 devices, the work that I have done
25 certainly is part of 3D devices.

1 S. CAMPBELL

2 The high-K material, for example,
3 I'm the one that brought that into the
4 semiconductor industry, and it's now used
5 commonly in 3D.

6 There are other areas in terms of
7 the materials and the processing
8 technology that were done in my research,
9 and some of those have carried over into
10 3D applications.

11 In terms of working directly on
12 3D, that date is about right.

13 Q. Thank you. Okay.

14 For the remainder of the
15 deposition, let's use August 21, 2018 as
16 the applicable date for questions in this
17 deposition as they relate to the state of
18 the art in your experience unless I state
19 otherwise. Is that okay?

20 A. Sure.

21 (Reporter seeks clarification.)

22 BY MR. JAMES:

23 Q. Is it fair to say that you do not
24 have personal experience designing a fully
25 integrated 3D NAND memory device?

1 S. CAMPBELL

2 A. You would have to explain to me
3 what you mean by "design."

4 Q. I actually think that's very
5 clear.

6 MR. DUNTEMAN: Objection.

7 Argumentative.

8 A. Perhaps you haven't worked in the
9 area. I'll make that an assumption.

10 There are multiple designers that
11 work on 3D NAND. You have the circuit
12 designers that determine what transistors
13 connect to which transistors. You have
14 process designers. This is what I spent
15 most of my career on. It's called the
16 process architecture, what processes
17 you're going to run, in what sequence,
18 what materials, how you're going to
19 deposit and how you're going to etch.

20 That's a process engineer and
21 some people would consider that design. I
22 certainly -- but again, design is a
23 malleable word and I want to make sure I
24 understand what you're saying.

25 People that are doing the circuit

1 S. CAMPBELL

2 design could never do the process design,
3 and the other side around is fairly
4 accurate as well. So --

5 Q. Okay.

6 A. So I don't think there's anybody
7 that could do the entire structure for a
8 3D NAND.

9 Q. Thank you for the clarification.

10 Is it fair to say that you do not
11 have personal experience with process
12 design for a fully integrated 3D NAND
13 memory device?

14 MR. DUNTEMAN: Objection. Vague.

15 A. That runs into a problem. I did
16 some work with a company on memory devices
17 and I had signed an NDA and I can't tell
18 you. I'm not allowed to disclose.

19 Q. That work occurred after August
20 21, 2018 --

21 A. Yes.

22 Q. All of the remaining questions
23 related to your experience are related to
24 the time period before August 21, 2018.

25 A. Oh, my apologies. I didn't

1 S. CAMPBELL

2 realize that.

3 Prior to 2018, I did not work in
4 3D NAND.

5 Q. Is it fair to say that you do not
6 have personal experience designing 3D NAND
7 structures -- strike that question.

8 Is it fair to say that you do not
9 have personal experience designing a gate
10 replacement process for a 3D NAND memory
11 device?

12 MR. DUNTEMAN: Objection. Form.

13 A. Explain to me what you mean by
14 "designing."

15 Q. Designing --

16 A. In particular, designing the
17 replacement process?

18 Q. Yes.

19 A. So are you asking the sequence of
20 the processes and the materials? I'm just
21 trying to understand the scope of what
22 you're asking.

23 Q. The sequence of processes, yes.

24 A. Certainly, I understand that
25 sequence and understand the processes and

1 S. CAMPBELL

2 the limitations of the processes that
3 would go into it.

4 Q. But the question is whether you
5 had personal experience with such
6 processes.

7 A. I've had experience in all of
8 those processes.

9 Q. Again, you've already testified
10 that you have not worked on 3D NAND prior
11 to August 21, 2018.

12 A. Yes.

13 Q. So I'm asking, is it fair to say
14 that you do not have personal experience
15 designing a gate replacement process for a
16 3D NAND memory device?

17 A. And what I'm saying is that that
18 process is not limited to 3D NAND. I have
19 designed that process for other
20 applications, but not for 3D NAND.

21 Q. Prior to August 21, 2018?

22 A. Yes.

23 Q. Is it fair to say that you did
24 not have personal experience designing 3D
25 NAND structures required for the gate

1 S. CAMPBELL

2 replacement process in a 3D NAND device?

3 MR. DUNTEMAN: Objection. Vague.

4 A. Again, because I'm under oath, I
5 would like to ask you to ask it one more
6 time.

7 Q. Is it fair to say that you did
8 not have personal experience designing 3D
9 NAND structures required for the gate
10 replacement process?

11 MR. DUNTEMAN: Objection. Asked
12 and answered.

13 A. I think I just answered that
14 question.

15 Q. You actually asked me to ask you
16 the question again. So please answer it.

17 A. I mean, my previous answer. I
18 think that's the same question.

19 Q. They're not. The first question
20 related to process of -- the process for
21 it, which means how do I exhume the
22 materials for the sacrificial layers and
23 then deposit the metal in those layers.

24 But then the second question
25 relates to the structures required to

1 S. CAMPBELL

2 support that process. So they're
3 different questions. So I'll ask it
4 again.

5 A. Oh, I missed that.

6 Q. Let me ask the question again.

7 Is it fair to say that you do not
8 have personal experience designing 3D NAND
9 structures required for the gate
10 replacement process?

11 MR. DUNTEMAN: Objection. Vague.

12 A. Okay. Again, I have designed
13 processes that removes sacrificial layers
14 and put in other materials prior to 2018,
15 but not applied to 3D NAND.

16 Q. Again, that doesn't answer my
17 question.

18 A. I don't know what I'd say.

19 MR. DUNTEMAN: Objection.

20 Argumentative.

21 Q. So as we discussed, the first --
22 the first question about the gate
23 replacement process was about the process
24 itself.

25 There are structures formed in 3D

1 S. CAMPBELL

2 NAND that require -- that are required for
3 that process.

4 The question I'm asking now
5 relates to those structures specifically
6 in your experience. I'll ask my question
7 again.

8 Is it fair to say that you did
9 not have personal experience designing 3D
10 NAND structures required to support the
11 gate replacement process?

12 MR. DUNTEMAN: Objection. Form.

13 A. I'm trying to parse your words.
14 Are you saying that doing the same or very
15 similar process in a different application
16 does not satisfy the question that you're
17 asking?

18 Q. Are you refusing to answer my
19 question?

20 A. I'm trying to understand your
21 question.

22 MR. DUNTEMAN: Objection.
23 Argumentative.

24 A. Prior to 2018 --

25 Q. You understand what a structure

1 S. CAMPBELL

2 is, correct?

3 A. Yes, I understand what a
4 structure is.

5 Q. And you understand what a process
6 is, correct?

7 A. Absolutely.

8 Q. And you understand that
9 structures are created by processes,
10 correct?

11 A. Yes.

12 Q. And you understand that processes
13 and structures are different, is that
14 correct?

15 A. Yes, of course.

16 Q. So when I ask if you have
17 experience designing structures required
18 to support the gate replacement process,
19 you understand what I mean, correct?

20 A. Yes.

21 Q. Okay. So then I'll ask my
22 question.

23 Is it fair to say that you do not
24 have personal experience designing 3D NAND
25 structures required to support the gate

1 S. CAMPBELL

2 replacement process?

3 MR. DUNTEMAN: Objection. Form.

4 A. This is a difficult question for
5 me because I made structures that are very
6 similar and using similar processes.

7 If the question is did I design a
8 process flow that's exactly like the 3D
9 process of -- well, basically a gate last
10 process, then not for 3D. I have not done
11 it for 3D.

12 Q. Okay. So your answer to the
13 question, is it fair to say that you did
14 not have personal experience designing 3D
15 NAND structures required to support the
16 gate replacement process, is no?

17 MR. DUNTEMAN: Objection.

18 Mischaracterizes testimony.

19 A. You're trying to force me to say
20 something that I'm not saying.

21 If the structures are the same or
22 very similar, but it's not applied in 3D,
23 I've made that structure, I've designed
24 that structure, but it just wasn't applied
25 in 3D.

1 S. CAMPBELL

2 I don't understand why that isn't
3 understandable to you.

4 Q. We could move on.

5 Is it fair to say that you did
6 not have personal experience designing the
7 placement of dummy channels in 3D NAND
8 memory devices?

9 A. Yes, that would be true.

10 Q. Is it fair to say that you did
11 not have personal experience designing the
12 structure of dummy channels in 3D NAND
13 memory devices?

14 A. Again true.

15 Q. Is it fair to say that you did
16 not have personal experience with the use
17 of dummy structures in any memory
18 technology developed in the prior 20
19 years?

20 A. Yes, that's true.

21 Q. So is it fair to say that you
22 didn't have personal experience as to why
23 dummy structures are used at pattern edges
24 in memory devices?

25 A. Again, this is as of 2018?

1 S. CAMPBELL

2 Q. Yes.

3 A. Or is this now?

4 Q. No. All of these questions are
5 prior to August 21, 2018.

6 A. The answer to that -- I'm sorry,
7 I agree with what you said.

8 Q. So the answer is yes?

9 A. The answer is yes.

10 Q. So is it fair to say that you
11 didn't have personal experience as to why
12 dummy structures are used at array edges
13 in memory devices. Let me clarify --

14 A. 2018, yes.

15 Q. Thank you.

16 And that's also true for 3D NAND
17 memory devices, is that correct?

18 A. There are aspects of 3D NAND that
19 I would have been aware of in 2018, but
20 not the entire structure.

21 Q. So is it fair to say you didn't
22 have personal experience as to why dummy
23 structures are used at array edges in 3D
24 NAND memory devices?

25 MR. DUNTEMAN: Objection. Vague.

1 S. CAMPBELL

2 A. As of 2018, I was not aware of
3 dummy structures. So yes.

4 Q. So then it's fair to say that you
5 did not have experience as to why dummy
6 channels are used in contact regions of 3D
7 NAND memory devices, is that correct?

8 MR. DUNTEMAN: Same objection.

9 A. Again, as of 2018, yes.

10 Q. So is it fair to say that you did
11 not have experience as to why dummy
12 channels would be interspersed with active
13 memory cells in a 3D NAND memory stack?

14 MR. DUNTEMAN: Same objections.

15 A. As of 2018, yes.

16 Q. Is it fair to say that you do not
17 have personal experience designing etch
18 chemistries for high aspect ratio features
19 of 3D NAND memory devices?

20 MR. DUNTEMAN: Objection. Form.

21 A. I have, prior to 2018, developed
22 high aspect ratio etch processes, but not
23 for the 3D stack specifically.

24 Q. Is it fair to say that you don't
25 have personal experience with the

1 S. CAMPBELL

2 formation of through-array contacts in 3D
3 NAND memory devices?

4 MR. DUNTEMAN: Same objection.

5 A. It's almost the same question.

6 As of 2018, no.

7 Q. If I use the term "ribbed via
8 cavity," do you understand what I'm
9 referring to?

10 A. Your mouth was pointed away from
11 the computer.

12 Q. Apologies. A little bit
13 handicapped on my end due to some computer
14 issues here.

15 If I use the term "ribbed via
16 cavity," do you understand what I'm
17 referring to?

18 A. Yes.

19 Q. Do you understand that a ribbed
20 via cavity was a known structure for
21 through-array contacts?

22 A. As of 2018 again?

23 Q. Always.

24 A. No, I'm sorry, I did not know
25 that prior to 2018.

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2 Q. Is it fair to say that you didn't
3 have any personal experience with the
4 formation of through-array contacts with
5 ribbed via cavities?

6 A. As of 2018, yes, I was not aware
7 of those.

8 Q. Did you know what a short circuit
9 was?

10 A. A short circuit?

11 Q. Yes.

12 A. Yes, of course. I taught
13 electrical engineering.

14 Q. Would a POSITA have known what a
15 short circuit was?

16 A. Yes.

17 Q. Would a POSITA have known how to
18 avoid short circuits generally?

19 A. It's kind of a vague question,
20 how to prevent short circuits.

21 A POSITA would understand what a
22 short circuit is and what is required to
23 remove it. The problem always is less
24 than the concept that I need to have some
25 way to break the conduction of that. The

1 S. CAMPBELL

2 problem is usually how to do it, not in
3 general what to do.

4 Q. In general, a POSITA would
5 consider a short circuit in a 3D NAND
6 memory device to be a bad thing, correct?

7 MR. DUNTEMAN: Objection.

8 A. Well, it depends on what
9 structure you're talking about. If you're
10 talking about a TAC, then you want to have
11 the lowest possible resistance from the
12 bottom of the TAC, top of the TAC, and
13 ideally it would be a short circuit.

14 Q. Well, what you just referred to
15 are intentionally created conductive
16 paths. I'm asking about unintentional
17 short circuits.

18 MR. DUNTEMAN: Objection.

19 Mischaracterizes the testimony.

20 Hold on, Dr. Campbell. Let me
21 get that objection on the record.

22 THE WITNESS: Sorry.

23 MR. DUNTEMAN: Okay. Go ahead.

24 A. The question answers itself. If
25 it's an unintended current path, then by

1 S. CAMPBELL

2 the word "unintended" it means you don't
3 want it there. So there isn't really much
4 of a question to be answered.

5 MR. JAMES: We've been going for
6 about an hour. Would you like to take
7 a break?

8 THE WITNESS: Sure.

9 MR. JAMES: How about we just
10 take a quick five minutes for this
11 one?

12 THE WITNESS: Okay.

13 (Recess taken from 9:58 a.m. to
14 10:06 a.m. CT)

15 BY MR. JAMES:

16 Q. You were not an expert in 3D NAND
17 memory design, were you?

18 MR. DUNTEMAN: Objection. Vague.

19 A. Not as of 2018.

20 Q. So what experience did you have
21 to opine on what structures would have
22 been suitable to fabricate a functional 3D
23 NAND memory device prior to August 21,
24 2018?

25 A. As I mentioned earlier, most of

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2 my experience over these years has been a
3 process architect. I've developed
4 individual processes, but they're always
5 incorporated into different structures.

6 I have been very successful in
7 that area. And the ability to understand
8 all of the materials that are used in 3D
9 NAND, I have decades of experience with
10 them. I know what they are. I know what
11 their limitations are. I know how they're
12 deposited. I know what materials will
13 etch them. I know what sequence you have
14 to put them in. All of the materials that
15 are in here are ones that I have worked
16 with for a long time.

17 So once one is given the basic
18 structure, it is in my bailiwick to be
19 able to understand the processes and the
20 materials that they're going to use in
21 order to achieve this goal.

22 So once I was exposed to the 3D
23 area, let's say I picked it up very
24 quickly. Yeah.

25 Q. But when you picked it up, it was

1 S. CAMPBELL

2 after August 21, 2018, correct?

3 A. Absolutely correct.

4 Q. So I'm about to ask you a series
5 of questions. All of the following
6 questions are asked in the general context
7 of 3D NAND memory. Is that understood?

8 A. Yes.

9 Q. And I'll let you know when that
10 stops being true. Understood?

11 A. Understood.

12 Q. Would it have been suitable --
13 would it have been a suitable option to
14 employ a circular TAC in a 3D NAND memory
15 stack?

16 MR. DUNTEMAN: Objection. Form.

17 A. It would -- I'm sorry, the first
18 part of it was would it --

19 Q. Would it have been a suitable
20 option to form through array -- I
21 apologize. I'll start again.

22 Would it have been a suitable
23 option to employ circular through-array
24 contacts in a 3D NAND memory stack?

25 A. It all depends on the design of

1 S. CAMPBELL

2 the 3D device. You can't say in every
3 case that that's the best thing to do, but
4 it certainly is an option.

5 Q. Would it have been a suitable
6 option to form through-array contacts and
7 peripheral contacts at the same time?

8 MR. DUNTEMAN: Objection. Form.

9 A. It would be advantageous to do
10 them at the same time.

11 Are you asking would a POSITA
12 know to do that?

13 Q. Would it have been a suitable
14 option to form through-array contacts and
15 peripheral contacts with the same
16 diameter?

17 A. As virtually everything in the
18 processing world, there are engineering
19 tradeoffs. So there are advantages to
20 doing that and disadvantages. And if you
21 want to say it's always good or always
22 bad, I can't say that. It all depends.

23 Q. But it would have been a suitable
24 option, correct?

25 A. It would be a suitable option,

1 S. CAMPBELL

2 again depending on the rest of the
3 structure of the array would it have been
4 a suitable option to form circular TACs in
5 a 3D NAND memory stack.

6 MR. DUNTEMAN: Objection.

7 Answered.

8 A. Would it be suitable to put them
9 into a TAC -- sorry, the TAC into an
10 array?

11 Q. Would it have been a suitable
12 option to form a circular TAC in a 3D NAND
13 memory stack?

14 A. Yes, yes.

15 Q. Would it have been a suitable
16 option to form a TAC having a ribbed via
17 cavity?

18 MR. DUNTEMAN: Objection. Form.

19 A. There are advantages to that.
20 But again, it all depends on the design of
21 your array and your processing
22 capabilities.

23 Q. In general, would it have been
24 suitable?

25 A. I can't say in general.

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2 MR. DUNTEMAN: Objection.

3 A. It depends on how you design your
4 array.

5 Q. Were circular TACs in 3D NAND
6 memory stacks known prior to August 21,
7 2018?

8 A. Yes.

9 Q. So there are applications where
10 such TACs would have been suitable,
11 correct?

12 A. Yes, there are some applications.

13 Q. Would it have been a suitable
14 option to form dummy channels in the
15 contact region of a 3D NAND memory device?

16 MR. DUNTEMAN: Objection. Form.

17 A. I'm trying to be as accurate as I
18 can. I have the sense that you're trying
19 to push me into saying that it will always
20 be a good thing, and that just isn't true.
21 It depends on the array.

22 Q. That's not what I'm asking.

23 In all these series of questions,
24 I'm just asking you what's suitable.

25 A. Okay. It's suitable if the array

1 S. CAMPBELL

2 accepts it.

3 Q. So for clarity, I will ask my
4 question one more time.

5 Would it have been a suitable
6 option to form dummy channels in the
7 contact region of a 3D NAND memory device?

8 A. Explain for me exactly what you
9 mean by contact area.

10 Q. Do you know what the contact
11 region of a 3D NAND memory device is?

12 A. Are we talking about the
13 staircase?

14 Q. The staircase can be part of the
15 contact region, sure.

16 A. So I've got to think about that
17 for a moment because normally TACs go
18 through the core memory --

19 Q. Let me -- there's a confusion.
20 Let me ask the question again.

21 Would it have been suitable to
22 form dummy channels in the contact region
23 of a 3D NAND memory device?

24 A. Yes. Again, if you're willing to
25 accept the tradeoffs, that's a

1 S. CAMPBELL

2 possibility.

3 Q. Would it have been a suitable
4 option to form dummy channels at array
5 edges?

6 MR. DUNTEMAN: Objection. Vague.

7 A. It is an option, yes, that would
8 be an option.

9 Q. Would it be a suitable option?

10 A. Suitable for who? For what?
11 What's the design? There are pluses and
12 minuses.

13 Q. Would it have been a suitable
14 option to form dummy channels at pattern
15 edges?

16 MR. DUNTEMAN: Same objection.

17 A. Same response. Is the benefit of
18 those structures worth the tradeoffs that
19 you have. It's an option, but it isn't
20 good for everything.

21 Q. Would it have been a suitable
22 option to form dummy channels interspersed
23 with active memory cells to deposit
24 etchant for the gate replacement process?

25 MR. DUNTEMAN: Same objection.

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A. Let me have you repeat it.

Q. Would it have been a suitable
option to form dummy channels interspersed
with active memory channels to deposit
etchant for the gate replacement process?

A. It's a little bit of a confusing
question to me because dummy structures
typically are filled structures, they have
dielectrics that fill the cavity, and
you're talking about using them for
sacrificial layer structure sequence.

So I guess is it possible...

You have to have some kind of
cavity to etch the sacrificial layer.

Q. Suppose -- let me clarify.

MR. DUNTEMAN: Counsel, let him
finish answering the question.

MR. JAMES: Okay.

MR. DUNTEMAN: Go ahead,
Dr. Campbell.

A. You want me to continue? I'm
just -- I don't know what's happening
here.

MR. DUNTEMAN: Yeah, fair enough.

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I was just pointing out to counsel let
him finish his answer, and then if we
need clarification we can do that.

But go ahead, counsel, sorry.

MR. JAMES: Thank you.

A. So --

Q. Let me clarify.

Suppose you have a 3 NAND memory
array where dummy holes and active memory
holes have both been etched. Then the
active memory holes have already been
filled with the memory cell structures,
yet the dummy holes remain open. That's
the context for my question.

A. Okay.

Q. So let me ask it again.

Would it have been a suitable
option to form dummy channels interspersed
with active memory channels to deposit
etchant for the gate replacement process?

MR. DUNTEMAN: Objection. Hold
on, hold on, Dr. Campbell.

THE WITNESS: Yep.

MR. DUNTEMAN: Objection. Vague.

1 S. CAMPBELL

2 MR. JAMES: I would like you not
3 to interrupt him when he does begin
4 his answer.

5 MR. DUNTEMAN: I was taking a
6 moment to put the objection on the
7 record before he answers.

8 But yes, continue.

9 Q. Mr. Campbell, I'd just advise you
10 to give your -- to pause briefly to give
11 your attorney an opportunity to object
12 prior to answering.

13 So I'll ask -- let me ask the
14 question one more time so the record is
15 clear.

16 A. Fine.

17 Q. Would it have been a suitable
18 option to form dummy channels interspersed
19 with active memory channels to deposit
20 etchant for the gate replacement process?

21 A. One has to consider in
22 designing -- I'm sorry, I'm not supposed
23 to use gestures -- in coming up with a
24 process flow to do the sacrificial layer,
25 the replacement, one would like to have

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2 structures with a hole, a cavity, that
3 allows the acid to attack the silicon
4 nitride.

5 If the dummy structures are not
6 filled, they do have a hole in the middle.
7 But typically, dummy structures are fairly
8 narrow and sometimes even tapered as they
9 go to the bottom.

10 So if the size of the dummy is
11 large enough to be able to provide the
12 movement of the acid to the sacrificial
13 layers on all the levels and that isn't
14 too large for taking up room in the memory
15 array, then yes, that can be done.

16 Q. And would you agree that it's
17 critical that the etchant be distributed
18 throughout the entire array so that the
19 sacrificial layers are completely removed?

20 MR. DUNTEMAN: Objection. Form.

21 A. What matters is that the
22 sacrificial layer between the contacts,
23 that is to say the staircase, the gate
24 contacts, and all of the channels that
25 those gates are designed for, that region,

1 S. CAMPBELL

2 the contacts, the gate and everything
3 between the two of them, has to be removed
4 so that the metal can be put in.

5 If there are other spaces that
6 don't act as a gate or some kind of an
7 electrical connection, then you wouldn't
8 have to.

9 Q. But the sacrificial layers
10 themselves need to be completely removed,
11 correct?

12 A. The sacrificial layers have to be
13 removed in the area where you're going to
14 put the gate electrode.

15 Q. And it would be bad, it would be
16 a bad thing that would result in a
17 non-functional device if those layers
18 weren't removed where you were going to
19 place the conductive electrodes, correct?

20 MR. DUNTEMAN: Objection. Vague.

21 A. Yes, yes.

22 Q. And to achieve that, you need to
23 make sure the etchant can reach all areas
24 of the sacrificial layers, correct?

25 MR. DUNTEMAN: Same objection.

1 S. CAMPBELL

2 A. I'll say yes.

3 Q. Would it have been a suitable
4 option to form dummy channels
5 interspersed -- apologies. I'm going to
6 ask a different question.

7 Would it have been a suitable
8 option to form dummy channels in the
9 contact region of a 3D NAND memory device
10 to prevent collapse during the gate
11 replacement process?

12 MR. DUNTEMAN: Same objection.

13 A. Yes.

14 Q. How about to provide support
15 after the gate replacement process?

16 MR. DUNTEMAN: Same objection.

17 A. Yes, although somewhat less
18 critical, but yes.

19 Q. A POSITA would have understood
20 that dummy channels provide support for a
21 3D NAND memory stack during and after gate
22 replacement, isn't that correct?

23 A. Yes.

24 Q. Would it have been a suitable
25 option to form dummy channels at array

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edge to say avoid formation of active
memory cells with defective bits?

MR. DUNTEMAN: Objection. Vague.

A. Well, let's move to the
declaration, if you don't mind, to answer
this question. Yes?

Q. You can get it from wherever you
want.

A. Sorry?

Q. You're more than welcome to look
at your declaration.

A. So in this topic, Dr. Lee opines
that one normally employs dummy structure
channels at the edge of the array and
cites two references.

The first -- the first referred
to a paper that is -- was not in 3D NAND.
In fact, was well before 3D NAND was
invented roughly 20 years ago, and that
paper did suggest that there are the
potential for the need of supports by the
edge of the array. But 20 years ago,
process technology was dramatically
different.

1 S. CAMPBELL

2 The other reference simply says
3 it may happen, but it doesn't say that it
4 does happen.

5 So I don't see a lot of
6 motivation to put these structures on the
7 edge of the array.

8 Q. Do you know what edge array
9 effects are?

10 A. What array effects are?

11 MR. DUNTEMAN: Objection. Vague.

12 Q. Array edge effects, do you know
13 what that means?

14 A. Well, there's etch effects.

15 Q. Edge effects.

16 A. Edge effects.

17 Q. And here I'm asking for your
18 personal understanding.

19 A. I will have to pass on that. No,
20 I do not. That's a term that's not
21 familiar to me.

22 Q. You've previously testified that
23 all millions or billions of transistors in
24 a 3D NAND memory device need to work, is
25 that correct?

1 S. CAMPBELL

2 A. Yes, of course.

3 Q. And you just testified that you
4 don't know what edge array effects are, is
5 that correct?

6 A. I'm not familiar with the term.

7 MR. JAMES: We haven't been going
8 for very long, but I could use five
9 minutes if we could go off the record.

10 (Recess taken from 10:32 a.m. to
11 10:39 a.m. CT)

12 MR. JAMES: I'm going to place
13 Exhibit 1001 in the chat. It's the
14 '322 Patent.

15 BY MR. JAMES:

16 Q. Let me know when you have it
17 open.

18 A. I have it open. Where do you
19 want to go?

20 Q. I'd actually like to start with
21 your declaration, and that's Exhibit 2021,
22 correct?

23 A. 2021.

24 Q. Will you turn to paragraph 155 of
25 your declaration?

1 S. CAMPBELL

2 A. Yes.

3 Q. There you testified that because
4 Nishikawa's TAC and peripheral contacts
5 form in spaces etched through different
6 materials, a POSITA would not have used a
7 common process, including etching forming
8 the openings at the same time as
9 petitioner argues, nor would a POSITA have
10 used the same etch chemistries as
11 petitioner asserts.

12 Do you see that?

13 A. Give me a moment to read through
14 it. Okay.

15 Q. Did I accurately recite --

16 A. I'm sorry, now that I've read it
17 carefully, I'd like the question.

18 Q. The question was, did I
19 accurately recite what you testified to in
20 your declaration?

21 A. Yes.

22 Q. Do you disagree that the '322
23 Patent discloses etching TACS and
24 peripheral contacts at the same time?

25 And if it helps, you can look at

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S. CAMPBELL

column 12, lines 28 to 49.

A. I have 12. What lines?

Q. 28 to 49.

A. Thank you.

All right. I've read that paragraph and, again, what is the question?

Q. Do you disagree that the '322 Patent discloses etching TACs and peripheral contacts at the same time?

A. I agree that it does say that one can etch both at the same time.

Q. Do you disagree that the '322 Patent does not disclose using different etch chemistries to form the TACs and the peripheral contacts at the same time?

A. If they're being etched at the same time, they would have to be etched with the same chemistry.

Q. In fact, column 12, lines 28 to 49, say that the same wet etch process is used, right?

A. I believe it says wet and/or dry etching.

1 S. CAMPBELL

2 Q. In either case, it would be the
3 same etch, correct?

4 A. Yes, that's correct.

5 Q. Do you disagree that using the
6 same etch to form peripheral and
7 through-array contacts was known to a
8 POSITA?

9 MR. DUNTEMAN: Objection. Form.

10 A. I really can't say if that's
11 known or not.

12 Q. The '322 Patent doesn't disclose
13 or propose any previously unknown etch
14 chemistries for simultaneously etching
15 peripheral and through-array contacts,
16 correct?

17 A. Yes, that's correct.

18 Q. If I say something is an
19 apparatus claim, would you understand what
20 I mean?

21 A. An apparatus plan?

22 Q. Apparatus claim.

23 A. I'm sorry, it's not coming
24 through.

25 Q. Oh.

1 S. CAMPBELL

2 A. Apparatus?

3 Q. You understand what a patent is,
4 right?

5 A. Yes, I understand patent.

6 Q. And you understand claims are at
7 the end of the patent?

8 A. Yes.

9 Q. And you understand that claims
10 define what the invention is?

11 A. Yes.

12 Q. So if I use the term "apparatus
13 claim," do you know what I mean?

14 A. Again, outside of my area. It's
15 more of a legal term, not an engineering
16 term.

17 Q. So you don't know what an
18 apparatus claim is?

19 A. I do not know what an apparatus
20 claim is.

21 Q. Do you know what an independent
22 claim is?

23 A. From the term, I assume that it's
24 independent of other claims.

25 Q. In general, do you understand the

1 S. CAMPBELL

2 difference between an apparatus and a
3 process?

4 A. Yes, certainly.

5 Q. And if a claim stated that it's a
6 device, would you consider it an
7 apparatus?

8 A. Again, you're asking me legal
9 questions. It seems reasonable, but I'm
10 not a lawyer. I don't know.

11 Q. Will you take a minute to browse
12 the claims at the end of the '322 Patent.

13 A. Okay.

14 Q. And let me know if you need me to
15 direct you there.

16 A. No, I know where they are.
17 Do you want me to read all 20,
18 just the ones that are still in dispute,
19 or what?

20 Q. One moment.
21 We just need to look at the first
22 line of Claim 1 which says: A
23 3-dimensional 3D memory device.

24 Do you see that?

25 A. Yes.

1 S. CAMPBELL

2 Q. I'll stipulate that that is an
3 apparatus under the law.

4 A. Okay.

5 Q. Do you see -- turn to Claim 8.
6 It also says a 3-dimensional 3D memory
7 device.

8 Do you see that?

9 A. Yes.

10 Q. And again, I'll stipulate that
11 under the law that makes Claim 8 directed
12 to an apparatus.

13 A. Okay.

14 Q. Do you see Claim 14? The first
15 line there says: A 3-dimensional memory
16 device.

17 A. Yes.

18 Q. And again, I'll stipulate that
19 that's an apparatus under the law.

20 MR. DUNTEMAN: I'm going to
21 object to all of these stipulations as
22 forming legal conclusions.

23 A. All right.

24 Q. Do these claims describe
25 processes or do they describe structures?

1 S. CAMPBELL

2 A. These are structures.

3 Q. I'm sorry, your testimony is it
4 describes structures, correct?

5 A. That's correct.

6 Q. So all of the claim structures in
7 the '322 Patent relate to 3D NAND memory
8 design. Do you agree?

9 A. If you wish, I can go through all
10 of them. Without reading them again, I
11 can't say. If you'd like me to take the
12 time to do that, I'd be happy to do that.

13 Q. Take your time.

14 A. All right. So the question again
15 is?

16 Q. So all of the claim structures in
17 the '322 Patent relate to 3D NAND memory
18 design. Do you agree?

19 A. All right. Let me finish my
20 reading.

21 All right. I can confirm that
22 all 20 claims refer to 3D structures.

23 Q. So all of the claim structures in
24 the 3D -- so all of the claim structures
25 in the '322 Patent relate to 3D NAND

1 S. CAMPBELL

2 memory design, correct?

3 MR. DUNTEMAN: Objection. Vague.

4 A. This comes back to the question
5 of the word "design." They're all related
6 to 3D structure. And if you mean by
7 design structure of these elements, then
8 the answer is yes. But again, the claims
9 are structures, as you point out.

10 MR. JAMES: I'm placing Exhibit
11 1046 into the chat, Nishikawa 123.

12 A. You have put it in the chat?

13 Q. I needed to click another button.
14 Apologies.

15 A. Okay. It came now.

16 All right. I have Nishikawa 123.

17 Q. Earlier you testified that a
18 POSITA would know how to avoid short
19 circuits, correct?

20 A. I believe I said a POSITA would
21 know what a short circuit is and finding a
22 solution to the short circuit is more
23 difficult. It depends on the situation.

24 Q. So your testimony is that a
25 POSITA would not necessarily know how to

1 S. CAMPBELL

2 avoid short circuits?

3 A. A POSITA would first have to find
4 out where the short circuit is occurring,
5 what's causing the short circuit, and then
6 develop a plan to change the process to
7 avoid those short circuits.

8 Q. But given a specific structure, a
9 POSITA would know how to avoid short
10 circuits, correct?

11 A. No, it's not correct, because
12 there could be multiple reasons for a
13 short circuit.

14 Q. Would a POSITA ever intentionally
15 modify a structure to have a short
16 circuit?

17 A. In our earlier discussion, you
18 said that a short circuit was an undesired
19 low resistance pathway. And if we're
20 still sticking with that admission, if a
21 short circuit is unintentional, then I
22 don't see how a POSITA would -- I'm not
23 sure how a POSITA would put that, that
24 would create such a structure.

25 Q. But if a POSITA had a structure

1 S. CAMPBELL

2 that did not have a short circuit, they
3 would never intentionally modify it to
4 have a short circuit, correct?

5 A. If we stay with the statement
6 that all short circuits are unintentional,
7 then yes, a POSITA would not intentionally
8 create a short circuit.

9 Well, let me even modify it --
10 oh, no, okay, it's fine.

11 Q. Let's turn to paragraph 56 of
12 your declaration.

13 A. All right. I'm at 56.

14 Q. I need one moment.

15 A. Okay. I am familiar with the
16 paragraph. What's the question?

17 Q. The modification -- do you see
18 the modification you made to Nishikawa's
19 Figure 16, which is Exhibit 1005?

20 A. Yes, I see it.

21 Q. Let me just place that in the
22 chat for the court reporter. You don't
23 need to open it.

24 Here you intentionally -- excuse
25 me, one second.

1 S. CAMPBELL

2 Here you intentionally create an
3 embodiment where the regions 410 and 420
4 would short circuit. Did you not?

5 A. I create a structure that
6 complied with the reasonably round
7 geometry, which is stipulated, changing
8 the -- let me finish, please -- changing
9 the back side contact vertical structure
10 into a round structure, and that was my
11 understanding of what was -- what was
12 called for.

13 Yes, it would intentionally
14 create a short circuit. I mean not to say
15 that exactly -- let me rephrase that.

16 It did create a short circuit.
17 We're aware of that. And that's why we're
18 saying you wouldn't do this. You would
19 not take the trenches that are on
20 Nishikawa and make them round.

21 Q. Where did you -- where did you
22 derive the motivation to place the
23 circular back side contact there as
24 opposed to at the ends of the separated
25 dielectrics 45?

1 S. CAMPBELL

2 A. It doesn't really matter where
3 you put that round structure. There's
4 always going to be a short circuit path.

5 Q. You realize your declaration
6 later contradicts that, correct?

7 A. No, I don't know that.

8 MR. DUNTEMAN: Objection.
9 Argumentative.

10 Q. We'll get there.

11 A. Could you cite what --

12 Q. Would a POSITA looking at
13 Nishikawa 123, which is Exhibit 1040, ever
14 modify Nishikawa Exhibit 1005 such that it
15 short circuits as you've shown in
16 paragraph 56?

17 A. Okay. I need to go back to 123.
18 And tell me where in 123 you want to
19 discuss.

20 Q. That wasn't my question.

21 A. Oh, sorry.

22 Q. Would a POSITA looking at
23 Nishikawa 123 ever modify Nishikawa such
24 that it short circuits as you've shown in
25 paragraph 56? I'm asking about a POSITA's

1 S. CAMPBELL

2 knowledge.

3 A. A POSITA would not do this, which
4 is the -- which is -- what we're trying
5 to -- what I'm trying to present, this is
6 essentially round structure.

7 If you were to convert this
8 trench in Nishikawa, it cannot provide the
9 isolation between 420 and 410.

10 Q. Okay. Let's turn to paragraph 60
11 of your declaration.

12 Here, with the placement of the
13 TAC at the end of the separated
14 dielectric, you don't argue that this
15 would be inoperable or that it would short
16 circuit, do you?

17 A. No, I don't.

18 Q. You merely argue that it would
19 not have been obvious to do that, is that
20 correct?

21 A. In this passage, I was trying to
22 show that if the trench structure, the
23 back side contact vertical structure, if
24 you're going to call that a TAC, and it
25 presumably can be, but if you change it

1 S. CAMPBELL

2 into a round structure, there is no place
3 on the array that you could place that
4 structure and still have isolation between
5 410 and 420.

6 This is just another example of
7 where it could be placed, and you'd still
8 have short circuits.

9 Q. That's not what you said. You
10 said that --

11 MR. DUNTEMAN: Objection.
12 Argumentative.

13 Q. -- it would cure the isolation
14 deficiencies, isn't that right?

15 A. Sorry, say it again?

16 Q. In paragraph 60, you said that it
17 would cure the isolation deficiencies,
18 isn't that right?

19 A. It says if a circular -- even if
20 a circular TAC was physically connected to
21 the end of the separator dielectric
22 structure 45, to cure isolation
23 deficiencies -- I will say that perhaps
24 that could have been worded better. It
25 probably should say in an attempt to cure

1 S. CAMPBELL

2 isolation deficiencies.

3 Q. So you're testifying that your
4 declaration is inaccurate?

5 A. I'm saying it could have been,
6 expressed a little better.

7 Q. Your declaration does not say
8 that this -- the embodiment of paragraph
9 60 short circuits, does it?

10 A. I tend to disagree with you.
11 Given what was --

12 Q. Apologies.

13 A. -- in paragraph 59 and the
14 wording here, an average person would
15 recognize that this was, again, a failure
16 to provide isolation.

17 I think it's strangling language
18 in order to come out with the idea that we
19 think that would actually provide
20 isolation.

21 Q. To the contrary, your declaration
22 says that, for example, the TAC's diameter
23 would have to be large enough to contact
24 the side of the device to maintain
25 isolation, which will require a larger

1 S. CAMPBELL

2 footprint.

3 A. Yep.

4 Q. So you're saying that a TAC
5 position there could provide isolation?

6 A. So if the -- go back to what it
7 says. The TAC's diameter would have to be
8 large enough to contact the side of the
9 device to maintain isolation. That is
10 absolutely true. And that would require a
11 larger footprint than a regular tranche.
12 Also true.

13 If you're confused about the red
14 circle, I can't help you there. But the
15 words in that sentence are absolutely
16 correct.

17 Q. How do you know where the edge of
18 the device is?

19 A. Well, in the sentence it says:
20 The TAC diameter would have to be large
21 enough to contact the side of the device,
22 so --

23 Q. I apologize. Please proceed.

24 A. Go ahead.

25 Q. In Nishikawa, how do you know

1 S. CAMPBELL

2 where the edge of the device is?

3 A. In Nishikawa, that's typically
4 the TAC side contact structure.

5 Q. Yeah, but how do you know where
6 the edge of the device is?

7 A. In Nishikawa, the separation
8 between 410 and 420 is a combination of
9 the separator dielectric structure and the
10 back side vertical structure.

11 So without the -- if the trench
12 were to turn into a circle and there's no
13 trench involved -- yes, that's a good
14 question, how would we determine the edge
15 of the device...

16 So it's a difficult question to
17 answer because we have ignored the trench
18 and we don't really say what would be in
19 its place.

20 So I can't answer that particular
21 question without knowing the -- more about
22 the structure with the trenches removed.
23 But you would have to hit to the edge of
24 the device in order to block shorting 410
25 and 420.

1 S. CAMPBELL

2 Q. You just testified that possibly
3 the trench -- the trench defines the side
4 of the device. Why would that circle need
5 to be any wider than the trench to provide
6 isolation if the trench is the edge?

7 MR. DUNTEMAN: Objection. Form.

8 A. If the trench is the edge, that
9 would suggest that there is a trench below
10 the circle. If that's the case, the
11 short -- excuse me -- the short circuit
12 would be prevented, but you are using a
13 lot more space for the structure --

14 Q. Why -- sorry.

15 A. -- and that's not necessary. You
16 have a very good isolation structure in
17 45. Modifying it this way is -- any
18 POSITA would know that that's not
19 desirable.

20 Q. But if the trench is the edge,
21 you can't make a circle that extends past
22 the end of the edge, correct?

23 A. So a circle could, in principal,
24 come in contact with the trench. It would
25 be a poor design in that the rectangular

1 S. CAMPBELL

2 trench coming in contact with a circle has
3 only a point where they aren't joined.

4 So, in principal, in an ideal
5 world, it could provide isolation. But in
6 a real world, you're likely to see leakage
7 and you're likely to see lower yield.

8 Q. If the trench were removed -- if
9 a circular TAC were employed instead of
10 the trench-shaped TAC, there would no
11 longer be a trench.

12 A. That's correct.

13 Q. And you testified that possibly
14 the trench defines the edge. So -- and
15 clearly both the trench-shaped TAC and the
16 circular TAC would extend all the way down
17 to the substrate, correct?

18 MR. DUNTEMAN: Objection. Vague.

19 A. Can I hear that again?

20 MR. JAMES: Court reporter, can
21 you read that back?

22 THE COURT REPORTER: Sure.

23 (The requested portion was read
24 back by the Court Reporter.)

25 A. Yes.

1 S. CAMPBELL

2 Q. So why would the circular TAC
3 need to be wider, have a diameter longer
4 than the width of the trench?

5 A. Excuse me. The issue here is not
6 the question you just asked me.

7 If we have both the trench and a
8 circular TAC, that's not what -- that is
9 not part of this discussion. This is not
10 an option that Micron came up with.

11 MR. JAMES: Move to strike that
12 answer as nonresponsive. Apologies.

13 A. -- going to modify the -- I'm
14 sorry, have I been struck?

15 MR. DUNTEMAN: No. Answer,
16 unless you're done, Dr. Campbell.

17 Q. Yes, please.

18 A. All right.

19 My understanding on this, and
20 again, I'm not a lawyer, is that the
21 response from Micron was to modify the
22 shape of the trench, not add another shape
23 to the trench.

24 So if you have this round circle,
25 this TAC, you can't have a trench. You've

1 S. CAMPBELL

2 used up the -- you can make more circles,
3 but you can't make the trench anymore --
4 it's -- you're not adding another
5 structure.

6 MR. JAMES: Move to strike the
7 entire response as nonresponsive.

8 Court reporter, can you read back
9 my original question again?

10 (The requested portion was read
11 back by the Court Reporter.)

12 BY MR. JAMES:

13 Q. I'll ask a different question.

14 In the proposed modification, the
15 trench is removed, the trench is no longer
16 there, there's not a trench, correct?

17 A. Correct.

18 Q. So, but, you testified that
19 possibly the trench defined where the edge
20 of the array is, correct?

21 A. Yes.

22 Q. And the edge of the array doesn't
23 change whether or not there's a trench
24 there, correct?

25 A. Okay, yes.

1 S. CAMPBELL

2 Q. And a circular TAC would run
3 through the entire 3D NAND memory stack
4 all the way to the substrate, correct?

5 A. Yes.

6 Q. So why would the circular TAC
7 need to be any wider than the trench was
8 or have a diameter larger than the width
9 of the trench-shaped TAC?

10 A. I don't have an answer to that.

11 Q. You're obligated to provide an
12 answer.

13 MR. DUNTEMAN: Objection. Asked
14 and answered.

15 A. If the trench is removed, there
16 still needs to be some kind of a structure
17 to terminate at least a block of memory
18 channels.

19 That structure is not shown and I
20 don't know what it would be or exactly
21 where it would be. The red hole would
22 have to reach to that particular
23 structure.

24 Since I don't know what the
25 structure is and I don't know where it is,

1 S. CAMPBELL

2 I can't say what the size of that red
3 circle would have to be?

4 Q. So you can't conclude that
5 placing a circular TAC, as you have in
6 your annotated version of Figure 16,
7 increases the array footprint, can you?

8 MR. DUNTEMAN: Objection.
9 Argumentative.

10 A. It all depends. There's more --
11 there isn't enough information to make
12 that statement.

13 Q. Thank you.

14 THE WITNESS: It's 11:30. Can we
15 do a lunch break?

16 MR. DUNTEMAN: Yeah, let's do
17 that.

18 MR. JAMES: Yes, absolutely.

19 (Recess taken from 11:30 a.m. to
20 12:16 p.m. CT)

21 BY MR. JAMES:

22 Q. All right. Mr. Campbell, let's
23 turn to paragraph 66 of your declaration.

24 A. Okay. Let me read it. Okay.

25 Q. Dr. Campbell, did you speak with

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anyone while we were on break?

A. My wife. Nobody else.

Q. Did you talk about the case?

A. No. We talked about our kids.

Q. What a beautiful conversation.

Did you review any materials
while we were on break?

A. No.

Q. All right. In paragraph 66 of
your declaration, you testify that
Nishikawa 123's teachings that openings 79
can have any suitable shape, such as
circular, rectangular or elongated trench
shape does not apply in Nishikawa's Figure
17 -- pardon -- Nishikawa 123's Figure 17.

Do you see that?

A. Yes.

Q. Then you provide the reasoning
that Nishikawa's Figure 17 depicts a
specific embodiment adding an optional
first comb-shaped word line 46A and a
second comb-shaped word line 46B, where
each comb-shaped word line is connected
control gate electrodes.

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S. CAMPBELL

Do you see that?

A. Yes, I do.

Q. Then you rely on Nishikawa 123 at
25, 32 to 35 to support this proposition.

Can you turn there? That's
Exhibit 1046.

A. Sorry, we're looking at Nishikawa
123 at 25?

Q. Yes, that is correct. 25, 32 to
35.

A. Okay. Okay, I'm on line 23. And
the lines?

Q. It's column 25, lines 32 to 35.

A. Thank you.

Q. 32 -- yeah, 32 to 35, that's
correct.

A. Yes.

Q. That passage reads: Electrodes
462 and 463 may comprise finger portions
of the same comb-shaped word line 46B,
while electrode 461 may comprise a finger
portion of a different comb-shaped word
line 46A.

Did I read that right?

1 S. CAMPBELL

2 A. Yes, you did.

3 Q. This does not say that 46A and
4 46B are optional, does it?

5 A. It doesn't say that they are
6 optional for this version.

7 Q. You don't cite any other portions
8 of Nishikawa 123 to support your
9 proposition that Nishikawa 123's teaching
10 of a circular TAC does not apply to Figure
11 17, do you?

12 A. I don't see any place where it is
13 found.

14 Q. So other than Nishikawa 123,
15 column 25, 32 to 35, you have no other
16 basis to believe that Nishikawa's -- I'm
17 sorry, I need to start over.

18 So other than Nishikawa 123 at
19 column 25, lines 32 to 35, you have no
20 other reason to believe that Nishikawa's
21 123 teaching a circular TAC does not apply
22 to Figure 17, correct?

23 MR. DUNTEMAN: Objection. Form.

24 A. Yes.

25 Q. All right. Let's walk through

1 S. CAMPBELL

2 Nishikawa -- well, first, did you consider
3 Nishikawa 123 as a whole when you arrived
4 at the conclusion that Nishikawa 123's
5 teaching of a circular TAC does not apply
6 to Figure 17?

7 A. Say it again, please?

8 Q. Did you consider Nishikawa 123 as
9 a whole when you arrived at the conclusion
10 that Nishikawa 123's teaching of a
11 circular TAC does not apply to Figure 17?

12 A. Yes.

13 Q. Okay. Let's walk through
14 Nishikawa 123 then. Let's start at column
15 6, lines 23 to 26. Again, this is
16 Nishikawa 123, Exhibit 1040 -- 1046.

17 A. Rows?

18 Q. We're starting with 6, 23 to 26.

19 A. All right.

20 Q. This section reads: A stack of
21 an alternating plurality of first material
22 layers (which can be insulating layers 32)
23 and second material layers (which can be
24 sacrificial material layers) is formed
25 over the top of the substrate.

1 S. CAMPBELL

2 You understand that this is an
3 intermediate step of creating a 3D NAND
4 memory array?

5 A. Yes.

6 Q. And it's a necessary step?

7 A. Yes.

8 Q. Let's move to column 7, 25 to 30?

9 A. All right.

10 Q. This section reads: The
11 sacrificial material layers 42 may
12 comprise an insulating material, a
13 semiconductor material, or a conductive
14 material. The second material of the
15 sacrificial material layers 42 can be
16 subsequently replaced with electrically
17 conductive electrodes, which can function,
18 for example, as control gate electrodes of
19 a vertical NAND device.

20 Did I read that right?

21 A. Yes, you did.

22 Q. Do you understand that there is
23 an intermediary step of form ago 3D NAND
24 memory array?

25 A. Yes.

1 S. CAMPBELL

2 Q. And it's a necessary step?

3 A. Yes.

4 Q. Let's turn to column 9, 16 to 19.

5 A. Okay.

6 Q. This section reads: Referring to
7 Figures 3A to 3D, separator trenches can
8 be formed through the insulating cap
9 layer, the alternating stack (32 to 34)
10 and optionally through the gate dielectric
11 layer.

12 Do you understand that the
13 separator trenches then extend through the
14 entire 3D NAND memory array from top to
15 bottom?

16 A. Yes.

17 Q. Let's turn to 9, 35 to 49.

18 A. All right.

19 Q. This section reads: Each
20 separator trench can be filled with a
21 dielectric material, which may be the same
22 as, or may be different from, the material
23 of the insulating layers 32. The
24 dielectric material that fills the
25 separator trenches is different from the

1 S. CAMPBELL

2 material the spacer -- different from the
3 material of the spacer materials 42. The
4 dielectric material that fills the
5 separator trenches is herein referred to
6 as a separator insulating material. For
7 example, the separator insulating material
8 can be undoped silicate glass or doped
9 silicate glass. Excess portions of the
10 separator insulating material can be
11 removed from above the top surface of the
12 alternating stack, for example, by
13 chemical mechanical polish (CMP) a recess
14 etch, or a combination thereof. Remaining
15 portions of the deposited separator
16 insulating material constitutes separator
17 insulator structure 47.

18 Did I read that right?

19 A. Yes, you did.

20 Q. So you understand that the
21 separator insulator structure is 47 run
22 through the entire array from top to
23 bottom, is that correct?

24 A. Yes.

25 Q. Let's go to column 9, 53 to 62.

1 S. CAMPBELL

2 A. All right.

3 Q. This section reads: In one
4 embodiment, the separator insulator
5 structures 47 can laterally separate each
6 layer within the alternating stack (32,
7 42) to separate the alternating stack (32,
8 42) into multiple regions, including
9 interdigitated structures in which fingers
10 of each material layer within the
11 alternating stack (32, 34) -- apologies --
12 (32, 42) extend along a first horizontal
13 direction and neighboring fingers are
14 laterally spaced from one another along a
15 second horizontal direction, hd2, that is
16 perpendicular to the first horizontal
17 direction, hd1. The separator insulator
18 structures 47 extend through the
19 alternating stack.

20 Did I read that right?

21 A. Yes.

22 Q. Let's turn to column 20, lines 30
23 to 60.

24 A. Column 20 and the numbers again?

25 Q. 30 to 60.

1 S. CAMPBELL

2 A. Thank you. All right.

3 Q. This section reads: Referring to
4 Figures 11A and 11B, at least one metallic
5 material can be deposited in the plurality
6 of lateral recesses 43, on the --

7 A. Sorry, sorry. Sorry to
8 interrupt, but I'm not following this. I
9 must have made a mistake. We are on
10 column 20?

11 Q. Lines 30 to 60.

12 A. 30 to 60.

13 Q. It should start referring to
14 Figures 11A and B?

15 A. Yes, there we go. All right.

16 Q. Okay. Nishikawa 123 at column
17 20, lines 30 to 60 reads: Referring to
18 Figures 11A and 11B, at least one metallic
19 material can be deposited in a plurality
20 of lateral recesses 43 on the sidewalls of
21 the access openings 59, and over the top
22 surface of the insulating cap layer 70.

23 As used herein, a metallic
24 material refers to an electrically
25 conductive material that includes at least

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2 one metallic element.

3 The metallic material can be
4 deposited by a conformal deposition
5 method, which can be, for example,
6 chemical vapor deposition (CVD), atomic
7 layer deposition (ALD), or electroless
8 plating, electroplating, or a combination
9 thereof.

10 The metallic material can be an
11 elemental metal, an intermetallic alloy of
12 at least two elemental metals, a
13 conductive nitride of at least one
14 elemental metal, a conductive metal
15 semiconductor alloy such as metal
16 silicide, alloys thereof, and combinations
17 or stacks thereof.

18 Non-limiting exemplary metallic
19 materials that can be deposited in the
20 plurality of lateral recesses 43 include
21 tungsten, tungsten nitride, titanium,
22 titanium nitride, tantalum, tantalum
23 nitride, cobalt and ruthenium.

24 In one embodiment, the metallic
25 material can comprise a metal such as

1 S. CAMPBELL

2 tungsten and/or metal nitride.

3 In one embodiment, the metallic
4 material for filling the plurality or
5 lateral recesses 43 can be a combination
6 of a titanium nitride layer and a tungsten
7 fill material.

8 In one embodiment, the metallic
9 material can be deposited by chemical
10 vapor deposition.

11 A plurality of electrically
12 conductive layers 46 can be formed in the
13 plurality of lateral recesses 43.

14 So this explains that conductive
15 layers 46 are the gate electrodes in
16 Nishikawa 123, is that correct?

17 A. That is correct.

18 Q. Let's turn to 22, 34 to 39.

19 A. All right.

20 Q. This reads -- let me know when
21 you're there.

22 A. I'm there.

23 Q. This section reads: Referring to
24 Figures 14A to 14B, source electrode (or a
25 source local interconnect) openings 79 can

1 S. CAMPBELL

2 be formed through the optional contact
3 level dielectric layer 80, the insulating
4 cap layer 70, the alternating stack (32,
5 42), and the gate dielectric layer 12.

6 The openings can have any
7 suitable shape such as circular,
8 rectangular, or elongated trench shape.

9 So this paragraph indicates that
10 the opening 79 will be formed through the
11 entire stack, is that correct?

12 A. I'd have to go to Figures 14A and
13 B to look at them.

14 Q. Please do.

15 A. Okay. I'm sorry, remind me what
16 the figure number is?

17 Q. You said you needed to look at
18 Figures 14A to B.

19 A. Yes, that's right.

20 Q. And you understand that the
21 optional contact level dielectric layer 80
22 and the insulating cap layer 70 cover the
23 top most conductive layer 46, correct?

24 A. Yes. 70 doesn't completely cover
25 46, but yes, it covers part of 46.

1 S. CAMPBELL

2 Q. How about the optional contact
3 level dielectric layer 80?

4 A. That covers everything.

5 Q. Let's turn to 24, 65 to 67.

6 A. All right.

7 Q. This section reads: Figure 17 is
8 a see-through top-down view in which
9 dielectric material layers overlying a
10 topmost electrically conductive layer 46
11 have been omitted for clarity.

12 Do you see that?

13 A. Yes, I see that.

14 Q. And that's the -- those are the
15 same, those are same conductive layers
16 that we formed in the left arm recesses
17 43, is that correct?

18 A. Yes.

19 Q. And you already testified that
20 the separator dielectric 47 separates the
21 entire stack, is that correct?

22 A. One minute. Yes, that's correct.

23 Q. So what Figure 17 is showing you
24 is the division of the conductive layer 46
25 into two separate halves, 46A and 46B,

1 S. CAMPBELL

2 correct?

3 A. Yes, that's correct.

4 Q. So let's turn to 25, 36 to 40.

5 A. All right.

6 Q. This passage reads: Each
7 electrically conductive layer 46 (i.e.,
8 each of the word-line-level electrically
9 conductive layers 46) formed within the
10 alternating stack includes two physically
11 disjointed portions (46A, 46B) between
12 optional neighboring pairs of back side
13 trenches.

14 These are the same conductive
15 layers 46 referred to in the previous
16 passage, correct?

17 A. Yes, that's correct.

18 Before we proceed, I would like
19 to take a look at this figure again to
20 make sure that what I'm saying is correct.

21 Can I take a peek back at the
22 figure?

23 Q. Take the time you need, but
24 there's no question pending, so there's
25 no -- there's no testimony you can

1 S. CAMPBELL

2 provide.

3 A. Thank you. Can you remind me of
4 the number of the figure?

5 Q. I actually don't know what you
6 are talking about.

7 A. The last one.

8 Q. Oh, 14. Figure 14.

9 A. Thank you.

10 Q. Yes.

11 A. Oh, yes. All right. Go ahead.

12 Q. The conductive layers of Figure
13 17 are labeled 46A and 46B to indicate
14 that the conductive layers 46 have been
15 operated into a left and right portion,
16 correct?

17 A. Yes, that's my understanding.

18 Q. And Figure 14 labels the
19 conductive layers 46, correct?

20 A. Figure 14?

21 Q. I'll direct to you 14A.

22 A. 14A, thank you.

23 14A is a cross-section. It
24 doesn't show the different signals. I'm
25 kind of confused as to -- to confirm.

1 S. CAMPBELL

2 Q. Because conductive layers in 14A
3 are labeled 46, correct?

4 A. Yes, 46 is the conductive layers.

5 Q. So there's no reason for a POSITA
6 to conclude that Figure 17 is a separate
7 embodiment from Figure 14, correct?

8 A. I can't say that that's true.
9 The fact that two labels are the same
10 doesn't mean the entire picture is not in
11 a different embodiment.

12 Q. Well, do you have any reason to
13 believe that 46, that 46 and Figure --
14 Figures 14 is any different from 46 in
15 Figure 17?

16 A. Only that this wasn't described
17 to be the same embodiment.

18 Q. It also wasn't described not to
19 be the same embodiment, isn't that
20 correct?

21 A. Yes.

22 Q. So sitting here today, do you
23 still believe that Figure 17 is a separate
24 embodiment from Figure 14?

25 A. I have no proof one way or the

1 S. CAMPBELL

2 other. So it certainly could be, but I
3 don't know it.

4 Q. All right. Just give me a
5 moment.

6 The function of the separator 47
7 in Nishikawa 123 is to separate the
8 conductive layers of Nishikawa into two
9 electrically isolated word line regions
10 46A and B, is that correct?

11 MR. DUNTEMAN: Objection. Vague.

12 MR. JAMES: What's vague about
13 that question, counsel?

14 MR. DUNTEMAN: It's unclear which
15 figure column or line you're referring
16 to.

17 MR. JAMES: Okay.

18 Q. Following the teachings of
19 Nishikawa, if the TACs were made to be
20 circular -- strike that question.

21 The purpose of the separator
22 dielectric 47 is to prevent the two word
23 line regions from short circuiting, is
24 that correct?

25 MR. DUNTEMAN: Objection. Same

1 S. CAMPBELL

2 objection.

3 A. Yes.

4 Q. If the TACs in Nishikawa 123 were
5 made to be circular, would a POSITA know
6 how to modify the separator 47 to maintain
7 that function?

8 A. You have to go a little bit
9 further into this question.

10 You said if the trench were to be
11 converted into a round structure -- is
12 that correct so far?

13 Q. I can read my question again.

14 A. All right. Ask it again.

15 Q. If the TACs in Nishikawa 123 were
16 made to be circular, would a POSITA know
17 how to modify the separator structure 47
18 to maintain its isolation function?

19 A. Given what 123 looked like in its
20 current embodiment, I don't think it is
21 obvious that a POSITA would find the
22 geometry that would allow what you're
23 suggesting.

24 Q. I'm talking about the separator
25 47, which is the zigzag structure.

1 S. CAMPBELL

2 A. Yes.

3 Q. Okay. Its function is to isolate
4 the two word line regions 410 and 420,
5 correct?

6 A. That's correct.

7 Q. So if there were no -- if there
8 were no trench between different instances
9 of 47 and Nishikawa 123, a POSITA would
10 know how to modify separator 47 to
11 maintain the separation between the two
12 word lines, correct?

13 A. So what two elements are you
14 putting together?

15 Q. There's two separate word line
16 regions, 410 and 420 in Nishikawa 123,
17 right?

18 A. The one I'm looking at on Figure
19 17 is 46A and 46B, but yes, there are two
20 lines.

21 Q. I'm sorry, 46A and 46B.

22 A. Yes.

23 Q. Those two word line regions need
24 to be electrically isolated from each
25 other, correct?

1 S. CAMPBELL

2 A. Yes, that's correct.

3 Q. And the purpose of separator 47
4 is to laterally divide the array to
5 maintain that separation so they can
6 function separately, correct?

7 A. Yes, that's correct.

8 Q. And a person of ordinary skill in
9 the art would know how to modify 47 if the
10 trench was absent to maintain separation
11 between the two word line regions,
12 correct?

13 A. That's where you leave me at. I
14 don't know that a POSITA would know that
15 or come up with that.

16 Q. Can you think of any ways a
17 POSITA might modify 47 to maintain that
18 isolation in the absence of the trench?

19 A. I wouldn't want to speculate.

20 Q. Actually, this is a hypothetical
21 and experts are required to answer
22 hypothetical questions.

23 MR. DUNTEMAN: Objection.

24 Argumentative. If he said that, he
25 would have to speculate to answer the

1 S. CAMPBELL

2 question, that's different than the
3 hypothetical and question that you're
4 describing. That could be answered
5 without speculation.

6 MR. JAMES: Are you instructing
7 the witness not to answer?

8 MR. DUNTEMAN: No.

9 Q. Then please answer the question.

10 MR. DUNTEMAN: Asked and
11 answered.

12 A. It is not immediately obvious to
13 me how if the trenches go away, how you
14 allow the two voltages to be isolated from
15 each other.

16 Q. But you do agree that the
17 function of 47 is to laterally separate
18 the two word line regions 46A and 46B,
19 correct?

20 A. Yes.

21 Q. Do you disagree that dummy memory
22 stack structures formed in dummy openings
23 are electrically non-functional, but are
24 purposefully used to provide mechanical
25 support, including preventing collapse of

1 S. CAMPBELL

2 materials during manufacturing steps,
3 e.g., back side recess formation, and to
4 continue providing mechanical support
5 after manufacture and during operation?

6 A. Yes.

7 Q. Yes, you disagree?

8 A. I'm sorry, say it again? I must
9 have misheard.

10 Q. Did you disagree with the
11 statement I just made?

12 A. I didn't -- I thought I agreed
13 with it, but please say it one more time
14 just to make sure.

15 Q. If you agreed, you agreed.

16 A. Okay.

17 Q. Do you disagree --

18 MR. DUNTEMAN: Dr. Campbell, go
19 ahead and state your answer actually
20 as you believe it.

21 MR. JAMES: I'm sorry, please
22 limit your commentary to objections to
23 my questions. There's no question
24 pending and you're speaking objections
25 and instructions are improper.

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S. CAMPBELL

MR. DUNTEMAN: Your argumentative responses to the witness asking you questions is improper and asking for clarification of the question.

Q. Do you disagree that providing the opening for the data line contacts next to the vertical memory array can effectuate damage to and/or defects at the edges of the vertical memory array, e.g., commonly referred to as edge array effects, accordingly an array of dummy pillar, e.g., dielectric pillar, is conventionally provided between the vertical memory array and the opening to set the edges of the vertical memory array back farther from the opening to mitigate of aforementioned damage to and/or defects at the edges of the vertical memory array?

A. So this is something that you --

MR. DUNTEMAN: Objection.

Compound.

A. This is obviously something that you are reading. What are you reading it from?

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S. CAMPBELL

Q. Do you disagree?

A. So you won't tell me where you're
reading it from?

Q. I'd like you to answer the
question.

A. I would like you to tell me where
it came from.

Q. That's not how this works.

A. The text that you read may very
well be appropriate for certain
structures, certain embodiments. I do not
believe that it is uniformly true.

Q. So you do not believe that such
structures are conventionally provided?

A. I -- okay, if we break it down
one step at a time -- let's do that, I
think that's a good idea.

The dummy structures do provide
mechanical support.

Q. Will you please answer my
question, Dr. Campbell?

A. Say it again then?

Q. Do you disagree that providing
the opening for the data line contacts

1 S. CAMPBELL

2 next to the vertical memory array can
3 effectuate damage to and/or defects at the
4 edges of the vertical memory array, e.g.,
5 commonly referred to as array edge
6 effects, accordingly an array of dummy
7 pillars, e.g., dielectric pillars, is
8 conventionally provided between the
9 vertical memory array and the opening to
10 set the edges of the vertical memory array
11 back farther from the opening and mitigate
12 the aforementioned damage to and/or
13 defects at the edges of the vertical
14 memory array?

15 MR. DUNTEMAN: Objection.

16 Compound. Vague.

17 A. As I said before, this may be
18 true in certain devices. I don't think
19 it's absolutely universal.

20 Q. In your opinion, would that
21 teaching be applicable to 3D NAND memory
22 devices?

23 A. When it's -- yes, that teaching
24 is relevant for some 3D structures.

25 Q. And again, earlier you testified

1 S. CAMPBELL

2 you have no idea what array edge effects
3 are, is that correct?

4 A. That is what I said.

5 MR. DUNTEMAN: Objection.

6 Mischaracterizes testimony.

7 Q. Do you have any idea what array
8 edge effects are?

9 A. The name would imply defects -- a
10 possibility of defects being formed near
11 the edge of where the array structures
12 terminate.

13 Q. But you have no experience with
14 array edge effects, correct?

15 A. That is correct.

16 Q. Do you disagree that the drawings
17 of Nishikawa are not to scale and that's
18 exhibit --

19 A. Which drawing?

20 Q. -- 1005, line -- column 3, line
21 53?

22 A. Nishikawa? Nishikawa 1? I need
23 to look it up.

24 Q. I gave you the exhibit number.
25 It's Exhibit No. 1005.

1 S. CAMPBELL

2 A. Okay. All right. I'm on
3 Nishikawa. Repeat, please, the column and
4 line?

5 Q. Column 3, line 53.

6 A. All right.

7 Q. And the question is: Do you
8 disagree that the drawings in Nishikawa
9 are not to scale?

10 A. In the text it says that drawings
11 are not drawn to scale. So I believe that
12 they're not drawn to scale.

13 Q. So what basis do you have to
14 conclude that there are not room for
15 additional structures in Nishikawa?

16 MR. DUNTEMAN: Objection.
17 Foundation.

18 A. One of the primary goals in
19 designing a 3D device is to pack as many
20 channels, many bits as you can possibly
21 achieve. That is the most important
22 parameter, the most bits you can produce
23 in a given area with an acceptable yield.

24 Q. But you categorically cannot
25 conclude that --

1 S. CAMPBELL

2 A. Can I finish?

3 Q. Oh, I apologize. Please continue
4 if you have something else?

5 A. The layout, the top view layout
6 that is shown in Nishikawa appears to
7 leave open areas where additional
8 structures could be formed without
9 penalty. That just isn't how these things
10 are designed. They are very tightly
11 packed. It's not just Nishikawa. It's
12 virtually any 3D device.

13 Q. But looking at Nishikawa itself,
14 it expressly teaches that the drawings are
15 not to scale. So you cannot conclude from
16 Nishikawa that there is not room for
17 additional structures, correct?

18 A. No, not correct. Adding
19 additional structures will invariably
20 reduce bit density, and so you have a
21 tradeoff. You have the advantage of these
22 new structures with the reality that they
23 take up. And when you already have good
24 isolation structures, why would you add
25 more?

1 S. CAMPBELL

2 Q. That's not the question.

3 You cannot conclude from the
4 reference that there's no room, correct?

5 A. From the reference, because it is
6 not drawn to scale, I cannot take that
7 figure as being good or bad. If it has
8 lots of empty space or if it doesn't have
9 lot of empty space, I can't make any
10 reference -- I can't make any conclusions
11 because that's what this says. But I know
12 that density is the most important
13 parameter in the device. So it's not
14 coming from the figure. It's coming from
15 what is well-known about 3D devices.

16 Q. Okay. But again, that's not the
17 question.

18 MR. JAMES: Court Reporter,
19 please read back my last question.

20 (The requested portion was read
21 back by the Court Reporter.)

22 MR. DUNTEMAN: Objection. Asked
23 and answered.

24 A. From the figure, I cannot draw a
25 conclusion one way or the other.

1 S. CAMPBELL

2 MR. DUNTEMAN: I think this is a
3 good time for the break, or any break.

4 Dr. Campbell, you want 10
5 minutes?

6 THE WITNESS: That would be
7 great.

8 MR. JAMES: We just took a
9 45-minute break. Actually, this is my
10 deposition, unless the request comes
11 from the witness, I'm --

12 THE WITNESS: Since our lunch
13 break, I prefer to have a 10-minute
14 break.

15 MR. JAMES: Okay. Then we've got
16 it.

17 (Recess taken from 1:15 p.m. to
18 1:27 p.m. CT)

19 BY MR. JAMES:

20 Q. Do you disagree that conductive
21 layers are recessed from interlayer --
22 strike that.

23 Do you disagree that conductive
24 layers are recessed from insulating layers
25 to increase leakage current suppression?

1 S. CAMPBELL

2 A. I believe that insulators
3 adjacent to conductors can mitigate
4 leakage currents.

5 Q. That's not the question.

6 MR. JAMES: Court Reporter, can
7 you read my question back?

8 THE COURT REPORTER: Sure.

9 (The requested portion was read
10 back by the Court Reporter.)

11 MR. DUNTEMAN: Asked and
12 answered. Objection.

13 THE WITNESS: Court Reporter,
14 could I get that one more time?

15 THE COURT REPORTER: Sure.

16 THE WITNESS: Thank you.

17 (The requested portion was read
18 back by the Court Reporter.)

19 A. Does conducting layers mean
20 recessed from the insulator? If that's
21 the question, then -- I apologize, but
22 there's a negative in there and I can't
23 understand what you're asking me.

24 Q. I'm asking you if you disagree
25 with the statement.

1 S. CAMPBELL

2 A. Yes, but the statement is
3 convoluted, difficult to follow.

4 Q. What's convoluted about it?

5 A. May I ask to repeat it, but do it
6 more slowly? Is that acceptable?

7 Could you please read it in a
8 slow manner?

9 (The requested portion was read
10 back by the Court Reporter.)

11 A. Okay. It all depends what the
12 recessing is used for. If you are
13 recessing in order to put in insulator,
14 then that would reduce leakage. But when
15 you say we're going to recess it, is that
16 just going to be in here? I don't know
17 what's going to be in that space. So it
18 depends on exactly what this process is
19 and how you follow it up.

20 Q. I've placed a reference in the
21 chat.

22 A. All right.

23 Q. If you'll open it.

24 MR. DUNTEMAN: Counsel, is this
25 reference an exhibit in IPR?

1 S. CAMPBELL

2 MR. JAMES: No, it's not.

3 MR. DUNTEMAN: Thank you.

4 A. All right. I have it up on my
5 screen. I have never seen it before, so
6 you'll have to walk me through what you
7 want.

8 Q. Just turn to column 7, line 16 to
9 17.

10 A. Maybe I have the wrong one.

11 Q. Page 7.

12 A. Okay, page 7. And what line?

13 Q. Can you read lines 16 and 17?

14 A. Also in the embodiment shown, the
15 first conducting layers 202 are recessed
16 from the etch pits 208 to increase the
17 leakage current suppression.

18 Q. You're welcome to review the
19 figures and my question is whether you
20 disagree with that statement.

21 A. I'm trying to find the figure
22 that goes with this.

23 Q. Take your time.

24 MR. DUNTEMAN: Counsel, is there
25 a question pending?

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S. CAMPBELL

MR. JAMES: Yes.

MR. DUNTEMAN: Court Reporter,
can you repeat, please?

(The requested portion was read
back by the Court Reporter.)

MR. JAMES: One second. That's
not the question pending.

Oh, there was something that's
not transcribed. The last thing I
said after "take your time" is -- or
rather was -- and my question is
whether you disagree with the
statement.

THE COURT REPORTER: Let me read
it again. It was transcribed.

(The requested portion was read
back by the Court Reporter.)

MR. JAMES: Thank you.

MR. DUNTEMAN: Thank you.

A. This is extremely difficult to
do. I don't know what these materials
are. I don't know, they're describing
something called a selector, although it
looks like it's a 3D stack, a

1 S. CAMPBELL

2 significantly different technology than
3 I'm used to -- is it -- or at least the
4 terminology is different.

5 So I really -- throwing something
6 on me like this I've never seen before,
7 the terminology is not -- I can't answer
8 your question.

9 Q. Do you or do you not disagree
10 with the statement?

11 A. I can't answer the question.

12 Q. Do you agree that that's what the
13 reference says?

14 A. Let's go back to --

15 Q. Sorry, let me ask a different
16 question.

17 Do you agree that -- and for the
18 record, the reference placed in the chat
19 is W02019/066829 to Lilak.

20 A. So these are polymer components.
21 This is apples and oranges. You want me
22 to answer what's the polymers, conducting
23 polymer. I don't know.

24 Q. I'll ask the question one more
25 time.

1 S. CAMPBELL

2 Do you disagree that Lilak at
3 page 7, lines 16 to 17, discloses also in
4 the embodiment shown the first conductive
5 layers 202 are recessed from etch pits,
6 from etch pits 208 to increase leakage
7 current suppression?

8 A. That's what it says, yes.

9 Q. And do you believe that recessing
10 conductive layers as such increases
11 leakage current suppression?

12 MR. DUNTEMAN: Objection. Asked
13 and answered.

14 A. Again, you're asking for a
15 universal yes or no, and I can't give that
16 you. It depends on the structure.
17 Depends on the materials.

18 Q. So the answer is you don't know
19 what that recessing conductive layer,
20 conductive layers in an alternating memory
21 stack increases leakage current
22 suppression?

23 MR. DUNTEMAN: Objection.
24 Mischaracterizes testimony.

25 A. So the answer is, I can't answer

1 S. CAMPBELL

2 it. You haven't given me enough
3 information and you refuse to give me the
4 information that I need.

5 Q. You're obligated to answer the
6 question.

7 A. It all depends.

8 MR. JAMES: I'll note that the
9 witness has refused to answer the
10 question.

11 MR. DUNTEMAN: I'll note that
12 he's not refused to answer. He is
13 simply not giving a yes or no that
14 counsel is looking for, despite
15 answering that context as required and
16 that it is not a yes or no answer.

17 Q. Do you disagree that conductive
18 layers can be recessed, proximate
19 contacts, such that material insulating
20 layers is closer to the contacts than the
21 material of the conductor layers, such
22 recesses and conductive layers can be
23 filled with insulative material, such as
24 that of an insulating liner, recesses can
25 be included if additional isolation from

1 S. CAMPBELL

2 contacts is desired. Adjacent contacts
3 can also be electrically insulated or
4 isolated from one another to avoid
5 capacitance in shorting, i.e., electrical
6 leakage?

7 MR. DUNTEMAN: Objection.

8 Q. Electrical isolation can be
9 accomplished, at least in part, by
10 separating adjacent contacts by a
11 distance.

12 Do you disagree with this
13 statement?

14 A. I do not disagree with that
15 statement. That is much better.

16 Q. Thank you. And apologies for any
17 confusion.

18 Do you disagree that dummy
19 channel structures are commonly provided
20 at the edge of memory cell regions
21 adjacent to contact region?

22 MR. DUNTEMAN: Objection. Vague.

23 A. Dummy structures are typically
24 found in the staircase area. No. I'll
25 leave it at that.

1 S. CAMPBELL

2 Q. Do you disagree with the
3 statement I just made or rather the
4 question I asked?

5 MR. DUNTEMAN: Objection. Asked
6 and answered.

7 A. Okay.

8 THE WITNESS: Can the reporter
9 please repeat it?

10 (The requested portion was read
11 back by the Court Reporter.)

12 A. I would disagree with that
13 statement as, in general, I see dummy
14 structures in the staircase area, not
15 adjacent.

16 Q. Okay.

17 MR. JAMES: Okay. I'm done.

18 THE WITNESS: Okay.

19 MR. DUNTEMAN: Okay. Let's take
20 about a 20-minute break, give or take,
21 for me to look back at this and we'll
22 reconvene then.

23 MR. JAMES: Okay.

24 (Recess taken from 1:47 p.m. to
25 2:19 p.m. CT)

1 S. CAMPBELL

2 EXAMINATION BY

3 MR. DUNTEMAN:

4 Q. Dr. Campbell, I have a couple of
5 questions for you.

6 A. Sure.

7 Q. Do you recall counsel asking you
8 whether it wouldn't have been suitable, a
9 suitable option to form a circular TAC in
10 a 3D NAND memory stack, and you responded
11 yes?

12 A. Yes, I recall that.

13 Q. Is a circular TAC a suitable
14 option in any 3D NAND device?

15 A. Yes. I'll just say yes, period.

16 Q. What about Nishikawa 123?

17 A. Nishikawa 123 --

18 Q. Sorry, I meant -- I withdraw the
19 question.

20 What about Nishikawa?

21 A. Nishikawa, because of the
22 multiple gate structures on each level,
23 makes the circular TAC very difficult.

24 Q. Could you have a circular TAC in
25 Nishikawa's Figure 16 as modified by

1 S. CAMPBELL

2 petitioner?

3 A. Nishikawa 16, I have to look it
4 up. One second.

5 MR. JAMES: Objection. Vague.
6 Objection. Form.

7 A. All right. 16? And you want to
8 know if a TAC could go through there?

9 Q. No, no. Is it your opinion you
10 could have a circular TAC as modified by
11 petitioner in Figure 16 of Nishikawa?

12 MR. JAMES: Objection. Misstates
13 evidence of record. Petitioner never
14 advanced such a combination.

15 Q. You can answer the question.

16 A. If the circular TAC is, in fact,
17 a reconstruction of the trench structure,
18 no, the circuit cannot work as designed.

19 Q. Sorry, I didn't mean to cut you
20 off. Is Nishikawa, Figure 16, a 3D NAND
21 device?

22 A. Yes, it's a 3D NAND device.

23 MR. JAMES: Objection to the last
24 question as leading.

25 Q. Do you recall counsel asking you

1 S. CAMPBELL

2 about modifying Nishikawa 123's
3 trench-shaped back side trench structure?

4 A. Yes.

5 Q. Do you recall -- withdraw that
6 for a moment.

7 Let's take a look at paragraph
8 60.

9 A. In Nishikawa?

10 Q. I'm sorry, in your declaration.

11 A. Declaration, okay.

12 Q. Okay. You recall counsel asking
13 you about the modification shown in Figure
14 16 as modified in paragraph 60 to your
15 declaration?

16 A. Yes, I recall that.

17 Q. You recall testifying that the
18 red circle as drawn in your declaration
19 here in paragraph 60 would need to
20 terminate in the device?

21 A. Yes.

22 MR. JAMES: Objection. Misstates
23 prior testimony.

24 Q. Sorry, what was your answer,
25 Dr. Campbell?

1 S. CAMPBELL

2 A. Yes.

3 Q. Where would the red circle as a
4 TAC need to terminate?

5 MR. JAMES: Objection. Vague.

6 A. In order for it to be a TAC, it
7 has to be in the array and on the other
8 end all the way down to the substrate.

9 Q. What do you mean when you say in
10 paragraph 60 the TAC's diameter would need
11 to be large enough to contact the side of
12 the device to maintain the isolation?

13 A. It means that we'd have to -- in
14 order for the device to work as expected,
15 410 and 420 have to be electrically
16 isolated.

17 Q. How would it maintain that
18 isolation?

19 A. Well, normally it maintains the
20 isolation with the trenches that are at
21 the point where the 45 structure is
22 terminated. The larger red circle is not
23 going to completely block the current --
24 sorry -- yeah, the current between 420 and
25 410 unless there is some other structure

1 S. CAMPBELL

2 in addition to the circle.

3 Q. What would that be, as an
4 example?

5 MR. JAMES: Objection. Vague.

6 A. Well, if you could put a trench
7 back in, that might do it and you have, of
8 course, to terminate the other side, the
9 upper side as well.

10 Q. Can you describe what you mean by
11 "upper side," just generally looking at
12 the figure in paragraph 60 that you've
13 modified?

14 A. At the figure, the certain
15 structure 45 terminates on the edge of the
16 figure and at the bottom edge of the
17 figure. So one would need to terminate
18 both of those in some manner.

19 Q. So focusing just on the bottom
20 red circle for a moment, does the TAC in
21 that modification terminate only on the
22 bottom side?

23 MR. JAMES: Objection. Vague.

24 A. Yes. Presuming that that red
25 circle is a TAC, that could terminate the

1 S. CAMPBELL

2 bottom of the 45 structure.

3 Q. Does it terminate on the side,
4 too?

5 A. No.

6 MR. JAMES: Objection. Vague.

7 A. This comes back to the
8 discussion --

9 MR. JAMES: Excuse me. Excuse
10 me. Objection. Leading.

11 THE WITNESS: Sorry.

12 MR. JAMES: Thank you.

13 A. This comes back to a discussion I
14 had previously that we don't know what
15 would be on the top and bottom structures.
16 As it is, it's not terminated.

17 Q. When you say "top," do you mean
18 coming out of the page or to the right or
19 left or the very top of the figure?

20 A. At the very top of the figure and
21 the bottom of the figure -- yeah,
22 they're -- the figure as it's shown, it's
23 not clear to me where 410 terminate and
24 420 terminate. We see a dash line at the
25 bottom and a dash line at the top. I

1 S. CAMPBELL

2 believe those are where the TAC -- sorry,
3 the trenches were.

4 So if that dash line means that
5 that's the end of 410 and 420, well, that
6 would be different. But that's not
7 what -- I mean, it doesn't say that. I
8 don't know how it's ending, how it's
9 terminating on the top and on the bottom
10 of the picture.

11 Q. Do you recall counsel asking you
12 about Nishikawa 123, Figure 17, and how
13 you formed the basis of your opinion that
14 Nishikawa 123's teaching of a circular TAC
15 does not apply to Figure 17?

16 A. Yes. We don't have a TAC in this
17 structure -- well, unless you, again,
18 assume that the trenches are TACs.

19 Q. Dr. Campbell, I'm going to ask
20 you to look at paragraphs 97 and 98 of
21 your declaration.

22 A. All right. Shall I just read it
23 to myself?

24 Q. Yeah, take a minute if you want
25 to take a look.

1 S. CAMPBELL

2 A. All right. 97 and 98?

3 Q. That's right. I'm sorry, not 98,
4 97.

5 A. 97. Just 97. Okay. I've read
6 it.

7 Q. Do you recall counsel asking you
8 about placing a dummy channel in
9 Nishikawa's memory stack in Figure 16
10 there in paragraph 97?

11 A. Yes.

12 Q. What are the features shown there
13 in Figure 16?

14 A. Excuse me.

15 MR. JAMES: Objection. Vague.

16 A. From the top, we have the trench
17 structure and at the bottom, the second
18 trench structure. Between the two, we
19 have the 45, which is the dielectric
20 separator structure. We have memory
21 strings, which are labeled 55, and we have
22 bit lines labeled 96. Oh, and there's a
23 connection from the bit lines to the top
24 device in the stack.

25 Q. What is that labeled as in the

1 S. CAMPBELL

2 figure?

3 A. 92.

4 Q. And then if you could scroll down
5 and take a look at Figure 1, are there any
6 additional features shown in this cross
7 section in the memory stack?

8 MR. JAMES: Objection. Vague.

9 A. Well, yes. It displays an
10 example of a peripheral device on the far
11 left and it also shows the contact, the
12 gate contacts on 66. So it shows a
13 staircase structure in addition to the
14 channel.

15 Q. Based on your understanding of
16 Nishikawa and looking at these figures,
17 can you just describe the density of this
18 memory stack?

19 MR. JAMES: Objection. Vague.

20 Objection. Foundation.

21 A. Looking at Figure 1, the channels
22 for the memory stack are tightly packed
23 and very little unused space.

24 Q. And based on your experience, do
25 you consider this a high density memory

1 S. CAMPBELL

2 stack?

3 MR. JAMES: Objection. Leading.

4 A. It is a diagram and it's not to
5 scale. The person who lays out this
6 structure will put those channels as close
7 as they possibly can, and of course there
8 will be a lot more channels than what
9 we're seeing.

10 I'll say also the contact region
11 would be more dense.

12 Q. Do you have an opinion whether
13 there is room in Nishikawa's memory stack
14 to add dummy channels -- withdrawn. Let
15 me rephrase.

16 Do you have an opinion whether
17 there's room for a dummy channel in
18 Nishikawa's memory stack?

19 MR. JAMES: Objection. Vague.

20 A. The memory array in Nishikawa
21 is -- act as tightly as it possibly can.
22 If you want to add -- we're talking about
23 TACs or dummies?

24 Q. Talking about dummy channels.

25 A. Dummy channel, okay, I'm sorry.

1 S. CAMPBELL

2 Well, the same thing arises. You
3 have a very tightly packed, a very high
4 aspect ratio of etch processes with
5 contacts. And if you are putting in dummy
6 structures in the contact region, there
7 will be a tradeoff between an area that is
8 being consumed by dummy channels versus
9 the benefit that arise.

10 Q. We'll get there about the
11 tradeoffs, but just more fundamentally, is
12 there room in the -- do you have an
13 opinion whether there's room for a dummy
14 channel in Nishikawa's memory stack?

15 A. Based on this figure, it would be
16 very difficult.

17 Q. Is your opinion based only on the
18 figures?

19 A. No. It's -- it's the need,
20 again, to use the very precious real
21 estate in order to achieve what you need.

22 Q. And what's that, what do you mean
23 by "what you need"?

24 A. What I mean is -- this goes back
25 to the tradeoff -- do you need those dummy

1 S. CAMPBELL
2 channels in order to provide the physical
3 support.

4 And in Nishikawa, certainly
5 Nishikawa 1, Nishikawa 123 as well, you
6 already have the support structure. You
7 don't need these dummy structures.

8 Q. To add a dummy channel, what
9 would a POSITA have to do to the memory
10 stack?

11 MR. JAMES: Objection. Vague as
12 to memory stack. Vague as to do.

13 A. The POSITA would have to develop
14 an etch process suitable for the dummy
15 structure. They'd have to develop the
16 insulating material that is put inside the
17 dummy stack -- dummy stack, sorry, dummy
18 structure -- and then determine the size
19 of the dummy and where they're going to be
20 located and how you're going to interface
21 those structures with the contacts.

22 I'll point out that this is not
23 easy, particularly the etching part.

24 MR. DUNTEMAN: No further
25 questions.

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FURTHER EXAMINATION

BY MR. JAMES:

Q. Can we just go back to paragraph
60 of your report?

A. 60 of the declaration?

Q. Yes. Thank you.

Are we there?

A. Yes. I'm just reading it. All
right.

Q. You drew this figure, correct?

MR. DUNTEMAN: Objection. Do not
answer that. He's calling for
attorney/client work product and
privileged information.

MR. JAMES: Excuse me. I
disagree. This is his declaration.
He has signed this. He has adopted
this. Everything in this is his work
product. He has testified to that.

BY MR. JAMES:

Q. Dr. Campbell --

MR. DUNTEMAN: I'm instructing
him not to answer that question.

MR. JAMES: All right. We'll

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S. CAMPBELL

call the board. Let's do it.

Are you willing to do that?

MR. DUNTEMAN: Give me five
minutes. We'll go off the record.

MR. JAMES: Yep. Bye.

(Recess taken from 2:43 p.m. to
2:52 p.m. CT)

MR. JAMES: Do you withdraw your
objection?

MR. DUNTEMAN: I'll withdraw the
instruction not to answer, but I'll
object insofar as you call for -- the
question calls for any substance of
privileged communications and I'll
remind the witness not to reveal the
substance of any communications.

A. This figure was developed in
discussions with an attorney at Latham &
Watkins. It was drawn by somebody at the
company. I did not draw it. It's a
product of our discussions.

MR. JAMES: He's opened the door,
counsel.

MR. DUNTEMAN: No, he hasn't. He

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S. CAMPBELL

didn't reveal any substance. He
simply answered the question that he
did not draw it.

BY MR. JAMES:

Q. So you did not draw this figure?

A. I did not physically draw it. We
had an outline --

MR. DUNTEMAN: Stop. Stop.

THE WITNESS: Sorry. You're
right. My bad.

A. -- weighed rough outline.

MR. DUNTEMAN: Stop.

MR. JAMES: Now the door's
opened.

MR. DUNTEMAN: No, it's not.

MR. JAMES: But I'm going to stop
out of courtesy.

BY MR. JAMES:

Q. You adopted this figure,
regardless of who drew it, correct?

A. Yes. By adopted, you mean I
agree with what it says? I'm trying to
understand a legal word in my vernacular.
What do you mean by "adopted"?

1 S. CAMPBELL

2 Q. It represents -- do you believe
3 that everything in your declaration is
4 true and accurate?

5 A. To the best of my knowledge,
6 yes.

7 Q. And do you believe that this
8 figure is true and accurate?

9 A. Yes, absolutely.

10 Q. How long was the outline that you
11 were --

12 MR. DUNTEMAN: Objection.
13 Do not answer that question.

14 Q. Who gave you the outline?

15 MR. DUNTEMAN: Counsel, we've
16 established this. Do not answer the
17 question.

18 Q. Do you recall that you frequently
19 testified that memory density is the most
20 important factor when designing a 3D NAND
21 memory array?

22 A. Yes.

23 Q. That's not true, is it?

24 MR. DUNTEMAN: Objection. Asked
25 and answered.

1 S. CAMPBELL

2 A. What's important is how many bits
3 you can provide for so many dollars.

4 That's -- in the end, that's what it comes
5 down to. There are other things that can
6 be useful, access rates and other things,
7 but those are the two biggest.

8 Q. But if you can't fabricate a
9 memory array that doesn't collapse, it
10 doesn't matter how many bits you can stick
11 in it, correct?

12 A. That's why I said -- well, okay,
13 then I should have said functional bits.

14 Q. Yeah, and -- so preventing array
15 collapse is as equally important as memory
16 density, correct?

17 A. Because if it collapsed, then you
18 won't have functional bits. So yes,
19 that's implied with what I said.

20 MR. JAMES: Thank you. Nothing
21 further.

22 MR. DUNTEMAN: Nothing here.

23 THE COURT REPORTER: Do you
24 need the rough again for this one,
25 counsel?

141

1 S. CAMPBELL

2 MR. DUNTEMAN: That would be

3 nice. Thank you.

4 (Time noted: 2:57 p.m. CT)

5
6 _____
7 STEPHEN CAMPBELL

8
9 Subscribed and sworn to before me

10 this ____ day of _____, 2026.

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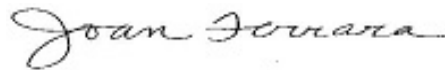
REPORTER CERTIFICATE

I, JOAN FERRARA, do hereby
certify:

That said proceedings were taken
at the time and place herein named;
and that the transcript is a true
record of the testimony as reported by
me, a disinterested person, and was
thereafter transcribed.

I further certify that I am not
interested in the outcome of the said
action, nor connected with, nor
related to any of the parties in said
action, nor to their respective
counsel.

IN WITNESS WHEREOF, I have
hereunto set my hand this 27th day of
January, 2026.

A handwritten signature in cursive script that reads "Joan Ferrara". The signature is written in dark ink and is positioned above a horizontal line.

JOAN FERRARA, RMR, FCRR

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DEPOSITION ERRATA SHEET

Case Caption: Micron Technology

DECLARATION UNDER PENALTY OF PERJURY

I declare under penalty of perjury
that I have read the entire transcript of my
Deposition taken in the captioned matter or
the same has been read to me, and the same
is true and accurate, save and except for
changes and/or corrections, if any, as
indicated by me on the DEPOSITION ERRATA
SHEET hereof, with the understanding that I
offer these changes as if still under oath.

STEPHEN CAMPBELL

Subscribed and sworn to on the ____ day of
_____, 2026, before me,

Notary Public, in and for the State of

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