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- (71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).
- (72) Inventors; and
- (71) Applicants: **LILAK, Aaron D.** [US/US]; 8126 SW Newbury Court, Beaverton, Oregon 97007 (US). **THEOFANIS, Patrick** [US/US]; 300 S Mentor Avenue #5, Pasadena, California 91106 (US). **KENCKE, David L.** [US/US]; 3839 NW 163rd Terrace, Beaverton, OR 97006 (US). **KOTL-**
- YAR, Roza** [US/US]; 1167 SW Chestnut Drive, Portland, Oregon 97219 (US).
- (74) Agent: **SULLIVAN, Stephen G.** et al.; SCHWABE, WILLIAMSON & WYATT, P.C., 1211 SW 5th, Ste 1900, Portland, Oregon 97204 (US).
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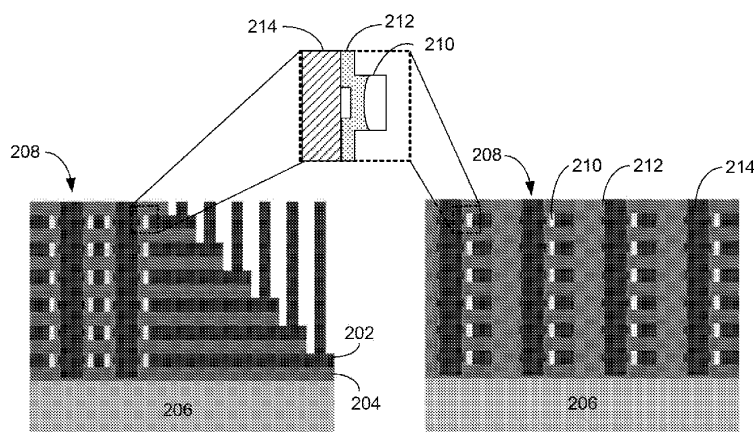


FIG. 2B

FIG. 2C

(57) Abstract: An integrated circuit structure includes a stack of alternating first conductive layers and insulator layers. A plurality of etch pits are through the first conductive layers. A plurality of selectors are in the etch pits adjacent to the first conductive layers. A memory material layer is adjacent to the plurality of selectors in the etch pits, wherein one of the plurality of selectors and the memory material layer is self-aligned and has a hemispherical side facing the corresponding etch pit.

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**DIRECT SELF-ASSEMBLY PROCESS FOR FORMATION OF SELECTOR OR
MEMORY LAYERS ON A VERTICAL RRAM MEMORY FOR LEAKAGE CURRENT
MINIMIZATION**

5 TECHNICAL FIELD

Embodiments of the disclosure are in the field of integrated circuit structures and, in particular, direct self-assembly process for formation of selector or memory layers on a vertical RRAM memory for leakage current.

10 BACKGROUND

For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory devices on a chip, lending to the fabrication of products with increased functionality. The drive for ever-more functionality, however, is not without issue. It has become increasingly significant to rely heavily on innovative fabrication techniques to meet the exceedingly tight tolerance requirements imposed by scaling.

Embedded memory with non-volatile memory devices, e.g., on-chip embedded memory with non-volatility can enable energy and computational efficiency. A non-volatile memory device such as resistive random access memory (RRAM) device or magnetic tunnel junction (MTJ) memory device is coupled with selector element to form a memory cell. A large collection of memory cells forms a key component of non-volatile embedded memory. However, with scaling of memory devices, the technical challenges of assembling a vast number of memory cells presents formidable roadblocks to commercialization of this technology today.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and 1B illustrate a cross-sectional views of a state-of-the-art vertical RRAM.

Figures 2A-2C are diagrams of a vertical memory array fabricated in accordance with the present embodiments.

Figure 3 illustrates a method of fabricating a structure comprising alternating horizontal layers of conductive layers and insulating layers upon which a vertical memory array will be formed.

Figure 4A illustrates an angled three-dimensional view of the vertical memory showing formation of etch pits.

Figure 4B illustrates a cross-sectional views of the vertical memory array of showing the interior of the etch pits after an optional wet etch is applied to the conductive layers to form lateral recesses.

Figure 5 illustrates an embodiment of the vertical memory array after the formation of the etch pits with substantially planer etch pit sidewalls.

Figure 6A-6C illustrate the vertical memory array after the array of etch pits are formed and after the etch pits are filled with a block copolymer comprising first and second polymer components and during a direct self-assembly (DSA) process.

Figure 7A illustrates a phase diagram for PS-b-PMMA demonstrating possible DSA morphologies as a function (f) of polymer component A, a polymer component B, and a Flory-Huggins X_n value.

Figure 7B illustrates example block copolymer depositions within a cross-section of confined etch pits for varying Flory-Huggins X_n values.

Figures 8A and 8B illustrate cross-sectional views the vertical memory array after DSA block copolymer deposition and after the second polymer component is removed from the vertical memory array.

Figures 9A and 9B illustrate the vertical memory array after the memory material layer is formed conformal to the first polymer component and edges of the insulating layers.

Figures 10A and 10B illustrate an angled three-dimensional view and a cross-sectional view the vertical memory array, respectively, after trenches are formed through the conducting layers and the insulating layers.

Figures 11A and 11B illustrate an angled three-dimensional view and a cross-sectional view the vertical memory array, respectively, after the first polymer component is removed from the exposed side of the trenches to create vacated regions.

Figure 12A-12C illustrate the vertical memory array after each of the vacated regions are filled with a selector layer.

Figures 13A-13C illustrate the vertical memory array according to a second embodiment of the disclosure, where the first polymer component of the BCP is replaced with the memory material layer, rather than the selectors, and the memory material layer is formed self-aligned to the first conductive layer.

Figures 14A and 14B are top views of a wafer and dies that include one or more embedded non-volatile memory structures utilizing direct self-assembly process for formation of selector or memory layers.

Figure 15 illustrates a block diagram of an electronic system, in accordance with an embodiment of the present disclosure.

Figure 16 is a cross-sectional side view of an integrated circuit (IC) device assembly that may include one or more embedded non-volatile memory structures utilizing direct self-assembly process for formation of selector or memory layers.

5 Figure 17 illustrates a computing device in accordance with one implementation of the disclosure.

DESCRIPTION OF THE EMBODIMENTS

A direct self-assembly process for formation of selector or memory layers on a vertical RRAM memory for leakage current are described. In the following description, numerous
10 specific details are set forth, such as specific material and tooling regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as single or dual damascene processing, are not described in detail in order to not unnecessarily obscure embodiments of the
15 present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale. In some cases, various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular,
20 these operations need not be performed in the order of presentation.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, “below”, “bottom”, and “top” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, and “side” describe the orientation
25 and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

Embodiments described herein may be directed to front-end-of-line (FEOL)
30 semiconductor processing and structures. FEOL is the first portion of integrated circuit (IC) fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are patterned in the semiconductor substrate or layer. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers. Following the last FEOL operation, the result is typically a wafer with isolated transistors (e.g., without any wires).

35 Embodiments described herein may be directed to back end of line (BEOL)

semiconductor processing and structures. BEOL is the second portion of IC fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are interconnected with wiring on the wafer, e.g., the metallization layer or layers. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections. In the BEOL part of the fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed. For modern IC processes, more than 10 metal layers may be added in the BEOL.

Embodiments described below may be applicable to FEOL processing and structures, BEOL processing and structures, or both FEOL and BEOL processing and structures. In particular, although an exemplary processing scheme may be illustrated using a FEOL processing scenario, such approaches may also be applicable to BEOL processing. Likewise, although an exemplary processing scheme may be illustrated using a BEOL processing scenario, such approaches may also be applicable to FEOL processing.

Non-volatile memory devices such as a resistive random access memory (RRAM) device depend on a phenomenon of resistance switching to store information. The non-volatile memory device functions as a variable resistor where the resistance of the device may switch between a high resistance state and a low resistance state. A non-volatile memory device may be coupled with a selector element to form a memory cell. The selector may be a volatile switching element that is placed in series with the non-volatile memory device. A large collection of such memory cells forms a key component of non-volatile embedded memory.

In accordance with one or more embodiments of the present invention, fabrication processes are described for a vertically integrated memory, such as 3D RRAM, memory in which a direct self-assembly process is used for formation of selector or memory layers for leakage current minimization. One or more embodiments described herein are directed to structures for and approaches to using self-aligned selector layers and/or self-aligned memory layers. In an embodiment, such a memory array is fabricated in the BEOL layers of an integrated circuit. The performance of such a memory may be faster than flash memory, and may be made with higher density than flash memory. In accordance with one or more embodiments of the present disclosure, a vertical string of memory elements is described. Such an architecture may provide a very dense memory architecture since it is a vertical rate in contrast to a planar memory array.

To provide context, state-of-the-art vertical memory arrays may be based on back end of line (BEOL) material. Typically, there are two devices at an intersection of a bitline and a wordline, e.g., a selector material and a memory material.

As an example, Figure 1A illustrates a cross-sectional view of a state-of-the-art vertical RRAM. The vertical RRAM 100A includes a lattice array of interleaved metal wordlines 102

and insulator layers 104 (e.g., silicon nitride, silicon oxide and the like). At the end of the wordlines 102, there is a vertical selective layer/device 106, a vertical memory layer 108 adjacent to the selector layer 106, and a vertical metal bitline 110 adjacent to the memory layer 108. These selector layers/devices 106 are required for RRAM integration due to their non-linear/rectifying I-V characteristics which serve to minimize leakage current from such devices.

There are self-aligned approaches to form the selector layer 106 between adjacent wordlines 102 in the RRAM array 100. In one approach, a conformal selector layer 106 comprising tantalum oxide (TaOx) may be disposed within a trench at the end of tantalum (Ta) wordlines 102, followed by deposition of the memory layer 108, the selector layer 106, and the metal bitline 110, which is conformal to the memory layer 108. One drawback to this approach is that a tantalum oxide selector layer 106 is not selective and will experience increase leakage current between adjacent tantalum wordlines 102 through the selector layer 106. In addition, the leakage current between adjacent wordlines 102 increases as the wordlines 102 are formed closer together.

Figure 1B illustrates another cross-sectional view of a state-of-the-art vertical RRAM 100B, and a second approach to form the selector layer. This approach generally relies upon material transformation of some region of the wordlines 102. In this approach a tantalum (Ta) or titanium nitride (TiN) wordline 102 is oxidized to form regions of tantalum oxide (TaOx) or titanium oxide (TiOx) which functions as a non-continuous selector layer/device 106. The memory layer 108 is also formed in a trench next to the selector layer 106, followed by depositing a metal bitline 110 in the trench is adjacent to the memory layer 108.

This second approach works well when the wordlines 102 are tantalum or titanium nitride and the insulator 104 comprises a silicon nitride insulator, but there are drawbacks. One drawback is that the process is constrained in a material system for the selector layer/device 106 in that the wordline 102 is transformed into the selector layer/device 106 and thus, the selector layer 106 is determined by material composition of the wordlines 102. For example, if tantalum wordlines 102 are used, then the selector layer 106 becomes tantalum oxide, and if titanium wordlines 102 are used, then the selector layer 106 becomes titanium oxide. Another drawback is that although forming a titanium oxide selector layer 106 via oxidation of titanium nitride wordlines 102 is selective, there are process concerns with respect to thermal budget. That is, this approach typically requires a relatively high thermal treatment to anneal the ends of the wordlines 102 that may not be compatible with other devices upon the same die (i.e., Ta oxidation may be optimal at 400C or more).

Example embodiments disclosed herein allow for the introduction of a selector layer/device in a manner that is self-aligning to the wordlines in a vertical RRAM that does not

experience the above limitations, and also provides a reduction in leakage current between adjacent wordlines. The example embodiments also allow for the introduction of resistance-changing memory layers that are also self-aligned to the wordlines in the vertical RRAM array. Both embodiments are enabled through direct self-assembly (DSA) and processing sequences.

5 To exemplify the present embodiments, Figures 2A-2C are diagrams of a vertical memory array fabricated in accordance with the present embodiments. Figure 2A illustrates an angled three-dimensional view of an integrated circuit structure comprising the vertical memory array. In one embodiment, the vertical memory array 200 may represent a 3D RRAM array. Figure 2B illustrates a cross-sectional views of the vertical memory array of Figure 1 along line
10 B, and Figure 2C illustrates a cross-sectional view of the vertical memory array of Figure 1 along line A.

Referring to Figures 2A-2C, the vertical memory array 200 includes a stack of alternating first conductive layers 202 and insulator layers 204 separating the first conductive layers 202. The first conductive layers 202 and insulator layers 204 are shown formed in a horizontal
15 direction over a substrate 206. In one embodiment, the first conductive layers 202 may comprise wordlines 202. In one embodiment, the conductive layers 202 may comprise Cu, Ru, Co, W, other metals and silicides, while the insulator layers 204 may comprise silicon nitride and the like.

A plurality of etch pits 208 are formed through the vertical array of the first conductive
20 layers 202 and the insulator layers 204. A plurality of selectors 210 are formed in the etch pits 208 adjacent to the first conductive layers 202. In one embodiment, the plurality of selectors 210 form a vertical non-continuous selective layer in the etch pits 208. A memory material layer 214 is formed adjacent to the plurality of selectors 210 and the insulating layers 204 in the etch pits 208. In one embodiment, one of the plurality of selectors 210 or the memory material layer 212
25 is self-aligned and has a hemispherical side facing the corresponding etch pit 208. A vertical second conductive layer 212 may fill-in areas of the etch pits 208 not occupied by the plurality of selectors 210 and the memory material layer 212.

In the embodiment shown in the expanded view (dashed box), all of the selectors 210 have a hemispherical side facing the memory material layer 212 and the etch pits 208.
30 According to the disclosed embodiments, the selectors 210 are introduced with a hemispherical side by utilizing a direct self-assembly (DSA) processing sequence. DSA utilizes principles of chemoepitaxy and graphoepitaxy to depose a block copolymer (BSP) comprising first and second polymer components into the etch pits 208. In one example embodiment, the first polymer component may comprise a polystyrene (PS) component and the second polymer
35 component may comprise a polymethylmethacrylate (PMMA) component.

Due to a constrained volume of the nanometer-scale width etch pits 208 having repetitive and regularly spaced conductive layers 202, the block copolymer distributes in a manner such that one of the polymer components (e.g., PS) adheres to the conductive region, while the second polymer component (e.g., PMMA) fills the remainder of the etch pits 208. These polymer components are then processed in a manner that allows one of the polymer components to be removed leaving vacated regions that act as a mold for formation of the selectors 210 and/or memory material layers 212 in the vertical memory array 200. In one embodiment, the DSA process results in the vacated regions having a hemispherical side facing the etch pits. Either the selective layer 210 or the memory material layer 212 are subsequently formed in these vacated regions, resulting in either the selective layer 210 or the memory material layer 212 also having a hemispherical side.

In one embodiment, the memory material layer 214 is conformal to the plurality of selectors 210 and the insulating layers 204. In one embodiment, the selector 210 may comprise materials such as an Al₂O₃ tunnel barrier, TaO_x, NbO_x, VO_x, or similar materials. In one embodiment, the memory material layer 212 may comprise HfO₂, TiO_x, TaO_x, NiO_x or the like. Also, in the embodiment shown, the first conductive layers 202 are recessed from the etch pits 208 to increase leakage current suppression.

The disclosed embodiments are advantageous in the sense that a self-aligned selector layer is introduced (whereas the existing approach does not) and eliminates or significantly reduces the sneak leakage problem between adjacent vertical wordlines. The disclosed embodiments also allows for increased vertical scaling as the insulating layers between the wordlines can be scaled much further as sneak leakage is not an issue. This allows for a greater number of vertical devices to be stacked without exceeding the capability of etch processes.

Another advantage is that the disclosed embodiments allow for any combination of wordline material and selector material, which enables the selector material to be optimized for device performance and leakage current concerns and the wordline to be optimized for resistivity and integration ease. Further, the disclosed embodiments eliminate the need for any material transformation of a section of the wordline to a new material, which frequently involves thermal processes which may be deleterious to other devices that may exist upon the wafer (i.e., gate workfunction materials of any logic circuitry or any metallization and contact structures).

As an exemplary processing scheme involving fabrication of a vertical RRAM array having a discontinuous or discrete selector layer, refer to the following Figures illustrating views of various stages in a method of fabricating a vertical memory array integrate circuit structure in accordance with an embodiment of the present disclosure, where like components have like reference numerals.

Referring to Figure 3, a method of fabricating an integrated circuit structure comprising vertical memory array 300 may begin by forming a stack of alternating horizontal conductive layers 202 and horizontal insulating layers 204 over substrate 206. In one embodiment, the vertical memory array 300 will form a vertical or 3D RRAM. Although vertical memory array 300 shows six conductive layers and seven insulating layers, any number of alternating conductor/insulator pairs may be utilized. The conductive layers 202 may be comprised of a metal such as Pt, Ti, Al, Ta, Ti, Ru or of electrically conductive materials such as TiN or other suitable conductive metals or materials. The insulating layer may be comprised of silicon dioxide, silicon oxynitride, silicon nitride, or other suitable insulating oxides, nitrides or carbides or of other materials. These depositions may be performed via a plasma-enhanced CVD process, an atomic-layer deposition process or via other suitable deposition processes.

Figure 4A illustrates an angled three-dimensional view of the vertical memory array 400 showing that after the alternating conductive and insulator layers 202 and 204 are formed, an array of etch pits 208 is formed through the alternating conductive and insulating layers 202 and 204 using standard etch and lithographic processing.

Figure 4B illustrates a cross-sectional view of the vertical memory array of Figure 4A along line A showing the interior of the etch pits 208. The etch pits 208 are formed to expose to expose sides of the conductive and insulating layers 202 and 204 in the stack. In one embodiment, the etch pits 208 may be of radius of several to several tens of nanometers. The etch pits 208 are shown with a square cross section, but in practice may be oval, circular, ellipsoidal or another shape.

Figure 4B also shows that according to an optional embodiment, a wet etchant may be used on the conductive layers 202 in the etch pits 208 prior to the applying the direct self-assembly process to form lateral recesses 402 in the conductive layers 202. This process recesses laterally the conductive layers 202 via a timed wet etch process. This process may yield additional increased leakage current suppression and improved yield.

Figure 5 illustrates an embodiment of the vertical memory array 500 after the formation of the etch pits 208, but without performing a subsequent wet etch on the conductive layers 202, which provides substantially planar etch pit sidewalls.

Figure 6A-6C illustrate the vertical memory array 600 after the array of etch pits 208 are formed (with lateral recesses in this example) and after a direct self-assembly process is performed to fill the etch pits 208 with a block copolymer comprising first and second polymer components 602 and 604. Figure 6A illustrates an angled three-dimensional view of the vertical memory array 600. Figure 6B illustrates a cross-sectional view of the vertical memory array 600 of Figure 6A along line B, and Figure 6C illustrates a cross-sectional view of the vertical

memory array 600 of Figure 6A along line A.

An example of a block copolymer is polystyrene-b-polymethylmethacrylate (PS-b-PMMA), where one polymer is hereinafter referred to as PS and the second as PMMA. As used herein, first and second polymer components 602 and 604 may alternatively be referred to as PS
5 602 and PMMA 604, respectively. Although the use of a PS/PMMA block copolymer will be described according to one embodiment, alternative block copolymers may also be used.

Direct self-assembly (DSA) is used to order the polymer components of the block copolymer in a defined manner, specifically, utilizing techniques of graphoepitaxy and chemoepitaxy. In graphoepitaxy, the volume for self-assembly is confined (i.e., from a radius or
10 cross-sectional distance of the etch pits 208), and sidewalls of the etch pits 208 are coated to wet one of the polymer components.

Using chemoepitaxy, molecules/chemicals nominally called “brushes” are grafted (i.e., covalently bound) to the existing sidewall pattern to guide the polymer components to specific locations. These molecules/brushes interact favorably with one of the polymer components (a 1-
15 brush or single color scheme), or two brushes may be selected that interact with one polymer component but not the other (a 2-brush or two color scheme). These brushes/polymers for DSA process are commercially available. Similarly, block copolymers may also be commercially available. The polymers can be readily engineered to provide different properties. These molecules/chemicals can be readily engineered to provide different properties.

20 One key parameter of interest is the Flory-Huggins χ parameter which describes how energetically favorable it is for the two polymer components 602 and 604 to mix. By controlling this parameter, the morphology of the resultant system can be controlled when the polymer components 602 and 604 are mixed in contact with a metallic or insulating surface.

Figure 7A illustrates a phase diagram for PS-b-PMMA demonstrating possible DSA
25 morphologies as a function (f) of the first polymer component (A) 602, the second polymer component (B) 604, and the Flory-Huggins χ_n value. Once applied, the two different polymer components will segregate depending on the fractions of the first polymer component (A) 602 relative to the second polymer component (B) 604, and the effect of changing the relative ratios is shown in the resultant morphologies of Figure 6A. “A” and “B” can represent either PS or
30 PMMA, since the phase diagram is symmetric about $f_A = 0.5$. For example, PS-b-PMMA can be formulated in a symmetric 50:50 blend that produces lamellar self-assembled domains. If the fraction is adjusted to 30:70 or 70:30, the polymer produces cylinders of the minority fraction assembled in a hexagonal pattern in a sea of the majority fraction.

According to the present disclosure, DSA f_A values that produce cylinder or spherical
35 morphologies are used to introduce self-aligned selectors 210 and/or memory layer 212, which

results in hemispherical sidewalls for the first polymer component 602 once applied to the conductive layers 202. The length-scale of the morphologies resultant from polymer deposition from Figure 7A may also be engineered as may be the thickness of the polymer coating applied to the conductive layers 202. The X value is multiplied by the overall number of monomer units, n , in each block fraction of the chain to produce an X_n value that dictates the intrinsic periodicity of the assembled system. Longer block copolymer chain lengths, with correspondingly higher X_n values, produce longer intrinsic periodicities. In such a manner, a polymer can be engineered to form these structures upon incoming structures of different dimension of both vertical thickness of conductive layers 202 and etch pits width so that a polymer component that is adjacent to one conductive layer 202 does not bridge to the polymer component adjacent to a neighboring conductive layer 202.

During the chemoepitaxy process, a PS-attractive thiol brush (not shown) is first grafted directly to the conductive layers 202 along the sidewalls of etch pits 208. The thiol brush bridges the insulating layers 204 provided the width of the insulating layers 204 is less than an intrinsic periodicity. If the regions separating the conductive layers 202 are separated by a distance greater than the characteristic length, the polymer will not bridge the conductive layers 202. Next, a second brush, based on an alcohol or phosphate end group is grafted to the insulator layers 204 dielectric surfaces along the sidewalls of etch pits 208.

Figure 7B illustrates example block copolymer depositions within a cross-section of confined etch pits 208 for varying Flory-Huggins X_n values. Depending upon the Flory-Huggins X_n value and the radius of the etch pit 208, the resultant morphology of the BCP is changed in a well-controlled and predictable manner. In one embodiment, the higher the Flory-Huggins X_n value during the graphoepitaxy process, the more unfavorable it is for the block copolymers to mix. In one embodiment, an X_n value of approximately 40-60 is selected, as shown on the right-hand side of Figure 7B, such that the first polymer component 602 (e.g., PS) adheres to the conductive layers 202 in the etch pits 208 with well-defined hemispherical cross-sections, while the second polymer component 604 (e.g., PMMA) fills in the remaining region of the etch pits 208.

Referring again to Figures 6A-6C, the PS component 602 is shown assembled over the conductive layers 202, and the PMMA component 604 is shown assembled over the insulator layers 204. In a manner described above, a BCP system may be customized for etch pits 208 having a radius of a few nanometers to several tens of nanometers. This process is highly repeatable. In subsequent processing steps, the PS component 602 is removed leaving trace PS chemicals on the conductive layers 202. Similarly, the PMMA component 604 is subsequently removed leaving trace PMMA chemicals on the insulating layers 204.

According to a further aspect of the example embodiments, the process may be tone inverted to swap the PS/PMMA regions in the resultant structure. For example, in an alternative embodiment, a PMMA attractive thiol brush, or a PS attractive hydroxyl brush, may be used such that the PS component 602 assembles over the insulating layers 204 and the PMMA component 604 assembles over the conductive layers 202. In subsequent processing steps, the PS component 602 is removed leaving trace PS chemicals on the insulating layers 204. Similarly, the PMMA component 604 is subsequently removed leaving trace PMMA chemicals on the conductive layers 202.

Various embodiments presented herein discuss forming the DSA layers, where the block copolymer may be PS-b-PMMA. However, in other examples, any other appropriate type of polymers may also be used. Examples of such polymers include, but are not limited to, poly(styrene)-b-poly(2-vinylpyridine) (PS-b-P2VP), poly(styrene)-b-poly(4-vinylpyridine) (PS-b-P4VP), poly(styrene)-b-poly(acrylic acid) (PS-b-PAA), poly(styrene)-b-poly(ethylene glycol) (PS-b-PEG), poly(styrene)-b-poly(imide) (PS-b-PI), and poly(styrene)-b-poly(dimethylsiloxane) (PS-b-PDMS). For any of these block co-polymers additives can be introduced to modify the pitch, and X_n value of the system. These systems and their processing may be at least in part analogous to the BCP comprising the PS-b-PMMA system discussed herein.

Figures 8A and 8B illustrate cross-sectional views of vertical memory array 800 after DSA block copolymer deposition and after the second polymer component 604 (e.g., PMMA) is removed from the vertical memory array. Figure 8A illustrates a cross-sectional view of the vertical memory array of Figure 6A along line B, and Figure 8B illustrates a cross-sectional view of the vertical memory array along line A. After the etch and removal of the second polymer component 604, the first polymer component 602 is left in place over the conducting layers 202. Etchants are available for polymer systems with exceptionally high etch selectivity. The PMMA component 604 has a higher etch rate using Ar/O₂, Ar, N₂/H₂, and Ar/CO/N₂ etch chemistries. Wet etches using acetic acid are almost infinitely selective to PMMA component in the polymer. Other etchants may be utilized for other polymer systems or for the described PS/PMMA system.

Figure 9A continues with cross-sectional views of the vertical memory array of Figure 6A along lines B and along line A, respectively. Figures 9A and 9B illustrate the vertical memory array 900 after the memory material layer 210 is formed in the etch pits 208 conformal to the first polymer component 212 and to edges of the insulating layers 204. In one embodiment, the memory material layer 212 may be formed by performing an isotropic deposition on the sides of the etch pits using atomic layer deposition (ALD) or chemical vapor deposition (CVD). In one embodiment, the memory layer 212 may represent any type of

resistance-changing layer. In one embodiment, the memory material layer 212 may comprise HfO₂, TiO_x, TaO_x, NiO_x or the like.

Figures 9A and 9B further illustrate the vertical memory array 900 after the second conductive layer 212 is formed in the etch pits 206 in regions vacated by the removed second polymer component 604. In one embodiment, the second conductive layer 212 fills the etch pits 208 in areas not already occupied by the first polymer component 602 and the memory material layer 212. In one embodiment, the second conductive layer 212 forms bitlines. In one embodiment, the second conductive layer 212 may comprise Cu, Ru, Pt, Co, Ni, W, Ta or another conductive material.

Figures 10A and 10B illustrate an angled three-dimensional view and a cross-sectional view the vertical memory array 1000, respectively, after trenches are formed through the conducting layers 202 and the insulating layers 204 to expose a side (and central region) of the etch pits, as shown. The trenches 1002 are also formed to separate the vertical memory array 1002 into rows, columns, and/or sub-arrays. The trenches 1002 are formed using standard lithographic and dry/plasma etch techniques.

Figures 11A and 11B illustrate an angled three-dimensional view and a cross-sectional view the vertical memory array 1100, respectively, after the first polymer component 602 is removed from the exposed sides of the etch pits 208 to create vacated regions 1102 having hemispherical cross-sections. The first polymer component 602 (e.g., PS) is removed via a wet etch using an acetic acid or another etchant.

Figure 12A-12C illustrate the vertical memory array 1200 after the plurality of selectors 210 are formed by filling each of the vacated regions 1102 with a selector layer, i.e. Figure 12A illustrates an angled three-dimensional view of the vertical memory array 1200. Figure 12B illustrates a top view, Figure 12C illustrates a cross-sectional view of the vertical memory array 1200 along line B, and Figure 12D illustrates a cross-sectional view of the vertical memory array 1200 of Figure 12A along line A.

In one embodiment, the plurality of selectors 210 form a vertical non-continuous selector layer in the etch pits 208, where each selector is formed in the vacated regions 1102 formed by the removed first polymer component 602 (e.g., PS). According to the disclosed embodiments, the vacated regions 1102 formed by the removed first polymer component 602 acts as a mold for the selectors 210. Because the vacated regions 1102 were formed by removal of the first polymer component 602 that had hemispherical cross-sections and aligned with the wordlines, the vacated regions 1102 likewise have hemispherical cross-sections and align with the wordlines. The selector layer is conformal to the vacated regions 1102 forming selectors 210 that are self-aligned with the conductive layers 202 and that also have hemispherical cross-sections. Also, the

selectors 210 wrap around three sides of the etch pits 208. In one embodiment, the selectors 602 may comprise one of an Al₂O₃ tunnel barrier, TaO_x, NbO_x, VO_x, or the like.

In one embodiment, the selectors 210 is inserted into the vacated regions 1102 via use of a CVD or other process. The vacated regions 1102 can be refilled or very nearly filled with the selector layer. However, this process is robust in the event that an incomplete fill results an airgap between the conductive layers 202 and the memory material layer 212 instead of a selector layer, which will prevent any localized leakage current while the memory will still switch through the adjacent region which is covered by a selector layer. This selector material will typically have a rectifying characteristic to its I-V curve and of particular interest are threshold switching selector materials. Selector materials may include materials such as Al₂O₃ tunnel barrier, TaO_x, NbO_x, VO_x, or similar materials.

Alternative embodiments of the process to replace the BCP system with the memory/bitline and selector layers are described below. One alternative embodiment would entail removal of the PMMA component from the top of the wafer and replacement of this layer with a mechanically stable layer such as SiO₂ before the trench formation.

Finally, the trenches 1002 are cleaned with a reactive ion or wet etch process and filled with an insulating material such as SiO₂, silicon oxynitride, or similar material. A staircase memory contact structure (if applicable) is formed and the vertical memory array is completed, as shown in Figure 2A-2C.

This structure is shown with a staircase contact in place for the memory arrays, and the dielectric which would be present around the staircase contact is omitted to show detail.

Figures 13A-13C illustrate the vertical memory array 1300 according to a second embodiment of the disclosure, where the first polymer component 602 of the BCP is replaced with the memory material layer 212, rather than the selectors 210, and the memory material layer 212 is formed self-aligned to the first conductive layer 202. The process of the second embodiment begins with the state of the vertical memory array of Figures 8A and 8B in which the second polymer component 604 (e.g., PMMA) is removed from the vertical memory array).

Figure 13A illustrates an angled three-dimensional view of the vertical memory array 1300 after the second polymer component 604 (e.g., PMMA) is removed from the etch pits 208 and is replaced by filling the etch pits 208 with the second conductive layer 214 in the regions vacated by the removed second polymer component 604. In one embodiment, the second conductive layer 214 is a metal that comprises the bitline of the vertical memory array 1300.

Figure 13B illustrate an angled three-dimensional view of the vertical memory array 1300 after trenches 1002 are formed to separate the vertical memory array into rows, columns or sub-arrays, and to open one side of the etch pits 208. Figure 13B further shows that once sides of

the etch pits 208 are exposed, the first polymer component 602 (PS) is removed from the exposed side of the trenches 1002 to create vacated regions 1302.

Figure 13C illustrate an angled three-dimensional cross-sectional view the vertical memory array 1300 after the vacated regions 1302 are filled with the memory material layer 212 that is conformal to the vacated regions 1302. In one embodiment, the memory material layer 212 is non-continuous, is self-aligned with the wordlines, and inherits the hemispherical cross-section of the vacated regions 1302. In one embodiment, the memory material layer to enter 12 is deposited into via a CVD, ALD or other process, Also, the memory material layer 212 wraps around three sides of the etch pits 208. This deposition need not completely fill the vacated region 1302 with the memory material layer 212, but should fill at least some portion of the vacated regions 1302. Thus, according to the second embodiment, the second polymer component 604 (PMMA) of the BCP is replaced with a bitline and the first polymer component 602 (PS) is replaced with the resistance-changing memory material layer.

At this point, the memory formed with this second embodiment of the invention is completed and additional processing may form a staircase contact or other contact structure. It should be readily apparent to those of ordinary skill in the art, the present embodiment refer to vertical conductor layers as bitlines and horizontal conductor layers as wordlines, but in an alternative embodiments this could be reversed.

The integrated circuit structures described herein may be included in an electronic device. As an example of one such apparatus, Figures 14A and 14B are top views of a wafer and dies that include one or more embedded non-volatile memory structures utilizing direct self-assembly process for formation of selector or memory layers, in accordance with one or more of the embodiments disclosed herein.

Referring to Figures 14A and 14B, a wafer 1400 may be composed of semiconductor material and may include one or more dies 1402 having integrated circuit (IC) structures formed on a surface of the wafer 1400. Each of the dies 1402 may be a repeating unit of a semiconductor product that includes any suitable IC (e.g., ICs including one or more embedded non-volatile memory structures having a bilayer selector, such as described above. After the fabrication of the semiconductor product is complete, the wafer 1400 may undergo a singulation process in which each of the dies 1402 is separated from one another to provide discrete “chips” of the semiconductor product. In particular, structures that include embedded non-volatile memory structures having an independently scaled selector as disclosed herein may take the form of the wafer 1400 (e.g., not singulated) or the form of the die 1402 (e.g., singulated). The die 1402 may include one or more embedded non-volatile memory structures based independently scaled selectors and/or supporting circuitry to route electrical signals, as well as

any other IC components. In some embodiments, the wafer 1400 or the die 1402 may include an additional memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., an AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 1402. For example, a memory array formed
5 by multiple memory devices may be formed on a same die 1402 as a processing device or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits
10 include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The
15 integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

Figure 15 illustrates a block diagram of an electronic system 1500, in accordance with an
20 embodiment of the present disclosure. The electronic system 1500 can correspond to, for example, a portable system, a computer system, a process control system, or any other system that utilizes a processor and an associated memory. The electronic system 1500 may include a microprocessor 1502 (having a processor 1504 and control unit 1506), a memory device 1508, and an input/output device 1510 (it is to be appreciated that the electronic system 1500 may have
25 a plurality of processors, control units, memory device units and/or input/output devices in various embodiments). In one embodiment, the electronic system 1500 has a set of instructions that define operations which are to be performed on data by the processor 1504, as well as, other transactions between the processor 1504, the memory device 1508, and the input/output device 1510. The control unit 1506 coordinates the operations of the processor 1504, the memory
30 device 1508 and the input/output device 1510 by cycling through a set of operations that cause instructions to be retrieved from the memory device 1508 and executed. The memory device 1508 can include a vertical memory array as described in the present description. In an embodiment, the memory device 1508 is embedded in the microprocessor 1502, as depicted in Figure 15. In an embodiment, the processor 1504, or another component of electronic system
35 1500, includes one or more embedded non-volatile memory structures having a self-aligned

selector, such as those described herein.

Figure 16 is a cross-sectional side view of an integrated circuit (IC) device assembly that may include one or more embedded non-volatile memory structures utilizing direct self-assembly process for formation of selector or memory layers, in accordance with one or more of the embodiments disclosed herein.

Referring to Figure 16, an IC device assembly 1600 includes components having one or more integrated circuit structures described herein. The IC device assembly 1600 includes a number of components disposed on a circuit board 1602 (which may be, e.g., a motherboard). The IC device assembly 1600 includes components disposed on a first face 1640 of the circuit board 1602 and an opposing second face 1642 of the circuit board 1602. Generally, components may be disposed on one or both faces 1640 and 1642. In particular, any suitable ones of the components of the IC device assembly 1600 may include a number of embedded non-volatile memory structures having a bilayer selector, such as disclosed herein.

In some embodiments, the circuit board 1602 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 1602. In other embodiments, the circuit board 1602 may be a non-PCB substrate.

The IC device assembly 1600 illustrated in Figure 16 includes a package-on-interposer structure 1636 coupled to the first face 1640 of the circuit board 1602 by coupling components 1616. The coupling components 1616 may electrically and mechanically couple the package-on-interposer structure 1636 to the circuit board 1602, and may include solder balls (as shown in Figure 16), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

The package-on-interposer structure 1636 may include an IC package 1620 coupled to an interposer 1604 by coupling components 1618. The coupling components 1618 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 816. Although a single IC package 1620 is shown in Figure 16, multiple IC packages may be coupled to the interposer 1604. It is to be appreciated that additional interposers may be coupled to the interposer 1604. The interposer 1604 may provide an intervening substrate used to bridge the circuit board 1602 and the IC package 1620. The IC package 1620 may be or include, for example, a die (the die 1402 of Figure 14B), or any other suitable component. Generally, the interposer 1604 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 1604 may couple the

IC package 1620 (e.g., a die) to a ball grid array (BGA) of the coupling components 1616 for coupling to the circuit board 1602. In the embodiment illustrated in Figure 16, the IC package 1620 and the circuit board 1602 are attached to opposing sides of the interposer 1604. In other embodiments, the IC package 1620 and the circuit board 1602 may be attached to a same side of the interposer 1604. In some embodiments, three or more components may be interconnected by way of the interposer 1604.

The interposer 1604 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some implementations, the interposer 1604 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 1604 may include metal interconnects 1610 and vias 1608, including but not limited to through-silicon vias (TSVs) 1606. The interposer 1604 may further include embedded devices 1614, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 1604. The package-on-interposer structure 1636 may take the form of any of the package-on-interposer structures known in the art.

The IC device assembly 1600 may include an IC package 1624 coupled to the first face 1640 of the circuit board 1602 by coupling components 1622. The coupling components 1622 may take the form of any of the embodiments discussed above with reference to the coupling components 1616, and the IC package 1624 may take the form of any of the embodiments discussed above with reference to the IC package 1620.

The IC device assembly 1600 illustrated in Figure 16 includes a package-on-package structure 1634 coupled to the second face 1642 of the circuit board 1602 by coupling components 1628. The package-on-package structure 1634 may include an IC package 1626 and an IC package 1632 coupled together by coupling components 1630 such that the IC package 1626 is disposed between the circuit board 1602 and the IC package 1632. The coupling components 1628 and 1630 may take the form of any of the embodiments of the coupling components 1616 discussed above, and the IC packages 1626 and 1632 may take the form of any of the embodiments of the IC package 1620 discussed above. The package-on-package structure 1634 may be configured in accordance with any of the package-on-package structures known in the art.

Figure 17 illustrates a computing device 1700 in accordance with one implementation of the disclosure. The computing device 1700 houses a board 1702. The board 1702 may include a number of components, including but not limited to a processor 1704 and at least one communication chip 1706. The processor 1704 is physically and electrically coupled to the board 1702. In some implementations the at least one communication chip 1706 is also physically and electrically coupled to the board 1702. In further implementations, the communication chip 1706 is part of the processor 1704.

Depending on its applications, computing device 1700 may include other components that may or may not be physically and electrically coupled to the board 1702. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 1706 enables wireless communications for the transfer of data to and from the computing device 1700. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1706 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1700 may include a plurality of communication chips 1706. For instance, a first communication chip 1706 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1706 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1704 of the computing device 1700 includes an integrated circuit die packaged within the processor 1704. In some implementations of the disclosure, the integrated circuit die of the processor includes one or more embedded non-volatile memory structures having a bilayer selector, in accordance with implementations of embodiments of the disclosure. The term “processor” may refer to any device or portion of a device that processes electronic

data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1706 also includes an integrated circuit die packaged within the communication chip 1706. In accordance with another implementation of embodiments of the disclosure, the integrated circuit die of the communication chip includes one or more embedded non-volatile memory structures having a bilayer selector, in accordance with implementations of embodiments of the disclosure.

In further implementations, another component housed within the computing device 1700 may contain an integrated circuit die that includes one or more embedded non-volatile memory structures having a self-aligned selector, in accordance with implementations of embodiments of the disclosure.

In various implementations, the computing device 1700 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1700 may be any other electronic device that processes data.

The above description of illustrated implementations of embodiments of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Example embodiment 1: An integrated circuit structure includes a stack of alternating first conductive layers and insulator layers. A plurality of etch pits are through the first conductive layers in the insulator layer. A plurality of selectors are in the etch pits adjacent to the first conductive layers. A memory material layer is adjacent to the plurality of selectors in the etch pits, wherein one of the plurality of selectors and the memory material layer is self-aligned and has a hemispherical side facing the corresponding etch pit.

Example embodiment 2: The integrated circuit structure of example embodiment 1, further comprising a vertical second conductive layer that fills-in areas of the etch pits not

occupied by the plurality of selectors and the memory material layer.

Example embodiment 3: The integrated circuit structure of example embodiment 1-2, wherein the plurality of selectors are self-aligned and have hemispherical sides, and wherein the plurality of selectors form a non-continuous selective layer.

5 Example embodiment 4: The integrated circuit structure of example embodiment 1-3, wherein the selectors comprise one of Al₂O₃ tunnel barrier, TaO_x, NbO_x, and VO_x, and the memory material layer comprises one of HfO₂, TiO_x, TaO_x, and NiO_x.

10 Example embodiment 5: The integrated circuit structure of example embodiment 1-4, wherein the first conductive layers are recessed within the etch pits to increase leakage current suppression.

Example embodiment 6: The integrated circuit structure of example embodiment 1-5, wherein the one of the selective layer and memory material layer are in a vacated region formed by a removed polymer component of a block copolymer.

15 Example embodiment 7: The integrated circuit structure of example embodiment 1-6, wherein the etch pits are filled with a block copolymer comprising a first polymer component and a second polymer component by a direct self-assembly (DSA) process.

Example embodiment 8: The integrated circuit structure of example embodiment 7, wherein the first polymer component and the second polymer component comprise a polystyrene (PS) component and polymethylmethacrylate (PMMA) component, respectively.

20 Example embodiment 9: The integrated circuit structure of example embodiment 7-8, wherein the PS component is assembled over the conductive layers and is subsequently removed leaving trace PS chemicals on the conductive layers, and wherein the PMMA component is assembled over the insulator layers and is subsequently removed, leaving trace PMMA chemicals on the insulating layers.

25 Example embodiment 10: The integrated circuit structure of example embodiment 7-9, wherein the PS component is assembled over the insulating layers and subsequently removed leaving trace PS chemicals on the insulating layers, and wherein the PMMA component is assembled over the conductive layers and subsequently removed leaving trace PMMA chemicals on the conductive layers.

30 Example embodiment 11: The integrated circuit structure of example embodiment 7-9, wherein direct self-assembly function values are used that produce cylinder or spherical morphologies to introduce self-aligned selectors.

Example embodiment 12: A method of fabricating a vertical memory array, the method comprises forming a stack of alternating conductive layers and insulating layers over a substrate.

35 An array of etch pits is formed through the alternating conductive layers and insulating layers,

exposing sides of the conductive layers and the insulating layers. A direct self-assembly process is performed to fill the etch pits with a block copolymer comprising a first polymer component and a second polymer component such that the first polymer component adheres to the conductive layers in the etch pits with hemispherical cross-sections, while the second polymer component fills in a remaining region of the etch pits. The second polymer component is removed from the etch pits. A memory material layer is formed in the etch pits conformal to the first polymer component and to edges of the insulating layers. A second conductive layer is formed in the etch pits in first regions vacated by the removed second polymer component. Trenches are formed in the conducting layers and the insulating layers to expose a side of the etch pits. The first polymer component is removed from the exposed sides of the trenches to create second vacated regions having hemispherical cross-sections. A plurality of selectors is formed by filling each of the second vacated regions with a selector layer that is conformal to the second vacated regions to form a plurality of selectors that are self-aligned to the first conductive layer and that have hemispherical cross-sections. The vertical memory array is filled with an insulating material.

Example embodiment 13: The method of example embodiment 12, further comprising: selecting DSA morphologies as a function (f) that produce cylinder or spherical morphologies for the first polymer component and the second polymer component.

Example embodiment 14: The method of example embodiment 13, further comprising: utilizing polystyrene-bpolymethylmethacrylate (PS-b-PMMA) as the block copolymer.

Example embodiment 15: The method of example embodiment 14, further comprising: selecting a Flory-Huggins X_n value of approximately 40-60.

Example embodiment 16: The method of example embodiment 12-15, further comprising: incompletely filling the second vacated regions with the selector layer.

Example embodiment 17: The method of example embodiment 12-16, further comprising: forming lateral recesses in the conductive layers facing the etch pits.

Example embodiment 18: The method of example embodiment 12-17, wherein the selectors comprise one of Al_2O_3 tunnel barrier, TaOx, NbOx, and VOx, and the memory material layer comprises one of HfO₂, TiOx, TaOx, and NiOx.

Example embodiment 19: The method of example embodiment 12-18, forming the first conductive layer as wordlines, and forming the second conductive layer as bitlines.

Example embodiment 20: A method of fabricating a vertical memory array comprises forming a stack of alternating conductive layers and insulating layers over a substrate. An array of etch pits is formed through the alternating conductive layers and insulating layers, exposing sides of the conductive layers and the insulating layers. A direct self-assembly process is

performed to fill the etch pits with a block copolymer comprising a first polymer component and a second polymer component such that the first polymer component adheres to the conductive layers in the etch pits with hemispherical cross-sections, while the second polymer component fills in a remaining region of the etch pits. The second polymer component is removed from the etch pits. The etch pits are filled with a second conductive layer in first regions vacated by the removed second polymer component. Trenches are formed in the conducting layers and the insulating layers to expose a side of the etch pits. The first polymer component is removed from the exposed sides of the trenches to create second vacated regions having hemispherical cross-sections. Each of the second vacated regions are filled with a memory material layer that is conformal to the second vacated regions such that the memory material layer is non-continuous, is self-aligned with the first conductive layers, and inherits the hemispherical cross-section of the vacated regions. The vertical memory array is filled with an insulating material.

Example embodiment 21: The method of example embodiment 20 further comprising: selecting DSA morphologies as a function (f) that produce cylinder or spherical morphologies for the first polymer component and the second polymer component.

Example embodiment 22: The method of example embodiment 21 further comprising: utilizing polystyrene-bpolymethylmethacrylate (PS-b-PMMA) as the block copolymer.

Example embodiment 23: The method of example embodiment 22 further comprising: selecting a Flory-Huggins X_n value of approximately 40-60.

Example embodiment 24: The method of example embodiment 20-23 further comprising: incompletely filling the second vacated regions with the memory material layer.

Example embodiment 25: The method of example embodiment 20-24 further comprising: forming lateral recesses in the conductive layers facing the etch pits.

CLAIMS**What is claimed is:**

1. An integrated circuit structure, comprising:
5 a stack of alternating first conductive layers and insulator layers;
a plurality of etch pits through the first conductive layers;
a plurality of selectors in the etch pits adjacent to the first conductive layers; and
a memory material layer adjacent to the plurality of selectors in the etch pits, wherein one
of the plurality of selectors and the memory material layer is self-aligned and has a
10 hemispherical side facing the corresponding etch pit.
2. The integrated circuit structure of claim 1, further comprising a vertical second
conductive layer that fills-in areas of the etch pits not occupied by the plurality of selectors and
the memory material layer.
15
3. The integrated circuit structure of claim 1, wherein the plurality of selectors are self-
aligned and have hemispherical sides, and wherein the plurality of selectors form a non-
continuous selective layer.
- 20 4. The integrated circuit structure of claim 1, wherein the selectors comprise one of Al₂O₃
tunnel barrier, TaO_x, NbO_x, and VO_x, and the memory material layer comprises one of HfO₂,
TiO_x, TaO_x, and NiO_x.
5. The integrated circuit structure of claim 1, wherein the first conductive layers are
25 recessed within the etch pits to increase leakage current suppression.
6. The integrated circuit structure of claim 1, wherein the one of the selective layer and
memory material layer are in a vacated region formed by a removed polymer component of a
block copolymer.
30
7. The integrated circuit structure of claim 6, wherein the etch pits are filled with a block
copolymer comprising a first polymer component and a second polymer component by a direct
self-assembly (DSA) process.
- 35 8. The integrated circuit structure of claim 7, wherein the first polymer component and the

second polymer component comprise a polystyrene (PS) component and polymethylmethacrylate (PMMA) component, respectively.

9. The integrated circuit structure of claim 8, wherein the PS component is assembled over
5 the conductive layers and is subsequently removed leaving trace PS chemicals on the conductive layers, and wherein the PMMA component is assembled over the insulator layers and is subsequently removed, leaving trace PMMA chemicals on the insulating layers.
10. The integrated circuit structure of claim 8, wherein the PS component is assembled over
10 the insulating layers and subsequently removed leaving trace PS chemicals on the insulating layers, and wherein the PMMA component is assembled over the conductive layers and subsequently removed leaving trace PMMA chemicals on the conductive layers.
11. The integrated circuit structure of claim 8, wherein direct self-assembly function values
15 are used that produce cylinder or spherical morphologies to introduce self-aligned selectors.
12. A method of fabricating a vertical memory array, the method comprising:
forming a stack of alternating conductive layers and insulating layers over a substrate;
forming an array of etch pits through the alternating conductive layers, exposing sides of
20 the conductive layers and the insulating layers;
performing a direct self-assembly process to fill the etch pits with a block copolymer comprising a first polymer component and a second polymer component such that the first polymer component adheres to the conductive layers in the etch pits with hemispherical cross-sections, while the second polymer component fills in a remaining region of the etch pits;
25 removing the second polymer component from the etch pits;
forming a memory material layer in the etch pits conformal to the first polymer component and to edges of the insulating layers;
forming a second conductive layer in the etch pits in first regions vacated by the removed second polymer component;
30 forming trenches in the conducting layers and the insulating layers to expose a side of the etch pits;
removing the first polymer component from the exposed sides of the trenches to create second vacated regions having hemispherical cross-sections; and
forming a plurality of selectors by filling each of the second vacated regions with a
35 selector layer that is conformal to the second vacated regions to form a plurality of selectors that

are self-aligned to the first conductive layer and that have hemispherical cross-sections; and filling the vertical memory array with an insulating material.

13. The method of claim 12, further comprising: selecting DSA morphologies as a function
5 (f) that produce cylinder or spherical morphologies for the first polymer component and the second polymer component.

14. The method of claim 13, further comprising: utilizing polystyrene-
bpolydimethylmethacrylate (PS-b-PDMM) as the block copolymer.
10

15. The method of claim 14, further comprising: selecting a Flory-Huggins X_n value of approximately 40-60.

16. The method of claim 12, further comprising: incompletely filling the second vacated
15 regions with the selector layer.

17. The method of claim 12, further comprising: forming lateral recesses in the conductive layers facing the etch pits.

20 18. The method of claim 12, wherein the selectors comprise one of Al_2O_3 tunnel barrier, TaO_x , NbO_x , and VO_x , and the memory material layer comprises one of HfO_2 , TiO_x , TaO_x , and NiO_x .

19. The method of claim 12 further comprising: forming the first conductive layer as
25 wordlines, and forming the second conductive layer as bitlines.

20. A method of fabricating a vertical memory array, comprising:
forming a stack of alternating conductive layers and insulating layers over a substrate;
forming an array of etch pits through the alternating conductive layers, exposing sides of
30 the conductive layers and the insulating layers;
performing a direct self-assembly process to fill the etch pits with a block copolymer comprising a first polymer component and a second polymer component such that the first polymer component adheres to the conductive layers in the etch pits with hemispherical cross-sections, while the second polymer component fills in a remaining region of the etch pits;
35 removing the second polymer component from the etch pits;

filling the etch pits with a second conductive layer in first regions vacated by the removed second polymer component;

forming trenches in the conducting layers and the insulating layers to expose a side of the etch pits;

5 removing the first polymer component from the exposed sides of the trenches to create second vacated regions having hemispherical cross-sections; and

filling each of the second vacated regions with a memory material layer that is conformal to the second vacated regions such that the memory material layer is non-continuous, is self-aligned with the first conductive layers, and inherits the hemispherical cross-section of the

10 vacated regions; and

filling the vertical memory array with an insulating material.

21. The method of claim 20, further comprising: selecting DSA morphologies as a function (f) that produce cylinder or spherical morphologies for the first polymer component and the
15 second polymer component.

22. The method of claim 21, further comprising: utilizing polystyrene-bpolymethylmethacrylate (PS-b-PMMA) as the block copolymer.

20 23. The method of claim 22, further comprising: selecting a Flory-Huggins X_n value of approximately 40-60.

24. The method of claim 20, further comprising: incompletely filling the second vacated regions with the memory material layer.

25

25. The method of claim 20, further comprising: forming lateral recesses in the conductive layers facing the etch pits.

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100A

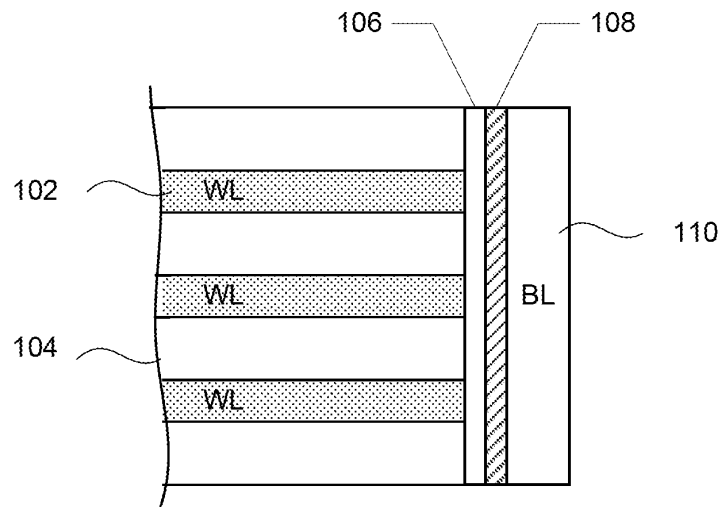


FIG. 1A

100B

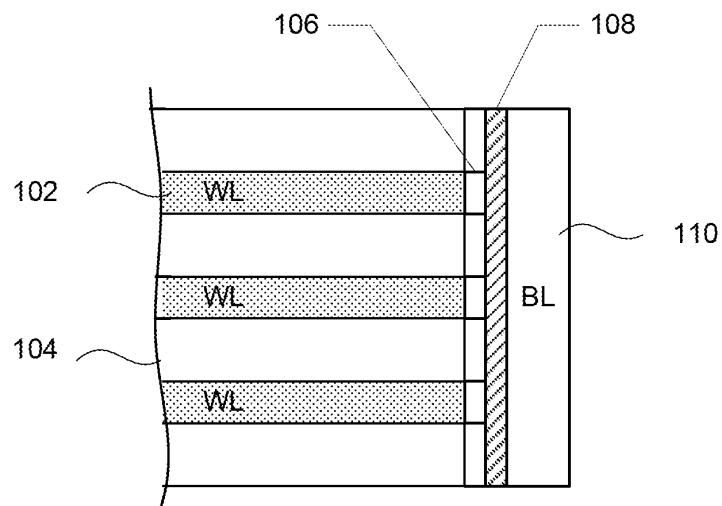


FIG. 1B

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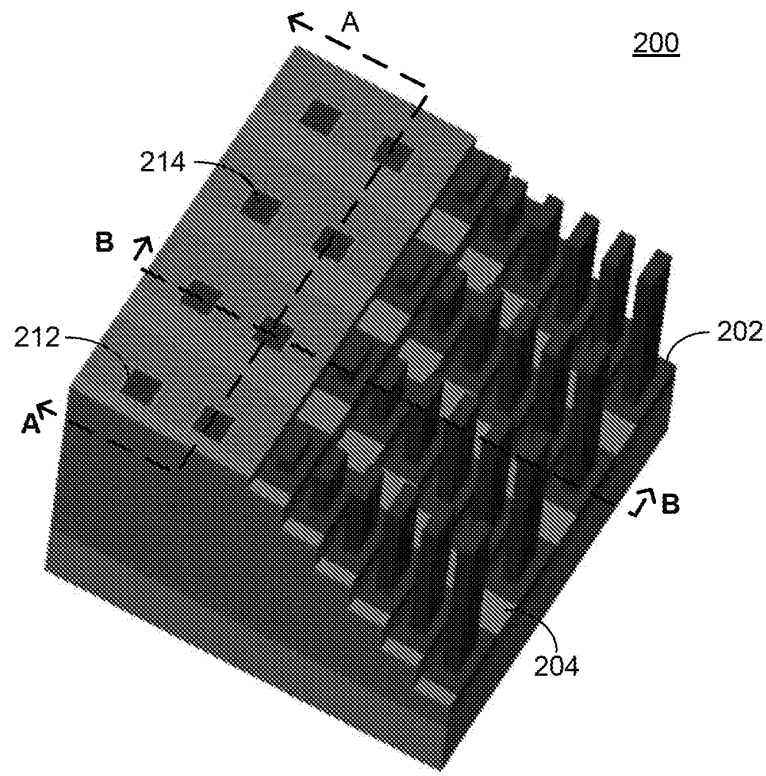


FIG. 2A

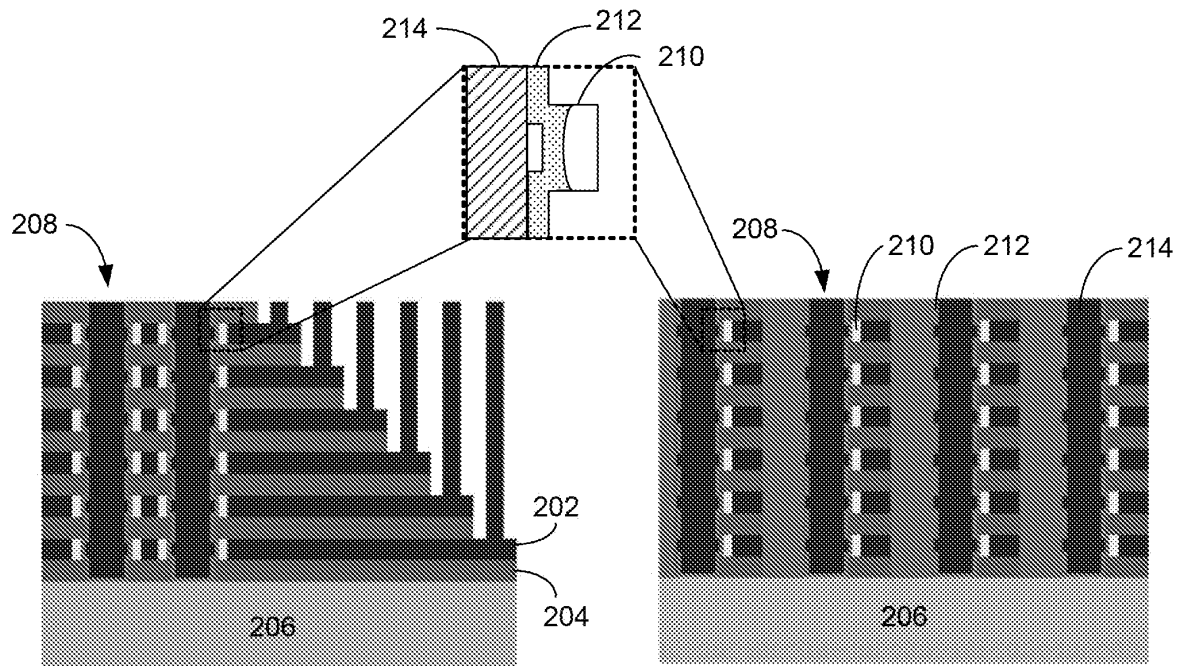


FIG. 2B

FIG. 2C

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300

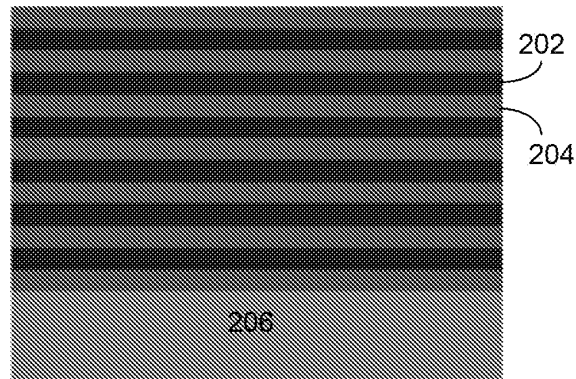


FIG. 3

400

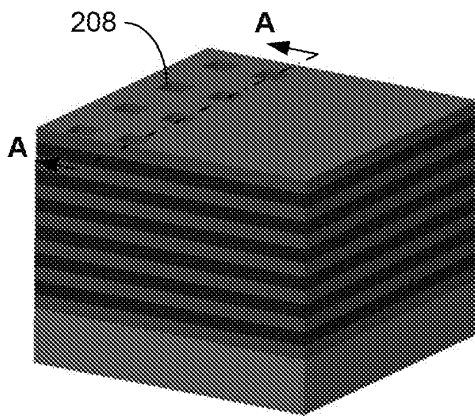


FIG. 4A

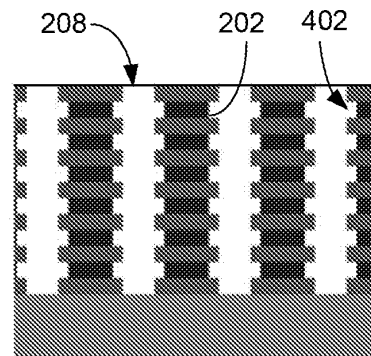


FIG. 4B

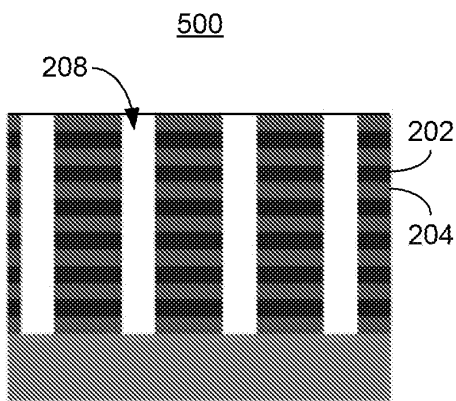


FIG. 5

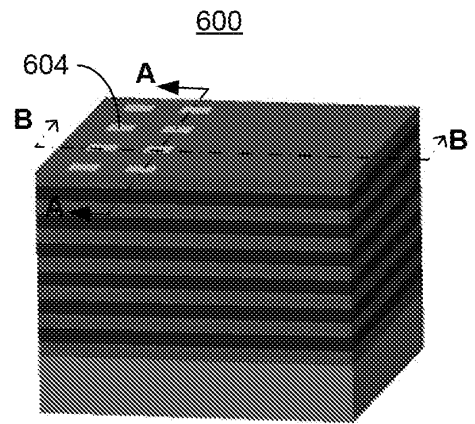


FIG. 6A

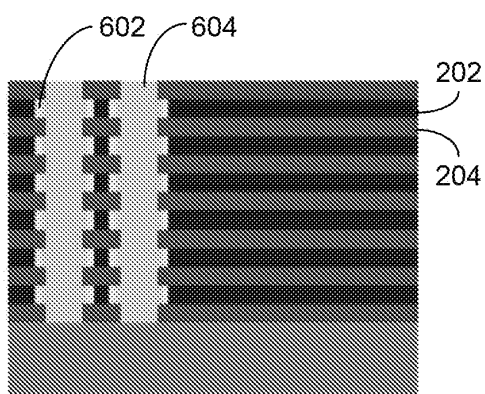


FIG. 6B

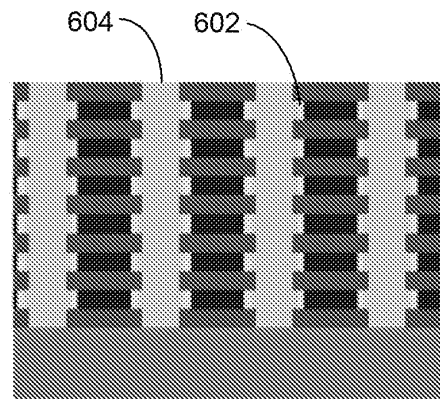
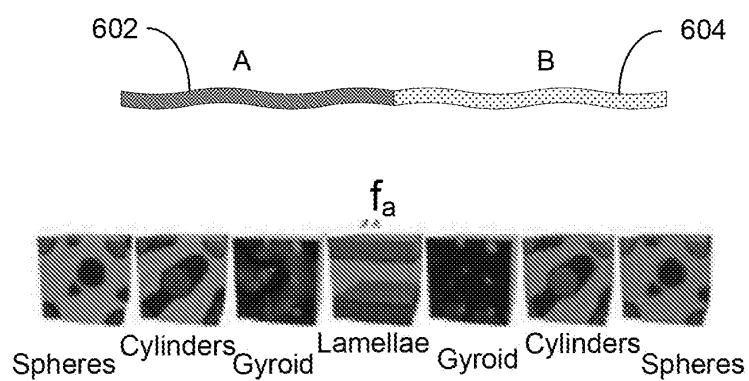
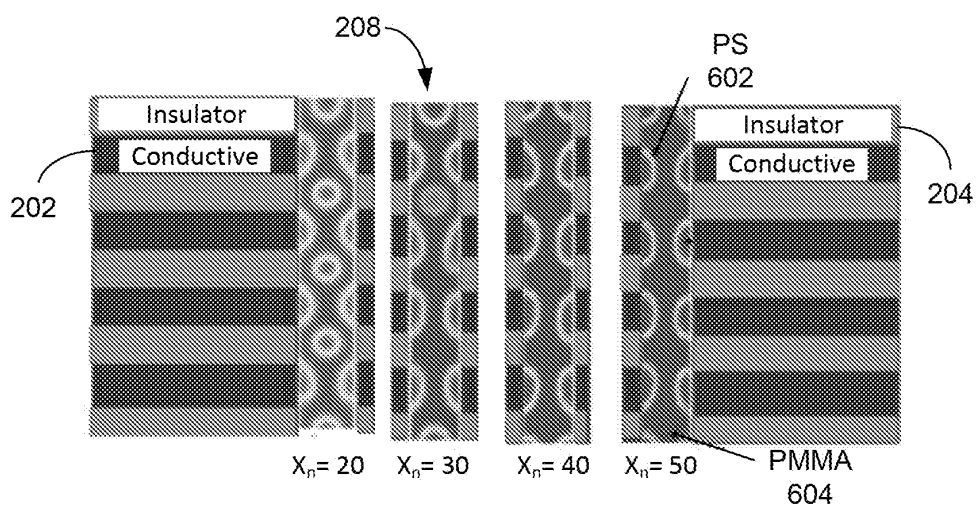


FIG. 6C

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**FIG. 7A****FIG. 7B**

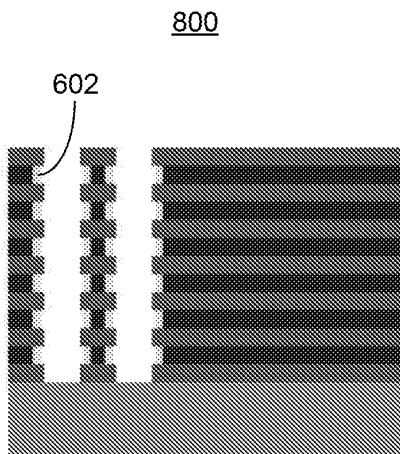


FIG. 8A

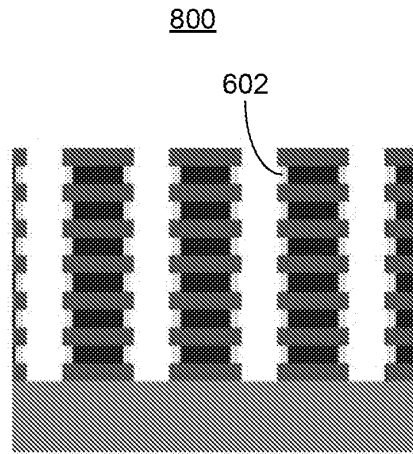


FIG. 8B

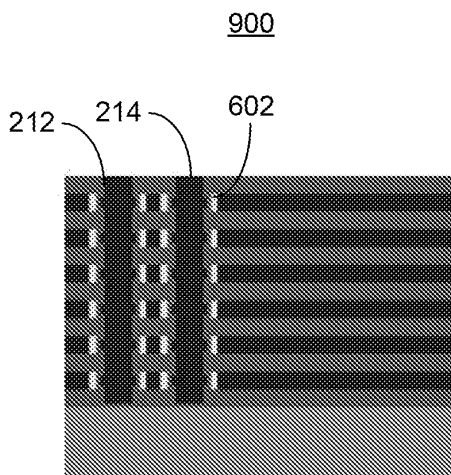


FIG. 9A

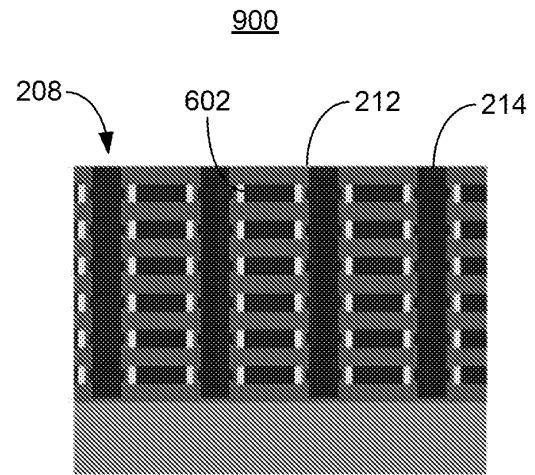


FIG. 9B

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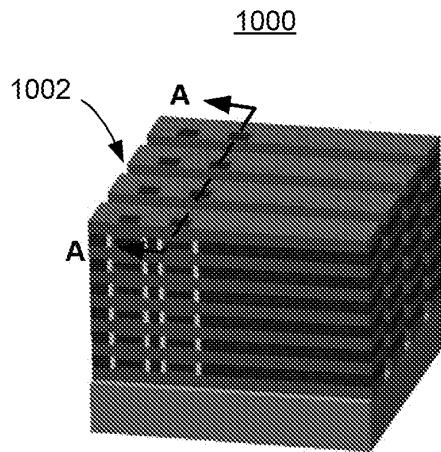


FIG. 10A

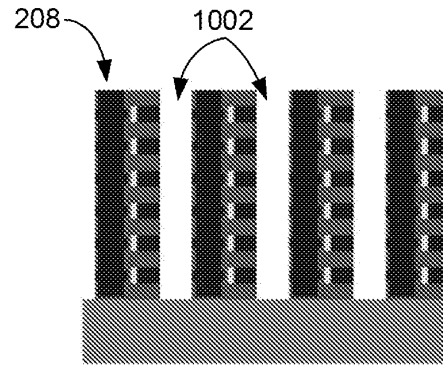


FIG. 10B

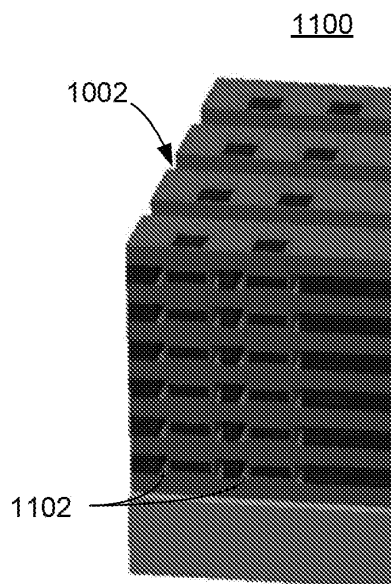


FIG. 11A

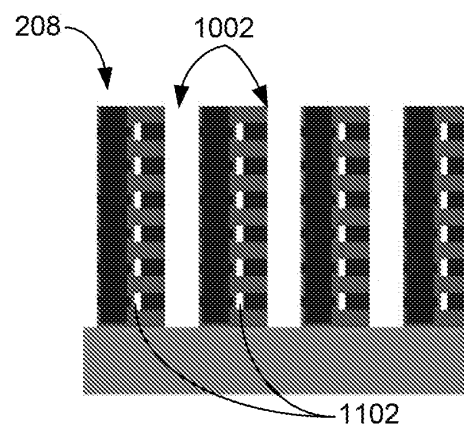


FIG. 11B

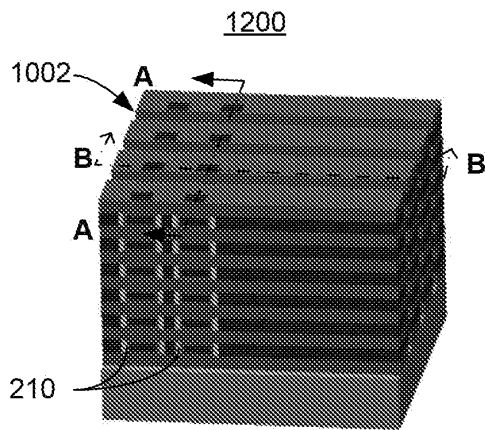


FIG. 12A

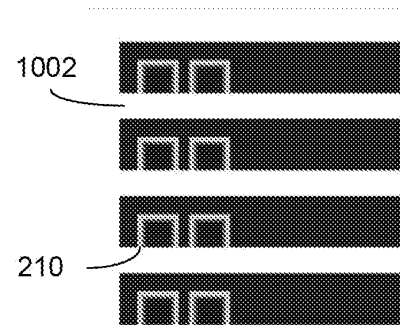


FIG. 12B

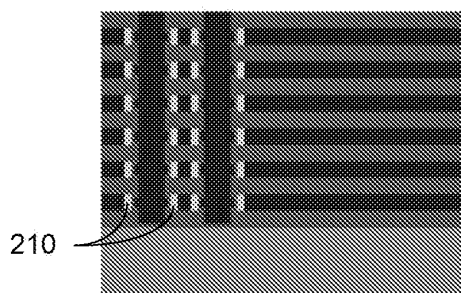


FIG. 12C

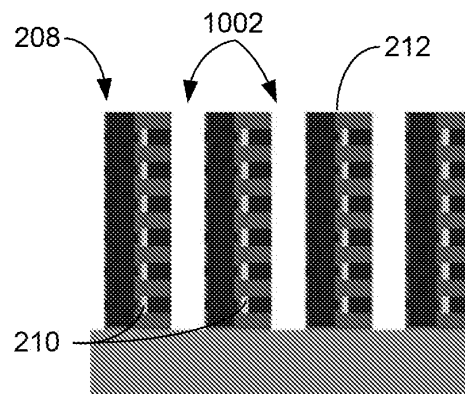


FIG. 12D

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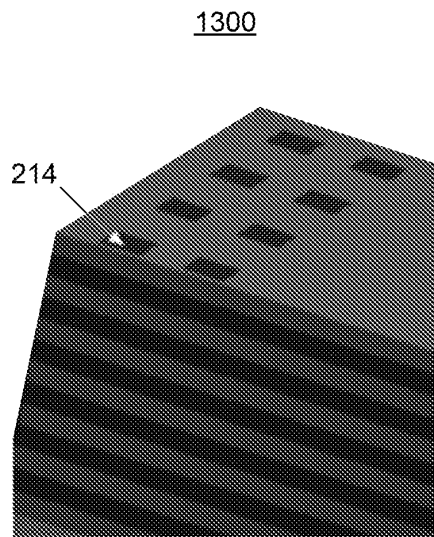


FIG. 13A

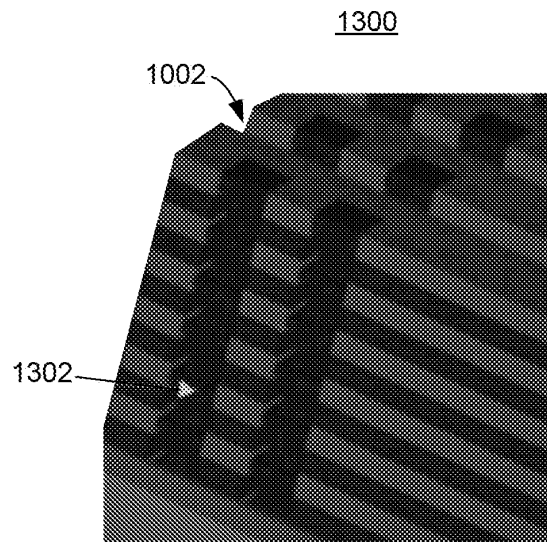


FIG. 13B

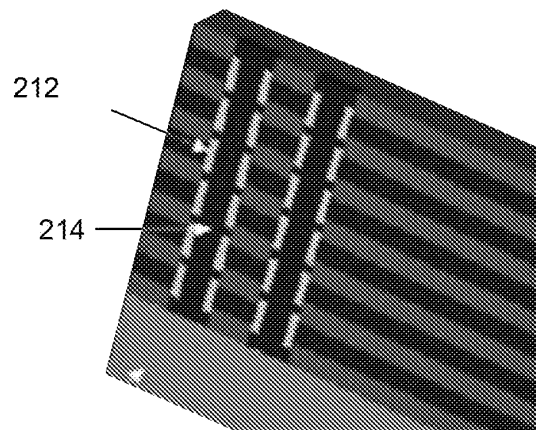
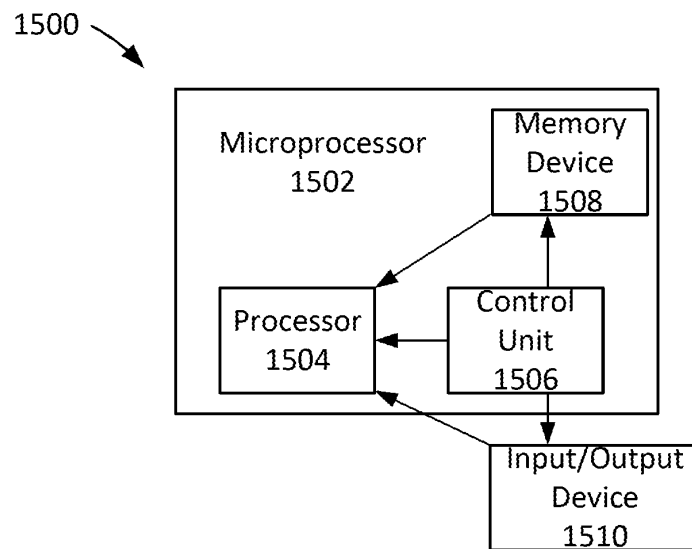
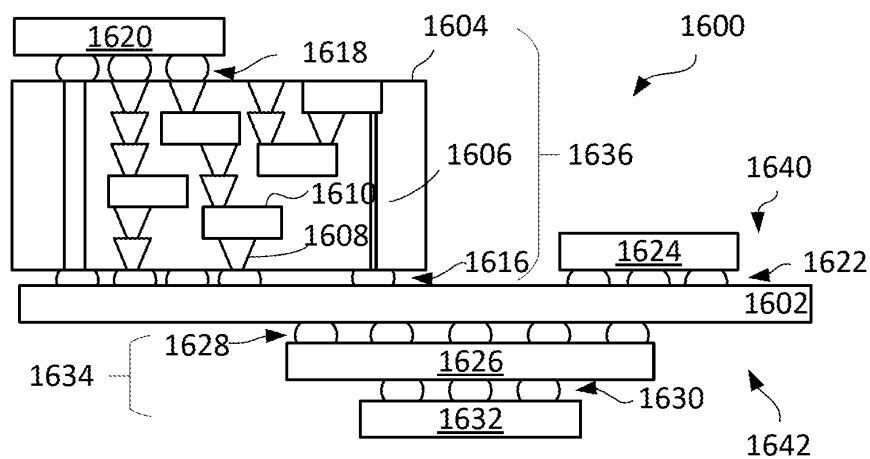


FIG. 13C

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**FIG. 15****FIG. 16**

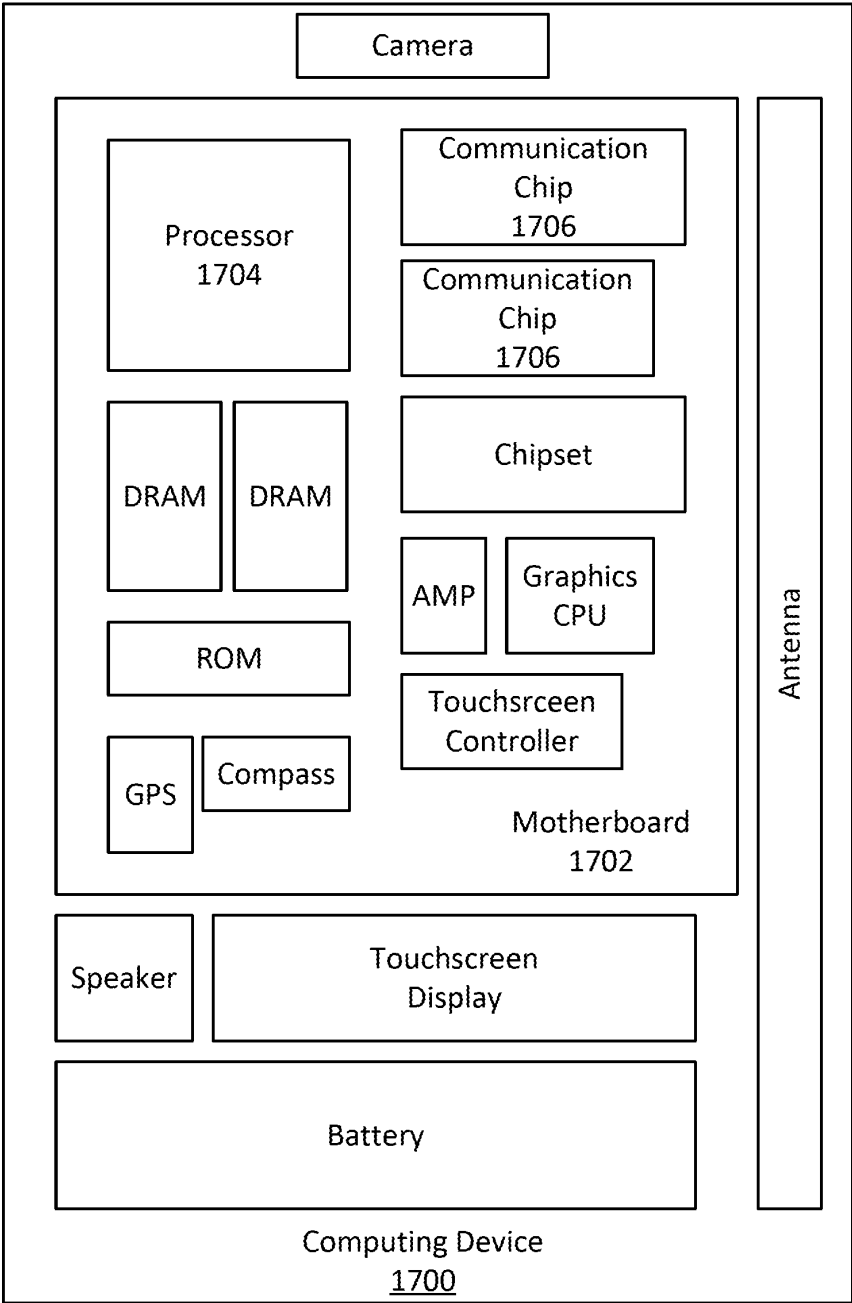


FIG. 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/053852

A. CLASSIFICATION OF SUBJECT MATTER H01L 45/00(2006.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H01L 45/00; H01L 21/768; H01L 21/8242; H01L 29/94; H01L 27/24; H01L 21/44		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & keywords: conductive layer, insulator, selector, etch pit, self-aligned, hemispherical, vertical, block copolymer, direct self-assembly (DSA), polystyrene (PS), polymethylmethacrylate (PMMA)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2017-0025476 A1 (HGST NETHERLANDS B. V.) 26 January 2017 See paragraphs [0009], [0030], [0037], [0041]; claims 1, 9; and figures 2C, 2G.	1-5
A		6-25
Y	US 9196530 B1 (INNOCENZO TORTORELLI et al.) 24 November 2015 See column 3, lines 14-31; claim 9; and figure 4.	1-5
A	US 2015-0028281 A1 (INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE) 29 January 2015 See paragraphs [0034]-[0035]; claim 1; and figures 5-6B.	1-25
A	US 2006-0199331 A1 (LINGYI A. ZHENG) 07 September 2006 See paragraphs [0040]-[0041]; claim 1; and figure 7.	1-25
A	US 2006-0249777 A1 (LEONARD FORBES et al.) 09 November 2006 See paragraphs [0017]-[0020]; claim 1; and figure 1.	1-25
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 08 March 2018 (08.03.2018)		Date of mailing of the international search report 08 March 2018 (08.03.2018)
Name and mailing address of the ISA/KR International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer KIM, Seong Woo Telephone No. +82-42-481-3348

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2017/053852

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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