

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: March 23, 2026

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00191
Patent 11,581,322

PATENT OWNER'S SUR-REPLY

TABLE OF CONTENTS

I.	Introduction.....	1
II.	Petitioner's Proposed Circular-TAC Modification Would Render Nishikawa Inoperable For Its Intended Purpose	2
A.	Circular TAC Results in Short-Circuits	2
1.	Dr. Campbell rebutted the Petition's proposed modification	2
2.	Petitioner's new theory contradicts the written description.....	3
3.	Petitioner's new modifications are flawed and it fails to show a motivation to combine or reasonable expectation of success	6
B.	Petitioner's additional arguments fail to show how circular TACs are a "suitable option" motivating the proposed modifications	10
C.	Petitioner's common-inventorship argument is wrong.....	13
D.	Circular TACs are not "unusually simple"	14
III.	Dummy Channels Would Not Have Been Obvious	15
A.	The ID was correct	15
1.	Edge defects	16
2.	Support is redundant	17
3.	Gate replacement process	19
4.	Petitioner's other arguments fail.....	20
5.	Petitioner improperly relies on a POSITA's knowledge to gap-fill for missing limitations.....	21
6.	Dr. Campbell's testimony	21

IV.	Petitioner's Ribbed TAC Arguments Fail	22
A.	The ID was correct and Petitioner fails to overcome the Board's concerns.....	22
B.	Petitioner improperly relies on a POSITA's knowledge to gap-fill missing limitations.....	25
V.	Petitioner's Equal-Diameter Arguments Fail	26
A.	Petitioner's reliance on figures to disclose relative proportions of peripheral contacts and TACs is wrong.....	26
B.	Petitioner fails to identify any primary or background references disclosing the claimed equal diameters or proportions.....	27
C.	Petitioner improperly relies on a POSITA's knowledge to supply missing limitations.....	29
VI.	Conclusion	29

TABLE OF AUTHORITIES**Page(s)****CASES**

<i>Arendi S.A.R.L. v. Apple Inc.</i> , 832 F.3d 1355 (Fed. Cir. 2016)	21
<i>Belden Inc. v. Berk-Tek LLC</i> , 805 F.3d 1064 (Fed. Cir. 2015)	29
<i>DSS Tech. Mgmt., Inc. v. Apple Inc.</i> , 885 F. 3d 1367 (Fed. Cir. 2018)	14, 21
<i>Idemitsu Kosan Co. v. SFC Co.</i> , 870 F.3d 1376 (Fed. Cir. 2017)	8
<i>In re Entresto</i> , 125 F.4th 1090 (Fed. Cir. 2025), <i>cert. denied sub nom.</i> <i>MSN Pharms., Inc. v. Novartis Pharms. Corp.</i> , No. 25-225, 2025 WL 3620413 (U.S. Dec. 15, 2025).....	17
<i>Intel Corp. v. PACT XPP Schweiz AG</i> , 61 F.4th 1373 (Fed. Cir. 2023)	<i>passim</i>
<i>Koninklijke Philips N.V. v. Google LLC</i> , 948 F.3d 1330 (Fed. Cir. 2020)	21
<i>KSR Int'l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	23
<i>Nystrom v. TREX Co.</i> , 424 F.3d 1136 (Fed. Cir. 2005), <i>aff'd</i> , 200 F. App'x 987 (Fed. Cir. 2006)	26, 28
<i>PAR Pharm., Inc. v. TWI Pharms., Inc.</i> , 773 F.3d 1186 (Fed. Cir. 2014), <i>aff'd</i> , 624 F. App'x 756 (Fed. Cir. 2015)	24
<i>Pioneer Pet Prods., LLC v. Oil-Dri Corp. of Am.</i> , IPR2022-00691, 2023 WL 5955777 (P.T.A.B. Sept. 12, 2023)	6

<i>Qualcomm Inc. v. Apple Inc.</i> , 24 F.4th 1367 (Fed. Cir. 2022), <i>rev’d</i> , 134 F.4th 1355 (Fed. Cir. 2025)	14
<i>Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.</i> , 97 F.4th 882 (Fed. Cir. 2024)	11, 17

REGULATIONS

37 C.F.R. § 1.84(p)(4).....	12
-----------------------------	----

EXHIBIT LIST

Ex.	Description
2001	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)
2002	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2003	Order Granting Stipulation to Extend Certain Deadlines Pursuant to Patent L.R. 4-2 and the Scheduling Order (ECF No. 141) Pursuant to Civil Local Rule 6-1(b), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 8, 2025), ECF No. 194
2004	Order Granting Motion to Stay Case Pending <i>Inter Partes</i> Review, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 14, 2025), ECF No. 243
2005	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending <i>Inter Partes</i> Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2006	Disclaimer in Patent Under 37 C.F.R. § 1.321(a)
2007	Declaration of Dr. Stephen A. Campbell ("Campbell")
2008	<i>Curriculum Vitae</i> of Dr. Stephen A. Campbell
2009	<i>Inside Solid State Drives (SSDs)</i> (Rino Micheloni et al. eds., 2d ed. 2018)

Ex.	Description
2010– 2017	RESERVED
2018	Order Granting Motion to Consolidate, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Aug. 21, 2024), ECF No. 106
2019	RESERVED
2020	U.S. Patent Application Publication No. 2007/0358593 A1, Published Dec. 14, 2017
2021	Declaration of Stephen Campbell in Support of Patent Owner's Response ("Campbell2")
2022	Transcript of the Deposition of Jack C. Lee, Ph.D., taken July 30, 2025, <i>Micron Tech., Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00034 ("Lee '254 Dep.")
2023	Harmeet Singh, <i>Overcoming Challenges in 3D NAND Volume Manufacturing</i> , 60 Solid State Technology 18 (July 2017)
2024	Thermo Fisher Scientific, <i>White Paper: The Challenge of Measuring Buried Critical Dimensions in High-Aspect-Ratio Structures: How Busy Fab Process Owners Can Reduce Time-to-Data in 3D NAND Metrology</i> , https://assets.thermofisher.com/TFS-Assets/MSD/Reference-Materials/helios-5-pxl-3d-nand-whitepaper-wp0025.pdf (last visited Aug. 5, 2025)
2025	Mark Lapedus, <i>What's Next for NAND?: Vendors Pin Hopes on 3D Memory, Raising Specter of 2D NAND Shortages; Other Memory Types Add to Uncertainty</i> , Semiconductor Eng'g (May 19, 2016), https://web.archive.org/web/20161127122539/https://semiengineering.com/whats-next-for-nand/ (last visited Aug. 15, 2025)

Ex.	Description
2026	Mark Lapedus, <i>3D NAND Flash Wars Begin: Market Overcrowding, More Efficient Manufacturing, and Growing List of Scaling Issues Create a Challenging Competitive Landscape</i> , Semiconductor Eng'g (Aug. 20, 2018), https://web.archive.org/web/20180822030129/https://semiengineering.com/3d-nand-flash-wars-begin/ (last visited Aug. 15, 2025)
2027	Mark Shirey & Janay Camp, <i>Digging Deep Into High Aspect Ratio Process Control for Memory Technology</i> , Semiconductor Eng'g (Oct. 18, 2018), https://web.archive.org/web/20250621011306/https://semiengineering.com/digging-deep-into-high-aspect-ratio-process-control-for-memory-technology/ (last visited Aug. 15, 2025)
2028	Mark Lapedus, <i>3D NAND Metrology Challenges Growing: Rising Costs and Gaps in Equipment Emerge as Technology Scales; New Tools Under Development</i> , Semiconductor Eng'g (Apr. 9, 2019), https://semiengineering.com/3d-nand-metrology-challenges-growing/
2029	Mark Lapedus, <i>3D NAND's Vertical Scaling Race: More Competition, Business Uncertainty, and Much More Difficult Manufacturing Processes</i> , Semiconductor Eng'g (Dec. 17, 2020), https://semiengineering.com/3d-nands-vertical-scaling-race/
2030	Yongsik Yu, <i>Tech Brief: Memory "Grows Up" with 3D NAND</i> , Lam Rsch. Newsroom (Apr. 11, 2016), https://newsroom.lamresearch.com/Tech-Brief-Memory-Grows-Up-with-3D-NAND (last visited Aug. 5, 2025)
2031	Mark Lapedus, <i>NAND Market Hits Speed Bump: Transition from Planar to 3D NAND is Harder and More Time-Consuming Than Expected</i> , Semiconductor Eng'g (June 21, 2017), https://web.archive.org/web/20180625071314/https://semiengineering.com/nand-market-hits-speed-bump/ (last visited Aug. 15, 2025)

Ex.	Description
2032	Mark Lapedus, <i>3D NAND Race Faces Huge Tech and Cost Challenges: Shakeout Looms as Vendors Struggle to Find Ways to Add More Layers and Increase Density</i> , Semiconductor Eng'g (May 23, 2019), https://web.archive.org/web/20190619034609/https://semiengineering.com/3d-nand-race-faces-huge-tech-and-cost-challenges/ (last visited Aug. 15, 2025)
2033	Mark Lapedus, <i>How to Make 3D NAND: Foundries Progress With Complex Combination of High-Aspect Ratio Etch, Metal Deposition and String Stacking</i> , Semiconductor Eng'g (May 23, 2016), https://semiengineering.com/how-to-make-3d-nand/ (last visited Aug. 15, 2025)
2034	Timothy Yang, <i>Creating Higher Density 3D NAND Structures: Identify the Manufacturing Issues Associated With Increased 3D NAND Density to Make the Best Tradeoffs and Avoid Structural Collapse</i> , Semiconductor Eng'g (Feb. 21, 2019), https://semiengineering.com/creating-higher-density-3d-nand-structures/ (last visited Aug. 15, 2025)
2035	Seong Jae Yoo et al., <i>Highly Selective Etching of SiN_x Over SiO₂ Using ClF₃/Cl₂ Remote Plasma</i> , 34 Nanotechnology 465302 (2023)
2036	Entegris, <i>White Paper: Considerations for Improving 3D NAND Performance, Reliability, and Yield</i> , https://www.entegris.com/content/dam/web/resources/white-papers/whitepaper-improving-3d-nand-performance-8443.pdf (last visited Aug. 5, 2025)
2037	RESERVED
2038	Transcript of the Deposition of Jack C. Lee, Ph.D., taken October 23, 2025, <i>Micron Tech. Inc. v. Yangtze Memory Techs. Co.</i> , IPR2025-00191
2039	Declaration of Robert B. Duntelman In Support of Patent Owner's Unopposed Motion for <i>Pro Hac Vice</i> Admission Under 37 C.F.R. § 42.10(c)

Ex.	Description
2040	Declaration of Robert B. Dunteman In Response To Petitioner's Objections to Evidence, with Appendices A-W [<i>served only</i>]

I. Introduction

The patentability of the challenged claims should be confirmed.

Petitioner's circular-TAC modification to Nishikawa would render Nishikawa's device inoperable. Petitioner advances new implementation theories absent from the Petition but still no motivation or expected success to change Nishikawa's TAC shape. Nor does Petitioner show circular TACs were suitable to solve a known problem in Nishikawa.

The Institution Decision ("ID") properly determined Petitioner failed to identify any improvement or benefit from adding dummy channels to Nishikawa. Petitioner's new arguments regarding edge defects, structural support, and gate replacement fail to overcome the Board's concerns that Nishikawa already disclosed support structures; processing tradeoffs would outweigh additional support.

Likewise, Petitioner's recasting of its ribbed TAC arguments as "short-circuit protection" fails to overcome the Board's concerns. Nor does Petitioner's "unintentional recess" theory show a POSITA would desire the combination.

Petitioner still improperly relies on figures to establish relative proportions of peripheral contacts and TACs—identifying no reference disclosing the claimed equal diameters, instead extrapolating from irrelevant disclosures.

In each case, Petitioner relies on legally insufficient general knowledge for missing limitations and motivations.

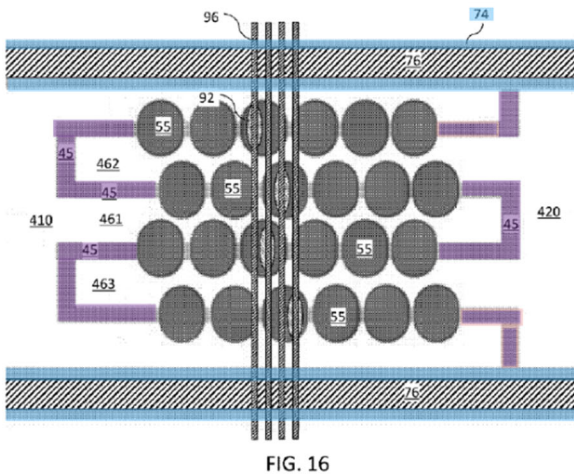
II. Petitioner's Proposed Circular-TAC Modification Would Render Nishikawa Inoperable For Its Intended Purpose

The Petition failed to show successful implementation of a circular TAC in Nishikawa. Wherever a circular TAC is placed a short circuit would result. POR 10-29. The Board should reject Petitioner's untimely, unsupported Reply arguments that fail to establish a motivation to combine or reasonable expectation of success.

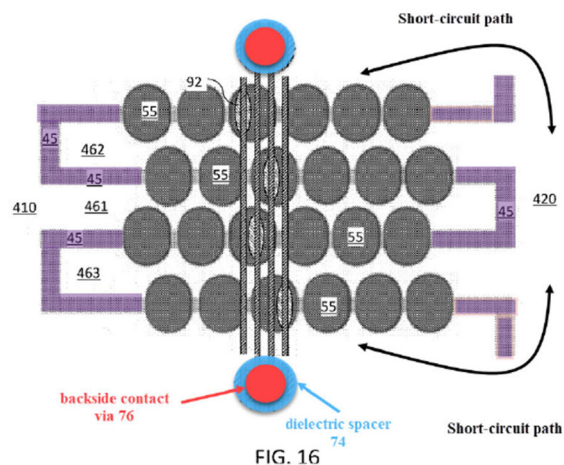
A. Circular TAC Results in Short-Circuits

1. Dr. Campbell rebutted the Petition's proposed modification

The Petition "*replac[es]* the backside contact via [i.e., trench] with a cylindrical TAC."¹ Pet.43, 50-51. This *replacement* would lack electrical separation between word lines and be inoperable:



Nishikawa Fig. 16 (annotated)



Nishikawa Fig. 16 (modified)

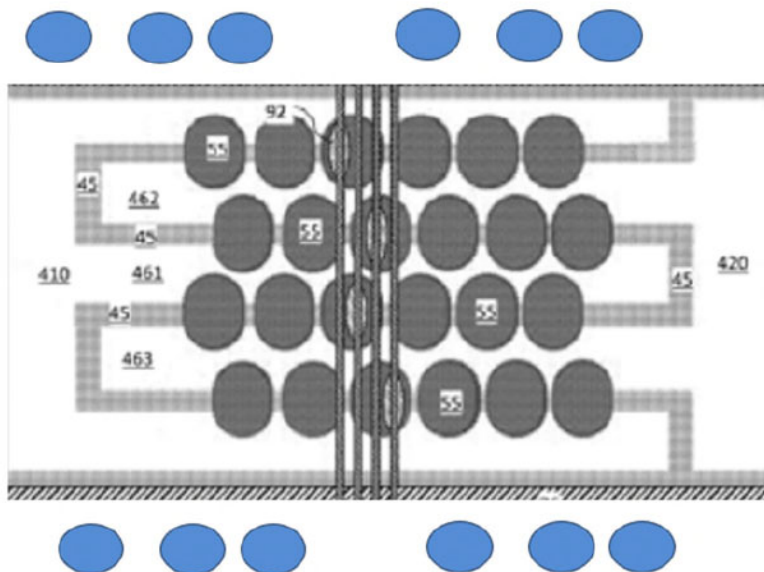
Campbell2 (Ex.2021) ¶¶49-59.

¹ All emphases added and citations omitted unless otherwise stated.

Petitioner criticizes Dr. Campbell's illustration as "not found in the Petition" and one that no POSITA would implement. Reply 2. Dr. Campbell's illustration appropriately showed one of many reasons why the *Petition* (which had no illustration) was wrong. Dr. Campbell testified further that a POSITA would not replace Nishikawa's trench *regardless* of circular TAC placement. Ex.1106, 72:21-73:4 ("There's always going to be a short circuit path."), 74:18-75:8.

2. Petitioner's new theory contradicts the written description

Petitioner's Reply presents a *new* theory based on a *new* modification of Nishikawa that still contradicts its specification. According to Petitioner, a POSITA would "implement the circular TACs with the separator [45] providing the isolation," where the dielectric separators [45] *include* "the [horizontal] top and bottom portions" because they "laterally separate gate sets." Reply 3, 5.



Id. 4 (modified Fig.16).

First, what Petitioner calls the horizontal “top and bottom portions” of the dielectric separators 45 are *not* part of 45, but are defined as “dielectric separators 74” associated with the trenches and backside contact structures 76. Nishikawa (Ex.1005) 6:57-59 (“A dielectric spacer 74 can be employed to provide electrical isolation for the backside contact via structure 76.”); Nishikawa123 (Ex.1046), 25:36-44 (“backside trenches [are] filled with the insulating spacers 74 and the backside contact structures 76”). Annotated Fig.16 below is illustrative:

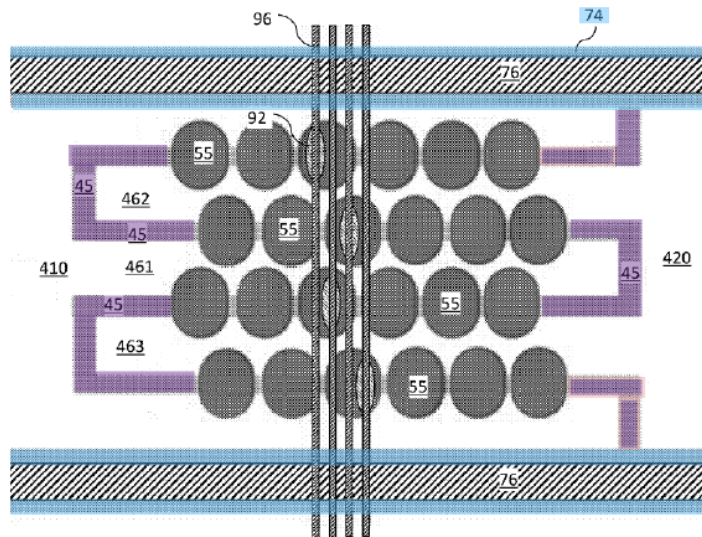


FIG. 16

Nishikawa Fig. 16 (annotated)

Second, Petitioner argues that because separators 45 “laterally separate the gate sets” they include the horizontal top and bottom portions (i.e., dielectric separators 74). But Nishikawa separators 45 laterally separate the “control gates,”

not “*gate sets*,” a Petitioner-coined term.² Nishikawa teaches that “separator dielectric structures 45 extend through the stack, contact portions of outer sidewalls of the memory stack structures 55, and laterally separate *the control gate electrodes 46*,” where the control gate electrodes are 461-463 in Figs.15-17.³ Nishikawa 14:60-15:42, 17:14-17. Thus, separators 45 laterally separate individual *control gate electrodes*, not gate-electrode “sets,” and do not include dielectric trench 74.

Patent Owner (“PO”) does not attack a strawman, as Petitioner argues. Reply 5. Petitioner admits word lines 410 and 420 must be electrically separated but failed to show Nishikawa accomplishing this using a circular TAC. *Id.* Dr. Campbell confirmed a POSITA would not, and *could* not, achieve necessary isolation using circular TACs in Nishikawa. Campbell2 ¶¶49-64; Ex.1106, 71:21-73:4.

² The term “gate sets” is absent from Nishikawa and Nishikawa123, but apparently refers to control gate electrodes 461-463 (collectively), located between two trench TACs.

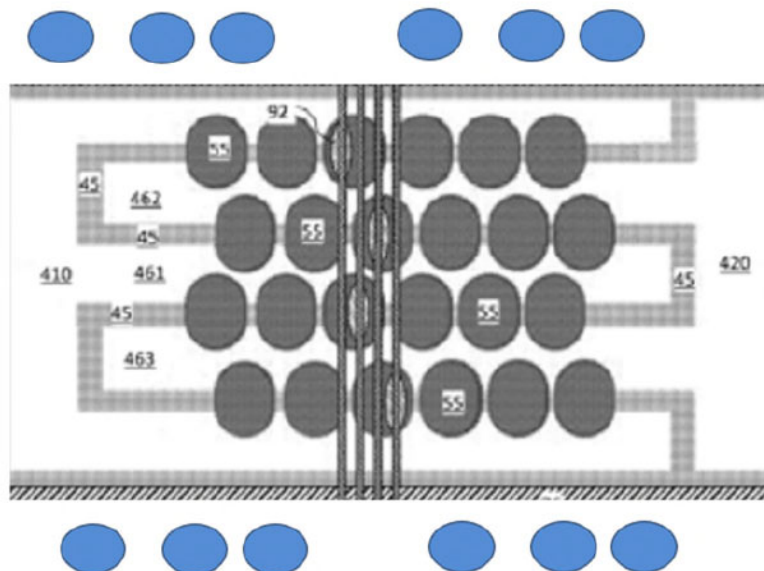
³ Control gate electrodes 461-463 are the prongs extending from word line regions 410 and 420 in Fig.16. Nishikawa 15:31-42; Nishikawa123, 25:44-48.

3. Petitioner's new modifications are flawed and it fails to show a motivation to combine or reasonable expectation of success

Petitioner advances at least three new purported examples of how a circular TAC would apply in Nishikawa. POR 23 n.2; Reply 3-4 (recharacterizing modified figure), 6-7 (new designs). The Board should reject these as untimely. *Pioneer Pet Prods., LLC v. Oil-Dri Corp. of Am.*, IPR2022-00691, 2023 WL 5955777, *12 (P.T.A.B. Sept. 12, 2023) (acknowledging “prejudice to [PO if] we consider the new arguments and evidence in Petitioner’s Reply”). Regardless, Petitioner’s designs fail.

a. Petitioner's first modification fails

Petitioner shows multiple, circular TACs “with the separator providing isolation” between word lines:



Reply 3-4. This design adds back a horizontal trench on top and bottom, which the Petition had *previously replaced* in its entirety with circular TACs. Pet.43, 50-51;

Ex.1106, 82:14-17 (“Q. In the proposed modification, the trench is removed, the trench is no longer there, there’s not a trench, correct? A. Correct.”). Petitioner’s “replacement” theory is flawed as explained in the POR at 11-27. Additionally, the top and bottom horizontal separators providing electrical isolation are *within*, and thus integral to, the trench. Removing the trench thus necessarily removes the top and bottom horizontal separators even if they were part of separators 45, as Petitioner contends.

This new modification of *retaining* a partial trench and *adding* circular TACs is further flawed because it has densely packed TACs, which Dr. Campbell explained would be problematic. Campbell2 ¶¶61-62. Petitioner concedes that the memory device “may include multiple instances” of the Fig.16 block and, as shown, the circular TACs in Petitioner’s redesign are within a neighboring memory block or a separately created area between two blocks. Reply 4 & n.2. These densely packed TACs would increase the trench’s lateral thickness, reducing storage density and discouraging a POSITA from making this change. Campbell2 ¶¶102, 104. Finally, deviating from Nishikawa and Nishikawa123, bit lines 96 in Petitioner’s modified figure do not cross over the TACs, which Petitioner fails to consider or provide a motivation for.⁴

⁴ The same is true for Petitioner’s other new implementations.

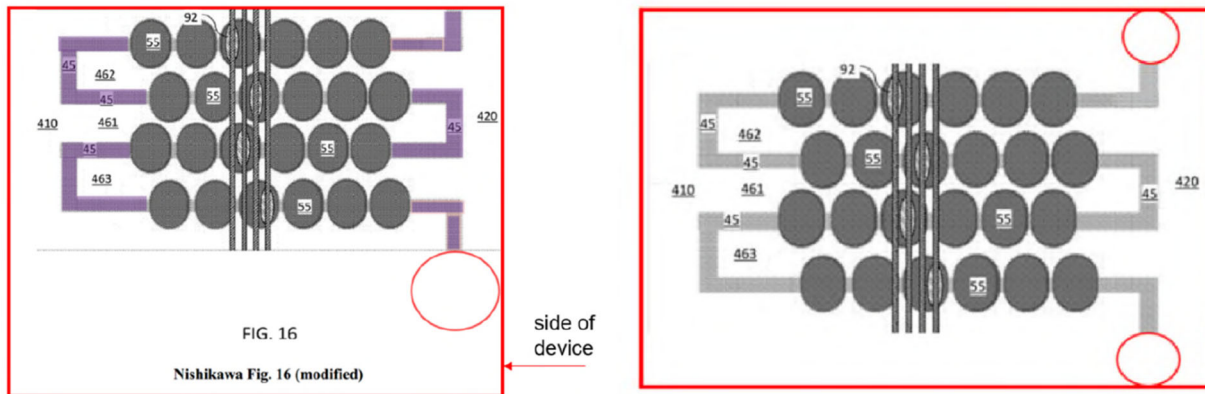
Notably, Petitioner fails to explain why a POSITA creating a trench for the horizontal “top and bottom portions” (i.e., dielectric spacers 74) would not place TACs *within* the trench, as Nishikawa teaches, but instead create *separate* holes for circular TACs, which would require more footprint and manufacturing complexity.

b. Petitioner's two new designs excluding horizontal separators are flawed

Petitioner argues, unsupported and incorrectly, that the POR's example placing a circular TAC at the end of separator 45 makes apparent “numerous operable implementations” of circular TACs. Reply 6-7.

Each of Petitioner's new “operable implementations” depends on drawing a device edge to touch the circular TAC:⁵

⁵ Petitioner misinterprets *Idemitsu Kosan Co. v. SFC Co.*, which allowed the petitioner to raise counter-arguments where “[PO] is the party that first raised [the] issue.” 870 F.3d 1376, 1380-81 (Fed. Cir. 2017). Here, *Petitioner* first argued Nishikawa could be modified to a circular TAC. Pet.39-51.



Reply 6-7. But nowhere does the record identify where the device edge is located and how large the resulting circular footprint must be. *Id.* Petitioner arbitrarily draws a line purporting to be the device's side (*id.* 6; Lee2 (Ex.1105) ¶13) and argues for another implementation that the circular TACs span the same width as the trenches.⁶ Reply 7. As Dr. Campbell testified, there was insufficient information to identify the true device edge. Ex.1106, 78:5-25, 83:6-84:3.

Petitioner also argues placing a circular TAC at the separator's end would not increase its footprint, ignoring Dr. Campbell's complete testimony and basic geometry. *Id.* 77:4-16 ("The TAC's diameter would have to be large enough to contact the side of the device to maintain isolation. That is absolutely true. And that

⁶ Petitioner's arbitrary device edge either adds insulating structure to Nishikawa, reducing memory density, or replaces the trench with insulating structure but creates no additional space. Neither implementation solves a problem in Nishikawa. *Infra* §II.B.

would require a larger footprint than a regular tranche. Also true.”). Even if a circular TAC did not increase TAC footprint, Dr. Campbell stated that “there is no place on the array that you could place that [circular TAC] and still have isolation between 410 and 420,” and this “[was] just another example of where it could be placed, and you’d still have short circuits.” *Id.* 74:18-75:8. Thus, Nishikawa123’s circular TAC disclosure creates an inoperable device when applied to Nishikawa’s Fig.16 architecture. POR 11-27.

Petitioner also provides no motivation for this modification, and Dr. Campbell testified there is none. Ex.1106, 79:2-19.

B. Petitioner’s additional arguments fail to show how circular TACs are a “suitable option” motivating the proposed modifications

As described previously (§II.A), Petitioner’s proposed placement of circular TACs in Nishikawa is not suitable. Likewise, Petitioner’s additional arguments fail to show a circular TAC was functionally suitable in Nishikawa and would motivate a POSITA to adopt it.

First, Petitioner argues that “similarities in architecture” would motivate a POSITA to apply Nishikawa123’s circular TAC to Nishikawa. Reply 7-8. Petitioner also relies on prior art disclosing circular contacts to argue that replacing a backside contact via with a cylindrical TAC was a “known technique” and “suitable option” for Nishikawa. Pet.43-51 (citing *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023)). But Petitioner identifies no problem *with Nishikawa*

that would motivate a POSITA to change its TAC to a circular geometry. *Intel*, 61 F.4th at 1380; POR 11, 24-27. That circular contact openings were known is insufficient. *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 887-88 (Fed. Cir. 2024). Nor does Petitioner show why its purported “improvements” would outweigh the complexity and increased short circuit likelihood from a circular TAC in Nishikawa’s design. Campbell2 ¶¶49-76.

Next, Petitioner mischaracterizes PO’s position by focusing on distinctions, or lack thereof, between embodiments of Nishikawa123 Figs.14A-C and 17. Reply 8-10. Without even referencing Figs.14A-C, the POR simply explained that Nishikawa123’s disclosure of openings 79 having “any suitable shape” *does not apply* to Fig.17’s embodiment. POR 24-27. That Nishikawa123 does not identify any circular TACs outside of Figs.14A-C’s description and that Fig.17’s description never references Figs.14A-C, only supports PO’s position. Petitioner also argues Fig.17 “describ[es] the view under Figures 14’s top dielectric layers (80),” Reply 9-10, but Figs.14B-D *already* provide a top-down view of Fig.14A showing what underlies dielectric layer 80.

Discussing Figs.14A-D, Nishikawa123 (22:38-39) identifies three possible shapes for openings 79: “circular, rectangular or elongated trench shape.” Nishikawa123 specifies that different shapes for opening 79 comprise different embodiments. *Id.* 22:39-41. Fig.17’s embodiment, like Fig.16 of Nishikawa, is

compatible with a “trench” shape and thus incompatible with Nishikawa123's circular opening embodiment.

For example, Fig.17's separated word lines 46A/B require electrical isolation to preserve the dual-cell configuration. A POSITA would have understood that a trench-shaped backside contact was necessary to achieve this separation and the circular opening described in Figs.14A-D embodiments of Nishikawa123 was incompatible with Fig.17.⁷ Campbell2 ¶74; Ex.1106, 73:22-75:8.

Further, the specification supports that circular TACs are not “optional” in Fig.17's architecture, as Petitioner contends. Reply 10. The language Petitioner relies on to argue trenches are optional modifies the *presence*, not shape, of backside trenches for certain purposes. Nishikawa123, 27:59-28:3 (distributing access openings “eliminates the need to employ the *optional backside trenches* for replacement of the sacrificial material layers” and “[i]f the backside trenches are *present*,” more rows of openings may be formed than if they were employed for gate replacement). Further, Fig.17 specifies backside contact via structures that “laterally extend[] along the first horizontal direction hd1” and “laterally separate two sets of

⁷ Figs.14B-D *do not* identify physically disjointed portions (46A, 46B) central to Fig.17, undermining Petitioner's argument that “common numerals” confirm these are the same structures. Reply 10 (citing 37 C.F.R. § 1.84(p)(4)).

interdigitated electrically conductive portions (46A, 46B)”—something the circular TAC of Figs.14A-C cannot do. *Id.* 26:43-49.

The Petition and Reply failed to propose a single circular TAC application in Nishikawa or Nishikawa123 that preserves isolation of the dual-cell configuration. POR 26-27. Thus, Petitioner failed to show it was “suitable.” Reply 2-7, 11.

C. Petitioner's common-inventorship argument is wrong

Petitioner argues that Nishikawa and Nishikawa123 describe the same device because it is “common for an author of a paper...to write a follow-up paper...that addresses other aspects that weren't addressed in the first paper.” Reply 10. But Petitioner does not explain how or why that logic applies to disparate patent filings, which are not academic papers. That Nishikawa and Nishikawa123 share inventors and were filed close in time supports the opposite—if circular TACs were an obvious design choice for Nishikawa's structure, Nishikawa would have said so.

Regardless, obviousness is determined from the perspective of a POSITA, not the inventor. ID 16. A POSITA would have understood that two patents with unique specifications and overwhelmingly different figures are distinct devices, regardless of inventorship and filing dates. POR 27. That Nishikawa Fig.16 and Nishikawa123 Fig.17 have similar architecture does not mean Nishikawa123's specification can indiscriminately be applied to Nishikawa's device, especially for aspects (like circular TACs) that would render Nishikawa inoperable. Campbell2 ¶¶65-68. A

POSITA would not have been motivated to combine different embodiments from these different patents. POR 27-28; Campbell² ¶¶65-68.

D. Circular TACs are not “unusually simple”

Petitioner argues there is no missing limitation because “Nishikawa[123] and other references disclose a circular TAC.” Reply 11. But Petitioner’s primary reference, *Nishikawa*, misses this limitation and Petitioner gap-fills with general knowledge, making the September 2025 memo guidance relevant.⁸ POR 29-35. To rely on general knowledge, Petitioner must show the missing limitation is “unusually simple” and the technology is “particularly straightforward.”⁹ ID 14, 15; *DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F. 3d 1367, 1374 (Fed. Cir. 2018). Even if circular TACs were well-known and “suitable,” which PO disputes,¹⁰ Petitioner fails to show

⁸ For this reason, at least Ground 1 fails under *Qualcomm Inc. v. Apple Inc.*, as the “basis of [this] ground” is not contained in a patent or printed publication. 24 F.4th 1367, 1373-75 (Fed. Cir. 2022).

⁹ All of Petitioner’s grounds rely on general knowledge.

¹⁰ Petitioner is wrong that PO “does not contest” that circular TACs were “a well-known and suitable option for connecting structures through a memory stack.” Compare Reply 11, with POR 24-32.

they are “unusually simple” and that 3D NAND technology is straightforward. Dr. Campbell explained that changing TAC shape to a circle is complex, involves redesigning a lithography mask, and requires specialized and time-intensive processes compared to forming angular features. POR 34-35 (citing Campbell ¶¶73-76). Mask-making aside, it is harder to maintain a continuous etch rate when creating a circular TAC. *Id.* Also, a narrower hole, like a circular TAC, is a higher aspect ratio and risks more tapering than Nishikawa's trench-shaped TAC. *Id.* Petitioner's modifications also would be susceptible to bowing or twisting within the TAC, incomplete etching, variations between the top and bottom of the TAC, and other complications. *Id.* These points are unrebutted. Reply 12.

III. Dummy Channels Would Not Have Been Obvious

A. The ID was correct

Petitioner argues the Board applied an “overly restrictive” obviousness standard because dummy channels were “both a known and suitable option” for addressing edge-effect and stability problems. Reply 12-13 (citing *Intel*, 61 F.4th at 1381). Petitioner is wrong. The Board correctly found Petitioner failed to identify any improvement or benefit to Nishikawa (ID 18-20), which is consistent with *Intel* because Petitioner failed to establish dummy channels as a suitable alternative to solving a known problem in Nishikawa.

Petitioner's Reply advances new untimely arguments, each of which fails.

1. Edge defects

Petitioner relies on new references to argue edge effects are problematic for 3D memory devices generally, and Nishikawa specifically, and that dummy channels were used in the memory cell region. Reply 13-14 (citing Exs. 1108-1111).

The Board correctly found that Petitioner failed to identify an advantage to adding dummy cells, even though cells at the array edge may be unused due to process variations. ID 19. Petitioner relies on new evidence describing certain “edge effects” to argue dummy channels are a suitable remedy. But Petitioner fails to show that Nishikawa’s device suffers from the edge defects described in these references, or that dummy channels would be a suitable alternative to a problem in Nishikawa’s design. POR 42; Campbell2 ¶¶90-98.

Petitioner argues PO misstates Dr. Lee’s testimony about dummy channels being sacrificed. Not so. PO simply highlighted the ID’s observation of Dr. Lee’s testimony that the dummy region at the edge of the array is “later sacrificed in processing,” which fails to satisfy the claim limitation. POR 43; ID 19. The ID (at 19) also correctly rejected Petitioner’s argument that it was typical to “refrain from using” channels on the edge during operation, rendering them dummy channels. Reply 14. Finally, Petitioner incorrectly equates creation of dummy channels from existing, unused memory cells on the array edge with *forming dummy channels filled with dielectric through the memory stack*, as required by the claim language.

Petitioner does not dispute that Nishikawa has no room to extend the memory cell pattern to accommodate dummy channels.¹¹ POR 45. Instead, Petitioner argues there is “always” room for dummies on the edge because “dummies are created by not using them in operation.” Reply 14-15. Petitioner misses the point. As the Board noted, this still “does not show an advantage to adding dummy channels.” ID 19. Nor does it solve any problems in Nishikawa that would motivate its use. *Intel*, 61 F.4th at 1380. Additionally, this argument fails to address the density, performance, and cost disadvantages of replacing active channels with dummy channels. POR 45.

Finally, Petitioner argues it does not rely on hindsight because “employing such dummies on the edge of the array was common.” Reply 15. But “[t]he mere fact that these possible arrangements existed in the prior art *does not provide a reason* that a skilled artisan would have” used them in Nishikawa. *Virtek*, 97 F.4th at 887-88; *In re Entresto*, 125 F.4th 1090, 1100 (Fed. Cir. 2025).

2. Support is redundant

The ID correctly rejected Petitioner's arguments that a POSITA would have been motivated to add dummy channels to Nishikawa for structural support. ID 19-20. In Reply, Petitioner again argues that additional support would not be redundant

¹¹ Including to extend the memory cell pattern to “result in an overall more uniform feature pattern,” which the ID correctly rejected. POR 45; Pet.59-60; ID 19.

but fails to address the concerns underlying the ID's finding—namely, that Nishikawa already provides adequate support and Petitioner failed to show how additional support would be desirable given processing trade-offs. *Id.*

The ID correctly found that Nishikawa already disclosed structures for providing structural support, at least through its separator dielectric structures. *Id.* Petitioner now argues that Nishikawa's separators provide only “proximate support” and only “in a small portion” of Nishikawa's device. Reply 16-20. But this mischaracterizes Nishikawa's architecture. Nishikawa's separator dielectric structures are not limited to a “small portion” of the device; they extend *throughout* the entire memory stack to “laterally separate various portions of the alternative stack (32, 42)” and “provide structural support to the insulating layers 32 after formation of the interlayer cavities.” Nishikawa 8:33-35, 10:8-17. Notably, the insulating layers 32, before and after gate stack formation, extend into the contact region 300, shown in Fig.1. Thus, Nishikawa's separators already provide the support Petitioner cites as the reason to add dummy channels.

The ID also found that Petitioner failed to explain why adding dummy channels to Nishikawa, which already has adequate support, would be “viewed as desirable” given additional processing trade-offs. ID 19-20. Petitioner still fails to adequately address this deficiency. Rather, Petitioner's Reply introduces new references purportedly showing that placing dummy channels throughout the device

and into the contact region was conventional and suitable. Reply 16-22. But the ID's concern was not whether spreading out dummy channels was "conventional" or "suitable" to provide support throughout the device. *Id.* 17. Petitioner's references fail to show why additional support was needed, or that adding additional support structures would outweigh trade-offs from additional processing in Nishikawa. ID 19-20. Petitioner asserts, unsupported, that Nishikawa's device "would benefit from support throughout its device just like these references," and that there is "no serious tradeoff" regarding additional support structures. Reply 20-23; POR 46-50. But Petitioner is wrong. *See* §§III.A.1-4.

3. Gate replacement process

Petitioner newly argues that dummy channels can "improve the gate replacement process" by introducing the etchant and metal during gate replacement. Reply 22. Petitioner suggests that "dummy holes" (Petitioner's term) are the same as Nishikawa's "memory openings" and Nishikawa123's "access openings" or "dielectric pillars." *Id.* This argument is not in the Petition.¹² Regardless, neither Petitioner nor Dr. Lee points to any reference, including Nishikawa and Nishikawa123, identifying dummy channels used for gate replacement, much less

¹² Petitioner's Reply cites to discussion of claim 1, not dummy holes.

using Petitioner's terms of "dummy holes," "dummy channel holes," or "dummy openings." Lee2 ¶¶38-39.

Petitioner relatedly argues that Nishikawa123 "includes both [dummy channels and a separator]" (Reply 22), but Petitioner relies on references to "access openings." *Id.* Nowhere does Nishikawa123 disclose dummy channels.

4. Petitioner's other arguments fail

Petitioner argues adding dummy channels to Nishikawa would have been obvious, despite impacts to chip size, density, and cost, because dummy channels mitigate edge effects and stability issues. Reply 22-23. Petitioner also argues only a small number of channels are affected, and "fabricating an operational device" is of equal concern as density and size. *Id.* But Petitioner's arguments still suffer from flaws identified by the ID. First, Petitioner has not shown Nishikawa suffers from stability issues; nor has Petitioner shown Nishikawa suffers from problematic edge effects. ID 19-20. Second, even if adding dummy channels would provide these purported benefits, Petitioner has not shown how a POSITA would view them as desirable given Nishikawa's existing structure, considering trade-offs with additional processing needed to create them, and at the expense of chip size, density, and cost. *Id.* Even if dummy channels were conventional and routine to fabricate, adding dummy channels to an already-dense memory array, as Petitioner proposes, introduces processing risks. POR 49-50.

5. Petitioner improperly relies on a POSITA's knowledge to gap-fill for missing limitations

Petitioner argues dummy channels are not missing because they were known. Reply 23. However, neither Nishikawa nor Nishikawa123, the actual references in Petitioner's obvious combinations, disclose dummy channels. Therefore, dummy channels are a missing limitation. POR 55; Reply 23-24. For a myriad of reasons explained by Dr. Campbell and in the POR, adding dummy channels is not "unusually simple," and Petitioner cannot rely on general knowledge. POR 55-58; Campbell2 ¶¶117-127. Etching and depositing various materials in a dense array is "the most difficult step in 3D NAND." Ex.2028, 4; Campbell2 ¶118. Petitioner also fails to show 3D NAND technology "particularly straightforward." POR 32-33; *DSS Tech.*, 885 F.3d at 1374.

Even if the dummy channel limitations are "peripheral," which they are not, reliance on common sense "must still be supported by evidence and a reasoned explanation," which Petitioner fails to provide. Reply 24; *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1363 (Fed. Cir. 2016). General knowledge "cannot be used as a wholesale substitute for reasoned analysis and evidentiary support." *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337-38 (Fed. Cir. 2020).

6. Dr. Campbell's testimony

Petitioner asks the Board to disregard "Dr. Campbell's testimony on issues pertaining to dummy channels" because he was not familiar with the terms "edge

array effects,” “array edge effects,” or “edge effects” at his deposition. Reply 24. But Petitioner and Dr. Lee did not use these terms in the Petition or opening declaration; nor do these terms appear in *any* reference they relied on, including those discussing dummy channels. These terms appear *only* in two references Petitioner cites for the first time in Reply—*after* Dr. Campbell’s deposition. Moreover, counsel never explained these terms to test Dr. Campbell’s actual knowledge of their underlying concepts.

IV. Petitioner’s Ribbed TAC Arguments Fail

A. The ID was correct and Petitioner fails to overcome the Board’s concerns

The ID correctly determined that Petitioner’s motivation to apply ribbed TACs to Nishikawa derived from the ’322 patent itself and that Petitioner failed to show a POSITA would find ribbed TACs desirable. ID 20-22. Petitioner advances new arguments and evidence in Reply that fail to overcome the ID’s concerns.

To start, Petitioner argues PO omitted a full description of the process surrounding ribbed cavities to “obfuscate” their use in the final product. Reply 26-27. Not so. It was Petitioner who argued that “[i]t was well[-]known that an option for a TAC or other through-memory structures was to have a ribbed shape, that is, forming recesses in one of the stack layers,” that “creates additional area for the insulating spacer.” Pet.75-77. *Nowhere* do the Petition or Dr. Lee argue about their

role in the final product, or that “these lateral recesses are hardly visibly in the final product due to a subsequent process step.” Reply 26.

On the merits, Petitioner's new argument fails to overcome deficiencies identified in the ID (at 20-22). First, the ID correctly found Petitioner failed to explain why providing “additional area for the dielectric liner (spacer)” is advantageous, “except that it serves the same purpose as the lateral recesses in the '322 patent.” *Id.* 21. Nor did the Petition explain how ribbed cavities solve any problem in Nishikawa that would motivate their use. *Intel*, 61 F.4th at 1381. Petitioner now recasts the same motivation as “short-circuit” protection. Reply 25-32. Specifically, Petitioner argues ribbed cavities create extra room for dielectric material to “prevent shorting the conductive layers from the TAC” and avoiding “leakage current.” *Id.* But this is the purpose taught by the '322 patent: ribbed cavities can provide space for a thicker dielectric layer deposition and the resulting spacer “can electrically insulate conductor layer [of the] TAC” from the “surrounding conductor layers” in memory stack. Ex.1001, 8:47-62. Thus, Petitioner's new motivation *still* “serves the same purpose as the '322 Patent” (Pet.77) and is “obtained solely from the challenged patent.” ID 21 (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007)). Petitioner identifies no motivation that does not originate from the '322 patent.

Second, the ID correctly found that Petitioner's "unintentional recess" argument fails because it did not show a POSITA would find the combination desirable, especially where Petitioner's own cited evidence teaches the importance of having "smooth sidewall[s]." ID 21-22. Without citing any authority, Petitioner's Reply argues the Board just got it wrong. Reply 33. Petitioner contends it does not rely on inherency, yet argues that the proper question is whether using typical and obvious etchants "would...result in unintentional recess." *Id.* In other words, Petitioner still argues the limitation is "necessarily...present[] or the natural result." POR 61-62 (citing *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1195 (Fed. Cir. 2014)). This argument fails and "[u]nintentional recesses are neither the natural result nor necessarily present in Nishikawa," as the POR explains. *Id.*

Petitioner's evidence suggesting it was a "challenge" to find an etchant that can etch without selectivity only proves PO's position. Reply 33. The same reference teaches both the importance of achieving "smooth sidewall[s]" and a solution to doing so (hydrofluorocarbon etching gases). POR 63-64. A POSITA would have sought and used gases that can etch without selectivity, including the specified solution. *Id.*

Thus, Petitioner still fails to show a POSITA would have desired the proposed combination.¹³

B. Petitioner improperly relies on a POSITA's knowledge to gap-fill missing limitations

Petitioner advances the same argument for why the ribbed TAC limitation is not missing as it does for the dummy channel limitation—it was disclosed in the prior art. *Supra* §III.A.5. Petitioner's arguments fail for the same reasons. None of the references in Petitioner's obviousness combinations discloses the claimed limitation. And Petitioner fails to respond to the myriad of reasons Dr. Campbell explained for why attempting ribbed TACs is not “unusually simple” and 3D NAND is not “particularly straightforward.” POR 32-33, 67-68; Campbell2 ¶¶87-89. Nor can Petitioner circumvent providing sufficient evidence to meet its obviousness burden by arguing the limitation is “peripheral.” *Supra* §III.A.5.

¹³ Petitioner again suggests PO has adopted a position that the claims require “largely undetectable and unintentional alleged recesses.” POR 60; Reply 32. PO never set forth this construction. POR 60.

V. Petitioner's Equal-Diameter Arguments Fail**A. Petitioner's reliance on figures to disclose relative proportions of peripheral contacts and TACs is wrong**

Petitioner argues that PO is “discount[ing] the relevance of figures” that purportedly disclose peripheral contacts and TACs with the same diameters. Not so.

Petitioner argues incorrectly that because the claims do not recite a “specific dimension,” *Nystrom* does not apply and Petitioner can use the figures to establish that the peripheral contacts and TACs have the same diameters. Reply 35-37. *Nystrom* governs and prohibits reading relative proportions into drawings, as Petitioner does here. Moreover, the recent P.T.A.B. decision Petitioner cites *supports PO*.

In *Nystrom*, the Federal Circuit rejected a decision by the Board comparing “relative dimensions” of drawings. *Nystrom v. TREX Co.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005) (“arguments based on drawings not explicitly made to scale in issued patents are unavailing”). The court confirmed its “disfavor in reading precise proportions into patent drawings which do not expressly provide such proportions.” *Id.* Here, Petitioner argues that figures inform the relative proportions of TACs and peripheral contacts described in the claimed language (i.e., equal diameters), which is exactly the kind of argument *Nystrom* rejected.

Further, in the Board's recent decision in unrelated IPR2024-00789, it rejected PO's arguments against Petitioner's reliance on figures because the claims

recited “relative *positioning*..., not specific dimensions or proportions.” Paper 37, 28 (Oct. 23, 2025).

B. Petitioner fails to identify any primary or background references disclosing the claimed equal diameters or proportions

Petitioner suggests *Nystrom* applies only to prevent reliance on figures when “the specification is completely silent on the issue.” Reply 36. But that is the situation here. Petitioner argues incorrectly that written descriptions in Nakajima and Mushiga “disclose TACs and peripheral contacts with the same diameters.” These references disclose forming certain contacts using the *same process* but are “completely silent” on diameters or proportions. *Id.* Petitioner attempts, but fails, to extrapolate this information from processing disclosures, citing no disclosure of the claimed equal diameters for peripheral contacts and TACs. *Id.* 35-40.

First, Tessariol does not disclose that both have the same diameter. Petitioner at best shows that Tessariol etched two holes, i.e., dummy-structure openings 56 and via openings 54, through the stack at the same time. *Id.* 34-35. Petitioner does not show that Tessariol discloses the TAC is formed through the stack and a peripheral contact outside the stack, as claimed. POR 73-74. Nor does Petitioner establish that the materials and structures *within* Tessariol's stack require the same etchant and etch steps as the materials and structures *outside* of the stack. *Id.* 73-75.

Second, Petitioner argues that a POSITA would understand Nakajima and Mushiga to disclose contacts of the same size based on descriptions of their

processing. Reply 36. But Petitioner provides no support for this conclusory statement.

For example, Petitioner cites various processing steps of Mushiga and argues Mushiga discloses forming its contacts using “the same processing steps at the same time.” *Id.* 36-37. Mushiga does not disclose relevant “timing” information. POR 70-71. Moreover, these steps omit diameter or proportions used in forming the contacts. *Id.* Petitioner again improperly resorts to Mushiga’s Figures, arguing they “depict[] peripheral contacts and TACs (both 586) with the same diameters.” Reply 36-38; *Nystrom*, 424 F.3d at 1149. But what Petitioner calls peripheral contacts and TACs, Mushiga defines as “insulating spacer[s],” not contact structures. Ex.1012, 10:40-41.

Petitioner also argues Nakajima discloses forming all its contacts “via the same process,” but does not identify where Nakajima discloses peripheral contacts and TACs having the same diameter. Reply 36. Petitioner argues using the same process is “consistent” with using the same diameter, citing only a 36-year-old textbook. *Id.* But the textbook does not disclose using the same size for different contacts anytime the same process is used, as Petitioner argues here. Ex.1035, 33.

Petitioner disputes that Nakajima incorrectly labeled a peripheral contact as C4 when it should be C3. Reply 38-40. Petitioner’s arguments are based entirely on Petitioner’s own observations of purported distinctions in Fig.2 without support. *Id.* In stark contrast, each of PO’s reasons why this peripheral contact was mislabeled

finds direct textual support in the specification. POR 71-73. Thus, Petitioner's arguments should be disregarded.¹⁴

Finally, even if prior art references disclose equal diameters, which they do not, Petitioner would show only that a POSITA *could* have, but not *would* have practiced the limitation. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). Thus, Petitioner fails to show a motivation to combine that renders the equal diameters limitations obvious.

C. Petitioner improperly relies on a POSITA's knowledge to supply missing limitations.

Petitioner refers back to its previous arguments for why there are no missing limitations. These arguments fail for the same reasons described *supra*.

VI. Conclusion

For the reasons above, the Board should deny the Petition for Inter Partes Review.

Respectfully submitted,

Dated: March 23, 2026

By: / Adam Greenfield /

Adam Greenfield (Reg. No. 60,331)
adam.greenfield@lw.com

¹⁴ Petitioner's arguments regarding diameters of peripheral contacts and TACs also fail because a POSITA would not have modified Nishikawa to include a circular TAC. *Supra* §§II.A-C; POR 69.

Latham & Watkins LLP
555 Eleventh Street, NW, Ste. 1000
Washington, D.C. 20004-1304
Telephone: 202.637.2308
Facsimile: 202.637.2201

*Counsel for Patent Owner
Yangtze Memory Technologies
Company, Ltd.*

CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Sur-Reply complies with the word count limitation of 37 C.F.R. § 42.24(c)(4) because the Patent Owner's Sur-Reply contains 5,585 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Sur-Reply exempted by 37 C.F.R. § 42.24(c).

By: / Adam Greenfield /

Adam Greenfield (Reg. No. 60,331)
adam.greenfield@lw.com
Latham & Watkins LLP
555 Eleventh Street, NW, Ste. 1000
Washington, D.C. 20004-1304
Telephone: 202.637.2308
Facsimile: 202.637.2201

*Counsel for Patent Owner
Yangtze Memory Technologies
Company, Ltd.*

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 23rd day of March, 2026, a true and correct copy of the foregoing **Patent Owner's Sur-Reply** was served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

Jeremy Jason Lang (Reg No. 73,604)
Jared Bobrow (admitted *Pro Hac Vice*)
Orrick, Herrington & Sutcliffe LLP
1000 Marsh Road
Menlo Park, CA 94025-1015
T: 650-614-7400
F: 650-614-7401
jlang@orrick.com
jbobrow@orrick.com
PTABDocketJL2@orrick.com
PTABDocketT6J1@orrick.com
PTABDocketJ3B3@orrick.com
MICRON-YMTC_OHS@orrick.com

Thomas James (Reg No. 74,109)
Orrick, Herrington & Sutcliffe LLP
353 N Clark Street, Suite 3600
Chicago, IL 60654
T: 312-924-9800
F: 312-924-9899
tjames@orrick.com

By: / Adam Greenfield /

Adam Greenfield (Reg. No. 60,331)
adam.greenfield@lw.com
Latham & Watkins LLP
555 Eleventh Street, NW, Ste. 1000
Washington, D.C. 20004-1304
Telephone: 202.637.2308

Facsimile: 202.637.2201

*Counsel for Patent Owner
Yangtze Memory Technologies
Company, Ltd.*