

Micron Technology, Inc. (Petitioner)
v.
Yangtze Memory Technologies Company, Ltd. (Patent Owner)

IPR2025-00191 (U.S. Patent No. 11,581,322)

Patent Owner YMTC's Demonstratives

April 27, 2026



Petitioner's Four Asserted Grounds Fail

Petition

Petitioner challenges the claims on the following grounds:

Ground 1: Claims 1-3, 6, 7-10, 13-16, and 19-20 are obvious over Nishikawa.

Ground 2: Claims 4-5, 11-12, and 17-18 are obvious over Nishikawa in view of Lu.

Ground 3: Claims 1-3, 6, 7-10, 13-16, and 19-20 are obvious over Nishikawa in view of Nishikawa2.

Ground 4: Claims 4-5, 11-12, and 17-18 are obvious over Nishikawa in view of Nishikawa2 and Lu.

Pet. 10



'322 Patent

Circular TACs Would Not Have Been Obvious (Claims 6, 8-20)

Dummy Channels Would Not Have Been Obvious (Claims 3, 6, 14-18, 20)

Petitioner's Ribbed TAC Arguments Fail (Claims 13-18, 20)

Petitioner's Equal-Diameter Arguments Lack Merit (Claims 6, 9-10, 15-16)



'322 Patent

Circular TACs Would Not Have Been Obvious (Claims 6, 8-20)

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The '322 Patent

THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

US 11,581,322 B2

(12) United States Patent
Guo et al.

(10) Patent No.: **US 11,581,322 B2**
(45) Date of Patent: **Feb. 14, 2023**

(54) **THREE-DIMENSIONAL MEMORY DEVICES
HAVING THROUGH ARRAY CONTACTS
AND METHODS FOR FORMING THE SAME**

(71) Applicant: YANGTZE MEMORY
TECHNOLOGIES CO., LTD., Wuhan
(CN)

(72) Inventors: Mei Lan Guo, Wuhan (CN); Yuchai Hu,
Wuhan (CN); Ji Xia, Wuhan (CN);
Hongbin Zhu, Wuhan (CN)

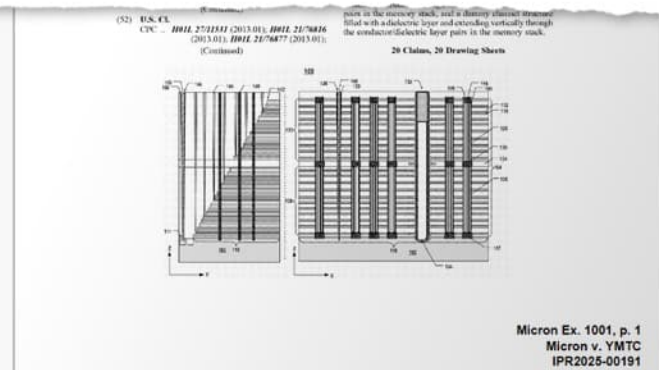
(73) Assignee: YANGTZE MEMORY
TECHNOLOGIES CO., LTD., Wuhan
(CN)

(51) Field of Classification Search
CPC: H01L 27/1331; H01L 21/76816; H01L
21/76877; H01L 29/5226
(Continued)

(56) References Cited
U.S. PATENT DOCUMENTS
8,442,861 B1 * 11/2017 Huang H01L 27/1337
10,594,891 B1 * 7/2019 Kim H01L 27/1337
(Continued)

FOREIGN PATENT DOCUMENTS
CN 10679063 A 12/2016
CN 10992746 A 9/2017

Patent No.: **US 11,581,322 B2**
Date of Patent: **Feb. 14, 2023**



Ex. 1001 ('322 Patent)



The '322 Patent – The Problem With Barrier Structures

In some 3D memory devices, interconnects can include through array contacts (TACs) for providing vertical interconnects between the stacked memory array device and peripheral device (e.g., for power bus and metal routing), thereby reducing metal levels and shrinking die size. TACs can be formed within barrier structures, which preserves a dielectric stack region within a memory stack for ease of etching the openings of the TACs. However, the regions enclosed by the barrier structures take up large area in the core array region where memory strings can be formed and also have a negative impact on the resistance of word lines. Moreover, the existing fabrication processes for forming the barrier structures become more challenging for the next-generation 3D memory devices (e.g., having 128 levels or more), which have less process margin.

Ex. 1001 ('322 Patent), 4:58-5:5

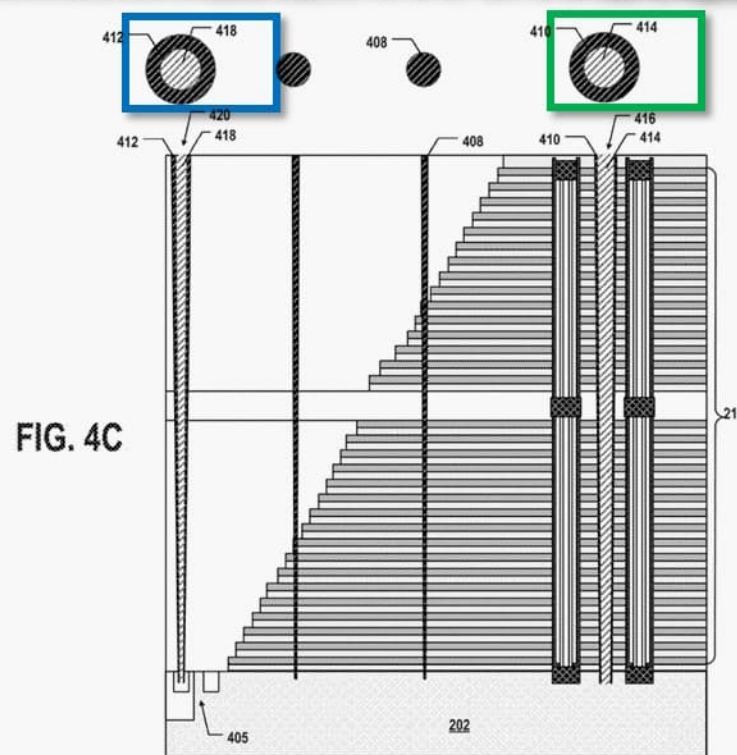
The '322 Patent's Solution

Various embodiments in accordance with the present disclosure provide a 3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures. For example, by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost. More process margin can also be obtained due to the elimination of etching and alignment steps for making the barrier structures, which enables high process extendibility for both current and future generations of 3D memory devices. Moreover, various embodiments of methods for forming the 3D memory device disclosed herein can allow TACs to be formed in the same fabrication process(es) for making other structures (e.g., peripheral contacts and/or dummy channel structures) and thus, further simplify the fabrication flow and reduce process cost.

Ex. 1001 ('322 Patent), 5:6-22

stack 104. In some embodiments, TAC 136 has a substantially circular shape in the plan view, and conductor layer 140 and spacer 138 are disposed radially from the center of TAC 136 in this order. Spacer 138 of TAC 136 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

Ex. 1001 ('322 Patent), 8:56-62



Ex. 1001 ('322 Patent),
Fig. 4C (annotated)



'322 Patent

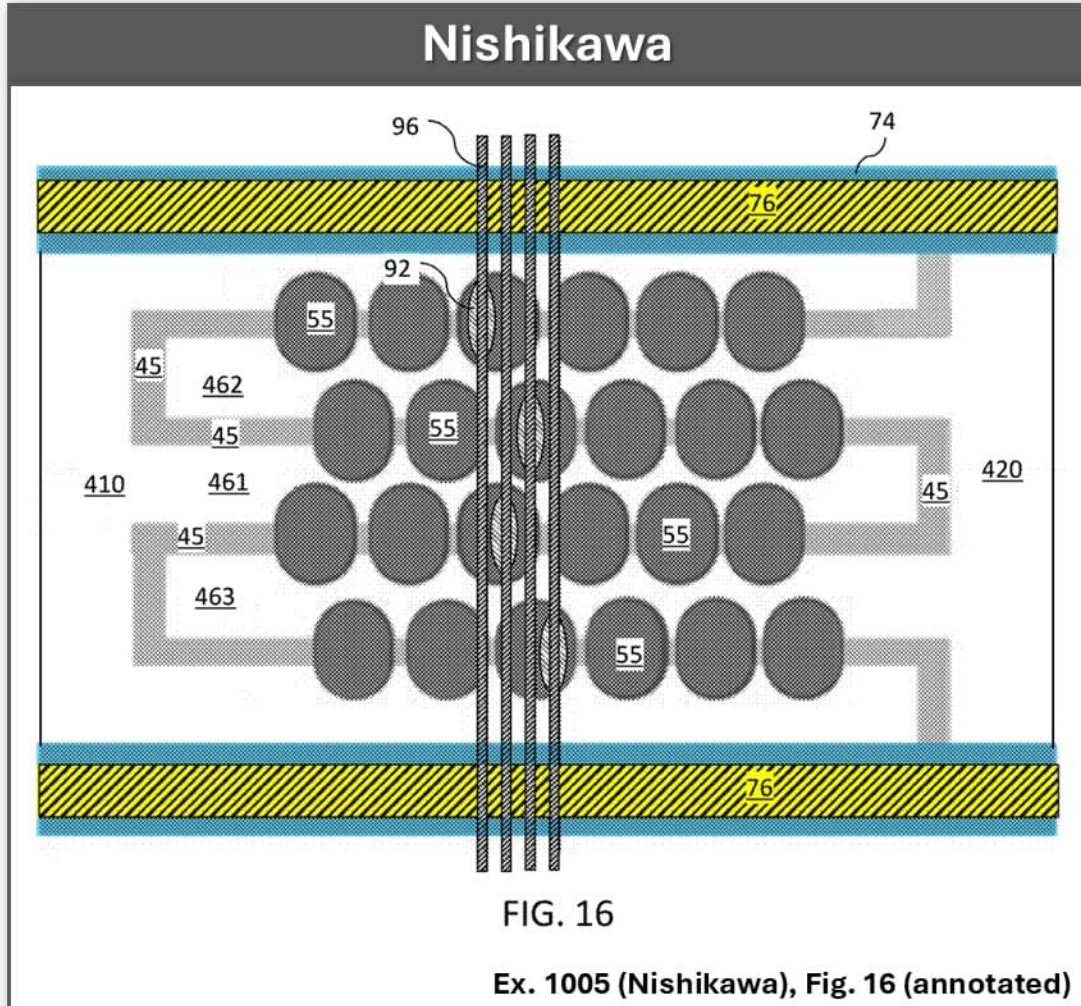
Circular TACs Would Not Have Been Obvious (Claims 6, 8-20)

Dummy Channels Would Not Have Been Obvious (Claims 3, 6, 14-18, 20)

Petitioner's Ribbed TAC Arguments Fail (Claims 13-18, 20)

Petitioner's Equal-Diameter Arguments Lack Merit (Claims 6, 9-10, 15-16)

Petitioner Modifies Nishikawa's Trench With A Circular TAC



Petition

In addition, a POSITA would have been motivated, with a reasonable expectation of success, to modify the trench-shaped common source contact (74, 76) of Nishikawa to instead be a cylindrical source contact for several reasons.

Pet. 51

Nishikawa Teaches A Vertical Structure With Dual Memory Cells

Nishikawa

(57)

ABSTRACT

A vertical memory device including dual memory cells per level in each memory opening can have dielectric separator dielectric structures that protrude into a facing pair of sidewalls of the memory stack structure within the memory opening. A pair of inactive sections of a vertical semiconductor channel facing the dielectric separator dielectric structures is laterally recessed from control gate electrodes. Control of the threshold voltage of such a vertical memory device can be enhanced because of the dielectric separator dielectric structures. The fringe field from the control gate electrodes is weaker due to an increased distance between the control gate electrodes and the inactive sections of the vertical semiconductor channel. The memory stack structure can have concave sidewalls that contact the dielectric separator dielectric structures and convex sidewalls that protrude toward the control gate electrodes.

Ex. 1005 (Nishikawa), Abstract

Nishikawa

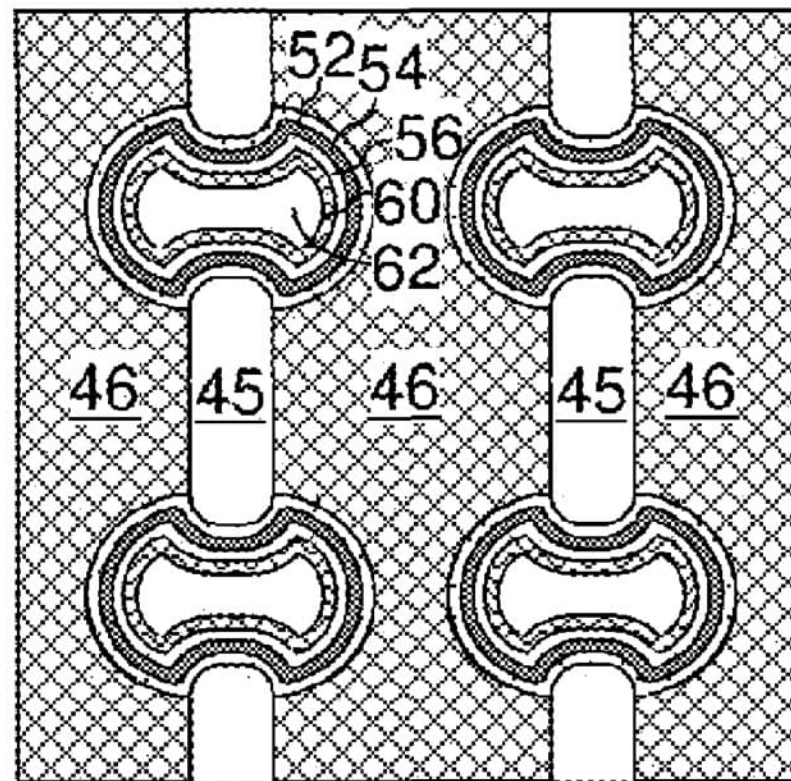
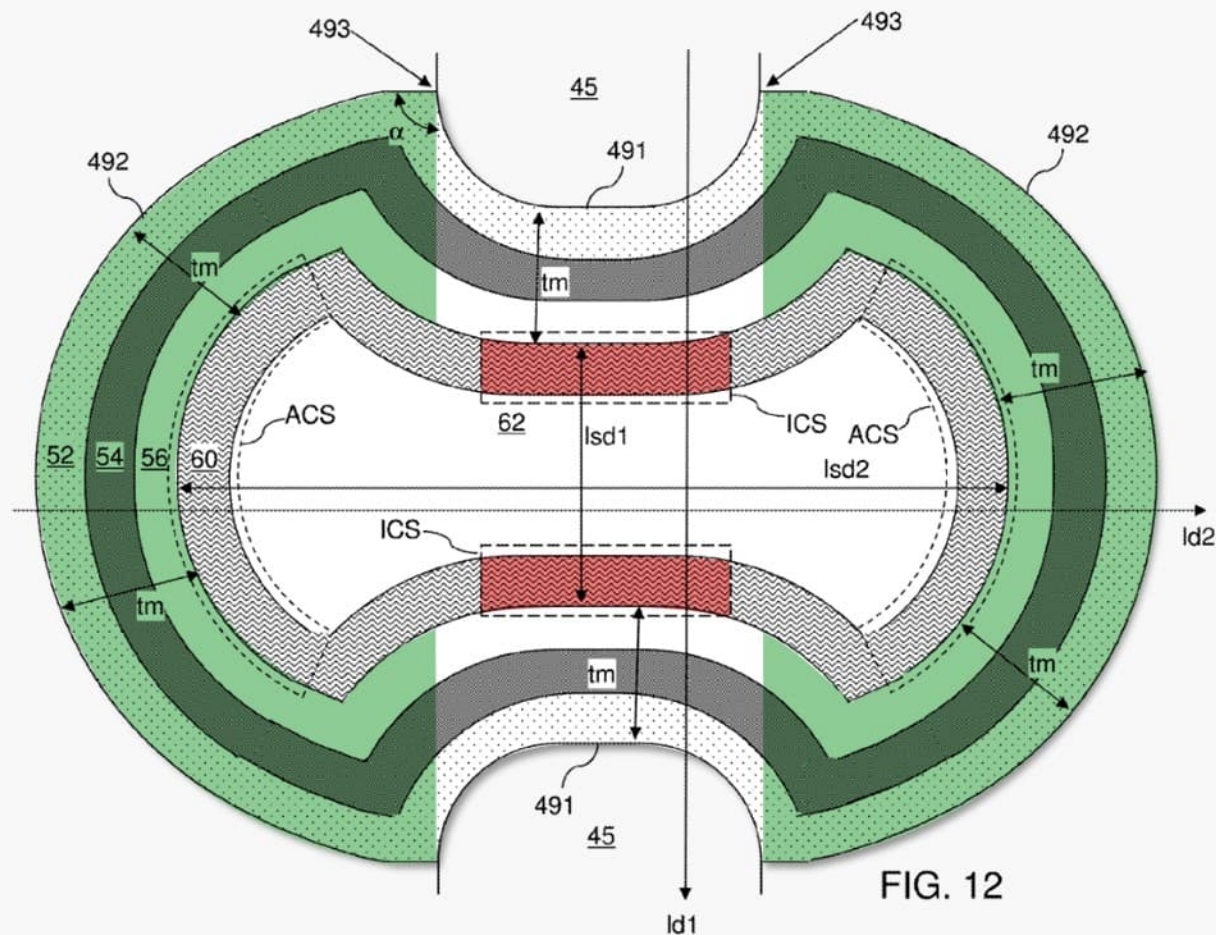


FIG. 11C

Ex. 1005 (Nishikawa), Fig. 11C

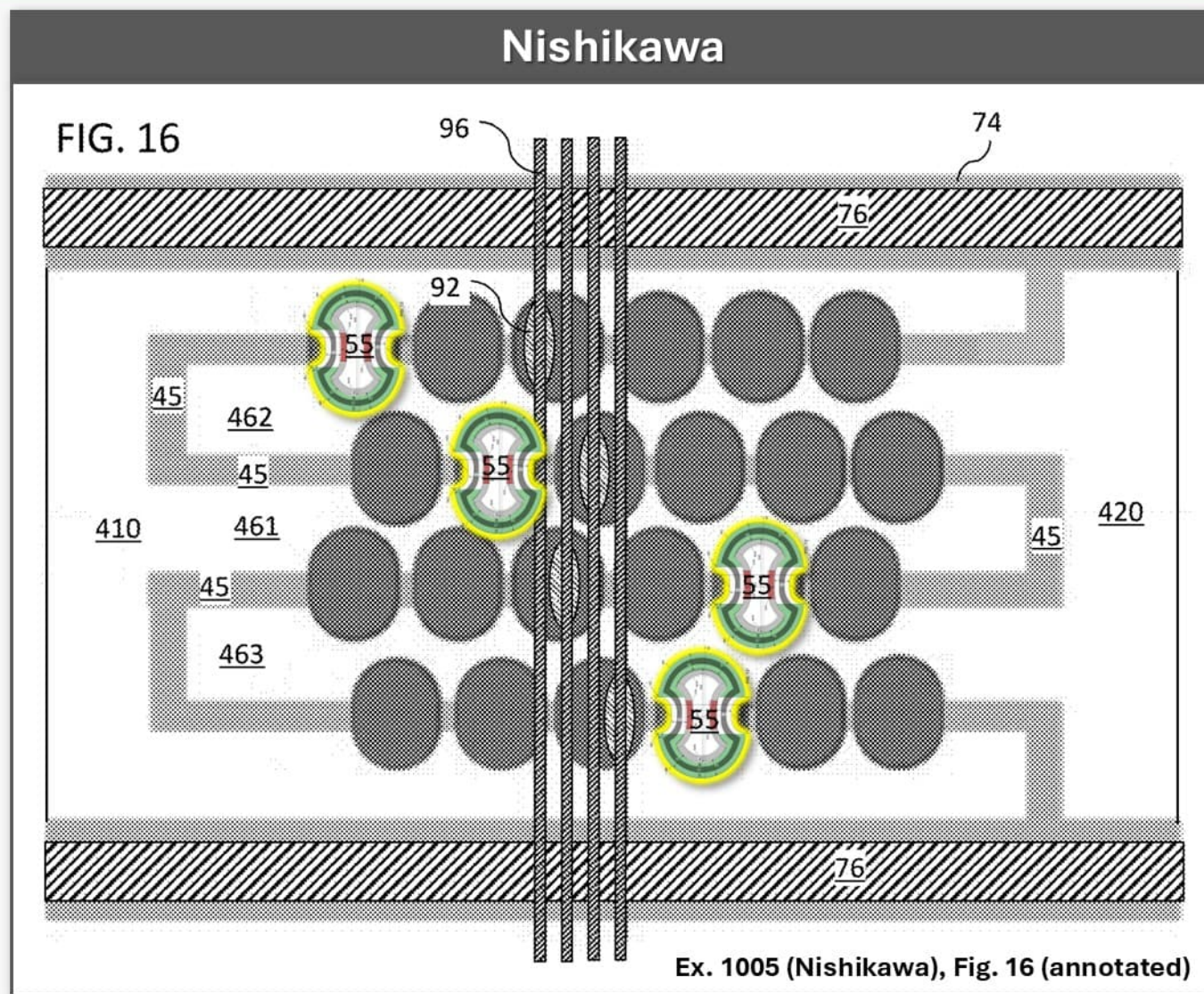
Nishikawa Teaches A Vertical Structure With Dual Memory Cells



Ex. 1005 (Nishikawa), Fig. 12 (annotated), 14:34-46, 14:60-15:2;
Ex. 2021 (Campbell POR Decl.) ¶ 50



Nishikawa Teaches A Vertical Structure With Dual Memory Cells



Nishikawa Requires Isolating Wordlines On Every Level

Nishikawa

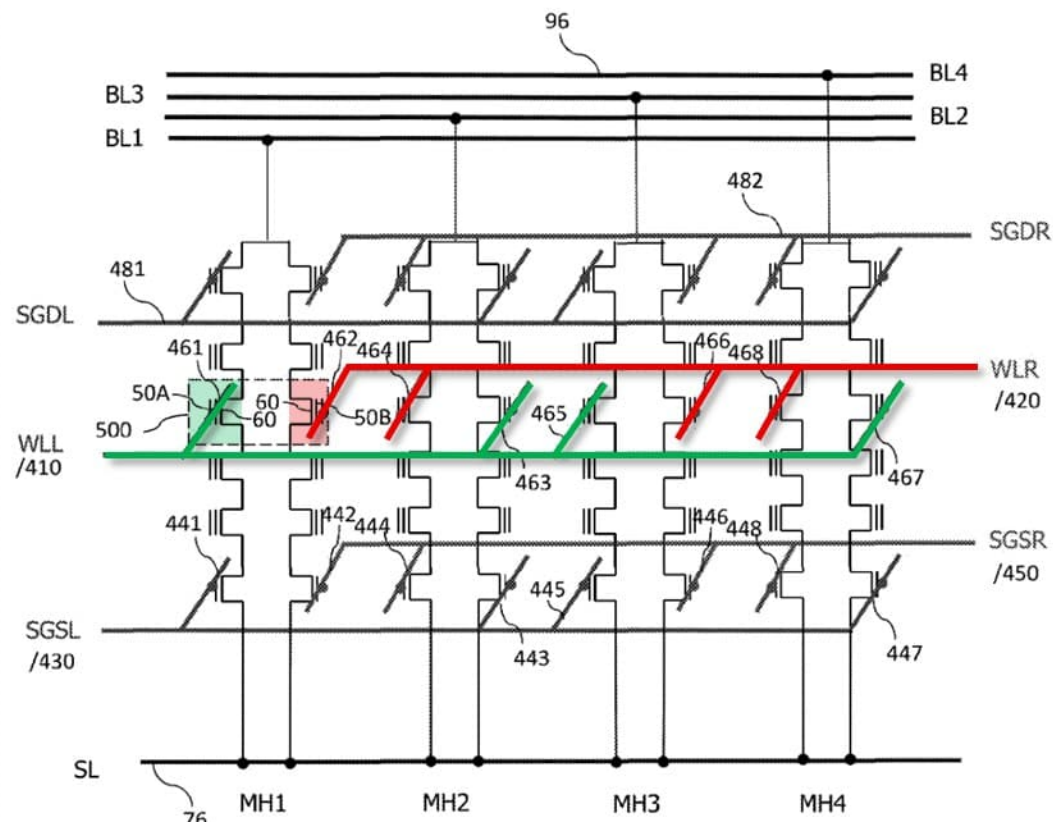
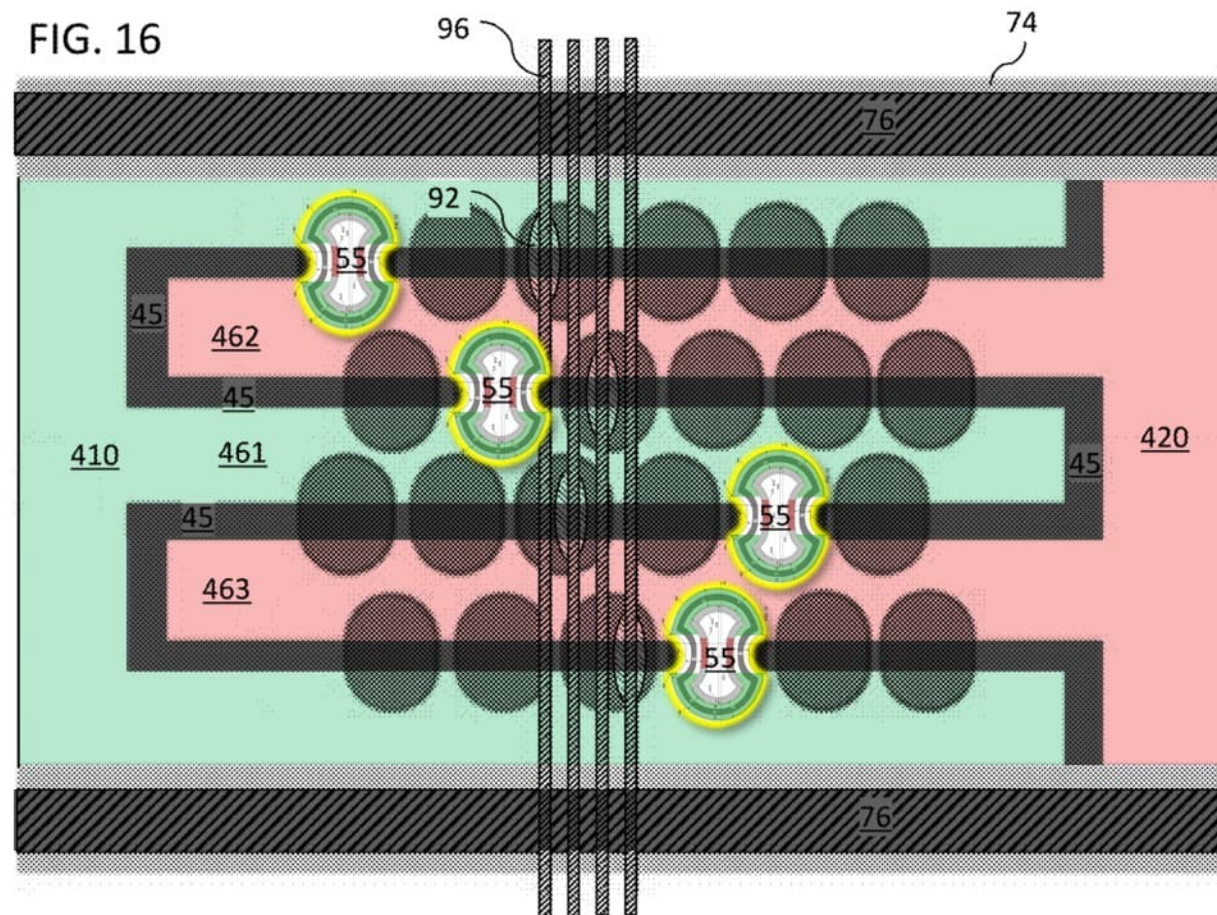


FIG. 14

Ex. 1005 (Nishikawa), Fig. 14 (annotated)

Nishikawa

FIG. 16



Ex. 1005 (Nishikawa), Fig. 16 (annotated)

Petitioner's Proposed Modifications To Nishikawa Would Not Work

Nishikawa

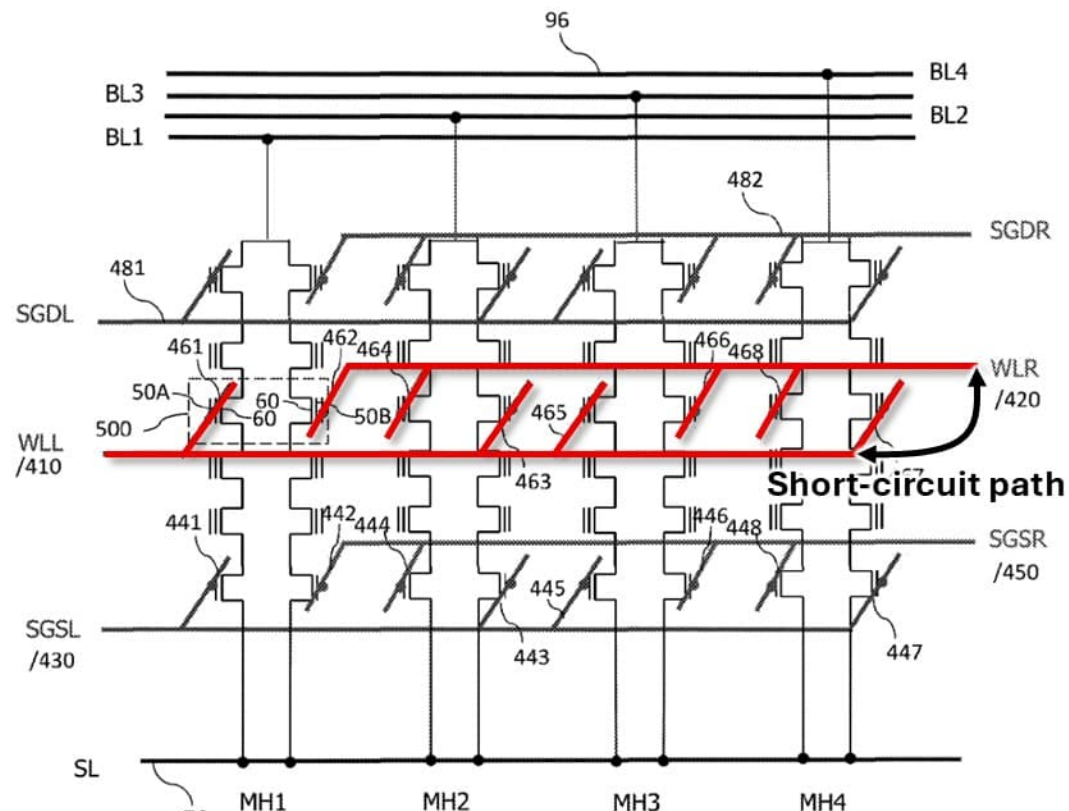
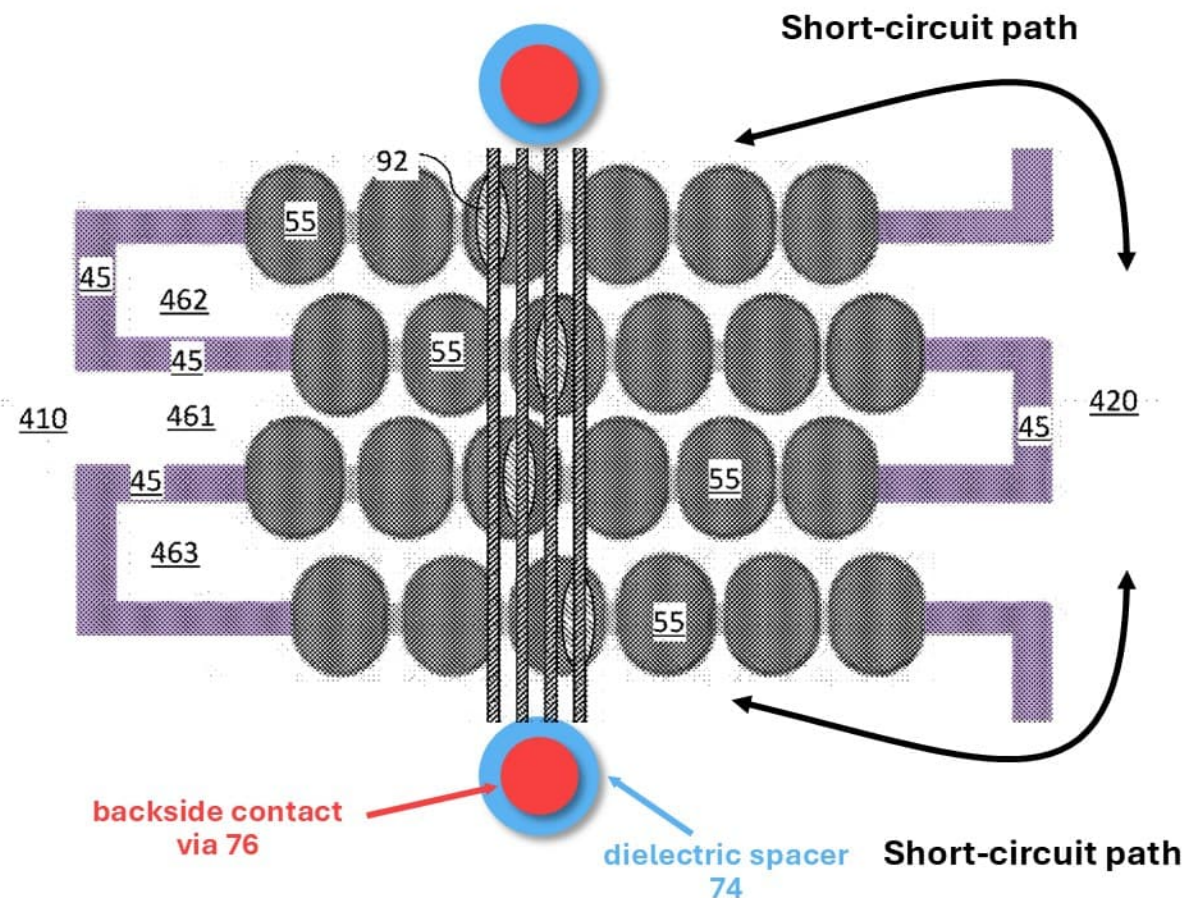


FIG. 14

Ex. 1005 (Nishikawa), Fig. 14 (annotated)

Nishikawa



backside contact
via 76

dielectric spacer
74

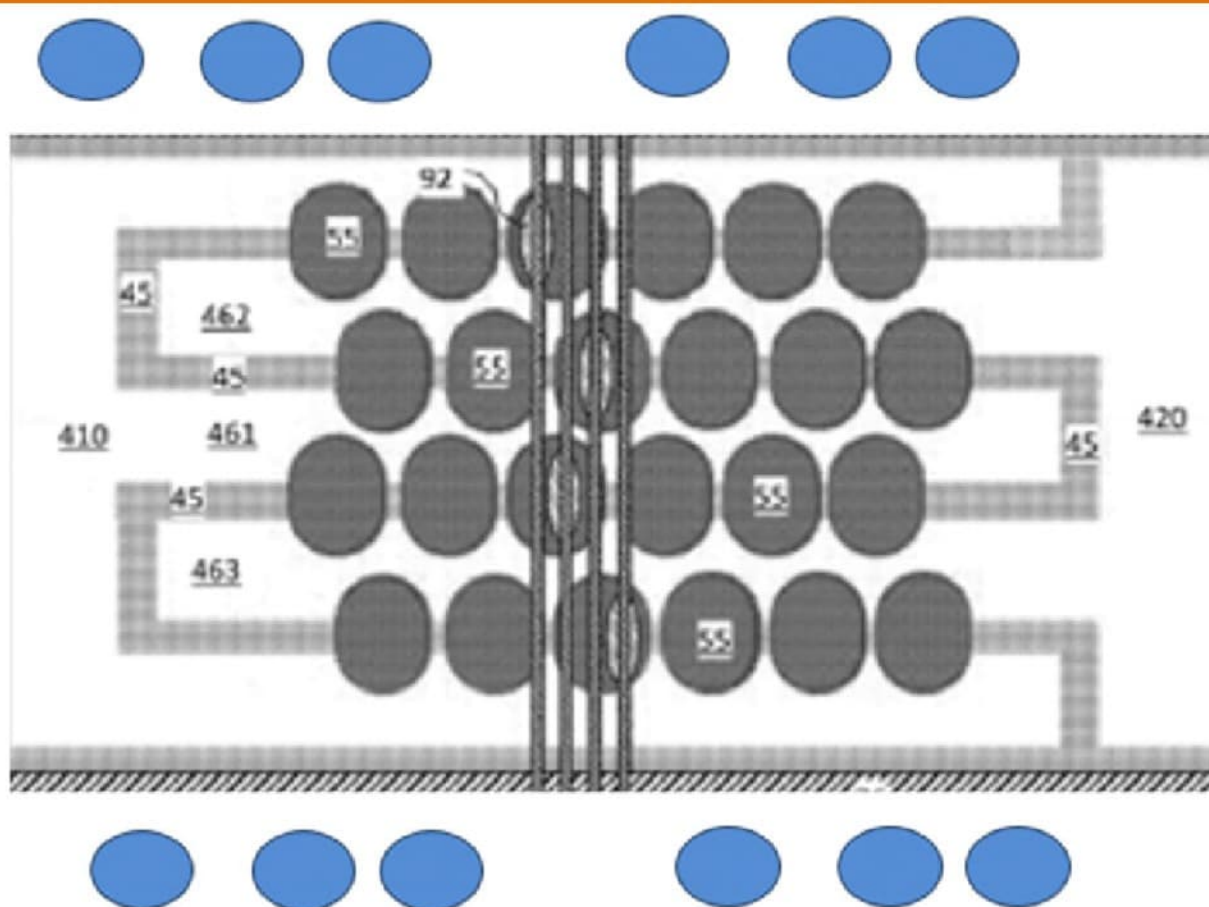
Short-circuit path

Patent Owner Response (modifying Ex. 1005 (Nishikawa), Fig. 16)



Petitioner's Proposed Modifications To Nishikawa Would Not Work

Petitioner's Reply



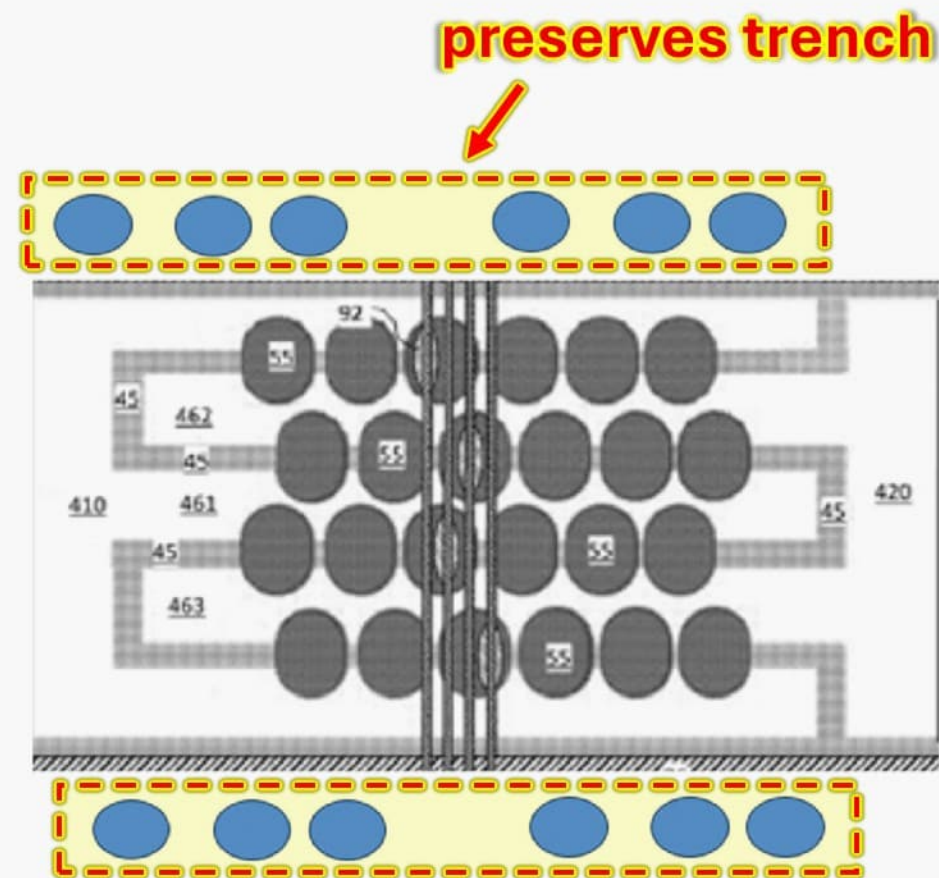
Reply 4

Multiple Circular TACs Contravenes Petitioner's Motivation To Modify Nishikawa

Petition

contact). The trench has a large footprint. Replacing the trench with smaller cylindrical source contact(s), in effect, recovers a large portion of that lost footprint, providing additional room for memory cells. In short, the modification increases the

Pet. 51



Ex. 1105 (Lee Reply Decl.) ¶ 10 (annotated)



Multiple Circular TACs Would Not Work

Dr. Campbell Second Declaration

62. And such densely packed TACs push the limits of physics because of parasitic capacitance—an undesired but unavoidable feature when conductive materials are in close proximity and separated by nonconductive materials—which would affect device performance.

Ex. 2021 (Campbell POR Decl.) ¶ 62

Multiple Circular TACs In A Trench Would Not Meet The Claims

1. A three-dimensional (3D) memory device, comprising:
a substrate;
a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;
a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;
a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate; and
a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones.

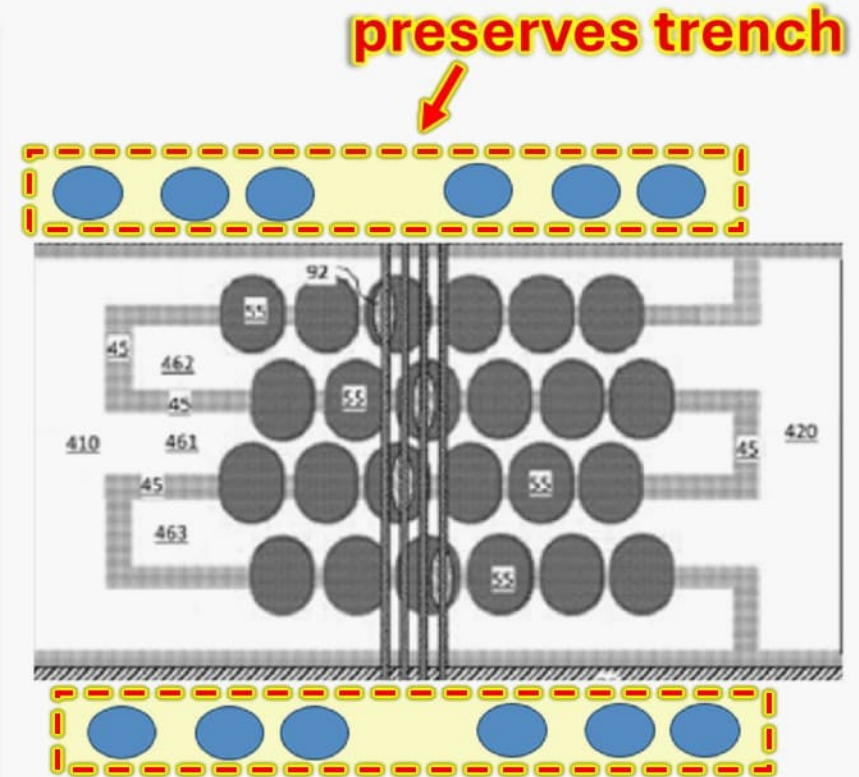
Ex. 1001 ('322 Patent), Claim 1

8. A three-dimensional (3D) memory device, comprising:
a substrate;
a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;
a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack; and
a through array contact (TAC) comprising a substantially circular section and extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate.

Ex. 1001 ('322 Patent), Claim 8

14. A three-dimensional (3D) memory device, comprising:
a substrate;
a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;
a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;
a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a substantially circular section; and
a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,
wherein:
a first diameter of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs; and
a peripheral contact is arranged outside the memory stack and in contact with a peripheral device on the substrate.

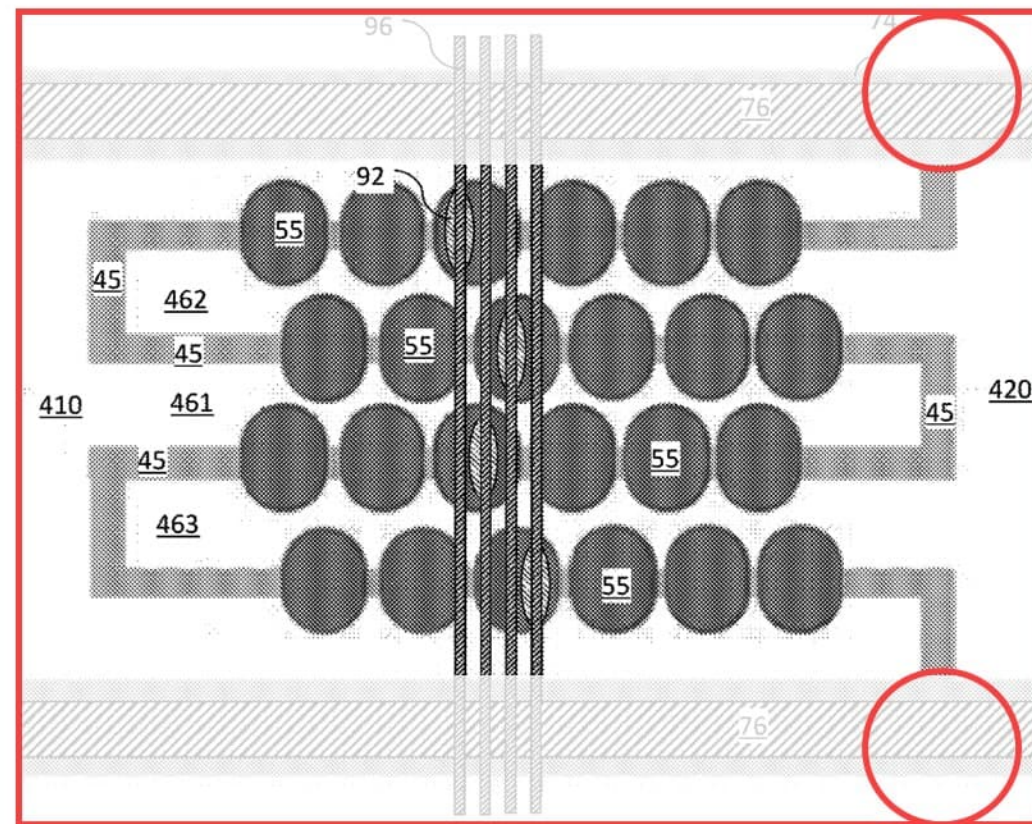
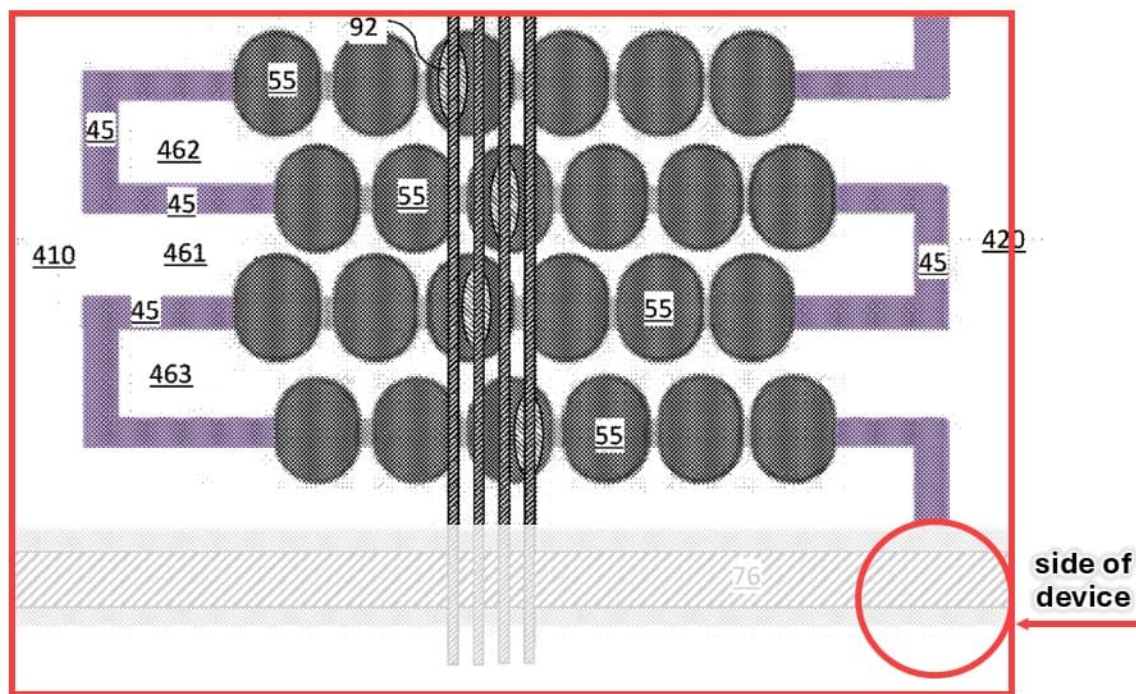
Ex. 1001 ('322 Patent), Claim 14



Ex. 1105 (Lee Reply Decl.) ¶ 10 (annotated)

Petitioner's Proposed Modifications To Nishikawa Would Not Work

Petitioner's Reply at 6-7



Ex. 1005 (Nishikawa), Fig. 16 (annotated)



Petitioner Concedes A Circular TAC Would Have To Contact The Device Edge

Petitioner's Reply

This is because, the circular TACs would be positioned at the edge of the device (e.g., where the trenches were) and isolate the two sides—all while *not* increasing the footprint:

Reply 7



Placing A Circular TAC At The Separator's End *Would* Increase The Device's Footprint

Patent Owner's Expert Dr. Campbell

Q. So you're saying that a TAC position there could provide isolation?

A. So if the -- go back to what it says. The TAC's diameter would have to be large enough to contact the side of the device to maintain isolation. That is absolutely true. And that would require a larger footprint than a regular tranche. Also true. If you're confused about the red circle, I can't help you there. But the words in that sentence are absolutely correct.

Ex. 1106 (Campbell Dep.), 77:4-16

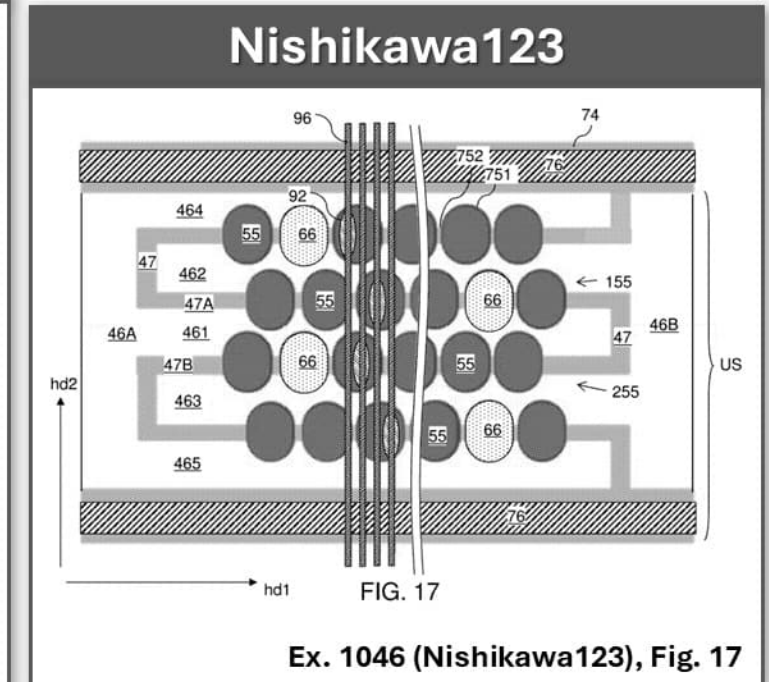
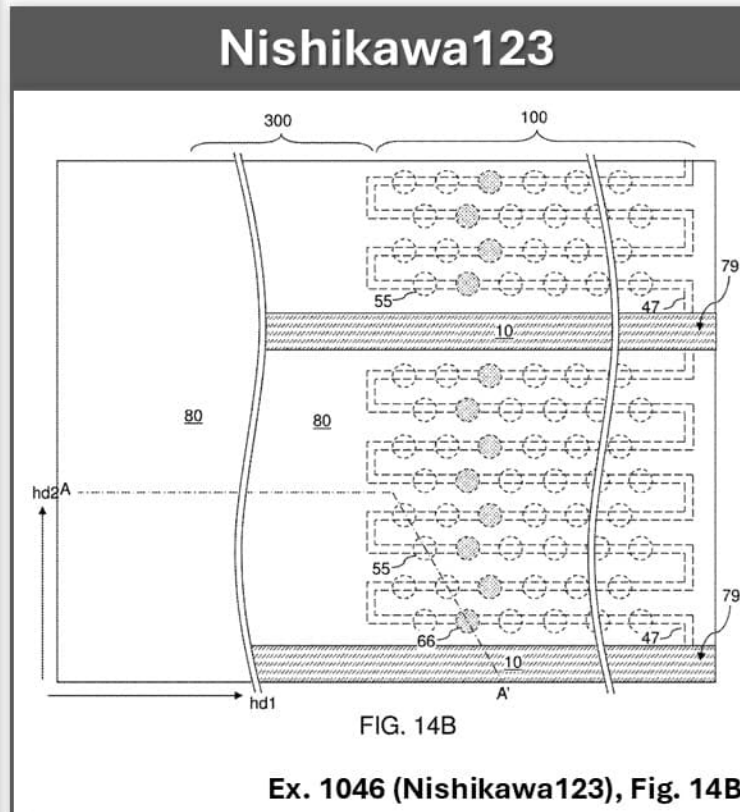
Nishikawa123's Disclosure Of A Circular TAC Does Not Apply To Nishikawa

Nishikawa123

Referring to FIGS. 14A-14D, source electrode (or source local interconnect) openings 79 can be formed through the optional contact level dielectric layer 80, the insulating cap layer 70, the alternating stack (32, 42), and the gate dielectric layer 12. The openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape. For example, in one embodiment, the openings 79 may comprise backside trenches 79. FIG. 14A is a vertical cross-sectional view of the exemplary structure, and FIG. 14B is a top-down view of the exemplary structure of FIG. 14A. FIGS. 14C and 14D provide additional top-down views of two different configurations for the arrangement of the dielectric pillar structures 66 that are compatible with the exemplary structure illustrated in FIGS. 14A and 14B. In other words, FIG. 14C illustrates a first configuration for memory stack structures 55 and dielectric pillar structures 66, and FIG. 14D illustrates a second configuration for memory stack structures 55 and dielectric pillar structures 66. FIGS. 14C and 14D illustrate a portion of the memory array region 100 in two exemplary configurations of the exemplary structure.

Each of the backside trenches 79 can extend horizontally along the first horizontal direction hd1. Each layer within the alternating stack (32, 46) is divided into multiple portions along the second horizontal direction hd2 that is perpendicular to the first horizontal direction hd1 by the backside trenches 79.

Ex. 1046 (Nishikawa123), 22:34-59



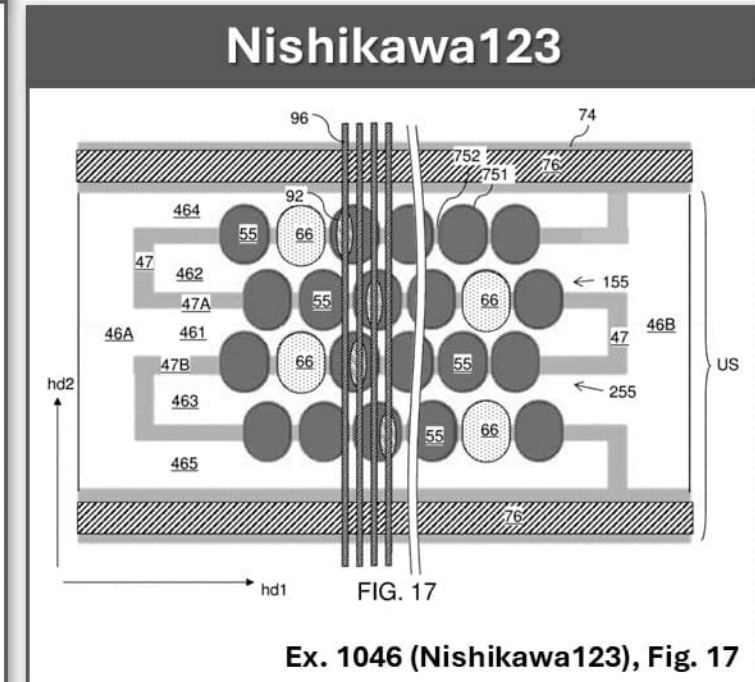
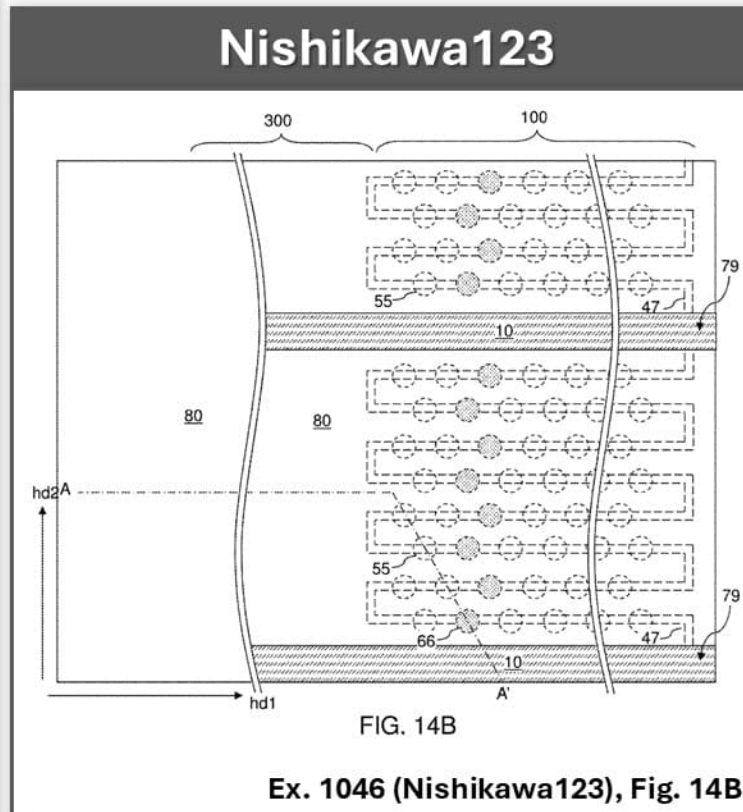
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Ex. 1046 (Nishikawa123), 22:34-59



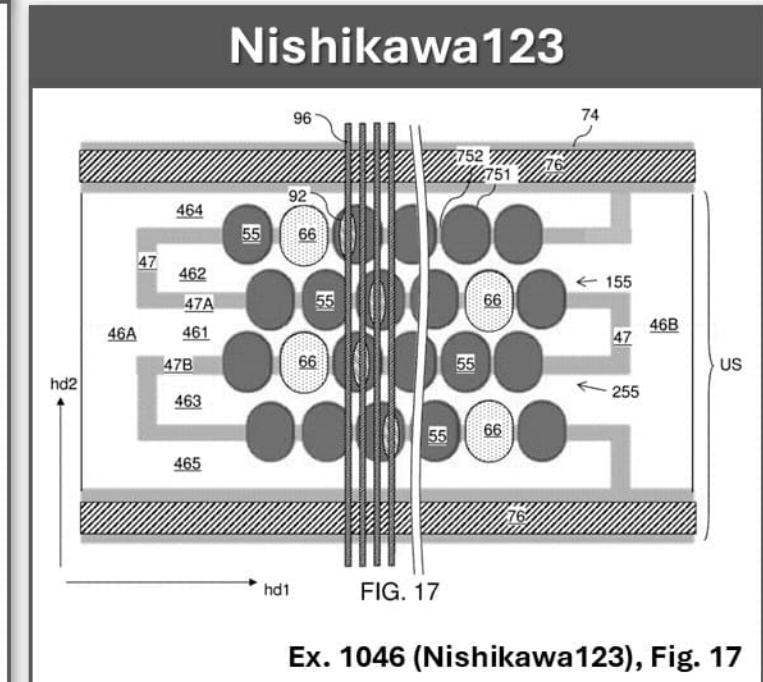
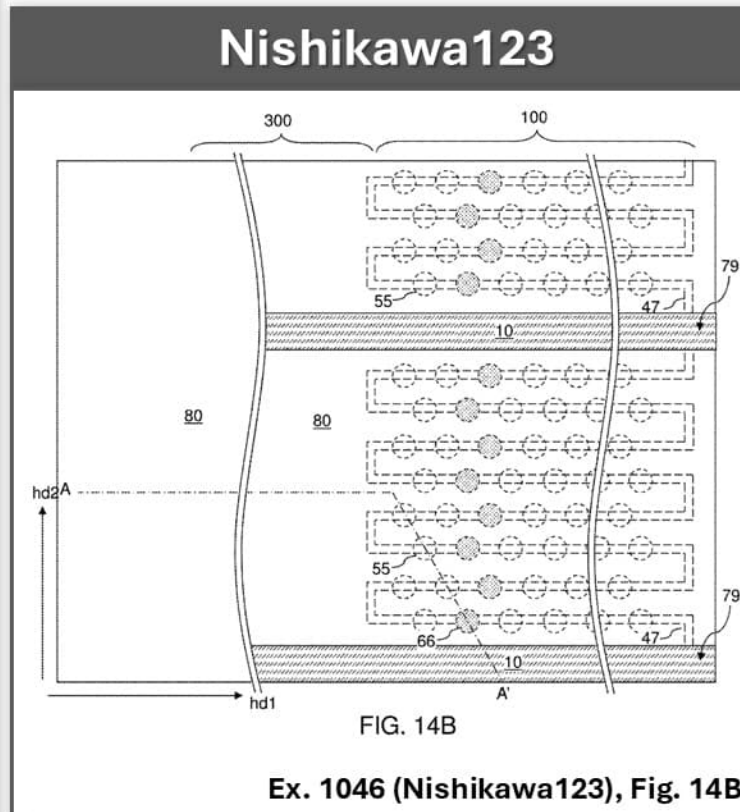
Nishikawa123's Disclosure Of A Circular TAC Does Not Apply To Nishikawa

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Each of the backside trenches 79 can extend horizontally along the first horizontal direction hd1. Each layer within the alternating stack (32, 46) is divided into multiple portions along the second horizontal direction hd2 that is perpendicular to the first horizontal direction hd1 by the backside trenches 79.

Ex. 1046 (Nishikawa123), 22:34-59



Nishikawa123's Disclosure Of A Circular TAC Does Not Apply To Nishikawa

Nishikawa123

Each electrically conductive layer 46 (i.e., each of the word-line-level electrically conductive layers 46) formed within the alternating stack (32, 46) includes two physically disjointed portions (46A, 46B) between each optional neighboring pair of backside trenches (which are filled with the insulating spacers 74 and the backside contact structures 76) that are laterally spaced from each other by a subset of the memory stack structures 55 and portions of the separator insulator structures 47. The two physically disjointed portions (46A, 46B) of each electrically conductive layer 46 comprises two interdigitated electrically conductive portions including multiple fingers (461, 462, 463, 464, 465) that extend along the first horizontal direction hd1. Each of the two interdigitated electrically conductive portions (46A, 46B) includes concave vertical sidewalls 751 that contact respective memory stack structures 55 and are adjoined among one another by planar vertical sidewalls 752 that extend along the first horizontal direction hd1. Multiple instances of the unit structure US can be repeated with periodicity along the second horizontal direction hd2.

Ex. 1046 (Nishikawa123), 25:36-55

Nishikawa123

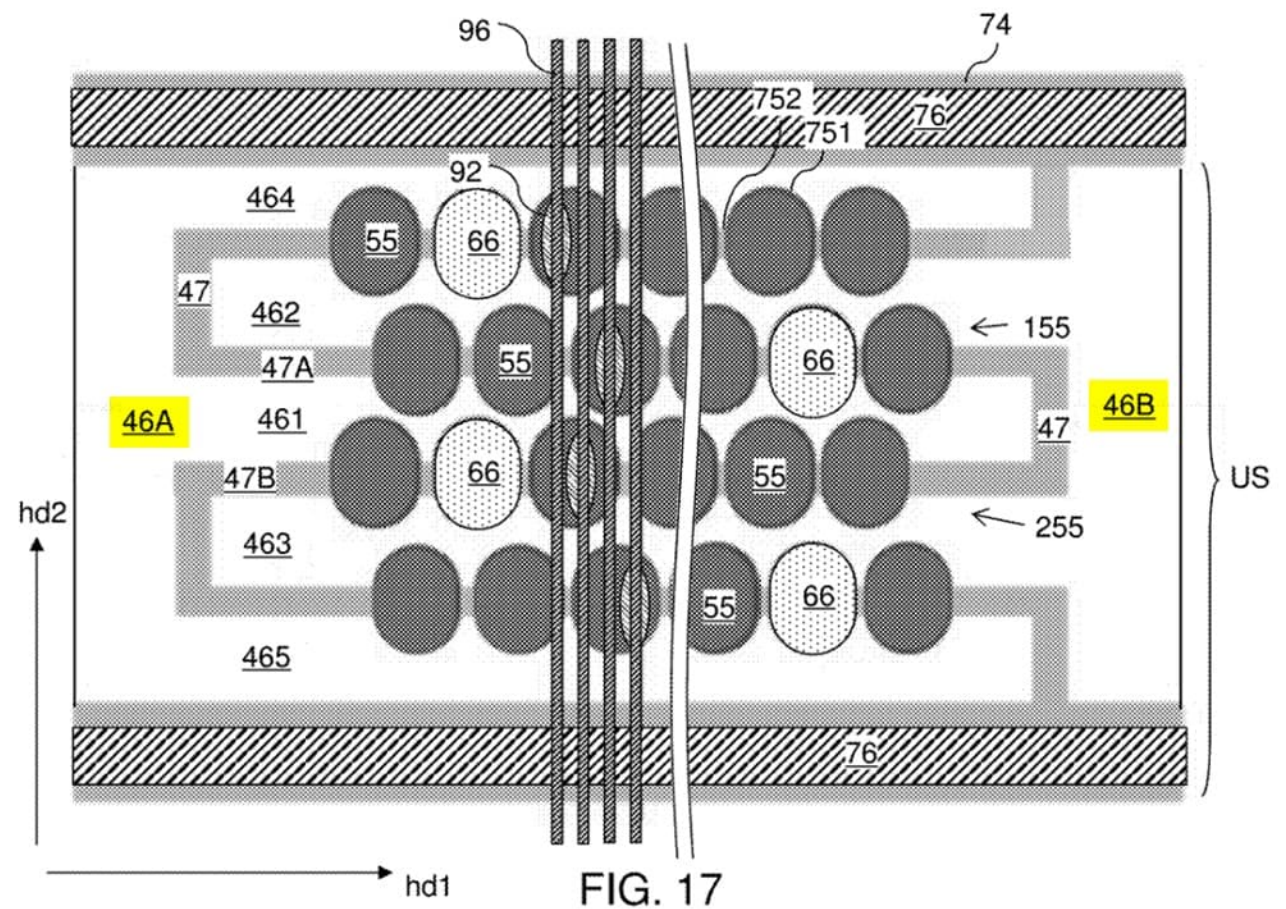


FIG. 17

Ex. 1046 (Nishikawa123), Fig. 17



'322 Patent

Circular TACs Would Not Have Been Obvious (Claims 6, 8-20)

Dummy Channels Would Not Have Been Obvious (Claims 3, 6, 14-18, 20)

Petitioner's Ribbed TAC Arguments Fail (Claims 13-18, 20)

Petitioner's Equal-Diameter Arguments Lack Merit (Claims 6, 9-10, 15-16)



Petitioner Has Not Met Its Burden Of Showing The Claimed Dummy Channels Were Obvious

Institution Decision

Because Petitioner has not shown the combined references to teach the claimed dummy channels of claim 14, Petitioner has not shown, by a reasonable likelihood, that claim 14 would have been obvious over Nishikawa or Nishikawa and Nishikawa123. Claims 3, 6, 15–18, and 20 also contain a “dummy channel” limitation. Consequently, we determine that Petitioner has not met its burden for claims 3, 6, 14–18, and 20.

ID 20



Petitioner Identifies Two Bases For Including Dummy Channels

Petitioner's Reply

2023) (“suitable”). As the Petition and Reply demonstrate, it is beyond dispute that (1) Nishikawa poses edge effect and stability problems, and (2) dummy channels were both a known and suitable option for addressing these problems.

Reply 13



Generalized Concerns About “edge effects” Are Not Enough

Institution Decision

We agree with Patent Owner. Although Dr. Lee attests that “it is common to refrain from using the cells at the array edge,” which are “sometimes referred to as dummy cells,” due to “processing variations,” this does not show an advantage to adding dummy channels. Ex. 1003 ¶ 141 (quoting Ex. 1024, 8:47–53). To the extent that Dr. Lee states that dummy

ID 19



Generalized Concerns About “edge effects” Are Not Enough

Dr. Lee's First Declaration

to as dummy cells.”). For modern processes, this has become even a greater issue. Ex. 1025 (U.S. Pat. 10,347,487 - Lee), 2:20-43 (“Edge of array issues may typically occur at the boundary between a chop mask and pitch double patterning. An abnormality at the edge of an array pattern can cause blowout or shorting issues, depending on the integration process. Conventionally, an abnormal edge pattern at the edge of array may be controlled by adding a dummy pattern region, which is later sacrificed in processing.”). Thus, one normally employs dummy channel structures at the edge of the array. Otherwise, these channel structures may be defective, and not properly store data.

Ex. 1003 (Lee Pet. Decl.) ¶ 141

Petitioner Relies On New References Not In Its Petition

Petitioner's Reply

Second, PO misstates Dr. Lee's testimony, suggesting that Dr. Lee recognizes that dummies are later sacrificed. Not so. Dr. Lee cited EX1025 to demonstrate the general principle of edge effects. Lee, ¶141. As EX1024, 8:47-53 and the above references (EX1108-EX1110) demonstrate, the typical and *suitable option* was to refrain from using the channels at the edge during operation (rendering them dummy channels). EX1111, Fig. 4B ("DUMMY MH" with no wiring); Lee2, ¶¶28-29.

Reply 14



Petitioner Relies On New References Not In Its Petition

Petition Exhibit List

Petition for Inter Partes Review of U.S. Patent No. 11,581,322

LISTING OF EXHIBITS

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent
1002	File History
1003	Declaration
1004	Curriculum
1005	U.S. Patent
1006	U.S. Patent
1007	U.S. Patent
1008	U.S. Patent
1009	U.S. Patent
1010	Michelson, "b"
1011	U.S. Patent
1012	U.S. Patent
1013	PCT Public
1014	U.S. Patent
1015	Arizono, "b"
1016	File History
1017	U.S. Patent ("Lee 2014")
1018	U.S. Patent al. ("Nishikawa")

Petition for Inter Partes Review of U.S. Patent No. 11,581,322

EXHIBIT NO.	DESCRIPTION
1019	U.S. Patent ("Lee 987")
1020	U.S. Patent al. ("Mason")
1021	U.S. Patent
1022	U.S. Patent
1023	U.S. Patent
1024	U.S. Patent
1025	U.S. Patent
1026	U.S. Patent
1027	U.S. Patent
1028	U.S. Patent
1029	U.S. Patent
1030	U.S. Patent
1031	U.S. Patent
1032	U.S. Patent
1033	U.S. Patent
1034	Wolf, "Silicon Technology"
1035	Wolf, "Silicon Technology"

Petition for Inter Partes Review of U.S. Patent No. 11,581,322

EXHIBIT NO.	DESCRIPTION
1036	U.S. Patent
1037	U.S. Patent
1038	Excerpt from the U.S. Pat. YMCB 2 A, October 2, 2 (PROTECT SEAL)
1039	U.S. Patent
1040	U.S. Patent
1041	U.S. Patent
1042	U.S. Patent
1043	Combined C Statistics (D https://www.fda.gov/oc/ohrt/combined-c-statistics)
1044	Plaintiff and Technology Assorted C1, 2, 2024 to 7, Mironi Tezi Group, LLC
1045	Docket from Mironi Tezi Group, LLC

Petition for Inter Partes Review of U.S. Patent No. 11,581,322

EXHIBIT NO.	DESCRIPTION
1046	U.S. Patent No. 9,935,123 to Nishikawa ("Nishikawa2")
1047	Printout, 11-26-2024, Bionomics (https://www.bionomics.com/science/genomics/) (d1qpw)

Exhibits Not Cited

Reply Exhibit List

Exhibit.

1001	U
1002	F
1003	D
1004	C
1005	U
1006	U
1007	U
1008	U
1009	U
1010	M
1011	U
1012	U
1013	P
1014	U
1015	A
1016	F
1017	U
1018	U
1019	U

Exhibit.

1020	U
1021	U
1022	U
1023	U
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1029	U
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1031	U
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1037	U

Exhibit.

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1042	M
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Exhibit.

1051	P
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1055	C
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1057	U
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1061	C
1062	C

Exhibit.

1063	L
1064	C
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1067	U
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1070	C
1071	U
1072	U

Exhibit.

1073	U
1074	U
1075	U
1076	U
1077	U
1078	U
1079	U
1080	U
1081	U
1082	U
1083	U

Exhibit.

1084	C
1085	U
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1090	U
1091	U
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1093	U
1094	U
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1096	U
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1100	U
1101	U

Exhibit.

1093	C
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1103	U
1104	U
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1243	U
1244	U
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1250	U

1108	U.S. Patent No. 11,043,507
1109	U.S. Patent Publication No. 2015/0029775A1
1110	U.S. Patent Publication No. 2019/0027434A1

Reply xii

xii

Petitioner's New References Also Can't Show Obviousness



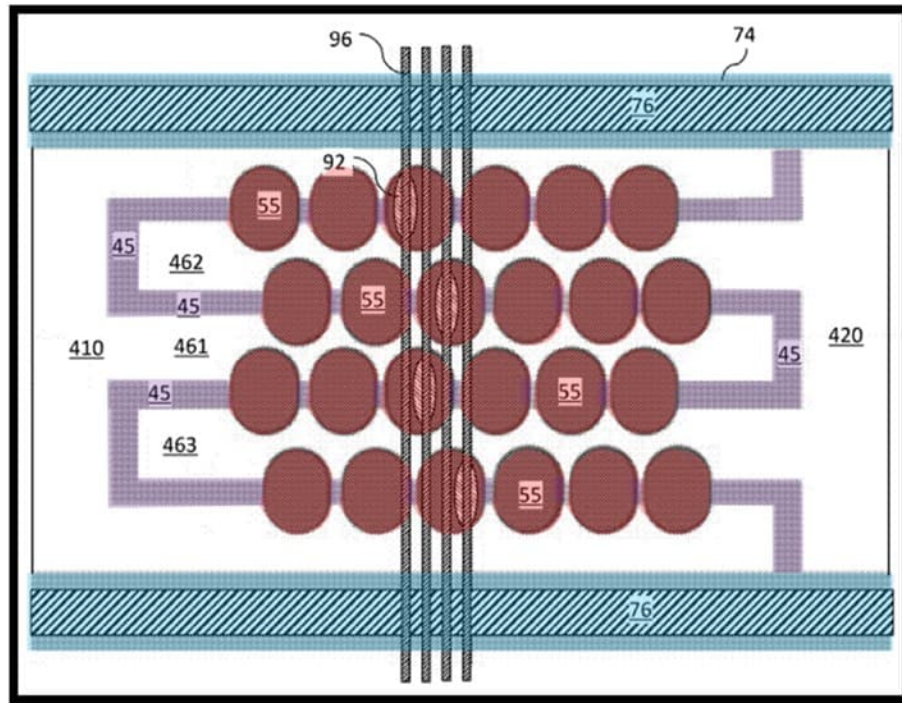
Virtek Vision International v. Assembly Guidance Systems

“The mere fact that these possible arrangements existed in the prior art does not provide a reason that a skilled artisan would have substituted the one-camera angular direction system in Keitler and Bridges with the two-camera 3D coordinate system disclosed in Briggs.”

Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc., 97 F.4th 882, 887 (Fed. Cir. 2024)

There Is No Room In Nishikawa's Memory Stack For Dummy Channels

Dr. Campbell's Second Declaration



Nishikawa Fig. 16 (annotated)

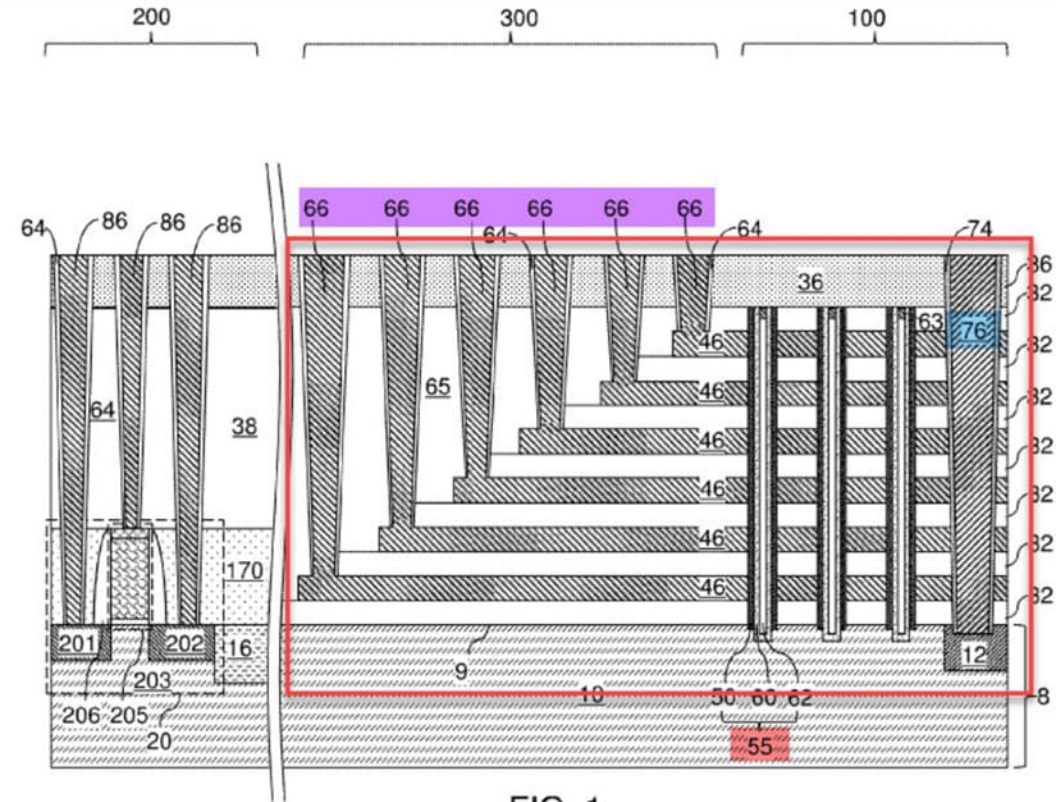


FIG. 1

Nishikawa Fig. 1 (annotated)

Ex. 2021 (Campbell POR Decl.) ¶ 97



Nishikawa's Design Already Provides Structural Support

Institution Decision

We also agree with Patent Owner's argument for point (3), that Nishikawa already discloses structures for providing structural support. Prelim. Resp. 9–10 (citing Ex. 1005, 10:10–12 (“Separator dielectric structures can provide structural support to the insulating layers 32 after formation of the interlayer cavities”)). We agree with Patent Owner that Petitioner does not address the support provided by these structures in Nishikawa, which is for the same purpose as Petitioner's added dummy channels; i.e., to support recesses caused by loss of sacrificial material during the gate replacement process. Prelim. Resp. 9–11; Pet. 60–63. To

ID 19-20

Nishikawa Already Has Structural Support

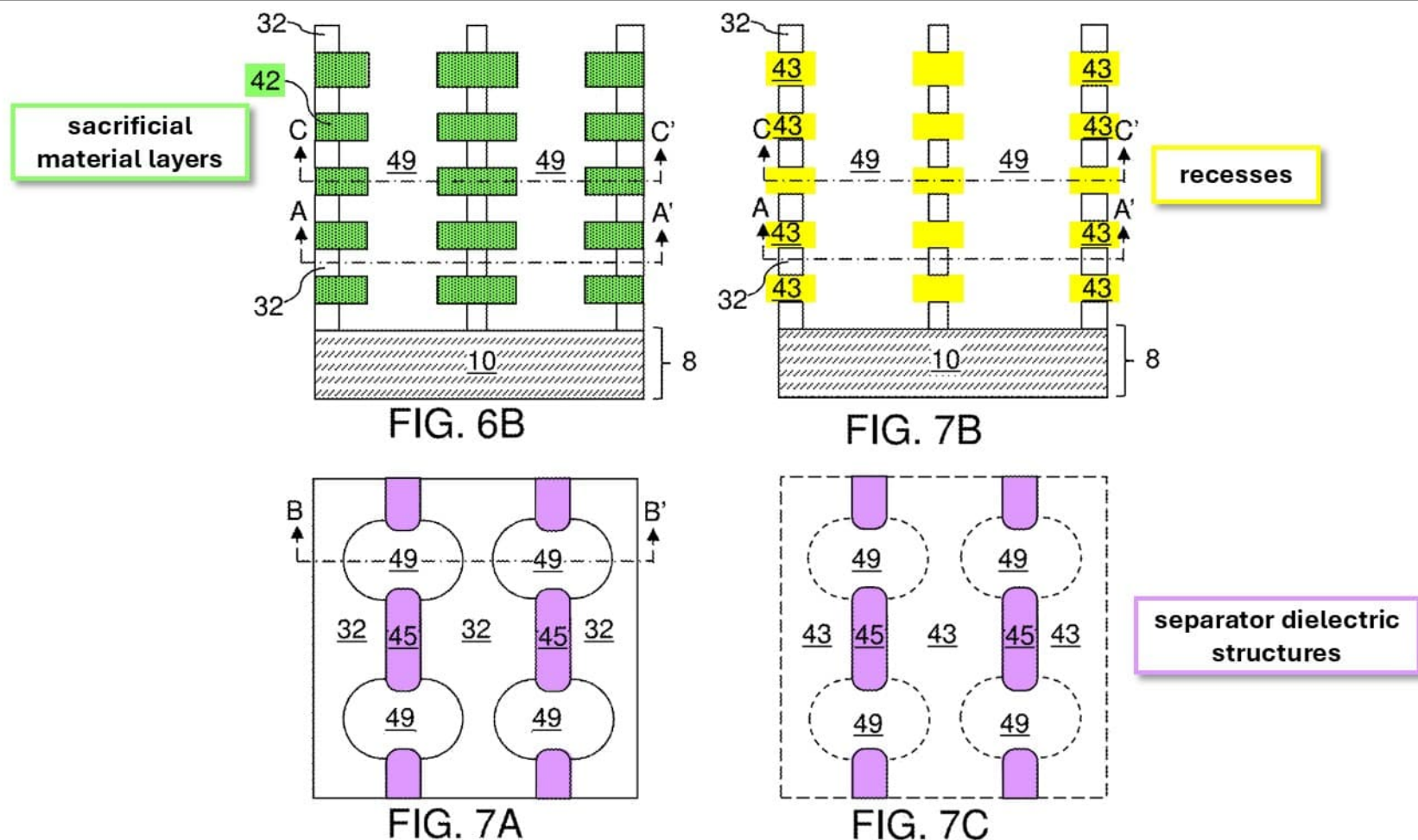
Nishikawa

An interlayer cavity (i.e., recess) 43 is formed at each level of the sacrificial material layers 42, and is connected to multiple memory openings 49. The separator dielectric structures 45 can provide structural support to the insulating layers 32 after formation of the interlayer cavities 43. Each interlayer cavity 43 may be located between a vertically neighboring pair of insulating layers 32. A planar bottom surface of an overlying insulating layer 32 and a planar top surface of an underlying insulating layer 32 can be physically exposed to each interlayer cavity 43.

Ex. 1005 (Nishikawa), 10:8-17

Nishikawa Already Has Structural Support

Nishikawa



Ex. 1005 (Nishikawa), Figs. 6B, 7A, 7B, 7C (annotated)

Nishikawa's Structural Support Extends Through The Stack

Nishikawa

The separator dielectric structures **45** extend through the stack, contact portions of outer sidewalls of the memory stack structures **55**, and laterally separate the control gate electrodes **46** of the plurality of charge storage elements (which are portions of the charge storage regions **54**). The patterned electrically conductive layers **46** comprise control gate electrodes of the multiple sets of at least two charge storage elements **54**. Each set of at least two charge storage elements comprises two regions located within a continuous portion of a charge trapping layer located at the same level.

Ex. 1005 (Nishikawa), 17:14-23

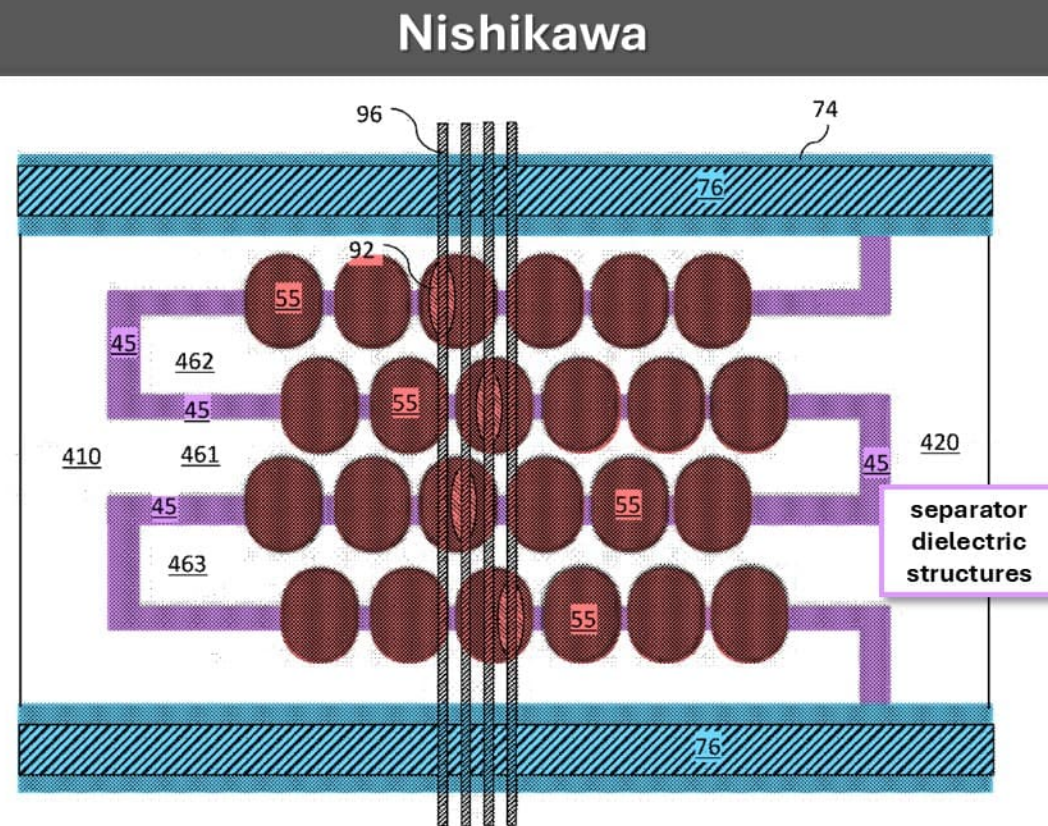


FIG. 16

Ex. 1005 (Nishikawa), Fig. 16 (annotated)

Petitioner's Reply

No separator

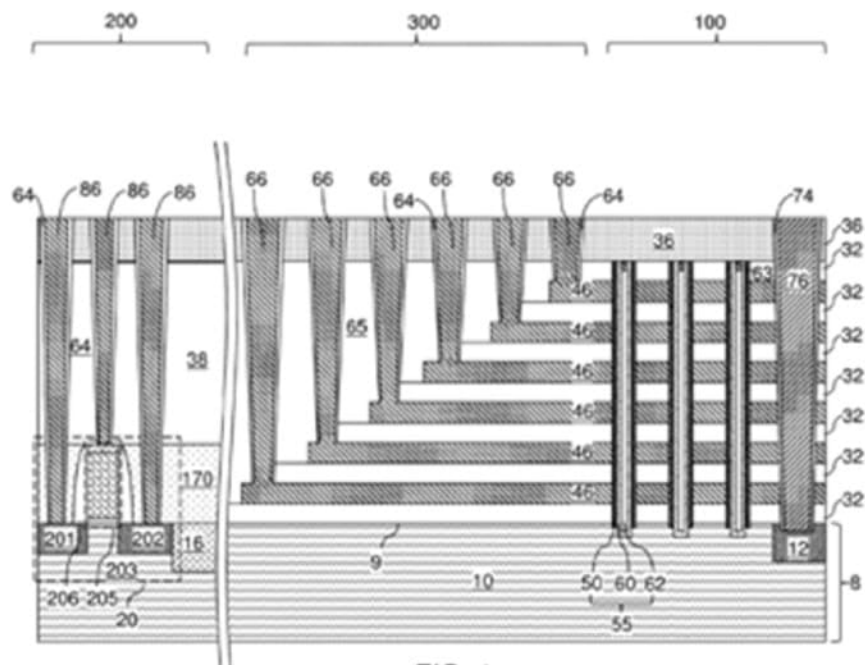
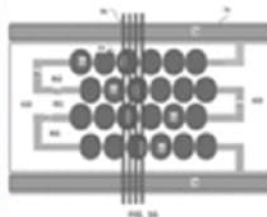


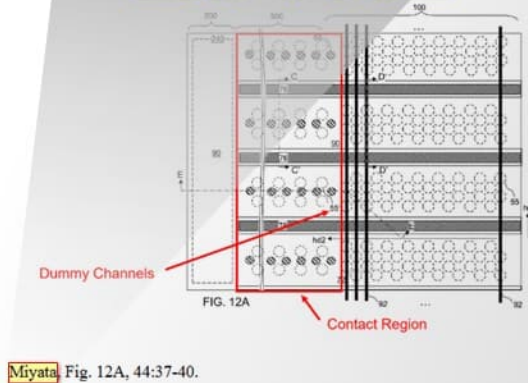
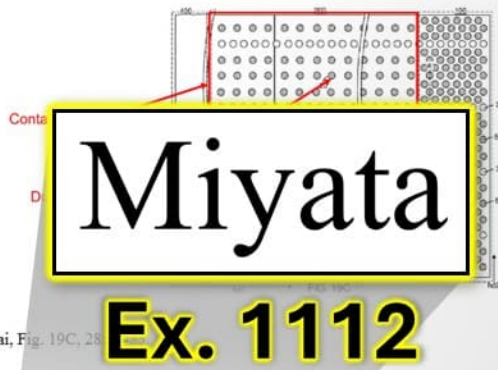
FIG. 1

Reply 16



Petitioner Again Relies On New References Not Cited In Petition

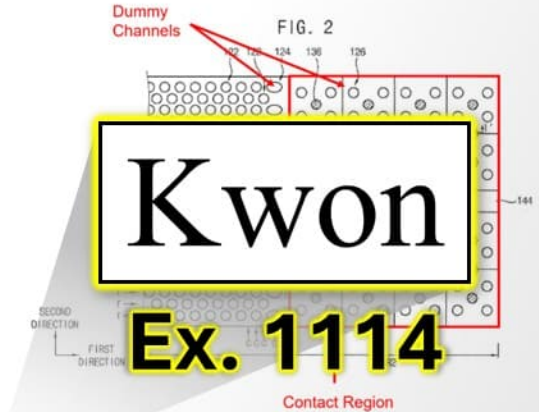
Petitioner's Reply



18



19



Kwon [0032], Fig. 2; Lee2, ¶¶33-37.

PO takes issue with the Petition's citation to Masamori, Kai, Park297, and Kim559 that show support structures throughout the device, because Nishikawa allegedly only has an array. POR, 50-54. Nishikawa is a full device and would benefit from support throughout its device just like these references. This "additional structural support," e.g., is shown in Masamori632, employing dummy channels from the array edge into the connection region:

20

Reply 18-20



Petitioner Again Relies On New References Not Cited In Petition

Petition Exhibit List

Petition for Inter Partes Review of U.S. Patent No. 11,581,322

LISTING OF EXHIBITS

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent
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1007	U.S. Patent
1008	U.S. Patent
1009	U.S. Patent
1010	Michaelson
1011	U.S. Patent
1012	U.S. Patent
1013	PCT Public
1014	U.S. Patent
1015	Actonius, "b
1016	File History
1017	U.S. Patent
1018	U.S. Patent
1019	U.S. Patent

Petition for Inter Partes Review of U.S. Patent No. 11,581,322

EXHIBIT NO.	DESCRIPTION
1019	U.S. Patent
1020	U.S. Patent
1021	U.S. Patent
1022	U.S. Patent
1023	U.S. Patent
1024	U.S. Patent
1025	U.S. Patent
1026	U.S. Patent
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1028	U.S. Patent
1029	U.S. Patent
1030	U.S. Patent
1031	U.S. Patent
1032	U.S. Patent
1033	U.S. Patent
1034	U.S. Patent
1035	U.S. Patent

Petition for Inter Partes Review of U.S. Patent No. 11,581,322

EXHIBIT NO.	DESCRIPTION
1036	U.S. Patent
1037	U.S. Patent
1038	U.S. Patent
1039	U.S. Patent
1040	U.S. Patent
1041	U.S. Patent
1042	U.S. Patent
1043	U.S. Patent
1044	U.S. Patent
1045	U.S. Patent

Petition for Inter Partes Review of U.S. Patent No. 11,581,322

EXHIBIT NO.	DESCRIPTION
1046	U.S. Patent No. 9,935,123 to Nishikawa ("Nishikawa")
1047	Printout, 11-25-2024, Technics (https://www.technics.com/science/gemetry/) (allpages)

Exhibits Not Cited

Reply Exhibit List

Exhibit

1001	U
1002	F
1003	D
1004	C
1005	U
1006	U
1007	U
1008	U
1009	U
1010	M
1011	U
1012	U
1013	P
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1016	F
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1061	C
1062	S

Exhibit

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Exhibit

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Exhibit

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1114	U
1115	U
1116	U

Exhibit

1107	Additional excerpts from Wolf, "Silicon Processing for the VLSI Era, Volume 1-Process Technology," Lattice Press (1986).
1108	U.S. Patent No. 11,043,307
1109	U.S. Patent Publication No. 2015/0029775A1
1110	U.S. Patent Publication No. 2019/0027434A1
1111	U.S. Patent No. 10,115,737 ("Iwase")
1112	U.S. Patent No. 9,449,987 ("Miyata")
1113	U.S. Patent No. 9,929,174 ("Mizutani")
1114	U.S. Patent Publication No. 2019/035942A1 ("Kwon")
1115	U.S. Patent Publication No. 2018/0190540 ("Liu")
1116	PCT Publication No. WO 2019/06820A1

1112	U.S. Patent No. 9,449,987 ("Miyata")
1113	U.S. Patent No. 9,929,174 ("Mizutani")
1114	U.S. Patent Publication No. 2019/035942A1 ("Kwon")

Reply xii



The Petition Never Relied On Nishikawa123 For Dummy Channels

Petitioner's Reply

But PO wholly ignores the Petition's showing that aside from support, the memory holes (and dummy holes) alternatively are suitable for introducing the etchant and metal during gate replacement. **Pet., 51.** Nishikawa2 also expressly discloses using

Reply 22



The Petition Never Relied On Nishikawa123 For Dummy Channels

Petition for *Inter Partes* Review of U.S. Patent No. 11,581,322

X. GROUND 1: NISHIKAWA IN VIEW OF THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 1-3, 6-10, 13-16, AND 19-20	34
A. Claim 1:	34
1. [1.PRE] "A three-dimensional (3D) memory device, comprising:"	34
2. [1.A] "a substrate;"	34
3. [1.B] "a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;"	35
4. [1.C] "a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;"	36
5. [1.D] "a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate; and" ...	39
6. [1.E] "a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones."	53
B. Claim 2:	57
1. [2] "The 3D memory device of claim 1, further comprising: a peripheral device on the substrate, a peripheral contact being arranged outside of the memory stack and in contact with the peripheral device."	57
C. Claim 3:	59
1. [3.PRE] "The 3D memory device of claim 2, further comprising:"	59
2. [3.A] "a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack." ..	59
3. [3.B] "wherein each of the dielectric layer in the dummy channel structure, a spacer in the TAC, and a spacer in the peripheral contact comprises silicon oxide."	65
D. Claim 6:	66

-ii-

Petition

X. GROUND 1: NISHIKAWA IN VIEW OF THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 1-3, 6-10, 13-16, AND 19-20	34
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6. [1.E] "a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones."	53

Pet. ii

The Petition Never Relied On Nishikawa¹²³ For Dummy Channels

Petition

need for the large trench. Lee, ¶ 125. Nishikawa provides two options for the gate replacement process: either through the backside trenches or the memory hole openings. Nishikawa, 6:29-44, 9:58-10:8. Moreover, the prior art described above

Pet. 51



'322 Patent

Circular TACs Would Not Have Been Obvious (Claims 6, 8-20)

Dummy Channels Would Not Have Been Obvious (Claims 3, 6, 14-18, 20)

Petitioner's Ribbed TAC Arguments Fail (Claims 13-18, 20)

Petitioner's Equal-Diameter Arguments Lack Merit (Claims 6, 9-10, 15-16)



Petitioner Has Not Met Its Burden Of Showing That Ribbed TACs Were Obvious

Institution Decision

Because Petitioner has not shown the combined references to teach the claimed diameters of claim 14, Petitioner has not shown, by a reasonable likelihood, that claim 14 would have been obvious over Nishikawa or Nishikawa and Nishikawa123. Claims 15–18 and 20 also contain a “dummy channel” limitation. Consequently, we determine that Petitioner has not met its burden for claims 13–18 and 20.

ID 22

Petitioner Originally Said Ribbed TACs Were Obvious Because They Were Known

Petition

Nishikawa renders this limitation obvious in view of the knowledge of a POSITA. It was well known that an option for a TAC or other through-memory structures was to have a ribbed shape, that is, forming recesses in one of the stack layers. For example, Cui discloses contacts 183 that travel through the staircase and through the entire array. Ex. 1037 (Cui), Fig. 14A, 25:51-53 (e.g., 183 contact on

Pet. 75



The Only Reason Petitioner Provided For The Modification Was From The '322 Patent

Petition

The ribbed via cavity serves the same purpose as the '322 Patent, namely, providing additional area for the dielectric liner. Ex. 1001, 13:38-51. In other words, there is additional space for the insulating spacer that surrounds the through-via. Ex. 1037 (Cui), 27:54-28:8. Accordingly, in view of the knowledge of a POSITA, it would have been obvious, and a POSITA would have been motivated, to create a ribbed via cavity in Nishikawa's through-array via holes. First, it was known to

Pet. 77



The Board Already Found That The Petition's Motivation Was Improper Hindsight

Institution Decision

¶ 129). However, neither Petitioner nor Dr. Lee explain why this additional area is advantageous, except that it serves the same purpose as the lateral recesses in the '322 patent. Ex. 1003 ¶ 173. But a reason to combine should not be obtained solely from the challenged patent. *KSR*, 550 U.S. at 421 (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”); *Metalcraft of Mayville, Inc. v. Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) (“[W]e cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention.”).

ID 21

On Reply, Petitioner Pivoted To A New “short circuit” Motivation

Petitioner's Reply

In sum, the record demonstrates that it was known that ribbed cavities create extra room to mitigate short-circuits and the capacitive coupling of conductor pairs.

PO does not (and cannot) dispute that Nishikawa teaches a conductive TAC. Thus, the ribbed cavities provide a well-known technique to address a problem (possible short circuits and isolation) that Nishikawa indisputably has. As such, the ribbed cavities are obvious.

Reply 31



Petitioner's New Argument Again Relies On New Evidence

Petitioner's Reply

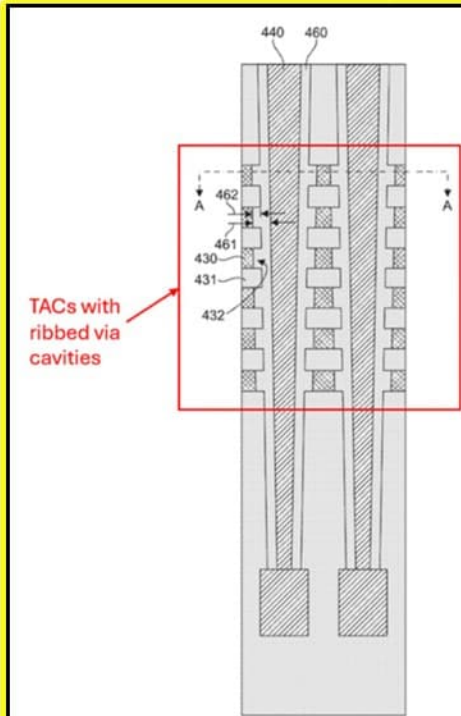


FIG. 7

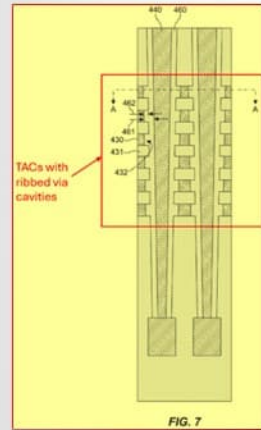


FIG. 7

[0048] ("conductive layers 430 can be recessed proximate contacts 440 such that material of insulative layers 431 is closer to the contacts 440 than the material of the conductive layers 430"). Notably, Liu discloses that "[r]ecesses can be included if additional isolation from the contacts 440 is desired" and "[i]n general, it is desirable to minimize capacitor coupling as much as possible." *Id.* Thus, it is desirable to have the recess to minimize capacitor coupling. Lilak, too, recesses conductive gates to create a longer path between the vertical wordlines around the dielectric layers to avoid leakage current in a 3D memory.

30

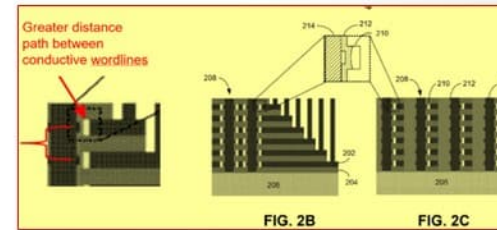


FIG. 2B

FIG. 2C

EX1116, 2B-2C, 7:12-17 ("Also, in the embodiment shown, the first conductive layers 202 are recessed from the etch pits 208 to increase leakage current suppression."). Lee2, ¶¶48-50.

In sum, the record demonstrates that it was known to provide extra room to mitigate short-circuits and the capacitive coupling. PO does not (and cannot) dispute that Nishikawa teaches that the ribbed cavities provide a well-known technique to avoid short circuits and isolation) that Nishikawa indisputably teaches that cavities are obvious.

PO admits that the '322 patent fails to explain the obviousness, because the '322 patent's silence demonstrates that PO is more than capable of selecting between the [se] known methods...." *Uber Techs.*,

31

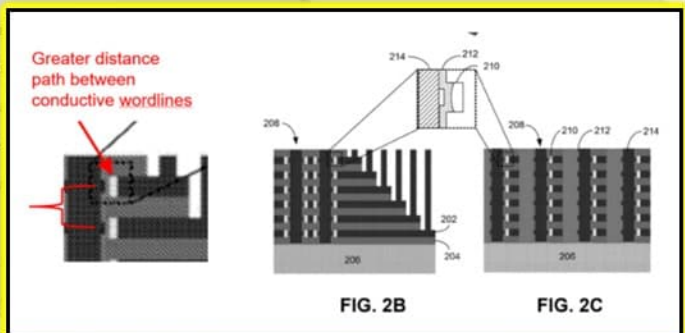


FIG. 2B

FIG. 2C

Ex. 1115**Ex. 1116**

Reply 30-31



Petitioner's New Argument Again Relies On New Evidence

Petition Exhibit List

Petition for Inter Partes Review of U.S. Patent No. 11,581,322

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1011	U.S. Patent
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1013	PCT Public
1014	U.S. Patent
1015	Actonius, "b
1016	File History
1017	U.S. Patent
1018	U.S. Patent

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1027	U.S. Patent
1028	U.S. Patent
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1031	U.S. Patent
1032	U.S. Patent
1033	U.S. Patent
1034	U.S. Patent
1035	U.S. Patent

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1044	U.S. Patent
1045	U.S. Patent

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Exhibits Not Cited

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Exhibit

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1005	U
1006	U
1007	U
1008	U
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1016	F
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1019	U

Exhibit

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Exhibit

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Exhibit

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1083	V
1084	A
1085	C
1086	H
1087	D
1088	U
1089	D
1090	A
1091	C
1092	C
1093	C
1094	D
1095	D
1096	O
1097	C
1098	O
1099	I
1100	C
1101	M
1102	D
1103	C
1104	C
1105	C
1106	C
1107	C
1108	C
1109	C
1110	C
1111	C
1112	C
1113	C
1114	C
1115	C
1116	C

Exhibit

Exhibit	Description
1107	Additional excerpts from Wolf, "Silicon Processing for the VLSI Era, Volume 1-Process Technology," Lattice Press (1986).
1108	U.S. Patent No. 11,043,307
1109	U.S. Patent Publication No. 2015/0029775A1
1110	U.S. Patent Publication No. 2019/0027434A1
1111	U.S. Patent No. 10,115,737 ("Iwata737")
1112	U.S. Patent No. 9,449,987 ("Myata")
1113	U.S. Patent No. 9,929,174 ("Mizutani")
1114	U.S. Patent Publication No. 2019/035942A1 ("Kwon")
1115	U.S. Patent Publication No. 2018/0190540 ("Liu")
1116	PCT Publication No. WO 2019/066829A1

1115 U.S. Patent Publication No. 2018/0190540 ("Liu")

1116 PCT Publication No. WO 2019/066829A1

Reply xii

Petitioner's New Argument Still Derives From The '322 Patent

TAC 136 can include a vertical opening through memory stack 104 and that is filled with filling materials. In some embodiments, TAC 136 includes a spacer 138 on a sidewall of the opening and a conductor layer 140 in contact with spacer 138 in the opening. Conductor layer 140 can include conductive materials, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Spacer 138 can electrically insulate conductor layer 140 of TAC 136 from surrounding conductor layers 110 in memory stack 104. In some embodiments, TAC 136 has a substantially circular shape in the plan view, and conductor layer 140 and spacer 138 are disposed radially from the center of TAC 136 in this order. Spacer 138 of TAC 136 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

Ex. 1001 ('322 Patent), 8:47-62



Petitioner's "unintentional recesses" Argument Also Fails

Petition

oxide and silicon nitride layers does not have the exact same selectivity towards each of silicon oxide and silicon nitride, and will result in uneven sidewalls, such that there are recesses in either the oxide layers or the sacrificial layers. Ex. 1039, (U.S. Pat. 11,075,084), 2:59-67 (In "3D NAND memory, it is important to have an etching gas which can etch both SiO₂ and SiN layers (or both SiO₂ and p-Si layers) without selectivity. In another words, *it is a challenge to find an etch gas that has similar high etch rates of SiO₂ and SiN in terms of getting a smooth sidewall* of high aspect ratio holes in 3D NAND memory."); Lee, ¶ 170. Thus, under PO's apparent

Pet. 74



The Board Recognized The Petition's Failure

Institution Decision

11,075,084)). Petitioner asserts that unintentional recesses are formed during etching because “it is a challenge to find an etch gas . . . in terms of getting a smooth sidewall of high aspect ratio holes in 3D NAND memory.” *Id.* at 74 (quoting Ex. 1039, 2:59–67); Ex. 1003 ¶ 170. However, Petitioner admits that same reference states that “it is important to have an etching gas which can etch both . . . layers without selectivity” to result in “a smooth sidewall.” Pet. 74 (quoting Ex. 1039, 59–67). Thus, Petitioner’s assertion that a person having ordinary skill in the art would seek to use etches that would result in the claimed first and second diameters is insufficiently supported.

ID 21-22



The Law Does Not Permit The Inherency Argument Petitioner Advances



PAR Pharmaceutical v. TWI Pharmaceuticals

“A party must, therefore, meet a high standard in order to rely on inherency to establish the existence of a claim limitation in the prior art in an obviousness analysis—the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed in the prior art.”

PAR Pharm., Inc. v. TWI Pharms., Inc., 773 F.3d 1186, 1195-96 (Fed. Cir. 2014)



'322 Patent

Circular TACs Would Not Have Been Obvious (Claims 6, 8-20)

Dummy Channels Would Not Have Been Obvious (Claims 3, 6, 14-18, 20)

Petitioner's Ribbed TAC Arguments Fail (Claims 13-18, 20)

Petitioner's Equal-Diameter Arguments Lack Merit (Claims 6, 9-10, 15-16)



There Is No Dispute That Nishikawa Does Not Disclose Equal-Diameter Contacts

Petition

4. [6.C] “wherein: a diameter of the TAC is at least equal to a diameter of the peripheral contact; and”

Nishikawa in view the knowledge of a POSITA renders this limitation obvious.

Pet. 67

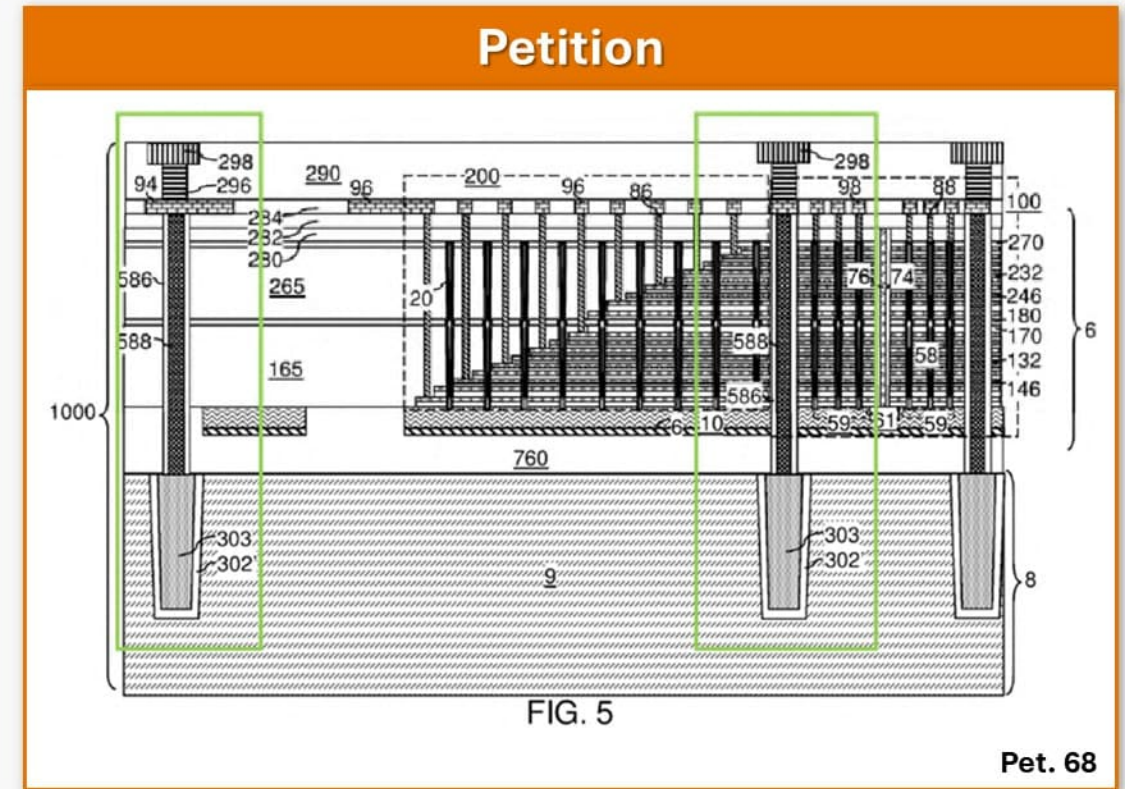


Petitioner Does Not Identify A Single Reference That Explicitly Discloses Equal-Diameter Contacts

Petition

specifically in the 3D memory space as well. For example, Mushiga discloses forming, at the same time, through-array contacts (588) having the same size and using the same processing steps:

Pet. 68



Petitioner Does Not Identify A Single Reference That Explicitly Discloses Equal-Diameter Contacts

Petition

Ex. 1012 (Mushiga), Fig. 5, 10:31-58; Lee, ¶¶ 160-61. As another example Nakajima discloses forming holes H1 through the stack for its TAVs (C4). One C4 structure is outside of the stack (on the right below):

Pet. 68

Petition

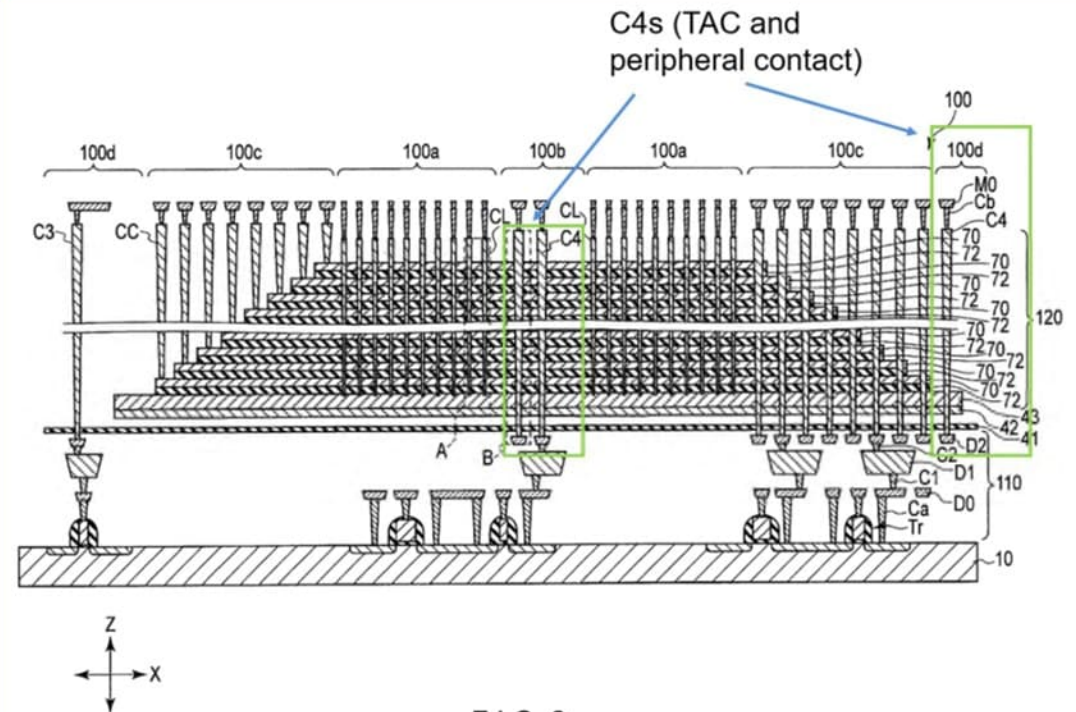
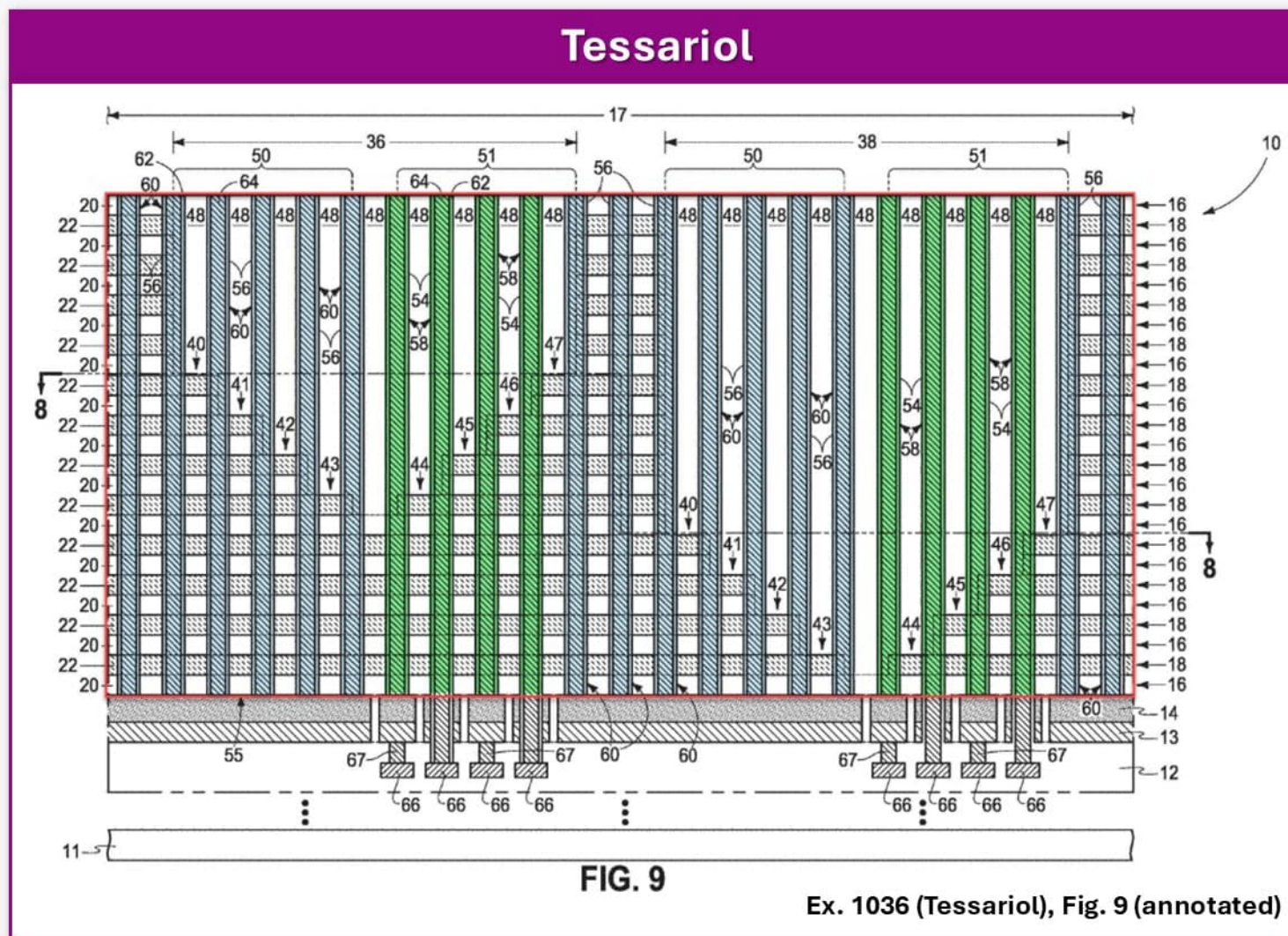


FIG. 2

Pet. 69

Petitioner Does Not Identify A Single Reference That Explicitly Discloses Equal-Diameter Contacts





Petitioner Does Not Identify A Single Reference That Explicitly Discloses Equal-Diameter Contacts

Petition

A POSITA would have been motivated to make the TAC and peripheral contacts the same size to employ a common process (including the hole size in masking steps) when forming the contacts. As can be seen above, this is precisely

Pet. 69



Petitioner Cannot Rely On Figures Alone To Establish Relative Dimensions



Nystrom v. TREX Co.

“The district court erred in not properly applying the principles set forth in our prior precedents that arguments based on drawings not explicitly made to scale in issued patents are unavailing.”

Nystrom v. TREX Co., Inc., 424 F.3d 1136, 1149 (Fed. Cir. 2005)

Petitioner's "same process, same diameter" Argument Relies On A False Premise

Petition

One common textbook approach was to make contacts the same size. Ex. 1035 (Wolf Vol. 2), 33. Using the same contact size was known and standard specifically in the 3D memory space as well. For example, Mushiga discloses

* * *

time (i.e., simultaneously)”), Fig. 9. But if the holes sizes are different, then modifications to the etch chemistries are necessary. E.g., Ex. 1035 (Wolf Vol. 2), 33; Lee, ¶ 162. Because of this well-known benefit, process technologies, e.g., etch chemistries, that achieve simultaneous etching of different holes had become textbook material before the '322 Patent was filed. *Id.*

Pet. 68, 70



Petitioner's "same process, same diameter" Argument Relies On A False Premise

Wolf, Volume 2

As the contact hole size decreases below 1 μm there is a strong decrease in etch rate with contact size dimension. To avoid long overetch times, contact holes of identical dimension would need to be used if this problem was not solved. Reference 156 describes a dry-etch process which overcomes this limitation. By adding 10% Cl_2 to a CHF_3 plasma the effective fluorine to carbon ratio in small holes is kept constant, maintaining uniform etch rates, independent of contact hole size. Nevertheless, it is very common that only one contact size is used. Larger contacts are implemented with multiple contact windows.

Ex. 1035, 33