

Micron Technology, Inc.
Petitioner
v.
Yangtze Memory Technologies Company, Ltd.
Patent Owner

Case No. IPR2025-00191
U.S. Patent No. 11,581,322

Micron's Hearing Demonstratives

April 27, 2026

Table of Abbreviations

Abbreviation	Description / Exhibit No.
'322 Patent	U.S. Patent No. 11,581,322 to Guo et al. (Ex. 1001)
Cui	U.S. Patent No. 10,304,852 (Ex. 1037)
Iwai	U.S. Patent No. 10,347,654 (Ex. 1022)
Kim559	U.S. Patent Publication No. 2018/0308559 (Ex. 1029)
Kwon	U.S. Patent Publication No. 2019/0035942 (Ex. 1114)
Liu	U.S. Patent Publication No. 2018/0190540 (Ex. 1115)
Lu	U.S. Patent No. 9,853,046 to Lu et al. (Ex. 1006)
Mushiga	U.S. Patent No. 10,354,980 (Ex. 1012)
Mizutani	U.S. Patent No. 9,929,174 (Ex. 1113)
Nakajima	U.S. Patent No. 10,777,501 to Nakajima et al. (Ex. 1009)
Nishikawa	U.S. Patent No. 9,837,431 to Nishikawa et al. (Ex. 1005)
Nishikawa2	U.S. Patent No. 9,935,123 to Nishikawa (Ex. 1046)
Tessariol	U.S. Patent Publication No. 2019/0081061 (Ex. 1036)

Claim 1

1. A three-dimensional (3D) memory device, comprising:
a substrate;
a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;
a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;
a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate; and
a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones.

Claim 3

3. The 3D memory device of claim 2, further comprising:
a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack, wherein each of the dielectric layer in the dummy channel structure, a spacer in the TAC, and a spacer in the peripheral contact comprises silicon oxide.

Claim 6

6. The 3D memory device of claim 1, further comprising:
a dummy channel structure filled with a dielectric layer
and extending vertically through the conductor/dielectric layer pairs in the memory stack; and
a peripheral contact arranged outside the memory stack
and in contact with a peripheral device on the substrate,
wherein:
a diameter of the TAC is at least equal to a diameter of the
peripheral contact; and
a diameter of the dummy channel structure is smaller than
each of a diameter of the TAC and a diameter of the
peripheral contact.

Claim 8

8. A three-dimensional (3D) memory device, comprising:
a substrate;
a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;
a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack; and
a through array contact (TAC) comprising a substantially circular section and extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate.

Road Map

- I. The IPR Grounds
- II. The '322 Patent
- III. State of the Art
- IV. Grounds 1 & 3: Nishikawa alone or in view of Nishikawa2

* No unique disputes as to Grounds 2 & 4.

Instituted Grounds

Ground	Prior Art	Claims
1	Nishikawa	~~1, 2, 3~~ , 6, 7, 8-10, 13-16, and 19-20 are obvious
2	Nishikawa + Lu	~~4-5~~ , 11-12, and 17-18 are obvious
3	Nishikawa + Nishikawa2	~~1, 2, 3~~ , 6, 7, 8-10, 13-16, and 19-20 are obvious
4	Nishikawa + Nishikawa2 + Lu	~~4-5~~ , 11-12, and 17-18 are obvious

Petition (Paper 1), 10.

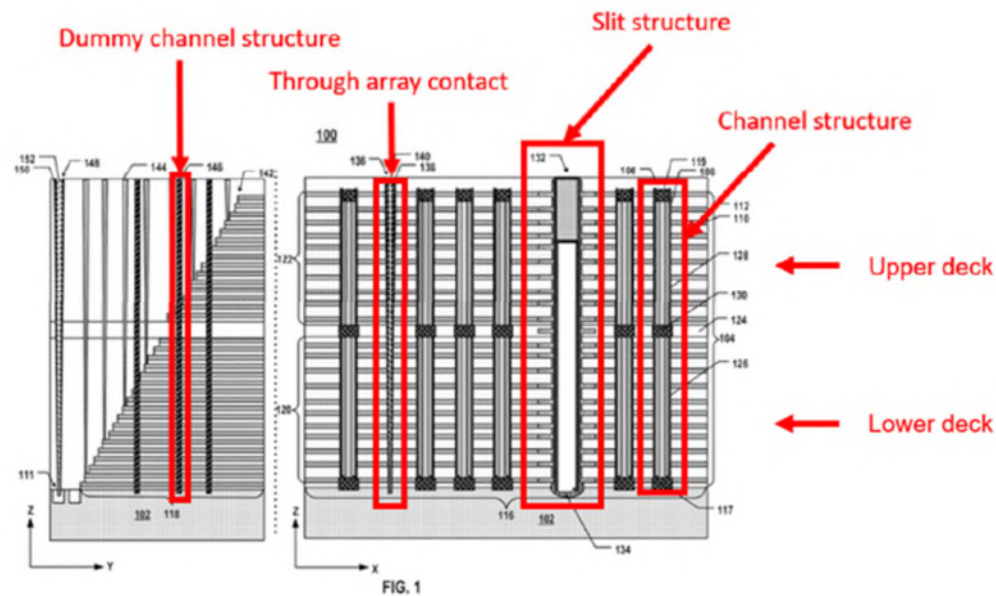
- No unique disputes as to Grounds 2 and 4.
- Patent Owner Disclaimed claims 1-2, 4-5, and 7.

Road Map

- I. The IPR Grounds
- II. The '322 Patent
- III. State of the Art
- IV. Grounds 1 & 3: Nishikawa alone or in view of Nishikawa2

The '322 Patent

- The '322 Patent relates to a 3D memory device with, e.g., a buried through-array contact ("TAC") and slit structure.



'322 Patent, Fig. 1 (Petition (Paper 1), 22).

The '322 Patent: Reason for Allowance

- The Reason for Allowance cites the (1) TAC and slit structures and (2) circular TAC as the features that allegedly distinguish the prior art.

5. Regarding claim 1, the known prior art does not teach the claim as a whole. In particular, the prior art does not disclose or fairly suggest the limitations: “a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate”; and “a slit structure extending vertically through the conductor/dielectric layer pairs in the memory stack and configured to separate the memory stack into a plurality of memory zones” in combination with the remaining limitations called for in claim 1.

7. Regarding claims 10 and 17, the known prior art does not teach the claim as a whole. In particular, the prior art does not disclose or fairly suggest the limitations: “a through array contact (TAC) comprising a substantially circular section and extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a spacer along a sidewall of the TAC and a conductor layer in contact with the spacer in the TAC and the substrate” in combination with the remaining limitations called for in claims 10 and 17.

8. None of the prior art on record contains such a limitation, nor given the prior art on record is it obvious to one of ordinary skill in the art to add said limitations as called for in claims 10 and 17. Therefore, claims 10 and 17 are allowed as it is not anticipated by or obvious over the teachings of the prior art on record. Furthermore, claims 11-12, 14-16 and 18-23 are also allowed as they depend from the allowed bases claim.

Ex. 1002, 249-50 (Petition (Paper 1), 26-27).

Road Map

- I. The IPR Grounds
- II. The '322 Patent
- III. State of the Art
- IV. Grounds 1 & 3: Nishikawa alone or in view of Nishikawa2

Circular "Contacts" Were Textbook Material

- The Petition demonstrates that circular contacts were textbook material.
- Circular contacts that provide a source connection (the function that Nishikawa's TACs provide) were also textbook material.

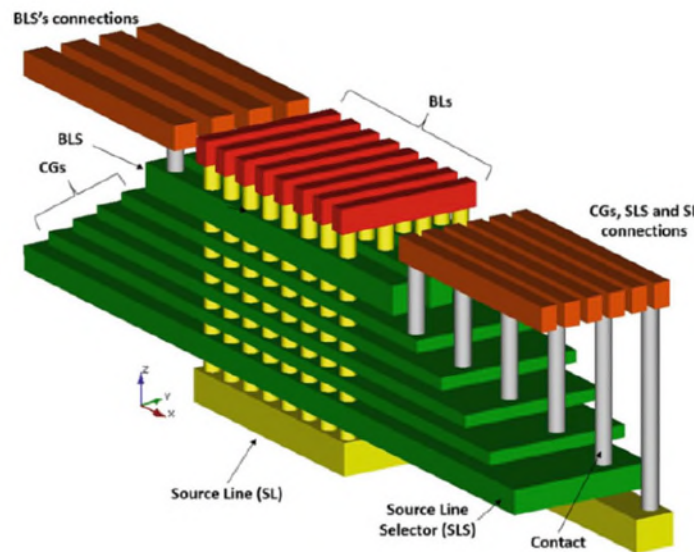


Fig. 4.13 Top bird's eye view of BiCS with gate connections

Ex. 1010, 109 (Petition (Paper 1), 15-16).

Circular Through-Array Contacts (TACs) Were Well Known in the Art

- The Petition demonstrates that circular TACs were well known in the prior art.

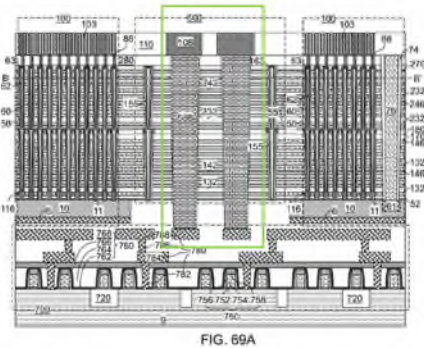


FIG. 69A

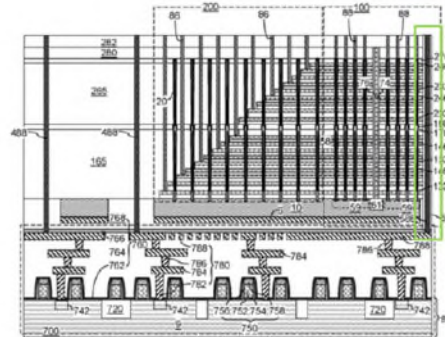
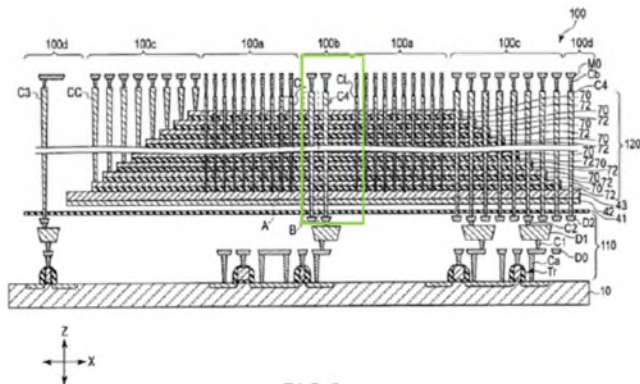


FIG. 16A



Slits Were Textbook Material

- The Petition demonstrates that slit structures to divide the array were textbook material.

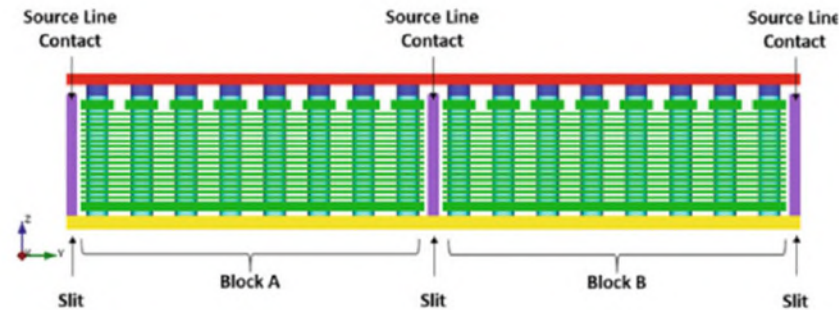


Fig. 6.8 Side view of Fig. 6.7

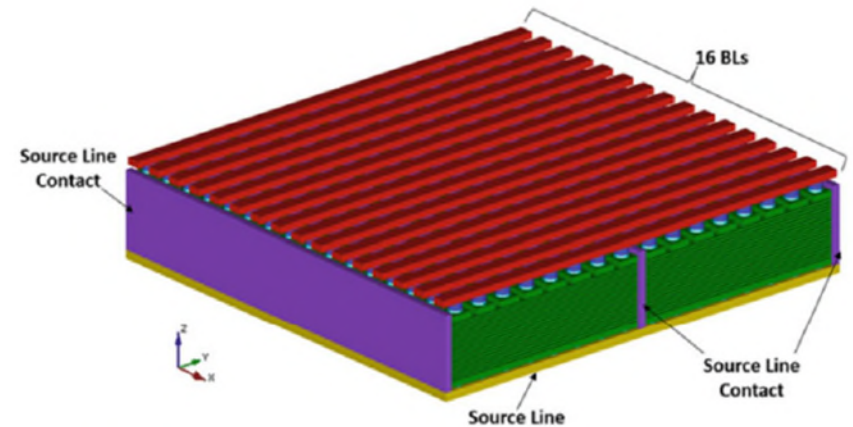


Fig. 6.7 Array slits

Ex. 1010, Figs. 6.7-6.8 (Petition (Paper 1), 20).

Road Map

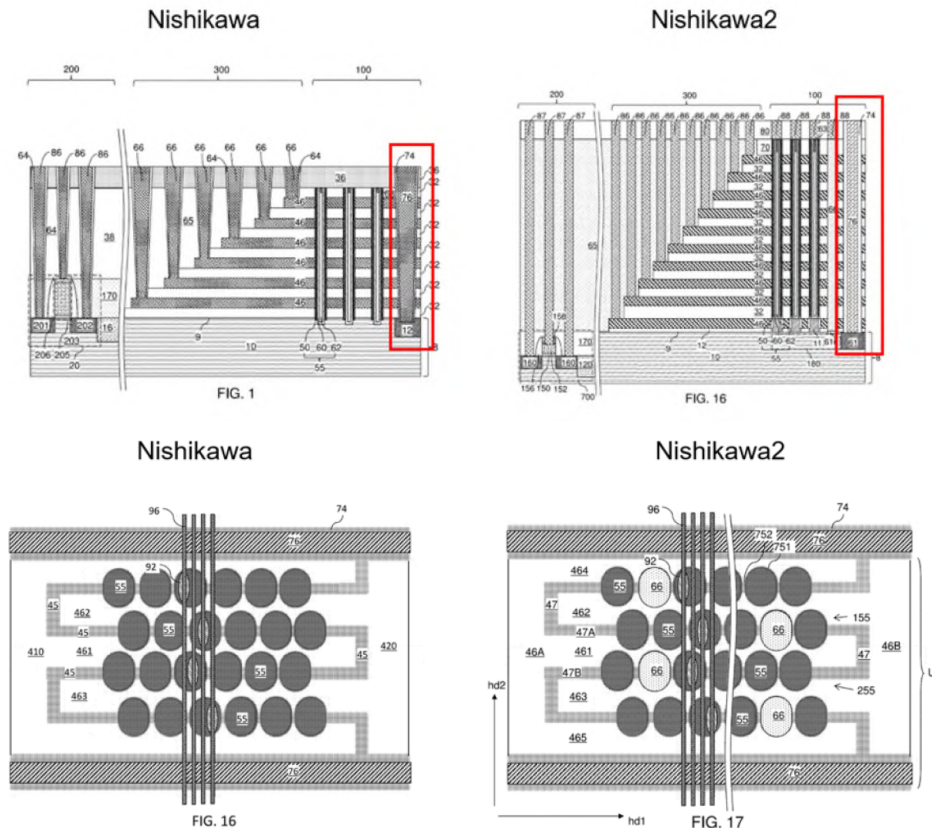
- I. The IPR Grounds
- II. The '322 Patent
- III. State of the Art
- IV. Grounds 1 & 3: Nishikawa alone or in view of Nishikawa2
 - A. A Circular TAC Was Obvious (claims 8-20)
 - B. The Addition of Dummy Channels Was Obvious (claims 3, 6, 14-20)
 - C. A Ribbed TAC Was Obvious (claims 13, 15-16)
 - D. TACs and Peripheral Contacts with Equal Diameters Were Obvious (claims 6, 15-16)

Road Map

- I. The IPR Grounds
- II. The '322 Patent
- III. State of the Art
- IV. Grounds 1 & 3: Nishikawa alone or in view of Nishikawa2
 - A. A Circular TAC Was Obvious (claims 8-20)
 - B. The Addition of Dummy Channels Was Obvious (claims 3, 6, 14-20)
 - C. A Ribbed TAC Was Obvious (claims 13, 15-16)
 - D. TACs and Peripheral Contacts with Equal Diameters Were Obvious (claims 6, 15-16)

(A) Petition's Showing—Circular TACs Were A Suitable Option: Nishikawa and Nishikawa2 Have the Same Architecture

- Nishikawa and Nishikawa2 have the same 3D memory architecture.



Nishikawa, Figs. 1, 16; Nishikawa2, Figs. 16, 17 (Petition (Paper 1), 44).

(A) Petition's Showing—Circular TACs Were A Suitable Option: Other Prior Art (1 of 2)

- (1) Circular TACs were well known.

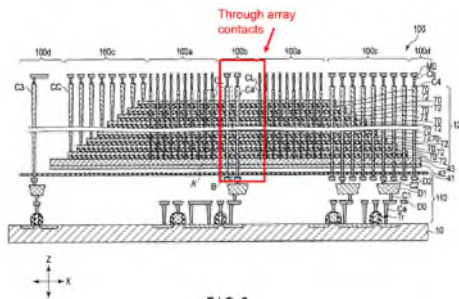


FIG. 2

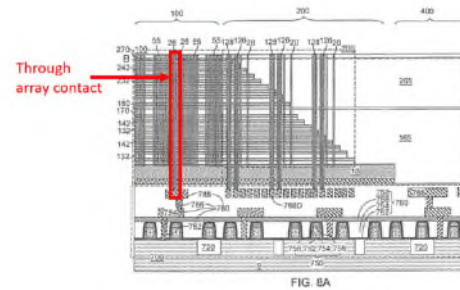
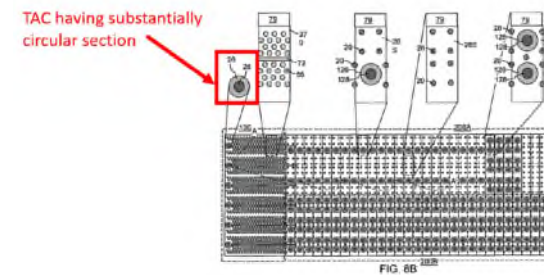
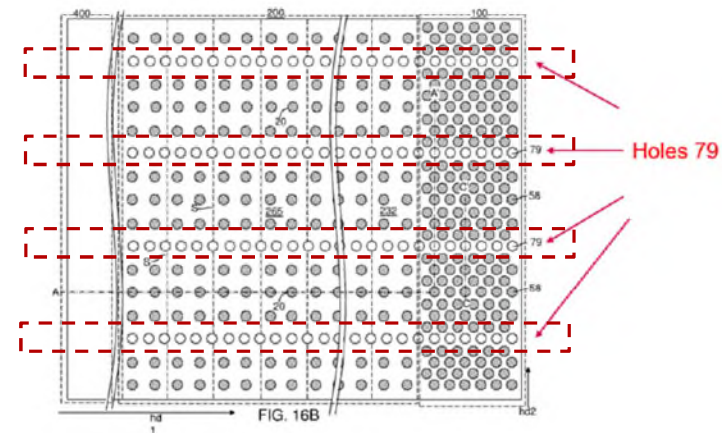
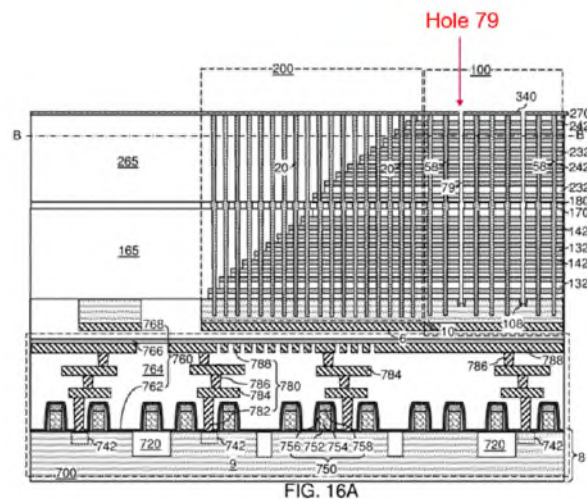


FIG. 8A



(A) Petition's Showing—Circular TACs Were A Suitable Option: Other Prior Art (2 of 2)

- (3) Circular TACs *for the gate replacement process* were well known.



Ex. 1022, Figs. 16A, 16B
(Petition (Paper 1), 49-50).

(A) Petition's Showing—Additional Motivation and Reasonable Expectation of Success

- Motivations:

1. Increase memory capacity by eliminating large backside trenches (Nishikawa2, 27:55-28:3),
2. Improve optional gate replacement process (Ex. 1022, 30:25-58), and
3. Improve source connection by spreading out connections throughout array (Exs. 1010, 111; 1023, Fig. 11).

- Reasonable Expectation of Success

1. Nishikawa ***already etches circular holes*** (which was routine in 3D memory prior art); and
2. Circular TACs were well known, including for source connections and the gate replacement process (e.g., Exs. 1009, 1010, 1020, 1021, and 1022).

Petition (Paper 1), 51-53.

(A) Patent Owner's Arguments Fail

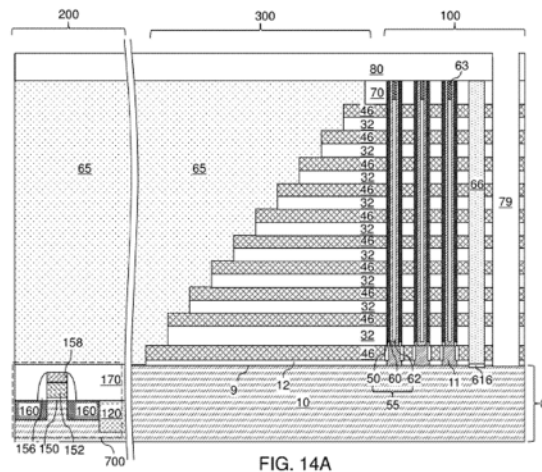
1. A circular TAC does not render Nishikawa inoperable;
 - a) PO's attempt to distinguish the applicability of Nishikawa2's TAC to Nishikawa fails;
 - b) PO's argument is based on a design that a POSITA would never implement.
2. There is no "missing limitation."

Reply (Paper 47), 2-12; POR (Paper 34), 11-35.

(A)(1)(a) Nishikawa and Nishikawa2 Disclose the Same Architecture

- PO argues that Nishikawa2's "circular" TAC statement is not relevant to Nishikawa2's Fig. 17, because the statement appears in the context of Figures 14A-C, which allegedly does not include "comb shaped" word lines.
- PO does not dispute that ***if the "circular" TAC statement is in the context of Nishikawa2's Figure 17, then the statement is applicable to Nishikawa.***

Reply (Paper 47), 8; POR (Paper 34), 24-27.



Nishikawa2

tric layer 12. The openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape. For example, in one embodiment, the openings 79 may comprise backside trenches 79. FIG. 14A is a vertical cross-sectional

Nishikawa2, Fig. 14A, 22:38-39 (Reply (Paper 47), 8).

(A)(1)(a) Nishikawa and Nishikawa2 Disclose the Same Architecture: PO Misreads Nishikawa2

- **Second**, Nishikawa2's Figures 14-17 describe the same embodiment:

Referring to FIGS. 14A-14D, source electrode (or source local interconnect) openings 79 can be formed through the optional contact level dielectric layer 80, the insulating cap layer 70, the alternating stack (32, 42), and the gate dielectric layer 12. The openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape. For

Referring to FIG. 15, an insulating material layer can be formed in each backside trench 79 and over the contact level dielectric layer 80 by a conformal deposition process. Exem-

A backside contact via structure 76 can be formed within each cavity. Each backside contact via structure 76 can fill a respective cavity. The contact via structures 76 can be

FIG. 17 is a see-through top-down view in which dielectric material layers overlying a topmost electrically conductive layer 46 have been omitted for clarity. Elongated contact

Each electrically conductive layer 46 (i.e., each of the word-line-level electrically conductive layers 46) formed within the alternating stack (32, 46) includes two physically disjoined portions (46A, 46B) between each optional neighboring pair of backside trenches (which are filled with the insulating spacers 74 and the backside contact structures 76)

Nishikawa2, 22:34-39, 23:4-46, 24:24-26, 24:65-67, 25:36-51 (Reply (Paper 47), 9-10) (Petition (Paper 1), 32).

(A)(1)(a) Nishikawa and Nishikawa2 Disclose the Same Architecture: Dr. Campbell's Testimony

- Dr. Campbell did not deny that Figures 14-17 describe the same embodiment.

Dr. Campbell

Q. So sitting here today, do you still believe that Figure 17 is a separate embodiment from Figure 14?

A. I have no proof one way or the other. So it certainly could be, but I don't know it.

Ex. 1106, 100:22-101:3 (Reply (Paper 47), 9).

- Nor could he, because the common numerals among Figures 14-17 mean that the figures describe the same structure.

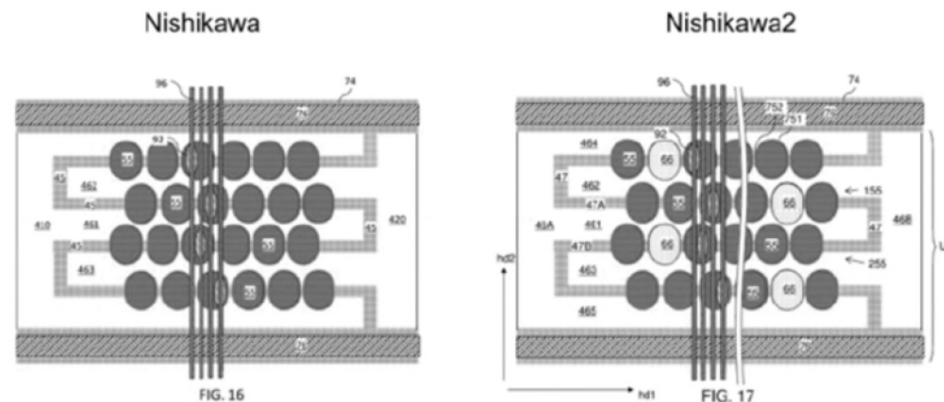
37 CFR 1.84(p)(4) ("same reference character must never be used to designate different parts") (Reply (Paper 47), 10).

(A)(1)(a) Nishikawa and Nishikawa2 Disclose the Same Architecture: Nishikawa2's Circular Statement Applies to Figure 17

- Thus, Nishikawa2's "circular" TAC argument applies to Figure 17 and indisputably demonstrates that Nishikawa is operable with a circular TAC:

Nishikawa2

tric layer 12. The openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape. For example, in one embodiment, the openings 79 may comprise backside trenches 79. FIG. 14A is a vertical cross-sectional



*Nishikawa, Fig. 16;
Nishikawa2, Fig. 17, 22:38-39
(Reply (Paper 47), 8).*

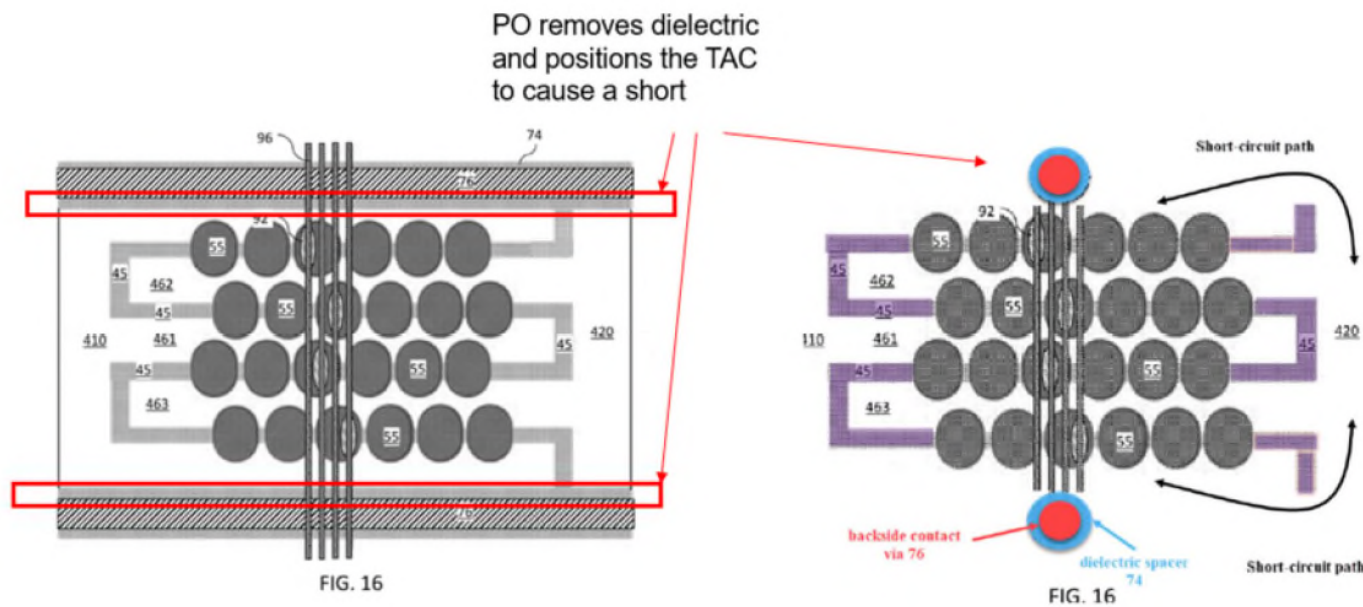
(A) Patent Owner's Arguments Fail

1. A circular TAC does not render Nishikawa inoperable;
 - a) PO's attempt to distinguish the applicability of Nishikawa2's TAC to Nishikawa fails;
 - b) PO's argument is based on a design that a POSITA would never implement.
2. There is no "missing limitation."

Reply (Paper 47), 2-12; POR (Paper 34), 11-35.

(A)(1)(b) PO's Inoperability Arguments Assume a Modification that No POSITA Would Implement

- To advance its inoperability argument against Nishikawa, PO (1) removes horizontal dielectric and (2) positions the TAC specifically to cause a short circuit.



Nishikawa Fig. 16 (annotated)

*POR (Paper 34), 18; Nishikawa, Fig. 16
(Reply (Paper 47), 3).*

(A)(1)(b) PO's Inoperability Arguments Assume a Modification that No POSITA Would Implement

- But even Dr. Campbell rejects that a POSITA would implement a modification that causes a short circuit:

Q. Would a POSITA looking at Nishikawa 123 ever **modify Nishikawa such that it short circuits** as you've shown in paragraph 56? I'm asking about a POSITA's knowledge?

A. **A POSITA would not do this**, which is the—which is—what we're trying to—what I'm trying to present, this is essentially round structure.

If you were to convert this trench in Nishikawa, it cannot provide the isolation between 420 and 410.

Ex. 1106, 73:22-74:9 (Reply (Paper 47), 2).

(A)(1)(b) PO's Inoperability Arguments Assume a Modification Inconsistent with the Petition and Nishikawa's Teachings

- The Petition—citing Nishikawa—demonstrates that Nishikawa expressly provides a separator structure that isolates the gate into two regions (and thus avoids a short circuit):

Petition

Nishikawa discloses two types of slits. First, Nishikawa discloses that “[e]ach memory opening 49 can be located between a pair of separator dielectric structures 45.” Nishikawa, 8:57-59. In other words, the separator dielectric structures, by themselves, divide the array into groups of memory cells.

Petition (Paper 1), 55; Reply (Paper 47), 3.

Nishikawa

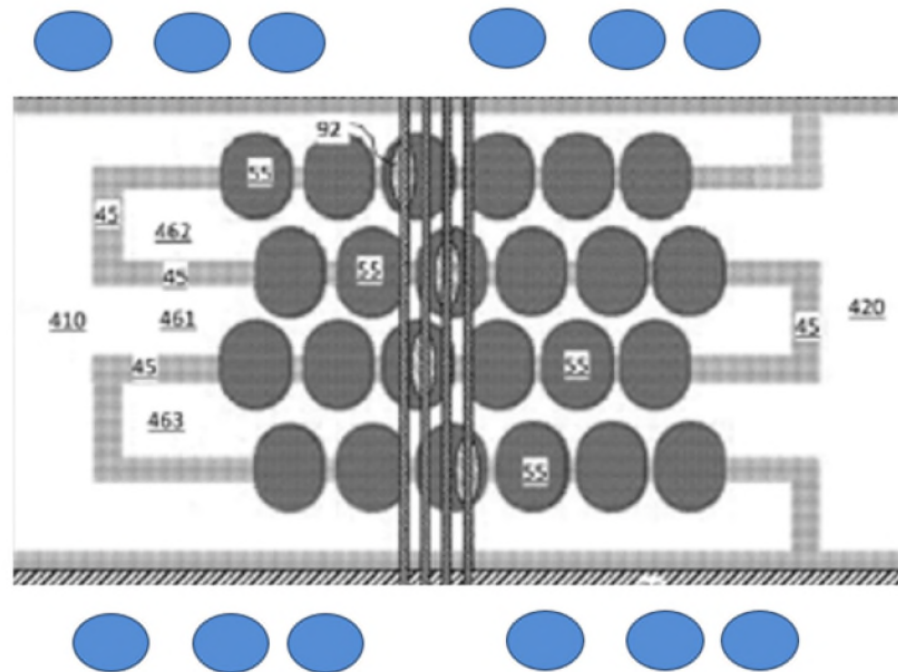
separator dielectric structures 45. In one embodiment, the separator dielectric structures 45 can laterally separate various portions of the alternating stack (32, 42).

The separator dielectric structures 45 extend through the stack, contact portions of outer sidewalls of the memory stack structures 55, and laterally separate the control gate electrodes 46 of the plurality of charge storage elements (which are portions of the charge storage regions 54). The

*Nishikawa, 8:33-35, 17:14-18;
Reply (Paper 47), 3-5.*

(A)(1)(b) Exemplary Modification That Does Not Cause a Short Circuit: a Separator Serves its Function to Divide the Gates

- As the Petition advances, Nishikawa's "separator" may "separate" the gates (sets 410 and 420).



Nishikawa, Fig. 16 (Reply (Paper 47), 4).

(A)(1)(b) Exemplary Modification That Does Not Cause a Short Circuit: PO Provides Its Own Operable Modification

- PO itself provides an operable modification, arguing only that it does not reduce footprint because it requires a large circular TAC to contact the side of the device:

POR

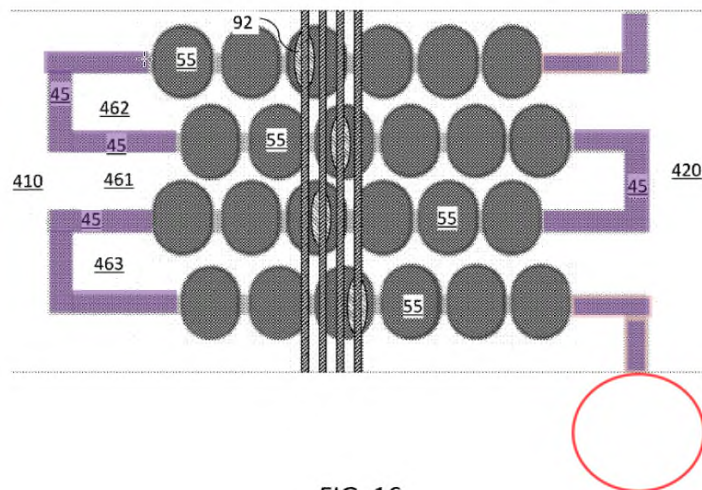


FIG. 16

Nishikawa Fig. 16 (modified)

Nishikawa, Fig. 16 (POR (Paper 34), 22).

Reply (addition PO's alleged end of device)

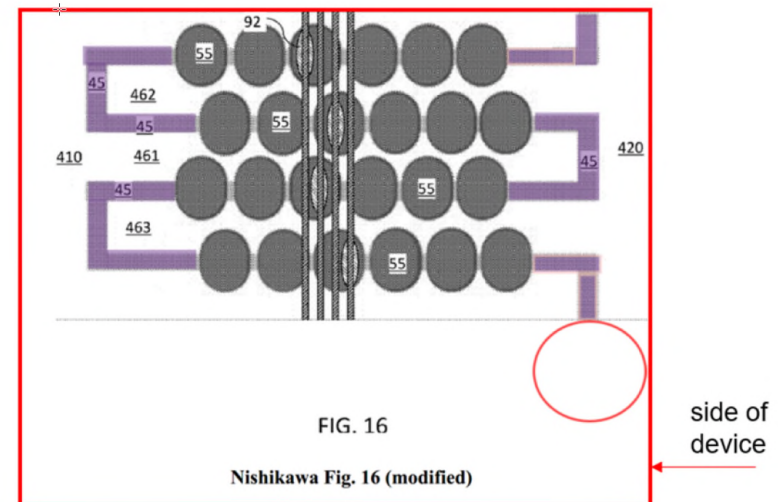


FIG. 16

Nishikawa Fig. 16 (modified)

Nishikawa, Fig. 16 (Reply (Paper 47), 6).

(A)(1)(b) Exemplary Modification That Does Not Cause a Short Circuit: A Circular TAC Does Not Increase the Device Size

- PO's "footprint" argument fails, because it manipulates the side of the device. There is additional space available within the same device size with a circular TAC.

PO's Implicit Side of Device

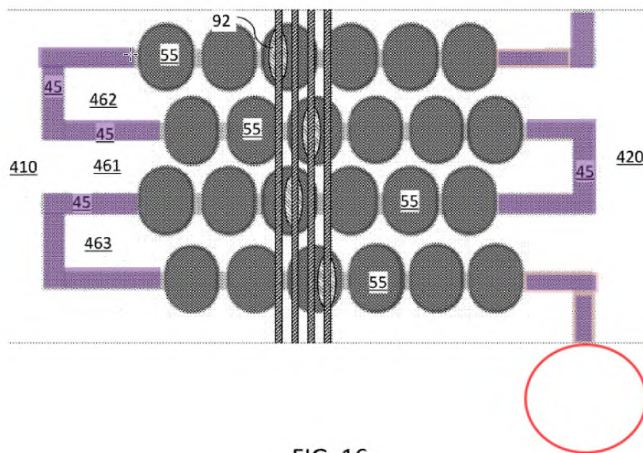


FIG. 16

Nishikawa Fig. 16 (modified)

*Nishikawa, Fig. 16 (POR
(Paper 34), 22).*

Actual Side of Device

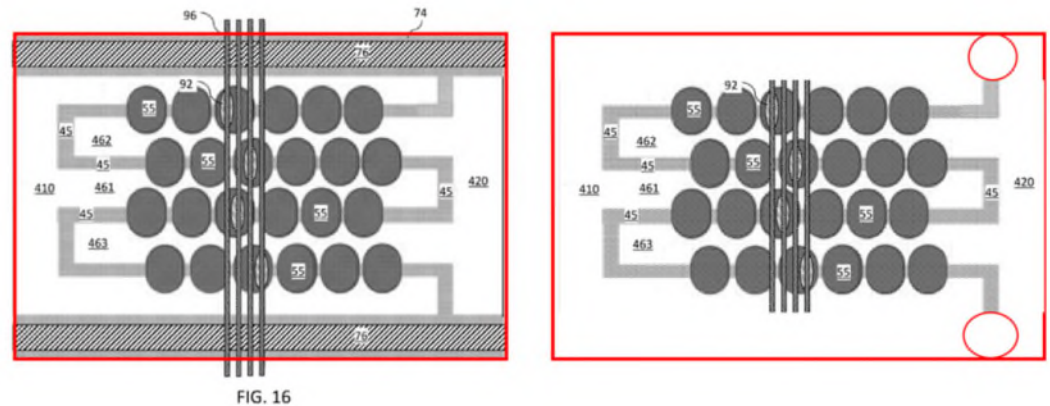


FIG. 16

*Nishikawa, Fig. 16 (Reply
(Paper 47), 7).*

(A)(1)(b) PO's New Sur-Reply Argument that the Record Does Not Identify a Device Edge Fails

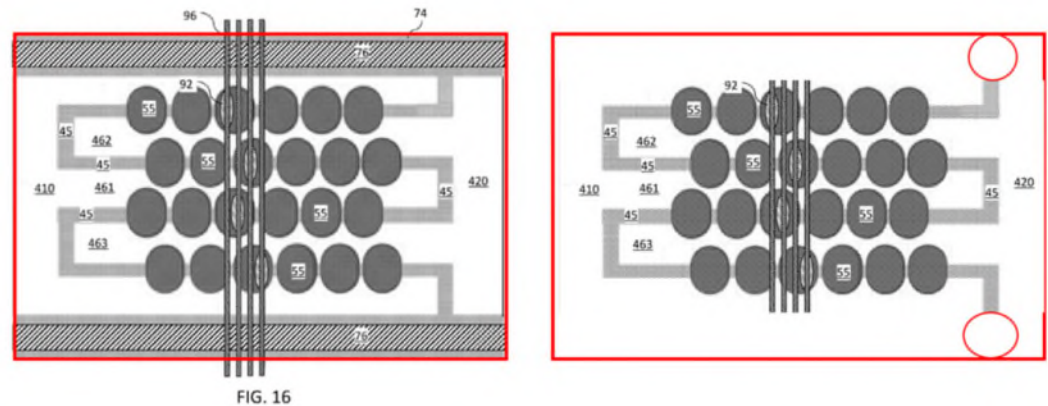
- In sur-reply, PO argues that the record does not identify any device edge for Nishikawa.

Sur-reply (Paper 55), 9)

Actual Side of Device (or Block)

FIG. 16 is a see-through top-down view of the exemplary device structure that illustrates global shapes of various components of the exemplary device structure according to an embodiment of the present disclosure.

Nishikawa, 3:35-38 (Petition (Paper 1), 34).



Nishikawa, Fig. 16 (Reply (Paper 47), 7).

(A)(1)(b) PO's New Argument Case Law is Inapposite

- PO alleges that the Reply's arguments are improper, relying on *Pioneer Pet Prods., LLC v. Oil-Dri Corp. of Am.*, IPR2022-00691, 2023 WL 5955777, at *12 (P.T.A.B. Sept. 12, 2023).
 - But *Pioneer* is inapposite. There, the Reply "introduces new theories and new evidence ... that depart significantly from the" Petition's arguments. *Id.*, at *10. That Reply "largely ignores" the inherency basis in the Petition (certain particles) and relies on new materials "beyond those described in the prior art relied on in the Petition." *Id.*
- The Reply rebuts the argument that Nishikawa is inoperable with a circular TAC, citing the same prior art and arguing that a dielectric separator (as the Petition advances) may avoid a short circuit.

Chamberlain Grp., Inc. v. One World Techs., Inc., 944 F.3d 919, 925 (Fed. Cir. 2019)
("Parties are not barred from elaborating on their arguments on issues previously raised.")

(A) Patent Owner's Arguments Fail

1. A circular TAC does not render Nishikawa inoperable;
 - a) PO's attempt to distinguish the applicability of Nishikawa2's TAC to Nishikawa fails;
 - b) PO's argument is based on a design that a POSITA would never implement.
2. There is no "missing limitation."

Reply (Paper 47), 2-12; POR (Paper 34), 11-35.

(A)(2) Nishikawa2 and Other Prior Art Disclose a Circular TAC

- Nishikawa2 expressly discloses the allegedly "missing limitation."

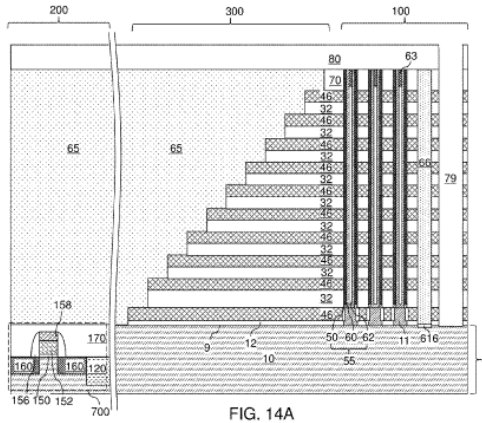


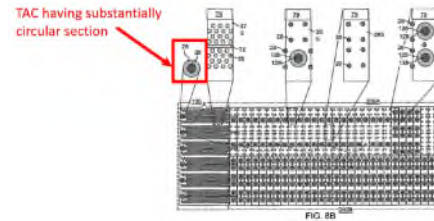
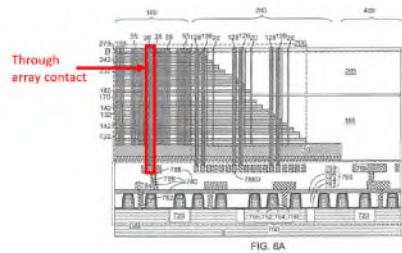
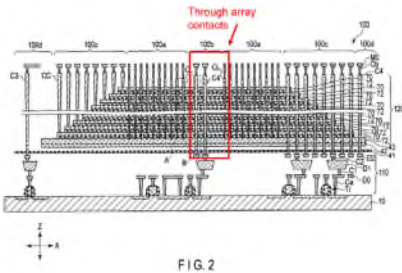
FIG. 14A

Nishikawa2

tric layer 12. The openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape. For example, in one embodiment, the openings 79 may comprise backside trenches 79. FIG. 14A is a vertical cross-sectional

Nishikawa2, Fig. 14A, 22:38-39 (Reply (Paper 47), 8, 11).

- The prior art of record is replete with examples of circular TACs.



Ex. 1009, Fig. 2; Ex. 1020, Figs. 8A, 8B (Petition (Paper 1), 44-46) (Reply (Paper 47), 11).

(A)(2) PO's Case Law Is Inapposite

- There is no missing limitation. Regardless, there is "reasoned analysis and evidence support" for circular TACs.

We disagree with Patent Owner. In *DSS Tech.*, the Federal Circuit held that reliance on “‘ordinary creativity’ ‘as a wholesale substitute for reasoned analysis and evidence support’” without providing “a reasoned explanation that avoids conclusory generalizations” is not sufficient “when dealing with a limitation missing from the prior art references.” 885 F.3d at 1376. There, the Federal Circuit explained that the Board did not identify any evidence to support its reliance on the ordinary creativity of the skilled artisan to supply the missing limitation. *See id.* at 1375; *see also id.* at 1376 (stating that to the extent the Board relies on declarant testimony, such “conclusory statements and unspecific expert testimony” are insufficient to support the Board’s findings). Unlike the situation presented in *DSS Tech.*, the Petitioner here provides sufficient evidence at this stage of the proceeding to support its contention implementing Nishikawa’s backside contact via cylindrical TACs was a suitable, well known option. *See e.g.*, Ex. 1003 ¶¶ 113–128 (citing, *inter alia*, Ex. 1005; Ex. 1010; Exs. 1020–1023; Ex. 1046).

ID (Paper 22), 14-15 (Reply (Paper 47), 11).

(A)(2) Nishikawa's Cursory Treatment of a "Circular" TAC Demonstrates It Is a Simple and Well-Known Option

- Nishikawa2 does not detail the circular TAC implementation because a POSITA "was more than capable of selecting between" these known TAC shapes.

Uber Techs., Inc. v. X One, Inc., 957 F.3d 1334, 1339 (Fed. Cir. 2020)
(Reply (Paper 47), 12).

Nishikawa2

tric layer 12. The openings 79 can have any suitable shape, such as circular, rectangular or elongated trench shape. For example, in one embodiment, the openings 79 may comprise backside trenches 79. FIG. 14A is a vertical cross-sectional

Nishikawa2, Fig. 14A, 22:38-39 (Reply (Paper 47), 11-12).

- And Nishikawa already etches circular contacts.

Petition (Paper 1), 51-53.

Road Map

- I. The IPR Grounds
- II. The '322 Patent
- III. State of the Art
- IV. Grounds 1 & 3: Nishikawa alone or in view of Nishikawa2
 - A. A Circular TAC Was Obvious (claims 8-20)
 - B. The Addition of Dummy Channels Was Obvious (claims 3, 6, 14-20)
 - C. A Ribbed TAC Was Obvious (claims 13, 15-16)
 - D. TACs and Peripheral Contacts with Equal Diameters Were Obvious (claims 6, 15-16)

(B) Petition's Showing—The Addition of Dummy Channels Would Have Been Obvious: the Edge Effect

- The Petition demonstrates that it would have been obvious to use dummy channels to address the known problem of the "edge effect" and increase yield.

In a typical flash cell array, cells located at the edge of the array are much more subject to processing variations than the cells not located at the edge. Because of this, it is common to refrain from using the cells at the array edge. Such cells, which extend around the perimeter of the array, are sometimes referred to as dummy cells. Array 42 is

Edge of array issues may typically occur at the boundary between a chop mask and pitch double patterning. An abnormality at the edge of an array pattern can cause blowout or shorting issues, depending on the integration process. Conventionally, an abnormal edge pattern at the edge of array may be controlled by adding a dummy pattern region, which is later sacrificed in processing. However,

*Exs. 1024, 8:47-53; 1025, 2:30-36
(Petition (Paper 1), 59-60).*

(B) Petition's Showing—The Addition of Dummy Channels Would Have Been Obvious: Additional Structural Support

- The Petition demonstrates that dummy channels (which can be made at the same time and with the same process as channels) add additional structural support for Nishikawa's optional gate-replacement process.

In addition, interstitial semiconductor-containing support structures (not expressly shown) can be formed within each M×N array of semiconductor-containing support structures 20. For example, if M is 3 and N is 2, a pair of semiconductor-containing support structures 20 can be inserted between the two rows of three semiconductor-containing support structures 20 at interstitial positions. Generally speaking, additional semiconductor-containing support structures 20 may be formed within each instance of an M×N array of semiconductor-containing support structures 20 to provide additional structural support during replacement of the first and second sacrificial material layers (142, 242) with first and second electrically conductive layers (146, 246).

FIGS. 5A-5L illustrate structural changes during formation of a memory stack structure, an optional dielectric core, and a drain region in a memory opening 49, which is one of the memory openings 49 in the exemplary structure of FIGS. 4A and 4B. The same structural change occurs simultaneously in each of the other memory openings 49 and in each support opening 19.

Exs. 1031, 30:14-27, 1027, 10:20-26 (Petition (Paper 1), 62-63).

(B) Institution Decision

- Preliminarily, the Board did not credit the Petition's showing because even if it were common to use dummy channels at the array edge:
 - (1) this does not show an "advantage,"
 - (2) one reference states the dummy region may later be "sacrificed" (and thus the dummies are not in the final product) and
 - (3) Nishikawa already discloses supporting structures.

We agree with Patent Owner. Although Dr. Lee attests that "it is common to refrain from using the cells at the array edge," which are "sometimes referred to as dummy cells," due to "processing variations," this does not show an advantage to adding dummy channels. Ex. 1003 ¶ 141 (quoting Ex. 1024, 8:47–53). To the extent that Dr. Lee states that dummy channels should be added, Dr. Lee attests that such a dummy region at the edge of the array is "later sacrificed in processing," which would not result in the claimed limitation of a "dummy channel structure . . . in the memory stack." *Id.* (citing Ex. 1025, 2:20–43).

during the gate replacement process. Prelim. Resp. 9–11; Pet. 60–63. To the extent that Petitioner's addition of dummy structures would result in additional structural support to Nishikawa's existing separator dielectric structures, Petitioner has not explained how such additional support beyond what Nishikawa discloses, in view of any tradeoffs with additional processing needed to create additional dummy channels, would be viewed as desirable by a person having ordinary skill in the art. Consequently, the

ID (Paper 22), 19-20.

PO's Arguments Fail

1. PO is incorrect that "edge effects" only exist in 2D devices: the common solution in 3D memory devices was to include dummy channels on the edge of 3D arrays to increase yield.
2. PO is incorrect that dummy channels would provide redundant support: the dummy channels provide support *throughout* the memory device.
3. PO's alleged complications of forming dummy channels is inconsistent with the record: there is no serious tradeoff, because these run-of-the-mill structures avoid defective edge cells and provide necessary support.
4. There is no "missing limitation."
5. Dr. Cambell was unaware of the conventional "edge effect" problem.

POR (Paper 34), 35-55; Reply (Paper 47), 12-24.

(B)(1) Obviousness Law

- Respectfully, Micron is not required to show that dummy channels in Nishikawa result in an "improvement or benefit" in a "categorical sense."

*Cisco Sys., Inc. v. K.Mizra LLC, 2024 U.S. App. LEXIS 20720, at *9-10 (Fed. Cir. Aug. 16, 2024)
(Reply (Paper 47), 12).*

- Instead, it need only show that dummy channels were a "known" or "suitable" option to address the edge effect or to provide additional support.

*Cisco Sys., Inc. v. K.Mizra LLC, 2024 U.S. App. LEXIS 20720, at *9-10 (Fed. Cir. Aug. 16, 2024); Intel Corp. v. PACT XPP Schweiz AG, 61 F.4th 1373, 1381 (Fed. Cir. 2023)
(Reply (Paper 47), 12).*

- The full trial record demonstrates that dummy channels were both known and suitable to address these problems.

(B)(1) The Edge Effect Was Not Unique to 2D Memories (1 of 2)

- It was "conventional" to use dummy channels at the edge of the array to address the edge effect problem.

In a conventional 3D memory device structure, data lines (e.g., bit lines, digit lines) are electrically coupled to vertical memory strings of a vertical memory array, and an opening is provided next to edges of the vertical memory array to accommodate data line contacts for each of the data lines. The data line contacts electrically couple the data lines to control logic circuitry to facilitate operations (e.g., read operations, write operations, erase operations) on the vertical memory strings of the vertical memory array. However, providing the opening for the data line contacts next to the vertical memory array can effectuate damage to and/or defects at the edges of the vertical memory array (e.g., commonly referred to as "array edge effects"). Accordingly, an array of "dummy" pillars (e.g., dielectric pillars) is conventionally provided between the vertical memory array and the opening to set the edges of the vertical memory array back farther from the opening and mitigate the aforementioned damage to and/or defects at the edges of the vertical memory array. Unfortunately, the area conventionally

Ex. 1108, 1:41-63 (Reply (Paper 47), 13-14).

(B)(1) The Edge Effect Was Not Unique to 2D Memories (2 of 2)

- It was "conventional" to use dummy channels at the edge of the array to address the edge effect problem.

[0026] FIG. 1B is a block diagram illustrating a portion of an array 101 of memory cells. In the example illustrated in FIG. 1B, the array 101 is configured in a cross-point memory array architecture, e.g., a three-dimensional (3D) cross-point memory array architecture. The multi-deck cross-point

[0033] Dummy material portions, e.g., portions 234-1 and 234-2, can include, for instance material formed to a lower tolerance and formed external, e.g., on an outer edge, to the active array portion 252. For example, in patterning a memory cell array, outer memory cell stack structures can be deformed or marginalities can be generated, caused by an iso-dense loading effect. Dummy material portions, if electrically inactive, e.g., isolated, as compared to the rest of the array, can be utilized to reduce undesired edge array effects. In a number of

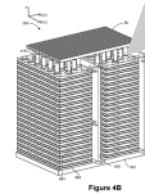
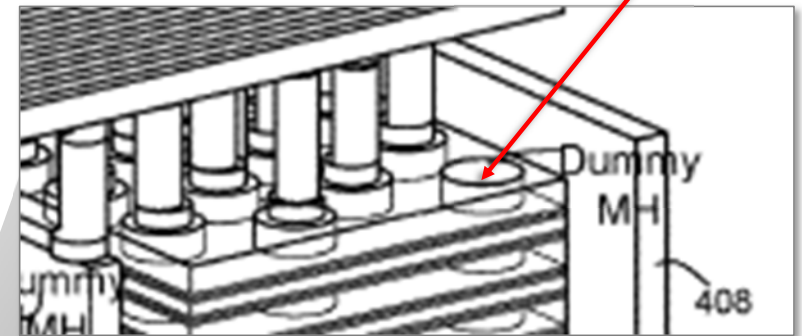
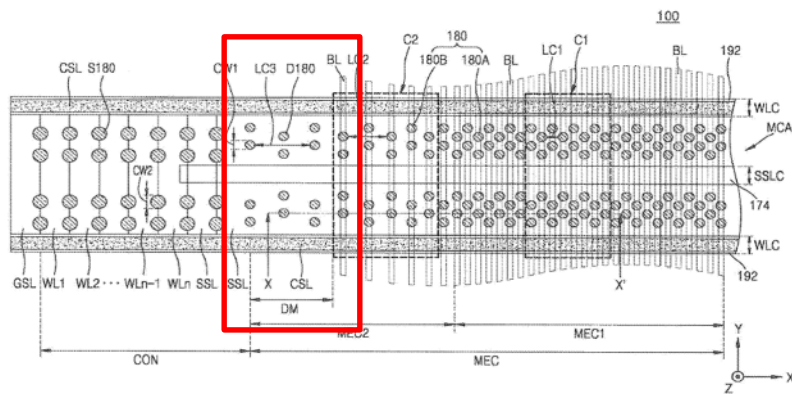
[0045] The edge region MEC2 of the memory cell region MEC may include a dummy channel region DM disposed at a portion adjacent to the connection region CON. A plurality of dummy channel structures D180 may be disposed in the dummy channel region DM of the edge region MEC2. The plurality of dummy channel structures D180 may have substantially the same configuration as the plurality of first channel structures 180A and the plurality of second channel structures 180B. In other words, each of the plurality of

Exs. 1109, [0026], [0033]; 1110, [0045] (Reply (Paper 47), 14).

(B)(1) A Suitable Option Was to Leave the Dummy Channels on the Edge of the Array in the Final Product (1 of 2)

- The Petition cites Ex. 1025 to explain the edge effect. The art demonstrates that leaving the dummy channels was a suitable and known option.

FIG. 1



Exs. 1110, Fig. 1; 1111, Fig. 4B
(Reply (Paper 47), 14).

(B)(1) A Suitable Option Was to Leave the Dummy Channels on the Edge of the Array in the Final Product (2 of 2)

- Dr. Lee explains—with supporting prior art—that dummy channels were left at the edge because the edge channels will always operate differently than the core channels.

Furthermore, an edge memory cell has a different condition compared with middle cells. In an edge cell, one side of a source/drain is connected to the select transistor while the other side is connected to a neighbor cell. However, in the middle cell, both sides are connected to neighbor cells. The potential of a floating gate is different between an edge cell and middle cells during operations. It causes abnormal electrical characteristics such as erase and program characteristics, as compared to middle cells. This is because the coupling ratio of the floating gate and the voltage condition applied around neighbor gates are different between an edge cell and a middle cell for each operation. It eventually results in wide V_{th} distributions of erase and program state.

Ex. 1015, 101 (Lee Reply Decl. ¶ 24) (Reply (Paper 47), 14).

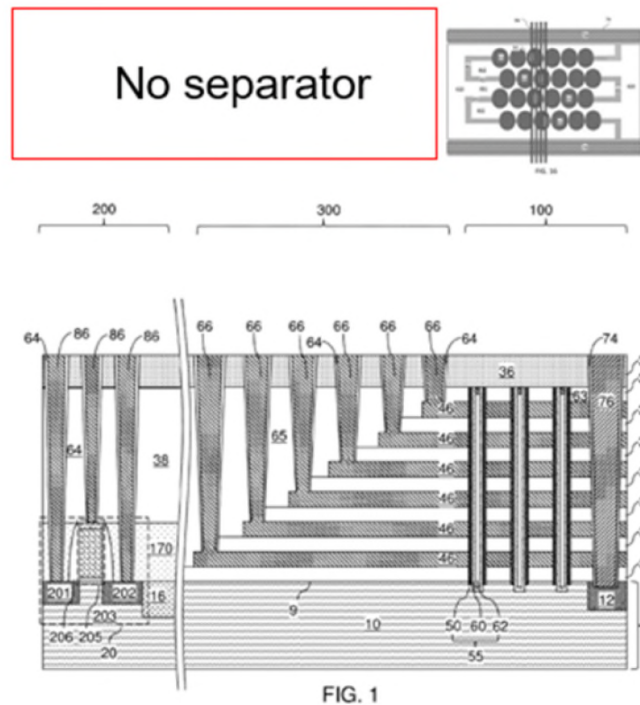
PO's Arguments Fail

1. PO is incorrect that "edge effects" only exist in 2D devices: the common solution in 3D memory devices was to include dummy channels on the edge of 3D arrays to increase yield.
2. PO is incorrect that dummy channels would provide redundant support: the dummy channels provide support **throughout** the memory device.
3. PO's alleged complications of forming dummy channels is inconsistent with the record: there is no serious tradeoff, because these run-of-the-mill structures avoid defective edge cells and provide necessary support.
4. There is no "missing limitation."
5. Dr. Cambell was unaware of the conventional "edge effect" problem.

POR (Paper 34), 35-55; Reply (Paper 47), 12-24.

(B)(2) PO's Argument that Nishikawa Does Not Need Additional Support Ignores Nishikawa's Full Device

- Nishikawa's separator does not provide structural support throughout Nishikawa's full device, that is, the separator does not extend from the edge of the array into the connection region.



Nishikawa, Figs. 1, 16 (Reply (Paper 47), 16).

(B)(2) The Record Contradicts PO's Argument That a Separator Renders "Additional Support" Unnecessary

- Nishikawa2 discloses both a separator and dummy channels (claim 3 recites: "a dummy channel structure filled with a dielectric layer").

Referring to FIGS. 12A and 12B, a dielectric material is deposited in the access openings 59 by a conformal deposition process. The dielectric material can include, for example, doped silicate glass, undoped silicate glass, or organosilicate glass. Examples of doped silicate glass mate-

portions of the deposited dielectric material. Each remaining portion of the dielectric material in the access openings 59 constitutes a dielectric pillar structure 66.

In one embodiment, the access openings 59 (which are a through-stack opening 49 within the second subset of through-stack openings 49) can have the same volume as each through-stack opening 49 within the first subset of through-stack openings 49. In this case, each dielectric pillar structure 66 can have substantially the same volume as a combination of an epitaxial channel portion 11, a memory film 50, a semiconductor channel 60, a dielectric core 62, and a drain region 63. As used herein, two elements have a

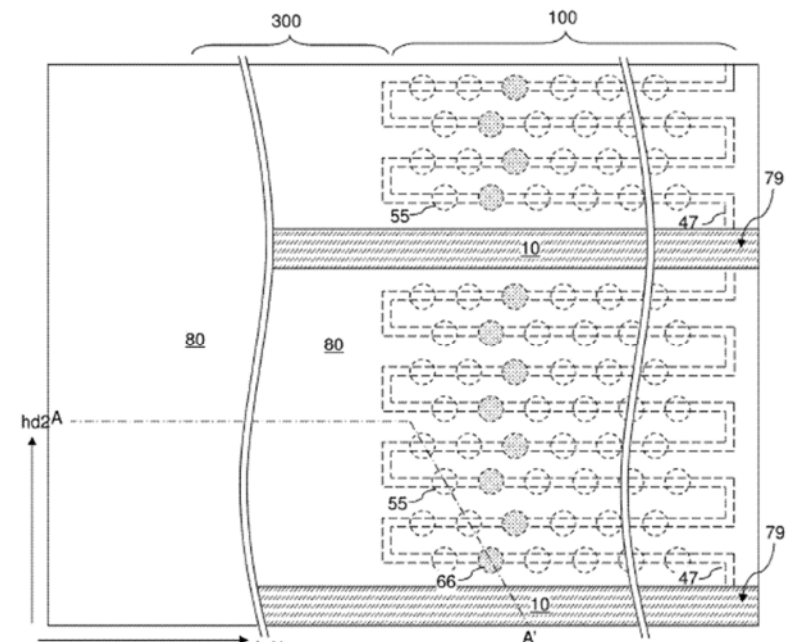


FIG. 14B

Nishikawa2, 21:40-44, 21:55-66, Fig. 14B (Reply (Paper 47), 22, 22 n. 6).

PO's Arguments Fail

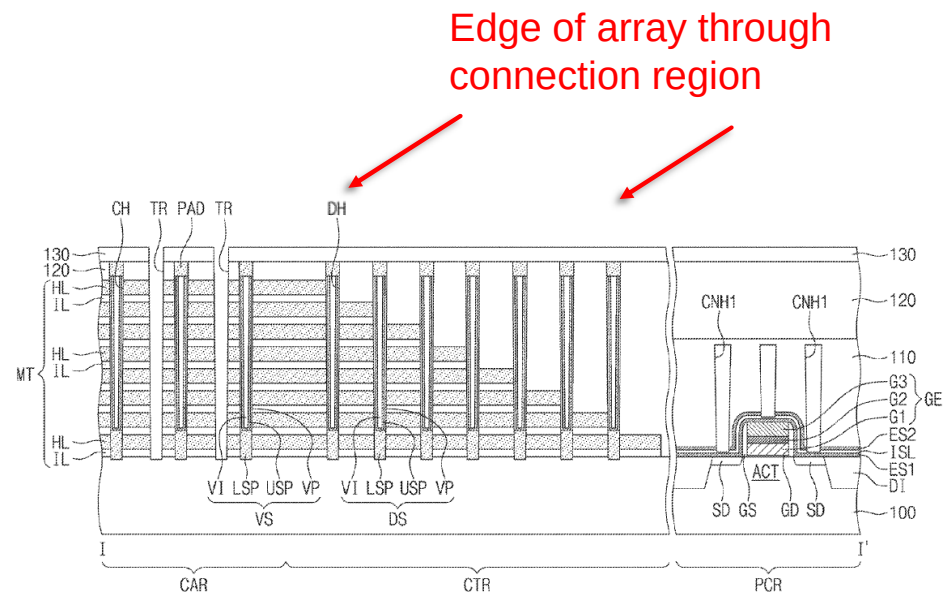
1. PO is incorrect that "edge effects" only exist in 2D devices: the common solution in 3D memory devices was to include dummy channels on the edge of 3D arrays to increase yield.
2. PO is incorrect that dummy channels would provide redundant support: the dummy channels provide support *throughout* the memory device.
3. PO's alleged complications of forming dummy channels is inconsistent with the record: there is no serious tradeoff, because these run-of-the-mill structures avoid defective edge cells and provide necessary support.
4. There is no "missing limitation."
5. Dr. Cambell was unaware of the conventional "edge effect" problem.

POR (Paper 34), 35-55; Reply (Paper 47), 12-24.

(B)(3) PO's Alleged Evidence Against Dummy Channels Supports the Addition of Dummy Channels

- PO argues that Kim counsels against dummy channels, because it stresses the need for "integration density, i.e., [memory] without dummy channels" (POR, 48).
- But Kim itself includes dummy channels.

[0047] The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region CTR. Dummy structures DS may be provided in the dummy holes DH. The dummy structures DS may be selectively provided only on the connection region CTR and not on the cell array region CAR. The dummy structures DS may be disposed adjacent to and spaced apart from the cell contacts CP. The dummy structures DS may physically support the stack structure ST on the connection region CTR. In some embodiments, identically or similarly to the vertical structure VS, each of the dummy structures DS may include a vertical insulation layer VP, an upper semiconductor pattern USP, a lower semiconductor pattern LSP, and a buried insulation pattern VI.



Ex. 1029, Fig. 13, [0047] (Petition (Paper 1), 62); (Reply (Paper 47), 23).

(B)(3) Dr. Cambell Admits that Fabricating an Operational Device Is of Equal Concern to Density

- Any insignificant impact on size pales in comparison to the concern of a manufacturing a functional device.

Q. Do you recall that you frequently testified that **memory density is the most important factor** when designing a 3D NAND memory array?

A. Yes.

Q. **That's not true, is it?**

A. **What's important is how many bits you can provide** for so many dollars. That's—in the end, that's what it comes down to. There are other things that can be useful, access rates and other things, but those are the two biggest.

Q. But **if you can't fabricate a memory array that doesn't collapse, it doesn't matter** how many bits you can stick in it, correct?

A. That's why I said—well, **okay, then I should have said functional bits.**

Q. Yeah, and—**so preventing array collapse is as equally important** as memory density, correct?

A. Because if it collapsed, then you won't have functional bits. So **yes, that's implied with what I said.**

Ex. 1106, 139:18-140:19 (Reply (Paper 47), 23).

PO's Arguments Fail

1. PO is incorrect that "edge effects" only exist in 2D devices: the common solution in 3D memory devices was to include dummy channels on the edge of 3D arrays to increase yield.
2. PO is incorrect that dummy channels would provide redundant support: the dummy channels provide support *throughout* the memory device.
3. PO's alleged complications of forming dummy channels is inconsistent with the record: there is no serious tradeoff, because these run-of-the-mill structures avoid defective edge cells and provide necessary support.
4. There is no "missing limitation."
5. Dr. Cambell was unaware of the conventional "edge effect" problem.

POR (Paper 34), 35-55; Reply (Paper 47), 12-24.

(B)(4) There Is No Missing Limitation: Dummy Channels Were the Conventional Solution for the Edge Effect

- A "missing limitation" cannot be what was "conventionally" used to address a well-known problem.

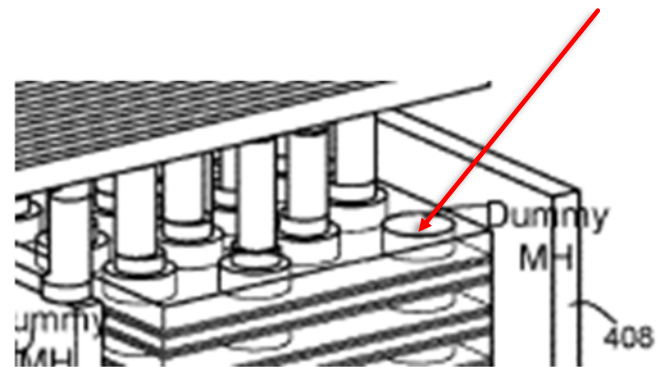
In a conventional 3D memory device structure, data lines (e.g., bit lines, digit lines) are electrically coupled to vertical memory strings of a vertical memory array, and an opening is provided next to edges of the vertical memory array to accommodate data line contacts for each of the data lines. The data line contacts electrically couple the data lines to control logic circuitry to facilitate operations (e.g., read operations, write operations, erase operations) on the vertical memory strings of the vertical memory array. However, providing the opening for the data line contacts next to the vertical memory array can effectuate damage to and/or defects at the edges of the vertical memory array (e.g., commonly referred to as "array edge effects"). Accordingly, an array of "dummy" pillars (e.g., dielectric pillars) is conventionally provided between the vertical memory array and the opening to set the edges of the vertical memory array back farther from the opening and mitigate the aforementioned damage to and/or defects at the edges of the vertical memory array. Unfortunately, the area conventionally

Ex. 1108, 1:41-63 (Reply (Paper 47), 13-14, 24).

(B)(4) Forming Dummy Channels Was Unusually Simple: Not Wiring the Edge and Connection Region Channel Structures

- Forming dummy channels—as was "conventional"—simply involves not wiring some of the channels (rendering them dummy channels):

In a typical flash cell array, cells located at the edge of the array are much more subject to processing variations than the cells not located at the edge. Because of this, it is common to refrain from using the cells at the array edge. Such cells, which extend around the perimeter of the array, are sometimes referred to as dummy cells. Array 42 is



Ex. 1024, 8:47-53 (Petition (Paper 1), 59-60).

Ex. 1111, Fig. 4B (Reply (Paper 47), 14, 24).

PO's Arguments Fail

1. PO is incorrect that "edge effects" only exist in 2D devices: the common solution in 3D memory devices was to include dummy channels on the edge of 3D arrays to increase yield.
2. PO is incorrect that dummy channels would provide redundant support: the dummy channels provide support *throughout* the memory device.
3. PO's alleged complications of forming dummy channels is inconsistent with the record: there is no serious tradeoff, because these run-of-the-mill structures avoid defective edge cells and provide necessary support.
4. There is no "missing limitation."
5. Dr. Cambell was unaware of the conventional "edge effect" problem.

POR (Paper 34), 35-55; Reply (Paper 47), 12-24.

(B)(5) Dr. Campbell Cannot Credibly Support PO's Position When He Was Unaware of a Conventional Problem Motivating Dummy Channels

- The edge effect was front and center in the Petition:

Petition

region on the edges. Lee, ¶ 141. It was well known that when a pattern stops (instead of extending into the dummy region), defects occur on the edge. *Id.* (citing Ex. 1024 (U.S. Pat. 5,945,717), 8:47-53 and Ex. 1025 (U.S. Pat. 10,347,487), 2:20-43 to explain the edge effect). Second, adding dummy structures would result in an overall

Ex. 1024

In a typical flash cell array, cells located at the edge of the array are much more subject to processing variations than the cells not located at the edge. Because of this, it is common to refrain from using the cells at the array edge. Such cells, which extend around the perimeter of the array, are sometimes referred to as dummy cells. Array 42 is

Ex. 1024, 8:47-53 (Petition (Paper 1), 59-60).

- These are well-known fabrication effects. Dr. Lee describes these in his opening declaration (Ex. 1003, ¶ 142) and in reply declaration (Ex. 1105, ¶¶ 22-27), citing Exs. 1024, 1026, 1107, 1108-10).

Petition (Paper 1), 59-60; Reply (Paper 47), 13-14.

(B)(5) Dr. Campbell Cannot Credibly Support PO's Position When He Was Unaware of a Conventional Problem Motivating Dummy Channels

- Yet in deposition, Dr. Campbell concedes he did not know what "edge effects" are:

Q. Array edge effects, do you know what that means?

A. Well, there's etch effects.

Q. Edge effects.

A. Edge effects.

Q. And here I'm asking for your personal understanding.

A. I will have to pass on that. No, I do not. That's a term that's not familiar to me.

Q. Do you have any idea what array edge effects are?

A. The name would imply defects—a possibility of defects being formed near the edge of where the array structures terminate.

Q. But you have no experience with array edge effects, correct?

A. That is correct.

*Ex. 1106, 60:8-21, 109:23-110:15
(Reply (Paper 47), 24-25).*

- The Board should disregard his testimony with respect to dummy channels, because he lacks the knowledge to testify regarding a conventional motivation for dummy channels.

Road Map

- I. The IPR Grounds
- II. The '322 Patent
- III. State of the Art
- IV. Grounds 1 & 3: Nishikawa alone or in view of Nishikawa2
 - A. A Circular TAC Was Obvious (claims 8-20)
 - B. The Addition of Dummy Channels Was Obvious (claims 3, 6, 14-20)
 - C. A Ribbed TAC Was Obvious (claims 13, 15-16)
 - D. TACs and Peripheral Contacts with Equal Diameters Were Obvious (claims 6, 15-16)

(C) Petition's Showing—Nishikawa's Stack Layers Include SiO Dielectric Layers and SiN Sacrificial Layers

- Nishikawa's 3D memory stack includes conventional SiO and SiN layers.

silicon nitride or polysilicon sacrificial layers. In an illustrative example, the insulating layers 32 can include silicon oxide (such as undoped silicate glass or doped silicate glass) and the sacrificial material layers 42 can be silicon nitride layers that can be subsequently removed, for example, by a wet etch employing phosphoric acid.

Nishikawa, 7:11-16 (Petition (Paper 1), 36, 74).

(C) Petition's Showing—Recesses in the Conductive or Dielectric Layers of the Alternating Stack Was a Challenge to Avoid

- A typical etch of the stack of alternating SiN sacrificial layers (which become the conductive layers) and SiO₂ dielectric layers results in unintentional recesses due the natural selectivity of etchants.

Although there are numbers of prior arts for SiO₂ etching with high selectivity to SiN, for certain applications, such as etching of multi-layered 3D NAND memory, it is important to have an etching gas which can etch both SiO₂ and SiN layers (or both SiO₂ and p-Si layers) without selectivity. In another word, it is a challenge to find an etch gas that has similar high etch rates of SiO₂ and SiN in terms of getting a smooth sidewall of high aspect ratio holes in 3D NAND memory.

- Thus, in view of typical prior art etches, natural recesses will occur in either the sacrificial layers (which become the conductive layers) or the dielectric layers.

Ex. 1039, 2:59-67 (Petition (Paper 1), 73-74, 81).

(C) Petition's Showing—It Was Known to Intentionally Create Recesses in the Sacrificial Layers to Create More Room for the Dielectric Spacer

- Just like the '322 patent, the prior art discloses creating recesses in the sacrificial gates to provide additional room for the insulating TAC spacer.

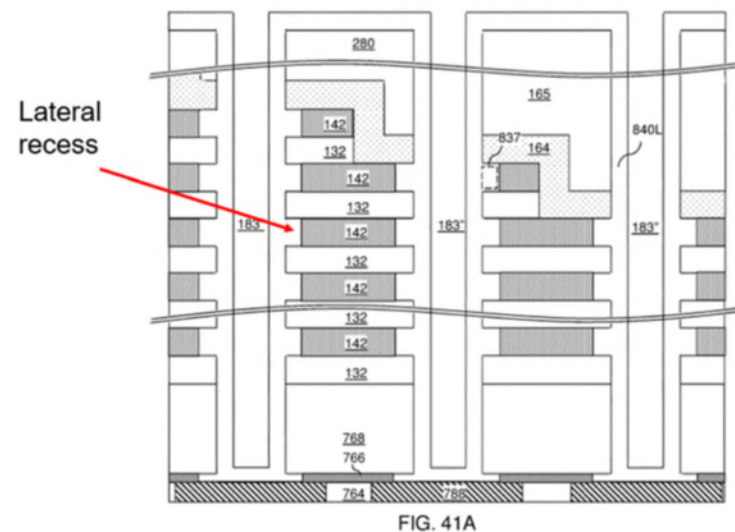
'322 Patent

some embodiments. Referring to FIG. 7B, at operation 706, to form the first spacer on the sidewall of the first opening, a plurality of shallow recesses are first formed by removing parts of the sacrificial layers abutting the sidewall of the first opening. At operation 708, a dielectric layer is deposited filling in the shallow recesses and on the sidewall and a bottom surface of the first opening. At operation 710, part of

Cui

sacrificial material layers (142, 242). Portions 84F of the conformal dielectric via liner 846L deposited at peripheries of the ribbed via cavities 183' fill the annular recesses AR (i.e., the rib regions). A neck portion 84N of the conformal dielectric via liner 846L can be formed around each set of at least one annular portions of the conformal dielectric via liner 846L that fill the annular recess(es) of each ribbed via cavity 183'. An annular seam 84S can be present within each

Cui



'322 Patent, 13:40-46; Cui, Fig. 41A, 27:54-61 (Petition (Paper 1), 76-77, 81).

(C) Institution Decision

- Preliminarily, the Board did not credit the extra space purpose as sufficiently explaining a motivation.

¶ 129). However, neither Petitioner nor Dr. Lee explain why this additional area is advantageous, except that it serves the same purpose as the lateral recesses in the '322 patent. Ex. 1003 ¶ 173. But a reason to combine should not be obtained solely from the challenged patent. *KSR*, 550 U.S. at 421 (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”); *Metalcraft of Mayville, Inc. v. Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) (“[W]e cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention.”).

ID (Paper 22), 21.

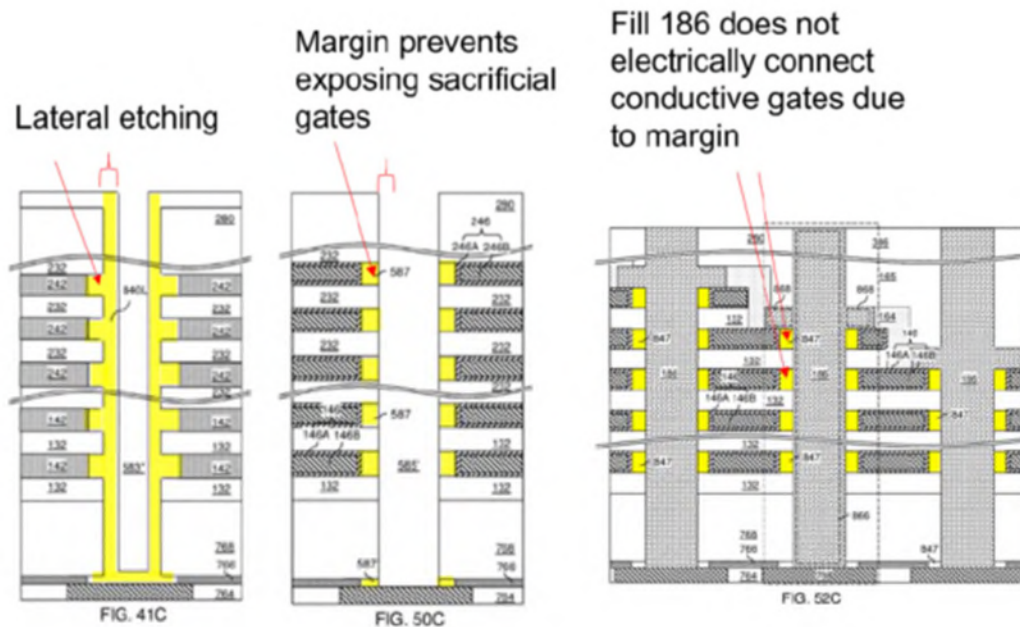
(C) Patent Owner's Arguments Fail

1. There is no hindsight: the extra space for the dielectric spacer is synonymous with reducing both short circuits and capacitive coupling (Micron's construction).
2. Micron does not advance an inherency theory (PO's construction)
3. There is no missing limitation.

Reply (Paper 47), 25-33; POR (Paper 34), 59-68.

(C)(1) Cui—from the Petition—Demonstrates that the Extra Space Reduces Short Circuits and Capacitive Coupling

- The extra space (resulting in extra dielectric spacer) allows for greater margin when etching the bottom of the dielectric liner, thereby preventing the conductive TAC core from connecting (or getting too close) to the conductive gates:



Cui, Figs. 41C, 50C, 52C (Reply (Paper 47), 29).

(C)(1) Liu Demonstrates that the Extra Space Reduces Capacitive Coupling Between the Conductive Layers and TAC Conductive Core

- Similarly, this extra space (resulting in extra dielectric spacer) is "desirable" to avoid capacitive coupling:

[0048] In some embodiments, illustrated in the side view of FIG. 7 and the top view of FIG. 8, conductive layers 430 can be recessed proximate contacts 440 such that material of insulative layers 431 is closer to the contacts 440 than the material of the conductive layers 430. Such recesses 432 in the conductive layers 430 can be filled with insulative material, such as that of an insulative liner 460. Recesses can be included if additional isolation from the contacts 440 is desired. The recesses 432 can be of any suitable depth 462.

* * *

leakage). Such electrical isolation can be accomplished at least in part by separating adjacent contacts by a distance 463 of at least about 200 nm in some embodiments. In general, it is desirable to minimize capacitor coupling as much as possible. Electrical isolation can be achieved when capacitance between adjacent contacts and between contacts and conductive layer material is acceptable for a given circuit.

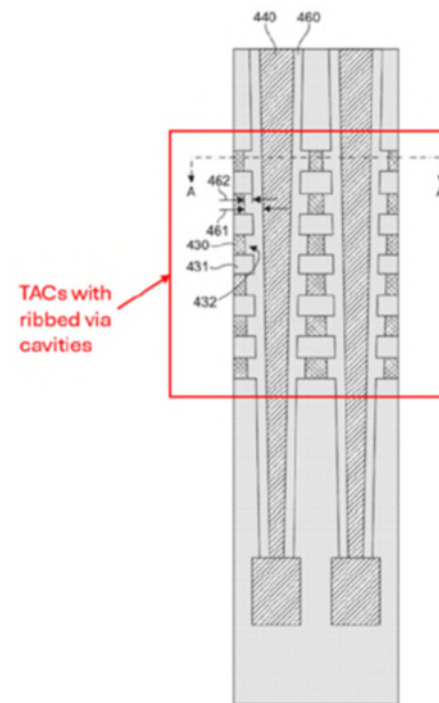


FIG. 7

Liu, Fig. 7, [0048] (Reply (Paper 47), 30).

(C)(1) Lilak Demonstrates that the Extra Space Reduces Capacitive Coupling Between the Conductive Layers and TAC Conductive Core

- Put another way, this extra space (resulting in extra dielectric spacer) avoids "leakage current":

In one embodiment, the memory material layer 214 is conformal to the plurality of selectors 210 and the insulating layers 204. In one embodiment, the selector 210 may comprise materials such as an Al₂O₃ tunnel barrier, TaOx, NbOx, VOx, or similar materials. In one embodiment, the memory material layer 212 may comprise HfO₂, TiOx, TaOx, NiOx or the like. Also, in the embodiment shown, the first conductive layers 202 are recessed from the etch pits 208 to increase leakage current suppression.

Greater distance
path between
conductive wordlines

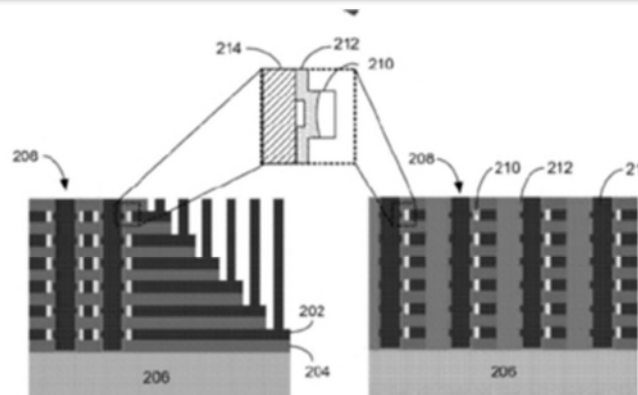
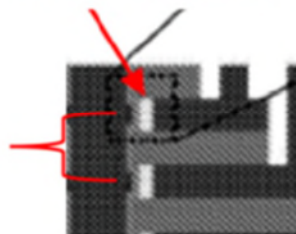


FIG. 2B

FIG. 2C

Ex. 1116, Figs. 2B-C, 7:12-17
(Reply (Paper 47), 31).

(C)(1) The '322 Patent's Silence Demonstrates That a POSITA Knew Why to Select the Conductive Gates for Recesses (1 of 2)

- There is no dispute that the '322 Patent is silent as to the purpose of the recesses in the conductive gate.

POR

Petitioner's improper reliance on the '322 Patent is underscored by its admission that the '322 Patent "provides virtually no explanation on creating these known rib regions." Pet. 77. In sum, Petitioner's motivation to combine fails and is derived

POR (Paper 34), 65 (Reply (Paper 47), 31).

- The '322 Patent's silence demonstrates that a POSITA was "more than capable of selecting between the[se] known methods" (consistent with Cui, Liu, and Lilak).

Uber Techs., Inc. v. X One, Inc., 957 F.3d 1334, 1339 (Fed. Cir. 2020) (Reply (Paper 47), 31-32).

- Put another way, the '322 Patent omits detailing the reason for the extra space, because "[a] patent ... preferably omits[] what is well known in the art").

Epistar Corp. v. ITC, 566 F.3d 1321, 1336 (Fed. Cir. 2009) (Reply (Paper 47), 31-32).

(C)(1) The '322 Patent's Silence Demonstrates That a POSITA Knew Why to Select the Conductive Gates for Recesses (2 of 2)

- In sur-reply, PO points to this silence as addressing "short[s]" and "leakage current," confirming a POSITA knew the purpose of the "extra space."

32. Specifically, Petitioner argues ribbed cavities create extra room for dielectric material to "prevent shorting the conductive layers from the TAC" and avoiding "leakage current." *Id.* But this is the purpose taught by the '322 patent: ribbed cavities can provide space for a thicker dielectric layer deposition and the resulting spacer "can electrically insulate conductor layer [of the] TAC" from the "surrounding conductor layers" in memory stack. Ex.1001, 8:47-62. Thus,

TAC 136 can include a vertical opening through memory stack 104 and that is filled with filling materials. In some embodiments, TAC 136 includes a spacer 138 on a sidewall of the opening and a conductor layer 140 in contact with spacer 138 in the opening. Conductor layer 140 can include conductive materials, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Spacer 138 can electrically insulate conductor layer 140 of TAC 136 from surrounding conductor layers 110 in memory stack 104. In some embodiments, TAC 136 has a substantially circular shape in the plan view, and conductor layer 140 and spacer 138 are disposed radially from the center of TAC 136 in this order. Spacer 138 of TAC 136 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

Sur-reply (Paper 55), 23; '322 Patent, 8:47-62.

(C) Patent Owner's Arguments Fail

1. There is no hindsight: the extra space provides the benefit of reducing both short circuits and capacitive coupling (Micron's construction).
2. Micron does not advance an inherency theory (PO's construction)
3. There is no missing limitation.

Reply (Paper 47), 25-33; POR (Paper 34), 59-68.

(C)(2) PO (1) Does Not Dispute that Unintentional Recesses Satisfy the Claim Language and (2) Concedes that Micron Advances an Obviousness Theory

- The Petition assumes that PO is not reading an intent element into the claim, and PO never asserted during trial that the limitation requires an intent element.

65, Fig. 3D. For infringement, however, PO interprets this claim to cover largely undetectable and unintentional alleged recesses. Ex. 1038 (Ex. B-1, YMTC's Contentions), 11, 28. As is well known, a typical etch through a stack of silicon

Petition (Paper 1), 73.

- PO concedes that Micron advances an obviousness—not an inherency—theory.

Petitioner also asserts Nishikawa renders obvious unintentional recesses because “it is a challenge to find” a gas that can etch “without selectivity.” Pet. 74.

POR (Paper 34), 63, 65 (Reply (Paper 47), 32-33).

(C)(2) The Record Demonstrates that a Typical 3D Memory Device Would Include Intentional Recesses

- PO responds with one example of an etchant that allegedly does not create recesses.
- But PO does not dispute that finding such an etchant was a "challenge."

Although there are numbers of prior arts for SiO₂ etching with high selectivity to SiN, for certain applications, such as etching of multi-layered 3D NAND memory, it is important to have an etching gas which can etch both SiO₂ and SiN layers (or both SiO₂ and p-Si layers) without selectivity. In another word, it is a challenge to find an etch gas that has similar high etch rates of SiO₂ and SiN in terms of getting a smooth sidewall of high aspect ratio holes in 3D NAND memory.

Ex. 1039, 2:59-67 (Petition (Paper 1), 73-74, 81) (Reply (Paper 47), 32-33).

(C) Patent Owner's Arguments Fail

1. There is no hindsight: the extra space provides the benefit of reducing both short circuits and capacitive coupling (Micron's construction).
2. Micron does not advance an inherency theory (PO's construction)
3. There is no missing limitation.

Reply (Paper 47), 25-33; POR (Paper 34), 59-68.

(C)(3) There Is No Missing Limitation: Regardless, the Prior Art Demonstrates That a POSITA Knew How and Why to Implement the Recesses

- The prior art treats the recesses as a well-known option:

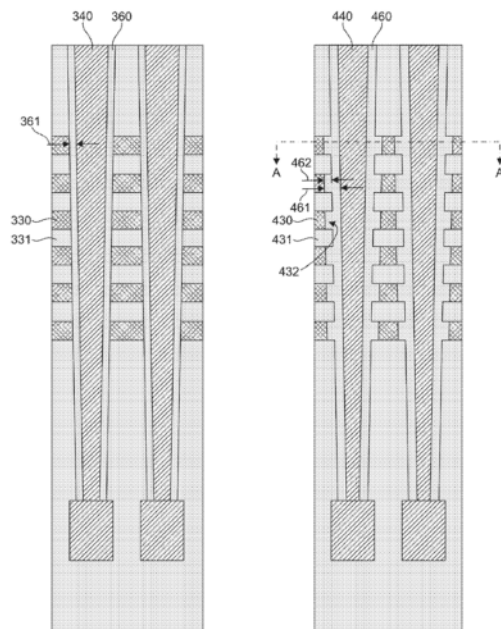


FIG. 6

FIG. 7

[0047] The contacts 340 can be electrically insulated or isolated from the conductive layers 330 to avoid capacitance and shorting (i.e., electrical leakage). In one aspect, the contacts 340 can be separated from the conductive layers 330 by insulative material. For example, insulative liners 360 can be disposed about the contacts 340 between the contacts and the conductive and insulative layers 330, 331 to insulate the contacts from the conductive layers. The insulative liners 360 can have any suitable thickness. In one aspect, as illustrated in FIG. 6, the insulative liners 360 can have a thickness 361 of at least about 5 nm between the contacts 340 and the conductive layer 330 material. The insulative liners 360 can be formed from any suitable insulative material, such as an oxide material, a nitride material, other insulative materials, or combinations thereof. The insulative liners 360 can contribute to separating and insulating the contacts 340 and the conductive layers 330 by a suitable distance.

[0048] In some embodiments, illustrated in the side view of FIG. 7 and the top view of FIG. 8, conductive layers 430 can be recessed proximate contacts 440 such that material of insulative layers 431 is closer to the contacts 440 than the material of the conductive layers 430. Such recesses 432 in the conductive layers 430 can be filled with insulative material, such as that of an insulative liner 460. Recesses can be included if additional isolation from the contacts 440 is desired. The recesses 432 can be of any suitable depth 462, but may be limited in a practical sense by structural considerations during manufacture, such as maintaining sufficient conductive layer material to prevent collapse of the structure. The contacts 440 and the material of the conductive layers 430 can be separated by a distance 461 of from about 5 nm to about 75 nm, which can be equal to a thickness of the insulative liners 460 between the contacts 440 and the conductive layer 430 material. Adjacent contacts can also be electrically insulated or isolated from one another to avoid capacitance and shorting (i.e., electrical leakage). Such electrical isolation can be accomplished at least in part by separating adjacent contacts by a distance 463 of at least about 200 nm in some embodiments. In

*Liu, Figs. 6-7, [0047]-[0048]
(Reply (Paper 47), 33).*

Road Map

- I. The IPR Grounds
- II. The '322 Patent
- III. State of the Art
- IV. Grounds 1 & 3: Nishikawa alone or in view of Nishikawa2
 - A. A Circular TAC Was Obvious (claims 8-20)
 - B. The Addition of Dummy Channels Was Obvious (claims 3, 6, 14-20)
 - C. A Ribbed TAC Was Obvious (claims 13, 15-16)
 - D. TACs and Peripheral Contacts with Equal Diameters Were Obvious (claims 6, 15-16)

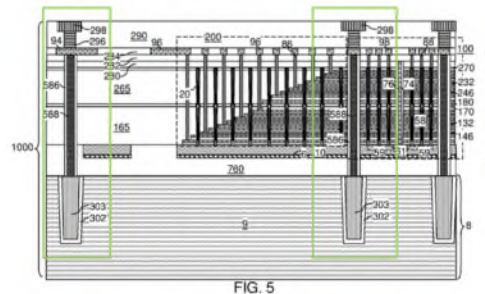
(D) Petition's Showing—To Save Time and Costs, the 3D Memory Prior Art Employs This "Very Common" Same Contact Size Solution

- The Petition shows that Tessariol, Mushiga, and Nakajima references all follow the approach of using the same contact size.

Tessariol

55 of vertically-alternating tiers 16, 18. In one embodiment, dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously). Regardless, in one embodiment, dummy-structure openings 56 and via openings 54 are formed using a single masking step (e.g., using masking material [not shown] formed atop structure 10). In one embodiment, dummy-structure openings 56 and

Mushiga



Nakajima

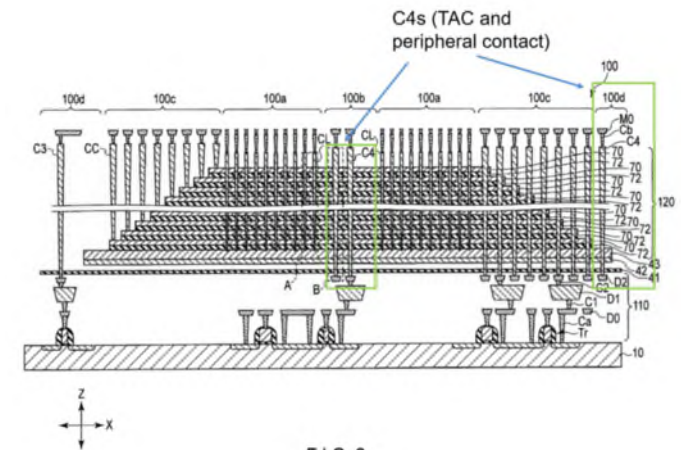


FIG. 2

Tessariol, [0037]; Mushiga, Fig. 5; Nakajima, Fig. 2 (Petition (Paper 1), 67-70).

(D) Patent Owner's Arguments Fail

1. Each argument fails for a threshold reason: PO fails to address that forming contacts is "very common" because it overcomes the over-etching problem.
2. PO is incorrect that forming contacts in the peripheral region and in the stack cannot be done with a "common process."
3. PO is incorrect that Mushiga and Nakajima do not describe a "common process."
4. PO is wrong on the law: the prior art figures demonstrate equal-diameters contacts.
5. PO's "missing limitation" argument fails (*supra*).

Reply (Paper 47), 34; POR (Paper 34), 59-68.

(D)(1) It Was a Textbook Solution to Employ Contacts with the Same Size to Overcome the Over-etching Problem

- One solution for "long overetch times" was using contacts with the same diameters.

Wolfe Textbook

As the contact hole size decreases below 1 μm there is a strong decrease in etch rate with contact size dimension. To avoid long overetch times, contact holes of identical dimension would need to be used if this problem was not solved. Reference 156 describes a dry-etch process which overcomes this limitation. By adding 10% Cl_2 to a CHF_3 plasma the effective fluorine to carbon ratio in small holes is kept constant, maintaining uniform etch rates, independent of contact hole size. Nevertheless, it is very common that only one contact size is used. Larger contacts are implemented with multiple contact windows.

*Ex. 1035, 33 (Petition (Paper 1), 67-70)
(Reply (Paper 47), 34).*

(D) Patent Owner's Arguments Fail

1. Each argument fails for a threshold reason: PO fails to address that forming contacts is "very common" because it overcomes the over-etching problem.
2. PO is incorrect that forming contacts in the peripheral region and in the stack cannot be done with a "common process."
3. PO is incorrect that Mushiga and Nakajima do not describe a "common process."
4. PO is wrong on the law: the prior art figures demonstrate equal-diameters contacts.
5. PO's "missing limitation" argument fails (*supra*).

Reply (Paper 47), 34; POR (Paper 34), 59-68.

(D)(2) The Premise of PO's Arguments Is Incorrect: a Common Process Etches Through Different Materials

- PO argues a "common process" cannot etch through "different materials."
- Tessariol alone rejects PO's argument:

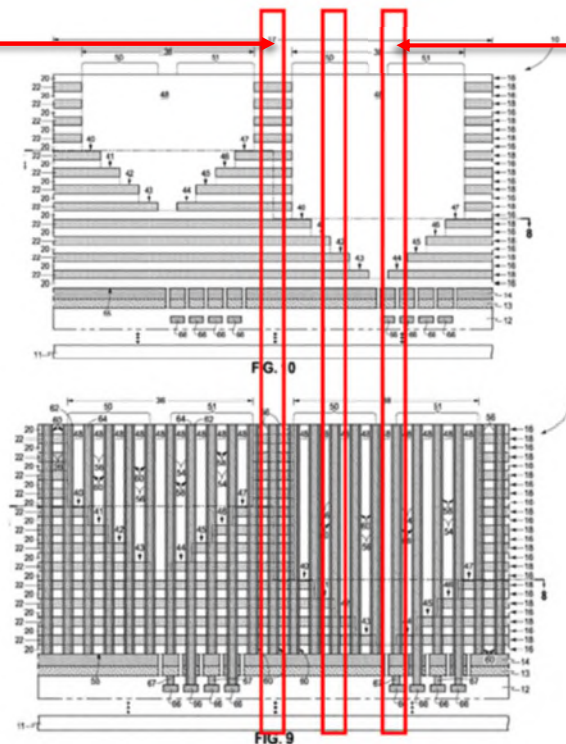
POR, 75 (Reply (Paper 47), 34).

Through the
stack

Through the
dielectric

55 of vertically-alternating tiers 16, 18. In one embodiment, dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously). Regardless, in one embodiment, dummy-structure openings 56 and via openings 54 are formed using a single masking step (e.g., using masking material [not shown] formed atop structure 10). In one embodiment, dummy-structure openings 56 and

*Tessariol, [0037], Figs. 9-10
(Reply (Paper 47), 34-35).*



(D) Patent Owner's Arguments Fail

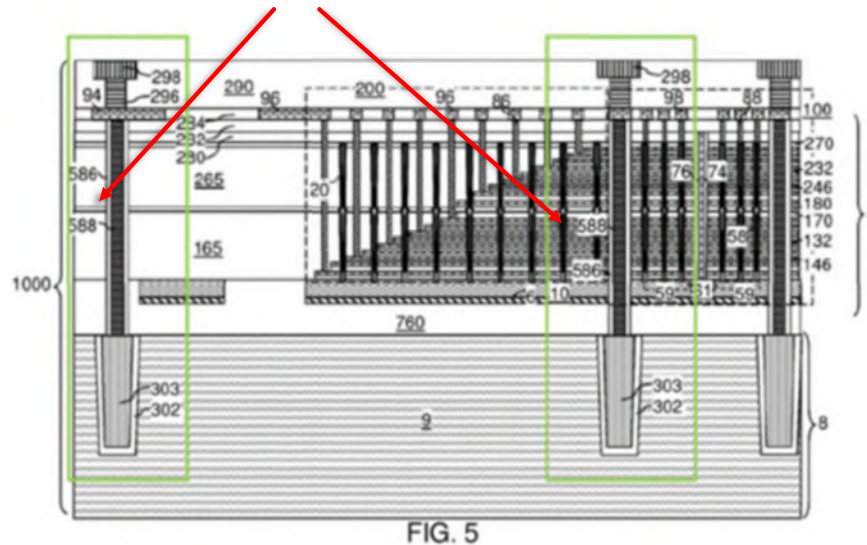
1. Each argument fails for a threshold reason: PO fails to address that forming contacts is "very common" because it overcomes the over-etching problem.
2. PO is incorrect that forming contacts in the peripheral region and in the stack cannot be done with a "common process."
3. PO is incorrect that Mushiga and Nakajima do not describe a "common process."
4. PO is wrong on the law: the prior art figures demonstrate equal-diameters contacts.
5. PO's "missing limitation" argument fails (*supra*).

Reply (Paper 47), 34; POR (Paper 34), 59-68.

(D)(3) Mushiga Describes a Single, Common Process to Form the Contacts

- Mushiga consistently refers to single steps in forming the peripheral contacts and TACs (both 588):

Same contacts



Mushiga, Fig. 5, 10:31-58 (Reply (Paper 47), 38).

Through-memory-level via cavities can be formed through the first and second contact level dielectric layers (282, 280), through the second alternating stack (232, 246), the first alternating stack (132, 146), the second retro-stepped dielectric material portion 265, and/or the first retro-stepped dielectric material portion 165, and through the insulating material layer 760 to a top surface of a respective one of the sacrificial pillar structures 303. An insulating spacer material layer can be conformally deposited and anisotropically etched to form an insulating spacer 586 having a tubular configuration at a periphery of each through-memory-level via cavity. At least one conductive material, such as a combination of a metallic liner and a metal fill material (e.g., tungsten) can be deposited in remaining volumes of the through-memory-level via cavities to form through-memory-level via structures 588. Each through-memory-level via structure 588 can contact a top surface of a respective one of the sacrificial pillar structures 303. The through-memory-level via cavities can be formed before or after formation of the electrically conductive layers (146, 246). For example, the cavities can be formed before formation of the electrically conductive layers (146, 246) and filled with a sacrificial or insulating material before formation of the through-memory-level via structure 588. Alternatively, the cavities can be formed through insulating pillars extending through the alternating stacks after formation of the electrically conductive layers (146, 246).

(D)(3) Nakajima Describes a Single, Common Process to Form the Contacts

- PO argues that Nakajima incorrectly labels the right contact (green) as C4 instead of C3, and thus the common process description does not apply. *POR, 72-73 (Reply (Paper 47), 38-39).*
- There is no clear error: (1) the C3 contacts do not go through the substrate, unlike all labeled C4 contacts, and (2) the C4 contacts consistently go through various amounts of dielectric.

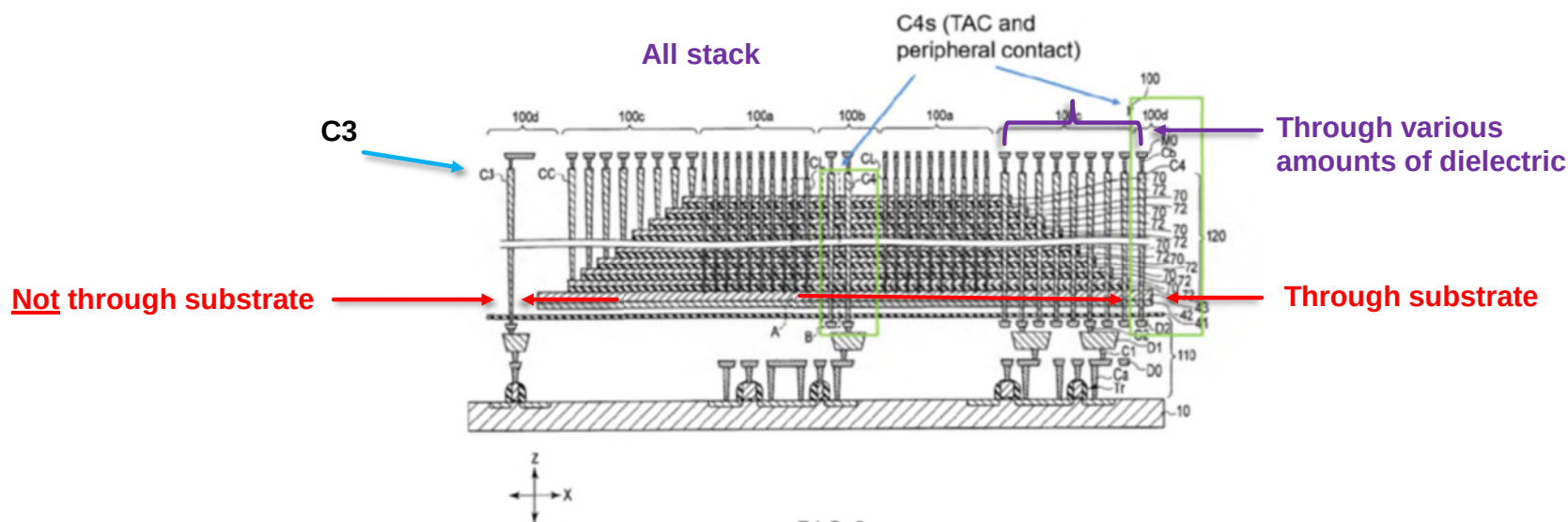


FIG. 2

Nakajima, Fig. 2, 10:31-58 (Reply (Paper 47), 39-40).

(D) Patent Owner's Arguments Fail

1. Each argument fails for a threshold reason: PO fails to address that forming contacts is "very common" because it overcomes the over-etching problem.
2. PO is incorrect that forming contacts in the peripheral region and in the stack cannot be done with a "common process."
3. PO is incorrect that Mushiga and Nakajima do not describe a "common process."
4. PO is wrong on the law: the prior art figures demonstrate equal-diameter contacts.
5. PO's "missing limitation" argument fails (*supra*).

Reply (Paper 47), 34; POR (Paper 34), 59-68.

(D)(4) PO Is Wrong on the Law (1 of 2)

- PO incorrectly argues that it is improper to rely on the figures of Mushiga and Nakajima as evidence that they disclose peripheral contacts and TACs with the same diameter.

POR, 69-70 (Reply (Paper 47), 35-36).

- **First**, it is only improper to rely on figures for precise, "specific dimensions."
 - PO's sur-reply ignores that Petitioner in Nystrom was attempting to prove with figures a "chime length of roughly $\frac{1}{2}$ **to 1 inch** for a whiskey barrel" (specific dimensions having "relative dimensions").

IPR2024-00789, FWD (Paper 37) (10/23/2025) (citing Nystrom v. TREX Co., Inc., 424 F.3d 1136, 1148-49 (Fed. Cir. 2005)) (Reply (Paper 47), 35-36) (Sur-reply (Paper 55), 26).

- **Second**, PO leaves out half the rule: "[P]atent drawings do not define the precise proportions of the elements ... **if the specification is completely silent on the issue.**"
 - **Here, the specification is not silent:** the specifications use the **same numerals** and describe **single steps**.

(D)(4) PO Is Wrong on the Law (2 of 2)

- PO fails to address that CFR 1.84(p)(4) mandates that the same numerals in figures denote the same structures.
- Thus, the common numerals, e.g., in Mushiga, demonstrate that the structures are the same.

CFR 1.84(p)(4) ("same reference character must never be used to designate different parts") (Reply (Paper 47), 36-40).

