Curriculum Vitae

Dr. Marwan Hassoun
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Major Highlights

30+ years of High-Tech Industrial, Academic, Intellectual Property, Entrepreneurship, and Innovation Experience

- MIT Sandbox Entrepreneurship and Innovation Fund –Director of Partnerships with responsibilities including: Creating partnerships and customization of the MIT Sandbox entrepreneurship and innovation program for other institutions with near term focus on Africa; Mentoring student groups at MIT on entrepreneurship, innovation, technology, organization, and intellectual property strategies; Present workshops on technical innovation and intellectual property strategy for startups; Review funding proposals from aspiring startup groups and coach them through prototyping, customer discovery, minimum viable product and fundraising stages; Since 2019, launch a sister innovation and entrepreneurship program in Morocco (as Executive Director of the UM6P Explorer Innovation Fund) including strategic planning, lectures, workshops, training on three campuses, 250+ students and over 20 mentors.
- Founded, co-founded, partnered, launched, and managed multiple technology startups over the last 22 years including RocketChips, KeyEye Communications, MadMax Optics, BooksOnBoard, TraChip, Green Semiconductor, Intellectual Inspiration and Intelligent Metabolomics spanning various technology areas and markets.
- Green Semiconductor Inc., Intellectual Inspiration, Consulting: Intellectual Property, Integrated Circuits, SoCs. Technical evaluation of IP portfolios; Expert witness for 40+ intellectual property, trade secret and technology dispute cases; Development of innovation and IP protection strategies for startups including development of new IP; Consulting with semiconductor companies on various design and strategic matters. Clients include Samsung, Texas Instruments, Qualcomm, Broadcom, MediaTek, STMicro, nVidia, Maxim, Marvell, HTC, ZTE, LG, Comcast, ViaSat, Huawei, Palo Alto Networks, Power Integration, Intellectual Ventures, RPX, Google, Apple, and Western Technology Ventures.
- Senior Vice President of Engineering at KeyEye Communication, Inc. Built and lead a team of 50+ Analog, DSP, Systems and Digital engineers distributed in Sacramento, Minneapolis, Florida, India and Australia to the development of industry's lowest power 10GBASE-T solution. The complex chip included custom DSP, 1Gsps 9-bit quad ADCs, 1Gsps 10-bit DACs, 3.2GHz PLLs and an IFFT/FFT custom ultra-low power processor for Echo/Next cancellation all operating as a single system. Also drove the intellectual property strategy, monetized the portfolio and directly involved in fund raising and M&A activities.
- Sr. Director of Engineering for the Communications Technology Division at Xilinx, Inc. This includes a team of 60+ engineers in Austin, Minneapolis, San Jose and Ames. Responsible for producing the high-speed serial Multi-Gigabit Transceiver technology in the platform FPGAs (Virtex Family) programmable to support over 10 different serial technologies. Producing 1st pass working silicon in extremely advanced process technologies using innovation in architecture, circuits, redundancy, calibration and error correction. Awarded innovation of the year award. Served on Patent Committee.
- President & Managing Partner in TraCHip, LLC, an intellectual property company and monetized various patent portfolios.
- Part of establishing and managing a startup company, RocketChips, INC (investor, partner and Vice President of Wired Products) from inception in 1997 till $280 Million acquisition. Managed multi-company and multi-country (Japan, India and US) IC design products as well as major customers including INTEL, SONY and OKI. Major products included cutting edge high-speed serial transceiver technology.
- Responsible for design of power management IC products and ASICs for mobile phones while

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consulting for Texas Instruments.

- 59 patents granted (42 US and 17 International) and 4 pending (US and International) in the areas of multi-gigabit serial transceivers, Programmable Logic Devices (FPGAs), high-speed high-resolution ADCs and DACs, Memories, RFID, DSP filters, Power Management, Machine Automation and Networking.
- Over 70 technical publications in National and International Journals and Conferences.
- Tenured professor in Electrical and Computer Engineering, Chair of the VLSI group and Co-Founded the Analog and Mixed-Signal VLSI Design Center at Iowa State University. Served as Director of the Center. Attracted sponsorship for the Center from major companies that include Texas Instruments, Honeywell, Rockwell, RocketChips, Non-Volatile Electronics and VTC.
- Established, drove, participated, and negotiated Intellectual Property Strategy at all positions since 1994.

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EXPERIENCE

Jun `17 – Present *Director of Partnerships (since 2020), Mentor (since 2017)*
MIT Sandbox Innovation Fund Program
Massachusetts Institute of Technology, Cambridge, MA
Responsible for creating partnerships and customization of the MIT Sandbox entrepreneurship and innovation program for other institutions with near term focus on Africa. Launched and currently serving as Executive Director at Université Mohammed VI Polytechnique (UM6P Explorer Innovation Fund Program), a sister program in Morocco.

Mar `08 – Present *President, CEO and Founder*
Green Semiconductor, Inc., Austin, TX and
Intellectual Inspiration, Boston, MA (relocated to Boston Area June 2017)
IP and technology consulting firm.

General Areas: Integrated Circuits design and productization (Analog, Digital and Mixed-Signal), Memories, Wired Networking, Processors, RF)
Technical evaluation of IP portfolios; Expert witness for intellectual property, trade secret and technology dispute cases; Development of IP protection strategy for startups including development of new IP through collaboration with companies' executives and engineers; Consulting with semiconductor companies on various design and strategic issues. Clients include Samsung, Texas Instruments, Qualcomm, Broadcom, MediaTek, STMicro, nVidia, Maxim, Marvell, HTC, ZTE, LG, Comcast, ViaSat, Huawei, Palo Alto Networks, Power Integration, Intellectual Ventures, RPX, Google, Apple, and Western Technology Ventures.

Litigation Services: Since 2003 included more than 50 cases retained as an expert witness. The work involved testimony and expert reports on invalidity, validity, non-infringement, and infringement as well as IPRs. The testimony included approximately 20 depositions and 7 court/hearing testimonies with over 50 expert reports authored. List of cases can be furnished upon request.

Aug `20 – Jul `21 *Professor of the Practice*
Department of Electrical and Computer Engineering
Tufts University, Medford, MA
Teaching VLSI (Very Large-Scale Integration) senior/graduate class. CMOS circuit design, structure of transistors, theory of operation, fabrication, state machines, FPGAs, SoCs, processors, memories, system timing.

Mar `03 – Aug `12 *President & Managing Partner*
TraCHip, LLC, Austin, TX
Private intellectual property company.

Mar `08 – Mar `10 *Chief Technology Officer*
Abbey House Media (dba BooksOnBoard), Austin, TX
Web commerce and software development startup focused on digital media including eBooks and Audio Books.

Oct `05 – Mar `08 *Senior Vice President of Engineering*
KeyEye Communications, Inc., Sacramento, CA

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Managed and built an organization with 50+ team members (Analog, Systems, DSP, Digital, Verification, Physical Design) with an innovative, startup oriented, staffing strategy across several design sites (Sacramento, Minneapolis, India and Australia). The result is industry's lowest power 10GBASE-T single chip product. In addition to the management and the vision, had hands-on reasonability for the power architecture, modeling and execution.

Jul `01 – Oct `05 *Senior Director of Engineering, Communications Technology Division*
Xilinx, Inc., Austin, TX

Managed an organization with 60+ team members across 4 sites in analog, digital and mixed-signal IC design, modeling, application engineering, systems engineering, product characterization, product engineering, production test engineering, advanced technologies, layout, CAD and information technology.

- Organizational and technical vision for Xilinx's high-speed serial I/O and ASSP technologies (180nm, 130nm, 90nm, 65nm and 45nm generations). This includes contributing to the vision for UXPi, an industry initiative for evangelizing 10Gbps technology, and the driving of industry standards to support further products.
- Products: Virtex-II PRO X (2 family members), Virtex-4 (5 family members) and RocketPHY (3 non-FPGA family members).
- Technical marketing support for both the platform FPGAs and the ASSPs.
- Customer support and interaction for current and future products.
- Partnership development with several tier 1 and tier 2 companies for process technology, packaging, licensing, high-speed connectors, high-speed backplanes and design. Including establishing industry initiatives at OIF and IEEE committees.
- Involvement in all aspects of the production of IC design including quality assurance and reliability.
- Served on patent committee for the Company.
- Recipient of the innovation of the year award for the Virtex-II Pro X product.

Mar `01 – Jul `01 *Co-Founder, President and CEO*
MadMax Optics, Inc., Austin, TX

Co-Founded the company to produce revolutionary simulation software for the optical component industry. Opened the main design center in Hamden, CT. Guided the company through the seed round financing. This included putting together a 5 year business plan, prospectus and investor presentations.

Aug `98 – Feb `01 *Vice President of Wired Products*
RocketChips, INC., Austin, TX (Acquired by **Xilinx**, Inc. in Nov 2000)

Contributed to the technical, managerial, organizational and marketing leadership for the company's three design centers in Minneapolis (MN), Ames (IA) and Austin (TX). Directly responsible for approximately 35 employees in Wired.

- Products and IP: SERDES and PCS layers for Gigabit Ethernet (IEEE 802.3z, 802.3ab), 2.5Gbps products for serial backplane applications (including OC-48), 10Gbps (IEEE 802.3ae and OC-192), IEEE 1394 and high-speed high-resolution ADCs and DACs (80Ms/s – 250Ms/s).
- Involved with the company since its inception in January 1997 as an early investor and technical and product development through the Iowa State University research work.
- Managed multi-company and multi-country (Japan, India and US) projects as well as major customers including INTEL, SONY and OKI.

Aug `96 - Jul `98 *Contract IC Designer* (Cellular and wireless ICs - power management)
Mixed-Signal Products Group

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Texas Instruments, Dallas, TX
Contract design for mixed-signal power management ASICs for cellular applications. Involved in the design, implementation and test of several high volume production integrated circuits (TPS202X, TPS203X, TPS204X, TPS208X and TPS209X).

Jun `95 - Jul `96 *Contract IC Designer* (Analog-to-Digital Converters)
Defense Systems & Electronics Group
Texas Instruments, Dallas, TX
Investigation and recommendation of a very high-speed high-resolution pipelined multi-path analog-to-digital converter architecture for communication applications.

Aug `00 - Dec `17 **Collaborating Professor**
Department of Electrical and Computer Engineering
Iowa State University, Ames, Iowa
- MS and PhD graduate students and serve on MS and PhD committees at ISU and at University of Texas, Austin.

Aug `94 - Jul `00 **Associate Professor with Tenure**
Department of Electrical and Computer Engineering
Iowa State University, Ames, Iowa
(On leave of absence from Aug 98-Jul 00. Several leaves while consulting for Texas Instruments)

Aug `88 - Jul `94 **Assistant Professor**
Department of Electrical and Computer Engineering
Iowa State University, Ames, Iowa

Research & Teaching
Hired in 1988 by ISU to start the VLSI area in the department. This included establishing research area in VLSI CAD (Symbolic Circuit Analysis, Synthesis Methods for Data Converters) and Analog and Mixed-Signal VLSI (Data Converters, Gigabit speeds Communication Circuits, Magneto-resistive devices).
The largest impact has been the establishment of industrial contacts and the founding of the Analog and Mixed-Signal VLSI Design Center. **The funding commitments on which Dr. Hassoun was a PI or Co-PI have grown to approximately $4.3 Million by 1998.**

Jan `85 - Jul `86 *Software Development Engineer*
Cupertino Integrated Circuits Division,
Hewlett Packard Company
Santa Clara, CA
Design, implementation, and maintenance of circuit design analysis product (HPSPICE).

EDUCATION

Jan 86 - Aug 1988 **Ph.D**. in *Electrical Engineering*, **Purdue University,** West Lafayette, IN.
Thesis: *Symbolic Analysis of Large-Scale Networks*
- Research Assistant (NSF grant) and a Teaching Assistant (VLSI area).

Jan 84 - Dec 1984 **M.S.** in *Electrical Engineering*, **Purdue University,** West Lafayette, IN.
Thesis: A *Study of a Semi-Direct Method for Computer Analysis of Large-Scale Circuits*
- Research Assistant (IBM grant).

Aug 80 -Dec 1983 **B.S.** in *Electrical Engineering*, **South Dakota State University,** Brookings, SD.

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- Teaching assistant during senior year.
- Minor in Computer Mathematics and Computer Science

PATENTS

59 patents granted (42 US and 17 International) and 4 pending (US and International) in the areas of multi-gigabit serial transceivers, Programmable Logic Devices (FPGAs), high-speed high-resolution ADCs and DACs, Memories (RAM), RFID, DSP filters, Power Management, Machine Automation and Networking.

Granted US Patents:

1. Richard Willham, Robert Weber, Marwan Hassoun, "Livestock Record System," U. S. Patent No. **5,322,034**, Jun 21, 1994.
2. Richard Willham, Robert Weber, Marwan Hassoun, "Individual Descriptive Record System," U. S. Patent No. **5,499,626**, Mar 19, 1996.
3. Roy Hastings, Marwan Hassoun, Neil Gibson, Marco Corsi, "Capacitive-summing switch-mode power conversion control," U. S. Patent No. **6,066,943**, May 23, 2000.
4. William Black, Marwan Hassoun, "Non-volatile magnetic circuit," U. S. Patent No. **6,317,359**, Nov 13, 2001.
5. William Black, Bodhisattva Das, Marwan Hassoun, "Non-volatile spin dependent tunnel junction circuit," U. S. Patent No. **6,343,032**, Jan 29, 2002.
6. Yvette Lee, Marwan Hassoun, "Segmented DAC calibration circuitry and methodology," U. S. Patent No. **6,489,905**, Dec 3, 2002.
7. Yvette Lee, Marwan Hassoun, "Current source calibration circuit," U. S. Patent No. **6,507,296**, Jan 14, 2003.
8. William Black, Bodhisattva Das, Marwan Hassoun, Edward Lee, "Nonvolatile programmable logic devices," U. S. Patent No. **6,542,000**, Apr 1, 2003.
9. Weibiao Zhang, Marwan Hassoun, "Apparatus for and method of performing a conversion operation," U. S. Patent No. **6,563,444**, May 13, 2003.
10. Justin Gaither, Marwan Hassoun, "Analog Signal Test Circuit and Method", U. S. Patent No. **6,653,827 B2**, Nov 25, 2003.
11. Ahmed Younis, Marwan Hassoun, "Method and System for VCO-Based Analog-To-Digital Conversion (ADC)," U. S. Patent No. **6,809,676** B1, Oct 26, 2004.
12. Moises Robinson, Shahriar Rokhsaz, Marwan Hassoun, Earl Swartzlander, Jr, "Voltage Controlled Oscillator ", U. S. Patent No. **7,315,220**, Jan 1, 2008.
13. Moises Robinson, Marwan Hassoun, Earl Swartzlander, Jr, "Method and Apparatus for Capacitance Multiplication within a Phase Locked Loop", U. S. Patent No. **7,307,460**, Dec 11, 2007.
14. Marwan Hassoun, Moises Robinson, David Tetzlaff, "Method and Apparatus for Redundant Transceiver Architecture," U. S. Patent No. **7,408,380**, Aug 5, 2008.
15. David Tetzlaff, Erich Goetting, Steven Young, Marwan Hassoun, Moises Robinson, "Method and Apparatus for Providing Frequency Synthesis and Phase Alignment in an Integrated Circuit," U. S. Patent No. **7,499,513**, Mar 3, 2009.
16. David Tetzlaff, Marwan Hassoun, "Method and Apparatus for Dynamic Port Provisioning Within A Programmable Logic Device", U. S. Patent No. **7,598,768**, Oct 6, 2009.
17. James Little, Marwan Hassoun, David Tetzlaff, Chang-Chi Liu, "Combined echo and crosstalk cancellation," U. S. Patent No. **7,920,461**, Apr 5, 2011.

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18. James Little, Marwan Hassoun, David Tetzlaff, Chang-Chi Liu, "Combined echo and crosstalk cancellation," U. S. Patent No. **8,488,438**, Jul 16, 2013.
19. Charles Studor, J. Kevin Nater, Marwan Hassoun, "System and method for managing the generation of brewed beverages using shared resources," U. S. Patent No. **8,515,574**, Aug 20, 2013.
20. Charles Studor, J. Kevin Nater, Marwan Hassoun, "Apparatus and method for brewed and espresso drink generation," U. S. Patent No. **8,688,277**, Apr 1, 2014.
21. James Little, Marwan Hassoun, David Tetzlaff, Chang-Chi Liu, "Combined echo and crosstalk cancellation," U. S. Patent No. **8,947,992**, Feb 3, 2015.
22. Charles Studor, Brent Clafferty, Stephen Miller, Marwan Hassoun, Pete Garcia, Lynn Hamrick, "Frothing assembly and method of operating the same," U. S. Patent No. **8,991,795**, Mar 31, 2015.
23. Charles Studor, J. Kevin Nater, Marwan Hassoun, "System and method for managing the generation of brewed beverages using shared resources," U. S. Patent No. **8,996,178**, Mar 31, 2015.
24. Charles Studor, Raymond Hudy, John Craparo, Marwan Hassoun, "Automated beverage generating system and method of operating the same," U. S. Patent No. **9,533,866**, Jan 3, 2017.
25. Charles Studor, J. Kevin Nater, Marwan Hassoun, "Automated beverage generation system and method of operating the same," U. S. Patent No. **9,545,170**, Jan 17, 2017.
26. Shahriar Rokhsaz, Brian Young, Marwan Hassoun, "Radio frequency identification (rfid) moisture tag(s) and sensors with extended sensing via capillaries," U. S. Patent No. **9,582,981**, Feb 28, 2017.
27. Shahriar Rokhsaz, Brian Young, Ahmed Younis, John Paulos, Abhay Misra, Benjamin Cooke, Marwan Hassoun, "Radio frequency identification (rfid) tag(s) and sensor(s)," U. S. Patent No. **9,607,188**, Mar 28, 2017.
28. Shahriar Rokhsaz, Brian Young, Ahmed Younis, John Paulos, Abhay Misra, Benjamin Cooke, Marwan Hassoun, "Radio frequency identification (rfid) tag(s) and sensor(s)," U. S. Patent No. **9,748,632** Aug 29, 2017.
29. Brian Young, Shahriar Rokhsaz, Ahmed Younis, Marwan Hassoun, "Power harvesting circuit and applications thereof," U. S. Patent No. **9,768,707**, September 19, 2017.
30. Charles Studor, Raymond Hudy, John Craparo, Marwan Hassoun, "Automated beverage generation system and method of operating the same," U. S. Patent No. **9,950,918**, Apr 24, 2018.
31. Shahriar Rokhsaz, Brian Young, Marwan Hassoun, "Radio frequency identification (rfid) moisture tag(s) and sensors with extended sensing via capillaries," U. S. Patent No. **10,069,205**, Sep 4, 2018.
32. John Craparo, Charles Studor, J. Kevin Nater, Jeffrey Mulhausen, Marwan Hassoun, "Facilitating beverage ordering and generation," U. S. Patent No. **10,043,226**, August 7, 2018.
33. Brian Young, Shahriar Rokhsaz, Ahmed Younis, Marwan Hassoun, "Power harvesting circuit and applications thereof," U. S. Patent No. **10,243,479**, Mar 26, 2019.
34. Shahriar Rokhsaz, Brian Young, Ahmed Younis, John Paulos, Abhay Misra, Benjamin Cooke, Marwan Hassoun, "Radio frequency identification (rfid) tag(s) and sensor(s)," U. S. Patent No. **10,243,255,** Mar 26, 2019.

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35. Charles Studor, Brent Clafferty, Stephen Miller, Marwan Hassoun, Pete Garcia, Lynn Hamrick, "Frothing assembly and method of operating the same," U. S. Patent No. **10,271,680**, Apr 30, 2019.
36. Charles Studor, Raymond Hudy, John Craparo, Marwan Hassoun, "Automated beverage generation system and method of operating the same," U. S. Patent No. **10,315,908**, Jun 11, 2019.
37. Charles Studor, J. Kevin Nater, Marwan Hassoun, "Automated beverage generation system and method of operating the same," U. S. Patent No. **10,638,870**, May 5, 2020.
38. Shahriar Rokhsaz, Brian Young, Marwan Hassoun, "Radio frequency identification (rfid) moisture tag(s) and sensors with extended sensing via capillaries," U. S. Patent No. **10,734,727**, Aug 4, 2020.
39. Charles Studor, Brent Clafferty, Stephen Miller, Marwan Hassoun, Pete Garcia, Lynn Hamrick, "Frothing assembly and method of operating the same," U. S. Patent No. **10,966,565**, April 6, 2021.
40. Shahriar Rokhsaz, Brian Young, Marwan Hassoun, "Radio frequency identification (rfid) moisture tag(s) and sensors with extended sensing via capillaries," U. S. Patent No. **11,205,851**, Dec 21, 2021.
41. John Craparo, Charles Studor, J. Kevin Nater, Jeffrey Mulhausen, Marwan Hassoun, "Facilitating beverage ordering and generation," U. S. Patent No. **11,250,524**, Feb 15, 2022.
42. Shahriar Rokhsaz, Brian Young, Marwan Hassoun, "Radio frequency identification (rfid) moisture tag(s) and sensors with extended sensing via capillaries," U. S. Patent No. **11,817,637**, Nov 14, 2023.

Granted International Patents:

43. R. Hastings, M. Hassoun, N. Gibson, M. Corsi, "Capacitive-summing switch-mode power conversion control and method," **EP0993104**, Jan 14, 2009
44. R. Hastings, M. Hassoun, N. Gibson, M. Corsi, "Method and control for capacitive totalization in a switching part," **AT421184**, Jan 15, 2009
45. R. Hastings, M. Hassoun, N. Gibson, M. Corsi, "Method and control for capacitive summation in a switched-mode power supply," **DE69940292**, Mar 5, 2009
46. M. Robinson, M. Hassoun, E. Swartzlander Jr, "Method and apparatus for capacitance multiplication in a phase-locked loop," **JP4856191**, Jan 18, 2012
47. E. Swartzlander Jr, M. Robinson, M. Hassoun, "Method and apparatus for capacitance multiplication within a phase locked loop," **CN101326721**, Mar 6, 2013
48. M. Robinson, M. Hassoun, E. Swartzlander Jr, "Method and apparatus for capacitance multiplication within a phase locked loop," **CA2632006**, Jul 16, 2013
49. C. Studor, J. K. Nater, M. Hassoun, "Apparatus and method for brewed and espresso drink generation," **EP2651270**, Feb 15, 2017
50. C. Studor, J. K. Nater, M. Hassoun, "Apparatus and method for brewed and espresso drink generation," **CN103596473**, May 17, 2017
51. C. Studor, R. Hudy, J. Craparo, M. Hassoun, "Automated beverage production system and method of operating the same," **JP6262329**, Jan 17, 2018
52. C. Studor, J. K. Nater, M. Hassoun, "Apparatus and method for brewed and espresso drink generation," **KR101859595**, May 18, 2018
53. J. Craparo, C. Studor, J. K. Nater, J. Mulhausen, M. Hassoun, "Promotion of ordering and production of beverages," **JP6409119**, Oct 17, 2018

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54. C. Studor, J. K. Nater, M. Hassoun, "Apparatus and method for brewed and espresso drink generation," **KR101970614**, Apr 19, 2019
55. C. Studor, J. K. Nater, M. Hassoun, "Automatic beverage production system, method and storage medium," **JP6672135**, Mar 25, 2020
56. J. Craparo, C. Studor, J. K. Nater, J. Mulhausen, M. Hassoun, "Beverage ordering and production promotion," **JP6686089**, Apr 22, 2020
57. C. Studor, R. Hudy, J. Craparo, M. Hassoun, "Automated beverage production system and method of operating the same," **KR102242855**, Apr 21, 2021
58. C. Studor, J. K. Nater, M. Hassoun, "Automatic beverage manufacturing method, system and computer readable storage medium," **CN107369254** , Jul 27, 2021
59. C. Studor, J. K. Nater, M. Hassoun, "Apparatus and method for brewed and espresso drink generation," **EP3175744**, Nov 29, 2023

GRANTS AND CONTRACTS

-During academic career from 1988 – 1998, secured 25 research grants while at Iowa State University and as part of the Analog and Mixed-Signal VLSI Design Center totaling approximately **$4.3 Million** from 1988- 1998. The sponsors included: Texas Instruments, Honeywell, Rockwell, RocketChips, Computing Devices International, Control Data Corporation (CDC), Defense Advanced Research Projects Agency (DARPA), National Science Foundation, Carver Trust Foundation, US Department of Education, Center for Non-Destructive Evaluation

1. Co-Principal Investigator (with Black, W., Lee, E. and Geiger, R.), "Mixed-Signal Circuits Laboratory," Carver Trust Foundation, **$1,000,000** (includes $500,000 required matching from Iowa State University), August 1998 - July 2000.
2. Principal Investigator (with Geiger, R., Black, W. and Lee, E.), "Analog and Mixed-Signal Center Membership," Texas Instruments, Inc., **$1,000,000**, Jan 1998 - Dec 2000 (continuation of grant 9).
3. Co-Principal Investigator (with Black, W., Lee, E.K.F. and Geiger, R.), "High Density and Low-energy Magneto-resistive Memory Circuits," Honeywell, Inc. (DARPA), **$151,091**, Sep 1997 - Dec 1998.
4. Co-Principal Investigator (with Geiger, R., Black, W., Lee, K., Wright, C.), "Restructuring Basic Electronic Circuits Education Around Integrated Circuit Technology of the 1990s," National Science Foundation Instrumentation and Laboratory Infrastructure Program **$200,000,** Aug 1997 - Jun 1999.
5. Co-Principal Investigator (with Black, W., Geiger, R., Lee, E.), Honeywell, Inc**.** (DARPA), **$22,400,** "Testing of Magneto-resistive Structures," Feb 1997 - April 1997 (continuation of grant 8).
6. Co-Principal Investigator (with Black, W., Geiger, R., Lee, E, Bergland, D., Sapatnekar, S., Tridandapani, S. and Weber, R.), "Gigabit Silicon Integrated Circuits," RocketChips, Inc., **$1,000,000**, Jan 1997 - Dec 2001.
7. Principal Investigator, "Linear IC Product Design", Texas Instruments, Dallas, TX, **$110,000**, Sep 96 - Aug 97.
8. Co-Principal Investigator (with Black, W., Geiger, R., Lee, E., Honeywell, Inc. (DARPA), **$100,000**, "Magneto-resistive Memories," May 1996 - April 1997.
9. Co-Principal Investigator (with Geiger, R., Black, W., Hassoun, M., and Lee, E., Texas

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Instruments, Inc., **$450,000**, "Analog and Mixed-Signal Center Membership," Jan 1996 - Dec 1998.

10. Principal Investigator (with Geiger, R., Lee, E. and Black, W., Rockwell International Inc., **$300,000**, "Analog and Mixed-Signal Center Membership," Aug 1996 - Dec 1999.
11. Principal Investigator, "Verification of a Pipeline Analog to Digital Converter for Communication", Texas Instruments, Dallas, TX, **$10,017**, Jan 96 - Aug 96 (continuation of grant 11).
12. Principal Investigator, "Pipeline Analog to Digital Converter for Communication", Texas Instruments, Dallas, TX, **$27,755**, Aug 95 - Aug 96.
13. Principal Investigator, "An Investigation of a Pipelined Analog-to-Digital Converter", Texas Instruments, Dallas, TX, **$37,105**, Jun 95 - Aug 95.
14. Co-Principal Investigator (with Richard Hester), "Low Power Analog-To-Digital Converter", Texas Instruments, Dallas, Texas, **$27,000**, Aug 93 - May 95.
15. Principal Investigator (with Jim Davis), "High Speed Multi-Protocol ActiveBus Prototype Development," Computing Devices International, Bloomington, Minnesota, **$2,500**, Aug 93-Dec 93 (continuation of grant 16).
16. Principal Investigator (with Jim Davis), "High Speed Multi-Protocol ActiveBus Prototype Development," Computing Devices International, Bloomington, Minn, **$15,000**, Aug 92-Aug 93.
17. Co-Principal Investigator (with V. Dalal, S. Burns, H. Hsieh, R. Weber, P. Garikepati), "Graduate Assistance in Microelectronics and Photonics," Department of Education, Washington, D.C., **$351,000**, Aug 90-Aug 93.
18. Principal Investigator, "Symbolic Analysis of Nonlinear Large-Scale Systems," Engineering Research Institute, Ames, Iowa, **$3,848**, Oct 92- Jul 93.
19. Faculty Associate (with Charles Wright, Jr.), "A laboratory to Support Computer-Aided Digital Systems Design," National Science Foundation Instrumentation and Laboratory Improvement Program, **$218,317**, Aug 90-Aug 92.
20. Principal Investigator, "Symbolic Sensitivity Analysis of Large-Scale Circuits," University Research Initiation Grant, Ames, Iowa, **$6,600**, Jul 91-Jun 92.
21. Principal Investigator, "Symbolic Circuit Simulation in the Time Domain," Engineering Research Institute, Ames, Iowa, **$4,240**, Oct 91- Jun 92.
22. Principal Investigator, "Application of VLSI Circuit Partitioning Technique to Dynamic Clustering of Distributed Multiprocessor Systems," Engineering Research Institute, Ames, Iowa, **$1,660**, Oct 90-Jun 91.
23. Co-Principal Investigator (with Art Pohm and Jim Davis), "Design of a New High Speed Serial Bus," Control Data Corporation (CDC), Minneapolis, Minnesota, **$114,000**, Aug 89-Dec 91.
24. Principal Investigator, "Investigation Proposal for Hardware Implementation of Non-Destructive Evaluation software," Center for Non-Destructive Evaluation, Ames, Iowa, **$5,000**, Aug 89-Jun 90.
25. Principal Investigator, "ASIC Hardware for Image Processing Applications," Engineering Research Institute, Ames, Iowa, **$4,000**, Oct 89- Jun 90.

GRADUATE STUDENTS

Major Professor for **26 Graduate Students** (8 PhDs and 20 *MS* (all thesis option)) from 1988 – 2005.

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TECHNICAL PUBLICATIONS

Authored or co-authored over 70 technical publications in Technical Journals, Conferences and six chapters of three different books on circuit analysis.

Refereed Journals

1. Jorgenson, J., Hassoun, M., Hsu, H., "Breakdown Verification for Fault Modeling in Laminate Microstrip Conductors," *International Journal of Microelectronics and Electronic Packaging*.
2. Zhang, R., Hassoun, M., Black, W., Das, B, Wong, K, "Demonstration of a Sensing Four States From A Single Pseudo-Spin Valve GMR Device," *IEEE Transactions on Magnetics*.
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   2) "Hierarchical Symbolic Analysis of Large-Scale Circuits."
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   Editor: Wai-Kai Chen
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INVITED TECHNICAL PRESENTATIONS

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Over 100 technical presentations at various conferences, workshops, Universities and companies, including workshops at MIT, UM6P, Texas A&M, University of Texas at Austin, Stanford, Iowa State University, Innography, HP, Texas Instruments, Rockwell International, Honeywell, CDC, and Non-Volatile Electronics.

HONORS AND AWARDS

Recipient: Distinguished Engineer Award, South Dakota State University
Recipient: Innovation of the year award, Xilinx, Inc.
Nominee: Iowa State University Faculty of the Year award
Inductee: Senior member Institute of Electrical and Electronics Engineers (IEEE)
Recipient: Warren Bost Teaching Award, Iowa State University
Nominee: ISU Foundation Early Teaching Achievement Award
Nominee: ISU Foundation Early Teaching Achievement Award
Inductee: Eta Kappa Nu (Electrical Engineering Honor Society)
Inductee: Tau Beta Pi (Engineering Honor Society)
Inductee: Phi Kappa Phi (National Honor Society)
Inductee: Alpha Lambda Delta (Freshman Honor Society)

PROFESSIONAL ACTIVITIES

Standards – Participant and voter on IEEE 802 Standards Committee (802.3 group).

Conferences & Workshops – Served as conference chair, on technical program committees, on organizing committees, publicity chair, special sessions chair and steering committees for more than 20 occasions covering more than 7 conferences and workshops.

Reviewer – Editor and Referee for IEEE, IEE and other journals in the area of VLSI and circuits and systems.

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