UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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ARM LTD., MEDIATEK INC,

Petitioners,

v.

DAEDALUS PRIME LLC,

Patent Owner.

_____

Case No.: IPR2025-00207

U.S. Patent No. 8,984,228

_____

DEPOSITION OF MARWAN HASSUON, PH.D.

Via Zoom Videoconference

Wednesday, November 12, 2025

Stenographically Reported by:

JUSTYNE N. JOHNSON

RPR, CSR. No. 14301

Job No. 608607

Pages 1-88

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The Deposition of MARWAN HASSUON, PH.D., was taken on behalf of Patent Owner, all parties appearing remotely via Zoom videoconference, beginning at 10:04 a.m., Pacific time, on November 12, 2025, before JUSTYNE JOHNSON, RPR, Certified Shorthand Reporter No. 14301.

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APPEARANCES:

FOR PATENT OWNER:

ASCENDA LAW GROUP, PC
BY: TAREK N. FAHMI, ESQ.
Attorney at Law
2010 North First Street
Suite 420
San Jose, California 95131
408.799.0612

FOR PETITIONERS:

DUANE MORRIS, LLP
BY: KEVIN P. ANDERSON, ESQ.
Attorney at Law
901 New York Avenue NW
Suite 700 East
Washington, D.C. 20001
202.776.7800

ALSO PRESENT:

Justin Ramirez-Hale, Exhibit Technician

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EXHIBIT 1008 United States Patent 26
Application Publication
No. US 2008/0126750 A1

INFORMATION TO BE SUPPLIED

(None)

WITNESS INSTRUCTED NOT TO ANSWER

(None)

TRANSCRIPT REQUESTED TO BE MARKED

(None)

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November 12, 2025| 10:04 a.m.

EXHIBIT TECHNICIAN: Thank you to everyone for attending this proceeding remotely, which we anticipate will run smoothly. Please remember to speak slowly and do your best not to talk over one another. Please be aware that we are recording this proceeding for backup purposes.

Any off-the-record discussions should be had away from the computer. Please remember to mute your mic for those conversations. Please have your video enabled to help the reporter identify who is speaking. If you are unable to connect with video and are connecting via phone, please identify yourself each time before speaking. We will provide a complementary, unedited recording of this deposition with the purchase of a transcript.

I apologize in advance for any technical-related interruptions. Thank you.

THE STENOGRAPHER: One moment.

MR. ANDERSON: I think the witness is trying to speak, but I don't hear anything from the witness. Can anybody else hear?

MR. FAHMI: No.

THE WITNESS: The headphones. How about now?

MR. ANDERSON: Okay. We can hear you now. Yeah.

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THE WITNESS: I'll stick with this.

THE STENOGRAPHER: One moment.

Good morning. We are going on the record at 10:04 a.m., on Wednesday, November 12, 2025, in the matter of Arm Ltd., v. Daedalus Prime LLC, in the matter of IPR2025-00207. Today's deposition is taking place remotely via Zoom videoconference.

My name is Justyne Johnson. I am a California certified shorthand reporter representing the firm Planet Depos, and my certification number is 14301. The deponent is Marwan Hassoun, Ph.D.

Counsel, can you please introduce yourselves.

MR. FAHMI: Good morning. This is Tarek Fahmi on behalf of the patent owner, Daedalus Prime.

MR. ANDERSON: And this is Kevin Anderson from Duane Morris on behalf of the Arm petitioner.

THE STENOGRAPHER: Dr. Hassoun, can you raise your right hand, please?

MARWAN HASSUON, PH.D.,

having first been sworn by the Certified Shorthand Reporter, was examined and testified as follows:

THE WITNESS: I do.

THE STENOGRAPHER: Go ahead, sir.

MR. FAHMI: Thank you.

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EXAMINATION

BY MR. FAHMI:

Q Good morning, Dr. Hassoun. Thank you for appearing for deposition today. Can you hear me okay?

A I can hear you fine.

Q Great. As I mentioned, my name's Tarek Fahmi. I'll be taking today's deposition, and I represent the patent owner, Daedalus Prime.

And as the court reporter mentioned, we're here today in connection with Inter Partes Review Number 2025-00207 in the U.S. Patent and Trademark Office, and that concerns U.S. Patent 8,984,228.

You provided a declaration in connection with this proceeding; is that right?

A Yes.

Q Have you ever given deposition testimony in a proceeding such as this before, Dr. Hassoun?

A Yes.

Q More than once?

A Yes.

Q I'll just remind you of a couple things, then. During today's deposition, I'll be asking a series of questions. And if at any time you either didn't hear a question or didn't understand it, just let me know. I'll be happy to repeat it or try to clarify it, if needed.

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Is that okay?

A Yes.

Q And as you're doing, if you would please wait until I finish asking the question before you give your answer, I'll try and do likewise and wait until you've finished your answer before asking another question. That way the court reporter has an easier time taking down what each of us is saying.

Is that all right?

A Yes.

Q Do you have any materials in the room with you today, Dr. Hassoun?

A What I have is on the computer. Mr. Anderson asked me -- sent me all the clean copies of all the exhibits. So that's what I have on my desktop.

Q Okay. Those are the exhibits that are referenced in your declaration; is that right?

A Yes. I'm not sure every one of them was, but there are a list of exhibits that Mr. Anderson sent me.

Q Okay. Can you let me know what those are, please?

A So I have Exhibit 1001, 1002, -3, -4 -- okay. Let me keep going. -18, -19... all the way through -24. So Exhibits 1001 through Exhibits 1024. And then I have IPR2025 -- there -- there's that warn -- the fire alarm, I

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was saying. I think we're going to have to take a 15-minute break. I apologize.

MR. FAHMI: No problem, sir. We'll break until you're back.

THE WITNESS: Thanks.

MR. FAHMI: Let's go off the record.

THE STENOGRAPHER: Off the record at 10:09 a.m.

(Off the record.)

THE STENOGRAPHER: Back on the record at 10:14 a.m.

MR. FAHMI: Thank you.

BY MR. FAHMI:

Q Dr. Hassoun, when we broke, you were telling us the list of materials that you have on the computer. I think you'd indicated that you had Exhibits 1001 through 1024, and then there were some other materials that you just started to mention.

A Okay. So the next one is IPR2025-00207 order institution.PDF. The next one is IPR2025-00207 order vacating denial.PDF, and then I have P9 IPR2025-00207 petitioner's response patent owner's request for disce- -- discretionary denial of institution.PDF, and the last one is petition for inter partes review of U.S. Patent Number 8984228.PDF.

Q Thank you. Are those documents unmarked, meaning

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there's no annotations or anything like that?

A To my knowledge, yes, these are clean. I did not open them yet.

Q Okay. And to your knowledge, they're true and correct copies of the documents that are on file with the USPTO; is that right?

A To the best of my knowledge as they are presented to me.

Q Is there anyone else in the room with you today, Dr. Hassoun?

A No.

Q Okay. Just a reminder that during today's deposition, you should not have any side channel communications with anyone, including Mr. Anderson, meaning no side channel communications on a chat or instant message, or anything like that.

Do you understand?

A Understood.

Q And while you're providing testimony today, you should not discuss the substance of your testimony with anyone, including Mr. Anderson, even during the break. Do you understand?

A Yes.

Q Is there any reason why you cannot give your full and honest and complete testimony in this proceeding

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today?

A No.

Q If at any time you need to take a break, just let us know, and we'll be happy to pause. Otherwise, if you're ready, we'll get started. Is that okay?

A Yes.

Q Can you tell me your current affiliations with any academic or private industry organizations?

A Sure. I have an appointment at MIT, a Massachusetts Institute of Technology. I'm the director of partnerships for the Sandbox Innovation Fund. That's my academic affiliation.

I also am the president of Intellectual Inspiration, which is my own consulting firm. And it's -- that's a d/b/a. Official name of the company is Green Semiconductor Incorporated.

(Mr. Ramirez-Hale left the videoconference.)

THE STENOGRAPHER: The technician just left. Should we go off the record?

(Mr. Ramirez-Hale joined the videoconference.)

THE STENOGRAPHER: Oh, he just joined.

MR. FAHMI: Okay.

THE STENOGRAPHER: I'm so sorry.

MR. FAHMI: That's all right. These things happen.

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BY MR. FAHMI:

Q Dr. Hassoun, in terms of your academic appointment at MIT, are you teaching any classes?

A I am not teaching any cla- -- official classes, no.

Q Is there anything unofficial that would have you teaching anything at the moment?

A Well, yes. It's -- the format of the Sandbox Innovation Fund is to work with startups -- student startups coming out of MIT. So we meet in small groups and advise those students on an individual basis. So it's a different paradigm of teaching, if you will.

Q Do any of those advisory roles that you're currently doing have anything to do with the subject matter of the '228 patent?

A No, none that I recognize. We deal with a lot of teams, but I'm pretty sure the ones on my -- advising have nothing to do with the subject matter.

Q And in terms of Intellectual Inspiration, your consulting firm, what sort of consulting are you doing?

A So some of it is, like, the function I'm serving right now, which is as an expert witness for IPRs, patent infringement cases, and trade secret cases. And I do have an arbitration case I have done. So that's part of the consulting.

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Another piece is focused on some technology for startups, which comes and goes. Right now, given my responsibility, I have none of those that are active. And the third aspect is consulting on patents -- patent portfolios and evaluating those for particular clients.

Q Does any of your current consulting work, other than in connection with the present IPR proceeding, have anything to do with the subject matter of the '228 patent?

A No, none.

Q Other than in connection with the present proceeding, do you have any professional affiliation with Arm Ltd.?

A I do not.

Q Have you had any such affiliation in the past?

A So I believe I've done an IPR in the past on behalf of Arm. And perhaps 20 years ago, we were looking at licensing an Arm core, which we never did.

Q What -- when you say "we were looking at licensing," who's the "we" in that sentence?

A So that was at KeyEye Communications, one of the companies I was working for at the time. It's a startup.

Q The other IPR matter that you worked on in connection with Arm, do you recall what that case was?

A I do not recall what that case was. No. It's in my CV, I believe. We can look it up, if we need to.

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Q Sure. Do you have a copy of your CV? That's Exhibit 1004.
A I do. Want me to open it?
Q Please.
THE STENOGRAPHER: Did you want me to mark that as well?
MR. FAHMI: No. That's fine, Justyne. Everything's been premarked, so we're good. Thanks.
THE WITNESS: Okay. I have it open.
BY MR. FAHMI:
Q And do you see that other IPR listed anywhere in the CV?
A No. I apologize. I don't see it. I don't have a listing of all the matters in the CV. So no, it's not in there.
Q Do you remember what the subject matter was?
A I don't. It's been a while. I'm sure it had to do with processors, but I do not recall the specifics.
Q Have you ever testified on behalf of or against the current patent owner, Daedalus Prime, in any proceeding?
A Not that I recall, no.
Q In connection with this matter, do you recall who retained you to provide testimony?
A Yes. Mr. Kevin Anderson.

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Q When was that? Do you remember?

A That would have been about a year and a half ago or so. I know -- I think the report -- the declaration was done in December of last year -- November, December, from my recollection. So it was a few months before that. That's where I get approximately, yeah, 15 to 18 months, I would say.

Q What were you asked to do when you were retained in this matter?

A I was asked to review the '228 patent and the material for that '228 patent, including prior art, and write a declaration with my opinion on the validity of certain of the claims of the '228 patent.

Q Other than the materials that are discussed in your declaration, did you review any other materials in connection with that retention?

A Not that I recall right now. No.

Q For the materials that are referenced in your declaration, were they provided to you for review, or did you conduct an independent investigation to locate those materials?

A I believe most of them were provided to me. I might have located some references that got included in there. But as I sit here today, I do not recall that -- you know, which is which.

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Q Have you done any preparation for today's deposition?
A I have.
Q What did you do?
A So I reviewed my declaration. I also reviewed the -- some of the IPR documents. For example, the institution decision for the '228. I also reviewed the '895 IPR material, including -- there was a declaration in -- final decision for that one. Those are the ones I recall.
I also read the patents and publications referenced in my report and my declaration. I also met with Mr. Anderson over the last couple of days.
Q Do you know approximately how much time you've spent in total preparing for today's deposition?
A It's a rough guess, between 30 to 40 hours would be my rough guess for it.
Q I'd like to turn to Exhibit 1007. This is the Blumrich reference. Do you have that with you?
A Yes. I've opened it.
Q Okay. You've seen this reference before; is that right?
A That is correct.
Q Okay. And you offered testimony concerning Blumrich as part of your declaration; is that right?

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A That is correct.
Q I'd ask you to turn to paragraph 118.
A Yes.
Q In paragraph 118, Blumrich is indicating the L2 as a "Point of Coherence." And then in the next paragraph, that is reiterated, saying, "the L2 caches serve as the point of coherence for all processors."
Do you see that?
A Yes.
Q In this context, what does that mean, "the point of coherence"?
A I would have to read that description to answer that question. Would you like me to do so?
Q Please.
A So the L2 Point of coherence in paragraph 119, line 4, it says "This function includes generating L1 individualizations when necessary," full stop. "Because the L2 caches are inclusive of the L1s, they can remember which processors could possibly have a valid copy of every line," full stop. "Memory consistency is enforced by the L1 [sic] slices by means of multi-casting selective L1 individualizations [sic], made possible by the fact that the L1s operate in write-through mode and the L2s are inclusive of the L1s."
So that's the description of what they mean by

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"Point of coherence."

Q What would a person of ordinary skill in the art understand this passage to be saying?

A Exactly what it says. It's be -- performing functions related to memory consistencies through, you know, the L2 -- enforced by the L2 slices.

Q What do you mean "the L2 slices"?

A That's what it says here. It says, "memory consistency is enforced by the L2 slices by means of multi-casting selective L1 individualization [sic]." So it's talking about L2 and portions of the L2.

Q You -- you said "individualizations." My copy reads "L1 invalidations."

A I apologize. It's "invalidations." My eyesight isn't that good.

Q That's fine. I just wanted to make sure we were looking at --

A Oh. It is "invalidations."

Q Would a person of ordinary skill in the art have an understanding of what "L2 slices" means in this context?

A I would need to further read the reference to tell you exactly what it means in light of this particular specification.

Q Does the phrase "L2 slices" have a recognized

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understanding or meaning in the art?

A It could be, yes. But this happens to be a patent publication, and the specification really is what I would go to first to explain what an L2 slice means in light of this particular patent application.

Q If you look at the top of the column that we've been looking at in paragraph 111, there's a discussion of the L2 storing data in 128-byte wide lines," and each of those lines being located in a single L2 slice.

Do you see that?

A Yes.

Q Does this inform your view of what the phrase "L2 slice" means in connection with this patent application?

A Yes. It indicates that 128-byte wide line "is located in a single L2-slice." So the L2 slice in -- I apologize. It was supposed to be done. Maybe it is. Let's keep going.

Q Oh, I'm -- I'm sorry. We didn't hear anything, but I -- are you saying the fire drill might be taking place?

A I just heard it again. It went away quickly, so we can continue.

Q Okay. Let -- let us know if you need to leave.

A You know, can we take a ten-minute break? Let me just investigate.

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Q Yeah. Of course.
A Thank you.
MR. FAHMI: Let's go off the record.
THE WITNESS: Thank you.
THE STENOGRAPHER: Off the record at 10:39 a.m.
(Off the record.)
THE STENOGRAPHER: Back on the record at 10:45 a.m.
BY MR. FAHMI:
Q Dr. Hassoun, we were discussing paragraph 111 of the Blumrich reference. And I think I had asked whether it informed your opinion about what an "L2 slice" means in the context of this patent application.
A Yes.
Q And can you tell us, then, what an "L2 slice" means in the context of this patent application?
A So it's at least 128-bit-wide line where each one is included in an L2 slice, so... that's what it is.
Q So do I understand correctly that an L2 slice is a portion of cache memory for a processor?
A Yes. L2 is a cache slice.
Q Sorry. You said "L2 is a cache slice." We will --
A L2 is a cache -- sorry. I didn't mean to speak over you.

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Q No. No. No. It's fine. Go ahead.
A So the -- there's an L2 cache, and the L2 cache is made up of L2 slices. And the L2 is a cache for a processor. Yes.
Q L- -- "L2" is short for level 2; is that right?
A Yes.
Q And that's a level in a cache hierarchy for this particular processor, is that correct?
A That is correct.
Q Is it the case that the lower the number in terms of an L designation, the further away from the processor core the cache is situated?
I'm sorry. I probably said that incorrectly. The lower the number in the L designation, the closer to the core the cache would be to that core; is that correct?
A The -- generally, the L1 through L3 designation, or higher numbers, refers to an access order from the processor. So to the extent that's what you mean, then that's what these numbers mean.
Q So if I understand you correctly, an L1 cache would be accessed before an L2 cache before an L3 cache; is that right?
A That's generally the understanding of, you know, a cache hierarchy. But you'd have to look at the particular implementation to see how an architecture or

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that algorithm uses those caches.

Q If I can have you look at paragraph 124 of Blumrich, there's mention of an IBMBlueGene processor.

Do you see that?

A Yes.

Q Are you familiar with the IBMBlueGene processor?

A I am not.

Q Paragraph 124 indicates that "the prior version of the IBMBlueGene processor used snoop filtering to maintain cache coherence."

Do you see that?

A I do.

Q And then in the next paragraph, Blumrich says "The embodiment discussed herein uses directory-based coherence."

Do you see that?

A I do.

Q Is there a difference between snoop filtering to maintain cache coherence and directory-based coherence?

A I don't know without looking up "snoop filtering" and the particular patent appli- -- patent they've referenced in paragraph 124.

Q Okay. If you look at the prior paragraphs, 121, 122, does that indicate a distinction between these snoop-filtering coherence and directory-based coherence?

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A So what -- you know, paragraphs 120, 121, and 122 -- they are speaking of general description of a directory-based coherence, and then it's describing snooping. The concept of snooping is -- as explained here, doesn't preclude it from being used in directory-based coherence. Again, it -- it's -- depends on how you architect the system. So even the concept of directory-based coherence, keeping a table of -- that indicates where in the status of a memory line, if you will, is also prevalent in any system that's doing cache coherence.

So the implementation is real -- the details of the implementation is what's really important to determine what's, say, the predominant way of doing the control or doing the cache coherence.

Q In directory-based coherence, a common directory is used to track and manage the data; is that right?

A Again, you're going to -- you know, I'd need to look at the system. But generally, it is. But as I say, that doesn't preclude the function of snooping being used as part of the implementation. Also, the directory could be distributed directorally [sic] versus a centralized directory. So, again, it's all dependent on the implementation.

Q Blumrich doesn't talk about the directory being

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distributed, does it?

A I would have to read Blumrich again to verify that statement.

Q You reviewed this reference as part of your almost 40 hours of preparation for the deposition, didn't you?

A I did, yes.

Q But you don't recall whether the reference discusses whether or not the directory can be distributed at this time; right?

A I do not, I'm afraid.

Q Would it surprise you to learn that there is no such mention of a distributed directory in Blumrich?

A Wouldn't surprise me either way. As I said, it's an implementation detail for a -- the system.

Q In a snooping-based system, coherence relies upon monitoring a shared bus; is that correct?

A A snooping-based system, my unders- -- again, I would need to look at the particular implementation to answer you how that snooping is being done. If I look at what this particular reference used to define "snooping," it talks about snooping as the process where the individual caches monitor address lines for accesses to memory locations that they have cached.

And then it continues saying, "When a write

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operation is observed to a location that" is -- to a location that "a cache has a copy of, the cache controller invalidates its own copy of the snooped memory region."

So that's what this reference is talking about when it comes to snooping. So how that snooping is implemented, I don't see that in that particular paragraph. And again, I would have to look into -- which I have not read -- U.S. Patent Number 7,386,685, which the reference talks about using snoop filtering to maintain cache coherence.

Q I see. So you didn't look at the '685 patent, which is referenced here, as part of your analysis to prepare your declaration; is that right?

A That is correct.

Q In paragraph 128, Blumrich says, "The request queue 302 buffers incoming read and write requests."

Do you see that?

A I do.

Q Those are read and write requests from a processor core; is that right?

A That would be my understanding, yes.

Q Let's turn to the Sistla reference. That's Exhibit 1008, please. If you can bring that up.

A Okay. I have it open.

Q Can I have you turn to paragraph 30, please?

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A Yes.
Q Just to be clear, Sistla was one of the references that you discussed in your declaration; is that correct?
A Yes, I relied on Sistra [sic] for an obviousness combination for a particular feature.
Q In paragraph 30, there's a discussion of an "on-die interconnect 320."
Do you see that?
A Yes.
Q And I think Sistla indicates that this on-die interconnect couples core-cache clusters; is that right?
A I'm sorry. I missed the last -- the word before "clusters." What --
Q Mm-hmm.
A Can you repeat what you said?
Q Core -- I'm sorry. Core-cache clusters. It's a hyphenated term, I think, in paragraph 30.
A Okay. So what's the whole question again?
Q Right. I think paragraph 30 is indicating that this on-die interconnect 320 is used to couple the core-cache clusters; is that right?
A Yes.
Q And one option for the on-die interconnect 320 is a ring interconnect; is that right?

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A Correct.
Q Another option for the on-die interconnect is a mesh interconnect; is that correct?
A Correct.
Q If you look a little bit further down the page in paragraph 34, there's a discussion of a scalability agent. Do you see that?
A Yes.
Q I believe Sistla indicates that the scalability agent can be distributed so that individual scalability agent units uniquely correspond to the core-cash clusters; is that right?
A That's what it says. Yes.
Q So would I be correct in understanding that the scalability agent is divided up or partitioned in some way so that the individual SA units are somehow associated with the core-cache clusters?
A It says here "uniquely correspond to core-cache clusters 3101 through 3104." So it's a correspo- -- it's talking about a correspondence.
Q Do you read that as sort of a one-to-one correspondence or is it one-to-many?
A My -- you know, just from reading the sentence, it says "uniquely correspond to core-cache clusters." So I would understand that as a one-to-one just from the

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sentence. But, again, I would have to refresh my memory by looking at the details of the embodiment and the description to see if that's really what they intended to say.

Q If you'd like, you know, take a minute or two, whatever time you need, to confirm your understanding of this passage.

A So just so I'm clear, you want me to confirm that it's a one-to-one correspondence --

Q I don't --

A Between?

Q Whether it's one-to-one or one-to-many, yeah.

A Okay. I will take a look.

Sorry. What was the paragraph number we were looking at?

Q We were looking at paragraph 34. And it makes reference to figure 4, if that helps.

A Yeah.

So figure 4 shows a one-to-one correspondence between a core-cache cluster 310 and an SA agent -- scalability agent unit 350. So the 1 corresponds to 1; the 4 corresponds to the 4. As far as how these things operate, there's -- if you go to paragraph 30, for example, it does talk about the plurality of core-cache clusters in communication with each other over the on-die

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interconnect.

So all I can say from -- about the one-to-one correspondence, the indic- -- is what I see in figure 4 where there's one core cluster and the corresponding scale of any -- scalability agent matching with each other.

Q Okay. Thank you. Let's turn to your declaration, please. This is Exhibit 1003.

Do you have that document?

A I do.

Q You -- I think you indicated that you had a chance to review your declaration during the preparation for the deposition; is that right?

A That is correct.

Q Would you turn to paragraph 51, please, on page 26?

A Okay.

Q In paragraph 51, you're offering an opinion concerning a person of ordinary skill in the art; is that right?

A Correct.

Q Did you consult any sources in arriving at this opinion about who that person of ordinary skill in the art would be?

A I'm sorry. I don't mean -- I don't know what you mean by consult sources.

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Q How did you arrive at this opinion?
A Based on reading the '228 patent and my 30-plus years of experience in academia and industry to understand, you know, the subject matter and putting myself back at that time understanding what a POSITA would be. So that's how I arrived at it.
Q Okay. "At that time," you mean December 2011; is that right?
A The time of the patent, yes.
Q In paragraph 51, you say that the person of ordinary skill in the art "would have held at least a bachelor's degree in electrical engineering, computer engineering, physics, or a similar field, with a focus on semiconductor technology and/or microelectronics"; correct?
A Correct.
Q In this context, what do you mean by "semiconductor technology"?
A For example, many of -- universities, institutions at that time had different paths -- for example, an electrical engineer can choose different concentrations. And some of them, at the time, were called the VLSI, for example, which stands for very large scale integration or an LSI, large scale integration. So there was -- that acronym was used. So that's really what

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I'm referring to.

And semiconductor technology, other institutions have a general -- more general areas of specialization even on the undergrad, which is microelectronics, which, again, would cover circuit design techniques.

Q Why would the person of ordinary skill in the art had to have done an undergraduate program with a focus on semiconductor technology or microelectronics?

A There's descriptions of the -- in the '228 related to building the systems. And it talks about processors and building the processors, so you need to understand the basics of that.

Q What do you mean by "the basics"?

A We're talking about processors and chips. And, therefore, those are the areas where that usually is covered is under microelectronics in undergraduate.

Q So what sort of aspects would the person of ordinary skill in the art have to have studied in order to be a person of ordinary skill in the art?

A All the components of electrical engineering or computer engineering. The way it works is they all -- all these courses build upon each other. Usually start the freshman basic courses and then we build upon it until we get a person to a point in time where they understand the general concepts of designing a circuit, designing a chip,

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or designing a processor, for example. So that's usually what one would have to understand.

And then on top of that, my opinion is you need two years of industry experience in the field of computer architecture design. Because at that point, the '228 is talking about caches and cache architecture and processor architecture. So that's where the additional specialization is needed for a person of ordinary skill in the art to understand this.

Q So there -- any particular classes that the person of ordinary skill in the art would have had to have taken as part of their undergraduate education?

A Of course. I mean, like I say, you start from the freshman level all the way to the senior level. From my recollection, for example, you would have to take several -- one or more microelectronics classes, one or more circuit classes, as part of the process, and one or more computer architecture classes during that process.

But it really depends on the various institutions as to how they cater their various subjects. And that's why the two years of industry or academic experience, in particular, computer architecture inval- -- and development in order to understand the processors and the cache architectures that the '228 is talking about.

Q So during this two-year period of industry or

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academic experience, what would the person of ordinary skill in the art had been doing?

A Well, they can be doing many things, including research, circuit design, processor design, system design, or even other -- you know, servers, any system -- designing any of the systems. So it could be any of that.

The key is that they're dealing with computer architecture design and development. They need to understand caches. They need to understand cache coherency. They need to understand processors, and they need to understand how those systems interact with each other. So that's what's required from a person of ordinary skill in the art at the time in order for them to read the '228 patent and understand it.

Q In the next couple of paragraphs, paragraphs 52 and 53, you're discussing claim construction; correct?

A Yes.

Q And you indicate that -- in paragraph 53 that "no specific claim term needs to be completely defined for purposes of" your analysis; is that right?

A Yes.

Q What do you mean by "completely defined"?

A So the plain and ordinary meaning is sufficient for a person of ordinary skill in the art to understand the terms of the '228 patents -- patent.

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Q Isn't the plain and ordinary meaning of a term the definition of that term?
A Yes. If I understood your question correctly.
Q Well, I am trying to determine what you mean by "completely defined." Is there something different in your mind between a complete definition of a term and the plain and ordinary meaning of that term?
A Not really, no. It's plain and ordinary meaning of the term.
Q Okay. So am I correct that in paragraph 53, what you're saying is your analysis uses the plain and ordinary meaning of the terms in the claim of the '228 patent; is that right?
A Yes. The plain and ordinary meaning in light of the specification. Absolutely, yes.
Q Okay. Let's turn to the '228 patent. This is Exhibit 1001. And I'll ask you to turn to the claims, which start in column 7.
A Okay.
Q Now, you obviously analyzed the claims of the '228 patent as part of your work in connection with the preparation of your declaration; correct?
A Yes.
Q Are there any terms in these claims that are explicitly defined in the patent?

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A Not sure I follow the question. But I'll give you my understanding of the claim. Every word in this claim gets its meaning from the claim itself and then from the specification. So not sure what you mean by which ones are and which ones are not.

One --

Q Let me see if I can -- I'm sorry.

A No. I was just going to say one of ordinary skill in the art, you know, would look at each one of these terms and try to understand them in light of the specification.

Q Let's take an example. So let's look at Claim 1. And Claim 1 uses the term "caching agent."

Do you see that?

A Yes.

Q Does the term "caching agent" have an ordinary and customary meaning in the art?

A The term is used interchangeably with many other terms that refer to the functions that are described in the '228 patent. But reading the '228 patent, one would understand what a caching agent would at least encompass in light of this specification.

Q What would that understanding be?

A I will go to the patent and show you where I would get that understanding. Just a warning, there's a

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lot of material on what a caching agent do in the '228 patent. And all of it does explain what caching agents -- at least a caching agent would at least do in light of the '228 patent. But I'm happy to do that.

Q Please, if you would.

A Do you want me to read them off as I find them or do you want me to wait until the end and list them all together? 'Cause like I say, it's going to be quite a few places.

Q What -- why don't you give us the list as you find them. And then if we need to, we can go back and talk about them.

A Okay. So I start with the abstract where it talks about a "caching agent to perform cache coherency operations for the plurality of cores and the" II- -- "IIO module." So that's one.

So another example is column 1, line 21, where it talks about "caching agent, meaning that dedicated logic is associated with the I/O component to handle cache coherency operations."

And it talks further about an explanation of how to maintain cache coherency. Line 36 -- or 37 to 38, it's talking about figure 2, and it talks -- it shows the "caching agent in accordance with the embodiment of the present invention."

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Another example is lines 56 and 57. It talks about a "caching agent that can be configured to support both CPU traffic and I/O traffic as well.

So again, for example, in paragraph -- in column 2, line 18, there's a discussion "in various embodiments, this caching agent may be a combined caching agent, both for the CPU as well as for the integrated I/O agent."

So then you have a description of figure 2 starting on column 2, line 36, all the way to at least column 3, line 3, where it's explaining the details of figure 2 and the components of an embodiment of a caching agent. And I highlighted it in case we go back to it.

So there's another explanation of what a caching agent does in column 4, approximately line 16, and probably all the way to line 31. Again, it's explaining the functionality of a caching agent.

So another explanation of what some of the functionality of a caching agent is column 5, line 50 through -- all the way to line 60? There's also explanation on column 5, line 61. There's more examples of embodiments. So from line 61 through line -- probably 6 -- column 6, line 14.

So another example is line -- column 6, line 25 through 29, where it's talking about caching agent

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"configured to handle cache coherency operations."

And you can see in some of the claims -- for example, Claim 6 explains some of what a caching agent may do for -- in the process of performing cache coherency. Claim 8 is another example of what a caching agent can do.

So that's generally what a person of ordinary skill in the art would read all these and understand the caching agent being -- performing operations to perform cache coherency.

Q So if I understood your last statement, the person of ordinary skill in the art would understand the various passages that you provided us as defining what the caching agent is and what it does; is that right?

A No. There's specific embodiments of what a caching agent can do, and one of ordinary skill in the art would understand it's performing cache coherency operations.

Q Okay. So one of the things a caching agent does is cache coherency operations; is that right?

A Well, that definitely is one of the things that would do, yes. And how it does it is -- there's various examples of that.

Q But if the person of ordinary skill in the art wanted to understand what the caching agent is, would they look to the passages that you've described for us?

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A They would look at the passages I describe in order to understand the embodiments for this particular application. But the -- they understand from the description that the caching agent is -- encompasses that, but encompasses caching agents that perform cache coherency operations. And in this particular application, it's for multicore processors and I/O, IIO modules.

Q Okay. So I'll go back to the question I originally posed, and that is: For the term "caching agent" as it is used in Claim 1, is there an ordinary and customary meaning of that term in the art?

A Well, again, in light of everything I -- we went through in the '228 patent, it's the performance of cache coherency.

Q So are you saying that anything that performs cache coherency is a caching agent as that term is used in Claim 1?

A You're going to have to show me what the "anything" is. I mean, I can look at the -- what you're referring to and I can evaluate it at that time. But, you know, for example, that's what I did with the prior art references, and I determined that those were caching agents as recited in the claims of the '228 patent.

Q I see. So you looked at an example for -- of something described in the prior art reference and decided

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whether or not that was a caching agent as recited in the claims of the '228 patent; is that right?

A Yes. I compared the reference and the operations it was doing with the operations described in the '228, and they were similar. And, therefore, they are the claimed caching agent.

Q Is the term "caching agent" used consistently in the claims of the '228 patent, meaning is it used the same way in each of the claims?

A Well, I mean, the -- some of the dependent claims, you know, add more functionality, you know, had elements to what a caching agent would do. So to that extent, it's broader in some claims than it is in others.

Q So the term "caching agent" means different things in different claims? Is that what you're saying?

A No. That's not what I said. I said the caching agent is broader in some claims than it is in another claim.

Q Can you give me an example of what you mean?

A Sure. So, for example, Claim 6 says, "The apparatus of Claim 1, wherein the caching agent is to receive an allocation transaction from the IIO module, the allocation transaction received in the IIO module from an I/O device coupled to the multicore processor."

So the caching agent in Claim 1 doesn't

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necessarily receive that -- this allocation transaction, but the caching agent in 6 does. So that's what I mean by the caching agents in Claim 1 is a broader definition of caching agent than Claim 6.

Q So using that understanding, the caching agent recited in Claim 1 is somehow different than the caching agent recited in Claim 6; is that right?

A No. It may or may not. The inclusion of the feature in Claim 6 in the caching agent doesn't make the caching agent in Claim 1 different. It might or might not be included, but that doesn't preclude it from being the caching agent of Claim 1, whether it was included or not.

Q All right. But I'm just looking at the term "caching agent." Is the thing that is a caching agent in Claim 1 different than the thing that is a caching agent in Claim 6?

A So Claim 6 depends from Claim 1 and, therefore, in -- for the caching agent in Claim 6 must include everything the caching agent does in Claim 1, plus the additional functionality that is recited in Claim 6.

Q So if I understand you correctly then, the term "caching agent" has a different meaning in the different claims depending on the limitations of the particular claim; is that right?

A No. I cannot explain it any better than I

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already explained it. So the answer is "no" to your last question.

Q Okay. But in the context of your analysis as set forth in your declaration, you did, as you told me, looked at the prior art and decided whether or not the prior art reference performed the function in order to decide whether it was the caching agent recited in the claim; is that right?

A I compared the functionality that the caching agent was performing in the prior art and the caching agent that is perform -- that was performed in the '228. And I did conclude the prior art caching agent is the claimed caching agent of the '228 claims.

Q Okay. Also in Claim 1, there's the phrase "cache coherency operations."

Do you see that?

A Yes.

Q Does the term "cache coherency operations" have an ordinary and customary meaning in the art?

A It does. And it encompasses, again, a wide number of functions that can be done in order to do cache coherency. And it depends on the system and the architecture as to how that cache coherency is done.

Q Okay. Can you tell me what the term "cache coherency operations" means in the art?

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A Again, let me go to the patent and see if I can give you the answer from the patent.

So the patent uses cache coherency and gives examples of how the -- it's the same -- a lot of the same passages I referred to you before, performing the functions of cache coherency. And the idea is that cache coherency is to make sure the integrity of the data that's being write -- written across different memories is intact, transmitted correctly. So...

Q Just to be clear, that's how the term is used in the '228 patent, the term being "cache coherency operations"?

A Yes. It's a term that's well known in the art. And the examples that the '228 patent give of how it's performing that confirms that.

Q So is the way the term "cache coherency operations" used in the '228 patent the same as the way that term is used in the art generally?

A Yes, it is.

Q And is the term "cache coherency operations" used consistently in each of the claims of the '228 patent?

A I believe the answer is yes. I haven't noted any discrepancy. But again, I would need to look at the particular claim still whether some of the independent claims narrow or add functionality to a broader recitation

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of cache coherency.

Q If you look at Claim 11, Claim 11 uses the phrase "allocation transaction."

Do you see that?

A Yes.

Q Does the phrase "allocation transaction" have an ordinary and customary meaning in the art?

A The -- it depends. It's a very general term of an allocation transaction. So it's a pretty broad term. But if it -- at least from the '228 patent, at least a read and write would be an allocation transaction. So those would be encompassed in an allocation transaction. But I can go look more specifically in the patent to answer you, you know, more accurately, if you'd like.

Q Is that your understanding of how allocation transaction is used in the '228 patent? It would be at least a read or a write?

A Yes. To at least that.

Q And Claim 11 requires that the integrated input/output module receive an allocation transaction from an I/O device; correct?

A Correct.

Q Claim 11 also requires that the caching agent receive the allocation transaction from the integrated input/output module; is that right?

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A Read that again slowly --
Q Sure.
A -- please.
Q Does Claim 11 require that the caching agent receive the allocation transaction from the integrated input/output modules?
A Technically, it says the method is "forwarding the allocation transaction to a caching agent of the multicore processor." And then the method requires "directly storing the data of the allocation transaction into the shared cache memory of the multicore processor."
So I would say yes. The forwarding -- that there is a receiving by the caching agent there.
Q I used the phrase "integrated input/output module," which appears in Claim 11. Does that term have an ordinary and customary meaning in the art?
A Well, yes. I mean, that -- the I/O is a very common term used, "input output," and it encompasses a plethora of different modules that can do it. And one of ordinary skill in the art would understand "integrated" to be on an integrated circuit. So I would say yes. IIO -- not sure I've seen "IIO," but integrated I/O is a common term -- would be a common term.
Q Let me go back for a moment to Claim 3. Sorry. I missed this one. Claim 3 uses the term "posted

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transaction."

Do you see that?

A Yes.

Q Does that term "posted transaction" have an ordinary and customary meaning in the art?

A So the answer is yes, but give me one second to complete my answer. I just want to look at the patent for a second here.

Yes. So if you look at claim -- sorry, column 5, line 3 to line 6, generally a posted transaction is a transaction which when sent by a source is considered complete by the source and the source does not receive a completion or other confirmation message regarding the transaction. So that is a general description of a posted transaction.

Q If we take a look at Claim 13, Claim 13 uses --

A 13, did you say?

Q 13. Yes. 1-3.

Claim 13 uses the term "evicted."

Do you see that?

A Yes.

Q Does the term "evicted" have an ordinary and customary meaning in the art?

A Again, my answer is yes when you're talking about caches. But let me look at the patent and see if it

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provides anything different or the same.

It's -- generally can be understood from column 4, lines -- about 5 to 12, and it is what my understanding would be of eviction in a cache system.

Q So the passage you just mentioned indicates that it is only "upon an eviction from the cache that the data is written to system memory"; right?

A Right.

Q So that seems to indicate that "eviction" is some type of removal of information from the cache; is that correct?

A That is correct. And it is describing figure 3, and there are at least a couple ways to handle eviction in a cache. And this happens to be one way to handle it. What you described as removal from the cache and the result is -- in this case in figure 3 is to save it, sending the data to memory.

Q If we -- we look at Claim 2, there's reference to a "table of requests."

Do you see that?

A Yes.

Q And then in column 2, beginning at about line 44 and continuing to about the end of that paragraph or so, there's a description that indicates "the table of requests may be a buffer or other temporary storage for

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holding incoming requests."

Do you see that?

A I do.

Q Is that how the term "table of requests" is used in Claim 2?

A That is my understanding. Yes.

Q And if we look at Claim 7, Claim 7 requires that the caching agent "directly store data of an [sic] allocation transaction into the shared" me- -- a shared "cache memory and not initiate a memory transaction to a system memory."

Do you see that?

A Yes.

Q And column 4 -- really the passage that you just pointed out to me beginning at about line 8, the specification explains that data can be loaded "from an I/O device directly into a processor cache, without the need for consuming any memory bandwidth."

Do you see that?

A I'm sorry. No. Am I on col- -- which column?

Q Column number 4.

A Yes.

Q Beginning maybe in line 8, "using method 300."

A Okay.

Q We're told that the method can "efficiently load

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data from an I/O device directly into a processor cache, without the need for consuming any memory bandwidth."

Do you see that?

A Yes.

Q Is that how a person of ordinary skill in the art would understand what's being recited in Claim 7?

A Yes. It's a write -- it's a write-back operation. I don't recall if the patent uses write-back operation or not. But that's what this is describing where you don't save to memory until, for example, a -- you can go straight from the I/O device to the cache and not write to memory until later on, if you need to.

Q Dr. Hassoun, we've been going for a while, and it's a little bit after 12:00. Would you like to break for lunch or just pause for a bit to get a glass of water or whatever?

A Yeah.

THE WITNESS: Can't hear you, Kevin.

MR. ANDERSON: I was just going to suggest we go off the record if we want to talk about the break.

MR. FAHMI: Sure. Yeah. Let's go off the record.

THE STENOGRAPHER: Off the record at 12:11 p.m.

(Off the record.)

THE STENOGRAPHER: Back on the record at

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12:26 p.m.

MR. FAHMI: Thank you.

BY MR. FAHMI:

Q Dr. Hassoun, during our break, did you discuss the substance of your testimony today with anyone?

A (Inaudible response.)

THE STENOGRAPHER: I didn't --

BY MR. FAHMI:

Q I'm sorry. We're not hearing you, Dr. Hassoun.

A I did not.

Q Thank --

A Is that coming in?

Q Yes.

A Yeah. Sorry.

Q Thanks.

A All right.

Q Let's turn to the Agarwal reference. This is Exhibit 1005, please. Do you have a copy --

A Okay.

Q -- of Agarwal?

A I do.

Q Great. And this is one of the references that you discussed in your declaration; correct?

A Correct.

Q I'm going to ask you, please, to turn to column

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16 and the discussion of "Proxy Cache Coherence" that begins at about line 25.

A Yes.

Q In this section, beginning at about line 35 or so, Agarwal uses the term "home tile."

Do you see that?

A Yes.

Q What would a person of the ordinary skill in the art understand Agarwal means by a "home tile"?

A So Agarwal continuously, in this section, talks about how a home tile is used. On line 36 of column 16 -- so it says a home tile "for a given portion of the main memory." So a portion of a main memory will have a so -- will be assigned to a particular tile.

And then there's explanation on what that means and how that works, I believe, column 19, lines 47 all the way to line -- column 20, line 25. There's an explanation of the -- what that means. I apologize. Also line -- column 19, line 4 through line 29. Well, for that matter of fact, actually the entire column. So line 19 -- let me answer the question again.

Also, the explanation -- the understanding of what a home tile means can be found line 9 -- column 19, line 4 all the way to column 20, line 25. There's an explanation of how that's used.

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Q I guess maybe we should back up a bit. What does Agarwal mean by "a tile"?

A So Agarwal references a tile with respect to figure 4, figure 5, and then has examples of what a tile looks like internally in figure 6A and figure 6B. So a lot of the description is in the passages I mentioned to you earlier. But I can look for more explanation of what a tile is for Agarwal, if you'd like.

Q If we go back to column 16 in the paragraph that begins at about line 35 or so, we're told that at least for tiles that are used as home tiles, those tiles would include a processor and a cache; correct?

A Yes.

Q And the home tile also includes a directory controller and directory storage; is that right?

A Correct.

Q What is the function of the directory controller?

A So the directory controller in combination with the directory, they perform cache coherency operations as detailed in these columns.

Q And is it correct that the directory controller of a home tile manages coherency for that home tile's assigned memory locations?

A One more time.

Q Is it correct that a home tile's directory

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controller manages coherency operations for that tile's assigned memory locations?

A That's part of what it does. So yes. But it also does it for all the other tiles that are trying to access that memory location.

Q So if I understand correctly, if a given processor core wants to access a particular memory address, it sends a request to the home tile that is associated with the directory controller responsible for that memory address; is that right?

A Well, it can do that, yes. If we look at figure 6A, for example, and the description of figure A, the sequence of operations are shown in the figure with reference to operations B1, B2, B3, -4, all the way through -- I think it describes it yet all the way through B7. So there's a sequence of operations that happen. But -- so it's -- what you described is part of what happens.

Q Okay. So let's walk through what figure 6A is showing, just so that we're not missing anything. What's shown by operation B1?

A Okay. So I'm going to open the text that refers to that so I can --

Q Sure.

A -- be as accurate as possible. Is that okay?

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Q Yeah, of course. Please.

A Yeah. Okay. So I'm going to do it from my declaration.

So I will refer to -- it's Agarwal 19:3-2025, but the paragraph I'll be looking at -- so I can put these side to side -- is paragraph 72 of my declaration.

Q Okay. Thank you.

A And... so the first question -- I think the question you asked me is "what does B1 mean"?

So B1 is an operation in tile 2. So in tile 2, when a processor 600 attempts to read data at an address from its cache 602 -- so 600 is attempting to read data at a particular address from 602. So in this case, if it finds it there, then it's good to go. If it doesn't find it there -- and the text -- the explanation says, "After a cache miss on tile 2," the miss -- "the miss goes through a message through the network to the home tile, tile 1, Action B2." So that takes me to tile 60- -- sorry, block 602 on tile 1.

Q Okay. And then we see in figure 6A, there's a process or an arrow labeled "B3." What is B3 showing?

A Okay. So for B3 -- let me find the text for it.

So for B3, if they -- if there's a cache miss on B3 that -- I'm sorry, on B2, then there's an access from B3 to the main memory.

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Q And, again, referring back to figure 6A, what is the step B4 showing?

A So B4 shows an example -- the data coming back from the main memory to block 602.

Q And referring to figure 6A, what is B5 showing?

A So B5 is an update of the directory storage with tile 2's address. So it's going to update the address in 602 -- in the directory storage 604, sorry. So that's what B5 is.

Q Again, referring to figure 6A, what is B6 showing?

A So B6 then sends the data value to tile -- back to tile 2, which originally requested it.

Q And then finally referring to 6A, what is B7 showing?

A And then the cache 602 sends the value to the processor 600. So it will send it back to the processor that originally requested the data.

Q So -- thank you for that description.

And based on that description, would you agree that in Agarwal, for any given memory address, there's one tile whose directory controller is responsible for coherence with respect to that memory address?

A So -- but it's all -- it is responsible for that. In addition, it's responsible for the coherence and the

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other caches, for example, in 602 of tile 2. So both 603 -- the controller in 603 and -- sorry, tile 2 and tile 1 come -- collectively have the responsibility for the coherence of the data. The memory 602 in tile 1 and 602 in tile 2.

Q Well, the controller 603 in tile 1 doesn't consult the controller 603 in tile 2 with respect to a memory address that the controller in tile 1 is responsible for, does it?

A So the disclosure doesn't specifically say it consults 603 of tile 1. But the process described, which is the data being -- you know, the cache miss from -- as a result of B1 comes from -- is controlled by the directory controller. And then the data being sent back from 602 of tile 1 back to 602 of tile 2 would be under the direction of the directory controller 603.

So they are working in unison in order to ensure, again, the cache coherency between 602 in tile 2, 602 in tile 1, and, in this case, the main memory.

Q Okay. I think we need to be clear about which controller we're talking about. Because in figure 6A of Agarwal, there are multiple 603, multiple 602, multiple 604, et cetera. So let's see if we can better distinguish those units from one another.

Figure 6A is showing a situation where tile 1 is

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the home tile for the data at the requested memory address. Would you agree?

A Yes.

Q And figure 6A is showing a situation where the directory controller 603 of tile 1 is responsible for the coherency with respect to that memory address. Would you agree?

A It's -- I agree that's part of what it is responsible for. Yes. But as I said before, both of 'em are involved, in the example we said, in the cache coherency between 602 of tile 2, 602 of tile 1, and the memory. Cache coherency is not just to memory. Cache coherency is the integrity of the data in the cache sis -- in the memory system which includes the caches.

Q Okay. Maybe I misunderstood what you were saying earlier. If I understood what you just said, the controller 603 of tile 1 is responsible for coherency concerning the data that's stored in the cache 602 of tile 2 because it's -- that data is associated with a memory address that falls under the responsibility of controller 603 of tile 1. Did I get that right?

A I think so. Yes. It's -- that's the process, yes.

Q And directory controllers of different home tiles don't share coherency responsibility for a single memory

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address; is that right?

A Okay. Ask me the question again.

Q Sure. I'll see if I can break it down a bit.

If we're talking about one given memory address, Agarwal doesn't describe a situation where the coherency responsibility for that given memory address is shared by directory controllers of two different home tiles; is that right?

A No. Because I'll go back to my previous answer for the previous example. The directory controller from 603 -- sorry, from tile 1 and the directory controller from tile 2 are involved in the process of ensuring the cache coherency between 602 in tile 2, 602 in tile 1, and the memory.

Q Okay. Can you show me in Agarwal where that's explained?

A Absolutely.

So I will point you to two places. First is the function of a directory controller in a tile. So if we go to column 2, approximately line 47... so line 47 states, "A coherence controller or the directory controller attached to that memory would check that directory entry stored along with the memory location in the directory state and would determine the action to take based on the request and current state of that memory location."

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Okay. So the coherence controller, it is the one that is going to make any determination on what to do with a request going into the cache 602. So the involvement of the coherence controller for local tile 2 is part of this process that is described here. That is the job of the coherence controller.

So from the beginning, the coherence controller of tile 2, even though it's not its home tile -- the address is not its home tile, that determination happens by the coherence controller. So that's the function the coherence controller. And then the data is sent to tile 2 -- or the request is sent to tile 2 where the directory controller there performs the other operations that we've discussed.

So the responsibility for that coherence falls under both of the -- both of the controllers because it's the controller in tile 2 at least. Because it has to -- the one to determine that there was a cache missed there, and, therefore, it has to make the request go to tile number 1.

Q Okay. So that passage you just pointed me to, column 2, beginning at line 47, that appears in the background section; right?

A Yes. But it's explaining what a cache -- a coherence controller does.

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Q And you know that the background section of a patent is describing what was done previously before the invention of the patent; correct?

A I understand.

Q In fact, the background section is usually used to describe problems with the prior art; right?

A Yes. But it's describing the function of the directory controller. And there's more, though, description that's not only in the background section of what the directory controller does. I was using that as an illustration. There's more. The directory controller of that tile is the one responsible for figuring out whether there's a hit or a miss.

I --

Q In fact --

A -- can go through more examples, if you'd like.

Q Well, I'd like to finish with this one first.

So this passage is actually referring to a coherence controller that was used in the so-called "alewife machine"; is that right?

A Yes. I believe that's correct. Let me check, please. Yeah.

Q Did you work on or with the alewife machine in connection with your appointment at MIT?

A I did not.

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Q So the passage that you referred to at line 47 is discussing coherence controller or a directory controller attached to the memory; right?

A Yes.

Q And we looked at figure 6A of Agarwal, and we established that tile 1 is the home tile for the memory address that is being requested; right?

A Correct.

Q So it's the directory controller of tile 1, if anything, that that passage in column 2 would be referring to. Wouldn't you agree?

A Mm, yes. I was showing generally what a coherence controller does. But I was going to walk you through more evidence of what a cache controller does.

Q Okay. But the specific issue we're concerned with is the question of whether it is the cache controller of the home tile alone that is responsible for the coherency operation associated with a memory address associated with that home tile?

A And my answer is that's not entirely encompassing of what the process is. Cache coherency, in the example we talked about, has to include the data in 602 in tile 2, 602 in tile 1, and the main memory. So the reason a request was sent from tile 2 to tile 1 is 'cause there was a cache miss in tile 2. And the cache miss in tile 2 is

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controlled by the directory controller. That's the job of the directory controller.

And the description I pointed you just shows generally the checking that the cache controller does. So if it's sitting in tile 2, then it's going to do that check, whether there's a miss or a hit. And that's where the responsibility collectively or coherence across the system is with all the cache controllers, the distributed portions of the directory controllers.

Q Okay. So other than the passage that you've already referenced in column 2, is there anything else in Agarwal that describes cache controller 603 in tile 2 on figure 6A as being responsible for the coherency operation associated with the requested memory address for which tile 1 is the home tile?

A So the answer is yes. There's more. And the description in columns 19 and 20 that I read from where we discussed, you know, B1 and then B2, which B2 happens when there's a miss, is controlled by the directory controller that belongs to that tile. It's not the directory controller of the home tile in tile 2 that decides there -- there's a miss. It's the directory controller in tile 2 that makes that determination. So collectively, these controllers ensure the cache coherency in the system.

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Q Okay. So forgive me, but that seems to be contrary to what Agarwal itself says in column 19. I'm looking at the passage that begins at column 8 -- excuse me, line 8 of column 19 where it says "cache 602 may be serving as an L2 cache after a miss in an L1 cache within the processor 600. After a cache miss, e.g. for a shared data read on tile 2" --

A I'm sorry. I missed the beginning where you started. Can you just start again, please?

Q Sure.

A Slowly, please. Sorry.

Q We can look right at the beginning of the paragraph that begins in line 7 of column 19. And it's discussing tile 2 and a processor attempting to read data at an address from its cache 602. And as you previously explained, that's what's shown as action B1. Are you with me?

A Yes.

Q Okay. So it says, "The cache 602 might be serving as an L2 cache after a miss in an L1 cache within the processor"; right?

A Mm-hmm.

Q And it says, "After the miss on tile 2, the miss goes as a message through the network to the home tile, tile number 1," and that's action B22.

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Do you see that?
A Yes.
Q Okay. So there's no indication that controller 603 in tile number 2 was involved in that process, is there?
A I disagree. It absolutely is.
Q Where --
A If you look --
Q -- does Agarwal say that?
A So the function of the directory controller, as described in many places in Agarwal, is to check for that miss. And I'll give you the examples of where it checks for misses. So I'll start with that second sentence from -- starting at line 10. Okay? It says, "After a cache miss" -- okay? -- "that determination for misses is done by the directory controller." Okay?
So, for example, if you look down... let's look at that -- so that's at least the first involvement of the directory controller of tile 2 in the process. And all these messages that you see going back, it talks -- the paragraph is talking about the messages, that's the responsibility of the directory controller.
Q I don't want to interrupt, but I'm not sure if you're finished with your answer.
A I am. I was going to give you more evidence of

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what the directory controller does. But that is my answer. That's where the involvement -- at least that's where the involvement of the directory controller of 6 -- of tile 2.

Q So you read Agarwal as somehow saying that the coherency responsibility for a given memory address is a shared responsibility amongst different directory controllers of different tiles; is that right?

A Or the coherency in the entire system, the answer is yes. As I explain, coherency includes the memory and the copies of the data and the various caches.

Q Let's look at column 29, please.

A Column -- which column, please?

Q 29.

A 29?

Q Yes.

A Okay.

Q In column 29, Agarwal is describing a situation where an I/O module wants to access memory, and he's referring to it as a "ProxyIO coherence protocol."

Do you see that?

A I see column 29. Where am I starting?

Q I think the discussion begins in the paragraph that starts around line 5.

A Okay.

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Q So --
A Yes.
Q -- as I understand it, in this situation when an I/O module wants to access a particular memory location, it sends the request to the directory controller that is associated with the home tile of that address; is that right?
A Yes. That is the process for the -- this mode to -- where the, for example, a write from I/O module 912 will go to the home tile for process.
Q Then the directory controller for that home tile handles the I/O request the same way it would handle a request from a processor's core similar to the fashion we discussed with respect to figure 6A; is that right?
A That is correct.
Q Let's turn back to column number 27, please.
A Column what? Sorry.
Q 27.
A 27. Yes.
Q In the paragraph that begins at about line 20 in column 27, Agarwal says, "The tile can also keep a small buffer that contains a list of outstanding transactions along with an acknowledgement counter associated with each."
Do you see that?

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A I do.

Q These buffers are maintained per tile; is that correct?

A I don't see that it says one way or the other.

Q Would it be a buffer for just the directory controller associated with that tile or for all of the directory controllers or do -- is it unclear?

A So this thing starts with saying "the coherence" on line 11 of column 27. Starts by talking about "The coherent scheme can be modified further by using the cache state that is used to store directory state for multiple purposes."

And continuing, it says, "The tile keeps track of the number of acknowledgment [sic] that have been returned from other tiles. This can be stored as a counter in the same set of bits that are used to store directory information. Each time an acknowledgment comes back, the counter is incremented or decremented."

And then it says that "the tile can also keep a small buffer that contains a list of outstanding transaction [sic] along with an acknowledgment counter associated with it [sic]. This information can also be stored in one of the memory storage locations normally used for cache and memory access, such as a memory retry FIFO."

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So it's not -- I would say it's more it's not 100 percent clear that a control is restricted to the tile.

Q So the fact that the passage says the tile can keep the buffer, you don't read that as indicating each tile keeps a similar buffer?

A Well... I mean, this starts with saying this is an extension of the scheme, the coherent scheme. I mean, it's talking about outstanding transactions, whether it's transactions to the tile itself or other tiles -- you know, from other tiles. I would say it's not 100 percent clear.

Q Okay. If we look in the next column, column 28, there's a section 5.1 that begins about line 10 for "I/O Coherence Examples."

Do you see that?

A Yes.

Q In that first paragraph under section 5.1, there's a discussion of an I/O module, and there's reference to "direct memory access" or "DMA transactions initiated from a tile."

Do you see that?

A Yes.

Q What would the person of ordinary skill in the art understand is meant by a "DMA transaction"?

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A So it depends on the context. I believe in this section, this is referring to the I/O module where the data is stored directly into memory or into ca- -- excuse me -- into the cache rather than directly to the memory. So, generally, a DMA is doing -- is storing data directly to a memory without involving the processor. And the memory could be a main memory; it could be a cache.

And in this example, they're using it -- there -- what it -- what this is describing, starting on line 23, it says, "An I/O module is also able to process a DMA transaction or otherwise store data directly into the cache" for a given -- "of a given tile."

So it's sending it straight there, but that falls under the definition of a DMA.

Q And in this description, what unit or item is initiating that DMA transaction?

A So line 2, 3 -- line 4 -- so it's saying, "enable the module 912 to process direct memory access (DMA) transactions initiated from a tile."

So it's a tile that initiates that transaction.

Q Would that be the processor of the tile?

A It doesn't say whether it's the processor or the controller. There's a controller in there, so it's not clear which one is initiating the DMA.

Q We've been going for about an hour. Do you need

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to take a break?
A Sure. I'll take a ten-minute break.
Q Sure. How long would you like? Ten minutes maybe?
A Ten sounds good.
MR. FAHMI: Okay. Let's go off the record.
THE STENOGRAPHER: Off the record at 1:25 p.m.
(Off the record.)
THE STENOGRAPHER: Back on the record at 1:40 p.m.
MR. FAHMI: Thank you.
BY MR. FAHMI:
Q Dr. Hassoun, can you please pull up your copy of the Sinharoy reference, please. It's Exhibit 1006.
A Yes.
Q You offered testimony concerning Sinharoy as part of your declaration; is that right?
A Yes.
Q Sinharoy is describing the IBM POWER7 processor; is that correct?
A Yes.
Q And that's a multicore processor; is that right?
A Yes.
Q And in addition to the multiple cores, the POWER7 processor has a multilevel cache hierarchy; is that

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correct?

A It does.

Q If you turn to page 16, please.

A Okay.

Q At the bottom of the left-hand column, the discussion regarding the "cache hierarchy" begins. And I believe Sinharoy indicates that each one of the cores has an L1 cache; correct?

A Yes.

Q Each one of the cores also has an L2 cache; is that right?

A Yes.

Q And there's also an L3 cache that's described as being made up of individual local L3 regions; is that right?

A Yes, amongst controllers -- amongst other things. But yes, generally, that's correct.

Q We take a look at page 18, please.

A Yes.

Q In the left-hand column, there's a more detailed discussion of the L2 cache that begins, and we're told in the second sentence under the "L2 cache" heading that it's "comprised of a single centralized controller with two address-hashed data arrays."

Do you see that?

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A Yes.
Q Is it your understanding that each core's individual L2 cache has a single centralized controller or is it one single centralized controller for all the L2 caches of all the cores?
A My understanding is each one of the L2 caches have their own -- has a centralized -- have a controller. That's my understanding.
Q If you turn to page 19, please.
A I'm there.
Q In the left-hand column, there's a heading for the "L3 cache," and the description of the L3 cache follows. Do you see that?
A Yes.
Q We're told that the L3 cache is a shared 32-megabyte cache composed of eight 4-megabyte regions. Do you see that?
A Yes.
Q And then a couple sentences later, "A given L3 region comprises a single centralized controller, with four address-hashed eDRAM cache data banks and four address-hashed SRAM directory banks."
Do you see that?
A Yes.
Q So, again, is it your understanding that each

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4-megabyte L3 region has its own cache controller or is there one cache controller for the entire 32-megabyte L3 cache?

A There -- each L3 region has a single centralized controller.

Q If you look over in the right-hand column, the second full paragraph in the right-hand column that begins "the centralized L3 region controller."

Do you see that?

A The centrali- -- yes.

Q Is that paragraph indicating that one 4-megabyte L3 region can access another 4-megabyte L3 region?

A So it does have a single lateral L3 region dispatch port. So data can go from L3 to -- from one L3 region to another L3 region through the controller.

Q What do you mean "through the controller"?

A Well, it says, "The centralized L3 region controller provides a single core/L2 dispatch port, a single lateral L3 region dispatch port," and so on.

So it's the controller that has the port. So it -- therefore, the data needs to go through the controller.

Q Pardon me. A couple of paragraphs down in that right-hand column on page 19, there's a paragraph that begins "storage accesses that miss both the L2 cache and

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the 4-megabyte local L3 region are broadcast to the coherence fabric and snooped by the memory controller, other L2 caches, possibly other L3 caches, and by the seven remote 4-megabyte L3 regions that comprise the remaining 28 megabytes of the on-chip L3 cache."

Do you see that?

A Yes.

Q So is it correct, then, that coherency amongst the caches is maintained by the snooping actions of these various constituents, the memory controller, the other L2 caches, the other L3 caches, and the other seven L3 regions?

A Yes.

Q There seems to be a distinction between the other L3 caches and the seven remote 4-megabyte L3 regions that Sinharoy's making in this passage. Do you know what he's referring to?

A Well, it says "possibly other L3 caches." Let me look for -- if there's any other L3 caches other than the 4-megabyte L3 regions that constitute the caches. The...

Let's see. So... well, let me go back for a second on the previous answer. I was reading the rest of the paragraph just to be clear. There's two ways that the L3 data can be shared between L3 regions. If you look at the paragraph we were looking at, and if you look -- count

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one, two, three, four -- five from the bottom, it says, "Whereas lateral cast-outs access a given 4-megabyte L3 region via a lateral L3 region dispatch port (see targeted cases below) or via the snoop dispatch port (see the [sic] state merge cases below)."

So just to be clear, you know, there's a couple of paths for the lateral -- the L3 lateral of the -- the lateral L3 region dispatch.

So what I was going to go now when you were asking me about the L3, the possible L3 -- other L3 caches.

So if you look on page 17, the second column, the -- so one, two, three, four -- fifth line down below the table, it says, "Since the POWER7 32-megabyte L3 cache resides on the processor chip, it provides lower latency access (even to 28 megabytes composed of nonlocal L3 regions) than the POWER6 off-chip 32-megabyte L3 cache."

So seems to indicate on top of the 32-megabit, you know, L3 caches, there's a 28-megabyte nonlocal L3 region, part of the L3 cache. So that's -- that might be what they're referring to there. But I don't recall seeing any further discussion of that L3 -- you know, the additional area of nonlocal L3 cache, unless -- let's see. Thirty-two... well, let me go back to that. Unless they're referring to... no. No, the 28 is 32 minus 4.

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So the non-local L3 region is not an additional reason. It's the other seven 4-megabyte pieces. So I don't know what other L3 region it's referring to in that sentence you described -- you showed me.

Q That's fine. If you look at the diagrams, figures 11 and 12 on page 24, it looks like there are arrangements where you could connect multiples of these POWER7 chips?

A Yes.

Q Could that sentence we were talking about be referring to L3 caches on different chips in an arrangement like what's shown in figure 11 or 12?

A It's possible. They -- there are -- there is description of cache coherency across multiple chips in these two pages here.

Q Okay. Let's go back to that part of the paragraph on page 19 that you raised. Again, we're looking at the paragraph that begins with "Storage accesses that miss both the L2" and the "local L3."

You pointed out there were a couple of situations covered in this paragraph. The first one being that "operations that miss the 4-megabyte local L3 region but hit in the remaining 28 megabytes of the L3 cache access the cache via the snoop dispatch ports."

Do you see that?

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A Yes.

Q Is that indicating that a core can access a different L3 region -- that is an L3 region that would be local to another core via the first core's controller's snoop dispatch port?

A I'm sorry. You -- you went silent for a fraction of a second, and I lost the beginning of the question. So if you could repeat it, please.

Q Sure. Yeah. No problem.

I'm wondering if this sentence is indicating that an operation by -- let's call it core 0 that misses core 0's local L3 region but hits in, let's say, core 1's L3 region, can core 0 then access the data that's in core 1's L3 region via core 0's L3 controller's snoop dispatch port?

A That's what that sentence is saying. So that's what happens on a miss. On the bottom of that sen- -- of that paragraph, it says where, yes, "lateral cast-outs access a given 4-megabyte L3 region via the L3 region dispatch port or via the snoop dispatch port. All of the cast-out scenarios are described in detail in the subsequent paragraph."

So I can go look, to answer your question, whether it's -- what is it that gets dispatched through the L3 region dispatch port, if that's helpful.

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Q Yeah. I think that is sort of what's being shown in figure 10 on the next page, at least partially. Isn't it that if there's a cast-out from a core's 4-megabyte local L3 region, it could be -- the data could be cast out into another core's 4-megabyte L3 region rather than all the way back to memory; is that right?

A It looks like it. There's the purple -- there's a solid purple line showing, you know, from the one L3 region and then the dotted ones indicating that the rest of them have that relationship back to the local L3 region.

Q And this is discussed in the text on page 20 below that figure 10 in the right-hand column. For example, the paragraph begins, "When a lateral cast-out from an L3 region" and goes on. And then sort of midway down that paragraph, there's a sentence that reads, "If the lateral cast-out is accepted by the targeted L3 region and needs to allocate a line (i.e., does not find an invalid slot), it also preferentially selects the LRU" -- and I assume that's least recently used -- "line from the second class, only displacing the first-class line if no second-class lines exist."

Do you see the passage I'm referring to?

A I do.

Q So is that indicating that if one L3 region wants

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to cast-out data into another L3 region, the controller for that other L3 region has to accept the data?

A That's what it says. Yes.

Q If I can have you turn to page 22, please.

A Yes.

Q In the right-hand column, the discussion of the "I/O subsystem" begins. And at the end of that first paragraph under that section heading, it indicates that the POWER7 I/O controllers "support cache injection."

Do you see that?

A Yes.

Q And this cache injection enables DMA write traffic to be written directly into the cache instead of memory; is that right?

A Yes.

Q This seems similar to the kind of DMA transaction we were talking about -- I think it was in connection with Agarwal; is that right?

A Yes. It's writing straight from the I/O into a cache rather than into memory. So it's without writing into memory.

Q And that's the case if a core's L2 or L3 owns a copy of that memory address; right?

A I don't recall it talked about the details of how that's done, you know, whether it owns it or what needs to

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happen. But, you know, the disclosure is that the writing can happen directly into the cache.

Q If you look back at page 17.

A Page 17?

Q Yes. Page 17.

A Mm-hmm.

Q In the right-hand column, the paragraph that begins "As shown in table 2," a little bit further down in that same paragraph, there's a discussion of "cache injection."

A Okay. Yeah, I see it.

Q And I think Sinharoy indicates that the DMA write operation from the I/O device can occur if the core's L2 or L3 "owns a copy of the targeted cache line."

A Yes. That's what it says. So it does disclose that cache needs to own it.

Q Can you turn to page 23, please?

A Okay.

Q In the left-hand column, in the second full paragraph, it begins, "The on-chip coherence interconnect routes two sets (even and odd cache line) of coherence requests through the horizontal trunk," et cetera.

Do you see that paragraph I'm referring to?

A I do.

Q So here, in this paragraph and the next one --

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and feel free to read them if you need to refresh your memory -- Sinharoy is talking about how the coherence is affected in the processor; is that right?

A So it is describing part of the communication regarding the coherence algorithm that's here where there's -- everybody receives that information. So it is broadcast.

Q And by "everybody," are you referring to the units that we discussed earlier -- I think it was on page 19 -- that there was the controllers for the L2 caches, the controllers for the different L3 regions, and, I guess, the I/O as well; is that right?

A Yes. And, also, this is discussing even they are sent to the SMP interconnects, which are the ones -- the interconnects that are used to connect the various chips if there are multiple chips that are attached together.

Q So each of those different controllers participate in this snooping behavior when something is broadcast on the coherence interconnect; is that right?

A Yes. All of the controllers are involved in the process.

Q In that regard, are they acting as peers or is one controller an agent or somehow under the direction of a different controller?

A Ask the question again, please.

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Q In the coherence operations that you just described, are the different controllers acting as peers or are -- is one acting under the direction of another?

A Well, I'm not -- I don't know what you mean by "peers." They're operating collectively, but they're doing different functions as they need to. For example, the controller that's broadcasting is performing that operation. The controllers that are listening are doing, you know, particular checks. But collectively, they perform the cache coherency operation.

Q So the ones that are listening, they're each listening with respect to the cache lines or memory addresses that they have responsibility for; is that right?

A They're listening to all of them, but yes. If there's a hit -- if they perceive a hit, they will get involved in the process.

Q I'd like to go back to the '228 patent, please. This was Exhibit 1001 that we discussed earlier today.

A Which patent? Sorry.

Q The '228 patent, the one that's the subject --

A Oh, '228.

Q -- of your declaration.

A Yes. That one.

Q If you could turn back to Claim 1, please.

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A Okay.

Q Earlier we discussed the term "caching agent." Do you remember that?

A Yes.

Q And Claim 1 indicates that the caching agent is a "single caching agent for the multicore processor.

Do you see that?

A Yes.

Q Do you understand the claim as saying that it's this single caching agent that is performing coherency operations for all of the cores and the integrated input/output module?

A Well, it's a single caching agent that includes a plurality of distributed portions. So collectively they are performing the caching agent function of cache coherency, exactly like the Sinharoy and Agarwal structure where you have a multiplicity of the distri- -- you know, you have portions that are distributed amongst the processors, and collectively they're responsible for the cache coherency function of the entire system.

Q Okay. So I'm only asking about what the claim says, Dr. Hassoun, not about any of the references. The -- it's -- as far as this claim is concerned, it's the single caching agent that includes the plurality of distributed portions that performs the coherency

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operations for all of the cores and the integrated input/output module; is that right?

A I don't know why you're rephrasing that, so I'm just going to read the claim. It's "a single caching" agents -- "agent for the" multi-processor -- "multicore processor, and including a plurality of distributed portions, each associated with a corresponding one of the plurality of cores."

I think it's as clear as it can get. I don't need to explain it any further.

Q It says, the caching agent performs "cache coherency operations for the plurality of cores and the IIO module"; is that right?

A That is correct.

Q And that is the same caching agent that is the single agent; is that right?

A Yes.

Q So that single caching agent maintains the coherence state across all of the cores and the IIO module; is that right?

A Maintains? It performs the operation. I don't know what you mean by "maintains." So it's performing these operations.

Q One of the operations would be to maintain the coherency state; isn't that true?

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A That's possible, yes.

Q During our breaks today, Dr. Agarwal [sic], did you discuss the substance of your testimony with anyone?

A I did not.

MR. FAHMI: Well, thank you. I appreciate your time today. I don't have any further questions at this time. I'll pass --

MR. ANDERSON: I don't have any --

MR. FAHMI: -- the witness.

MR. ANDERSON: Oh, I'm sorry. I apologize.

I don't have any questions. We can go off the record.

THE STENOGRAPHER: Off the record at 2:25.

(Time noted 2:25 p.m.)

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CERTIFICATE OF SHORTHAND REPORTER - NOTARY PUBLIC

I, JUSTYNE N. JOHNSON, Certified Reporter and Notary Public within and for the State of California do hereby certify:

That MARWAN HASSUON, PH.D., the witness whose deposition is hereinbefore set forth, was duly sworn by me before the commencement of such deposition and that such deposition was taken before me and is a true record of the testimony given by such witness.

I further certify that the adverse party, TAREK FAHMI, ESQ., was represented by counsel at the deposition.

I further certify that the deposition of MARWAN HASSUON, PH.D., occurred via Zoom videoconference, on Wednesday, November 12, 2025, commencing at 10:04 a.m. to 2:25 p.m.

I further certify that I am not related to any of the parties to this action by blood or marriage, I am not employed to any of the parties to this action, and that I am in no way interested, financially or otherwise, in the outcome of this matter.

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IN WITNESS WHEREOF, I have hereunto set my hand this 12th day of November, 2025.

My commission expires: October 31, 2026

Justyne Johnson
_____

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