

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Arm Ltd, MediaTek Inc.,

Petitioners

v.

Daedalus Prime LLC,

Patent Owner

Patent No. 8,984,228
Case No. IPR2025-00207

**PETITIONER'S RESPONSE TO PATENT OWNER'S REQUEST FOR
DIRECTOR REVIEW**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	THE STANDARD FOR DIRECTOR REVIEW IS NOT MET	1
III.	INDEPENDENT, UNCHALLENGED FINDINGS SUPPORT THE JUDGMENT FOR MANY OF THE CHALLENGED CLAIMS	3
IV.	CLAIMS 6 AND 11: THE BOARD IDENTIFIED THE CLAIMED TRANSACTION PATH.....	3
	A. The Board Properly Analyzed Agarwal’s Disclosure of Claim 11	3
	B. Sinharoy: The Board Relied on the Petition’s Specific IIO-to-Caching-Agent Mapping	5
V.	CLAIMS 2, 3, AND 16: THE BOARD IDENTIFIED THE CLAIMED TOR AND DEDICATED ENTRY	7
	A. Claim 2 (Agarwal): The Board Resolved the Only Dispute PO Presented	7
	B. Claim 3: The Board Adopted the Petition’s Obviousness Showing for the “Dedicated Entry”	8
	C. Claim 16: PO Argued It Only Through Claims 2 and 3	10
VI.	CLAIM 1: THE BOARD GAVE EFFECT TO “EACH ASSOCIATED WITH A CORRESPONDING ONE” OF THE CORES	11
VII.	THE ALTERNATIVE ISSUE-PRECLUSION RULING DOES NOT WARRANT REVIEW	13
	A. The Board Did Not Misstate PO’s Position	13
	B. The ‘1344 IPR Litigated And Decided The “Associated” Issue.....	14

TABLE OF AUTHORITIES

<i>In re Magnum Oil Tools Int’l, Ltd.</i> , 829 F.3d 1364 (Fed. Cir. 2016)	2
<i>KSR Int’l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007)	7
<i>Ohio Willow Wood Co. v. Alps S., LLC</i> , 735 F.3d 1333 (Fed. Cir. 2013).....	14

LIST OF EXHIBITS

<u>Exhibit</u>	<u>Description</u>
Ex-1001	U.S. Patent No. 8,984,228 to Liu et al. (“the ’228 patent”).
Ex-1002	Patent Center Prosecution History of U.S. Patent No. 8,984,228.
Ex-1003	Declaration of Dr. Marwan Hassoun.
Ex-1004	Curriculum Vitae of Dr. Marwan Hassoun.
Ex-1005	U.S. Patent No. 7,805,575 to <i>Agarwal</i> et al. (“ <i>Agarwal</i> ”).
Ex-1006	B. <i>Sinharoy</i> et al., “IBM POWER7 Multicore Server Processor,” IBM Journal of Research and Development, vol. 5, no. 3, pp. 1:1-1:29 (2011) (“ <i>Sinharoy</i> ”).
Ex-1007	U.S. Patent Appl. Pub. No. 2011/0219188 to Blumrich et al. (“ <i>Blumrich</i> ”).
Ex-1008	U.S. Patent Appl. Publ. No. 2008/0126750 to Sistla (“ <i>Sistla</i> ”).
Ex-1009	<i>Multicore Processors and Systems</i> (S.W. Keckler et al. eds., 2009) (“ <i>Keckler</i> ”).
Ex-1010	U.S. Patent Appl. Pub. No. 2006/0041715 to Chrysos et al. (“ <i>Chrysos</i> ”).
Ex-1011	G. Blake et al., “A Survey of Multicore Processors,” IEEE Signal Processing Magazine, vol. 26, no. 6, pp. 26-37 (Nov. 2009) (“ <i>Blake</i> ”).
Ex-1012	V. Getov et al., “Codesign for Systems and Applications: Charting the Path to Exascale Computing,” Computer, vol. 44, no. 11, pp. 19-21 (Nov. 2011).
Ex-1013	T. Zhou, “Deriving Voltage Tolerance Specification for Processor Circuit Design,” 2011 IEEE 20th Conference on Electrical Performance of Electronic Packaging and Systems, pp. 17-20 (Oct. 2011).

<u>Exhibit</u>	<u>Description</u>
Ex-1014	Library of Congress Record: IBM Journal of Research and Development.
Ex-1015	MARC Record: IBM Journal of Research and Development.
Ex-1016	IBM Journal of Research and Development, vol. 5, no. 3 (2011).
Ex-1017	M.R. Marty, <i>Cache Coherence Techniques for Multicore Processors</i> , Ph.D. Dissertation, University of Wisconsin – Madison (2008) (“ <i>Marty</i> ”).
Ex-1018	Docket Control Order
Ex-1019	Infringement Contentions Cover
Ex-1020	IPR2023-01344 Paper 10 05/28/2024 Patent Owner’s Response
Ex-1021	IPR2023-01344 Paper 20 10/22/2024 Patent Owner’s Sur-reply
Ex-1022	Median Time To Trial
Ex-1023	Declaration of Kelley Hayes Greenfield

I. INTRODUCTION

Petitioner Arm Ltd. (“Petitioner”) respectfully submits this response to Patent Owner Daedalus Prime LLC’s (“PO”) Request for Director Review of the Final Written Decision (Paper 39), as authorized by Paper / Exhibit 3101, the Director’s order dated October 6, 2026. The Request should be denied.

The Board held all challenged claims (1–7, 11–14, and 16–19) unpatentable on five grounds. The trial included expert testimony, an oral hearing, and briefing on the FWD in IPR2023-01344 (which invalidated substantially identical claims in the child patent on the same Sinharoy prior art asserted in the present IPR). FWD 2–3, 58. The Request says it “does not ask the Director to reweigh competing evidence” or “to choose between competing expert opinions.” Req. 1–2. That is nonetheless what it asks. Each limitation the Request calls a “missing finding” is one the Petition mapped to specific prior-art disclosures. The Board summarized that mapping and resolved the arguments PO actually made. Where the Request offers different theories, it offers them for the first time in this Request.

II. THE STANDARD FOR DIRECTOR REVIEW IS NOT MET

Director Review is generally granted to address (1) an abuse of discretion, (2) important issues of law or policy, (3) erroneous findings of material fact, or (4) erroneous conclusions of law. USPTO, *Revised Interim Director Review Process* , June 29, 2026. The requesting party bears the burden of showing such an error.

The process is not a vehicle for new evidence or new arguments that could have been presented to the Board. *Id.* PO primarily invokes only the third and fourth categories. Req. 1. PO invokes an alleged issue of law or policy solely in its preclusion argument, which is addressed in Section VII.

PO cannot meet that burden, for three reasons. First, there is no erroneous finding. A requester's disagreement with how the Board weighed competing evidence is not an error of fact. For each disputed limitation, the FWD identifies the Petition pages and declaration paragraphs it credits. It also explains why it credited Dr. Hassoun over Dr. Bagherzadeh, whose testimony it found conclusory. FWD 35–37. The Board's reasoning would satisfy even the standard a reviewing court applies, because its path can reasonably be discerned. *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016). Granting review to restate findings the record already supports would serve no purpose.

Second, there is no erroneous conclusion of law. Petitioner bore the burden of proving unpatentability by a preponderance of the evidence, 35 U.S.C. § 316(e), and the Board held it to that burden. The Request relies on *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364 (Fed. Cir. 2016), but that case involved a Board decision resting on a theory the petitioner never presented. 829 F.3d at 1375–81. This case is the opposite. Each time, the Board relied on the theory and evidence in the Petition, as developed in a Reply that responded to PO's arguments. Where the

Request offers different theories, it offers them for the first time in this Request, and the process does not permit that.

Third, any alleged error is not material. The Director Review criteria are limited to *material* errors of fact. An error that cannot change the outcome does not justify review.

III. INDEPENDENT, UNCHALLENGED FINDINGS SUPPORT THE JUDGMENT FOR MANY OF THE CHALLENGED CLAIMS

The Request seeks relief only for claims 1–3, 6, 11, and 16–18. Req. 15. Because the alleged errors could not change the outcome for many of those claims, they are not material errors warranting Director Review. For example, the FWD determined claim 1 unpatentable based on Agarwal (Gr. 1) and Sinharoy (Gr. 2A). FWD 58-59. The Request attacks only the Agarwal analysis of limitation 1e (Req. § IV). It does not challenge the Sinharoy merits finding for claim 1 (FWD 47–50).

Similarly, the FWD determined claim 2 unpatentable on Agarwal (Gr. 1) and Sinharoy + Blumrich (Gr. 2B). FWD 58-59. The Request’s claim 2 argument addresses only Agarwal (Req. § III.B). It identifies no error in Ground 2B’s finding for claim 2 (FWD 55). For claim 6, the Request challenges the Sinharoy analysis (Req. § II.B). It does not challenge the Agarwal finding for claim 6 (FWD 41–42).

IV. CLAIMS 6 AND 11: THE BOARD IDENTIFIED THE CLAIMED TRANSACTION PATH

A. The Board Properly Analyzed Agarwal’s Disclosure of Claim 11

The Request does not challenge the FWD's Agarwal analysis for claim 6. FWD 42 (citing Pet. Reply 19; Ex. 1005, 28:23–32). PO's "intervening path" argument for claim 6 is directed only to Sinharoy. Req. 3–4.

For claim 11, the Request argues that the Board answered an "unasserted 'proxy' limitation" rather than the claimed recipient. Req. 4–6. But "proxy" was PO's term and argument. PO argued the '228 patent "teaches proxying IIO traffic [to] a shared CPU/IIO coherency agent" and this "proxying step (and the identity of the recipient)" is missing from Agarwal. PO Resp. 31; FWD 43. The Board answered the argument as PO framed it. It agreed with Petitioner the specification "mirrors the claim language . . . but it does not impose further restrictions (proxy or otherwise) on the forwarding." FWD 43–44 (quoting Pet. Reply 21).

The "identity of the recipient" argument also fails on its own terms. The recipient recited in claim 11 is "a caching agent . . . shared by a plurality of cores . . . and the IIO module." The Petition identified that recipient as the same distributed caching agent mapped for limitations 1d and 1e. The home tile's directory controller and directory storage are one distributed portion of that agent. Pet. 33. The Board found that Agarwal's directory controllers collectively form a single caching agent that performs coherency operations for both the cores and the IIO module. FWD 33–38. Forwarding the transaction to the home tile's directory controller is therefore forwarding it to a portion of the shared caching agent. That

is the same way the '228 patent's Figure 6 caching agent is distributed across slices. Ex. 1001, 6:22–29. PO's contrary argument is simply its rejected "single caching agent" argument restated, as Petitioner explained to the Board. Pet. Reply 20. PO's Sur-Reply did not address claim 11 at all. FWD 44.

B. Sinharoy: The Board Relied on the Petition's Specific IIO-to-Caching-Agent Mapping

The Request's claim the Board relied on a single Sinharoy sentence (Req. 3) misreads the FWD. The Board cited Petition page 58. FWD 52. Pages 58-59 explain (1) Sinharoy's integrated I/O controllers are the claimed IIO module and connect PCI devices through an I/O hub; (2) an I/O device sends a cache-injection "write operation" (the allocation transaction); and (3) the coherence fabric's L3 "write machines" receive that operation and write the data into the L3 cache. Pet. 57–60 (citing Ex. 1006, 17, 19, 22; Ex. 1003 ¶¶ 417–429, 441–447). Sinharoy states "I/O controllers also support cache injection, which enables DMA write traffic to be written directly into a cache, instead of to memory." Pet. 41 (quoting Ex. 1006, 22). PO did not dispute Sinharoy's I/O controllers are the claimed IIO module. *See* Pet. 41; FWD 47 (only limitation 1e disputed for claim 1).

PO's Response described the same path. It stated that in Sinharoy "the I/O controllers implement cache injection by writing into an L3 region." PO Resp. 40. In other words, the transaction moves from the IO device, through the integrated

I/O controller (the IIO module), to the L3 region controller (a portion of the caching agent). PO's real dispute was whether the L3 controllers form a "single" caching agent. *Id.* at 40–41; PO Sur-Reply 25–26. The Board resolved that dispute against PO, and the Request does not challenge that resolution. FWD 49–50.

The '1344 IPR record confirms the point. There, PO did not dispute that Sinharoy's "two integrated I/O controllers" are an IIO module interfacing with IO devices such as I/O hub chips and PCI adapters. It did not dispute that the caching agent performs coherency operations for those integrated I/O controllers, which "support cache injection." And it did not dispute that the processor receives allocation transactions from IO devices and stores their data directly into the shared cache. The Board so found. IPR2023-01344, Paper 31 at 21–23. PO did not appeal. The only new element in claim 6 is that the caching agent receives the transaction "from the IIO module." Sinharoy discloses that element when it describes I/O-device DMA writes injected into the cache through the integrated I/O controllers, as PO's own description of Sinharoy acknowledges. PO Resp. 40.

The Request's focus on the word "or" in "via an integrated I/O controller or the SMP interconnect" (Req. 4) also fails. The Petition identified both the integrated I/O controllers and the SMP interconnect as IIO modules under limitation 1c, and PO disputed neither. Pet. 40–44; FWD 47. When either of two disclosed paths satisfies the claim, identifying both is not a failure of proof. Nor

did the Board need to make an inherency finding. The issue is obviousness, and the Board could account for what a person of ordinary skill would understand from Sinharoy's disclosure that I/O-originated DMA writes are injected into the cache through the integrated I/O controllers. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Claim 11 adds nothing new. PO argued claim 11 against Sinharoy only by repeating its claim 6 argument (PO Resp. 41–42), and the Board properly decided claim 11 on that basis. FWD 53.

V. CLAIMS 2, 3, AND 16: THE BOARD IDENTIFIED THE CLAIMED TOR AND DEDICATED ENTRY

A. Claim 2 (Agarwal): The Board Resolved the Only Dispute PO Presented

PO's claim 2 argument was that the TOR must be a single, "centralized," "shared" structure, and that Agarwal's per-tile buffer is not. PO Resp. 21–27; PO Sur-Reply 20–24. Petitioner responded that the '228 patent itself discloses a separate TOR in each distributed caching-agent portion. Pet. Reply 13–18 (citing Ex. 1001, Fig. 5, 5:31–33, 2:67–3:3). The Board recited both positions and then found that "Agarwal's buffer corresponds to the TOR." FWD 38–40. At the hearing, PO abandoned the premise of its own argument. It conceded that "we're not precluding the table of requests from being distributed" and that "we're not saying it has to be a single physical table of requests." Tr. 27:10–28:18.

The new attributes the Request now says are missing (that the buffer is

within the caching agent, stores pending requests, and serves both sources) were addressed in the Petition and were never disputed by PO. The Petition explained that Agarwal’s “small buffer that contains a list of outstanding transactions” is part of the directory state maintained by each directory controller (*i.e.*, within the caching agent). The Petition further explained that the buffer stores outstanding transactions “involving the plurality of cores and I/O module,” because the home tile performs coherence processing for I/O-module requests “just as it would” for core requests. Pet. 24–25, 21–22 (citing Ex. 1005, 27:11–25, 29:5–31; Ex. 1003 ¶¶ 204–213). PO agreed that Agarwal’s buffer is a “structure that tracks outstanding transactions for that tile’s directory controller” and stated, “Indeed, Agarwal describes such a local buffer.” PO Resp. 22–24. PO cannot fault the Board for failing to make findings on issues it never contested. The ’228 patent also defines the TOR broadly, as “a buffer or other temporary storage for holding incoming requests.” Pet. 24 (quoting Ex. 1001, 2:46–48); FWD 40. And as noted above, the Request does not address the independent Ground 2B finding for claim 2. FWD 55.

B. Claim 3: The Board Adopted the Petition’s Obviousness Showing for the “Dedicated Entry”

The Request argues that the Board identified only “a transaction type,” not a dedicated entry. Req. 7–9. But the Petition did not argue that Blumrich’s queue expressly reserves an entry. It made an obviousness argument, which the Board

adopted. FWD 55. Sinharoy discloses a pool of operational resources in each L3 controller. That pool includes “eight read machines,” “24 lightweight RC machines,” and “ten write machines.” The write machines handle data writes, including “I/O cache injection operations.” Pet. 64–65 (citing Ex. 1006, 17–20). Sinharoy therefore already segregates capacity by transaction class: writes, including cache-injection writes, go to resources set aside for them. The Petition explained that a cache-injection write is a “posted transaction” under the ’228 patent’s own definition. It further explained that, because the write machines include temporary storage, “it would be obvious to include dedicated queues or resources (i.e., dedicated entry) to store such a write transaction (i.e., posted transaction).” Pet. 68–69 (citing Ex. 1001, 5:3–7; Ex. 1003 ¶¶ 476–479); Pet. Reply 28–29. PO itself acknowledged that Sinharoy’s “specialized RC and write machines manage different transaction types.” PO Resp. 43; *see* Pet. Reply 28.

The Board summarized exactly this reasoning: “when Sinharoy’s ‘write machines perform cache injection operations, they write into L3 cache,’” and that write “is a ‘posted transaction.’” FWD 55. The Board then found that PO’s arguments had been “previously addressed and found to be lacking,” and credited Dr. Hassoun’s testimony throughout. FWD 36–37, 56. That is a reasoned adoption of a specific, evidence-backed obviousness theory, not a missing finding. *Belden* does not suggest otherwise. The Petition supplied both the structure (resources

dedicated by transaction class) and the reason to dedicate an entry to posted writes, supported by expert testimony (Ex. 1003 ¶ 478).

PO's point that Blumrich's queue receives core requests (Req. 8; Ex. 2007, 26:15–21) misses the combination. Petitioner relied on Sinharoy, not Blumrich, for the core and IIO request sources and for the write machines that handle I/O cache injection. Blumrich was cited for using a request queue to track pending requests. Pet. 64–68; Pet. Reply 28 (“PO does not dispute that Sinharoy's structure holds caching operations for core and IIO requests.”). Moreover, in the IPR2023-01344 proceeding PO did not dispute that Sinharoy taught the claims of the child '895 patent that are substantively identical to claims 2 and 3. Pet. 63 n.7.

C. Claim 16: PO Argued It Only Through Claims 2 and 3

The Request faults the Board for not separately analyzing claim 16's TOR limitation. Req. 9–10. But PO never argued claim 16 separately. Its Response said only that “all of the reasons for patentability of Claims 2 and 3 discussed above apply equally to Claim 16.” PO Resp. 49. The Petition mapped limitation 16[e] to the same claim 2 and claim 3 analysis, applied to each processor in Sinharoy's multi-chip system. Pet. 71. A Board decision that treats a claim the same way the parties did is not error. The Request's new argument that the record does not establish “the first IIO module as a source of requests” (Req. 9) was never raised to the Board. It also fails on the merits: Sinharoy's integrated I/O controllers are the

first IIO module of each POWER7 chip, and their cache-injection writes are handled by that chip's write machines. Pet. 57–58, 66–67, 70–71.

VI. CLAIM 1: THE BOARD GAVE EFFECT TO “EACH ASSOCIATED WITH A CORRESPONDING ONE” OF THE CORES

The Request's claim 1 argument goes only to Agarwal. As shown in Section III, the unchallenged Sinharoy merits finding sustains the unpatentability of claim 1. Moreover, the Board noted that PO's argument related to this term was “all but identical to the one made and rejected in the '1344 IPR in connection with Sinharoy.” FWD 33. PO does not address this finding and should not be heard to re-litigate losing positions that it did not appeal on identical claim language.

PO's argument also fails on the merits. PO argued that Agarwal's directory controllers are associated with memory regions rather than cores, because home tiles are assigned by address. PO Resp. 12–15; PO Sur-Reply 14–17. The Request now argues the words “at least some” versus “each.” Req. 10–12. PO did not challenge the “at least some” in its response or sur-reply. Either way, the Board's finding rests on more than one sentence. FWD 33–38. The Petition relied on Agarwal's Proxy Cache Coherence (“PCC”) embodiment, in which “the directory controller and directory storage are distributed across the tiles—e.g., directory controller 603 and directory storage 604 within each core.” The Petition also cited Figures 6A–6B, in which “[e]ach tile includes a processor 600, L2/L3 cache 602,

directory controller 603, and directory storage 604.” Pet. 17–18 (citing Ex. 1005, 16:27–34, 11:11–26, Fig. 6B); FWD 26, 34. The Petition also relied on Agarwal’s teaching “[e]ach of at least some of the processor cores includes a directory controller,” and explained “[e]ach directory controller 603 / directory storage 604 pair” is associated with the processor 600 in its tile. Pet. 23–24 (citing Ex. 1005, 4:7–8, 6:35–36). In the PCC configuration the Board credited (FWD 28-29, 33-38), every core has its own controller portion. That is a one-to-one correspondence.

PO’s address-homing point does not negate that correspondence. Dr. Hassoun explained, and the Board credited, that Agarwal’s distributed portions each manage a slice of the shared cache while collectively serving every core. That is the same arrangement the ’228 patent describes, in which each caching-agent portion is “associated with a corresponding core and LLC bank or slice.” Ex. 1001, 2:67–3:3; FWD 31–38. PO conceded at the hearing that, in the ’228 patent’s Figure 6, each portion 715 is associated with “the core that’s next to it,” and that the last-level cache remains “a shared cache.” Tr. 22:2–19. The ’228 patent thus contemplates portions that are each tied to a core while also serving shared, address-partitioned cache slices that any core may access. PO’s position that a portion cannot be “associated” with its core if it also serves other cores’ requests for its slice would read Figure 6 out of the claims. The Board reasonably rejected that position. FWD 33–38. The Request’s reliance on *Merck* adds nothing. The

Board gave meaning to every term. It simply declined to read in PO's "functional association" gloss, which has no basis in the intrinsic record. *See* Pet. Reply 11–13.

VII. THE ALTERNATIVE ISSUE-PRECLUSION RULING DOES NOT WARRANT REVIEW

The Board decided *Sinharoy* on the merits and stated it "need not rely on issue preclusion." FWD 22 & n.16. PO concedes that "[c]orrection of estoppel alone may therefore not alter the judgment." Req. 13–14. Director Review of an alternative holding not affecting the outcome is advisory and should be denied.

A. The Board Did Not Misstate PO's Position

The Request says the Board misstated the record when it observed that PO "seemingly accepts" claim 1 is subject to issue preclusion. Req. 12. PO's briefs support the Board's qualified observation. PO told the Board "[a]t most, any preclusive effect is limited to the narrow 'single caching agent' characterization in Claim 1, and it has no effect on Claims 11 or 16." Paper 35 at 2, 7. Its reply brief repeated "[a]t most, any preclusive effect is limited to the Board's prior determination regarding the 'single caching agent' aspect of Claim 1." Paper 37 at 7. PO stated it "does not ask the Board to revisit that determination" and "is not challenging the correctness of the prior FWD." *Id.* at 2, 7. PO devoted a separate section arguing preclusion could not reach claims 11 and 16, while offering no comparable claim-level argument for claim 1. Paper 35 at 6–7; Paper 37 at 4–5.

Against that record, the Board’s statement that PO “seemingly” accepted preclusion of claim 1 was a fair, hedged reading, and the Board cited the pages on which it relied. FWD 22 (citing PO Reply Br. 4–5). The Board also did not rest on any concession. It separately recounted and rejected PO’s identity-of-issues argument about the “associated” limitation. FWD 20–22. A characterization that affects no holding is not a material error.

B. The ‘1344 IPR Litigated And Decided The “Associated” Issue

Nor does the ruling present an policy question warranting Director attention. The Board applied settled law that PO “does not dispute.” FWD 20, 22. Claims need not be identical and it is the identity of the issues that determines whether collateral estoppel applies. *Ohio Willow Wood Co. v. Alps S., LLC*, 735 F.3d 1333, 1342 (Fed. Cir. 2013). The ’895 patent’s claim 1 recites the same “single caching agent . . . includ[ing] a plurality of distributed portions each associated with a corresponding one of the plurality of cores” limitation, in the same words, as claim 1 of the ’228 patent. FWD 16 n.7; IPR2023-01344, Paper 31 at 7; Paper 34 at 1.

PO’s premise is that the ’1344 Board decided only “logical unity” and never decided whether Sinharoy’s portions are associated with corresponding cores. Req. 12–13; Paper 35 at 4–6. The ’1344 decision refutes that premise. In resolving limitation 1g., the ’1344 Board found that the claimed “single caching agent” like each of Sinharoy’s local L3 regions that share capacity, data flow logic, and

control flow logic “with one another and their associated L2 cache for a particular core.” IPR2023-01344, Paper 31 at 27–28. The Board relied on Sinharoy’s description of “the tight coupling between a given 256-KB L2 cache and its corresponding 4-MB local L3 region.” *Id.* at 26 n.8 (quoting Sinharoy at 19). It then held that Petitioner had shown limitation 1g, in its entirety, disclosed or suggested by Sinharoy. *Id.* at 28. That is a finding on the core-association question that was necessary to the judgment that the ‘895 patent’s claim 1 was unpatentable.

PO’s “address-homing” theory is a new argument about the same limitation and the same reference. PO had every opportunity to make it in the ’1344 IPR, where it argued that Sinharoy’s L3 regions are snooped and accessed by other cores. *Id.* at 24–26. The ’1344 Board considered PO’s argument and found it “does not alter our determination.” *Id.* at 28. A party cannot avoid preclusion by offering a new argument or new evidence on an issue already decided.

Finally, the Request’s reference to the vacatur of the original discretionary-denial decision (Req. 14) has no bearing on the preclusion analysis.

VIII. CONCLUSION

PO’s Request does not identify any issues that legitimately fall within the criteria for Director Review. At most, PO’s Request identifies factual findings with which it disagrees and which the Request discusses only part of the Board’s analysis and does not establish that the findings, as a whole are erroneous.

October 14, 2026

Respectfully submitted,

Kevin P. Anderson

USPTO Reg. No. 43,471

CERTIFICATION

As authorized by Paper / Exhibit 3101, the Director's order dated October 6, 2026, this brief contains 15 pages.

Dated: October 14, 2026

By: Kevin P. Anderson
Kevin P. Anderson, Lead Counsel
Reg. No. 43,471

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(a), the undersigned certifies that on October 14, 2026 a copy of the foregoing Response was served Pursuant to 37 CFR § 42.105 and agreement on counsel via electronic download to the following attorneys:

Tarek Fahmi

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Date: October 14, 2026

By: Kevin P. Anderson
Kevin P. Anderson