# A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme

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***Abstract*— While the performance of flash memory exceeds hard disk drives in almost every category, the cost of flash memory must come down in order to gain wider acceptance in mass storage applications. This paper describes a 3.3 V-only 32 Mb NAND flash memory that achieves not only high performance but also low cost with a 94.9 mm$^2$ die size, improved yields, and a simple process with 0.5 $\mu$m CMOS technology. Die size is reduced by eliminating high voltage operation on the bitlines through a self boosted program inhibit voltage generation scheme. Incremental-step-pulse programming results in a 2.3 MB/s program data rate as well as improved process variation tolerance. Interleaved data paths and a boosted wordline results in a 25 ns burst cycle time and a 24 MB/s read data rate. Maximum operating current is less than 8 mA.**

## I. Introduction

SINCE first being introduced, the capabilities of flash memory have improved dramatically. Device density, performance, and endurance have all seen orders of magnitude improvement. When compared to magnetic media based hard disk drives (HDD), flash memory offers higher performance, lower power consumption, increased reliability, and greater portability. However, the acceptance of flash memory in the solid state mass storage market has not yet met expectations mainly due to its cost. Even when compared to the "expensive" PC Card type HDD's, flash memory cards cost over 10 times as much. This high cost of flash, and not density limitations, is the biggest obstacle against the acceptance of high capacity flash memory cards.

The NAND type flash memory [1], [2] was originally developed to target solid state mass storage applications. Toward this end, NAND offers a small cell size, low power consumption, and fast page based read/program operations. In addition, the small erase block size and fast erase times of NAND make it a very manageable memory. This 32 Mb NAND flash memory further enhances the key features of the NAND architecture. The new device not only improves on performance features, but cost has been reduced as well through a small die size and yield improvement techniques.

To inhibit programming of selected cells in previous NAND flash memories, a high voltage is supplied directly through the bitlines of program inhibited cells. The high voltage is passed to the NAND string channel to prevent Fowler-Nordheim tunneling from occurring. However, a large capacity charge pump is required to set the highly capacitive bitlines to the inhibit voltage. This charge pump occupies a large silicon area and increases both program time and current consumption. To avoid having to supply high voltages through the bitlines, this flash memory utilizes a self-boosting scheme to generate the required program inhibit voltage on the NAND string channel. With the self boosting scheme, the maximum voltage on the bitlines is $V_{cc}$. Low voltage only bitlines not only eliminate large charge pump area, but also reduces the cell array size since a tighter bitline pitch is allowed with the less stringent bitline isolation requirements.

The page buffer scheme in this flash memory allows the programmed cell $V_t$ to be optimized on a cell-by-cell basis even though a page of cells are programmed simultaneously. One drawback, however, is that the page program speed is determined by the slowest programmed cell within the page. While simply using a higher program voltage would result in a faster program time, easily programmed cells might be overprogrammed. In this device, incremental step pulse programming (ISPP) is introduced to dynamically optimize program voltage according to cell characteristics on a cell-by-cell basis. With ISPP, a typical 2.3 MB/s program performance is achieved while still maintaining a very tight programmed cell threshold voltage distribution. In addition, excellent process and environmental variation tolerance is also obtained. This improved variation tolerance improves the yield of the device.

A 24 MB/s read throughput is achieved with interleaved data paths and boosted wordlines. The device is fabricated on a 0.5 $\mu$m CMOS process with a die size of 94.9 mm$^2$. The device organization is shown in Section II. The page buffer and basic device operation is explained in Section III. In Section IV, self boosted program inhibit voltage generation and its benefits are described. The details of ISPP are presented in Section V. Performance measurements of a fabricated device are summarized in Section VI.

## II. Device Organization

To minimize the die size, the 34 603 008 cells are organized in a single 8 k row by (4 k + 128) column array. An extra 128 b are added to each row to form a spare data area. The cells in the spare data area are not different from any other cell and are part of the same read/program/erase unit as the other cells in the same row. While not restricted in any way, the spare data area

Manuscript revised July 28, 1995.
The authors are with the Sumsung Electronics Co., Ltd., Kyungki-Do, Korea.
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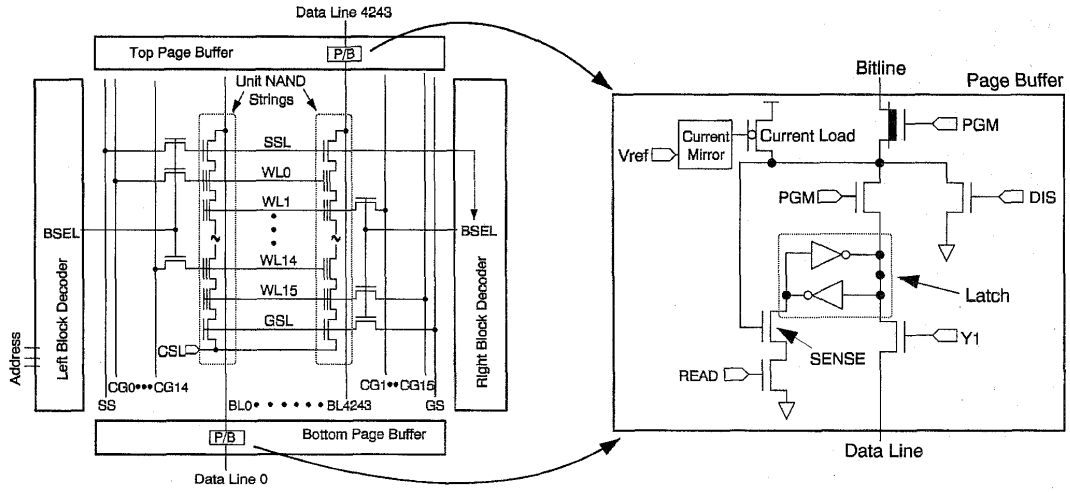



Fig. 1. Cell array organization and simplified page buffer circuit.

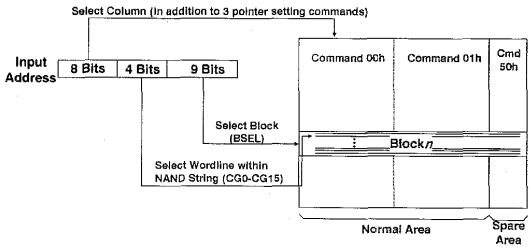
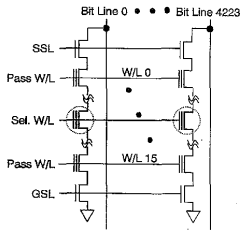



Fig. 2. Address decoding scheme.




Key Bias Conditions

| | Erase | Read | Program |
|---|---|---|---|
| Sel. W/L | 0 | 0 | 15/20 |
| Pass W/L | 0 | 4.5 | 10 |
| SSL | F | 4.5 | Vcc |
| GSL | F | 4.5 | 0 |
| "0" B/L | F | 1.8 | 0 |
| "1" B/L | F | 0.7 | Vcc |
| Bulk | 21 | 0 | 0 |

Fig. 3. Key bias conditions for erase, read, and program operations. Shaded boxes indicate bias conditions that are different from previous NAND flash memory.

is typically used to store system data and/or ECC data. If not used, access to the spare data area can be disabled altogether to make the size of each row exactly 4 kb. Each cell in the memory array is part of a unit NAND string which consists of 16 cells and two select transistors (controlled by SSL and GSL) as shown in Fig. 1. A single contact connects two symmetrically opposed unit NAND strings to the bitline, resulting in 1 contact per 32 cells. This minimal contact overhead results in the very small cell size of the NAND architecture.

Program and read operations are performed in page units of (512 + 16) bytes. A page corresponds to a row of cells and is accessed by a single wordline. The basic erase unit is a block of 16 pages, or (8 k + 256) bytes. Each block corresponds to a row of unit NAND strings and are selected through separate block select signals (BSEL). Individual word lines are accessed through a combination of the BSEL and the common gate lines (CG0–CG15) as shown in Fig. 1. CG0–CG15 are connected to the WL0–WL15 of each row of unit NAND strings through pass transistors. All pass transistors of a block are activated together by the block's BSEL signal. The BSEL signal and CG lines are independently decoded from the given input address as shown in Fig. 2. Block decoder design is simplified through the use of a common set of CG signals between all blocks. The BSEL signal is generated from the left and right block decoders where the right block decoder is activated by the left one. This split block decoder design allows a 0.95 $\mu$m wordline pitch. To accommodate the 1.4 $\mu$m bitline pitch, page buffers are split into top and bottom banks. The page buffers in the top bank are connected to odd numbered bitlines while those in the bottom bank are connected to even numbered bitlines.

## III. Device Operation

In order to perform page based read and program operations, a page buffer is attached to each bitline. The key components of the page buffer are a latch and a sense transistor as shown in Fig. 1. Though simple in design, the page buffer serves several important functions. First, it senses and latches cell data during read operations. Second, it holds program status data during program operations. And third, it controls cell-by-cell program optimization during program verify operations. Bias conditions for ERASE, READ, and PROGRAM operations are shown in Fig. 3.

ERASE operations can be performed in single or multiple block units, where up to all 512 blocks can be erased simultaneously. With lines CG0–CG15 of Fig. 1 grounded, the BSEL of selected block(s) are set high while those of unselected blocks are set low. This grounds the wordlines

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of selected blocks and floats the wordlines of unselected blocks. A 21–V 3.5–ms erase pulse is then applied to the bulk. In the selected blocks, the erase voltage creates a large (21 V) potential difference between the bulk and the control gates. This causes F-N Tunneling of electrons off the floating gate and into the bulk, resulting in a typical cell threshold voltage of −3 V. Since overerasure is not a concern in NAND flash, cells are deliberately overerased to −3 V to ensure that only a single erase pulse is required. Also, the low erased cell threshold voltage provides additional margin against upward threshold voltage shifts that arise from cycling. Unselected blocks are not affected by the erase pulse due to the coupling of the floating control gate to the bulk. The floating control gate is composed of the source side of BSEL transistor, a metal connection from the source to the poly wordline, and the poly wordline. The coupling ratio can be calculated by considering capacitances connected to the floating wordline. These capacitances include source-junction capacitance, source and gate overlap capacitance, poly and metal field capacitance, and poly wordline capacitance over the (pocket p-well) bulk. Of these, the capacitance between the poly wordline and the bulk (which is responsible for the coupling to the erase voltage) is two orders of magnitude larger than the sum of the rest. The coupling ratio computes to over 98%, more than sufficient to prevent F-N Tunneling from occurring. An erase verify operation is performed on each of the selected blocks to ensure that the threshold voltage of all cells in the blocks are below −1 V. Verification of all cells in a block is performed in parallel through a single read operation which only requires 7.5 $\mu$s.

In READ operations, a page of cell data is simultaneously transferred to the page buffer latches then read out in a sequential burst. To sense a row of cells, the page buffer latches are first initialized to "0" (logical low value), the bitlines are discharged to 0 V, and the SSL and GSL lines are raised to 4.5 V as shown in period $t1$ of Fig. 4. The selected wordline is then applied by 0 V and a 4.5 V pass voltage is applied to the unselected wordlines in period $t2$. Since the 4.5 V on unselected wordlines is higher than the threshold voltage of both programmed and erased cells, all unselected cells will act as pass transistors. On the other hand, the 0 V selected wordline will only turn on erased cells. This causes unit NAND strings with an erased selected cell to form a path to ground and those with a programmed selected cell to be open. In period $t3$, the direct sensing path from bitline to latch is disabled by setting PGM of Fig. 1 low so that the latch value can only be changed through the SENSE transistor. A rising $V_{\text{ref}}$ enables the PMOS current mirror load which supplies a 2 $\mu$A load current to each bitline. Bitlines of cells associated with erased selected cells sink the load current and remain low while programmed cell bitlines go to a high potential. The high potential on a programmed cell bitline turns on the associated SENSE transistor and flips the latch to a "1" in period $t4$. Thus, programmed cell latches hold "1" and erased cell latches continue to hold the initial "0" value. These latch values are inverted later in the read path to read as the proper logical levels. Since all latches in a page are set simultaneously, after period $t4$, the latch data can be read out in a sequential burst cycle.

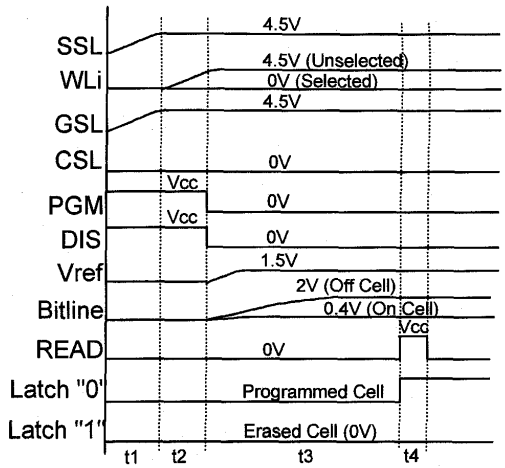


Fig. 4. Circuit timing waveform for read operation.

In program operations, the page buffer latches are first serially loaded with program data: "0" for cells to be programmed and "1" for cells to be program inhibited. Program cycles are then repeated until all cells with "0" latch values are properly programmed. Each program cycle consists of a short program pulse followed by a verify operation in order to avoid over programming of the "0" latch cells. More specifically, the 40 $\mu$s program cycle consists of the following steps:

1) Bitline setup (8 $\mu$s): set bitline voltage level according to program data in the associated page buffer latch: 0 V for programming and $V_{\text{cc}}$ to inhibit programming.
2) Program (20 $\mu$s): apply a short pulse of the program voltage to the selected wordline.
3) Wordline discharge (4 $\mu$s): The high voltage on the selected wordline is discharged so that a low verify voltage can be applied in step 4 below.
4) Program verify (8 $\mu$s): check the threshold voltage of programmed cell to see if it is above the target level.

Further details of the program step are presented in conjunction with the self boosted generation of the program inhibit voltage in Section IV. In the verification step, the latches of cells that are sufficiently programmed are switched from "0" to "1" to inhibit further programming. Bias conditions for the verify operation are similar to the read operation except that the latches hold program status data (they are not initialized to all "0"s) and 0.7 V, instead of 0 V, is applied on the selected wordline. Under these conditions, a latch value is switched from "0" to "1" when the threshold voltage of the associated cell is over 0.7 V; that is, the cell is sufficiently programmed. "1" value latches are not affected since latches can only be flipped from "0" to "1" in the verify operation. Program cycles are repeated until all page buffer latches hold a "1" or the program operation timeout of 10 cycles has been exceeded.

While the ERASE, PROGRAM, and READ operations are similar to the previous NAND device [3], there are notable

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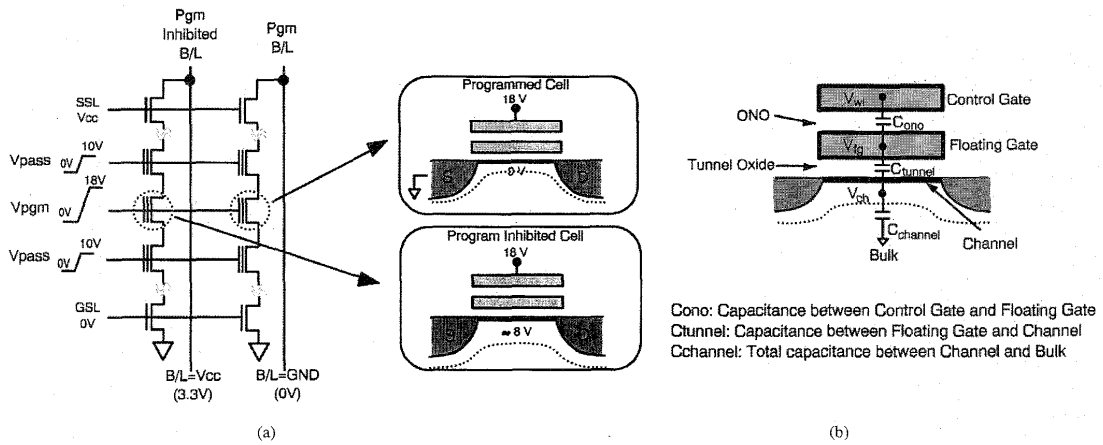


Fig. 5. Self boosted program inhibit voltage generation. (a) Bias conditions for self boosting. (b) Capacitance model for coupling ratio calculation.

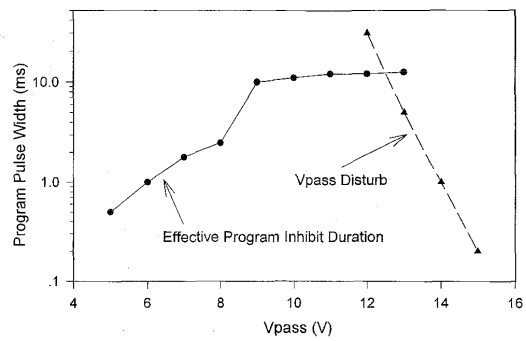


Fig. 6. Program pulse width and $V_{\text{pass}}$ margin test.

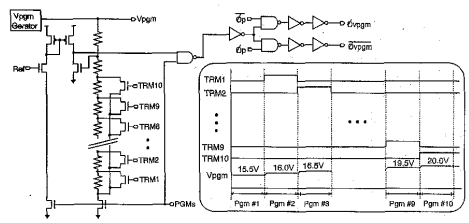

Fig. 7. Circuit and timing diagram for generating incremental program voltages.

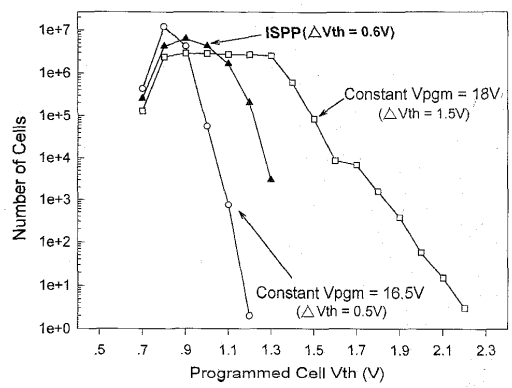


Fig. 8. Comparison of programmed cell threshold voltage distribution in devices with ISPP and without ISPP (constant voltage programming with 16.5 and 18 V).

differences in the bias voltages. The differences are 1) $V_{\text{cc}}$ is applied to the bitlines of program inhibited cells instead of a high voltage, 2) the program voltage is an incremental step pulse from 15.5–20 V, and 3) pass wordlines in read and verify operations are pumped to 4.5 V instead of applying $V_{\text{cc}}$. The reasons for these bias voltage differences are explained in the following sections.

## IV. Self Boosted Program Inhibit Voltage

In previous NAND flash memory, a high program inhibit voltage (e.g., 8 V in [3]) was supplied to the NAND string channel directly through the bitlines. However, there are several disadvantages with this method:

1) A large capacity charge pump is required to supply the high voltage on the highly capacitive bitlines. This charge pump will occupy much silicon area.
2) Time and extra current are required to set up the bitline to a high voltage.
3) Further scaling down of the memory is burdened by the high voltage bitline isolation requirements.
4) The page buffer size is increased due to the high voltage input path and increased transistor size to handle high voltages.

In this device, a self-boosting scheme provides the necessary program inhibit voltage of approximately 8 V even though bitlines are only biased to $V_{\text{cc}}$.

The bias conditions for supplying program inhibit voltages to the channel of selected cells is shown in Fig. 5(a). With the SSL transistors turned on and the GSL transistors turned off, the bitline voltages for cells to be programmed are set to 0 V, while the bitline voltages for cells to be program

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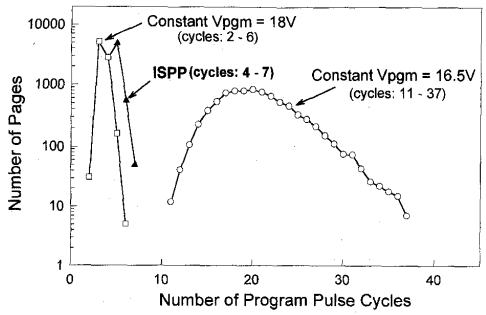


Fig. 9. Comparison of program time in device with ISPP and without ISPP.

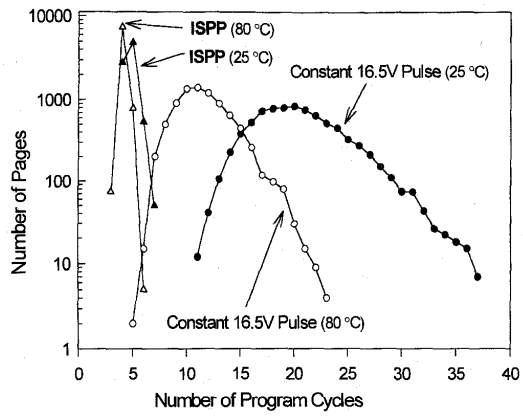


Fig. 10. Program speed variation with temperature in both a device with ISPP and a device without ISPP.

inhibited are set to $V_{cc}$. A 0 V bitline ties the channel of the associated unit NAND string to ground. When the program voltage is applied to the gate of the selected cell, the large potential difference between gate and channel results in F-N tunneling of electrons on to the floating gate, programming the cell. In program inhibited cells, the $V_{cc}$ bitline initially precharges the associated channel. When the wordlines of the unit NAND string rise (selected wordline to the program voltage and unselected wordlines to the pass voltage), the series capacitances through the control gate, floating gate, channel, and bulk are coupled and the channel potential is boosted automatically. Assuming a single boosted pass cell, and the model of Fig. 5(b), the boosted channel voltage, $V_{ch}$, can be estimated as follows:

$$V_{ch} = \frac{C_{ins}}{C_{ins} + C_{channel}} V_{wl} \tag{1}$$

where $C_{ins}$ is the total capacitance between control gate and channel ($C_{ono}$ in series with $C_{tunnel}$)

$$C_{ins} = \frac{C_{ono}\, C_{tunnel}}{C_{ono} + C_{tunnel}}.$$

In program inhibited strings, as the coupled channel voltage rises to $V_{cc} - V_t$ (of the SSL transistor), the SSL transistor shuts off (Fig. 4(a)) and the channel becomes a floating node.

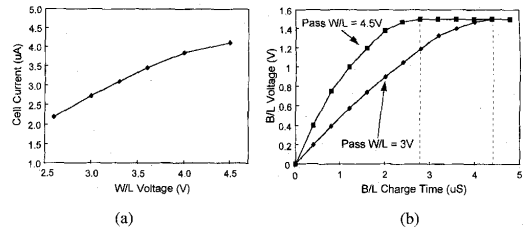


Fig. 11. Benefits of a boosted word line. (a) Wordline voltage versus cell current. (b) Programmed cell bitline sensing time when $I_{load} = 1/2\ I_{cell}$.

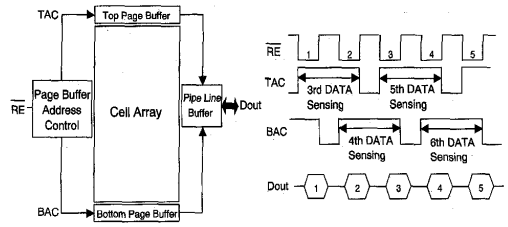


Fig. 12. Interleaved data paths and clock timing diagram.

By calculating (1), it is determined that the floating channel voltage rises to approximately 80% of the gate voltage. Thus, channel voltages of program inhibited cells are boosted to approximately 8 V when program (15.5–20 V) and pass (10 V) voltages are applied to the control gates. This high channel voltage prevents F-N tunneling from occurring in the program inhibited cells.

Through the self-boosted generation of program inhibit voltages, program cycle operating current is reduced by 40% to 4.3 mA. Also, the bitline setup time within each 40 $\mu$s program cycle is less than 8 $\mu$s, saving approximately 20 $\mu$s in bitline precharge time. The effectiveness of the self-boosting scheme is evident in the fact that all 512-byte cells within a page can be programmed on a byte-by-byte basis without program interference. In Fig. 6, it can be seen that self-boosting can effectively maintain program inhibit voltages in program pulses greater than 10 ms when $V_{pass}$ is over 9 V. This is much longer than the required 20 $\mu$s of this device. Also, while the effectiveness of self boosting in generating the inhibit voltage increases with the pass voltage, when the pass voltage is too high, unselected cells will start to get programmed by the pass voltage itself ($V_{pass}$ Disturb in Fig. 6).

## V. Incremental Step Pulse Programming

The intelligent page buffer described in Section III allows cell-by-cell $V_t$ optimization even though a page of cells are programmed simultaneously. However, an unavoidable side effect of this cell-by-cell optimization is that program speed is determined by the slowest programmed cell within the page. Cell program times can vary widely due to nonuniformity in the process ($T_{ox}$, coupling ratio) or changes in the environment ($V_{cc}$, temperature). High program speeds cannot simply be achieved by increasing program voltage since this can result in overprogramming problems that will affect the read and verify operations.

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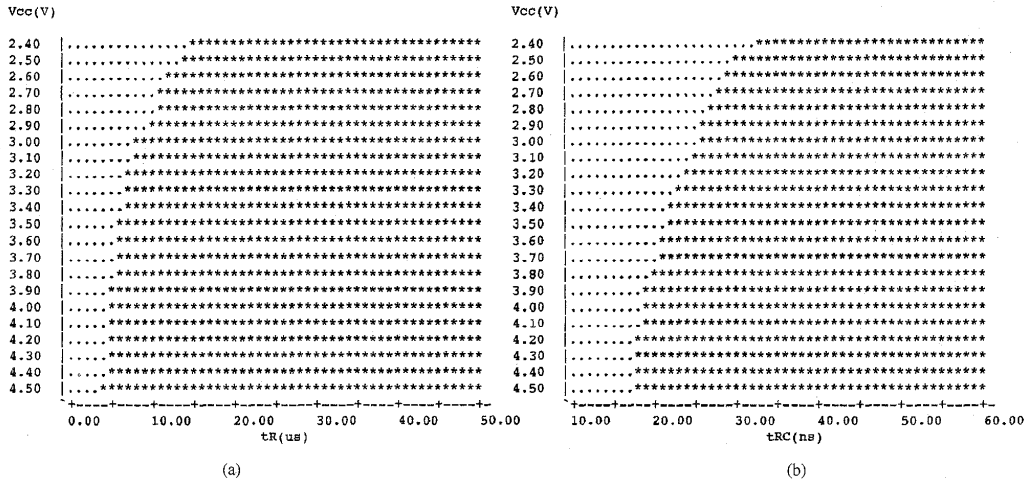


Fig. 13. Schmoo plots showing (a) random cell access. (b) serial burst cycle times.

Incremental step pulse programming (ISPP) achieves fast program performance under process and environmental variations while still keeping a tight programmed cell $V_t$ distribution. ISPP effectively covers process variations by allowing "easily" programmed cells to be programmed with a lower program voltage and difficult-to-program cells to be programmed with a higher program voltage. After an initial 15.5 V program pulse, each subsequent pulse (if required) is incremented in 0.5 V steps up to 20 V. The step pulse is generated by controlling signals that short resistors in the voltage divider shown in Fig. 7. Since sufficiently programmed cells are automatically switched to the program inhibit state in the verification step, easily programmed cells are not affected by the higher program voltages.

A 1 V program pulse increment is approximately as effective as five pulses without the increment. Thus, ISPP has the effect of increasing pulse width [4] without actually increasing the program time by dynamically optimizing program voltage to cell characteristics. Through program pulse/verify cycles, programmed cell $V_t$ is maintained to within 0.6 V as shown in Fig. 8. Fig. 9 shows the distribution of the number of program cycles for all 8 k pages in devices with and without ISPP. With ISPP, a page is typically programmed within five program pulses (200 $\mu$s). While the 18 V constant program voltage device of Fig. 9 shows a slightly faster programming time than the device with ISPP, it can be seen in Fig. 8 that the fast programming device also has a very wide $V_t$ distribution. Similarly, while the constant 16.5 V program voltage device of Fig. 8 has the tightest $V_t$ distribution, it can be seen in Fig. 9 that the tight distribution is obtained at the expense of program speed. ISPP provides an optimum combination of both a tight $V_t$ distribution *and* a fast program time.

Generally, cells tend to be programmed more easily at higher temperatures. In Fig. 10, it can be seen that the device with ISPP is very resistant to temperature dependent variations. The starting voltage in the ISPP scheme is deliberately set low so that additional margin is obtained against variations (e.g. temperature) that cause cells to program more easily. ISPP is also effective under conditions where cells become difficult to program since the incrementing program voltage is an automatic adjustment to these cells.

By effectively adjusting to process and environment variations, ISPP maintains consistent program performance which helps improve the yield of the device. Marginal cells that were previously out-of-spec when conditions were varied are brought within-spec with ISPP. While adjustments to a reference cell have been reported to compensate for die-by-die or sector based process variations [5], ISPP is able to compensate for cell-by-cell variations that can exist within a die.

## VI. Device Performance

Cell sensing speed in read and verify operations is dependent on the current driving capability of the cells. In this device, pass wordlines are pumped to 4.5 V to increase cell current from 2–4 $\mu$A as shown in Fig. 11(a). This larger cell current allows a larger current load (current mirror in Fig. 1) to be used which reduces bitline charge-up time by 37% as shown in Fig. 11(b). Through wordline boosting, 528-bytes of cell data is transferred to the page buffers in 7.5 $\mu$s. A Schmoo plot of the transfer time ($t_R$) is shown in Fig. 13(a).

To offer read and write burst cycle times of 25 ns, the data paths between the top and bottom page buffers are interleaved as shown in Fig. 12. Dual stage pipelining and prefetching of page buffer data results in a very short data latency (relative to RE) of 15 ns. A Schmoo plot of the burst read cycle time ($t_{RC}$) is shown in Fig. 13(b). The total time to read out a page is 7.5 $\mu$s + (528 $\times$ 25 ns) = 20.7 $\mu$s. This corresponds to an effective throughput of 24 MB/s. The typical time to program a page of cells is (528 $\times$ 25 ns) + 200 $\mu$s = 213.2 $\mu$s, for an effective throughput of 2.4 MB/s. A single block can be erased in 3.5 ms.

The endurance characteristics of the 32-Mb NAND flash memory are shown in Fig. 14. After approximately 100–k program and erase cycles, electron trapping in the oxide causes

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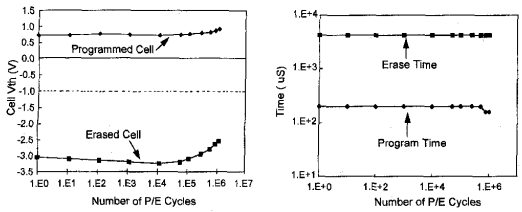


(a) (b)

Fig. 14. The effect of device cycling on program and erase performance. (a) Cell threshold voltage shifts. (b) Erase and program time variation viewed externally.

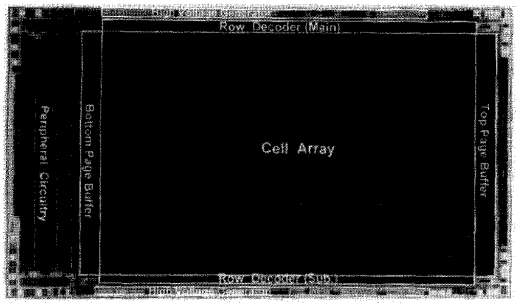


Fig. 15. Chip micrograph.

a general upward shift of cell $V_t$. In Fig. 14(a), it can be seen that the shift is more pronounced in erased cells. However, since the device is designed with sufficient margin against $V_t$ shifts (cells only need to be below $-1$ V to verify correctly), the electron trapping does not affect device performance until well over $10^6$ P/E cycles. In program operations, as the number of P/E cycles approaches $10^6$, the higher $V_t$ of the erased cells helps program cells more easily. This actually results in a shorter program time as shown in Fig. 14(b).

## VII. Summary

A 32 Mb NAND flash memory configured in 4 M $\times$ 8 that operates on a single 3.3 V supply has been successfully developed. Die size has been minimized with a single array architecture and a self-boosted program inhibit voltage generation scheme that reduces charge pump area and allows a tight bitline pitch. ISPP has shown not only to improve program performance but also to improve the yield of the device. In addition, the NAND flash memory achieves high levels of serial access performance through the use of wordline boosting and interleaved data paths.

Fig. 15 shows a micrograph of the 32 Mb NAND flash memory chip. Key device characteristics and parameters are summarized in Table I. The chip has been implemented with a 0.5 $\mu$m design rule, resulting in a die size of 94.9 mm$^2$ and an effective cell size of 1.6 $\mu$m$^2$. A triple-well CMOS process on a p-type substrate is used where the memory array is in the pocket p-well and isolated from the substrate through a surrounding n-well. Only NMOS transistors are used in the high voltage circuits and interconnect is limited to single metal and double poly to simplify the overall process.

TABLE I
Device Characteristics and Attributes

| | | | |
|---|---|---|---|
| • Vcc: | Single 3.3V ± 10% | • Process: | 0.5μm P-Substrate CMOS, Triple Well, Double Poly, Single Metal |
| • Organization: | (4M + 128k) x 8 | | |
| • Address/Command/ Data Input: | Multiplexed, 8 pins | • Effective Cell Size: | 1.6μm$^2$ |
| • Page Size: | (512+16) Byte | • Die Size: | 7.34x12.93= 94.9mm$^2$ |
| • Block Size: | (8k + 256) Byte | • Interpoly Dielectric: | 17nm (Effective) |
| • Cell Access Unit: | Read - Page<br>Program - Page<br>Erase - Block | • Tunnel Oxide: | 9nm |
| | | • Gate Oxide: | 40nm (High Voltage)<br>11nm (Low Voltage) |

## Acknowledgment

The authors thank D. Chin and O. H. Kwon for their support and encouragement throughout this project. Also, the helpful comments and suggestions of S. Ali, T. S. Jung, and J. H. Sim are greatly appreciated by the authors.

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