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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	0299-0004.01
First Inventor	G. R. Mohan Rao
Title	IMPROVED LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM
Express Mail Label No.	

APPLICATION ELEMENTS

See *MPEP chapter 600 concerning utility patent application contents.*

1. ☒ **Fee Transmittal Form** (e.g., PTO/SB/17)
2. ☒ **Applicant claims small entity status.** See 37 CFR 1.27.
3. ☒ **Specification** [*Total Pages* 18]
   Both the claims and abstract must start on a new page
   (For information on the preferred arrangement, see MPEP 608.01(a))
4. ☒ **Drawing(s)** (35 U.S. C. *113*) [*Total Sheets* 5]
5. **Oath or Declaration** [*Total Sheets* 3]
   a. ☒ Newly executed (original or copy)
   b. ☐ A copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 18 completed)
   i. ☐ DELETION OF INVENTOR(s)
   Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or Computer Program *(Appendix)*
   ☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission** *(if applicable, items a. - c. are required)*
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ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers** (cover sheet & document(s))
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10. ☐ **37 CFR 3.73(b) Statement** *(when there is an assignee)* ☒ **Power of Attorney**
11. ☐ **English Translation Document** *(if applicable)*
12. ☒ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☒ Copies of citations attached
13. ☐ **Preliminary Amendment**
14. ☐ **Return Receipt Postcard** (MPEP 503) *(Should be specifically itemized)*
15. ☐ **Certified Copy of Priority Document(s)** *(if foreign priority is claimed)*
16. ☐ **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
17. ☐ Other: _____

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Prior application information: *Examiner* _____ *Art Unit:* _____

19. CORRESPONDENCE ADDRESS

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Name (Print/Type)	David M. Mundt	Registration No. (Attorney/Agent)	41,207

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IMPROVED LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Inventor: G. R. Mohan Rao

CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application is a Non-Provisional Patent Application, claiming priority under 35 U.S.C. §119(e) to U.S. Provisional Application Serial No. 61/509,257, entitled "Improved Lifetime Mixed Level NAND Flash System," filed July 19, 2011, the complete disclosure thereof being incorporated herein by reference. This application also incorporates by reference the complete disclosure of United States Pat. No. 7,855,916, entitled "Nonvolatile Memory Systems with Embedded Fast Read and Write Memories," filed on October 22, 2008 by inventor G.R. Mohan Rao, and issued on December 21, 2010. This application also incorporates by reference the complete disclosure of United States Pat. Appl. No. 12/915,177, entitled "Nonvolatile Memory Systems with Embedded Fast Read and Write Memories," filed on October 29, 2010 (US 2011/0060870 A1) by inventor G.R. Mohan Rao.

TECHNICAL FIELD

[002] This application relates to a system and method for providing reliable storage through the use of non-volatile memories and, more particularly, to a system and method of increasing the reliability and lifetime of a NAND

flash storage system, module, or chip through the use of a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage without substantially raising the cost of the NAND flash storage system. The memory in a total non-volatile memory system may contain some SRAM (static random-access memory), DRAM (dynamic RAM), RRAM (resistive RAM), PCM (phase change memory), MAGRAM (magnetic random-access memory), NAND flash, and one or more HDDs (hard disk drives) when storage of the order of several terabytes is required. The SLC non-volatile memory can be flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

BACKGROUND OF THE DISCLOSURE

[003] Non-volatile memories provide long-term storage of data. More particularly, non-volatile memories can retain the stored data even when not powered. Magnetic (rotating) hard disk drives (HDD) dominate this storage medium due to lower cost compared to solid state disks (SSD). Optical (rotating) disks, tape drives and others have a smaller role in long-term storage systems. SSDs are preferred for their superior performance (fast access time), mechanical reliability and ruggedness, and portability. Flash memory, more specifically NAND flash, is the dominant SSD medium today.

[004] RRAM, PCM, MAGRAM and others, will likely play a larger role in the future, each of them having their own advantages and disadvantages. They

may ultimately replace flash memories, initially for use as a "write buffer" and later to replace "SLC flash" and "MLC flash." MLC NAND flash is a flash memory technology using multiple levels per cell to allow more bits to be stored using the same number of transistors. In SLC NAND flash technology, each cell can exist in one of two states, storing one bit of information per cell. Most MLC NAND flash memory has four possible states per cell, so it can store two bits of information per cell.

[005] These semiconductor technology driven "flash alternatives," i.e., RRAM, PCM, MAGRAM and others, have several advantages over any (SLC or MLC) flash because they: 1) allow data to be written over existing data (without prior erase of existing data), 2) allow for an erase of individual bytes or pages (instead of having to erase an entire block), and 3) possess superior endurance (1,000,000 write-erase cycles compared to typical 100,000 cycles for SLC flash and less than 10,000 cycles for MLC flash).

[006] HDDs have several platters. Each platter contains 250-5,000 tracks (concentric circles). Each track contains 64 to 256 sectors. Each sector contains 512 bytes of data and has a unique "physical (memory) address." A plurality of sectors is typically combined to form a "logical block" having a unique "logical address." This logical address is the address at which the logical block of physical sectors appears to reside from the perspective of an executing application program. The size of each logical block and its logical address (and/or address ranges/boundaries) is optimized for the particular operating system (OS) and software applications executed by the host processor. A computer OS organizes data as "files." Each file may be located

(stored) in either a single logical block or a plurality of logical blocks, and therefore, the location of files typically traverses the boundaries of individual (physical) sectors. Sometimes, a plurality of files has to be combined and/or modified, which poses an enormous challenge for the memory controller device of a non-volatile memory system.

[007] SSDs are slowly encroaching on the HDD space and the vast majority of NAND flash in enterprise servers utilizes a SLC architecture, which further comprises a NAND flash controller and a flash translation layer (FTL). NAND flash devices are generally fragmented into a number of identically sized blocks, each of which is further segmented into some number of pages. It should be noted that asymmetrical block sizes, as well as page sizes, are also acceptable within a device or a module containing devices. For example, a block may comprise 32 to 64 pages, each of which incorporates 2 - 4 Kbit of memory. In addition, the process of writing data to a NAND flash memory device is complicated by the fact that, during normal operation of, for example, single-level storage (SLC), erased bits (usually all bits in a block with the value of '1') can only be changed to the opposite state (usually '0') once before the entire block must be erased. Blocks can only be erased in their entirety, and, when erased, are usually written to '1' bits. However, if an erased block is already there, and if the addresses (block, page, etc.) are allowed, data can be written immediately; if not, a block has to be erased before it can be written to.

[008] FTL is the driver that works in conjunction with an existing operating system (or, in some embedded applications, as the operating system) to

make linear flash memory appear to the system like a disk drive, i.e., it emulates a HDD. This is achieved by creating "virtual" small blocks of data, or sectors, out of flash's large erase blocks and managing data on the flash so that it appears to be "write in place" when in fact it is being stored in different locations in the flash. FTL further manages the flash so that there are clean/erased places to store data.

[009] Given the limited number of writes that individual blocks within flash devices can tolerate, wear leveling algorithms are used within the flash devices (as firmware commonly known as FTL or managed by a controller) to attempt to ensure that "hot" blocks, i.e., blocks that are frequently written, are not rendered unusable much faster than other blocks. This task is usually performed within a flash translation layer. In most cases, the controller maintains a lookup table to translate the memory array physical block address (PBA) to the logical block address (LBA) used by the host system. The controller's wear-leveling algorithm determines which physical block to use each time data is programmed, eliminating the relevance of the physical location of data and enabling data to be stored anywhere within the memory array and thus prolonging the service life of the flash memory. Depending on the wear-leveling method used, the controller typically either writes to the available erased block with the lowest erase count (dynamic wear leveling); or it selects an available target block with the lowest overall erase count, erases the block if necessary, writes new data to the block, and ensures that blocks of static data are moved when their block erase count is below a certain threshold (static wear leveling).

[0010] MLC NAND flash SSDs are slowly replacing and/or coexisting with SLC NAND flash in newer SSD systems. MLC allows a single cell to store multiple bits, and accordingly, to assume more than two values; i.e., '0' or '1'. Most MLC NAND flash architectures allow up to four (4) values per cell; i.e., '00', '01', '10', or '11'. Generally, MLC NAND flash enjoys greater density than SLC NAND flash, at the cost of a decrease in access speed and lifetime (endurance). It should be noted, however, that even SLC NAND flash has a considerably lower lifetime (endurance) than rotating magnetic media (e.g., HDDs), being able to withstand only between 50,000 and 100,000 writes, and MLC NAND flash has a much lower lifetime (endurance) than SLC NAND flash, being able to withstand only between 3,000 and 10,000 writes. As is well known in the art, any "write" or "program" to a block in NAND flash (floating gate) requires an "erase" (of a block) before "write."

[0011] Despite its limitations, there are a number of applications that lend themselves to the use of MLC flash. Generally, MLC flash is used in applications where data is read many times (but written few times) and physical size is an issue. For example, flash memory cards for use in digital cameras would be a good application of MLC flash, as MLC can provide higher density memory at lower cost than SLC memory.

[0012] When a non-volatile storage system combines HDD, SLC and MLC (setting aside volatile memory for buffering, caching etc) in a single (hybrid) system, new improvements and solutions are required to manage the methods of writing data optimally for improved life time (endurance) of flash memory. Accordingly, various embodiments of a NAND flash storage system

that provides long lifetime (endurance) storage at low cost are described herein.

[0013] The following description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present disclosure is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

SUMMARY OF THE DISCLOSURE

[0014] According to one embodiment of the present disclosure, there is provided a system for storing data which comprises at least one MLC non-volatile memory module (hereinafter referred to as "MLC module") and at least one SLC non-volatile memory module (hereinafter referred to as "SLC module"), each module comprises a plurality of individually erasable blocks. The data storage system according to one embodiment of the present disclosure further comprises a controller for controlling both the at least one MLC module and the at least one SLC module. In particular, the controller maintains an address map comprising a list of individual logical address ranges each of which maps to a similar range of physical addresses within either the at least one MLC module or the at least one SLC module. After each write to (flash) memory, the controller conducts a data integrity check

to ensure that the data was written correctly. When the data was not written correctly, the controller modifies the table so that the range of addresses on which the write failed is remapped to the next available range of physical addresses within the at least one SLC module. The SLC module can be (NAND) flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

[0015] According to another embodiment of the present disclosure, there is provided a system for storing data which comprises a controller that is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC non-volatile module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The present disclosure will be more fully understood by reference to the following detailed description of one or more preferred embodiments when read in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout the views and in which:

[0017] FIG. 1 is a block diagram of a computer system incorporating one embodiment of the present disclosure;

[0018] FIG. 2 is a drawing depicting a translation table/address map in accordance with one embodiment of the present disclosure;

[0019] FIGS. 3a and 3b are a flow chart illustrating an exemplary method for use in implementing one embodiment of the present disclosure; and

[0020] FIG. 4 is a block diagram depicting one embodiment of the present disclosure for implementation within a NAND flash module.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

[0021] The present disclosure is directed to the reliable storage of data in read and write memory, and, in particular, to the reliable storage of data in non-volatile memory, such as, for example, NAND flash. Generally, and in particular regard to NAND flash memory, two separate banks of NAND flash are maintained by a controller. One bank contains economical MLC NAND flash, while a second bank contains high endurance SLC NAND flash. The controller conducts a data integrity test after every write. If a particular address range fails a data integrity test, the address range is remapped from MLC NAND flash to SLC NAND flash. As the SLC NAND flash is used to boost the lifetime (endurance) of the storage system, it can be considerably lesser in amount than the MLC NAND flash. For example, a system may set SLC NAND flash equal to 12.5% or 25% of MLC NAND flash (total non-volatile memory storage space = MLC + SLC).

[0022] Turning to the Figures and to Figure 1 in particular, a computer system 10 depicting one embodiment of the present disclosure is shown. A processor 12 is coupled to a device controller 14, such as a chipset, using a

data link well known in the art, such as a parallel bus or packet-based link. The device controller 14 provides interface functions to the processor 12. In some computer systems, the device controller 14 may be an integral part of the (host) processor 12. The device controller 14 provides a number of input/output ports 16 and 18, such as, for example, serial ports (e.g., USB ports and Firewire ports) and network ports (e.g., Ethernet ports and 802.11 "Wi-Fi" ports). The device controller 14 may also control a bank of, for example, DRAM 20. In addition, the device controller 14 controls access to one or more disks 24, such as, for example, a rotating magnetic disk, or an optical disk, as well as two or more types of NAND flash memory. One type of NAND flash memory is a MLC NAND flash memory module 26. Another type of NAND flash memory is a SLC NAND flash memory module 28.

[0023] The device controller 14 maintains a translation table/address map which may include address translations for all devices in the computer system. Nonetheless, the discussion in the present disclosure will be limited only to NAND flash memory modules. In particular, the device controller 14 maintains a translation table that maps logical computer system addresses to physical addresses in each one of the MLC- and SLC- NAND flash memory modules 26 and 28, respectively. As MLC flash memory is less expensive than SLC flash memory, on a cost per bit basis, the translation table will initially map all logical NAND flash addresses to the MLC NAND flash memory module 26. The address ranges within the translation table will assume some minimum quantum, such as, for example, one block, although

a smaller size, such as one page could be used, if the NAND flash has the capability of erasing the smaller size quantum.

[0024] A "read-modify-write" scheme is used to write data to the NAND flash. Data to be written to NAND flash is maintained in DRAM 20. After each write to an address within a particular address range, the device controller 14 will – as time permits – perform a read on the address range to ensure the integrity of the written data. If a data integrity test fails, the address range is remapped from the MLC NAND flash memory module 26 to the next available address range in the SLC NAND flash memory module 28.

[0025] Figure 2 illustrates one embodiment of a translation table/address map of the present disclosure. In Figure 2a, a list of logical address ranges (R0-RN) is translated to physical address ranges. As illustrated, all of the logical address ranges are translated to blocks on the MLC NAND flash memory module 26. However, through the application of a data integrity verification check (explained in more detail below) it is determined that, for example, address range R2 corresponds to failed quanta of data stored in block 2 of the MLC NAND flash memory module 26. Figure 2b shows the quanta of data which failed the data integrity verification check (see Figure 2a) remapped to the next available range of physical addresses within the SLC NAND flash memory module 28, in this example, SLC/block 0.

[0026] Figures 3a and 3b are a flow chart illustrating a method for utilizing a NAND flash memory system incorporating one embodiment of the present disclosure. The method begins in a step 100, when a command to write a quantum of data stored in DRAM to a particular location in NAND flash

memory is received. In step 102, the quantum of data is read from DRAM into memory within the device controller (which acts as the memory controller). In step 104, both the logical address range and the NAND flash physical address range to which the quantum of data is to be written, is read into memory of the device controller. In step 106, the quantum of data to be written is combined with the contents of the NAND flash memory. In step 108, the NAND flash physical address range to be written is erased. In step 110, the combined data is written to the appropriate NAND flash physical address range. In step 112 the NAND flash physical address range that was written in step 110 is read into device controller memory.

[0027] The flowchart continues in Figure 3b. In step 114 the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical address range and the quantum of data to be written. In step 116, if the retained data matches the newly stored data in the NAND flash memory, the write was a success, and the method exits in step 118. However, if the retained data does not match the newly stored data in the NAND flash memory, the method executes step 120, which identifies the next quantum of available SLC NAND flash memory addresses. In step 122, a check is made to determine if additional SLC NAND flash memory is available, and, if not, the NAND flash memory system is marked as failed, prompting a system alert step 124. However, if additional SLC NAND flash memory is available, the failed NAND flash physical address range is remapped to the next available quantum of SLC NAND flash

memory in step 126. Execution then returns to step 110, where the write is repeated.

[0028] Another application of one embodiment of the present disclosure, not depicted in any of the drawings, is to allocate "hot" blocks; i.e., those blocks that receive frequent writes, into the SLC NAND flash memory module 28, while allocating "cold" blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26. This could be accomplished within the device controller 14 described above, which could simply maintain a count of those blocks that are accessed (written to) most frequently, and, on a periodic basis, such as, for example, every 1000 writes, or every 10,000 writes, transfer the contents of those blocks into the SLC NAND flash memory module 28.

[0029] Figure 4 depicts another embodiment of the present disclosure. The embodiment is entirely resident within a NAND flash module 50. In particular, a standard NAND flash interface 52 is managed by flash translation layer (FTL) logic 54. The flash translation layer (FTL) 54 manages two NAND flash memory banks 56 and 58, whereby memory bank 56 comprises a plurality of MLC NAND flash memory modules 60a and a plurality of SLC NAND flash memory modules 62a. Memory bank 58 comprises a plurality of MLC NAND flash memory modules 60b and a plurality of SLC NAND flash memory modules 62b.

[0030] This embodiment of the present disclosure could function similarly to the system level embodiment discussed earlier with reference to Figures 1 - 3b, but the control functions, such as maintenance of the translation

table/address map (Figure 2), could be conducted within the flash translation layer (FTL) 54 instead of in a device controller 14.

[0031] Embodiments of the present disclosure relate to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of multi-level cell (MLC) and single-level cell (SLC) NAND flash storage. The above description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. While this disclosure contains descriptions with reference to certain illustrative aspects, it will be understood that these descriptions shall not be construed in a limiting sense. Rather, various changes and modifications can be made to the illustrative embodiments without departing from the true spirit, central characteristics and scope of the disclosure, including those combinations of features that are individually disclosed or claimed herein. Furthermore, it will be appreciated that any such changes and modifications will be recognized by those skilled in the art as an equivalent to one or more elements of the following claims, and shall be covered by such claims to the fullest extent permitted by law.

Claims

What is claimed is:

1. A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module; and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module.

2. The system of claim 1, wherein the minimal quanta of addresses is equal to one block.

3. The system of claim 1, wherein the minimal quanta of addresses is equal to one page.

4. The system of claim 1, wherein the MLC non-volatile memory module is NAND flash memory.

5. The system of claim 1, wherein the SLC non-volatile memory module is NAND flash memory.

6. The system of claim 1, wherein the MLC non-volatile memory module is resistive random-access memory (RRAM).

7. The system of claim 1, wherein the SLC non-volatile memory module is resistive random-access memory (RRAM).

8. The system of claim 1, wherein the MLC non-volatile memory module is phase change memory (PCM).

9. The system of claim 1, wherein the SLC non-volatile memory module is phase change memory (PCM).

10. The system of claim 1, wherein the SLC non-volatile memory module is magnetic random-access memory (MAGRAM).

11. The system of claim 1, wherein the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller allocates those blocks that receive the most frequent writes to the at least one SLC non-volatile memory module.

12. The system of claim 11, wherein the controller determines which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of said blocks is accessed.

13. The system of claim 12, wherein the controller allocates those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

14. The system of claim 13, wherein the controller causes the transfer of content on a periodic basis.

ABSTRACT

[0032] A flash controller for managing at least one MLC non-volatile memory module and at least one SLC non-volatile memory module. The flash controller is adapted to determine if a range of addresses listed by an entry and mapped to said at least one MLC non-volatile memory module fails a data integrity test. In the event of such a failure, the controller remaps said entry to an equivalent range of addresses of said at least one SLC non-volatile memory module. The flash controller is further adapted to determine which of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and allocating those blocks that receive frequent writes to the SLC non-volatile memory module and those blocks that receive infrequent writes to the MLC non-volatile memory module.

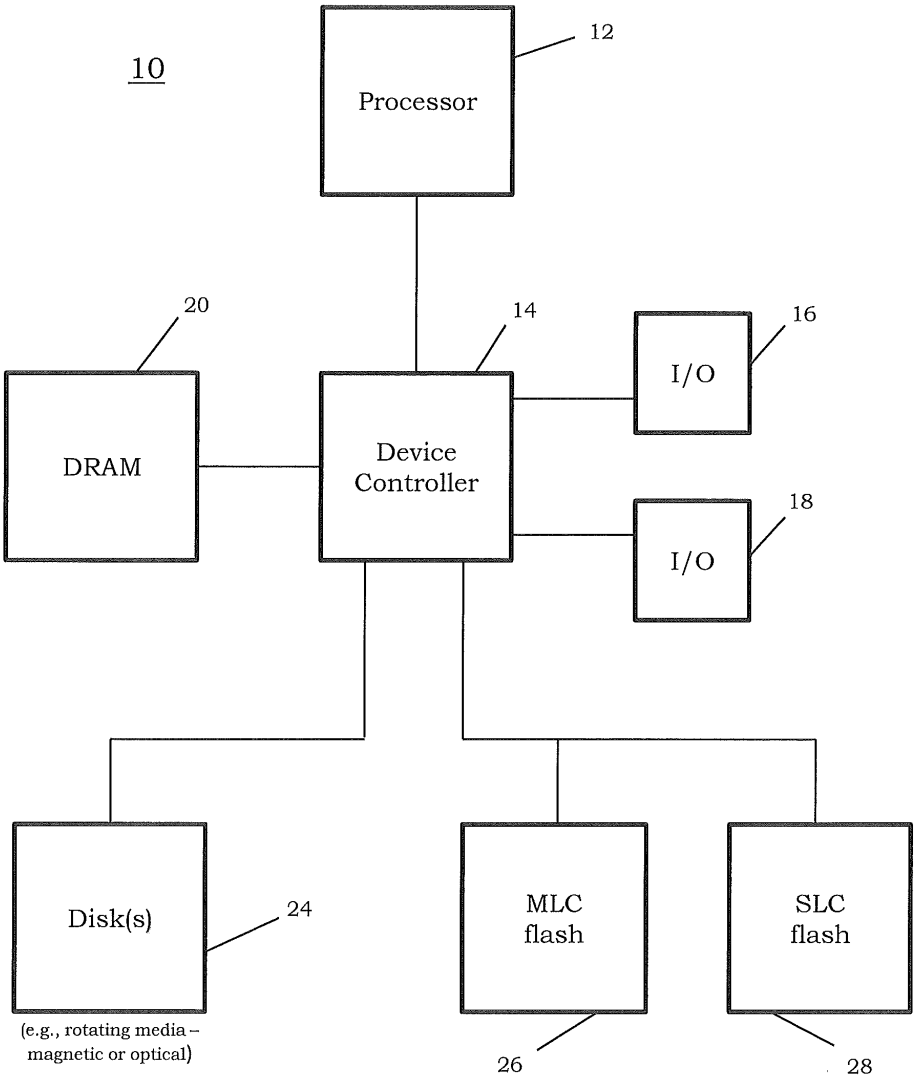

10
Processor
12
20
14
16
DRAM
Device Controller
I/O
18
I/O
Disk(s)
24
(e.g., rotating media – magnetic or optical)
MLC flash
SLC flash
26
28

FIG. 1

Failed Data Integrity Test

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	MLC/Block 2
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

FIG. 2a

Remapping to SLC flash module

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	SLC/Block 0
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

FIG. 2b

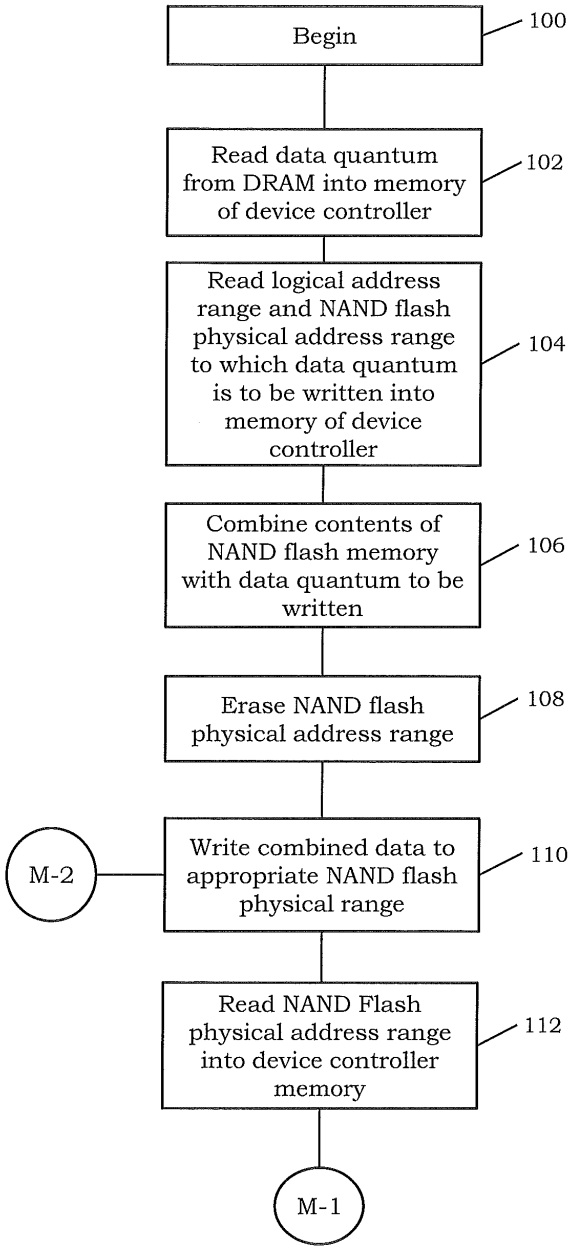

Begin
100
Read data quantum from DRAM into memory of device controller
102
Read logical address range and NAND flash physical address range to which data quantum is to be written into memory of device controller
104
Combine contents of NAND flash memory with data quantum to be written
106
Erase NAND flash physical address range
108
M-2
Write combined data to appropriate NAND flash physical range
110
Read NAND Flash physical address range into device controller memory
112
M-1

FIG. 3a

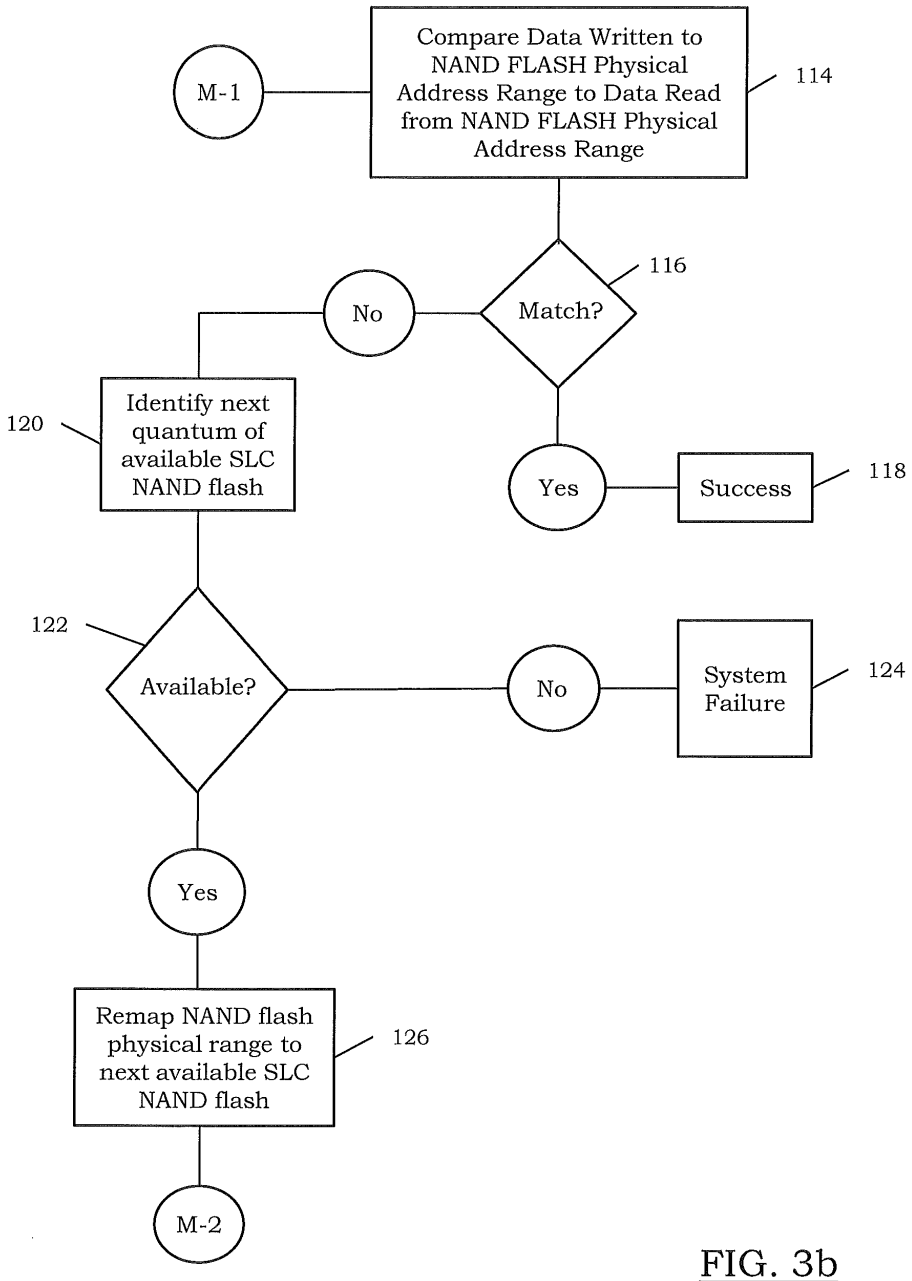
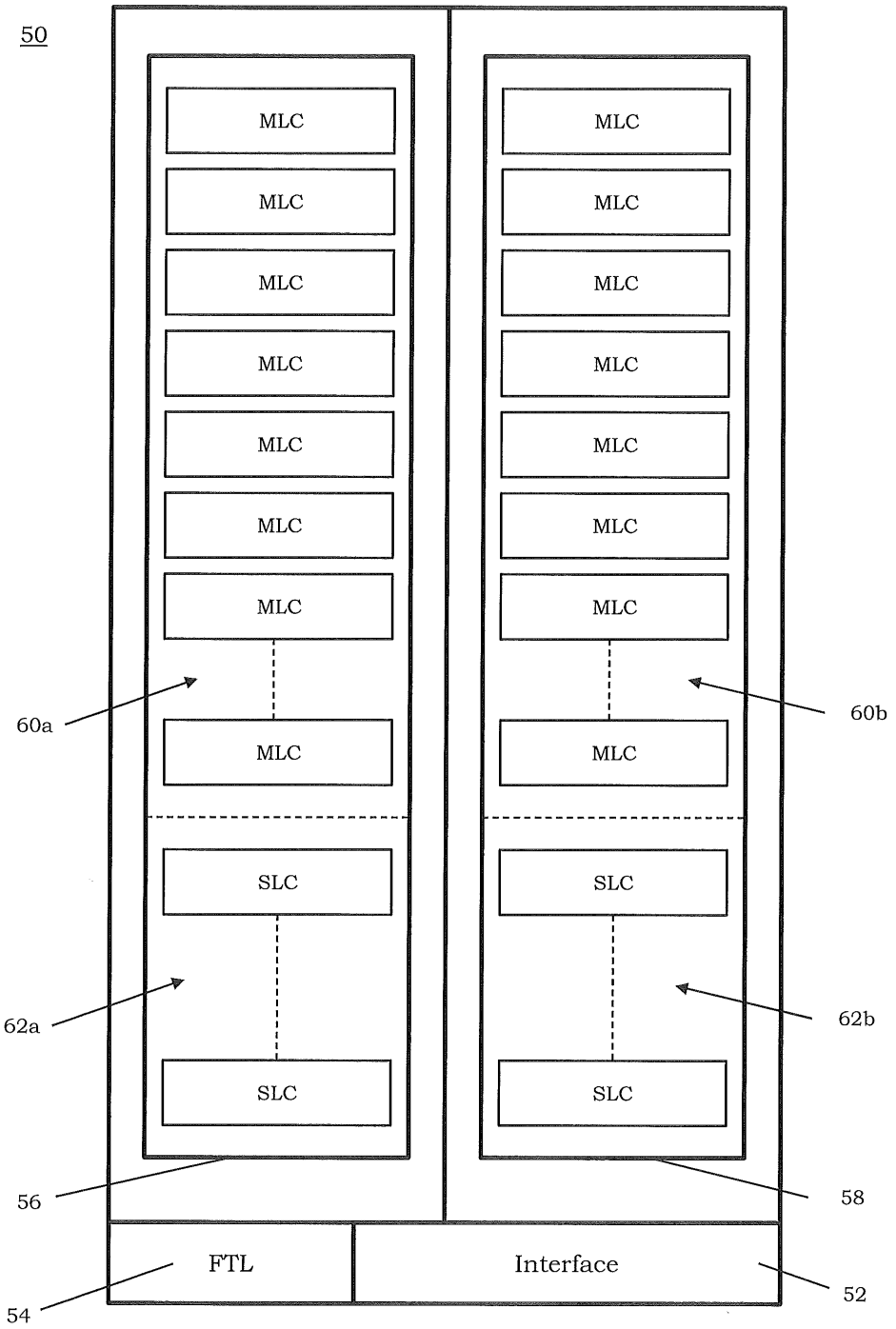

M-1
Compare Data Written to NAND FLASH Physical Address Range to Data Read from NAND FLASH Physical Address Range
114
Match?
116
No
Yes
Success
118
Identify next quantum of available SLC NAND flash
120
Available?
122
No
System Failure
124
Yes
Remap NAND flash physical range to next available SLC NAND flash
126
M-2

FIG. 3b


50
MLC
MLC
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MLC
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MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
MLC
60a
60b
SLC
SLC
SLC
SLC
62a
62b
56
58
FTL
Interface
54
52

FIG. 4

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13455267
	Filing Date	
	First Named Inventor	G. R. Mohan Rao
	Art Unit	
	Examiner Name	
	Attorney Docket Number	0299-0004.01

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7855916		2010-12-21	G. R. Mohan Rao	

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U.S.PATENT APPLICATION PUBLICATIONS

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	1	20110060870	A1	2011-03-10	G. R. Mohan Rao	

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	1	QINGSONG WEI et al., WAFTL: A Workload Adaptive Flash Translation Layer with Data Partition, IEEE 27th Symposium on Massive Storage Systems and Technologies (MSST), May 23-27, 2011	☐
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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/David M. Mundt/	Date (YYYY-MM-DD)	2012-04-25
Name/Print	David M. Mundt	Registration Number	41,207

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	39	Tae-Sun Chung et al., A Survey of Flash Translation Layer, Journal of Systems Architecture 55, pp332-343, 2009	☐
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/455,267	04/25/2012	G. R. Mohan Rao	0299-0004.01	6684

70653 7590 06/17/2014
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REIDLINGER, RONALD LANCE

ART UNIT	PAPER NUMBER
2824	

MAIL DATE	DELIVERY MODE
06/17/2014	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 13/455,267	Applicant(s) RAO, G. R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	AIA (First Inventor to File) Status No

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A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

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Status

1)☒ Responsive to communication(s) filed on *25 April 2012*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-14* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-12* is/are rejected.

8)☒ Claim(s) *13 and 14* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☒ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *25 April 2012* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

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3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

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1) ☒ Notice of References Cited (PTO-892)

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3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Continuation of Attachment(s) 2). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :4/25/2012, 4/25/2012 & 4/25/2012.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

2. Claims 1-14 are currently pending.

3. Claim 1 is independent.

Claim Objections

4. Claims 2 and 3 are objected to because of the following informalities:

"A minimal quanta of addresses" used in claims 2 and 3 lacks antecedent basis. Either "a minimum quanta of addresses" should be replaced with "a ~~minimum~~ minimal quanta of addresses" in claim 1, or "a minimal quanta of addresses" should be replaced with "a ~~minimal~~ minimum quanta of addresses" in claims 2 and 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

6. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 1-5 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Gorobets et al. (U.S. Patent Application Publication No. 2010/0172179).**

Regarding claim 1, Gorobets et al. teach,

A system for storing data (e.g. Fig. 20) comprising:

at least one MLC non-volatile memory module (Fig. 20 Main Portion MLC No. 2003) comprising a plurality of individually erasable blocks (this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one SLC non-volatile memory module (Fig. 20 Binary Portion No. 2001) comprising a plurality of individually erasable blocks (again, this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]); and

a controller (Fig. 8 Memory Manager No. 300) coupled to the (Flash Memory No. 200) at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module (See Fig. 20), the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules (maps logical addresses to physical addresses, see ¶ [0096]), the address map comprising a list of logical address ranges (e.g. a block) accessible by a computer system (logical addresses), the list of logical address ranges having a minimum quanta of addresses (the mimimum quantity of addresses is different depending on the operation, for an erase, a block is the minimum erase unit and a page is the minimum programming unit, see ¶ [0017]), wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or

within the at least one MLC non-volatile memory module (maps logical addresses to physical addresses, see ¶ [0096]); and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses (Fig. 20 block 2018) within the at least one MLC non-volatile memory module (Main Portion (MLC) No. 2003), fails a data integrity test (e.g. failure programming only the upper page, but still usable as binary, see ¶ [0165]), and, in the event of such a failure, the controller remaps (No. 2017) the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module (remapped to the spare binary block, see ¶ [0165]).

Regarding claim 2, Gorobets et al. teach,

The system of claim 1, wherein the minimal quanta of addresses is equal to one block (for an erase operation, a block is the minimum erase unit, see ¶ [0017]).

Regarding claim 3, Gorobets et al. teach,

The system of claim 1, wherein the minimal quanta of addresses is equal to one page (for a program operation, a page is the minimum programming unit, see ¶ [0017]).

Regarding claims 4 and 5, Gorobets et al. teach that the entire device (i.e. both SLC and MLC) is NAND flash memory. See e.g. Fig. 5 or ¶ [0010].

Claim Rejections - 35 USC § 103

8. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been

> obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. **Claims 6-9 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of De Ambroggi et al. (U.S. Patent Application Publication No. 2009/0268513) and Kund et al. (U.S. Patent Application Publication No. 2010/0058018).**

Regarding claims 6-9, Gorobets et al. fail to teach that the memory could be anything other than flash EEPROM or other types of charge trapping memory see e.g. ¶ [0010] describing the various types of memory.

De Ambroggi et al. teach that one type of resistive memory (RRAM), Phase Change (PCRAM or PCM) can be configured to be partially SLC and partially MLC.

Kund et al. teach generally that "Emerging memory technologies such as resistive memory (e.g., resistive random access memories such as phase change random access memory (PCRAM), conductive bridge random access memory

(CBRAM), and magnetic random access memory (MRAM)) offer certain advantages over DRAM, Flash and other conventional types of memory devices in terms of switching speeds, size, power consumption, and non-volatility." ¶ [0016].

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the flash EEPROM taught by Gorobets et al. with the PCM taught by De Ambroggi et al. in view of the PCM advantages over flash EEPROM taught by Kund et al.

11. **Claim 10 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of Chen et al. (U.S. Patent Application Publication No. 2009/0307418) and Kund et al.**

Regarding claim 10, Gorobets et al. fail to teach that the memory could be anything other than flash EEPROM or other types of charge trapping memory see e.g. ¶ [0010] describing the various types of memory.

Chen et al. teach that MRAM could be used as SLC in conjunction with some other memory type being used as MLC to create a hybrid density memory. See e.g. ¶ [0031].

Kund et al. teach generally that "Emerging memory technologies such as resistive memory (e.g., resistive random access memories such as phase change random access memory (PCRAM), conductive bridge random access memory (CBRAM), and magnetic random access memory (MRAM)) offer certain advantages over DRAM, Flash and other conventional types of memory devices in terms of switching speeds, size, power consumption, and non-volatility." ¶ [0016].

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the SLC flash EEPROM taught by Gorobets et al. with the SLC MRAM in view of the MRAM advantages over flash EEPROM taught by Kund et al.

12. **Claims 11 and 12 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of Segal et al. (U.S. Patent Application Publication No. 2011/0271043).**

Regarding claim 11, Gorobets et al. teach, that for wear leveling the system may exchange hot (heavily used) blocks with cold (little used) blocks or spare blocks using a hot count. See ¶ [0172]. Gorobets et al. fail to teach that the exchange would be for SLC portions. Albeit, this would likely happen over the course of normal operation as the MLC with the highest counts are most likely to have programming failure and be allocated to SLC. See ¶ [0165]. Additionally Gorobets et al. teach that areas such as a cache area which will have a higher hot count should be in the binary (SLC) area. See ¶ [0164].

Segal et al. teach that MLC spare blocks can be reallocated to SLC spare blocks in response to a determination that the MLC blocks have exceeded the P/E cycle rating. See ¶¶ [0040 & 0049]. This would ensure that the blocks that are accessed most frequently (the blocks with the highest P/E cycle counts) would be allocated as SLC.

This has a clear advantage over the method taught by Gorobets et al. in that the MLC blocks with the highest P/E cycle counts are allocated to SLC prior to failing in which it may be too late.

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to allocate the MLC blocks with the highest hot counts to the SLC to maximize the life of the memory.

Regarding claim 12, both Gorobets et al. and Segal et al. teach that the controller determines which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of said blocks is accessed (See Gorobets et al. hot counts ¶¶ [0164 and 0172-174] and Segal et al. P/E cycle count ¶¶ [0040 & 0049].

Allowable Subject Matter

13. Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach that the controller allocates those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R LANCE REIDLINGER whose telephone number is (571)270-7353. The examiner can normally be reached on 11:30am - 9:00pm Mon-Thur and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571)272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R LANCE REIDLINGER/
Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 13/455,267	Applicant(s)/Patent Under Reexamination RAO, G. R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	Page 1 of 1

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*	C	US-2010/0058018	03-2010	Kund et al.	711/167
*	D	US-2009/0307418	12-2009	Chen et al.	711/105
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	F	US-			
	G	US-			
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	I	US-			
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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13455267
	Filing Date	
	First Named Inventor	G. R. Mohan Rao
	Art Unit	
	Examiner Name	
	Attorney Docket Number	0299-0004.01

U.S.PATENTS

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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1:56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/David M. Mundt/	Date (YYYY-MM-DD)	2012-04-25
Name/Print	David M. Mundt	Registration Number	41,207

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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	Attorney Docket Number	0299-0004.01

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/David M. Mundt/	Date (YYYY-MM-DD)	2012-04-25
Name/Print	David M. Mundt	Registration Number	41,207

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.L.R

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"20090307418".pn.	US-PGPUB; USPAT	OR	ON	2014/06/14 00:30
L2	5281	365/185.03,185.09.ccls.	US-PGPUB; USPAT	OR	ON	2014/06/14 01:15
S1	1	13/455267.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:05
S2	2	12/567771.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:07
S3	5314	SLC! and MLC!	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:09
S4	3345	S3 and address and page	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:10
S5	904	S4 and test$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:10
S6	662	S5 and (map mapped mapping re$1map$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:11
S7	177	S4 and test$3 with fail$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:11
S8	143	S7 and (map mapped mapping re$1map$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2014/06/13 13:11

			DERWENT; IBM_TDB			
S9	1915	SLC! same test$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:13
S10	1160	MLC! same test$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:14
S11	46	S9 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:14
S12	1	13/096736.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:42
S13	2	"20100172179".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:43
S15	2	12/348825.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:14
S16	6	(("5671128") or ("6948026") or ("20030110343") or ("20030123301") or ("20050144516") or ("20090187798")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/06/13 14:17
S17	3	S16 and count	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:17
S18	0	"20110860870".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:25
S19	5	"2011060870".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2014/06/13 14:25

			IBM_TDB			
S20	3	"20110060870".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:25
S21	7	(US-20090268513-$ or US-20090327590-$ or US-20110271043-$ or US-20100172179-$).did. or (US-8379460-$ or US-8417988-$ or US-8422303-$).did.	US-PGPUB; USPAT	OR	ON	2014/06/13 14:34
S22	5	S21 and count	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:34
S23	10982	address with block with page	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 15:07
S24	2	S23 and S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 15:07
S25	1	S21 and MRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 15:29
S26	61	MRAM with MLC	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 15:30
S27	7	advantages with MRAM with PCRAM with (flash eeprom)	US-PGPUB; USPAT	OR	ON	2014/06/13 16:16
S28	118	(("G R Mohan") near2 (Rao)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/06/13 16:48
S29	5196	SLC and MLC	US-PGPUB; USPAT	OR	ON	2014/06/13 16:49
S30	8	S3 and S28	US-PGPUB; USPAT	OR	ON	2014/06/13 16:49
S31	205	gorobets near2 sergey.in.	US-PGPUB; USPAT	OR	ON	2014/06/13 16:59
S32	245	wear adj leveling.ti.	US-PGPUB; USPAT	OR	ON	2014/06/13 16:59
S33	4	S31 and S32	US-PGPUB; USPAT	OR	ON	2014/06/13 17:00
S34	84	flag same slc same MLC	US-PGPUB;	OR	ON	2014/06/13

			USPAT			19:54
S35	1	"20060171210".pn.	US-PGPUB; USPAT	OR	ON	2014/06/13 19:56
S36	2	flag same Tlc same MLC	US-PGPUB; USPAT	OR	ON	2014/06/13 19:59
S37	411	flag same ((three triple tri!) adj (level state bit) TLC) same (MLC DLC BLC (double two bi) adj (level state bit))	US-PGPUB; USPAT	OR	ON	2014/06/13 20:03
S38	403	flag same ((three triple tri!) adj (level state bit) TLC) same ((double two bi) adj (level state bit))	US-PGPUB; USPAT	OR	ON	2014/06/13 20:04
S39	176601	"365".clas. "711".clas.	US-PGPUB; USPAT	OR	ON	2014/06/13 20:04
S40	90	S37 and S39	US-PGPUB; USPAT	OR	ON	2014/06/13 20:04

EAST Search History (Interference)

<This search history is empty>

6/14/2014 1:16:35 AM
C:\Users\rreidlinger\Documents\EAST\Workspaces\13455267.wsp

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BIB DATA SHEET

CONFIRMATION NO. 6684

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/455,267	04/25/2012 RULE	365	2824	0299-0004.01

APPLICANTS

INVENTORS

G. R. Mohan Rao, Richardson, TX;

**** CONTINUING DATA ****************************

This appln claims benefit of 61/509,257 07/19/2011

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **

05/04/2012

Foreign Priority claimed	❑ Yes ☑ No		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	❑ Yes ☑ No	❑ Met after Allowance	TX	5	14	1
Verified and Acknowledged	/R LANCE REIDLINGER/ Examiner's Signature	Initials				

ADDRESS

LAW OFFICES OF EUGENE M. CUMMINGS, P.C.
ONE NORTH WACKER DRIVE
SUITE 4130
CHICAGO, IL 60606
UNITED STATES

TITLE

LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

FILING FEE RECEIVED		
530	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13455267	RAO, G. R. MOHAN
	Examiner	**Art Unit**
	LANCE REIDLINGER	2824

CPC- SEARCHED		
Symbol	**Date**	**Examiner**

CPC COMBINATION SETS - SEARCHED		
Symbol	**Date**	**Examiner**

US CLASSIFICATION SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
365	185.03, 185.09	6/14/2014	RLR

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
Inventor Search Conducted in EAST	6/13/2014	RLR
See EAST Search history	6/14/2014	RLR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**

/LANCE REIDLINGER/ Examiner.Art Unit 2824	

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13455267
	Filing Date	
	First Named Inventor	G. R. Mohan Rao
	Art Unit	
	Examiner Name	
	Attorney Docket Number	0299-0004.01

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.L.R

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13455267
	Filing Date	
	First Named Inventor	G. R. Mohan Rao
	Art Unit	
	Examiner Name	
	Attorney Docket Number	0299-0004.01

	37	ROBERTO BEZ et al., Introduction to Flash Memory, Proceedings of the IEEE, Vol. 91, No. 4, April 2003	☐
	38	SEAGATE TECHNOLOGY LLC, The Transition to Advanced Format 4K Sector Hard Drives, April 2010	☐
	39	Tae-Sun Chung et al., A Survey of Flash Translation Layer, Journal of Systems Architecture 55, pp332-343, 2009	☐
	40	INTEL, Understanding the Flash Translation Layer (FTL) Specification, December 1998	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/R Lance Reidlinger/	Date Considered	06/14/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.L.R

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13455267
	Filing Date	
	First Named Inventor	G. R. Mohan Rao
	Art Unit	
	Examiner Name	
	Attorney Docket Number	0299-0004.01

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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OR

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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Signature	/David M. Mundt/	Date (YYYY-MM-DD)	2012-04-25
Name/Print	David M. Mundt	Registration Number	41,207

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EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.L.R

Patent Application
Attorney Docket No.: 0299-0004.01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	13/455,267
Confirmation No.	:	6684
Inventor	:	G. R. Mohan Rao
Filed	:	04/25/2012
TC/A.U.	:	2824
Examiner	:	Reidlinger, Ronald L.
Title	:	IMPROVED LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM
Docket No.	:	0299-0004.01

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this filing; and

Remarks begin on page 5 of this filing.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (amended) A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module [[,]] ; wherein the controller is adapted to:

a) ~~maintaining~~ maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module; ~~and wherein the controller is adapted to~~

b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and

d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

2. (amended) The system of claim 1, wherein the ~~minimal~~ minimum quanta of addresses is equal to one block.

3. (amended) The system of claim 1, wherein the ~~minimal~~ minimum quanta of addresses is equal to one page.

4. (previously presented) The system of claim 1, wherein the MLC non-volatile memory module is NAND flash memory.

5. (previously presented) The system of claim 1, wherein the SLC non-volatile

memory module is NAND flash memory.

6. (previously presented) The system of claim 1, wherein the MLC non-volatile memory module is resistive random -access memory (RRAM).

7. (previously presented) The system of claim 1, wherein the SLC non-volatile memory module is resistive random-access memory (RRAM).

8. (previously presented) The system of claim 1, wherein the MLC non-volatile memory module is phase change memory (PCM).

9. (previously presented) The system of claim 1, wherein the SLC non-volatile memory module is phase change memory (PCM).

10.(previously presented) The system of claim 1, wherein the SLC non-volatile memory module is magnetic random-access memory (MAGRAM).

11. - 13. (canceled).

14.(amended) The system of claim ~~13~~ 1, wherein the controller causes the transfer of content on a periodic basis.

REMARKS

Applicant has carefully reviewed and considered the Office Action of June 17, 2014. In response to the Office Action, Applicant makes the following remarks:

Claim Status

Applicant has canceled dependent claims 11, 12 and 13. Independent claim 1 and dependent claims 2, 3 and 14 have been amended.

Allowable Subject Matter and Claim Amendments

Dependent claims 13 and 14 stand objected to as being dependent upon rejected base claim 1, but have been indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. Applicant has amended independent claim 1 to incorporate the allowable subject matter of claim 13 as well as the subject matter contained in intervening claims 11 and 12. Applicant has done so in order to expedite prosecution of this application and prepare it for issuance and without any concession or acquiescence in the rejections of the base claim(s). Applicant reserves all the right to pursue additional claims, including broader claims, supported by Applicant's specification in continuation applications.

In addition, Applicant has amended dependent claims 2 and 3 to refer to "a minimum quanta of addresses" consisted with the language of claim 1 and in Applicant's specification. Finally, because claim 13 has been canceled, Applicant has amended claim 14 to be dependent on claim 1.

CONCLUSION

Applicant respectfully submits that this application is now in condition for allowance. However, should Examiner be of the opinion that further amendment or response is required, Applicant encourages Examiner to contact the undersigned attorney at the telephone number set forth below. The Commissioner is authorized to charge fees or deficiencies or credit any overpayments to Eugene M. Cummings, P.C., Deposit Account No. **50-4199**, with reference to attorney docket number (0299-0004.01).

Respectfully submitted,

By: /David M. Mundt/

Eugene M. Cummings, Reg. No. 41,207
Law Offices of Eugene M. Cummings, P.C.
55 W Monroe St., Suite 3500
Chicago, Illinois 60603
Telephone: (312) 984-0144
Facsimile: (312) 984-0146

Electronic Acknowledgement Receipt	
EFS ID:	19899115
Application Number:	13455267
International Application Number:	
Confirmation Number:	6684
Title of Invention:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM
First Named Inventor/Applicant Name:	G. R. Mohan Rao
Customer Number:	70653
Filer:	David Michael Mundt
Filer Authorized By:	
Attorney Docket Number:	0299-0004.01
Receipt Date:	19-AUG-2014
Filing Date:	25-APR-2012
Time Stamp:	11:11:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment Copy Claims/Response to Suggested Claims	Amendment.pdf	191241 7a32bb92dfbad2d85db0d7cf548480b493a2e1db	no	6

Warnings:

Information:

Total Files Size (in bytes):	191241

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/455,267	Filing Date 04/25/2012	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	08/19/2014	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 11	Minus	** 20	=	X $ =	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/KATRINA . TURNER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

70653 7590 09/02/2014
EUGENE M. CUMMINGS, P.C.
55 W. MONROE
SUITE 3500
CHICAGO, IL 60603

EXAMINER
REIDLINGER, RONALD LANCE

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/02/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/455,267	04/25/2012	G. R. Mohan Rao	0299-0004.01	6684

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	12/02/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

70653 7590 09/02/2014
EUGENE M. CUMMINGS, P.C.
55 W. MONROE
SUITE 3500
CHICAGO, IL 60603

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/455,267	04/25/2012	G. R. Mohan Rao	0299-0004.01	6684

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	12/02/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
REIDLINGER, RONALD LANCE	2824	365-185030

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/455,267	04/25/2012	G. R. Mohan Rao	0299-0004.01	6684

70653 7590 09/02/2014
EUGENE M. CUMMINGS, P.C.
55 W. MONROE
SUITE 3500
CHICAGO, IL 60603

EXAMINER
REIDLINGER, RONALD LANCE

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/02/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/455,267	Applicant(s) RAO, G. R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *communication(s) submitted 19 August 2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-10 and 14*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HARRY W BYRNE/ Primary Examiner, Art Unit 2824	/R. L. R./ Examiner, Art Unit 2824

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

2. Claims 1-10 and 14 are pending.

3. Claim 1 is independent.

Allowable Subject Matter

4. Claims 1-10 and 14 are allowed.

5. The following is an examiner's statement of reasons for allowance:

The prior art of record fails to teach that the controller allocates those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

DETAILED ACTION

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R LANCE REIDLINGER whose telephone number is (571)270-7353. The examiner can normally be reached on 11:30am - 9:00pm Mon-Thur and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571)272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R. L. R./
Examiner, Art Unit 2824

/HARRY W BYRNE/
Primary Examiner, Art Unit 2824

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13455267	RAO, G. R. MOHAN
	Examiner	**Art Unit**
	LANCE REIDLINGER	2824

CPC						
Symbol					**Type**	**Version**
G11C		16	/	3495	F	2013-01-01
G06F		12	/	0246	I	2013-01-01
G06F		2212	/	7202	A	2013-01-01
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CPC Combination Sets							
Symbol				**Type**	**Set**	**Ranking**	**Version**
			/				
			/				

/LANCE REIDLINGER/ Examiner.Art Unit 2824 (Assistant Examiner)	08/25/2014 (Date)	**Total Claims Allowed:** 11	
/HARRY W BYRNE/ Primary Examiner.Art Unit 2824 (Primary Examiner)	08/25/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4

U.S. Patent and Trademark Office

Part of Paper No. 20140825

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13455267	RAO, G. R. MOHAN
	Examiner	**Art Unit**
	LANCE REIDLINGER	2824

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
365	185.03	G	1	1	C	16 / 34 (2006.0)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
365	185.09	201	148	158	163

/LANCE REIDLINGER/ Examiner.Art Unit 2824 (Assistant Examiner)	08/25/2014 (Date)	**Total Claims Allowed:** 11
/HARRY W BYRNE/ Primary Examiner.Art Unit 2824 (Primary Examiner)	08/25/2014 (Date)	O.G. Print Claim(s): 1 O.G. Print Figure: 4

U.S. Patent and Trademark Office

Part of Paper No. 20140825

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13455267	RAO, G. R. MOHAN
	Examiner	**Art Unit**
	LANCE REIDLINGER	2824

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
4	4														
5	5														
6	6														
7	7														
8	8														
9	9														
10	10														
	11														
	12														
	13														
11	14														

/LANCE REIDLINGER/ Examiner.Art Unit 2824 (Assistant Examiner)	08/25/2014 (Date)	**Total Claims Allowed:** 11	
/HARRY W BYRNE/ Primary Examiner.Art Unit 2824 (Primary Examiner)	08/25/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4

U.S. Patent and Trademark Office Part of Paper No. 20140825

EAST Search History

EAST Search History (Prior Art)

<This search history is empty>

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	919	single adj (level bit data) adj (cell memory element).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:04
L2	2720	(plural multiple multi) adj (level bit data) adj (cell memory element).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:05
L3	1138	MLC!.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:05
L4	651	SLC!.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:05
L5	3190	2 3	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:05
L6	3063	1 2	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:05
L7	2725	5 and 6	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:05
L8	101412	"365".clas.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
L9	1486	7 and 8	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
L10	3807	365/185.03.ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
L11	1818	365/185.09.ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
L12	5784	365/201.ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
L13	10934	10 11 12	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
L14	885	13 and 7	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:07
L15	282940	address.clm.	US-PGPUB; USPAT;	OR	ON	2014/08/25 07:07

			UPAD			
L16	389370	(table map).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:08
L17	17911	15 near3 16	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:08
L18	284287	test$3.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:08
L19	4	7 and 17 and 18	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:08
L21	1	13/"Term Removed"	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:10
L28	1266	1 4	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:15
L29	652	28 and 5	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:15
L30	134	13 and 29	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:16
L31	5	18 and 30	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:16
L32	11706	365/148,158,163,171,173.ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:17
L33	17	29 and 32	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:17

8/25/2014 7:18:29 AM
C:\Users\rreidlinger\Documents\EAST\Workspaces\13455267.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13455267	RAO, G. R. MOHAN
	Examiner	**Art Unit**
	LANCE REIDLINGER	2824

CPC- SEARCHED		
Symbol	**Date**	**Examiner**

CPC COMBINATION SETS - SEARCHED		
Symbol	**Date**	**Examiner**

US CLASSIFICATION SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
365	185.03, 185.09	6/14/2014	RLR

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
Inventor Search Conducted in EAST	6/13/2014	RLR
See EAST Search history	6/14/2014	RLR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
365	185.03, 185.09, 201, 148, 158, 163	8/25/2014	RLR

/LANCE REIDLINGER/ Examiner.Art Unit 2824	

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CONFIRMATION NO. 6684

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/455,267	04/25/2012 RULE	365	2824	0299-0004.01

APPLICANTS

INVENTORS

G. R. Mohan Rao, Richardson, TX;

**** CONTINUING DATA ****************************

This appln claims benefit of 61/509,257 07/19/2011

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **

05/04/2012

Foreign Priority claimed	❑ Yes ☑ No		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	❑ Yes ☑ No	❑ Met after Allowance	TX	5	14	1
Verified and Acknowledged	/R LANCE REIDLINGER/ Examiner's Signature	Initials				

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TITLE

LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

FILING FEE RECEIVED		
530	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

BIB (Rev. 05/07).