Memory SUMMIT

SLC & MLC Hybrid

SiliconMotion

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Flash Memory SUMMIT

Agenda

- **SSD Today & Challenges**
  - **The Hybrid SLC + MLC concept**
- **The Hybrid Technology**
- **About Silicon Motion**

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SSD today & Challenges

- Why SSD have not taken off → #1 price..
  - 95% of SSD products today used SLC NAND components
  - SLC price is about 3X MLC with the same density
  - 90%+ of NAND output from flash makers is MLC NAND
  - SSD won't become mainstream applications without using MLC NAND
- What are the technical concerns to use MLC for SSD applications?
  - Performance -- longer programming time
  - Endurance – low program/erase cycles

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Performance concern

- MLC is slow in host write CMD, especially for ran. write
  - NAND flash requires "erase" before writing data to old blocks.
  - MLC need 2 ms to 3 ms, and SLC need 1.5 ms to erase a block
  - MLC need average 800 us to program a page (strong page 200 to 400 us, weak page 1.2 to 1.5ms). SLC only need 200 us.
- How to improve MLC SSD performance?
  - NAND flash components might not be able to improve very much
  - Controller's architecture in cache management and flash memory control

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Endurance Concern

- MLC has limited endurance
  - The program and erase cycle of each MLC block is limited
  - MLC is around 5K to 10K cycles, SLC is 100k cycles
- How to improve endurance of SSD with MLC NAND?
  - Better wear-leveling algorithm –> Treat all NAND components as one memory unit (global wear-leveling)
  - Overcome data swapping endurance concern by storing the frequently updated data in the reliable area.

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Suggested controller architectures

- Add caching mechanism
  - Bigger internal SRAM as cache
  - Utilize DRAM as cache
- Use both SLC and MLC (hybrid mode)

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The Hybrid SLC+MLC Concept

	Pure SLC Based Flash	Pure MLC Based Flash
Performance	**Fast access speed** (2 times > MLC) Good!	**Slow access speed**
Durability	**Good endurance** (10~20 times > MLC) Good!	**Poor endurance** (5K-10K program/erase)
Cost	**Expensive** (2-3 times > MLC)	**Cheaper** Good!

Why not combine SLC & MLC chips in SSD?

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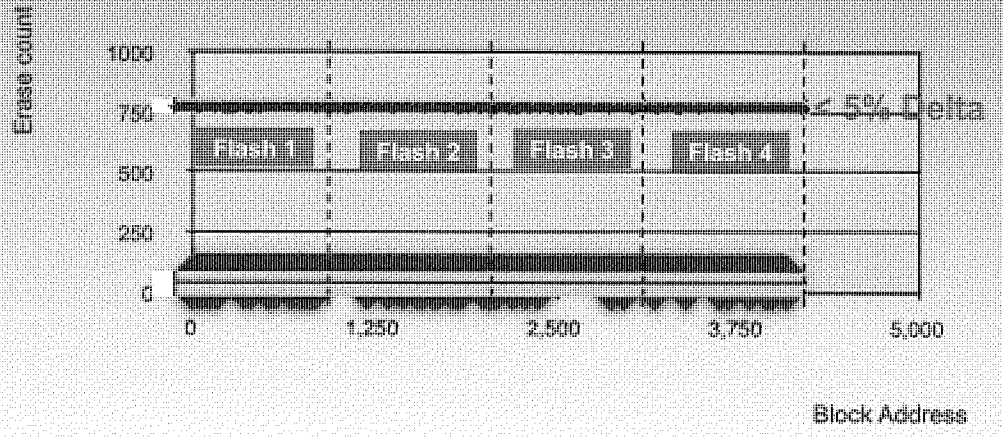
Global Wear Leveling Technology

SMI Global Wear Leveling would even the erase count of all blocks, effectively wear level the entire SSD to extend the life expectancy..

- Manage all NAND flash components as one unified flash memory.
- Map host device's logical addresses into NAND flash physical addresses equally and randomly.
- Endurance will be further improved when the total density increases.



Example: SM2240
Program: Fill to 50% capacity, Copy 256M-> Compare >Delete
Flash Type: K9F8G08U0M x 4

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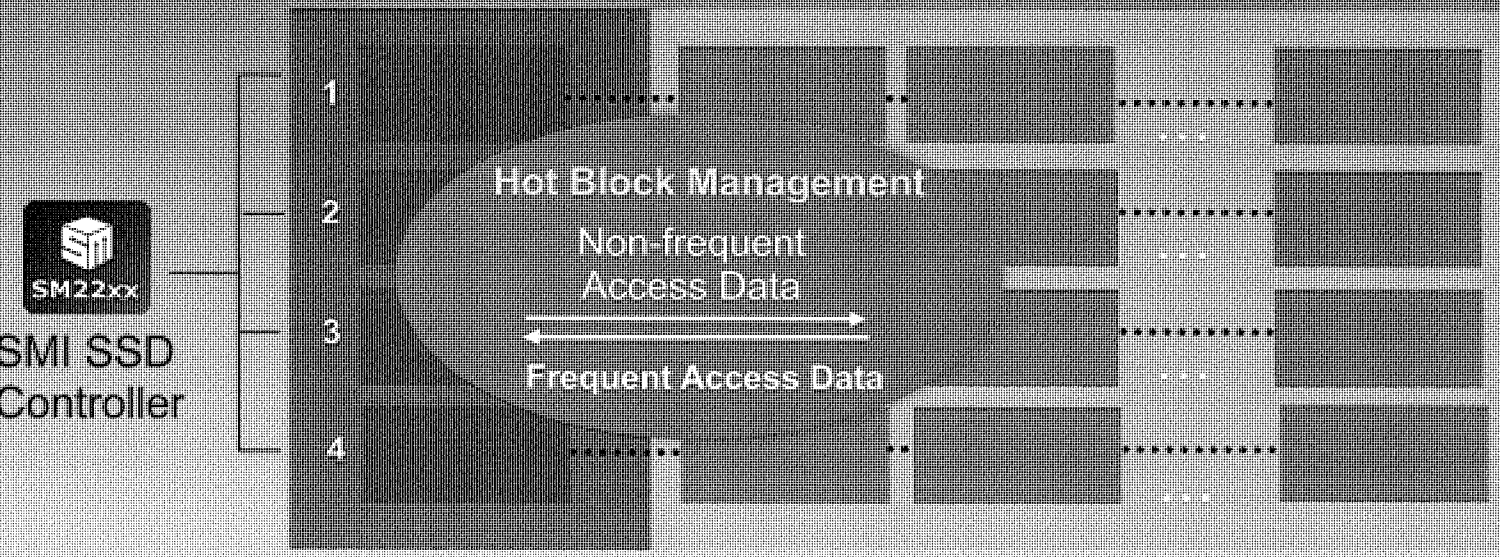
SMI SLC + MLC Hybrid Technology



MLC cost with SLC performance and endurance!

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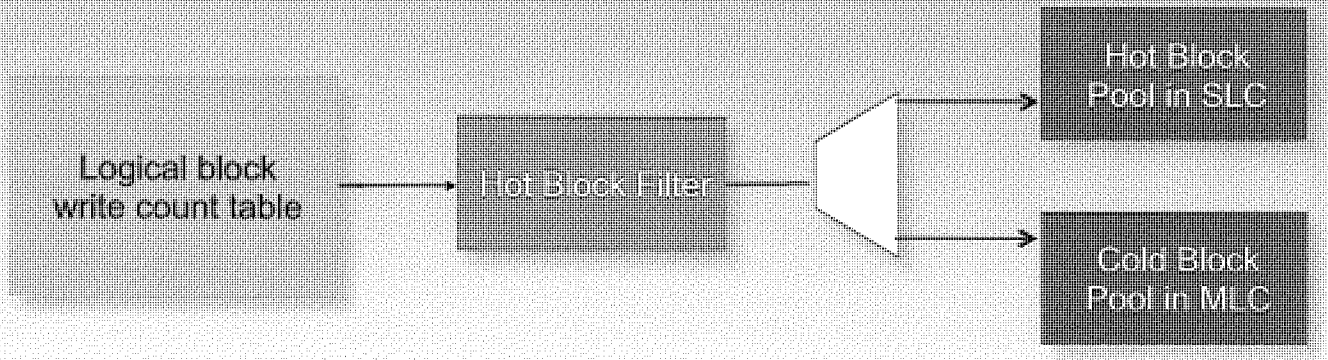
Hybrid SSD Technology

- SMI's proprietary "Hot Block Filter" & Flash management would monitor the flash write status and pick up Hot Blocks
  - Hot Block means a block whose data is frequently updated
- Move "Hot (physical) Blocks" whose logical blocks are frequently updated into SLC area, for better performance & endurance
- Move 'Cold (physical) Blocks' whose logical blocks are less frequently updated into MLC, for storage



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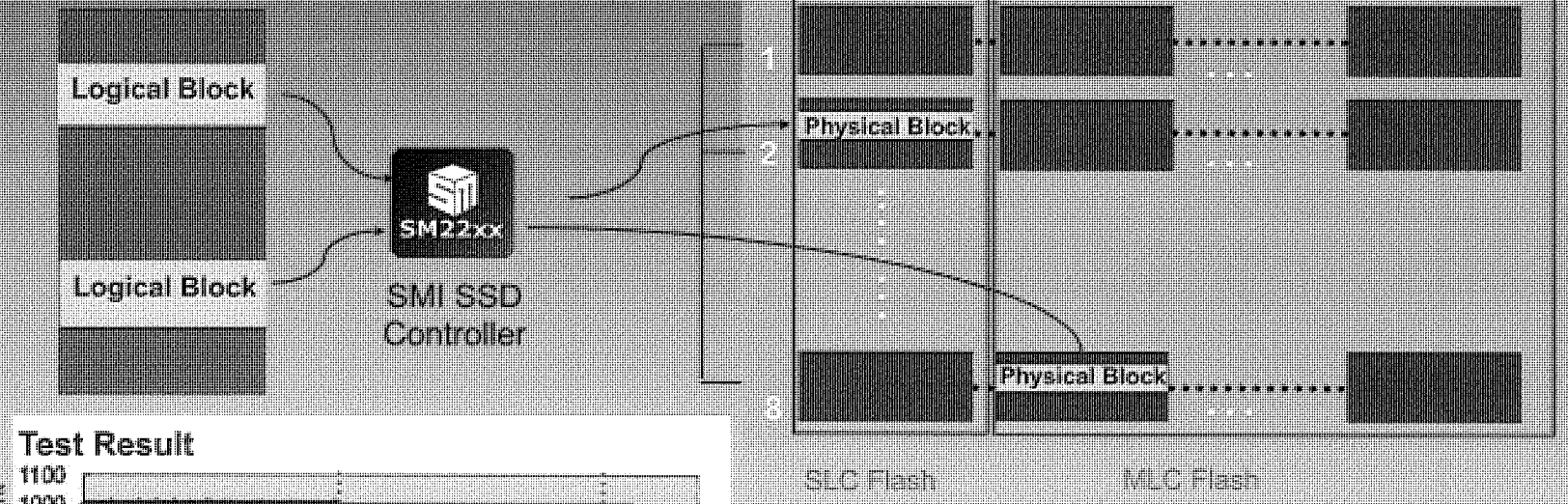
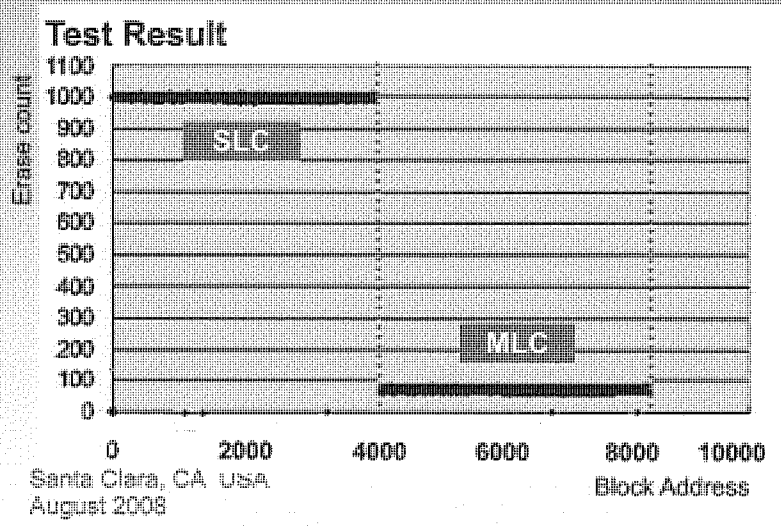
Hybrid Wear Leveling Result





- Example: SM2240 (captured from FPGA)
- Program: Fill 5.5GB (6GB total). Copy 500MB data-> Compare ->Delete
- Flash Type: K9K8Gx2 + K9LBGx2

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An Overview on SMI Hybrid SSD

- SMI hybrid SSD SLC/MLC ratio is configurable depends on the targeted application(s).

- Assuming overall frequent data is 'X' GB: Hybrid SSD = X GB in SLC + (total capacity – X)GB in MLC

  - Through "SMI Hot Block Filter", 'X' GB frequent data will be automatically moved to SLC portion. Result in a hybrid SSD that performs as a pure SLC SSD in read/write & endurance, and save the cost difference with MLC.

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Hybrid SLC/MLC SSD Benefits

- For Example: a 72 GB hybrid SSD (8GB SLC + 64GB MLC).
  - In a typical consumer application: if frequent updated data size is ~ 8GB, through Hot Block Filter of the hybrid SSD, the 8GB hot data will mostly located in SLC flash.

Benefits

- Cost: fraction of pure SLC
- Performance: 2 times > pure MLC
- Endurance: 3 times > pure MLC
- Data integrity as SLC
- User experience as the SLC

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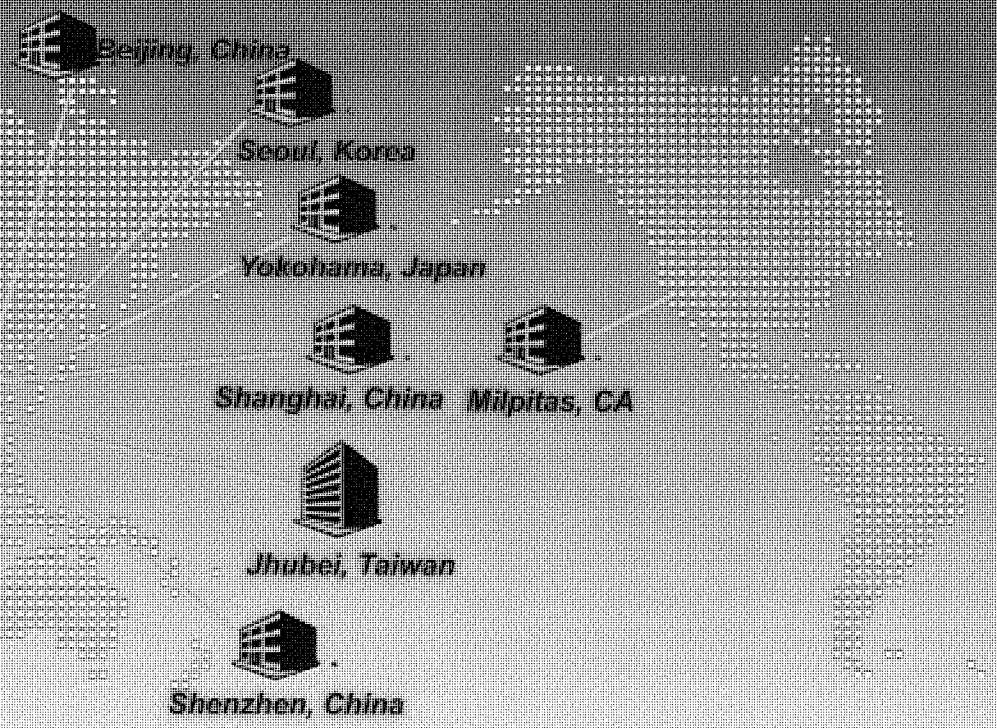
SMI WW Operations Support Global Focus



Headquarters:	Jhubei, Taiwan
Other Operations:	Seoul (Korea), Milpitas (USA), Shenzhen, Shanghai, and Beijing (China), Yokohama (Japan)
Employees:	600+ (380+ Engineers)
Distributors:	N. America, Europe, China, Singapore, Taiwan, Korea, Singapore

Santa Clara, CA USA
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Flash Memory Summit

PATA/SATA SSD Product Roadmap

PATA

SM223
- CFA4.1 UDMA5
- 2-CH, 8 CE/ch
- R/W: 50/45 MB/s
- 4 bit RS ECC
- Static WL within MU
- MP: Now

SM2231
- PATA, UMDA6
- 2-CH, 8 CE/ch
- R/W: 50/45 MB/s
- 13/24b 1KB BCH ECC
- Global WL
- MP: Q3'08

SM2233
- PATA. UDMA6
- 4-CH, 16 CE/ch
- R/W: 100/80 MB/s
- 8bit BCH ECC
- Global Wear Leveling
- PATA- BGA-144
- MP: Q3,'08

SATA

SM2240
- SATA II, UDMA6
- 4-CH, 16 CE/ch
- R/W: 100/80 MB/s
- 8bit BCH ECC
- Global Wear Leveling
- SATA- QFP-128
- MP: Q3, '08

SM2242
- SATA II, UMDA6
- 4-CH, 16 CE/ch
- R/W: 100/80 MB/s
- 13/24b 1KB BCH ECC
- Global Wear Leveling
- SATA- QFP-128
- MP: Q1, '09

SM2250
- 32-bit RISC CPU
- SATA II, 8-CH, 16 CE/ch
- R/W: 200/180MB/s
- 13/24b 1KB BCH ECC
- External DRAM Buffer
- High Speed NAND
- MP: Q2 '09

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Thank You!

Q&A

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