

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,

Petitioner

v.

VERVAIN, LLC,

Patent Owner

Inter Partes Review Case No. IPR2025-00214

Patent 9,997,240

PETITION FOR *INTER PARTES* REVIEW OF

U.S. PATENT NO. 9,997,240

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CASES

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LIST OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 9,997,240, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1002	Declaration of Carl Sechen, Ph.D.
1003	U.S. Provisional Application No. 61/509,257, titled “IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM” by Rao
1004	U.S. Patent No. 7,855,916, titled “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES,” to Rao
1005	U.S. Patent No. 8,891,298, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1006	Excerpts from prosecution history of ‘298 patent
1007-1009	<i>Intentionally omitted</i>
1010	Excerpts from prosecution history of ‘240 patent
1011-1024	<i>Intentionally omitted</i>
1025	Excerpts from Rino Micheloni, et al., INSIDE NAND FLASH MEMORIES (Springer 2010)
1026	Excerpts from NONVOLATILE MEMORY TECHNOLOGIES WITH EMPHASIS ON FLASH: A COMPREHENSIVE GUIDE TO UNDERSTANDING AND USING NVM DEVICES (Joe E. Brewer & Manzur Gill eds. Wiley-IEEE Press 2008)
1027	Excerpts from MICROSOFT COMPUTER DICTIONARY (5 th ed. 2002)
1028-1029	<i>Intentionally omitted</i>

1030	Yu Cai et al., <i>Program Interference in MLC NAND Flash Memory: Characterization, Modeling and Mitigation</i> (IEEE 2013)
1031	Kang-Deog Suh et al., <i>A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme</i> , 30 IEEE J. Solid State Circuits 1149 (Nov. 1995)
1032	Eitan Yaakobi et al., <i>Error Characterization and Coding Schemes for Flash Memories</i> (2010 IEEE Globecom Workshops, Miami, FL at 1856-60)
1033	Evans, Chris, “Enterprise MLC: How flash vendors are boosting MLC write endurance” (June 3, 2011)
1034	Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008)
1035	Ashish Jagmohan et. al., <i>Adaptive Endurance Coding for NAND Flash</i> (2010 IEEE Globecom Workshops, Miami, FL at 1841-45)
1036	Sungjin Lee et al., <i>FlexFS: A Flexible Flash File System for MLC NAND Flash Memory</i> (2009 USENIX Annual Technical Conference, San Diego, CA, June 14-19, 2009)
1037	Minyoung Sung & Kanghee Kim, <i>Asymmetric Flash Volume Management</i> , 58 IEEE Transactions on Consumer Electronics 455 (May 2012)
1038	Greg Atwood et al., <i>Intel StrataFlash™ Memory Technology Overview</i> at 4, Intel Technology J. (Q4 1997)
1039	Taehee Cho et al., “A 3.3 V 1 Gb multi-level NAND flash memory with non-uniform threshold voltage distribution,” <i>2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers</i> , ISSCC (Cat. No. 01CH37177) (2001)
1040	U.S. Patent No. 6,456,528, titled for “SELECTIVE OPERATION OF A MULTI-STATE NON-VOLATILE MEMORY SYSTEM IN A BINARY MODE” to Chen

1041	U.S. Patent No. 8,078,794, titled “HYBRID SSD USING A COMBINATION OF SLC AND MLC FLASH MEMORY ARRAYS,” to Lee et al.
1042	U.S. Patent Appl. Pub. No. 2008/0140918, titled “HYBRID NON-VOLATILE SOLD STATE MEMORY SYSTEM” by Sutardja
1043	U.S. Patent Appl. Pub. No. 2009/0327591, titled “SLC-MLC COMBINATION FLASH STORAGE DEVICE,” by Moshayedi
1044	U.S. Patent Appl. Pub. No. 2010/0172179, titled “SPARE BLOCK MANAGEMENT OF NON-VOLATILE MEMORIES,” by Gorobets et al.
1045	U.S. Patent No. 8,634,240, titled “NON-VOLATILE MEMORY AND METHOD WITH ACCELERATED POST-WRITE READ TO MANAGE ERRORS,” to Gavens et al.
1046	U.S. Patent No. 8,806,301, titled “DATA WRITING METHOD FOR A FLASH MEMORY, AND CONTROLLER AND STORAGE SYSTEM USING THE SAME,” to Yu et al.
1047	U.S. Patent Appl. Pub. No. 2010/0115192, titled “WEAR LEVELING METHOD FOR NON-VOLATILE MEMORY DEVICE HAVNG SINGLE AND MULTI LEVEL MEMORY CELL BLOCKS,” by Lee
1048	U.S. Patent Appl. Pub. No. 2011/0271043, titled “SYSTEM AND METHOD FOR ALLOCATING AND USING SPARE BLOCKS IN A FLASH MEMORY,” to Segal et al.
1049	U.S. Patent Appl. Pub. No. 2011/0153912, titled “MAINTAINING UPDATES OF MULTI-LEVEL NON-VOLATILE MEMORY IN BINARY NON-VOLATILE MEMORY,” by Gorobets et al.
1050	U.S. Patent No. 5,930,167, titled “MULTI-STATE NON-VOLATILE FLASH MEMORY CAPABLE OF BEING ITS OWN TWO STATE WRITE CACHE,” to Lee et al.

1051	U.S. Patent Appl. Pub. No. 2010/0172180, titled “NON-VOLATILE MEMORY AND METHOD WITH WRITE CACHE PARTITIONING,” by Paley et al.
1052	<i>Intentionally omitted</i>
1053	U.S. Patent Appl. Pub. No. 2009/0268513, titled “MEMORY DEVICE WITH DIFFERENT TYPES OF PHASE CHANGE MEMORY,” by De Ambroggi et al.
1054	U.S. Patent Appl. Pub. No. 2009/0307418, titled “MULTI-CHANNEL HYBRID DENSITY MEMORY STORAGE DEVICE AND CONTROL METHOD THEREFOR,” by Chen et al.
1055	U.S. Patent Appl. Pub. No. 2010/0058018, “MEMORY SCHEDULER FOR MANAGING INTERNAL MEMORY OPERATIONS,” by Kund et al.
1056-1060	<i>Intentionally omitted</i>
1061	Duane H. Oto et al., <i>High-Voltage Regulation and Process Considerations for High-Density 5 V-Only E²PROM’s</i> , SC-18 IEEE J. Solid State Circuits 532 (Oct. 1983)
1062	Gheorghe Samachisa et al., <i>A 128K Flash EEPROM Using Double-Polysilicon Technology</i> , SC-22 IEEE J. Solid State Circuits 676 (Oct. 1987)
1063	Masaki Momodomi et al., <i>An Experimental 4-Mbit CMOS EEPROM with a NAND-Structured Cell</i> , 24 IEEE J. Solid State Circuits 1238 (Oct. 1989)
1064	Tae-Sun Chung et al., <i>A survey of Flash Translation Layer</i> , 55 J. Systems Architecture 332-43 (2009)
1065	Yoshiba Iwata et al., <i>A High-Density NAND EEPROM with Block-Page Programming for Microcomputer Applications</i> , 25 IEEE J. Solid-State Circuits 417 (Apr. 1990)

1066	Simona Boboila and Peter Desmoyers, <i>Write Endurance in Flash Drives: Measurements and Analysis</i> , Usenix Conference (Feb. 2010)
1067	SiliconSystems, <i>Increasing Flash SSD Reliability</i> , StorageSearch.com (April 2005)
1068	Taehee Cho et al., <i>A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single Level Modes</i> , 36 IEEE J. Solid State Circuits 1700 (Nov. 2001)
1069	Ken Takeuchi, <i>A Multipage Cell Architecture for High-Speed Programming Multilevel NAND Flash Memories</i> , 33 IEEE J. Solid-State Circuits 1228 (Aug. 1998)
1070-79	<i>Intentionally omitted</i>
1080	Docket list for <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex., filed March 8, 2024)
1081	Docket list for <i>Vervain, LLC v. Kingston Technology Company, Inc.</i> , No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024)
1082	First Amended Complaint, Doc. No. 9 in <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex.)
1083	Signed Agreed Scheduling Order, Doc. No. 16 in <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex.)

I. INTRODUCTION:

Phison Electronics Corporation (“Phison” or “Petitioner”) requests *inter partes* review (“IPR”) of all claims 1-10 (the “Challenged Claims”) of U.S. Patent No. 9,997,240, entitled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Dr. G.R. Mohan Rao (the “‘240 patent”) (Ex. 1001), which is assigned to Vervain, LLC (“Vervain” or “Patent Owner”). The ‘240 patent issued on Jun. 12, 2018, from U.S. Appl. No. 14/950,553, which was filed Nov. 24, 2015, as a continuation of U.S. App. No. 14/525,411, filed Oct. 28, 2014 (now U.S. Patent No. 9,196,385, “the ‘385 patent”) which was a continuation of U.S. Appl. No. 13/455,267, filed Apr. 25, 2012, which issued as U.S. Patent No. 8,891,298 (the “‘298 patent,” Ex. 1005) on Nov. 18, 2014. (Ex. 1001). Each of the ‘240, ‘385 and ‘298 patents incorporated by reference Dr. Rao’s U.S. Patent No. 7,855,916,¹ and claimed priority from U.S. Provisional App. No. 61/509,257, filed on July 19, 2011 (“Provisional,” Ex. 1003, *e.g.*, ‘240 1:1:17-20).

¹ (‘240 1:23-30, “Rao ‘916,” Ex. 1004.) Rao ‘916, entitled “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES,” was incorporated along with U.S. Patent No. 8,194,452 to Dr. Rao of the same title and specification (‘240 1:30-36).

The ‘298, ‘385 and ‘240 patents, along with U.S. Patent Nos. 10,950,300 (“the ‘300 patent”), 11,830,546 (“the ‘546 patent”), 11,854,612 (“the ‘612 patent”), 11,967,369 and 11,967,370, all with the same title and based on the same Apr. 25, 2012, specification and claiming July 19, 2011, priority, are currently asserted (First Amended Complaint, Ex. 1082) by the Patent Owner against Petitioner in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex. filed March 8, 2024).² Petitioner has petitioned for reviews by this Board in pending *Phison*

² That complaint was dismissed in part on Dec. 2, 2024. (Docket List [Ex. 1080] entry 38.) All the patents are also asserted against a customer of Phison in *Vervain, LLC v. Kingston Technology Company, Inc., Kingston Digital, Inc., and Kingston Technology Corp.*, No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024). The first four patents were earlier asserted in *Vervain, LLC v. Micron Technology, Inc.*, No. 6:21-cv-00487 (W.D. Tex. filed May 10, 2021, settled April 21, 2023) and *Vervain, LLC v. Western Digital Corp.*, No. 6:21-cv-00488 (W.D. Tex. filed May 10, 2021, settled Aug. 8, 2023). Micron petitioned this Board for review in *Micron Technology, Inc. v. Vervain, LLC*, IPR2021-01547 (‘298 patent), -01548 (‘385 patent), -01549 (‘240 patent), and -01550 (‘300 patent), which were instituted on April 8 and 11, 2022, and terminated on April 4, 2023, on settlement after hearing but prior to final written decision.

Electronics Corp. v. Vervain, LLC, PGR2024-00047,³ PGR2024-00048,⁴ IPR2025-00212,⁵ and IPR2025-00213.⁶

This Petition demonstrates by a preponderance of the evidence that the Challenged Claims are unpatentable as claiming a long-known hybrid memory system of distinct Single-Level Cell (“SLC”) and Multi-Level Cell (“MLC”) NAND flash memory modules “adapted” to perform two optional functions of directing data preferentially to the SLC module, under two circumstances: (1) failure of a “data integrity test” (7:47-54 [claim 1]; 8:42-49 [claim 6]); and (2) in conjunction with (a) “allocation/segregation” of “blocks” in the MLC and SLC modules to according to relative frequency of “writes” (7:55-62 [claim 1]; 8:37-41 [claim 6]), (b) “transfer” of the “contents” of “counted blocks” to the SLC module “after reaching the predetermined count value” (7:62-8:7 [claim 1]; 8:50-59 [claim 6]). These functions were suggested in the specification as improving “lifetime (endurance),” but, in the detail recited, they had long been disclosed in the extensive NAND flash memory art which included many error management and wear leveling techniques for

³ (‘546 patent, accorded filing date Aug. 27, 2024 [Paper No. 5].)

⁴ (‘612 patent, accorded filing date Sept. 25, 2024 [Paper No. 5].)

⁵ (‘298 patent, filed Nov. 25, 2024.)

⁶ (‘385 patent, filed Dec. 4, 2024.)

avoiding premature failure of hybrid systems. For Ground 1 of invalidity, Petitioner starts with one published hybrid memory system (U.S. Patent No. 8,634,240 to Gavens et al.⁷) with multiple error management techniques and shows that a POSITA would apply known wear leveling techniques for the common objective of avoiding premature failure, thereby showing independent claims 1 and 6 obvious in view of the knowledge of the POSITA. Conversely, for Grounds 2 and 3, Petitioner starts respectively with two published hybrid memory systems (U.S. Patent Appl. Pub. No. 2009/0327591, by Moshayedi,⁸ and U.S. Patent Appl. Pub. No. 2008/0140918, by Sutardja⁹) with multiple wear leveling techniques and shows that a POSITA would apply known error management techniques for the common objective of avoiding premature failure, thereby showing claims 1 and 6 obvious in view of the knowledge of the POSITA. Under each Ground, the remaining Challenged Claims are also obvious over the asserted document in view of that document and other knowledge of the POSITA.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8:

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1):

Petitioner Phison Electronics Corporation is the real party-in-interest.

⁷ (“Gavens,” Ex. 1045, published Apr. 28, 2011 [cover].)

⁸ (“Moshayedi,” Ex. 1043.)

⁹ (“Sutardja,” Ex. 1042.)

B. Related Matters Under 37 C.F.R. § 42.8(b)(2):

As set forth further at note 3 *supra*, the ‘240 patent (along with seven other patents based on the same specification) is currently asserted by Vervain against Phison and its customer (separately) in the Western District of Texas. In the Phison case, a claim construction hearing is tentatively scheduled for December 5, 2024, and jury selection is tentatively scheduled for December 15, 2025 (*Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259, Doc. No. 16 (W.D. Tex. July 15, 2024) (Ex. 1083). Resolution of this Petition may simplify that litigation and promote settlement.

C. Lead and Back Up Counsel Under 37 C.F.R. § 42.8(b)(3):

Pursuant to 37 C.F.R. § 42.8(b)(3), lead counsel for this Petition is Hsuanyeh Chang, PhD (Reg. No. 73,431) and back-up counsel are Stephen Y. Chow (Reg. No. 31,338), Douglas E. Chin (Reg. No. 66,713), and Peter Yi (Reg. No. 61,790). Pursuant to 37 C.F.R. § 42.10(b), Petitioner has filed a power of attorney designating the above-identified counsel.

D. Service Information Under 37 C.F.R. § 42.8(b)(4):

Service information under 37 C.F.R. § 42.8(b)(4) for the Petition is as follows:

Lead Counsel	Back-Up Counsel
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III. ADDITIONAL REQUIREMENTS:

A. Payment of Fees Under 37 C.F.R. § 42.15:

The required fees are submitted from Deposit Account No. 50-6685 (Order No. 1280-0013). If any additional fees are due at any time during this proceeding, the Office is authorized to charge such fees to Deposit Account No. 50-6685 (Order No. 1280-0013).

B. Timing Under 37 C.F.R. § 42.102:

The present petition for *inter partes* review is filed more than nine months after the grant of the ‘240 patent.

C. Grounds for Standing Under 37 C.F.R. § 42.104(a):

Petitioner certifies that: (1) the ‘240 patent is eligible for *inter partes* review; and (2) Petitioner is not barred or estopped from requesting *inter partes* review of any claims of the ‘240 patent on the grounds identified herein.

IV. NAND FLASH TECHNOLOGY BACKGROUND

Petitioner’s expert, Dr. Carl Sechen, has provided in his declaration (“Sechen,” Ex. 1002) a deep analysis of the state of NAND flash technology implicitly relied on by the ’240 patent, the embodiments admitted or advanced in the specification, the evolution of the claims through prosecution and their remaining defects, and invalidity of those claims over the prior art in view of the POSITA’s knowledge of the art. Following is a summary of the NAND flash memory technology underlying the ‘240 patent base claims to a “system for storing data,” based on known MLC and SLC NAND flash modules and a “controller” coupled to them and maintaining known NAND flash address mapping and “adapted” to perform optional, also known, error management and wear leveling.

A. Characteristic Nature of NAND Flash Memory

A **NAND flash cell** is a type of transistor with a floating gate that can retain electrical charges associated with “threshold voltages” that, applied to a control gate,

allows conduction of electrical current from drain to source. (Sechen ¶¶ 26 [Fig. 2.1(a)], 40 [Figures 6 and 7 from Atwood {Ex. 1038}] and 41.)

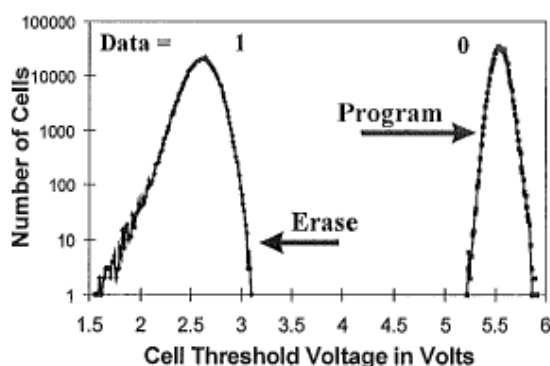


Figure 6: Single bit/cell array threshold voltage histogram

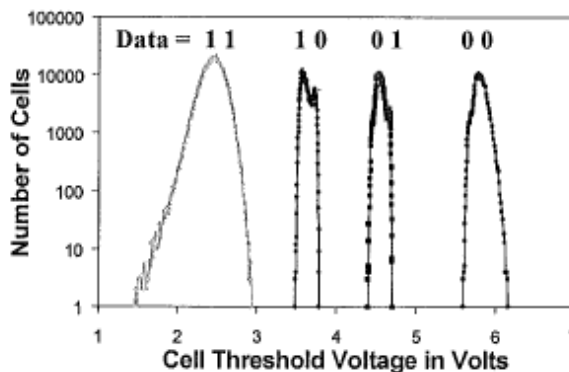


Figure 7: Two bit/cell array threshold voltage histogram

These threshold voltages may be chosen to represent information to be stored, in “classic” NAND memory operation, using two threshold voltage levels (Figure 6), the lower level to represent (“store”) a logical “1” and the higher level to store a “0” of one bit of digital computer data. (*Id.*) The same storage cell can use four threshold voltage levels (Figure 7) to represent four values corresponding to two bits of binary computer data (which in NAND memory operation is sourced from two distinct groups, “pages,” of logical data). (*Id.*) An n power of two (2^n : eight, sixteen, . . .) threshold levels may be used in NAND flash operation to represent corresponding bits of n pages (*id.* ¶¶ 40 and 42-43). But a cell or group of cells do not constitute “memory,” which requires circuitry for selecting, programming (writing) and reading the cell or group of cells (*id.* ¶¶ 26 and 29).

To form **NAND flash memory**, storage cells are hard wired in strings (bit-line “columns”) and word-line “rows” forming “**pages**” each typically 2K storage cells **programmed** (written) **page by page**. (*Id.* ¶ 26.) NAND flash is so characterized by wiring of its storage cells in typically 64-page “**blocks**,” individually **erased in unison** to prepare for writing of new pages (*id.* ¶¶ 28-30). Unlike magnetic hard disk drives and other technologies that allow “write in place” of data at a physical location assigned to prior versions, in NAND flash programming, an update to stored data must be written to a physical location that is erased in preparation (“erase before write”); erasure, a much longer process than writing, is done in the background, when there are no user-requested read or write operations. (*Id.*) To maintain logical visibility to the user of a NAND flash memory device such as a Solid State Drive (“SSD”) (shown at Sechen ¶ 30), there are maintained and updated tables in or available to a **NAND flash device controller**, shown as a hardware module or chip on an SSD circuit board (*id.*) to “map” logical locations to physical locations in the NAND flash memory array (“**L2P mapping**”), which update for each data write (*id.* ¶¶ 30 and 31). The physical instances of NAND flash pages and blocks determine the **Physical Block** Addresses (“PBA”) mapped from the construct of **Logical Block** Addresses (“LBA”). (*Id.* ¶¶ 32-34.) This mapping and remapping is performed with the software **Flash Translation Layer** (“**FTL**”) of the controller. (*Id.* ¶¶ 31-38.) The physical reading, writing and erasing

of NAND flash cells is performed by circuitry in a NAND flash memory module, shown in multiples in Sechen paragraphs 29 and 30 (“flash,” “flash memory” or just “NAND”) on a board, along with a block diagram identifying reading, writing and erasing functions (*id.* ¶ 29). A POSITA would understand this to be a **NAND flash memory or module**. (*Id.* ¶ 30.)

B. Characteristic NAND Flash Memory Management

Sechen paragraphs 34-38 outline common processes in the use of NAND flash memory. These include **bad block management** and **garbage collection** to make available adequate numbers of blocks for new writes without unnecessary, time-consuming erasures. Typically, “hot” data, *i.e.*, frequently updated (such as system data, and “cold” (not-“hot”) data are clustered in respective physical blocks in order to facilitate efficient (fewer erase-and-re-writes) collecting of “valid” (un-updated) stored data and freeing up the blocks they otherwise occupy. Related “**wear leveling**” processes (“dynamic” at the time of writing and “static” in the background) even out write and erase stresses on NAND memory blocks – which have limited expected “endurance” (“lifetime”) – aiming to avoid premature failure or retirement of enough blocks that would compromise system use. (Sechen ¶ 39 [**system lifetime**].)

C. Introduction of MLC and SLC Flash

Multi-level cell (MLC) NAND flash, developed in 1992-97, as described in Atwood (Ex. 1038), was the use of the NAND storage cell with four threshold voltage levels to represent two bits of information. (Sechen ¶¶ 40-41.) The first known use of the term “SLC” was in a 2001 article that called the established technology “**single-level program cell NAND flash (SLC)**” and compared it with then new MLC. (Ex. 1039, Sechen ¶ 42.) Although the terms have been shortened over the years, a POSITA would understand that “MLC” refers to the use of NAND storage cells, each storing two bits written in two passes – a “lower” (least significant bit, “LSB”) logical page and then a distinct “upper” (most significant bit, “MSB”) logical page. (*Id.* ¶ 43.) That is, MLC flash memory allows writing **two logical data pages into one physical page of memory**. As reviewed at Sechen paragraph 43 (particularly Sechen note 17), the programming of MLC memory is more complex and stressful than SLC because of MLC’s narrower window for distinct threshold charges and its multiple passes of writing; also, a page-wide set of latches (page buffer) is required for reading *each* level of logical page programming. Thus, a POSITA would understand that different circuitry is required for **MLC NAND flash memory** than for **SLC NAND flash memory**, and that **SLC NAND flash memory is incapable of storing more than one logical data page in one physical page of memory**.

Two-state operation of MLC (later called **pseudo-SLC**) was disclosed by 2002. (Sechen ¶ 49; U.S. Patent No. 6,456,528 to Chen for “Selective Operation of a Multi-State Non-Volatile Memory System in a Binary Mode” [“Chen ‘528,” Ex. 1040] [one-bit *mode* of writing only one logical data page into one MLC physical page of memory]). This mode of MLC use, applying the MLC memory circuitry and pulsed/phased writing, has inferior performance and endurance relative to “real” SLC. A SanDisk suite of patents (incorporating by reference among others, Chen ‘528) disclosed lower-density (pSLC) *mode* use of MLC modules through partitioning and configuration for multiple purposes, including faster processing for caching writes and error management (*e.g.*, Gavens [Ex. 1045]; U.S. Patent No. 8,806,301 to Yu et al., published Apr. 14, 2011 [Ex. 1046], explained at Sechen ¶¶ 53-56).

D. Known Hybrid Use of SLC and MLC NAND Flash Modules with Strategies of Preferential Mapping, Wear Leveling and Error Management

Because of the compression of its threshold levels and its multiple passes of writing, MLC NAND flash was well-known to wear more quickly (have less “endurance”) and perform more slowly than SLC NAND flash. (Sechen ¶¶ 40-42.) Thus, it was proposed as early as 2008 to use hybrid systems of **SLC modules** and **MLC modules** in which more **frequently written/updated data**, such as system data, user directories, and certain user files, would be written **preferentially to a**

more robust **SLC module** while less frequently updated data would be written to the MLC module. (Sechen ¶ 46; Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008) [“Duann,” Ex. 1034]; U.S. Patent No. 8,078,794 to Lee et al., published Sept. 4, 2008 [“Lee ‘794,” Ex. 1041].)

This **SLC module preference** was applied in 2008-09 to a variety of **wear leveling** techniques to avoid premature failure of a system by some components reaching their endurance limits before others. (Sechen ¶¶ 47-48 and 58-60; *e.g.*, Sutardja [Ex. 1042]; Moshayedi [Ex. 1043].)

Additional tools or techniques were known in the art before the priority date to avoid premature failure by applying **error management near the end of life** of the system, with **preferential writing to SLC** upon failure of some “data integrity test” at an MLC location. (Sechen ¶¶ 53-56 and 58-61, *e.g.*, Gavens [Ex. 1045].)

The availability to the POSITA of these **preferential writing to SLC** techniques to avoid premature failure make obvious the base claims 1 and 6 of the ‘240 patent. (Sechen ¶ 62, Sections X(A), XI(A) and XII(A).)

V. THE ‘240 PATENT: Specification

The core disclosed system of known MLC NAND flash and SLC NAND flash modules is described multiple times in the specification. (*E.g.*, 4:17-20, 6:59-7:2; Sechen ¶ 69.) Fig. 4 shows a physical memory device module including two banks each including 8+ **MLC flash memory modules** and 2+ **SLC NAND flash memory**

modules). A controller “coupled” to the MLC and SLC modules performs L2P/FTL functions essential for NAND flash operation and also performs common wear leveling. (2:66-3:31 [BACKGROUND FTL/wear leveling]; *compare* Sechen ¶¶ 34-36.) Only two features are proposed in the DETAILED DESCRIPTION, for “increasing the reliability and lifetime of a NAND flash storage system” (4:66-7:28).

The first, “data integrity test” feature is shown as the NAND flash method steps of Figs. 3A and 3B, explained in the text (6:7-45). Dr. Sechen identifies (¶ 71) ambiguities even as to the recited comparison of “stored data” and “retained data.”

The second feature is functionally explained in two sentences, the first describing what appears to be wear leveling by “**allocat[ing]** ‘hot’ blocks i.e., those blocks that receive frequent writes, into the **SLC NAND flash memory module 28**, while allocating ‘cold’ blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26.” (6:46-52 [emphasis added].) The second sentence suggests implementation of the first by “**maintain[ing]** a count of those blocks that are accessed (written to) most frequently” and “**transfer[ring]** the contents of those blocks into the SLC NAND flash memory module 28” – “on a periodic basis” such as “every 10,000 writes.” (6:52-58 [emphasis added].) Dr. Sechen identifies (¶ 73) multiple fundamental ambiguities, including (1) whether the described functions refer to logical or physical blocks, (2) whether they are performed on a dynamic (writing as directed by the host) or static (background)

basis, and (3) what is the “transfer” condition of “periodic basis” in view of the exemplary threshold (10K being the full expected MLC “life”). Petitioner shows that the extensive prior art discloses or makes obvious the multiple alternatives in the detail disclosed and claimed, where the condition of “transfer” was limited to “after reaching the predetermined count value” by the amendment leading to the issuance of the ‘240 patent (Sechen ¶ 81, Jan. 22, 2018, [‘240] Amendment at 2-3, 3-4 [Ex. 1010 at 99-100, 100-101].)

VI. The Challenged Claims of the ‘240 Patent (37 C.F.R. § 42.104(b)(1):

Independent **claims 1** (7:12-8:4) **and 6** of the ‘240 patent, supported by no more than the known MLC-SLC hybrid system with known controller L2P functionality plus “embodiments” of two optional features, vary from claim 1 of the first, ‘298 patent (Ex. 1005) only by verbal mix-and-match of the ambiguous specification description of a wear leveling feature.¹⁰ As shown in note 9 and further

¹⁰ Each recites a “system for storing data” with two elements, the MLC and SLC non-volatile memory (“NVM”) modules and a coupled “controller.” (*Compare* ‘298 7:7-15 *with* ‘240 7:30-37 [claim 1] *and* 8:20-28,) The ‘298 controller is “adapted” to perform four functions labeled a)-d), with function a) being the L2P mapping necessary for NAND flash function (‘298 7:16-25), while the ‘240 controllers are limited to the identically described L2P function [a] (‘240 7:37-46, 8:27-36, labels

below, claims 1 and 6 parse the wear leveling description into controller function [c] (as labeled) segregation/allocation of relative “hot blocks” and “cold blocks” into SLC and MLC respectively and controller function [d] of transferring “after reaching the predetermined count value” of MLC/all blocks.

Dependent Claims: Claims 2-5 and 7-10 respectively limit the systems of claims 1 and 6 to the use of MLC “flash” with SLC “flash” or the alternative RRAM, PCM and MAGRAM technologies.

In view of the claims and disclosure of the ‘240 patent, the accompanying prior art references and supporting declaration of Dr. Sechen (Ex. 1002), Petitioner

added to below quotations of claim language). ‘298 controller function b) (“data integrity test”) (‘298 7:26-32) is repeated verbatim for ‘240 data integrity test function [b] (‘240 7:47-54, 8:42-49). But ‘298 controller function c) (determine most frequently accessed blocks) (8:1-5) and function d) (“allocate” by transferring contents) (8:6-9) are reflected in different combinations and permutations of the two-sentence wear leveling disclosure (‘240 6:46-58) in ‘240 claims function [c] (7:55-62 [claim 1 “segregate” MLC/SLC by write frequency], 8:37-41 [claim 6 “allocate” MLC/SLC by write frequency) and transfer “after reaching the predetermined count value” function [d] (7:62-8:7) [claim 1 count value for MLC blocks], 8:50-59 [claim 6 count value for all blocks]).

respectfully requests cancellation of the Challenged Claims as summarized (pursuant to 37 C.F.R. § 42.104(b)(1), -(2), -(4) and -(5) below.

Grounds	Exhibits
<p>Ground 1: Claims 1-10 are unpatentable under U.S.C. § 103 as obvious over Gavens and incorporated disclosures in view of a POSITA's knowledge of NAND flash technology.</p>	<p>1001, 1002, 1003, 1025, 1039, 1040, 1041, 1042, 1043, 1045, 1049, 1050, 1051, 1053, 1054, 1055</p>
<p>Ground 2: Claims 1-10 are unpatentable under U.S.C. § 103 as obvious over Moshayedi in view of a POSITA's knowledge of NAND flash technology.</p>	<p>1001, 1002, 1025, 1042, 1043, 1045, 1053, 1054, 1055</p>
<p>Ground 3: Claims 1-10 are unpatentable under U.S.C. § 103 as obvious over Sutardja in view of a POSITA's knowledge of NAND flash technology.</p>	<p>1001, 1002, 1025, 1042, 1043, 1045, 1053, 1054, 1055</p>

VII. Person of Ordinary Skill in the Art

A person of ordinary skill in the art at the time of the claimed invention would have a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least two years of experience in the design, development, implementation, or management of memory devices and systems. A person with an advanced degree in a relevant field would require less experience than noted above. As is common, one could obtain equivalent knowledge and perspective from other life experiences as well. (Sechen ¶¶ 60-61.)

VIII. 37 C.F.R. § 42.104(b)(3): CLAIM CONSTRUCTION

Under 37 C.F.R. § 42.100(b), claims in an *inter partes* review proceeding are construed using the same standard as that in a civil action. This includes “construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent,” *id.* The standard for claim construction is set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

The terms “MLC non-volatile memory modules” (7:31-32 and 8:21-22) and “SLC non-volatile memory module” (7:33-34 and 8:23-25) have distinct, established, customary meanings for a POSITA (Section IV *supra* and Sechen Section V) where “memory” and “module” also have distinct meanings:

- “MLC memory modules” means “modules comprising MLC non-volatile memory” *where*

“MLC non-volatile memory” means “non-volatile memory cells arranged with circuitry capable of storing multiple logical pages in a single physical page of cells” and

- “SLC memory module” means “module comprising SLC non-volatile memory” *where*

“SLC non-volatile memory” means “non-volatile memory cells arranged with circuitry incapable of storing multiple logical pages in a single physical page of cells”

Dr. Sechen explained (§ 90) why a POSITA would only understand “SLC” and “MLC” to refer to distinct NAND flash memory circuitry. Most tellingly, despite Dr. Rao’s knowledge of use of MLC in 2-state *mode*, corroborated by his Information Disclosure Statements from the original application,¹¹ Dr. Rao described and

¹¹ (Ex. 1006 at 26-36, notably Taehee Cho et al., *A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single Level Modes*, 36 IEEE J. Solid State Circuits 1700, 1700 (Nov. 2001) [Ex. 1068] and Ken Takeuchi, *A Multipage Cell Architecture for High-Speed Programming Multilevel NAND Flash Memories*, 33 IEEE J. Solid-State Circuits 1228, 1230 Figs. 5-7 (Aug. 1998) [Ex. 1069].)

claimed his invention as a system with distinct, known MLC and SLC memory modules, “adapted” to two operational features – but not 2-state *mode* operation of only one MLC memory. In addition to explicit references to distinct modules (e.g., 4:17-20, 6:59-7:2, Fig. 4), Dr. Rao incorporated Rao ‘916 (Ex. 1004), his proposal to operate a known SLC memory module (Figs. 6a and 8 [100K p-e cycle endurance]) in a purportedly new way.

“Blocks”: Petitioner maintains its position in the court litigation that the term is indefinite as to whether it refers to logical or physical blocks (Sechen ¶¶ 73 and 90) but will show here that the recited limitations are met under either construction.

“Controller”: Petitioner maintains in the court litigation that the term is indefinite for, among other things, failing to provide necessary structure or algorithms, but will show that the recited functions are met by the art.

“Data Integrity Test”: Petitioner maintains in the court litigation that this term (across multiple patents) means “a test that compares stored data to retained data.” As noted by Dr. Sechen (¶ 87), the claim recitation of that test is defective. To the extent understandable, the art discloses the claimed use of the test.

“Allocate,” “Segregate,” “Infrequently,” “Frequently,” “Most Frequently,” “Access,” “Count,” “Counted Block,” “Periodic,” “Predetermined Count Value,” “Transfer,” and “Content”: As reviewed by Dr. Sechen (¶¶ 83, 88 and 94), these terms are ambiguous due to their mix-and-match

use and some new appearances in the claims, exacerbating their ambiguity, particularly in the two-sentence “wear leveling” disclosure. As shown below, the extensive choices among prior art wear leveling techniques disclose or render obvious the different claim 1 and claim 6 recitations, especially given the dominant condition of “after reaching the predetermined count value.”

* * * * *

Grounds for Review Under 37 C.F.R. § 42.104(b)(4) -(5):

IX. GROUND 1: The Challenged Claims Are Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA

The Challenged Claims are obvious under *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007) because there is no gap between the hybrid SLC-MLC NAND flash system performing ordinary, necessary L2P/FTL functions and “adapted” to perform optional functions of directing data to the SLC module upon failure of a data integrity test or segregating/aggregating MLC/SLC blocks or transferring them to the SLC module for wear leveling. Starting with a Gavens NAND flash system with multiple alternative error management operations including directing data to SLC, a POSITA would be motivated to use that system compatibly with known wear leveling operations, meeting the Challenged Claim limitations directed to avoiding premature system failure.

A. Claim 1 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶ 96): Gavens (Ex. 1045), among the SanDisk portfolio and incorporating by reference others of that portfolio,¹² is a publication that discloses a complete multi-modal NAND flash system with the ordinary L2P/FTL function of its controller, a variety of error management schemes, and the capability of and compatibility for employing other known tools (disclosed in incorporated documents and exemplified in [Sechen ¶¶ 58-61]) used to avoid premature NAND system failure.

(Sechen ¶ 97): Hybrid memory systems of MLC memory modules and SLC memory modules have long availed of the endurance advantages of SLC. (*E.g.*, Lee '794 [Ex. 1041], Sutardja [Ex. 1042], and Moshayedi [Ex. 1043].) As reviewed at

¹² See, e.g., U.S. Patent No. 6,456,528 to Chen (“Chen ‘528”), Ex. 1040, incorporated by reference at Gavens 16:29-40; U.S. Patent Appl. Pub. No. 2011/0153912 (“Gorobets ‘912”), Ex. 1049, incorporated by reference at Gavens 20:53-59; U.S. Patent No. 5,930,167 to Lee et al. (“Lee ‘167”), Ex. 1050, incorporated by reference at Gavens 17:57-67; U.S. Patent Appl. Pub. No. 2010/0172180, to Paley et al. (“Paley”), Ex. 1051, incorporated by reference at Gavens 8:41-42.

[Sechen ¶ 49] and in Gavens itself (*e.g.*, 12:6-10) 2-state (pSLC) mode of MLC operation enjoys superior endurance compared to MLC in normal mode – though not as superior as “real” SLC memory which uses different circuitry. It would be obvious to a POSITA to use a “real” SLC module for the purposes contemplated in Gavens.

1. [1a] at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

(Sechen ¶¶ 100-101): Gavens memory chip 100 “includes a memory array 200 of memory cells with each cell capable of being configured as a multi-level cell (“MLC”)” (8:19-21). It may be organized in erasable blocks erased together in a “flash” operation (Fig. 6, 11:4-20). Gavens discloses element **[1a]**.

2. [1b] at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks;

(Sechen ¶ 102): Gavens discloses “[a] first portion has each memory cell storing one bit of data and [a] second portion has each memory cell storing more than one bit of data” (4:32-34, 12:6-8 [memory operating in 1-bit mode “binary” or “SLC” memory]). The first portion, “configured as lower density storage[,] . . . operates with a wider margin of error than that of the second portion” (18:16-20, also 12:6-10, 21:6-9). As explained in [Sechen ¶ 97], it would be obvious to a POSITA to substitute a “real” SLC flash memory module for Gavens’s first portion with a similar, if not wider margin of error than binary mode MLC (*see* [Sechen ¶

49]) and achieve similar, if not better, results with the same NAND flash controller Fig. 1(102) with great expectation of success. Gavens, in view of the knowledge of the POSITA's knowledge of NAND flash, discloses the obvious use in the claimed system of element **[1b]**.

3. **[1c] a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller [a] maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;**

(Sechen ¶ 103): Gavens discloses controller 102 which “cooperates with the memory chip and controls and manages high level operations” (Fig. 1(102), 8:32-33). “[O]ne or more memory chip[s] 100 [are] managed by a controller 102” (8:17-18). It would be obvious to have one or more of those NAND flash chips be “native” SLC flash chips (modules), with the controller directing host commands and data to the SLC and MLC NAND chips with their particular circuitry “to perform memory operations on the memory array 200” (8:25-29.) “A memory block management system implemented in the controller stages the sectors and maps and stores them to the physical structure of the memory array” (8:36-39.) Gavens discloses updating “a directory in a block management system embedded in the firmware of the

controller (see Fig. 1)” to direct accesses to one or the other portions of the memory (17:17-19, 18:47-49, 18:64-66). Ordinary NAND flash organization and mapping operation (*see* [Sechen ¶¶ 27-29, 33, and 34]) is explained, with “the page being a minimum unit of programming and reading” (11:9-29). (*Also* Paley [Ex. 2051] ¶¶ [0020] (“prevalent LBA interface”) and [0155]; Micheloni Fig. 18.3 [“logical-physical translation”].)

(Sechen ¶ 106): Gavens discloses the ordinary NAND controller of element [1c].

4. [1d] [b] determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

(Sechen ¶ 107): As explained in [Sechen ¶ 88], the literal reading of this function [b] (logical range fails) is absurd. Assuming that the recited test is of the data represented in the mapped physical location, there are many procedures that might be considered “data integrity tests,” including by error detection code in various error correction code processes (“ECC”), where “failure” does not disrupt ordinary user-requested operations and “end-of-life” action is taken only when the degree of failure overwhelms resources allocated to ECC. [Sechen ¶¶ 51 and 52.] Gavens discloses multiple operations for error management, most relying on ECC

and deployment near the end-of-life. [Sechen ¶¶ 53-55.] Two embodiments disclose the ‘240 Fig. 3A and 3B operation of comparing read data to original data and then remapping to SLC if there is no match, thereby satisfying the abbreviated recitation in controller function [b] of element [1d].¹³

(Sechen ¶ 108): In one variant of the Gavens post-write-read error management embodiment of Figs. 14 and 15 (explaining text at 16:13-17:42), user data is written to the higher density (*e.g.*, MLC) portion as a “first copy.” (16:41-45.) Then, in a “post write read,” there may be a check for errors “by comparison with the **original copy** which may be cached” (16:46-49 [emphasis added]). If the number of error bits is less than a predetermined amount, the first copy is deemed valid and subsequent reads of the data page will be from that copy with any errors corrected by ECC. (16:50-56.) If the number is greater, then a copy is written to the lower density, lower error rate SLC portion; this is performed in one embodiment by copying from a cached copy (“of the original data”) or in another embodiment from application of ECC to the first copy. (17:9-14.) In incorporated Paley (Ex. 2051), it was noted that “[u]sing RAM in a write cache operating with flash memory has been disclosed” (¶ [0027]); the ‘240 specification shows in Fig. 1 DRAM 20

¹³ (Sechen ¶ 110) These actions are directed by the controller and are applicable to SLC modules as well as binary mode operation of MLC.

which is where data to be written in the data integrity check apparently is first held (6:9-15). Thus, this variant discloses that stored data that fails a data integrity test against retained (cached) original data to be written causes remapping of the original data to the SLC portion.

(Sechen ¶ 109): In alternative post-write-read error management embodiments of Figs. 16 and 17 (explained at 17:43-19:24), the more robust portion is further divided into a first section for caching incoming data (simultaneously with a “first copy” written into the higher density portion) and a second section for storing rewrites from the higher density portion. (18:21-29.) In a variant, the first copy (in higher density) is compared with the cached copy in the first section of the more robust portion in the on-chip data latches (18:30-44), and if the number of error bits is greater than a threshold, then a copy is rewritten from the cached copy to the rewrite section of the more robust portion. (18:53-66.)

(Sechen ¶¶ 110, 111): Gavens, in both the variants recited, discloses the data integrity test controller function [b] of element [1d].

5. [1e] wherein the controller is further adapted to [c] determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module, and [d] maintain a count value of the blocks in the MLC non-volatile memory module determined to have received frequent writes and that are accessed most frequently on a periodic basis when the count value is a predetermined count value, transfer the contents of the counted blocks in the MLC non-volatile memory module determined to have received frequent writes after reaching the predetermined count value to the SLC non-volatile memory module and which determined blocks in the SLC are determined in accordance with the next equivalent range of physical addresses determined by the controller.

(Sechen ¶ 112): The recited “determine and segregate” controller function [c] is not tied to controller function [d)] explicitly. All that is required is that the controller is “adapted” to “determine” which of the blocks in the NAND flash system are “accessed most frequently” and which receive “frequent writes” or “infrequent writes.”

(Sechen ¶ 113): The “determination” limitation is met by Gavens’s “[t]racking the age of each block by maintaining a hot count that records the number of erase/program cycling each block has undergone” (Fig. 19(720), 20:18-21) and using that tracking to determine under whatever criteria is set (none in the ‘240 specification or claims) for “most frequently” or “frequently” or “infrequently”

accessed/written (equated by the ‘240 specification at 6:54, *see* Sechen note 52 [use of linked lists, design choice as to reference count]). It is obvious that by these counts, the physical blocks are “segregated” by whatever criteria is chosen.

As to segregation by logical blocks, the concept of dynamically allocating to SLC “hot” data and to MLC “cold” data was well known. (Sechen ¶¶ 47-49, 116, Lee ‘794 (Ex. 1041, Figs. 3, 5A, 5B, 6:58-66), Sutardja (Ex. 1042, Fig. 7(A) (506) & (508)) and Moshayedi (Ex. 1043, ¶ [0024].) Sutardja and Moshayedi also disclose wear-leveling techniques, compatible with Gavens’s late-in-life error management, that count access/writes/erases to physical blocks and transfer or move contents accordingly (Sechen ¶¶ 116-119, 125, Sutardja Fig. 7E, ¶ [0141], Moshayedi ¶ [0032]), satisfying the “transfer” controller function [d] limitation.

(Sechen ¶¶ 120, 121): The Gavens embodiments of post-write-read mapping to 2-state memory [Sechen ¶¶ 108 and 109], deployed after the physical block reaches a threshold erase/program count (Fig. 19 (730, 740), 20:21-29), satisfy the transfer after reaching a predetermined count value limitation for controller function [d]: when those blocks exceeding the threshold (receiving the most frequent writes) are written with data that fails a data integrity test, they are rewritten (transferred) to SLC. (*Also* Chen ‘528 [Ex. 1040] 10:41-60 and Paley ‘180 [Ex. 1051] ¶ [0542] [reconfiguring physical block as pseudo-SLC].) These transfer procedures meet the [1e] condition of “on a periodic basis,” as no time period is stated, but merely the

reaching of the “thresholds” exemplified in the specification and the allowance-decisive claim limitation of transfer “after “reaching the predetermined count value,” which dominates and determines any periodicity applicable.

(Sechen ¶ 125): Gavens and incorporated references (with the POSITA’s knowledge of obvious substitution of a “pure” SLC module for its partitioned and pSLC configured MLC module), in view of background knowledge of wear leveling exemplified by Sutardja, Moshayedi, and Lee ‘794 (with “pure SLC” modules, and as background processes compatible with Gavens’ error management techniques), disclose in multiple ways the “segregate” function [c] and “transfer” function [d] of element [1e].

* * * * *

(Sechen ¶ 126): Gavens, with its incorporated references, meets each limitation of claim 1 with (1) known hybrid SLC-MLC NAND flash memory module systems and its mixed SLC-mode and MLC-mode operation of MLC memory meeting elements [1a]-[1c] and (2) the POSITA’s understanding that Gavens’s extensive teachings, along with the knowledge of the POSITA of many NAND flash operations to avoid premature failure, include or render obvious the purportedly life-enhancing operational elements [1d]-[1e], including the purportedly inventive transfer “after reaching a predetermined count value” controller function [d].

B. Claims 2-5 Are Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 127-142): Claims 2-5, the system of claim 1 wherein [2] “*the MLC and SLC each comprise flash memories,*” [3] “*the MLC comprises a flash memory and the SLC comprises a resistive random access memory (RRAM),*” [4] “*the MLC comprises a flash memory and the SLC comprises a phase change memory [PCM],*” and “*the MLC comprises a flash memory and the SLC comprises a magnetic random-access memory (MAGRAM),*” are also obvious because Gavens describes a NAND flash system of multiple MLC NAND flash modules some operated in 2-level mode (Fig. 4, 9:49-50, 1:18-19, 4:14-18), where an actual SLC flash module obviously can be substituted for 2-level mode blocks (Sechen ¶¶ 97, 102), and to the extent that claims 3-5 are even enabled, they are obvious in view of background knowledge, corroborated by the Examiner’s rejection ([Sechen ¶ 78], citing Gorobets ‘179 (Ex. 1044) in view of De Ambroggi (Ex. 1053) (RRAM, PCM) or Chen ‘418 (Ex. 1054) (MRAM) and Kund (Ex. 1055) (alternative technologies having advantages over flash memory)).

C. Claim 6 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

As explained at note 9 *supra*, claim 6 is identical to claim 1 except for different statements of segregate/allocate SLC/MLC controller function [c] and transfer to SLC “after reaching predetermined count value” controller function [d] which are in

the same “adapted to” element [1e] in claim 1 and split into two “adapted to” elements [6d] and [6f] in claim 6. Thus, for claim elements [6a]-[6c] and [6e][data integrity test controller function [b], Petitioner incorporates here by reference respectively the arguments of Sections IX(A)(1)-(4) for elements [1a]-[1d]

- 1. [6d] wherein the controller [c] allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and**

Recitation in distinct element [6d] of controller function [c] “allocation” of “hot blocks” into SLC and “cold blocks” into MLC, separate from the element [1e]/[6f] construable condition of “maintaining a count value” for “segregation” of the same write-frequency defined blocks in element [1e] (Section IX(A)(5)), makes no functional difference as the counts are taught by Gavens, so that the arguments at Section IX(A)(5) apply and are incorporated here. However, this separation from the transfer controller function [d] in element [6f] shows clearly that element [6d] is anticipated by the dynamic allocation of hot and cold data (logical blocks) of Lee ‘794 (Ex. 1041, Figs. 3, 5A, 5B, 6:58-66), Sutardja (Ex. 1042, Fig. 7(A) (506) & (5089)) and Moshayedi (Ex. 1043, ¶ [0024]) (*See* Sechen ¶¶ 47-49, *but also* Sutardja Fig. 7E, ¶ [0141] and Moshayedi ¶ [0032] [counting physical blocks].)

2. [6f] wherein the controller is further adapted to [d] maintain a count value of the blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.

(Sechen ¶¶ 154-157.) Incorporated by reference are the arguments at Section IX(A)(5) for element [1e]. Element [6f] is broader than element [1e] in not being limited to MLC blocks (*compare* 7:62-63 [claim 1 count value for MLC blocks] *with* 8:50 [claim 6 count value for “those blocks”]) for “counted blocks” transferred “after reaching the predetermined count value.” As Gavens specifically tracks the age of all blocks (Sechen ¶ 113), the broader scope of element [6f] counting is disclosed by Gavens as well as by Moshayedi and Sutardja.

* * * * *

Gavens, with its incorporated references, meets each limitation of ‘240 claim 6 where (1) known hybrid SLC-MLC NAND flash memory module systems and mixed SLC-mode/MLC-mode operation of MLC memory meet elements [6a]-[6c] and (2) the POSITA’s understanding that Gavens’s extensive teachings, along with the knowledge of the many operations used to avoid premature failure, include or render obvious the purported lifetime-enhancing features of elements [6d]-[6f],

including the purportedly inventive transfer “after reaching a predetermined count value” controller function [d].

D. Claims 7-10 Are Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA.

(Sechen ¶¶ 158-165): Claims 7-10 modify the system of claim 6 exactly the same way that claims 2-5 modify the system of claim 1. Petitioner incorporates by reference the arguments of Section IX(B).

X. Ground 2: The Challenged Claims Are Obvious Over Moshayedi in View of Knowledge of the POSITA

The Challenged Claims are obvious under *KSR* because, starting with a Moshayedi’s system with multiple alternative wear leveling operations, a POSITA would be motivated to use Moshayedi with known error management operations together meeting the limitations directed to avoiding premature system failure.

A. Claim 1 Is Obvious Over Moshayedi in View of Knowledge of the POSITA.

(Sechen ¶¶ 166-167): Moshayedi (Ex. 1043) is a publication that discloses a complete hybrid NAND flash system with both MLC and SLC modules, ordinary L2P/FTL functions of a controller, a variety of wear leveling schemes, and the capability of and compatibility for employing other known tools (exemplified in [Sechen ¶ 58-61]) used to avoid premature system failure. Moshayedi, in view of the knowledge of the POSITA, discloses the limitations of claim 1:

1. [1a] at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

(Sechen ¶¶ 170-171): Moshayed, entitled, “SLC-MLC COMBINATION FLASH STORAGE DEVICE,” shows in Fig. 1 (114) four channels of “chips of flash (e.g., the first chip can be a K9K8G08 SLC flash, and the rest can be K9G8G08 MLC flash)” (¶ [0038]). Moshayed discloses the MLC module of element [1a].

2. [1b] at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks;

(Sechen ¶ 173): *See* [Sechen ¶¶ 170 and 171], which recite the use of SLC flash chips shown as Fig. 1(112), thus disclosing the SLC module of element [1b].

3. [1c] a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller [a] maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

(Sechen ¶¶ 174-175): Fig. 1 (102) shows a controller 102 coupled to the four channels of SLC and MLC chips. Paragraph [0025] explains that controller 102 “controls operations of the flash storage device 10.” Paragraph [0026] discloses controller 102 coupled to the SLC and MLC flash memory chips by an I/O bus.

Paragraph [0036] explains that the controller controls the writing and erasing of data to the channels of flash memory in the memory array.

(Sechen ¶¶ 176-177): Paragraph [0006] explains that a logical block address (LBA) is mapped to a location within a physical block in the flash memory system. Paragraphs [0036] and [0038] explain “virtual-to-physical mapping (V2P) that is standard L2P mapping for NAND flash. Paragraph [0044] explains that the system firmware assigns LBAs to the physical address. Paragraph [0037] explains that V2P RAM 214 in controller 200 (architecture of controller 102) includes one or more tables that serve to record the physical block address of a specific virtual block. Fig. 3 and paragraph [0039] show V2P entries. Moshayedi discloses the L2B controller function [a] of element [1d].

4. [1d] wherein the controller is adapted to [b] determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module; and

(Sechen ¶ 178): Paragraph [0031] discloses that “data structures or linked lists may store information about the number of data errors that have occurred in read operations corresponding to each of the data blocks” and that the information “may allow controller to select a data block from which to move dynamic data in favor of static data.” Additional information about read error relative to their frequency or

accumulation is explained. Paragraph [0033] explains that the information regarding the number of data read errors associated with a given data block may be used to determine whether the data is dynamic or static, where dynamic data may be “relocated to data blocks with less wear.” As SLC is indicated in paragraphs [0007] and [0022] to have 100 times the endurance of MLC, a POSITA would understand “blocks with less wear” to mean SLC. Moshayedi says as much at paragraph [0009], which explains that static and dynamic data are to be kept in MLC and SLC, respectively. This discloses that failures of some data integrity test on a physical block resulting in “read errors” may be relocated (moved by decoding and encoding as explained in [Sechen note 45]) to a less worn block. A POSITA would understand that an SLC block would have less wear per p-e cycle than an MLC block or be likely at the end-of-life of MLC blocks to have more life. This would align with the apparent rationale for the ‘240 patent’s Figs. 3A and 3B direction to SLC of data stored in a worn location, wear being the focus of the patent and of Gavens’s late-in-life error management.

(Sechen ¶¶ 179-180): Element [1d] (controller function [b]) not only fails to identify what is to be tested with any apparent reason but does not qualify the test as one triggered by a NAND flash operation such as a write or as a comparison to something else. If the Board does not read a comparison between stored and retained data into claim element [1d] as Phison has requested in the court proceeding [Sechen

¶ 93], Moshayedi meets its literal limitation if the recited test is applied to the data stored in the physical range of addresses. Alternatively, a POSITA seeking to avoid premature failure of a memory system would look not only to wear leveling but to known error management techniques such as those disclosed in Gavens. [Sechen ¶¶ 108 and 109.]

(Sechen ¶ 186): Moshayedi, by its error management of paragraphs [0031] and [0033], discloses or through knowledge of the POSITA of Gavens, the data integrity test controller function [b] of element [1d].

5. [1e] wherein the controller is further adapted to [c] determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module, and [d] maintain a count value of the blocks in the MLC non-volatile memory module determined to have received frequent writes and that are accessed most frequently on a periodic basis when the count value is a predetermined count value, transfer the contents of the counted blocks in the MLC non-volatile memory module determined to have received frequent writes after reaching the predetermined count value to the SLC non-volatile memory module and which determined blocks in the SLC are determined in accordance with the next equivalent range of physical addresses determined by the controller.

(Sechen ¶ 182): Moshayedi discloses that the controller determines which physical blocks in the MLC flash and the SLC flash are accessed most frequently (¶

[0009], explains that write frequency is reflected in erase frequency) by maintaining an erase count for each physical block. Additionally, Moshayedi discloses that the controller determines which logical blocks in the MLC flash and the SLC flash are written most frequently by maintaining a write count of them. Moshayedi meets both the “segregate” controller function [c] and the transfer “after reaching the predetermined count level” controller function [d], counting access/writes to logical or physical blocks.

(Sechen ¶ 183): Moshayedi discloses multiple actions in response to various use counts kept in linked lists. [Sechen ¶ 48.] Moshayedi discloses the common transfer of the “hot data” of logical blocks to the SLC module at the time of updating, where the drive

keeps track of the number of times that data for each logical block address (LBA) has been written to the flash memory, and determines whether to store newly received data associated with a particular LBA in SLC flash or in MLC flash, depending on the number of writes that have occurred for that particular LBA.

(¶ [0024].) This discloses the “segregate” controller function [c], using the logical block construction, as well as the transfer “after reaching the predetermined count value.” Also, claim 4 recites transferring the logical block from an MLC chip to an SLC chip. Fig. 3 states “This block is moved from MLC.”

(Sechen ¶ 184): Alternatively, paragraph [0030] explains that the data contained within a block with the highest erase count is swapped with data from a block with the lowest erase count.

(Sechen ¶ 185): The physical block erase count list may be used to move data between MLC flash and SLC flash in another variant of traditional wear leveling

once a block in MLC flash reaches a threshold erase count (e.g., 500), the next write operation to that block triggers a swap where the data from the MLC flash block is written to a block in SLC flash. In this manner, data for an LBA that is frequently written and causes frequent erasures is moved to SLC flash which can perform more erase cycles than MLC flash.

(¶ [0032].)

(Sechen ¶ 186): Fig. 7A (712) and paragraphs [0047] and [0060] explain that, if the erase count of an MLC block “is over a specified number (e.g., 1000),” then there is processed an MLC flash data swap to SLC flash. The purpose is to keep hot data in SLC. Fig. 8 (802), (812) and paragraphs [0049] and [0050] explain that, if an MLC block has an erase count that reaches “500,” then data in the MLC block is copied to a free block of SLC and wear leveling for MLC is performed based on erase count. These processes can be used for “segregating” data in physical blocks to meet controller function [c] or “transferring” that content to SLC “after reaching the predetermined count value.” As explained at [Sechen ¶¶ 73, 88 and 94], the

“periodic basis” characterization of transfer conflicts with NAND flash operation in random writing of data and background garbage collection, as well as with the “thresholds” exemplified in the specification and the decisive claim limitation of transfer “after “reaching the predetermined count value” (§ 81 above), which dominates and determines any periodicity applicable.

(Sechen ¶ 188): Moshayedi, under either logical or physical block construction, discloses the controller function [c] and the transfer “after reaching the predetermined count value” controller function [d], and thus element [1e].

* * * * *

(Sechen ¶ 189): Moshayedi meets each limitation of ‘240 claim 1 with (1) its known hybrid SLC-MLC NAND flash memory module systems meeting elements [1a]-[1c], (2) its disclosed “read error” process or known, compatible art meeting the “data integrity test” controller function [b] of claim element [1d], and (3) its wear leveling, under either logical or physical block construction, meeting the “segregate” controller function [c] and the purportedly inventive transfer “after reaching a predetermined count value” controller function [d] and thus claim element [1e]. Thus, claim 1 is obvious over Moshayedi in view of knowledge of the POSITA.

B. Claims 2-5 Are Obvious Over Moshayedi in View of Knowledge of the POSITA.

(Sechen ¶¶ 190-204): Claims 2-5, the system of claim 1 wherein [2] “*the MLC and SLC each comprise flash memories,*” [3] “*the MLC comprises a flash memory*

and the SLC comprises a resistive random access memory (RRAM),” [4] “the MLC comprises a flash memory and the SLC comprises a phase change memory [PCM],” and “the MLC comprises a flash memory and the SLC comprises a magnetic random-access memory (MAGRAM),” are also obvious because Moshayedi recites the use of MLC flash chips (Fig. 1(114)) and SLC flash chips (Fig. 1(112)) (Sechen ¶¶ 170, 171 and 173), and to the extent that claims 3-5 are even enabled, they are obvious in view of background knowledge, corroborated by the Examiner’s rejection ([Sechen ¶ 78], citing Gorobets ‘179 (Ex. 1044) in view of De Ambroggi (Ex. 1053) (RRAM, PCM) or Chen ’418 (Ex. 1054) (MRAM) and Kund (Ex. 1055) (alternative technologies having advantages over flash memory)).

C. Claim 6 Is Obvious Over Moshayedi in View of Knowledge of the POSITA.

As explained at note 9 *supra*, claim 6 is identical to claim 1 except for different statements of segregate/allocate SLC/MLC controller function [c] and transfer to SLC “after reaching predetermined count value” controller function [d] which are in the same “adapted to” element [1e] in claim 1 and split into two “adapted to” elements [6d] and [6f] in claim 6. Thus, for claim elements [6a]-[6c] and [6e][data integrity test controller function [b], Petitioner incorporates here respectively the arguments of Sections X(A)(1)-(4) for elements [1a]-[1d]].

1. **[6d] wherein the controller [c] allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and**

Recitation in distinct element [6d] of controller function [c] “allocation” of “hot blocks” into SLC and “cold blocks” into MLC, separate from the element [1e]/[6f] construable condition of “maintaining a count value” for “segregation” of the same write-frequency defined blocks in element [1e] (Section X (A)(5)), makes no functional difference as the counts are taught by Moshayedi, so that the arguments at Section X(A)(5) apply and are incorporated here. However, this separation from the transfer controller function [d] in element [6f] shows clearly that element [6d] is anticipated by the dynamic allocation of hot and cold data (logical blocks) of Lee ‘794 (Ex. 1041, Figs. 3, 5A, 5B, 6:58-66), Sutardja (Ex. 1042, Fig. 7(A) (506) & (5089)) and Moshayedi (Ex. 1043, ¶ [0024]) (*See* Sechen ¶¶ 47-49, *but also* Sutardja Fig. 7E, ¶ [0141] and Moshayedi ¶ [0032] [counting physical blocks].)

2. [6f] wherein the controller is further adapted to [d] maintain a count value of the blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.

(Sechen ¶¶ 154-157.) Incorporated by reference are the arguments at Section X(A)(5) for element [1e]. Element [6f] is broader than element [1e] in not being limited to MLC blocks (*compare* 7:62-63 [claim 1 count value for MLC blocks] *with* 8:50 [claim 6 count value for “those blocks”]) for “counted blocks” transferred “after reaching the predetermined count value.” As Moshayedi discloses the use of linked lists for tracking a variety of block uses for all blocks (*see* Section X(A)(5)), the broader scope of element [6f] counting is disclosed by Moshayedi.

* * * * *

Moshayedi meets each limitation of ‘240 claim 6 with (1) its hybrid SLC-MLC NAND flash memory module systems meeting elements [6a]-[6c], (2) its disclosed “read error” process or known, compatible art meeting the “data integrity test” controller function [b] of claim element [6e], and (3) its wear leveling embodiments meeting, under either logical or physical block construction, the “segregate” controller function [c] and the purportedly inventive transfer “after reaching a predetermined count value” controller function [d] and thus claim

elements [6d] and [6f]. Thus, claim 1 is obvious over Moshayedi in view of knowledge of the POSITA.

D. Claims 7-10 Are Obvious Over Moshayedi in View of Knowledge of the POSITA.

(Sechen ¶¶ 219-226): Claims 7-10 modify, the system of claim 6 the same way that claims 2-5 modify the system of claim 1. Petitioner incorporates by reference the arguments of Section X(B).

XI. Ground 3: The Challenged Claims Are Obvious Over Sutardja in View of Knowledge of the POSITA

The Challenged Claims are obvious under *KSR* because, starting with Sutardja's (Ex. 1042) NAND flash system with multiple alternative wear leveling operations including directing data to SLC, a POSITA would be motivated to use that system compatibly with error management operations together meeting the Challenged Claim limitations directed to avoiding premature system failure.

A. Claim 1 Is Obvious Over Sutardja in View of Knowledge of the POSITA.

(Sechen ¶¶ 227-229): Sutardja is a published reference that discloses a complete hybrid NAND flash system using MLC and SLC modules, with the ordinary L2P/FTL function of its controller, a variety of wear leveling schemes, and the capability of and compatibility for employing other known tools (exemplified in [Sechen ¶¶ 58-61]) used to avoid premature NAND system failure. Sutardja, in view of the knowledge of the POSITA, discloses the limitations recited in claim 1:

1. [1a] at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

(Sechen ¶¶ 231-233) Sutardja, entitled “HYBRID NON-VOLATILE SOLID STATE MEMORY SYSTEM,” shows at Fig. 2 shows a First Solid-State Nonvolatile Memory (“NVM”) 204 and a Second Solid-State NVM 206. Paragraph [0108] explains that memories 204 and 206 “may include single-level cell (SLC) flash memory or multi-level cell (MLC) flash memory”. Claim 37 discloses a single-level cell (SLC) flash memory and a multi-level cell (MLC) flash memory. As well-known to the POSITA, a flash memory includes many blocks, and the individually erasable block is the defining portion of NAND “flash” (*see* [Sechen ¶ 28], Sutardja ¶ [0157] [block is a group of memory cells erased together].) A POSITA would understand from paragraph [0106] that the first NVM may be MLC flash memory modules. Sutardja discloses the MLC module of element [1a].

2. [1b] at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks;

(Sechen ¶ 234-235): *See* [Sechen ¶ 231], which recites the use of SLC flash memory, which may be included in the second memory. A POSITA would understand from paragraph [0106] that the second NVM may be an SLC module. Sutardja discloses the claimed SLC module of element [1b].

3. **[1c] a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller [a] maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;**

(Sechen ¶¶ 255-257): Fig. 3 shows a controller 252 that is coupled to both the first NVM 204 and the second NVM 206. Paragraph [118] explains this coupling as communication. Paragraph [0009] explains, in the generic (prior art) SSD system that controller 102 “reads or writes data to the flash memory 104.”

(Sechen ¶¶ 237-238): Sutardja uses NAND flash standard L2P mapping (see [Sechen ¶¶ 32-34]) as corroborated by disclosure of that mapping in its wear leveling and other features. (*E.g.*, Abs., ¶ [0107] [map logical addresses corresponding to data to physical addresses]). A POSITA would understand that Sutardja’s various modules use the basic NAND flash system of L2P mapping. Sutardja discloses controller function [a] of element **[1d]**.

4. [1d] wherein the controller is adapted to [b] determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

(Sechen ¶ 239): Sutardja Figs. 5 (406) and 7D, ¶¶ [0134]-[0139] and [0151], disclose a “degradation” test of a physical location (range of physical addresses). Fig. 7D and paragraph [0151] explain the test as writing data to that location, reading back the data, writing the data to that location a second time (after a predetermined time), reading back the data a second time, then comparing the data read back the first time and the data read back the second time, resulting in a “degradation value” for that physical address. The values that show degradation (failing that data integrity test) allow estimation of the maximum life cycle for a block used for the wear leveling processes to “normalize” wear. A POSITA understands that such normalization is the wear leveling to avoid failure of one portion of the memory ahead of others. Paragraph [0139] discloses that using the number of write cycles remaining (from the estimated maximum), the wear leveling process may assign all new writes to another one of the memories than the one which is approaching the end of its useful life. Paragraph [0135] discloses periodically testing the first, lesser write cycle lifetime (MLC) NVM, so that paragraph [0139] would call for remapping to the second, greater write cycle lifetime (SLC) NVM if the test on the MLC

location has “failed” by having high degradation values. The degradation test thus is used with multiple Sutardja wear leveling processes directed to avoiding failure of some physical memory locations ahead of others.

(Sechen ¶ 240): Starting from that objective of Sutardja, it would be obvious to a POSITA to use other known tools to avoid premature failure [e.g., Sechen ¶¶ 58-61]. These tools include other end-of-life mitigations such as the known error management techniques disclosed in Gavens, including two post-write-read error-management embodiments that themselves satisfy element [1d] (Sechen ¶¶ 108 and 109). Those processes are compatible with Sutardja’s Figs. 7A-8; for example, Gavens’s post-write-read direction to SLC can be fit after Sutardja Fig. 7A (510).

(Sechen ¶ 241): Sutardja’s degradation test of paragraphs [0134]-[0139] and [0151], discloses, or applying knowledge of the POSITA makes obvious the data integrity test controller function [b] of element **[1d]**.

5. [1e] wherein the controller is further adapted to [c] determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module, and [d] maintain a count value of the blocks in the MLC non-volatile memory module determined to have received frequent writes and that are accessed most frequently on a periodic basis when the count value is a predetermined count value, transfer the contents of the counted blocks in the MLC non-volatile memory module determined to have received frequent writes after reaching the predetermined count value to the SLC non-volatile memory module and which determined blocks in the SLC are determined in accordance with the next equivalent range of physical addresses determined by the controller.

Sutardja discloses multiple wear leveling schemes for non-volatile memory (“NVM”) systems, which include (1) dynamically biasing (segregating/allocating) writing of data with logical addresses differentiated (segregated/allocated) by relative write frequencies (§ [0013][first group more frequent than second]) to physical addresses differentiated by relative wear (ratio of historical writes to expected “write cycle lifetime” (§§ [0010], [0012])), including between first high-density NVM of 10K write cycle usable lifetime (like MLC) and second lower density (single bit per storage cell) NVM of 100K write cycles (like SLC) (§§ [0006], [0011]) and (2) at appropriate times (background or predetermined), “move” (§§ [0126][ordinary static data wear leveling, *compare* ‘240 3:27-31, Sechen ¶ 35])

[0132][one memory full], [0166][to free a block for incoming write that may be dynamically biased, [0167][remapping by swapping], [0168][end-of-life]].

(Sechen ¶¶ 242-245): Satisfying element [1e]’s “determine” and “segregate” controller function [c] relative to physical blocks, Sutardja Fig. 3 (260) and paragraphs [0110]-[0111] and [0121] disclose that wear leveling module 260 tracks the number times the write and/or erase operations are performed on each physical block in the first and second NVMs 204 (MLC) and 206 (SLC). Satisfying the controller function [c] under a logical block construction, Sutardja Fig. 4A (306) and paragraph [0129] discloses that the write monitoring module 306 tracks the logical addresses to which data is frequently written by measuring frequencies at which data is written to the logical addresses. (*Also* Fig. 4B (356), ¶ [0113] [write mapping module determines actual write frequencies of logical addresses]; Fig. 7A (504) and (512), ¶¶ [0146], [0147] [receive write frequencies for logical addresses from the host and measure actual write frequencies]; Fig. 8 (604) and (612), ¶¶ [0155], [0156].) (Sechen ¶ 247): Sutardja discloses operation of a hybrid MLC-SLC NAND flash system in a “flow” diagram (Figs. 7A-7E) that has several branches (Figs. 7B-7E) determining whether it is “[t]ime to perform” certain analyses (Fig. 7B [514][“data shift analysis”], [516][“degradation analysis”] and [518][“wear analysis”]). The base algorithm is shown in Fig. 7A: step 504 (“Receive Write Frequencies For Logical Addresses From Host”), step 506 (“Map Logical Addresses

With Low Write Frequencies To First Memory”], step 508 (“Map Logical Addresses With High Write Frequencies To Second Memory”), and step 510 (“Write Data According To Mapping”). This base algorithm, without the branches, is the known biased mapping and writing of data, with transfer directed to SLC memory of the data of the most frequently written LBAs (“hot data” of logical blocks) [Sechen ¶¶ 46-48, 58 and 60]. Paragraph [0146] discloses the controller mapping the logical addresses having write frequencies greater than a predetermined threshold to the second NVM (SLC).

(Sechen ¶¶ 246, 248): For the “data shift” branch, Fig. 7C (520), (522) and paragraph [0149] disclose determining if the number of write operations to the first block of the first NVM (MLC) during a predetermined time is greater than the predetermined threshold, then the logical addresses that correspond to the first block of the first NVM (MLC) are mapped to a second block of the second NVM (SLC). This is an example of a time “periodic basis” recited in element [1e]

In the degradation analysis branch, Fig. 7D, reviewed at Section XI(A)(5), also conducted on a time periodic basis, remaps (and subsequently writes) data mapped to a physical location found to exceed a degradation value that is a proxy for wear level (writes/expected write cycle life) also satisfies the transfer to SLC “on a periodic basis” and “after reaching the predetermined count value” controller function [d] limitation.

(Sechen ¶ 249): In the “wear leveling” branch, Fig. 7E (550) and paragraph [0153] disclose determining if the wear level of the first NVM (MLC) is greater than a predetermined threshold, and if so, mapping all logical blocks to physical blocks of the second NVM (SLC). Paragraph [0128] discloses that the wear leveling module also biases mapping to the more robust memory of data in the less robust memory when the write operations exceed a predetermined threshold.

Both dynamic biased writing and “move” operations (¶¶ [0126], [0132], and [0166]-[0168]), in conjunction with the recited wear thresholds and periodic bases, satisfy the controller function [d] recitation of “transfer” of “content” of the “counted block [logical or physical]” controller function [d]. While remapping may involve the next write to the logical address, paragraph [0167] discloses remapping of periodically determined “relatively frequent rewritten logical addresses to blocks with low wear levels [as that ratio for SLC blocks likely would be]” and that “[r]emapping may involve swapping data in two blocks.” That concept of swapping is known and explained, for example, in the wear leveling techniques disclosed at Moshayedi (Ex. 1043) paragraphs [0029], [0030], and [0032] [*see* Sechen ¶¶ 48, 73, note 45 {transfer}], Sutardja paragraph [0168] also discloses transfer of data in blocks that have “surpassed their write cycle lifetime.” (Sechen ¶ 251.)

(Sechen ¶¶ 250-255): Sutardja discloses more types of counting and transfer, and thus, under either the logical or physical block construction, discloses the

“segregate” controller function [c] and the transfer “after reaching the predetermined count value” controller function [d] required by claim element [1e].

* * * * *

(Sechen ¶ 256): Sutardja meets each limitation of ‘240 claim 1 with (1) its known hybrid SLC-MLC NAND flash memory module systems meeting elements [1a]-[1c], (2) its disclosed “degradation test” process or known, compatible art meeting the “data integrity test” controller function [b] of claim element [1d], and (3) its wear leveling embodiments, under either logical or physical block construction, meeting the “segregate” controller function [c] and the purportedly inventive transfer “after reaching a predetermined count value” controller function [d] and thus claim element [1e]. Thus, claim 1 is obvious over Sutardja in view of knowledge of the POSITA.

B. Claims 2-5 Are Obvious Over Sutardja in View of Knowledge of the POSITA.

(Sechen ¶¶ 257-271): Claims 2-5, the system of claim 1 wherein [2] “*the MLC and SLC each comprise flash memories,*” [3] “*the MLC comprises a flash memory and the SLC comprises a resistive random access memory (RRAM),*” [4] “*the MLC comprises a flash memory and the SLC comprises a phase change memory [PCM],*” and “*the MLC comprises a flash memory and the SLC comprises a magnetic random-access memory (MAGRAM),*” are also obvious because Sutardja recites the use of “multi-level cell (MLC) flash memory” and “single-level cell (SLC) flash

memory” (Sutardja ¶ [0108], Claim 37, Sechen ¶¶ 231, 232 and 234), and to the extent that claims 3-5 are even enabled, they are obvious in view of background knowledge, corroborated by the Examiner’s rejection ([Sechen ¶ 78], citing Gorobets ‘179 (Ex. 1044) in view of De Ambroggi (Ex. 1053) (RRAM, PCM) or Chen ’418 (Ex. 1054) (MRAM) and Kund (Ex. 1055) (alternative technologies having advantages over flash memory)).)

C. Claim 6 Is Obvious Over Sutardja in View of Knowledge of the POSITA.

As explained at note 9 *supra*, claim 6 is identical to claim 1 except for different statements of segregate/allocate SLC/MLC controller function [c] and transfer to SLC “after reaching predetermined count value” controller function [d] which are in the same “adapted to” element [1e] in claim 1 and split into two “adapted to” elements [6d] and [6f] in claim 6. Thus, for claim elements [6a]-[6c] and [6e][data integrity test controller function [b], Petitioner incorporates here by reference respectively the arguments of Sections XI(A)(1)-(4) for elements [1a]-[1d].)

- 1. [6d] wherein the controller [c] allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and**

Recitation in distinct element [6d] of controller function [c] “allocation” of “hot blocks” into SLC and “cold blocks” into MLC, separate from the element [1e]/[6f] construable condition of “maintaining a count value” for “segregation” of

the same write-frequency defined blocks in element [1e] (Section XI(A)(5) *supra*), makes no functional difference as the counts are taught by Sutardja, so that the arguments at Section XI(A)(5) apply and are incorporated here. However, this separation from the transfer controller function [d] in element [6f] shows clearly that element [6d] is anticipated by the dynamic allocation of hot and cold data (logical blocks) of Lee ‘794 (Ex. 1041, Figs. 3, 5A, 5B, 6:58-66), Sutardja (Ex. 1042, Fig. 7(A) (506) & (5089)) and Moshayedi (Ex. 1043, ¶ [0024]) (*See* Sechen ¶¶ 47-49, *but also* Sutardja Fig. 7E, ¶ [0141] and Moshayedi ¶ [0032] [counting physical blocks].)

2. [6f] wherein the controller is further adapted to [d] maintain a count value of the blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.

(Sechen ¶¶ 283-284.) Incorporated here are the arguments at Section XI(A)(5) for element [1e]. Element [6f] is broader than element [1e] as not limited to MLC blocks (*compare* 7:62-63 [claim 1 count value for MLC blocks] *with* 8:50 [claim 6 count value for “those blocks”]) for “counted blocks” transferred “after reaching the predetermined count value.” As Sutardja discloses tracking of a variety

of block uses for all blocks (*see* Section XI(A)(5)), the broader scope of element [6f] counting is disclosed by Sutardja.

* * * * *

Sutardja meets each limitation of ‘240 claim 6 with (1) its hybrid SLC-MLC NAND flash memory module systems meeting elements [6a]-[6c], (2) its disclosed “degradation test” process or known, compatible art meeting the “data integrity test” controller function [b] of claim element [6e], and (3) its wear leveling embodiments meeting, under either logical or physical block construction, the “segregate” controller function [c] and the purportedly inventive transfer “after reaching a predetermined count value” controller function [d] and thus claim elements [6d] and [6f]. Thus, claim 1 is obvious over Sutardja in view of knowledge of the POSITA.

D. Claims 7-10 Are Obvious Over Sutardja in View of Knowledge of the POSITA.

(Sechen ¶¶ 286-293): Claims 6-10 modify the system of claim 6 exactly the same way that claims 2-5 modify the system of claim 1. Petitioner incorporates by reference the arguments of Section XI(B).

XII. THE PENDING LITIGATIONS IN THE WESTERN DISTRICT OF TEXAS DO NOT WARRANT DENYING INSTITUTION.

With eight current patents asserted by Vervain against Phison based on varying word claims to the same two “data integrity test” and “wear leveling” functions described in the same specification for a known hybrid SLC-MLC NAND

flash memory, review by this Board is more appropriate than by the District Court where those word variations can escape scrutiny. Construction of the multiple terms of the eight patents are restricted in number (12) in the District Court (per “side” in related cases as present here), even counting contentions of indefiniteness. As demonstrated in the above-stated grounds (Sections IX-XI), the case against this patent is compelling. Balancing of the six factors set forth by the Board in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential) does not warrant denying institution here. Rather, institution would best serve the interest in “system efficiency, fairness, and patent quality” (*id.* at 5), allowing due resolution of the substantial patentability questions (*id.* at 15).

As to *Fintiv* Factor 5, the petitioner and defendant in the parallel proceeding are the same party. Phison filed this petition expeditiously, where it received first notice of Vervain’s assertion in the Complaint filed March 8, 2024, and the Amended Complaint filed May 13, 2024 (Ex. 1082). No substantive opinions have issued regarding the scope or validity of the Challenged Claims. The parallel proceeding is in an early stage: the Court recently granted-in-part Phison’s motion to dismiss (*see* Docket List [Ex. 1080] entries 12, 24, 26 and 38), Phison has not otherwise answered, fact discovery has not yet proceeded beyond automatic disclosure and Phison’s invalidity and subject-matter eligibility contentions were filed on August 16, 2024, and claim construction materials exchanged in accordance

with the Scheduling Order (Ex. 1083). A *Markman* hearing, initially scheduled for December 5, 2024, is postponed until January 9, 2025. ([Ex. 1080] entry 39) Thus, as to Factor 3, there has not been overriding investment in the parallel proceeding; to the contrary, the requirements of the parallel proceeding limited Markman construction to twelve terms between the parties for eight patents of verbal variations of the same specification. Thus, as to Factor 4, there is overlap, in the greater inclusiveness of the requested review as the District Court will not consider all the issues properly raised in this Petition, pending PGR2024-00047, PGR2024-00048, and IPR2025-00212, and others that Petitioner may petition.

Factors 1 and 2 do not significantly weigh for or against instituting the requested IGR. Petitioner does not know if the District Court will stay the case if trial by this Board is instituted and the Court has *tentatively* set jury selection for December 15, 2025 (Scheduling Order [Ex. 1083] at 4).

Regarding the sixth factor, the merits strongly weigh in favor of instituting trial as shown through the strength of the grounds in this Petition. “Other circumstances” favor institution. As described at note 3 *supra*, there are separate suits by Patent Owner Vervain (following the same template) against Phison and a customer (Kingston Docket List [Ex. 1081]). This presents the complexity of eight patents with method and apparatus claims that Vervain asserts against multiple, sometimes competing products (that thus must be held confidential between the

defendants) that implicate third-party actors who may be implicated in divided or indirect infringement as users who select the configuration or performance of the claimed system. Moreover, unlike Phison, its customer defendant in the other case moved to dismiss for improper venue and to transfer (Kingston Docket List [Ex. 1081] entries 13 and 20) with attendant discovery and confidentiality proceedings (*id.* entries 15 and 16).

The interest of the public in cleaning away such verbal variants of questionable innovation in the eight Vervain patents are best served by the requested review. The Board may take notice that such litigation, if it reaches trial, will have been drastically reduced in claims and theories asserted – beginning with the limitation of terms for construction for eight patents. An IPR trial, in contrast, may resolve all Challenged Claims of a patent, substantially simplifying district court trial without the extensive district court discovery for which the America Invents Act offered this alternative before the Board. And, of course, Petitioner has shown its case to be compelling.

XIII. CONCLUSION

Petitioner submits that for the reasons set forth above, it has been shown that more likely than not, the Challenged Claims are invalid under all of 35 U.S.C. § 103 and should reviewed by the Board and canceled.

Petition for *Inter Partes* Review of U.S. Patent No. 9,997,240

Date: December 6, 2024

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CERTIFICATION OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above-captioned Petition for *Inter Partes* Review of U.S. Patent No. 9,997,240 (and accompanying exhibits), was served in its entirety on December 6, 2024, upon Patent Owner's correspondent of record via USPS Priority Mail:

*Patent owner's correspondent
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CERTIFICATION OF WORD COUNT (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the attached Petition, including footnotes, but not the cover page, exhibit list, table of contents, mandatory notices, and certifications, contains 13,438 words, as measured by the Word Count function of Microsoft Word. This is less than the limit of 14,000 words as specified by 37 C.F.R. § 42.24(a)(i).

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