

A 128K Flash EEPROM Using Double-Polysilicon Technology

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Abstract—A highly manufacturable 128K flash EEPROM was developed based on a new cell. Programming is achieved through hot-electron injection and erasing through electron tunneling from the floating gate to the drain. The cell is 20 percent larger than an EPROM cell and contains an integral series transistor which ensures self-limited erasing, reduces leakage, and increases the cell current. The flash EEPROM device can withstand thousands of program/erase cycles. Endurance failures are due to threshold window closing caused by electron trapping in the gate oxide. Typical erase time is 1 s to clear the entire memory.

I. INTRODUCTION

THE EPROM, when introduced in the mid-70's, was perceived as a tool for system prototyping before a design is committed to ROM. But the EPROM became widely used in mass-produced systems and today it is the second largest memory market, second only to the DRAM. An important reason for EPROM's popularity is its small cell size and hence high density and low cost. The cell is a single MOS transistor structure with a double-polysilicon gate. The cell is programmed by channel hot-electron injection. It is programmed only when both drain and gate are raised to high voltages. Therefore X - Y addressing of a cell in an array is simple and no byte select transistors are required.

One shortcoming of the EPROM is that its ceramic package with a quartz window adds significantly to the cost. One-time-programmable (OTP) EPROM's packaged in plastic packages do not have this cost problem, but cannot be fully tested after assembly.

The floating-gate tunneling oxide (FLOTOX) EEPROM technology was introduced as an improved EPROM. The advantage of EEPROM over EPROM is significant system flexibility due to on-board programming and erasing and high endurance [1]. The disadvantage is its large cell size. The EEPROM cell relies on the Fowler-Nordheim tunneling mechanism for both programming and erasing. A separate select transistor per cell is needed when implemented in a memory array. Because of this, the FLOTOX cell size is two to three times the size of an EPROM cell

[1]–[3]. Other EEPROM technologies are available but all have drawbacks besides the cell size disadvantage [4]. MNOS EEPROM's have limited data storage time. Textured-poly EEPROM's require triple-poly technology and high internal programming voltage.

Flash EEPROM technology offers nearly the same cell size as EPROM and provides electrical erasability. It can be housed in an inexpensive plastic package and still be fully tested. "Flash" refers to the fact that the entire memory array, or at least a large block of it, is erased at the same time during the erase operation. It is not possible to erase only a single byte. Small cell size is achieved through the use of channel hot-electron injection for programming, like EPROM's. Erasing is accomplished by Fowler-Nordheim tunneling.

Different flash EEPROM cell concepts have been proposed [5]–[7] but none has been successfully implemented in a flash EEPROM product until now.

This paper describes a flash EEPROM device based on a new cell structure [8] that combines the strengths of previously investigated cell concepts. The cell size is small and shrinkable and the operation is reliable. A 128K flash EEPROM has been designed, tested, and transferred to production. The device is highly manufacturable.

II. CELL STRUCTURE

Fig. 1 shows a drawing and an SEM photograph of the cross section of the new flash EEPROM. As shown on the figure, the first- (lower) level polysilicon is the floating gate. The second-level polysilicon forms the control gates and the word lines in an array. One edge of each gate is etched with a self-aligned etching process. The diffusion adjacent to the floating gate is the drain. The gate oxide thickness is around 200 Å. The dielectric between the polysilicon gates is an oxide-nitride-oxide (ONO) stack with a capacitive equivalent oxide thickness of 450 Å. ONO has low leakage current and low defect density, providing superior charge retention performance. Devices reported in this paper have about 2- μ m effective channel length.

Cell layout is shown in Fig. 2. The cell can be thought of as two transistors in series. One is a floating-gate memory transistor, similar to an EPROM cell. The other is a simple

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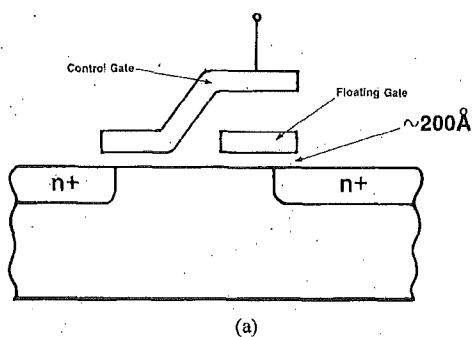


Fig. 1. (a) Cross section of the flash EEPROM cell. (b) SEM cross section.

enhancement transistor controlled by the control gate, i.e., the word line. Unlike ultraviolet (UV) light erasing, electrical erasing is not self-limiting. Electrical erasing can (and usually does) leave the floating gate positively charged, thus turning the memory transistor into a depletion-mode transistor. The series enhancement transistor is needed to prevent current flow under this condition.

Due to the presence of the series enhancement transistor, the control gate is wider in a flash EEPROM cell than in an EPROM cell. For this reason, this flash EEPROM cell size is about 20 percent larger than the size of an EPROM cell for the same set of design rules and is scalable as shown in Fig. 3.

III. CELL PERFORMANCE

The purpose of the series enhancement transistor in this flash EEPROM cell is to prevent the leakage current in a memory array during programming and/or reading caused by an overerased cell. This structure eliminates the need for adaptive erasing [7], which may be difficult to implement in a high-density memory.

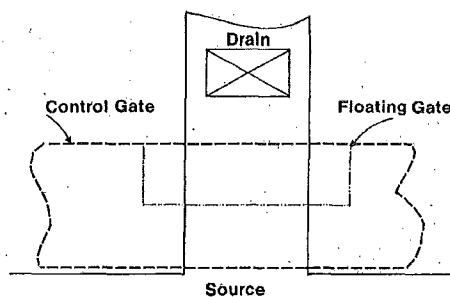


Fig. 2. Layout of the flash EEPROM cell.

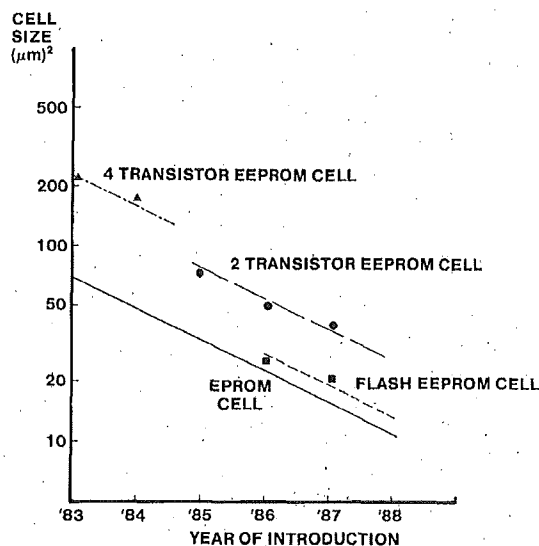


Fig. 3. Scaling trends of the flash EEPROM cell, in comparison to other EPROM and EEPROM cells.

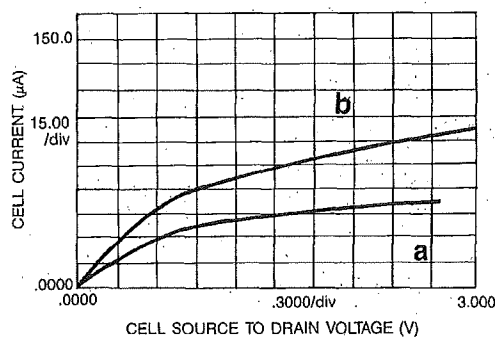


Fig. 4. Drain current versus drain voltage of the flash EEPROM cell (a) after UV erase, and (b) after electrical erase. The gate voltage is 3.5 V for both characteristics.

The extra cell size added by the series enhancement transistor in Fig. 1 can also be justified on the basis of improved cell current and programming characteristics even without considering the benefit of electrical erasability. The improvement is a result of the high gain of the series transistor and the shorter floating gate length that

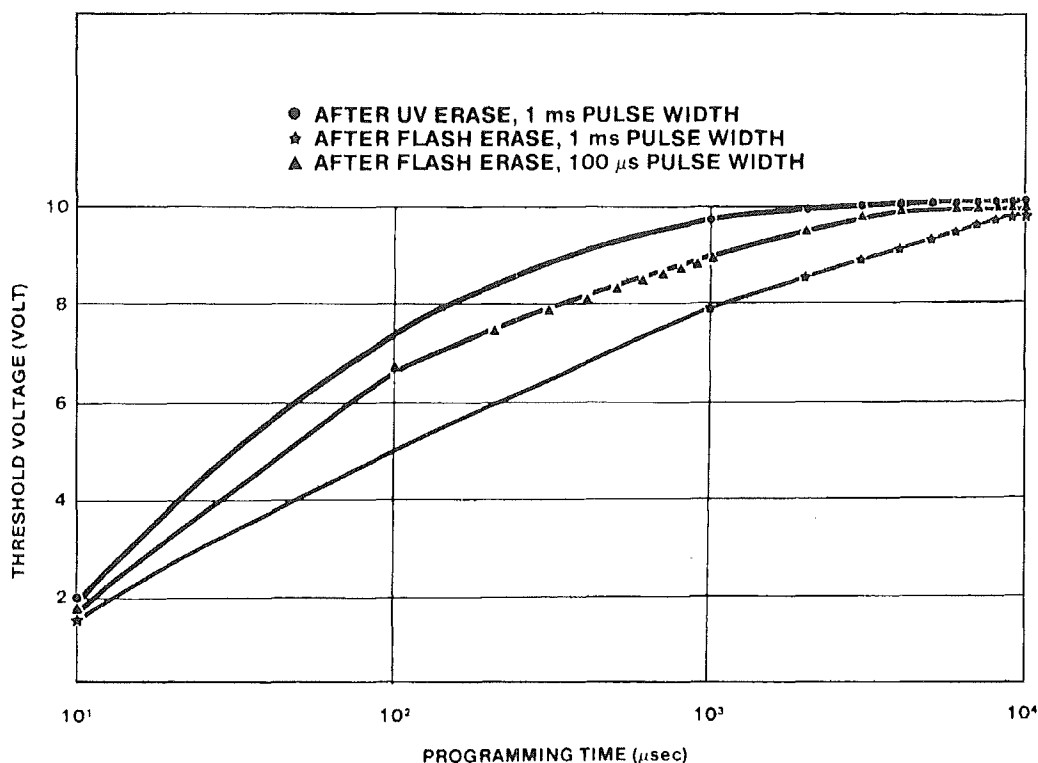


Fig. 5. Programming characteristic of the flash EEPROM cell with different programming algorithms. The gate and drain voltages during programming are 16 and 9 V, respectively.

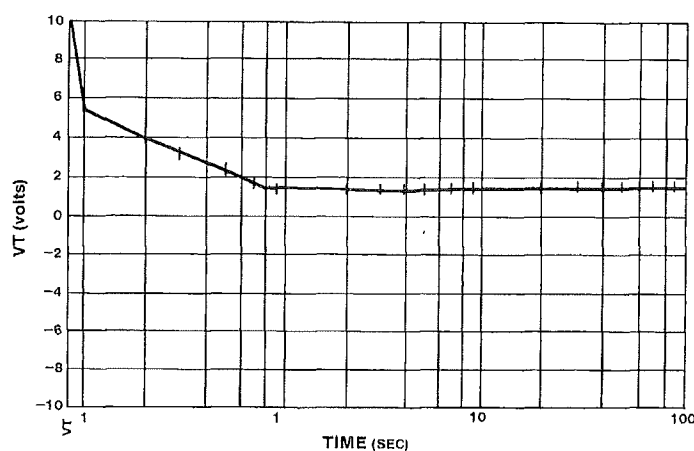


Fig. 6. Erase characteristic of the flash EEPROM cell. The drain is at 19 V and the source and the gate are grounded.

can be used without causing current leakage due to punchthrough. The read current improvement in an electrically erased cell is even greater (about 60 percent higher than an EPROM cell for the same design rules) due to the positive charge on the floating gate. The difference in cell current after UV and electrical erasures is shown in Fig. 4.

A fresh flash EEPROM cell can be programmed at a speed comparable to an EPROM cell. It is known, however, that the initial programming rate dV_T/dt deteriorates

after an electrical erase [5]. This is attributed to the positive charge on the floating gate which causes the maximum rate of hot-electron injection to occur at a lower control gate voltage than before the electrical erase. Previously proposed solutions were to increase the drain voltage [5] or dope the channel heavily [9]. Instead of one long programming pulse, many shorter 100- μ s pulses are used in this EEPROM so that efficient hot-electron injection can take place in periods of lower gate voltage during the word-line

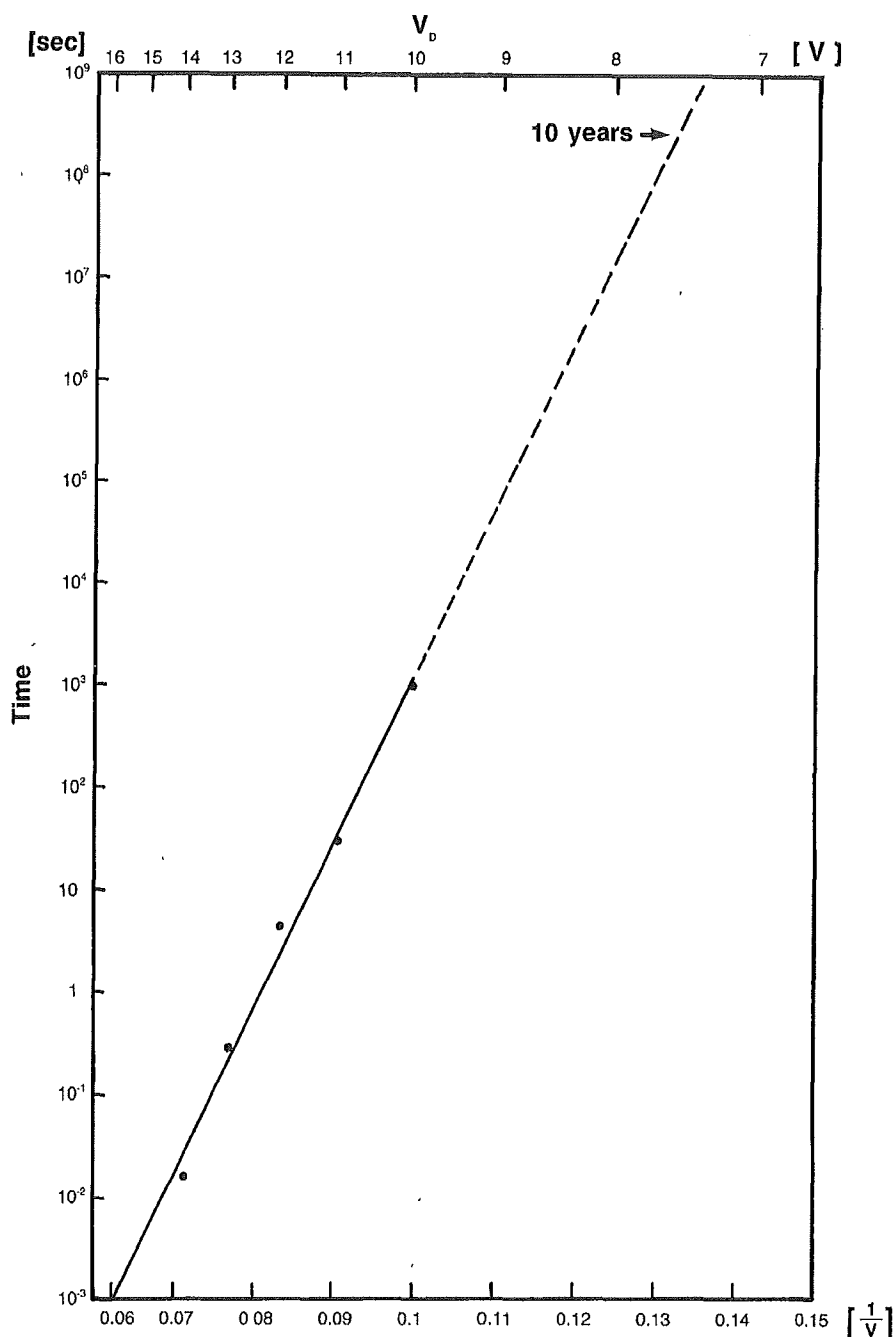


Fig. 7. Read disturb characteristic of flash EEPROM cell.

ramp-up. Fig. 5 shows the programming characteristic of the flash EEPROM cell with different programming algorithms.

Erasing is the result of Fowler–Nordheim tunneling of electrons from the floating gate to the drain diffusion. Erasing is completed in about 1 s with 19 V applied to the drain as shown in Fig. 6. Further erasing only increases the positive charge on the floating gate and V_T remains at the threshold of the series enhancement transistor. The initial

seemingly very rapid drop of V_T in Fig. 6 is an artifact of data presentation as $t = 0$ cannot be represented on the logarithmic time scale.

Read disturb is examined in Fig. 7. During read, a small voltage is applied to the drain and one must ensure that data are not disturbed by slow “erasing” over a long period of time. Fig. 7 plots the time it takes for V_T to decrease by 0.5 V. A read disturb time of longer than ten years can easily be achieved at 2-V reading voltage.

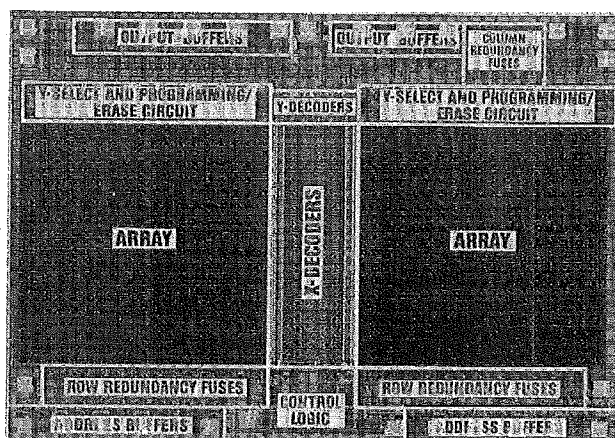


Fig. 8. Chip photomicrograph of the 128K flash EEPROM.

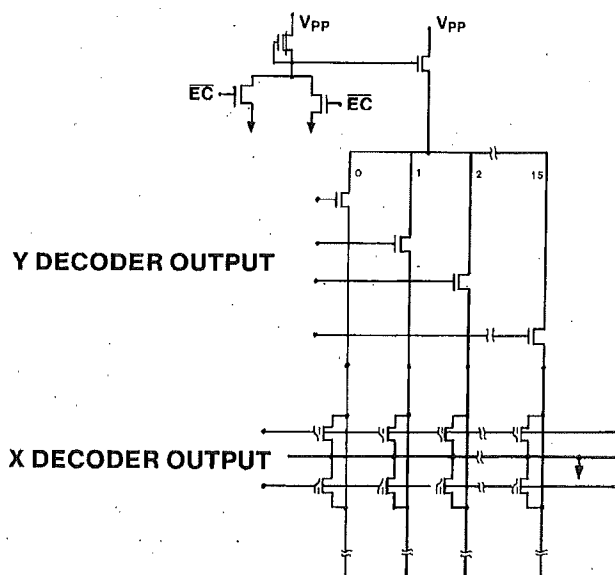


Fig. 9. Erase control circuit of the 128K EEPROM.

IV. CIRCUIT DESIGN

A 128K flash EEPROM has been designed, tested, and transferred to production. The circuit design was derived from a production 128K EPROM and utilizes most of the peripheral circuit layout of the original EPROM. Thus, the cell size ($43 \mu\text{m}^2$) and chip size ($4.6 \times 3.4 \text{ mm}^2$) are identical to those of earlier EPROM's using $2.5\text{-}\mu\text{m}$ NMOS technology. The gate oxide thickness in the peripheral circuit is $600 \text{ \AA}$. A die photograph is shown in Fig. 8. The pinout is compatible with the 128K EPROM.

The flash EEPROM requires a 21-V power supply for programming and erasing. Erasing is accomplished by applying high voltage to all of the bit lines through an erase control circuit shown in Fig. 9. During flash erase, the erase control signal $\overline{\text{EC}}$ is low, all Y-decoder outputs are high, and all X-decoder outputs are low. About 19 V are applied to the bit lines. The erase time is below 1 s (Fig. 6) to clear the entire memory.

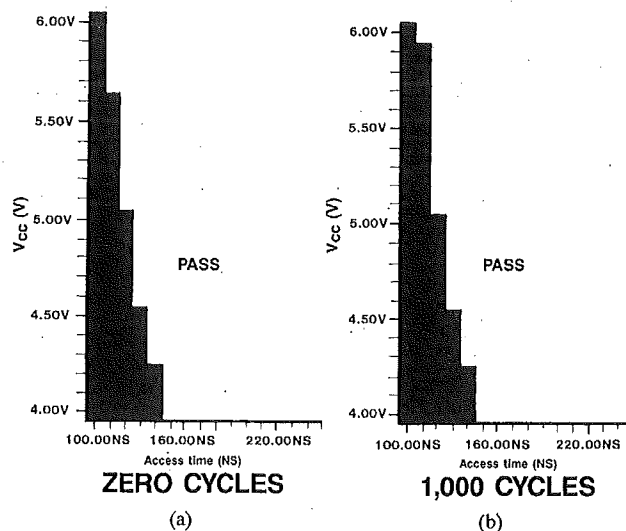
Fig. 10. Access time versus V_{cc} for the 128K flash EEPROM at room temperature: (a) before cycling and (b) after 1000 program/erase cycles.

TABLE I
 V_{cc} MARGIN VERSUS NUMBER OF PROGRAM/ERASE CYCLES
FOR THE 128K FLASH EEPROM

CYCLE	1	10	100	200	500	1000	2500	5000
V_{cc} MAX (volts)	9	9	9	9	8.4	7.5	6.4	5.6
V_{cc} MIN (volts)	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6

This flash EEPROM has a typical access time of 140 ns as shown in Fig. 10 and an excellent speed distribution as a result of the large cell current (Fig. 4). The manufacturing yield is comparable to its EPROM counterpart.

V. PROGRAM/ERASE ENDURANCE

The 128K flash EEPROM can withstand thousands of program/erase cycles. The wearout mode is a decrease in V_{cc} margin as shown in Table I (9 V in Table I is a tester limit). Speed is not degraded until the V_{cc} margin fails as shown in Fig. 10.

The wearout mechanism is believed to be electron trapping in the gate oxide near the drain. Electrons may be trapped in the oxide on their way to the floating gate during programming. The density of trapped electrons increases with increasing program/erase cycles. Trapped electrons induce a field that slows down the programming speed, thus causing a gradual reduction of V_T after programming as illustrated in Fig. 11. The rate of V_T reduction in this cell is comparable to that observed when erasing was achieved by tunneling between the polysilicon gates [5]. This suggests that the high field in the gate oxide during erasing does not significantly increase the rate of V_T window closing. One may suspect that electron trapping takes place in UVEPROM's to a comparable degree.

Fig. 12 illustrates two facts. First, useful program/erase cycles can be increased simply by increasing the initial V_T after programming. Fig. 12(a) shows that quite a large V_T

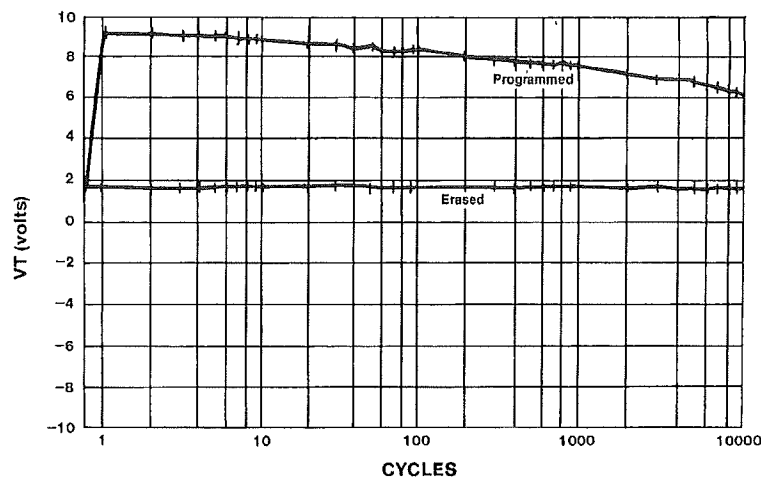


Fig. 11. The program/erase characteristic of a single flash EEPROM cell.

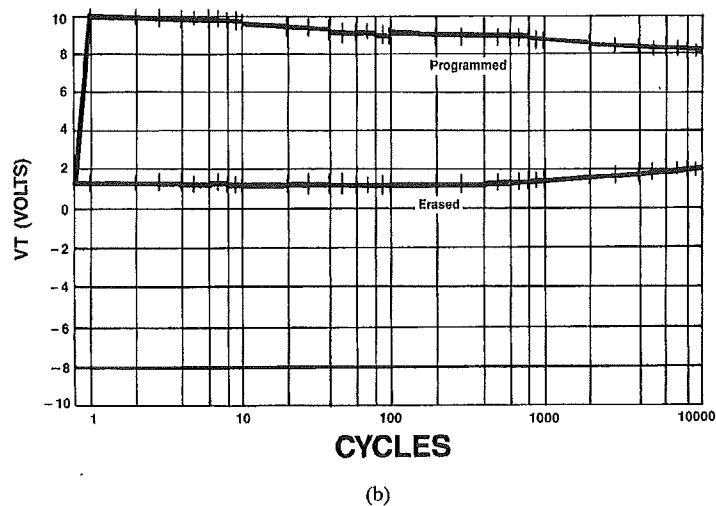
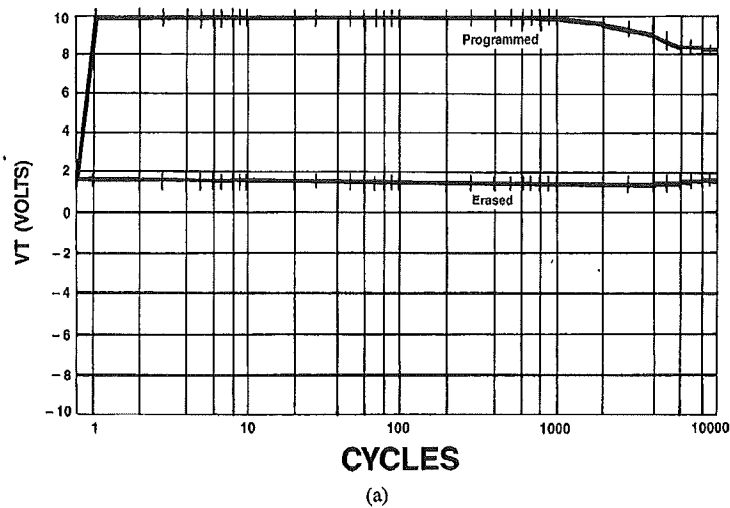


Fig. 12. (a) Endurance characteristic of a fresh cell. (b) Endurance characteristic of the same cell as in (a) after it was cycled for 10 000 program/erase cycles and baked at 350°C for 5 h in N₂.

window is still available at 10 000 cycles because of an increased initial V_T . $V_T = 10$ V is a tester limit. Second, the V_T window can be restored by a 350°C bake, further supporting the electron trapping model. After 10 000 cycles, the cell was baked at 350°C for 5 h in nitrogen ambient. Afterwards it was cycled again and the results are plotted in Fig. 12(b). V_T was raised from 8 V before the bake to over 10 V after the bake.

VI. RETENTION

128K flash EEPROM devices were baked at 250°C for 1000 h in the programmed state. The voltage margin of the cells was measured before and after bake. No drop in voltage margin was found for experiments done on fresh devices or on devices cycled for 1000 cycles. These results confirm the good quality of the oxides as grown and also show that the high quality and integrity of oxides is preserved after a certain number of cycles.

VII. CONCLUSION

A 128K flash EEPROM has been developed and reported. The essence of this development is a simple and reliable cell design. The integral select transistor in series with the floating-gate transistor makes the cell about 20 percent larger than an EPROM cell for the same design rule. This transistor eliminates the need for adaptive erasing, greatly reduces the leakage current during programming and/or read, and increases the cell read current. The result is a highly manufacturable flash EEPROM with a die size comparable to that of an EPROM.

The problem of slow programming of electrically erased cells was overcome by using a pulse programming scheme. Advanced gate oxide technology makes reliable erasing possible through Fowler-Nordheim tunneling of electrons from the floating gate to the drain. The erase time is less than 1 s. Electron trapping in gate oxide occurs during hot-electron-injection programming. This causes the threshold window to close. The 128K flash EEPROM can withstand thousands of program/erase cycles.

Compared with EPROM's, this flash EEPROM technology offers higher erase speed, in-system reprogrammability, and potentially lower cost due to reduced testing and package costs. Compared with one-time-programmable EPROM, this flash EEPROM technology offers reprogrammability and full testability after assembly.

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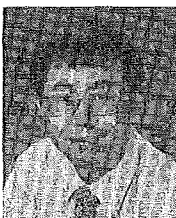
From 1960 to 1981 he was with the Polytechnical Institute of Bucharest, Semiconductor Devices and Integrated Circuits Department as an Assistant Professor (1960-1967), Associate Professor (1967-1977), and Professor (1977-1981).

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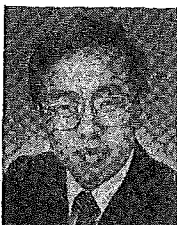
After two years of military service he joined Simon Electron Company in Taiwan as a designer of Hi-Fi systems in 1974. He joined SEEQ Technology, Inc., San Jose, CA, in 1984 where he was engaged in failure analysis of EPROM memories. In 1985 he joined the group in charge of the development of flash EEPROM's. He is currently involved in flash cell circuit design and

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Dr. Hu is a former recipient of the General Telephone and Electronics Fellowship and the University of California Science Fellowship. He has been awarded several U.S. and international patents on semiconductor devices and technology. He is Associate Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES. He has authored or coauthored one book and over 140 research journal articles.