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APPLICATION NUMBER: 14/525,411
FILING DATE: *October 28, 2014*
PATENT NUMBER: 9196385
ISSUE DATE: *November 24, 2015*



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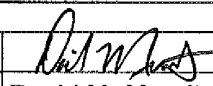
Kathi

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UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>	Attorney Docket No.	0299-0004.02
	First Named Inventor	G.R. Mohan Rao
	Title	IMPROVED LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM
	Express Mail Label No.	

APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents.</i>	Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
1. ☐ Fee Transmittal Form (PTO/SB/17 or equivalent) 2. ☒ Applicant asserts small entity status. See 37 CFR 1.27 3. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent. 4. ☒ Specification <i>[Total Pages 18]</i> Both the claims and abstract must start on a new page. <i>(See MPEP § 608.01(a) for information on the preferred arrangement)</i> 5. ☒ Drawing(s) (35 U.S.C. 113) <i>[Total Sheets 5]</i> 6. ☒ Inventor's Oath or Declaration <i>[Total Pages 2]</i> <i>(Including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))</i> a. ☒ Newly executed (original or copy) b. ☐ A copy from a prior application (37 CFR 1.63(d)) 7. ☒ Application Data Sheet * See note below. See 37 CFR 1.76 (PTO/AIA/14 or equivalent) 8. ☐ CD-ROM or CD-R In duplicate, large table, or Computer Program <i>(Appendix)</i> ☐ Landscape Table on CD 9. Nucleotide and/or Amino Acid Sequence Submission <i>(If applicable, Items a. - c. are required)</i> a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ADDRESS TO: ACCOMPANYING APPLICATION PAPERS 10. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee _____ 11. ☐ 37 CFR 3.73(c) Statement ☒ Power of Attorney <i>(when there is an assignee)</i> 12. ☐ English Translation Document <i>(If applicable)</i> 13. ☐ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached 14. ☐ Preliminary Amendment 15. ☐ Return Receipt Postcard <i>(MPEP § 503) (Should be specifically itemized)</i> 16. ☐ Certified Copy of Priority Document(s) <i>(If foreign priority is claimed)</i> 17. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 18. ☐ Other: _____

*Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 must be included in an Application Data Sheet (ADS).
 (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

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Name (Print/Type) David M. Mundt			October 28, 2014		
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IMPROVED LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Inventor: G. R. Mohan Rao

CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application is a Non-Provisional Patent Application, claiming priority under 35 U.S.C. §119(e) to U.S. Provisional Application Serial No. 61/509,257, entitled "Improved Lifetime Mixed Level NAND Flash System," filed July 19, 2011, the complete disclosure thereof being incorporated herein by reference. This application also incorporates by reference the complete disclosure of United States Pat. No. 7,855,916, entitled "Nonvolatile Memory Systems with Embedded Fast Read and Write Memories," filed on October 22, 2008 by inventor G.R. Mohan Rao, and issued on December 21, 2010. This application also incorporates by reference the complete disclosure of United States Pat. Appl. No. 12/915,177, entitled "Nonvolatile Memory Systems with Embedded Fast Read and Write Memories," filed on October 29, 2010 (US 2011/0060870 A1) by inventor G.R. Mohan Rao.

TECHNICAL FIELD

[002] This application relates to a system and method for providing reliable storage through the use of non-volatile memories and, more particularly, to a system and method of increasing the reliability and lifetime of a NAND

flash storage system, module, or chip through the use of a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage without substantially raising the cost of the NAND flash storage system. The memory in a total non-volatile memory system may contain some SRAM (static random-access memory), DRAM (dynamic RAM), RRAM (resistive RAM), PCM (phase change memory), MAGRAM (magnetic random-access memory), NAND flash, and one or more HDDs (hard disk drives) when storage of the order of several terabytes is required. The SLC non-volatile memory can be flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

BACKGROUND OF THE DISCLOSURE

[003] Non-volatile memories provide long-term storage of data. More particularly, non-volatile memories can retain the stored data even when not powered. Magnetic (rotating) hard disk drives (HDD) dominate this storage medium due to lower cost compared to solid state disks (SSD). Optical (rotating) disks, tape drives and others have a smaller role in long-term storage systems. SSDs are preferred for their superior performance (fast access time), mechanical reliability and ruggedness, and portability. Flash memory, more specifically NAND flash, is the dominant SSD medium today.

[004] RRAM, PCM, MAGRAM and others, will likely play a larger role in the future, each of them having their own advantages and disadvantages. They

may ultimately replace flash memories, initially for use as a “write buffer” and later to replace “SLC flash” and “MLC flash.” MLC NAND flash is a flash memory technology using multiple levels per cell to allow more bits to be stored using the same number of transistors. In SLC NAND flash technology, each cell can exist in one of two states, storing one bit of information per cell. Most MLC NAND flash memory has four possible states per cell, so it can store two bits of information per cell.

[005] These semiconductor technology driven “flash alternatives,” i.e., RRAM, PCM, MAGRAM and others, have several advantages over any (SLC or MLC) flash because they: 1) allow data to be written over existing data (without prior erase of existing data), 2) allow for an erase of individual bytes or pages (instead of having to erase an entire block), and 3) possess superior endurance (1,000,000 write-erase cycles compared to typical 100,000 cycles for SLC flash and less than 10,000 cycles for MLC flash).

[006] HDDs have several platters. Each platter contains 250-5,000 tracks (concentric circles). Each track contains 64 to 256 sectors. Each sector contains 512 bytes of data and has a unique “physical (memory) address.” A plurality of sectors is typically combined to form a “logical block” having a unique “logical address.” This logical address is the address at which the logical block of physical sectors appears to reside from the perspective of an executing application program. The size of each logical block and its logical address (and/or address ranges/ boundaries) is optimized for the particular operating system (OS) and software applications executed by the host processor. A computer OS organizes data as “files.” Each file may be located

(stored) in either a single logical block or a plurality of logical blocks, and therefore, the location of files typically traverses the boundaries of individual (physical) sectors. Sometimes, a plurality of files has to be combined and/or modified, which poses an enormous challenge for the memory controller device of a non-volatile memory system.

[007] SSDs are slowly encroaching on the HDD space and the vast majority of NAND flash in enterprise servers utilizes a SLC architecture, which further comprises a NAND flash controller and a flash translation layer (FTL). NAND flash devices are generally fragmented into a number of identically sized blocks, each of which is further segmented into some number of pages. It should be noted that asymmetrical block sizes, as well as page sizes, are also acceptable within a device or a module containing devices. For example, a block may comprise 32 to 64 pages, each of which incorporates 2 - 4 Kbit of memory. In addition, the process of writing data to a NAND flash memory device is complicated by the fact that, during normal operation of, for example, single-level storage (SLC), erased bits (usually all bits in a block with the value of '1') can only be changed to the opposite state (usually '0') once before the entire block must be erased. Blocks can only be erased in their entirety, and, when erased, are usually written to '1' bits. However, if an erased block is already there, and if the addresses (block, page, etc.) are allowed, data can be written immediately; if not, a block has to be erased before it can be written to.

[008] FTL is the driver that works in conjunction with an existing operating system (or, in some embedded applications, as the operating system) to

make linear flash memory appear to the system like a disk drive, i.e., it emulates a HDD. This is achieved by creating “virtual” small blocks of data, or sectors, out of flash’s large erase blocks and managing data on the flash so that it appears to be “write in place” when in fact it is being stored in different locations in the flash. FTL further manages the flash so that there are clean/erased places to store data.

[009] Given the limited number of writes that individual blocks within flash devices can tolerate, wear leveling algorithms are used within the flash devices (as firmware commonly known as FTL or managed by a controller) to attempt to ensure that “hot” blocks, i.e., blocks that are frequently written, are not rendered unusable much faster than other blocks. This task is usually performed within a flash translation layer. In most cases, the controller maintains a lookup table to translate the memory array physical block address (PBA) to the logical block address (LBA) used by the host system. The controller’s wear-leveling algorithm determines which physical block to use each time data is programmed, eliminating the relevance of the physical location of data and enabling data to be stored anywhere within the memory array and thus prolonging the service life of the flash memory. Depending on the wear-leveling method used, the controller typically either writes to the available erased block with the lowest erase count (dynamic wear leveling); or it selects an available target block with the lowest overall erase count, erases the block if necessary, writes new data to the block, and ensures that blocks of static data are moved when their block erase count is below a certain threshold (static wear leveling).

[0010] MLC NAND flash SSDs are slowly replacing and/or coexisting with SLC NAND flash in newer SSD systems. MLC allows a single cell to store multiple bits, and accordingly, to assume more than two values; i.e., '0' or '1'. Most MLC NAND flash architectures allow up to four (4) values per cell; i.e., '00', '01', '10', or '11'. Generally, MLC NAND flash enjoys greater density than SLC NAND flash, at the cost of a decrease in access speed and lifetime (endurance). It should be noted, however, that even SLC NAND flash has a considerably lower lifetime (endurance) than rotating magnetic media (e.g., HDDs), being able to withstand only between 50,000 and 100,000 writes, and MLC NAND flash has a much lower lifetime (endurance) than SLC NAND flash, being able to withstand only between 3,000 and 10,000 writes. As is well known in the art, any "write" or "program" to a block in NAND flash (floating gate) requires an "erase" (of a block) before "write."

[0011] Despite its limitations, there are a number of applications that lend themselves to the use of MLC flash. Generally, MLC flash is used in applications where data is read many times (but written few times) and physical size is an issue. For example, flash memory cards for use in digital cameras would be a good application of MLC flash, as MLC can provide higher density memory at lower cost than SLC memory.

[0012] When a non-volatile storage system combines HDD, SLC and MLC (setting aside volatile memory for buffering, caching etc) in a single (hybrid) system, new improvements and solutions are required to manage the methods of writing data optimally for improved life time (endurance) of flash memory. Accordingly, various embodiments of a NAND flash storage system

that provides long lifetime (endurance) storage at low cost are described herein.

[0013] The following description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present disclosure is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

SUMMARY OF THE DISCLOSURE

[0014] According to one embodiment of the present disclosure, there is provided a system for storing data which comprises at least one MLC non-volatile memory module (hereinafter referred to as “MLC module”) and at least one SLC non-volatile memory module (hereinafter referred to as “SLC module”), each module comprises a plurality of individually erasable blocks. The data storage system according to one embodiment of the present disclosure further comprises a controller for controlling both the at least one MLC module and the at least one SLC module. In particular, the controller maintains an address map comprising a list of individual logical address ranges each of which maps to a similar range of physical addresses within either the at least one MLC module or the at least one SLC module. After each write to (flash) memory, the controller conducts a data integrity check

to ensure that the data was written correctly. When the data was not written correctly, the controller modifies the table so that the range of addresses on which the write failed is remapped to the next available range of physical addresses within the at least one SLC module. The SLC module can be (NAND) flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

[0015] According to another embodiment of the present disclosure, there is provided a system for storing data which comprises a controller that is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC non-volatile module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The present disclosure will be more fully understood by reference to the following detailed description of one or more preferred embodiments when read in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout the views and in which:

[0017] FIG. 1 is a block diagram of a computer system incorporating one embodiment of the present disclosure;

[0018] FIG. 2 is a drawing depicting a translation table/address map in accordance with one embodiment of the present disclosure;

[0019] FIGS. 3a and 3b are a flow chart illustrating an exemplary method for use in implementing one embodiment of the present disclosure; and

[0020] FIG. 4 is a block diagram depicting one embodiment of the present disclosure for implementation within a NAND flash module.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

[0021] The present disclosure is directed to the reliable storage of data in read and write memory, and, in particular, to the reliable storage of data in non-volatile memory, such as, for example, NAND flash. Generally, and in particular regard to NAND flash memory, two separate banks of NAND flash are maintained by a controller. One bank contains economical MLC NAND flash, while a second bank contains high endurance SLC NAND flash. The controller conducts a data integrity test after every write. If a particular address range fails a data integrity test, the address range is remapped from MLC NAND flash to SLC NAND flash. As the SLC NAND flash is used to boost the lifetime (endurance) of the storage system, it can be considerably lesser in amount than the MLC NAND flash. For example, a system may set SLC NAND flash equal to 12.5% or 25% of MLC NAND flash (total non-volatile memory storage space = MLC + SLC).

[0022] Turning to the Figures and to Figure 1 in particular, a computer system 10 depicting one embodiment of the present disclosure is shown. A processor 12 is coupled to a device controller 14, such as a chipset, using a

data link well known in the art, such as a parallel bus or packet-based link. The device controller 14 provides interface functions to the processor 12. In some computer systems, the device controller 14 may be an integral part of the (host) processor 12. The device controller 14 provides a number of input/output ports 16 and 18, such as, for example, serial ports (e.g., USB ports and Firewire ports) and network ports (e.g., Ethernet ports and 802.11 “Wi-Fi” ports). The device controller 14 may also control a bank of, for example, DRAM 20. In addition, the device controller 14 controls access to one or more disks 24, such as, for example, a rotating magnetic disk, or an optical disk, as well as two or more types of NAND flash memory. One type of NAND flash memory is a MLC NAND flash memory module 26. Another type of NAND flash memory is a SLC NAND flash memory module 28.

[0023] The device controller 14 maintains a translation table/address map which may include address translations for all devices in the computer system. Nonetheless, the discussion in the present disclosure will be limited only to NAND flash memory modules. In particular, the device controller 14 maintains a translation table that maps logical computer system addresses to physical addresses in each one of the MLC- and SLC- NAND flash memory modules 26 and 28, respectively. As MLC flash memory is less expensive than SLC flash memory, on a cost per bit basis, the translation table will initially map all logical NAND flash addresses to the MLC NAND flash memory module 26. The address ranges within the translation table will assume some minimum quantum, such as, for example, one block, although

a smaller size, such as one page could be used, if the NAND flash has the capability of erasing the smaller size quantum.

[0024] A “read-modify-write” scheme is used to write data to the NAND flash. Data to be written to NAND flash is maintained in DRAM 20. After each write to an address within a particular address range, the device controller 14 will – as time permits – perform a read on the address range to ensure the integrity of the written data. If a data integrity test fails, the address range is remapped from the MLC NAND flash memory module 26 to the next available address range in the SLC NAND flash memory module 28.

[0025] Figure 2 illustrates one embodiment of a translation table/address map of the present disclosure. In Figure 2a, a list of logical address ranges (R0-RN) is translated to physical address ranges. As illustrated, all of the logical address ranges are translated to blocks on the MLC NAND flash memory module 26. However, through the application of a data integrity verification check (explained in more detail below) it is determined that, for example, address range R2 corresponds to failed quanta of data stored in block 2 of the MLC NAND flash memory module 26. Figure 2b shows the quanta of data which failed the data integrity verification check (see Figure 2a) remapped to the next available range of physical addresses within the SLC NAND flash memory module 28, in this example, SLC/ block 0.

[0026] Figures 3a and 3b are a flow chart illustrating a method for utilizing a NAND flash memory system incorporating one embodiment of the present disclosure. The method begins in a step 100, when a command to write a quantum of data stored in DRAM to a particular location in NAND flash

memory is received. In step 102, the quantum of data is read from DRAM into memory within the device controller (which acts as the memory controller). In step 104, both the logical address range and the NAND flash physical address range to which the quantum of data is to be written, is read into memory of the device controller. In step 106, the quantum of data to be written is combined with the contents of the NAND flash memory. In step 108, the NAND flash physical address range to be written is erased. In step 110, the combined data is written to the appropriate NAND flash physical address range. In step 112 the NAND flash physical address range that was written in step 110 is read into device controller memory.

[0027] The flowchart continues in Figure 3b. In step 114 the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical address range and the quantum of data to be written. In step 116, if the retained data matches the newly stored data in the NAND flash memory, the write was a success, and the method exits in step 118. However, if the retained data does not match the newly stored data in the NAND flash memory, the method executes step 120, which identifies the next quantum of available SLC NAND flash memory addresses. In step 122, a check is made to determine if additional SLC NAND flash memory is available, and, if not, the NAND flash memory system is marked as failed, prompting a system alert step 124. However, if additional SLC NAND flash memory is available, the failed NAND flash physical address range is remapped to the next available quantum of SLC NAND flash

memory in step 126. Execution then returns to step 110, where the write is repeated.

[0028] Another application of one embodiment of the present disclosure, not depicted in any of the drawings, is to allocate “hot” blocks; i.e., those blocks that receive frequent writes, into the SLC NAND flash memory module 28, while allocating “cold” blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26. This could be accomplished within the device controller 14 described above, which could simply maintain a count of those blocks that are accessed (written to) most frequently, and, on a periodic basis, such as, for example, every 1000 writes, or every 10,000 writes, transfer the contents of those blocks into the SLC NAND flash memory module 28.

[0029] Figure 4 depicts another embodiment of the present disclosure. The embodiment is entirely resident within a NAND flash module 50. In particular, a standard NAND flash interface 52 is managed by flash translation layer (FTL) logic 54. The flash translation layer (FTL) 54 manages two NAND flash memory banks 56 and 58, whereby memory bank 56 comprises a plurality of MLC NAND flash memory modules 60a and a plurality of SLC NAND flash memory modules 62a. Memory bank 58 comprises a plurality of MLC NAND flash memory modules 60b and a plurality of SLC NAND flash memory modules 62b.

[0030] This embodiment of the present disclosure could function similarly to the system level embodiment discussed earlier with reference to Figures 1 - 3b, but the control functions, such as maintenance of the translation

table/address map (Figure 2), could be conducted within the flash translation layer (FTL) 54 instead of in a device controller 14.

[0031] Embodiments of the present disclosure relate to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of multi-level cell (MLC) and single-level cell (SLC) NAND flash storage. The above description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. While this disclosure contains descriptions with reference to certain illustrative aspects, it will be understood that these descriptions shall not be construed in a limiting sense. Rather, various changes and modifications can be made to the illustrative embodiments without departing from the true spirit, central characteristics and scope of the disclosure, including those combinations of features that are individually disclosed or claimed herein. Furthermore, it will be appreciated that any such changes and modifications will be recognized by those skilled in the art as an equivalent to one or more elements of the following claims, and shall be covered by such claims to the fullest extent permitted by law.

Claims

What is claimed is:

1. A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module; and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module.

2. The system of claim 1, wherein the minimal quanta of addresses is equal to one block.
3. The system of claim 1, wherein the minimal quanta of addresses is equal to one page.
4. The system of claim 1, wherein the MLC non-volatile memory module is NAND flash memory.
5. The system of claim 1, wherein the SLC non-volatile memory module is NAND flash memory.
6. The system of claim 1, wherein the MLC non-volatile memory module is resistive random-access memory (RRAM).
7. The system of claim 1, wherein the SLC non-volatile memory module is resistive random-access memory (RRAM).
8. The system of claim 1, wherein the MLC non-volatile memory module is phase change memory (PCM).
9. The system of claim 1, wherein the SLC non-volatile memory module is phase change memory (PCM).

10. The system of claim 1, wherein the SLC non-volatile memory module is magnetic random-access memory (MAGRAM).
11. The system of claim 1, wherein the controller is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller allocates those blocks that receive the most frequent writes to the at least one SLC non-volatile memory module.
12. The system of claim 11, wherein the controller determines which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of said blocks is accessed.
13. The system of claim 12, wherein the controller allocates those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.
14. The system of claim 13, wherein the controller causes the transfer of content on a periodic basis.

ABSTRACT

[0032] A flash controller for managing at least one MLC non-volatile memory module and at least one SLC non-volatile memory module. The flash controller is adapted to determine if a range of addresses listed by an entry and mapped to said at least one MLC non-volatile memory module fails a data integrity test. In the event of such a failure, the controller remaps said entry to an equivalent range of addresses of said at least one SLC non-volatile memory module. The flash controller is further adapted to determine which of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and allocating those blocks that receive frequent writes to the SLC non-volatile memory module and those blocks that receive infrequent writes to the MLC non-volatile memory module.

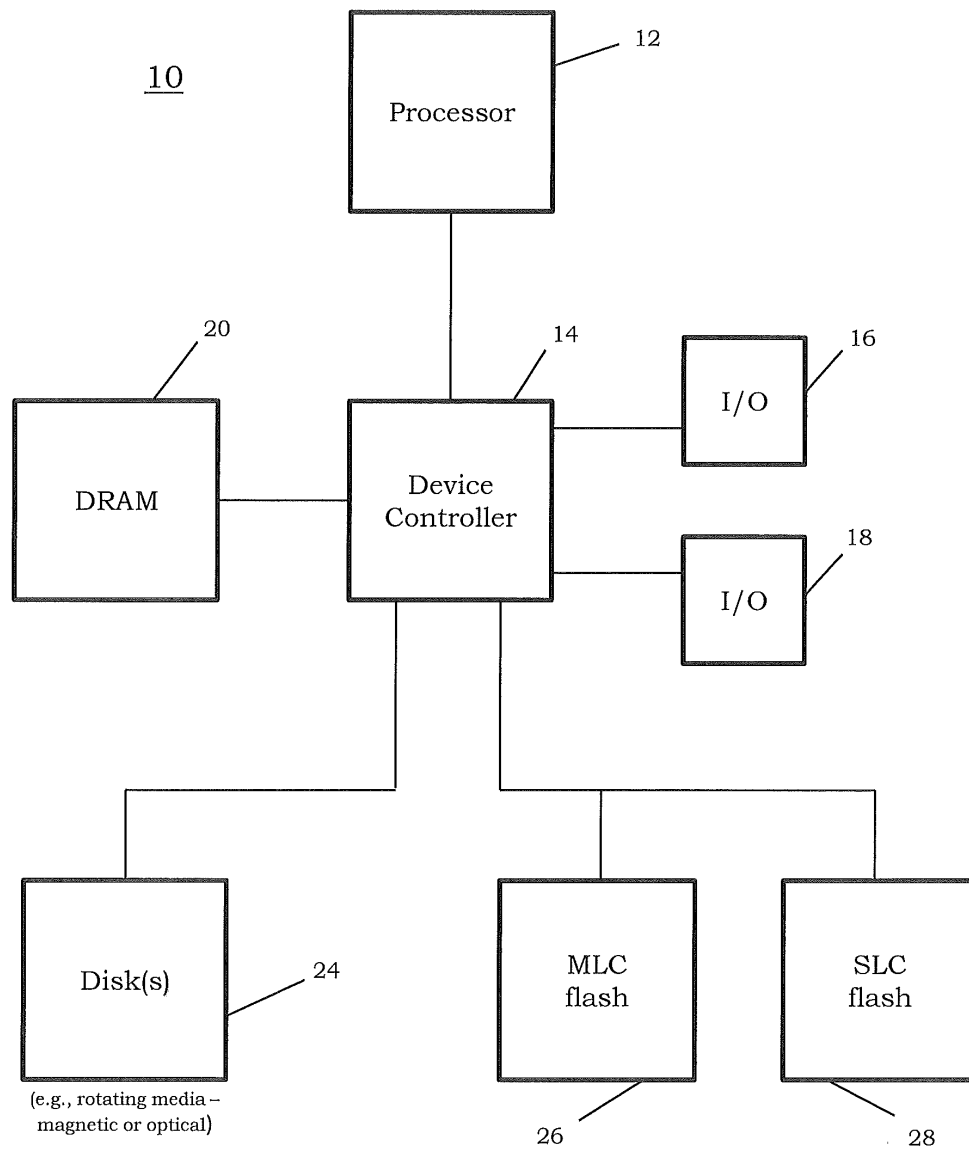


FIG. 1

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	MLC/Block 2
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

Failed Data Integrity Test →

FIG. 2a

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	SLC/Block 0
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

Remapping to SLC flash module →

FIG. 2b

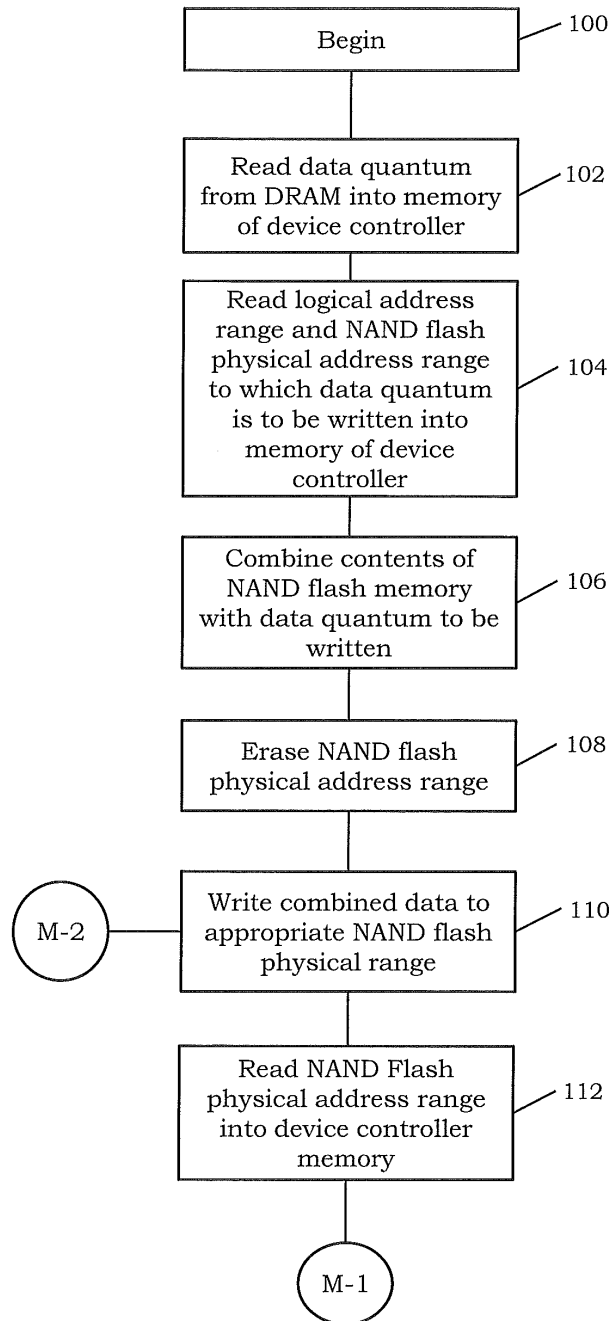


FIG. 3a

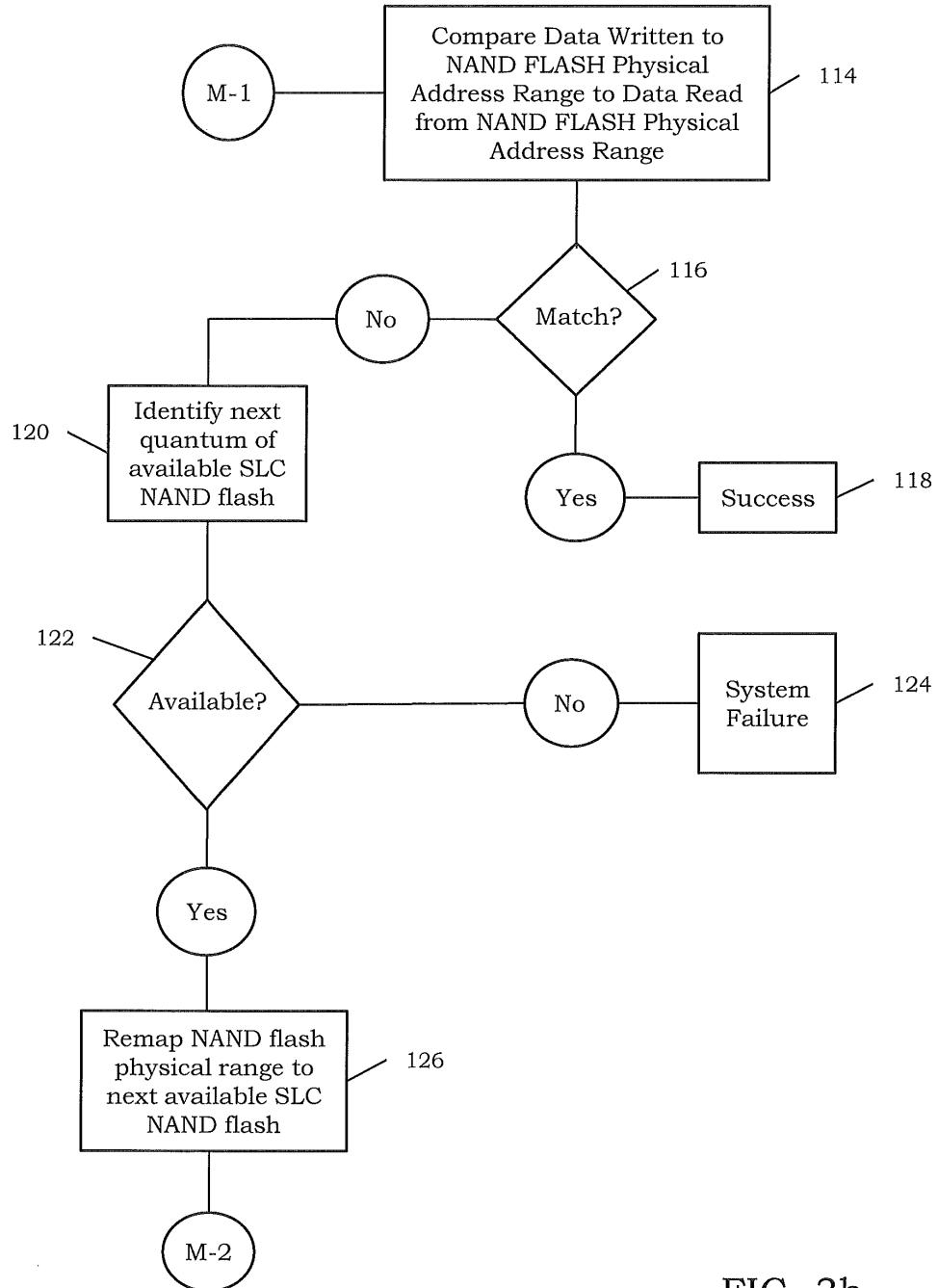


FIG. 3b

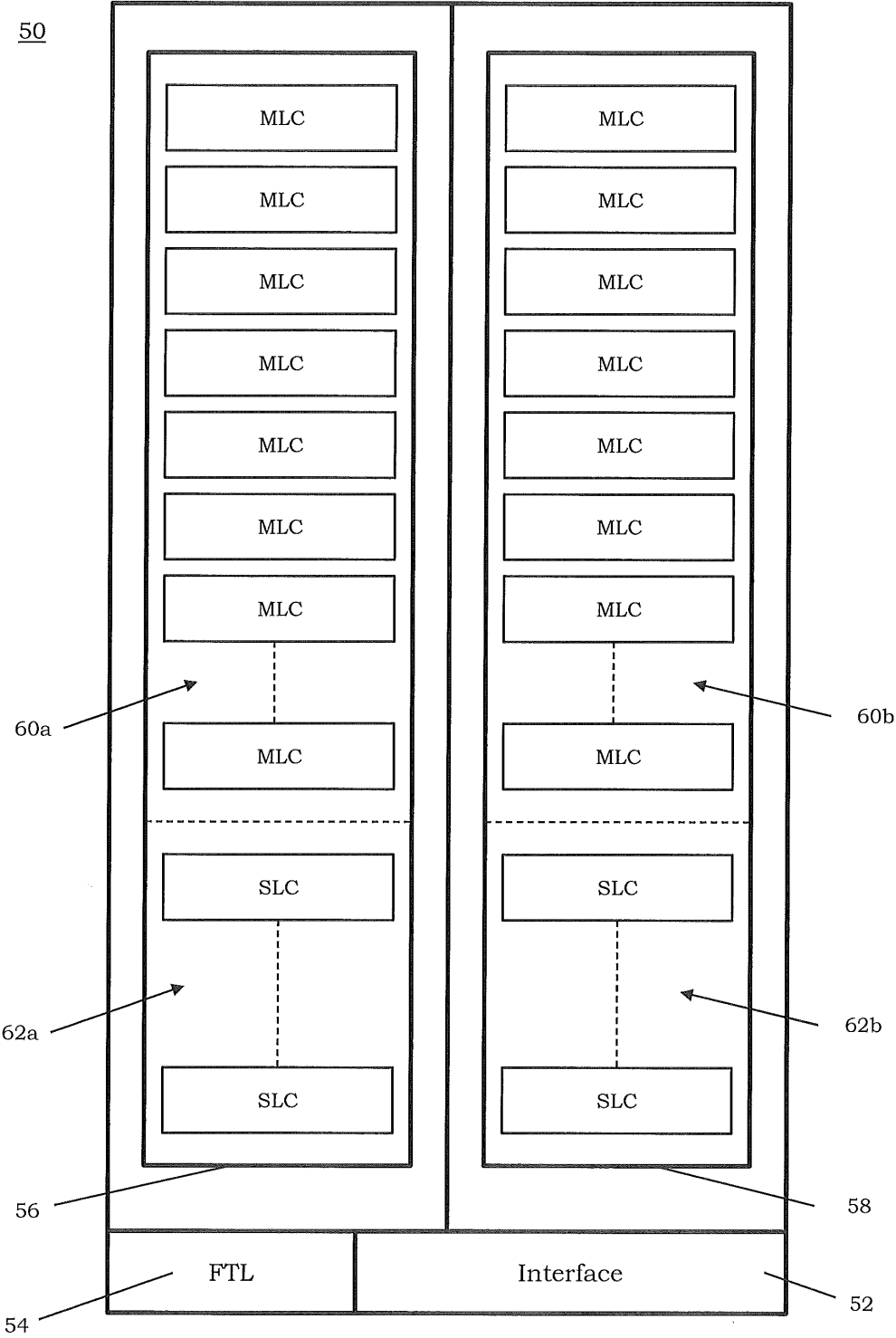


FIG. 4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No. : 14/525,411
Confirmation No. : 5177
Inventor : G.R. Mohan Rao
Filed : 10/28/2014
TC/A.U. : TBD
Examiner : TBD
Title : IMPROVED LIFETIME MIXED LEVEL NON-VOLATILE
MEMORY SYSTEM
Docket No. : 0299-0004.02

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

In response to the Notice of Incomplete Reply of January 12, 2015, and prior to examination on the merits, please amend the above-identified application as follows:

Amendments to the *Specification* begin on page 2 of this paper;

Amendments to the *Claims* are reflected in the listing of the claims beginning on page 3 of this paper;

Amendments to the *Drawings* begin on page 7 of this paper; and

Remarks being on page 8 of this paper.

Amendments to the Specification

Please amend the Specification as follows:

[0018] FIGS. 2A and 2B ~~are is-a drawings~~ depicting a translation table/address map in accordance with one embodiment of the present disclosure;

[0019] FIGS. 3Aa and 3Ba are a flow chart illustrating an exemplary method for use in implementing one embodiment of the present disclosure; and

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-14 (canceled)

15. (new) A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a flash translation layer (FTL); wherein the FTL is adapted to:

a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller

remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and

d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

16. (new) The system of claim 15, wherein the minimal minimum quanta of addresses is equal to one block.

17. (new) The system of claim 15, wherein the minimal minimum quanta of addresses is equal to one page.

18. (new) The system of claim 15, wherein the MLC non-volatile memory module is NAND flash memory.

19. (new) The system of claim 15, wherein the SLC non-volatile memory module is NAND flash memory.

20. (new) The system of claim 15, wherein the MLC non-volatile memory module is resistive random-access memory (RRAM).
21. (new) The system of claim 15, wherein the SLC non-volatile memory module is resistive random-access memory (RRAM).
22. (new) The system of claim 15, wherein the MLC non-volatile memory module is phase change memory (PCM).
23. (new) The system of claim 15, wherein the SLC non-volatile memory module is phase change memory (PCM).
24. (new) The system of claim 15, wherein the SLC non-volatile memory module is magnetic random-access memory (MAGRAM).
25. (new) The system of claim 15, wherein the FTL causes the transfer of content on a periodic basis.
26. (new) The system of claim 15, wherein the FTL is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed less frequently by maintaining a count of the number of times each one of the blocks is accessed.

27. (new) The system of claim 26, wherein the FTL is further adapted to allocate those blocks that receive less frequent writes by transferring the respective contents of those blocks to the at least one MLC non-volatile memory module.

28. (new) The system of claim 27, wherein the system for storing data further comprises at least one hard disk drive (HDD).

29. (new) The system of claim 28, wherein the FTL is further adapted to allocate those blocks that receive the least frequent writes by transferring the respective contents of those blocks to the at least one HDD.

Amendments to the Drawings

Please replace sheets 2-4 with the Replacement Sheets accompanying this Response.

REMARKS

In response to Notice of Incomplete Reply of January 12, 2015, Applicant makes the following remarks:

ADS

Applicant has filed herewith a proper ADS pursuant to 37 CFR 1.76(c)(2).

Claim Status

Applicant has canceled claims 1-14 and added new independent claim 15 and dependent claims 16-29.

Amendments to the Specification and the Drawings

Applicant has amended the Specification to be in compliance with 37 CFR 1.74 and 37 CFR 1.77(b)(9). The amendments to the Specification do not contain any new matter. Applicant has also amended the Drawings to be in compliance with 37 CFR 1.84(u)(1).

Amendments to the Claims

Applicant has canceled claims 1-14 and added new independent claim 15 and dependent claims 16-29. The new claims are supported by Applicant's disclosure at, for example, paragraphs [0002] and [0029] - [0031].

CONCLUSION

Applicant respectfully submits that in light of the arguments set forth in this paper, this application is now in condition for allowance, and requests that a timely Notice of Allowance be issued. However, should Examiner be of the opinion that further amendments or response are required, Applicant encourages Examiner to contact the undersigned attorney at the telephone number set forth below. Further, although no additional fees are believed to be due at this time, the Commissioner is authorized to charge any additional fees or deficiencies or credit any overpayments to The Law Offices of Eugene M. Cummings, P.C., Deposit Account No. 50-4199 with reference to attorney docket number 0299-0004.02.

Respectfully submitted,

The Law Offices of Eugene M. Cummings,
P.C.

By: /David M. Mundt/
David M. Mundt, Reg. No. 41,207
One North Wacker Dr., Suite 4130
Chicago, Illinois 60606
(312) 984-0144 (Telephone)
(312) 984-0146 (Facsimile)

Failed Data Integrity Test →

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	MLC/Block 2
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

FIG. 2A

Remapping to SLC flash module →

LOGICAL ADDRESS RANGE	PHYSICAL ADDRESS RANGE
R0	MLC/Block 0
R1	MLC/Block 1
R2	SLC/Block 0
R3	MLC/Block 3
R4	MLC/Block 4
RN	MLC/Block N

FIG. 2B

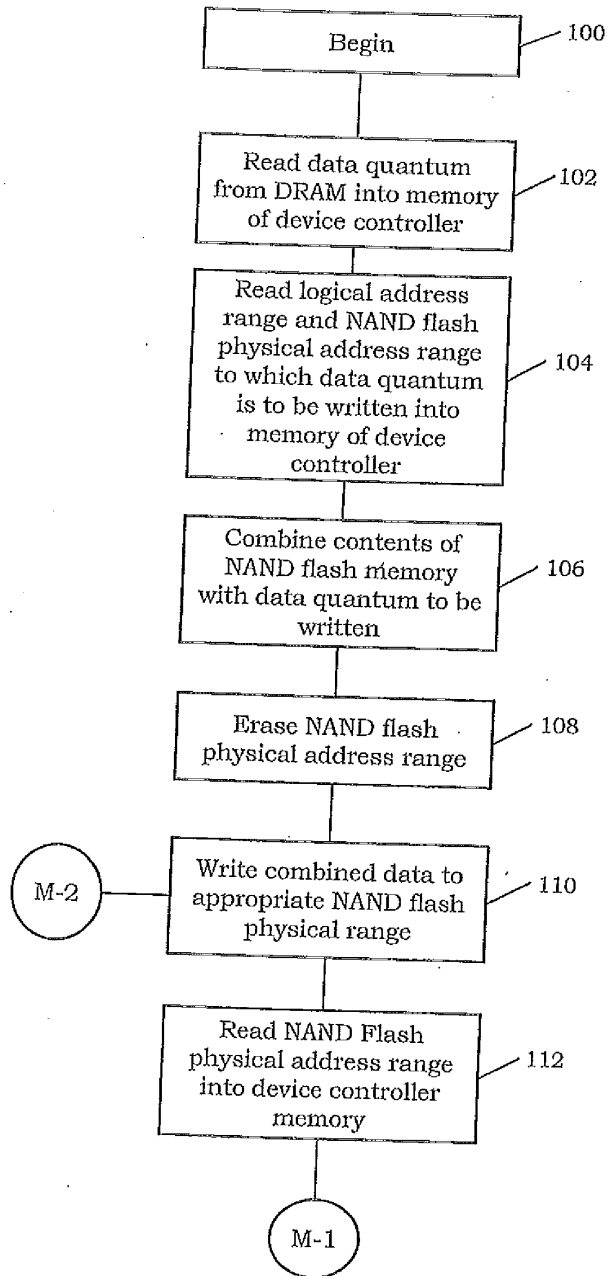


FIG.3A

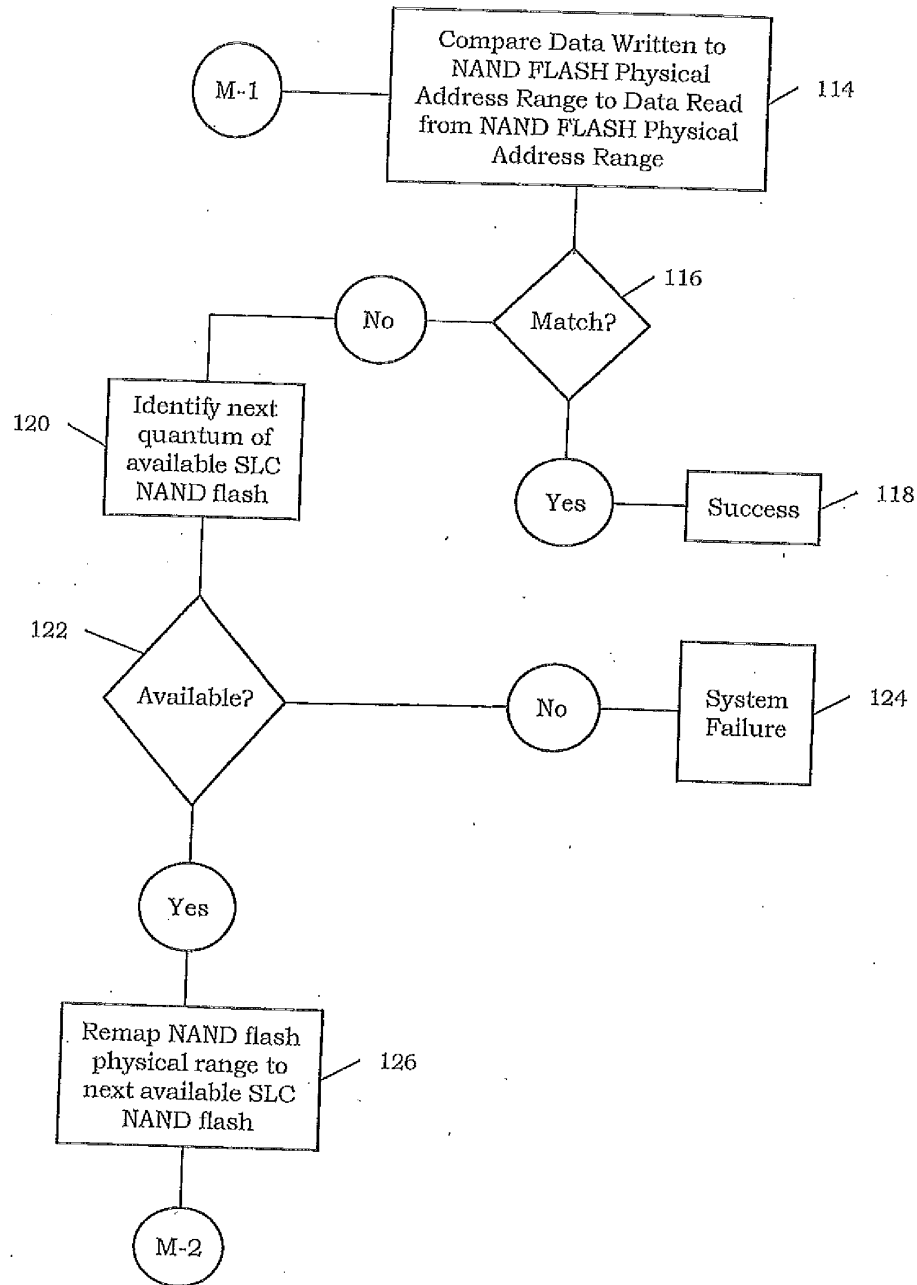


FIG.3B



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

25883 7590 09/15/2015
HOWISON & ARNOTT, L.L.P.
P.O. BOX 741715
DALLAS, TX 75374-1715

EXAMINER

REIDLINGER, RONALD LANCE

ART UNIT PAPER NUMBER

2824

DATE MAILED: 09/15/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/525,411	10/28/2014	G.R. Mohan Rao	GRTD-32620	5177

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	12/15/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25883 7590 09/15/2015
HOWISON & ARNOTT, L.L.P
P.O. BOX 741715
DALLAS, TX 75374-1715

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/525,411	10/28/2014	G.R. Mohan Rao	GRTD-32620	5177

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	12/15/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
REIDLINGER, RONALD LANCE	2824	365-185030

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/525,411	10/28/2014	G.R. Mohan Rao	GRTD-32620	5177

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P.O. BOX 741715
DALLAS, TX 75374-1715

EXAMINER

REIDLINGER, RONALD LANCE

ART UNIT	PAPER NUMBER
----------	--------------

2824

DATE MAILED: 09/15/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/525,411	Applicant(s) RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to communication(s) submitted 24 June 2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 15-29. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
 a) ☐ All b) ☐ Some *c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____	5. ☒ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____
--	--

/HARRY W BYRNE/ Primary Examiner, Art Unit 2824	/R. L. R./ Examiner, Art Unit 2824
--	---------------------------------------

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. Claims 15-29 are pending.
3. Claim 15 is independent.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.
5. The application has been amended as follows:

Claim 16. (Currently Amended) The system of claim 15, wherein the ~~minimal~~ minimum quanta of addresses is equal to one block.

Claim 17. (Currently Amended) The system of claim 15, wherein the ~~minimal~~ minimum quanta of addresses is equal to one block.
6. The amendment is to correct a transcription error of claim 17 and to eliminate the redundant language with no antecedent basis.

Allowable Subject Matter

7. Claims 15-29 are allowed.
8. The following is an examiner's statement of reasons for allowance:

The prior art of record fails to teach that the FTL allocates those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R LANCE REIDLINGER whose telephone number is (571)270-7353. The examiner can normally be reached on 11:30am - 9:00pm Mon-Thur and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571)272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2824

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R. L. R./
Examiner, Art Unit 2824

/HARRY W BYRNE/
Primary Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 14/525,411	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-7,855,916 B2	12-2010	Rao; G. R. Mohan	G11C16/10	365/185.05
*	B	US-2009/0268513 A1	10-2009	De Ambroggi; Luca	G11C11/005	365/163
*	C	US-2009/0307418 A1	12-2009	Chen; Ming-Dar	G06F11/1048	711/105
*	D	US-2010/0058018 A1	03-2010	Kund; Michael	G11C7/04	711/167
*	E	US-2010/0172179 A1	07-2010	Gorobets; Sergey Anatolievich	G06F12/0246	365/185.09
*	F	US-2011/0050870 A1	03-2011	HANARI; Jun	H04N13/0438	348/56
*	G	US-2011/0271043 A1	11-2011	SEGAL; Avigdor	G11C29/82	711/103
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification 	Application/Control No. 14525411	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN	
	Examiner LANCE REIDLINGER	Art Unit 2824	

CPC						
Symbol					Type	Version
G11C		29		76	F	2013-01-01
G06F		11		1068	I	2013-01-01
G11C		11		5621	I	2013-01-01
G11C		11		5678	I	2013-01-01
G06F		11		1072	I	2013-01-01
G11C		29		52	I	2013-01-01
G11C		2211		5641	A	2013-01-01

CPC Combination Sets						
Symbol			Type	Set	Ranking	Version

/LANCE REIDLINGER/ Examiner.Art Unit 2824 (Assistant Examiner)	09/08/2015 (Date)	Total Claims Allowed: 15	
/HARRY W BYRNE/ Primary Examiner.Art Unit 2824 (Primary Examiner)	09/08/2015 (Date)	O.G. Print Claim(s) 15	O.G. Print Figure 2a and 2b

Issue Classification 	Application/Control No. 14525411	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner LANCE REIDLINGER	Art Unit 2824

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION														
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED									
						G	1	1	C	29 / 52 (2006.01.01)										
CROSS REFERENCE(S)																				
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																			

/LANCE REIDLINGER/ Examiner.Art Unit 2824 (Assistant Examiner)	09/08/2015 (Date)	Total Claims Allowed: 15	
/HARRY W BYRNE/ Primary Examiner.Art Unit 2824 (Primary Examiner)	09/08/2015 (Date)	O.G. Print Claim(s) 15	O.G. Print Figure 2a and 2b

Issue Classification 	Application/Control No. 14525411	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner LANCE REIDLINGER	Art Unit 2824

☐ Claims renumbered in the same order as presented by applicant																☐ CPA		☐ T.D.		☐ R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original						
	1	3	17																		
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/LANCE REIDLINGER/ Examiner.Art Unit 2824 (Assistant Examiner)	09/08/2015 (Date)	Total Claims Allowed: 15	
/HARRY W BYRNE/ Primary Examiner.Art Unit 2824 (Primary Examiner)	09/08/2015 (Date)	O.G. Print Claim(s) 15	O.G. Print Figure 2a and 2b

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	763	Rao near2 Mohan.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:29
L2	0	Rao near2 "G.R. Mohan".in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:32
L3	0	"G.R. Mohan".in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:32
L4	3729956	Gl.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:32
L5	3881395	R!.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:32
L6	65851	rao.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:32
L7	17889	mohan.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:33
L8	295	4 and 5 and 6 and 7	US-PGPUB;	OR	ON	2015/09/08

EAST Search History

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			04:33
L9	2054	SLC! same test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
L10	1297	MLC! same test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
L11	68	L9 and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
L12	7281	SLC! and MLC!	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
L13	4720	L12 and address and page	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
L14	273	L13 and test\$3 with fail\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
L15	220	L14 and (map mapped mapping re\$1map\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:35
L16	189	g11c2029/1806.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2015/09/08 04:45

EAST Search History

			IBM_TDB			
L17	2537	g11c2211/5641.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:47
L18	2421	g11c29/76.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:48
L19	764	g11c29/765.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:48
L20	1234	g11c29/50004.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:49
L21	5523	g06f11/1068,1072.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:50
L22	4527	g11c11/5621.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:51
L23	14820	16 17 18 19 20 21 22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:51
L24	68	11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/08 04:52
L37	2	13/455267.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2015/09/08 04:58

EAST Search History

			JPO; DERWENT; IBM_TDB			
S1	1	13/455267.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:05
S2	2	12/567771.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:07
S3	5314	SLC! and MLC!	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:09
S4	3345	S3 and address and page	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:10
S5	904	S4 and test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:10
S6	662	S5 and (map mapped mapping re\$1map\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:11
S7	177	S4 and test\$3 with fail\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:11
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S9	1915	SLC! same test\$3	US-PGPUB; USPAT;	OR	ON	2014/06/13 13:13

EAST Search History

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S10	1160	MLC! same test\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:14
S11	46	S9 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:14
S12	1	13/096736.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:42
S13	2	"20100172179".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 13:43
S15	2	12/348825.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:14
S16	6	((("5671128") or ("6948026") or ("20030110343") or ("20030123301") or ("20050144516") or ("20090187798"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/06/13 14:17
S17	3	S16 and count	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:17
S18	0	"20110860870".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:25
S19	5	"2011060870".pn.	US-PGPUB; USPAT;	OR	ON	2014/06/13 14:25

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S20	3	"20110060870".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:25
S21	7	(US-20090268513-\$ or US-20090327590-\$ or US-20110271043-\$ or US-20100172179-\$).did. or (US-8379460-\$ or US-8417988-\$ or US-8422303-\$).did.	US-PGPUB; USPAT	OR	ON	2014/06/13 14:34
S22	5	S21 and count	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 14:34
S23	10982	address with block with page	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 15:07
S24	2	S23 and S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 15:07
S25	1	S21 and MRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 15:29
S26	61	MRAM with MLC	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/13 15:30
S27	7	advantages with MRAM with PCRAM with (flash eeprom)	US-PGPUB; USPAT	OR	ON	2014/06/13 16:16
S28	118	((("G R Mohan") near2 (Rao)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/06/13 16:48
S29	5196	SLC and MLC	US-PGPUB; USPAT	OR	ON	2014/06/13 16:49

EAST Search History

S30	8	S3 and S28	US-PGPUB; USPAT	OR	ON	2014/06/13 16:49
S31	205	gorobets near2 sergey.in.	US-PGPUB; USPAT	OR	ON	2014/06/13 16:59
S32	245	wear adj leveling.ti.	US-PGPUB; USPAT	OR	ON	2014/06/13 16:59
S33	4	S31 and S32	US-PGPUB; USPAT	OR	ON	2014/06/13 17:00
S34	84	flag same slc same MLC	US-PGPUB; USPAT	OR	ON	2014/06/13 19:54
S35	1	"20060171210".pn.	US-PGPUB; USPAT	OR	ON	2014/06/13 19:56
S36	2	flag same Tlc same MLC	US-PGPUB; USPAT	OR	ON	2014/06/13 19:59
S37	411	flag same ((three triple tri!) adj (level state bit) TLC) same (MLC DLC BLC (double two bi) adj (level state bit))	US-PGPUB; USPAT	OR	ON	2014/06/13 20:03
S38	403	flag same ((three triple tri!) adj (level state bit) TLC) same ((double two bi) adj (level state bit))	US-PGPUB; USPAT	OR	ON	2014/06/13 20:04
S39	176601	"365".clas. "711".clas.	US-PGPUB; USPAT	OR	ON	2014/06/13 20:04
S40	90	S37 and S39	US-PGPUB; USPAT	OR	ON	2014/06/13 20:04
S41	1	"20090307418".pn.	US-PGPUB; USPAT	OR	ON	2014/06/14 00:30
S42	5281	365/185.03,185.09.ccls.	US-PGPUB; USPAT	OR	ON	2014/06/14 01:15
S43	11	("20040213031" "20060268608" "20080106946" "20080270072" "20090049364" "20090073763" "20090177851" "20100142270" "20120030528" "20120268994" "5673383").PN.	US-PGPUB; USPAT	OR	ON	2014/06/14 17:54
S44	3733	365/185.03.ccls.	US-PGPUB; USPAT	OR	ON	2014/06/14 18:01
S45	629	flag and S44	US-PGPUB; USPAT	OR	ON	2014/06/14 18:01
S46	27101	read\$3 adj voltage	US-PGPUB; USPAT	OR	ON	2014/06/14 18:02
S47	332	S45 and S46	US-PGPUB; USPAT	OR	ON	2014/06/14 18:02
S48	178033	first near2 read\$3	US-PGPUB; USPAT	OR	ON	2014/06/14 18:02
S49	124427	second near2 read\$3	US-PGPUB; USPAT	OR	ON	2014/06/14 18:02
S50	179	S48 and S49 and S46 and S45	US-PGPUB; USPAT	OR	ON	2014/06/14 18:03
S51	1	masaki near2 fujio.in.	US-PGPUB; USPAT	OR	ON	2014/06/14 18:08
S52	31	masaki near2 fujiu.in.	US-PGPUB; USPAT	OR	ON	2014/06/14 18:09
S53	725	flag same S48 same S49	US-PGPUB; USPAT	OR	ON	2014/06/14 18:22

EAST Search History

S54	69	S44 and S53	US-PGPUB; USPAT	OR	ON	2014/06/14: 18:22
S55	92	S53 same (word adj line wordline)	US-PGPUB; USPAT	OR	ON	2014/06/14: 18:24
S56	39	S44 and S55	US-PGPUB; USPAT	OR	ON	2014/06/14: 18:24
S57	5	flag and S52	US-PGPUB; USPAT	OR	ON	2014/06/14: 18:30

EAST Search History (Interference)

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L25	101	g11c2029/1806.cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:53
L26	1205	g11c2211/5641.cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:53
L27	1056	g11c29/76.cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:53
L28	377	g11c29/765.cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:54
L29	574	g11c29/50004.cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:54
L30	2553	g06f11/1068,1072.cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:54
L31	2088	g11c11/5621.cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:54
L32	6751	25 26 27 28 29 30 31	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:54
L34	247	flash adj translation adj layer.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:55
L35	337	(flash adj translation adj layer FTL).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:55
L36	21	32 and 35	US-PGPUB; USPAT; UPAD	OR	ON	2015/09/08: 04:55
S58	919	single adj (level bit data) adj (cell memory element).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25: 07:04
S59	2720	(plural multiple multi) adj (level bit data) adj (cell memory element).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25: 07:05
S60	1138	MLCl.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25: 07:05
S61	651	SLCl.clm.	US-PGPUB; USPAT;	OR	ON	2014/08/25: 07:05

EAST Search History

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S62	3190	S59 S60	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:05
S63	3063	S58 S59	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:05
S64	2725	S62 and S63	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:05
S65	101412	"365".cls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
S66	1486	S64 and S65	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
S67	3807	365/185.03.ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
S68	1818	365/185.09.ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
S69	5784	365/201.ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
S70	10934	S67 S68 S69	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:06
S71	885	S70 and S64	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:07
S72	282940	address.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:07
S73	389370	(table map).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:08
S74	17911	S72 near3 S73	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:08
S75	284287	test\$3.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:08
S76	4	S64 and S74 and S75	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:08
S77	1	13/"Term Removed"	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:10
S78	1266	S58 S61	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:15
S79	652	S78 and S62	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:15
S80	134	S70 and S79	US-PGPUB; USPAT;	OR	ON	2014/08/25 07:16

EAST Search History

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S82	11706	365/148,158,163,171,173.ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:17
S83	17	S79 and S82	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/25 07:17

9/ 8/ 2015 5:45:14 AM**C:\ Users\ rreidlinger\ Documents\ EAST\ Workspaces\ 13455267.wsp**



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BIB DATA SHEET

CONFIRMATION NO. 5177

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/525,411	10/28/2014	365	2824	GRTD-32620		
APPLICANTS GREENTHREAD, LLC, DALLAS, TX; INVENTORS G.R. Mohan Rao, Allen, TX; ** CONTINUING DATA ***** This application is a DIV of 13/455,267 04/25/2012 PAT 8891298 which claims benefit of 61/509,257 07/19/2011 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY ** 11/04/2014						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and / R Lance Reidlinger/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TX	SHEETS DRAWINGS 5	TOTAL CLAIMS 15	INDEPENDENT CLAIMS 1
ADDRESS HOWISON & ARNOTT, L.L.P. P.O. BOX 741715 DALLAS, TX 75374-1715 UNITED STATES						
TITLE LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM						
FILING FEE RECEIVED 730	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

Search Notes 	Application/Control No. 14525411	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner LANCE REIDLINGER	Art Unit 2824

CPC- SEARCHED		
Symbol	Date	Examiner
G11C 11/5621, 2211/5641, 2029/1806, 29/50004, 29/76, 29/765	9/8/2015	RLR
G06F 11/1068, 11/1072	9/8/2015	RLR

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Reviewed Parent Application Search/Prosecution History	9/8/2015	RLR
Inventor Search Conducted in EAST	9/8/2015	RLR
See EAST Search History	9/8/2015	RLR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
G11C	11/5621, 2211/5641, 2029/1806, 29/50004, 29/76, 29/765	9/8/2015	RLR
G06F	11/1068, 11/1072	9/8/2015	RLR

/LANCE REIDLINGER/ Examiner.Art Unit 2824	
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Subject: Private PAIR Correspondence Notification for Customer Number 25883

Sep 15, 2015 05:23:09 AM

Dear PAIR Customer:

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UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 25883 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

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Application	Document	Mailroom Date	Attorney Docket No.
14525411	NOA	09/15/2015	GRTD-32620
	892	09/15/2015	GRTD-32620

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