

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,

Petitioner

v.

VERVAIN, LLC,

Patent Owner

Inter Partes Review Case No. IPR2025-00215

Patent 10,950,300

PETITION FOR *INTER PARTES* REVIEW OF

U.S. PATENT NO. 10,950,300

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LIST OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 10,950,300, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1002	Declaration of Carl Sechen, Ph.D.
1003	U.S. Provisional Application No. 61/509,257, titled “IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM” by Rao
1004	U.S. Patent No. 7,855,916, titled “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES,” to Rao
1005	U.S. Patent No. 8,891,298, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1006	Excerpts from prosecution history of ‘298 patent
1007	U.S. Patent No. 9,196,385, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1008	Excerpts from prosecution history of ‘385 patent
1009	U.S. Patent No. 9,997,240, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1010	Excerpts from prosecution history of ‘240 patent
1011	<i>Intentionally omitted</i>
1012	Excerpts from prosecution history of ‘300 patent
1013-1024	<i>Intentionally omitted</i>
1025	Excerpts from Rino Micheloni, et al., INSIDE NAND FLASH MEMORIES (Springer 2010)

1026	Excerpts from NONVOLATILE MEMORY TECHNOLOGIES WITH EMPHASIS ON FLASH: A COMPREHENSIVE GUIDE TO UNDERSTANDING AND USING NVM DEVICES (Joe E. Brewer & Manzur Gill eds. Wiley-IEEE Press 2008)
1027	Excerpts from MICROSOFT COMPUTER DICTIONARY (5 th ed. 2002)
1028-1029	<i>Intentionally omitted</i>
1030	Yu Cai et al., <i>Program Interference in MLC NAND Flash Memory: Characterization, Modeling and Mitigation</i> (IEEE 2013)
1031	Kang-Deog Suh et al., <i>A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme</i> , 30 IEEE J. Solid State Circuits 1149 (Nov. 1995)
1032	Eitan Yaakobi et al., <i>Error Characterization and Coding Schemes for Flash Memories</i> (2010 IEEE Globecom Workshops, Miami, FL at 1856-60)
1033	Evans, Chris, “Enterprise MLC: How flash vendors are boosting MLC write endurance” (June 3, 2011)
1034	Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008)
1035	Ashish Jagmohan et. al., <i>Adaptive Endurance Coding for NAND Flash</i> (2010 IEEE Globecom Workshops, Miami, FL at 1841-45)
1036	Sungjin Lee et al., <i>FlexFS: A Flexible Flash File System for MLC NAND Flash Memory</i> (2009 USENIX Annual Technical Conference, San Diego, CA, June 14-19, 2009)
1037	Minyoung Sung & Kanghee Kim, <i>Asymmetric Flash Volume Management</i> , 58 IEEE Transactions on Consumer Electronics 455 (May 2012)
1038	Greg Atwood et al., <i>Intel StrataFlash™ Memory Technology Overview</i> at 4, Intel Technology J. (Q4 1997)

1039	Taehee Cho et al., “A 3.3 V 1 Gb multi-level NAND flash memory with non-uniform threshold voltage distribution,” <i>2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers</i> , ISSCC (Cat. No. 01CH37177) (2001)
1040	U.S. Patent No. 6,456,528, titled for “SELECTIVE OPERATION OF A MULTI-STATE NON-VOLATILE MEMORY SYSTEM IN A BINARY MODE” to Chen
1041	U.S. Patent No. 8,078,794, titled “HYBRID SSD USING A COMBINATION OF SLC AND MLC FLASH MEMORY ARRAYS,” to Lee et al.
1042	U.S. Patent Appl. Pub. No. 2008/0140918, titled “HYBRID NON-VOLATILE SOLD STATE MEMORY SYSTEM” by Sutardja
1043	U.S. Patent Appl. Pub. No. 2009/0327591, titled “SLC-MLC COMBINATION FLASH STORAGE DEVICE,” by Moshayedi
1044	U.S. Patent Appl. Pub. No. 2010/0172179, titled “SPARE BLOCK MANAGEMENT OF NON-VOLATILE MEMORIES,” by Gorobets et al.
1045	U.S. Patent No. 8,634,240, titled “NON-VOLATILE MEMORY AND METHOD WITH ACCELERATED POST-WRITE READ TO MANAGE ERRORS,” to Gavens et al.
1046	U.S. Patent No. 8,806,301, titled “DATA WRITING METHOD FOR A FLASH MEMORY, AND CONTROLLER AND STORAGE SYSTEM USING THE SAME,” to Yu et al.
1047	U.S. Patent Appl. Pub. No. 2010/0115192, titled “WEAR LEVELING METHOD FOR NON-VOLATILE MEMORY DEVICE HAVNG SINGLE AND MULTI LEVEL MEMORY CELL BLOCKS,” by Lee
1048	U.S. Patent Appl. Pub. No. 2011/0271043, titled “SYSTEM AND METHOD FOR ALLOCATING AND USING SPARE BLOCKS IN A FLASH MEMORY,” to Segal et al.

1049	U.S. Patent Appl. Pub. No. 2011/0153912, titled “MAINTAINING UPDATES OF MULTI-LEVEL NON-VOLATILE MEMORY IN BINARY NON-VOLATILE MEMORY,” by Gorobets et al.
1050	U.S. Patent No. 5,930,167, titled “MULTI-STATE NON-VOLATILE FLASH MEMORY CAPABLE OF BEING ITS OWN TWO STATE WRITE CACHE,” to Lee et al.
1051	U.S. Patent Appl. Pub. No. 2010/0172180, titled “NON-VOLATILE MEMORY AND METHOD WITH WRITE CACHE PARTITIONING,” by Paley et al.
1052-1055	<i>Intentionally omitted</i>
1056	U.S. Patent App. Pub. No. 2009/0172267, “REFRESH METHOD OF A FLASH MEMORY,” by Oribe et al.
1057	U.S. Patent No. 5,936,971, titled “MULTI-STATE FLASH EEPROM SYSTEM WITH CACHE MEMORY, to Harari et al.
1058	PCT Pub. No. WO 03/027828, “METHOD OF WRITING DATA TO NON-VOLATILE MEMORY,” by Gorobets et al.
1059-1060	<i>Intentionally omitted</i>
1061	Duane H. Oto et al., <i>High-Voltage Regulation and Process Considerations for High-Density 5 V-Only E²PROM’s</i> , SC-18 IEEE J. Solid State Circuits 532 (Oct. 1983)
1062	Gheorghe Samachisa et al., <i>A 128K Flash EEPROM Using Double-Polysilicon Technology</i> , SC-22 IEEE J. Solid State Circuits 676 (Oct. 1987)
1063	Masaki Momodomi et al., <i>An Experimental 4-Mbit CMOS EEPROM with a NAND-Structured Cell</i> , 24 IEEE J. Solid State Circuits 1238 (Oct. 1989)
1064	Tae-Sun Chung et al., <i>A survey of Flash Translation Layer</i> , 55 J. Systems Architecture 332-43 (2009)

1065	Yoshiba Iwata et al., <i>A High-Density NAND EEPROM with Block-Page Programming for Microcomputer Applications</i> , 25 IEEE J. Solid-State Circuits 417 (Apr. 1990)
1066	Simona Boboila and Peter Desmoyers, <i>Write Endurance in Flash Drives: Measurements and Analysis</i> , Usenix Conference (Feb. 2010)
1067	SiliconSystems, <i>Increasing Flash SSD Reliability</i> , StorageSearch.com (April 2005)
1068	Taehee Cho et al., <i>A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single Level Modes</i> , 36 IEEE J. Solid State Circuits 1700 (Nov. 2001)
1069	Ken Takeuchi, <i>A Multipage Cell Architecture for High-Speed Programming Multilevel NAND Flash Memories</i> , 33 IEEE J. Solid-State Circuits 1228 (Aug. 1998)
1070	Garth Goodson & Rahul Iyer, <i>Design Tradeoffs in a Flash Translation Layer</i> , HPCA [High Performance Computer Architecture] WEST 2010 Conference, Bangalore, India
1071-1079	<i>Intentionally omitted</i>
1080	Docket list for <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex., filed March 8, 2024)
1081	Docket list for <i>Vervain, LLC v. Kingston Technology Company, Inc.</i> , No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024)
1082	First Amended Complaint, Doc. No. 9 in <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex.)
1083	Signed Agreed Scheduling Order, Doc. No. 16 in <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex.)

I. INTRODUCTION:

Phison Electronics Corporation (“Phison” or “Petitioner”) requests *inter partes* review (“IPR”) of all claims 1-12 (the “Challenged Claims”) of U.S. Patent No. 10,950,300, entitled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Dr. G.R. Mohan Rao (the “‘300 patent”) (Ex. 1001), which is assigned to Vervain, LLC (“Vervain” or “Patent Owner”). The ‘300 patent is the fourth of ten patents so far issued on the same Apr. 25, 2012, specification and the same title, collectively referred to here as “the Lifetime Patents.”¹ Each of those

¹ The ‘300 patent issued on Mar. 16, 2021, from U.S. Patent Appl. No. 16/006,299 (excerpts in Ex. 1012), which was filed Jun. 12, 2018, as a continuation of U.S. Patent Appl. No. 14/950,553 (excerpts in Ex. 1010), filed Nov. 24, 2015 (now U.S. Patent No. 9,997,240, the “‘240 patent,” Ex. 1009), as a continuation of U.S. App. No. 14/525,411 (excerpts in Ex. 1008), filed Oct. 28, 2014 (now U.S. Patent No. 9,196,385, the “‘385 patent,” Ex. 1007), as a continuation of U.S. Appl. No. 13/455,267 (excerpts in Ex. 1006), filed Apr. 25, 2012 (now U.S. Patent No. 8,891,298 (the “‘298 patent,” Ex. 1005). Six other patents issued on applications continued from the above, U.S. Patent Nos. 11,830,546 (the “‘546 patent”), 11,854,612 (the “‘612 patent”), 11,967,369 (the “‘369 patent”), 11,967,370 (the “‘370 patent”), 12,119,054 (the “‘054 patent”) and 12,136,455 (the “‘455 patent”).

patents incorporated by reference Dr. Rao's U.S. Patent No. 7,855,916,² and claimed priority from U.S. Provisional App. No. 61/509,257, filed on July 19, 2011 ("Provisional," Ex. 1003, *e.g.*, '300 1:24-27).

All that was described in the 2012 common specification³ and incorporated Rao '916, and all that was claimed in the first three Lifetime Patents, was a known hybrid NAND flash memory system of known "**MLC**" and "**SLC**" memory "**modules**" and a controller with known, necessary flash memory logical-to-physical

² (*E.g.*, '300 1:28-35, "Rao '916," Ex. 1004.) Rao '916, entitled "NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES," was incorporated along with U.S. Patent No. 8,194,452 to Dr. Rao of the same title and specification ('300 1:35-41).

³ Its particular selection of terminology and limited descriptions must be read in view of the disclosure and use of terms in the forty documents filed with the Apr. 25, 2012 '298 application (cited here by "IDS#_" in reference to their listing on the three Information Disclosure Statements filed that day [Ex. 1006 at 26-36]), which, *e.g.*, distinguished "**MLC memory**" and its binary (1-bit) "**mode**" use from the older memory later called "**SLC**" – which does not conversely allow multi-bit use (*e.g.*, Declaration of Dr. Carl Sechen ["Sechen," Ex. 1002] ¶¶ 42-44, 49, explaining some of the IDS documents).

mapping functions, “adapted” to perform a variant of ordinary flash “wear leveling” and a variant of known error management in a “data integrity test,” failure of which results in remapping to the **SLC module** of data previously mapped to the failed location (*e.g.*, ‘298 [Ex. 1005] 7:8-8:9, ‘385 [Ex. 1007] 7:12-8:4).

The Apr. 25, 2012, common specification assumed the known structure and operational – including “lifetime” – needs of a hybrid flash memory system of the specified, known MLC and SLC “**memory modules.**” More than six years after that filing, the ‘300 patent application was untethered from even that skeletal disclosure by introducing in its claims the terms, “**memory space,**” “**memory elements**” and “**random access volatile memory,**” that were mentioned ambiguously or not at all in the specification, added to a mix-and-matching of ambiguous and inconsistent words used in the specification to describe its variants of “data integrity test” and “wear leveling.” The seven post-2018 Lifetime Patents issued on no more than that 2012 common specification for multiple claim rewritings using the new terms, pivoting on known flash system roles of random access volatile memory (“RAVM”).

So far, the first eight of the Lifetime Patents have been asserted (First Amended Complaint, Ex. 1082) by the Patent Owner against Petitioner in *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex. filed March 8,

2024).⁴ Petitioner has petitioned for reviews by this Board in pending *Phison Electronics Corp. v. Vervain, LLC*, PGR2024-00047,⁵ PGR2024-00048,⁶ IPR2025-00212,⁷ IPR2025-00213,⁸ and IPR2025-214.⁹

⁴ That complaint was dismissed in part on Dec. 2, 2024. (Docket List [Ex. 1080] entry 38].) All eight patents are also asserted against a customer of Phison in *Vervain, LLC v. Kingston Technology Company, Inc., Kingston Digital, Inc., and Kingston Technology Corp.*, No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024). The first four patents were earlier asserted in *Vervain, LLC v. Micron Technology, Inc.*, No. 6:21-cv-00487 (W.D. Tex. filed May 10, 2021, settled April 21, 2023) and *Vervain, LLC v. Western Digital Corp.*, No. 6:21-cv-00488 (W.D. Tex. filed May 10, 2021, settled Aug. 8, 2023). Micron petitioned this Board for review in *Micron Technology, Inc. v. Vervain, LLC*, IPR2021-01547 (‘298 patent), -01548 (‘385 patent), -01549 (‘240 patent), and -01550 (‘300 patent), which were instituted on April 8 and 11, 2022, and terminated on April 4, 2023, on settlement after hearing but prior to final written decision.

⁵ (‘546 patent, accorded filing date Aug. 27, 2024 [Paper No. 5].)

⁶ (‘612 patent, accorded filing date Sept. 25, 2024 [Paper No. 5].)

⁷ (‘298 patent, filed Nov. 25, 2024.)

⁸ (‘385 patent, filed Dec. 4, 2024.)

This Petition demonstrates by a preponderance of the evidence that the Challenged Claims are unpatentable, despite unsupported abstraction to “memory spaces” and “memory elements,” as reading on long-known hybrid memory systems of distinct Single-Level Cell (“SLC”) and Multi-Level Cell (“MLC”) NAND flash memories with data seen by a user at a logical address mapped and remapped to different physical memory locations in ordinary flash operation by an ordinary flash controller that ordinarily performs “wear leveling” in a variety of ways to avoid premature failure (and thus “maximize” or “enhance” system “lifetime” or “endurance”) and may optionally apply error management techniques that include remapping to SLC memory upon failure of a “data integrity test” in order to “enhance endurance.” One of such known systems is presented in Ground 1 of invalidity, the published hybrid multiple-endurance mode NAND flash memory system of U.S. Patent No. 8,634,240 to **Gavens** et al.,¹⁰ which discloses multiple

⁹(‘240 patent, filed Dec. 6, 2024.)

¹⁰(“Gavens,” Ex. 1045, published Apr. 28, 2011 [cover].) It has a controller with a block management software module performing the ordinary functions of a flash translation layer (“FTL”) satisfying both the independent claims and claim 2 specifying FTL as a software module. As explained below, it is obviously

error management techniques, including a “data integrity test” and resultant mapping as recited in independent claims 1 and 12, and more particularly to SLC memory as recited in dependent claim 7. It is further shown that the newly recited RAVM is a common component of NAND flash memory systems, including those disclosed by Gavens through its incorporated references for flash block management, satisfying the independent claims – both in the dynamic (DRAM) and static (SRAM) varieties recited in dependent claims 5 and 6 respectively, and by inclusion in the controller, satisfying dependent claim 3. Consistent with the understanding of “memory space” dictated by prosecution amendment to the independent claims of mapping to “memory element,” claim 10 “wear leveling” is commonly and compatibly applied in hybrid flash memory systems, as in Gavens as explained by its incorporated references and further exemplified by U.S. Patent No. 8,078,794 to Lee et al.,¹¹ U.S. Patent Appl. Pub. No. 2008/0140918, by Sutardja,¹² and U.S. Patent Appl. Pub. No. 2009/0327591, by Moshayedi,¹³ where Sutardja and Moshayedi disclose multiple

implementable as an MLC-SLC hybrid, satisfying the requirements of the independent claims and dependent claims 4, 8, 9, and 11.

¹¹ (“**Lee ‘794**,” Ex. 1041, published Sept. 4, 2008.)

¹² (“**Sutardja**,” Ex. 1042.)

¹³ (“**Moshayedi**,” Ex. 1043.)

compatible wear leveling techniques that would meet alternative understandings of claim 10. Thus, under Ground 1, all the Challenged Claims are also obvious over Gavens and incorporated references, in view of knowledge of the POSITA.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8:

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1):

Petitioner Phison Electronics Corporation is the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2):

As set forth further at note 4 *supra*, the ‘300 patent (along with seven other patents based on the same specification) is currently asserted by Vervain against Phison and its customer (separately) in the Western District of Texas. In the Phison case, a claim construction hearing is tentatively scheduled for January 9, 2025, and jury selection is tentatively scheduled for December 15, 2025 (*Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259, Doc. No. 16 (W.D. Tex. July 15, 2024) (Ex. 1083). Resolution of this Petition may simplify that litigation and promote settlement.

C. Lead and Back Up Counsel Under 37 C.F.R. § 42.8(b)(3):

Pursuant to 37 C.F.R. § 42.8(b)(3), lead counsel for this Petition is Hsuanyeh Chang, PhD (Reg. No. 73,431) and back-up counsel are Stephen Y. Chow (Reg. No. 31,338), Douglas E. Chin (Reg. No. 66,713), and Peter Yi (Reg. No. 61,790). Pursuant to 37 C.F.R. § 42.10(b), Petitioner has filed a power of attorney designating the above-identified counsel.

D. Service Information Under 37 C.F.R. § 42.8(b)(4):

Service information under 37 C.F.R. § 42.8(b)(4) for the Petition is as follows:

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Petitioner consents to electronic service at the email addresses above.

III. ADDITIONAL REQUIREMENTS:

A. Payment of Fees Under 37 C.F.R. § 42.15:

The required fees are submitted from Deposit Account No. 50-6685 (Order No. 1280-0014). If any additional fees are due at any time during this proceeding,

the Office is authorized to charge such fees to Deposit Account No. 50-6685 (Order No. 1280-0014).

B. Timing Under 37 C.F.R. § 42.102:

The present petition for *inter partes* review is filed more than nine months after the grant of the '300 patent.

C. Grounds for Standing Under 37 C.F.R. § 42.104(a):

Petitioner certifies that: (1) the '300 patent is eligible for *inter partes* review; and (2) Petitioner is not barred or estopped from requesting *inter partes* review of any claims of the '300 patent on the grounds identified herein.

IV. NAND FLASH TECHNOLOGY BACKGROUND

Petitioner's expert, Dr. Carl Sechen, has provided in his declaration ("Sechen," Ex. 1002) a deep analysis of the state of NAND flash technology implicitly relied on by the '300 patent, the embodiments admitted or advanced in the specification, the evolution of the claims through prosecution and their remaining defects, and invalidity of those claims over the prior art in view of the POSITA's knowledge of the art. Following is a summary of the NAND flash memory technology underlying the '300 patent base claims to a "system for storing data," based on known MLC and SLC NAND flash modules and a "controller" coupled to

them and maintaining known NAND flash address mapping and “adapted” to perform optional, also known, error management and wear leveling.

A. Characteristic Nature of NAND Flash Memory

A **NAND flash cell** is type of transistor with a floating gate that can retain electrical charges associated with “threshold voltages” that, applied to a control gate, allows conduction of electrical current from drain to source. (Sechen ¶¶ 26 [Fig. 2.1(a)], 40 [Figures 6 and 7 from Atwood {Ex. 1038}] and 41.)

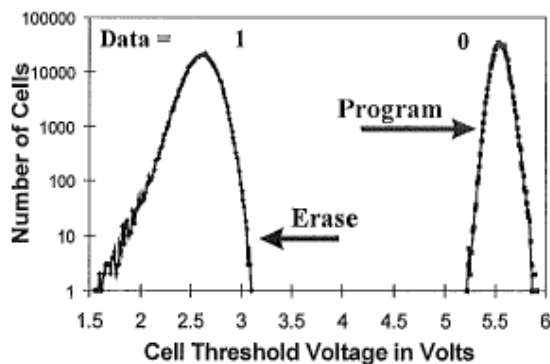


Figure 6: Single bit/cell array threshold voltage histogram

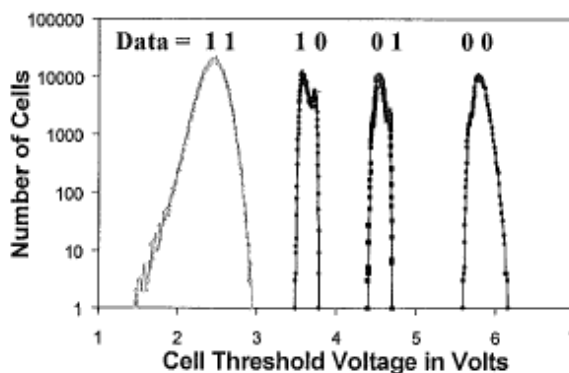


Figure 7: Two bit/cell array threshold voltage histogram

These threshold voltages may be chosen to represent information to be stored, in “classic” NAND memory operation, using two threshold voltage levels (Figure 6), the lower level to represent (“store”) a logical “1” and the higher level to store a “0” of one bit of digital computer data. (*Id.*) The same storage cell can use four threshold voltage levels (Figure 7) to represent four values corresponding to two bits of binary computer data (which in NAND memory operation is sourced from two distinct groups, “pages,” of logical data). (*Id.*) An n power of two (2^n : eight, sixteen, . . .)

threshold levels may be used in NAND flash operation to represent corresponding bits of n pages (*id.* ¶¶ 40 and 42-43). But a cell or group of cells do not constitute “memory,” which requires circuitry for selecting, programming (writing) and reading the cell or group of cells (*id.* ¶¶ 26 and 29).

To form **NAND flash memory**, storage cells are hard wired in strings (bit-line “columns”) and word-line “rows” forming “**pages**” each typically 2K storage cells **programmed** (written) **page by page**. (*Id.* ¶ 26.) NAND flash is so characterized by wiring of its storage cells in typically 64-page “**blocks**,” individually **erased in unison** to prepare for writing of new pages (*id.* ¶¶ 28-30). Unlike magnetic hard disk drives and other technologies that allow “write in place” of data at a physical location assigned to prior versions, in NAND flash programming, an update to stored data must be written to a physical location that is erased in preparation (“erase before write”); erasure, a much longer process than writing, is done in the background, when there are no user-requested read or write operations. (*Id.*) To maintain logical visibility to the user of a NAND flash memory device such as a Solid State Drive (“SSD”) (shown at Sechen ¶ 30), there are maintained and updated tables in or available to a **NAND flash device controller**, shown as a hardware module or chip on an SSD circuit board (*id.*) to “map” logical locations to physical locations in the NAND flash memory array (“**L2P mapping**”), which update for each data write (*id.* ¶¶ 30 and 31). The physical instances of NAND

flash pages and blocks determine the **Physical Block** Addresses (“PBA”) mapped from the construct of **Logical Block** Addresses (“LBA”). (*Id.* ¶¶ 32-34.) This mapping and remapping is performed with the software **Flash Translation Layer** (“FTL”) of the controller with **address tables** in **controller RAM** and **backup** in the flash memory. (*Id.* ¶¶ 31-38.) The physical reading, writing and erasing of NAND flash cells is performed by circuitry in a NAND flash memory module, shown in multiples in Sechen paragraphs 29 and 30 (“flash,” “flash memory” or just “NAND”) on a board, along with a block diagram identifying reading, writing and erasing functions (*id.* ¶ 29). A POSITA would understand this to be a **NAND flash memory or module**. (*Id.* ¶ 30.)

B. Characteristic NAND Flash Memory Management

Sechen paragraphs 34-38 outline common processes in the use of NAND flash memory. These include **bad block management** and **garbage collection** to make available adequate numbers of blocks for new writes without unnecessary, time-consuming erasures. Typically, “hot” data, *i.e.*, frequently updated (such as system) data, and “cold” (not-“hot”) data are clustered in respective physical blocks in order to facilitate efficient (fewer erase-and-re-writes) collecting of “valid” (un-updated) stored data and freeing up the blocks they otherwise occupy. Related “**wear leveling**” processes (“dynamic” at the time of writing and “static” in the background) even out write and erase stresses on NAND memory blocks – which have limited

expected “endurance” (“lifetime”) – aiming to avoid **premature failure** or retirement of enough blocks that would compromise system use. (Sechen ¶ 39 [system lifetime].)

C. Introduction of MLC and SLC Flash

Multi-level cell (MLC) NAND flash, developed in 1992-97, as described in Atwood (Ex. 1038), was the use of the NAND storage cell with four threshold voltage levels to represent two bits of information. (Sechen ¶¶ 40-41.) The first known use of the term “SLC” was in a 2001 article that called the established technology “**single-level program cell NAND flash (SLC)**” and compared it with then new MLC. (Ex. 1039, Sechen ¶ 42.) Although the terms have been shortened over the years, a POSITA would understand that “MLC” refers to the use of NAND storage cells, each storing two bits written in two passes – a “lower” (least significant bit, “LSB”) logical page and then a distinct “upper” (most significant bit, “MSB”) logical page. (*Id.* ¶ 43.) That is, MLC flash memory allows writing **two logical data pages into one physical page of memory**. As reviewed at Sechen paragraph 43 (particularly Sechen note 17), the programming of MLC memory is more complex and stressful than SLC because of MLC’s narrower window for distinct threshold charges and its multiple passes of writing; also, a page-wide set of latches (page buffer) is required for reading *each* level of logical page programming. Thus, a POSITA would understand that different circuitry is required for **MLC NAND flash**

memory than for SLC NAND flash memory, and that SLC NAND flash memory is incapable of storing more than one logical data page in one physical page of memory.

Two-state operation of MLC (later called **pseudo-SLC**) was disclosed by 2002. (Sechen ¶ 49; U.S. Patent No. 6,456,528 to Chen for “Selective Operation of a Multi-State Non-Volatile Memory System in a Binary Mode” [“Chen ‘528,” Ex. 1040] [one-bit *mode* of writing only one logical data page into one MLC physical page of memory]). This mode of MLC use, applying the MLC memory circuitry and pulsed/phased writing, has inferior performance and endurance relative to “real” SLC. A SanDisk suite of patents (incorporating by reference among others, Chen ‘528) disclosed lower-density (pSLC) *mode* use of MLC modules through partitioning and configuration for multiple purposes, including faster processing for caching writes and error management (*e.g.*, Gavens [Ex. 1045]; U.S. Patent No. 8,806,301 to Yu et al., published Apr. 14, 2011 [Ex. 1046], explained at Sechen ¶¶ 53-56).

D. Known Hybrid Use of SLC and MLC NAND Flash Modules with Strategies of Preferential Mapping, Wear Leveling and Error Management

Because of the compression of its threshold levels and its multiple passes of writing, MLC NAND flash was well-known to wear more quickly (have less “endurance”) and perform more slowly than SLC NAND flash. (Sechen ¶¶ 40-42.)

Thus, it was proposed as early as 2008 to use hybrid systems of **SLC modules** and **MLC modules** in which more **frequently written/updated data**, such as system data, user directories, and certain user files, would be written **preferentially to** a more robust **SLC module** while less frequently updated data would be written to the MLC module. (Sechen ¶ 46; Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008) [“Duann,” Ex. 1034]; U.S. Patent No. 8,078,794 to Lee et al., published Sept. 4, 2008 [“Lee ‘794,” Ex. 1041].)

This **SLC module preference** was applied in 2008-09 to a variety of **wear leveling** techniques to avoid premature failure of a system by some components reaching their endurance limits before others. (Sechen ¶¶ 47-48 and 58-60; *e.g.*, Sutardja [Ex. 1042]; Moshayedi [Ex. 1043].)

Additional tools or techniques were known in the art before the priority date to avoid premature failure by applying **error management near the end of life** of the system, with **preferential writing to SLC** upon failure of some “data integrity test” at an MLC location. (Sechen ¶¶ 53-56 and 58-61, *e.g.*, Gavens [Ex. 1045].)

The availability to the POSITA of these **preferential writing to SLC** techniques to avoid premature failure make obvious the “data integrity” claims 1 and 12 and the “wear leveling” claim 10 of the ‘300 patent. (Sechen Sections X(A), -(L) and -(J).)

V. THE ‘300 PATENT: Common Specification and Divergence of the ‘300 Claims

The common specification of the Lifetime Patents discloses no more technology than known, hybrid MLC and SLC NAND flash memory module systems with two proposed features of operation, variants of common flash wear leveling and error management. The first three patents claimed that known system with those operational features and were issued based on the perceived novelty of their recited “transfer” following “failure” of their recited “data integrity test.” In the 2018 application resulting in the ‘300 patent, the same 2012 system was rewritten in abstractions not mentioned in the specification, elevating to a claim element a RAVM ordinarily present in different capacities in flash memory systems and not clearly identified in the common specification, much less as an advance in the art.

A. The Common Specification Recited and Relied on a Known Hybrid System of MLC and SLC Modules and Its Operation.

The core disclosed system of known MLC NAND flash and SLC NAND flash modules is described multiple times in the specification. (*E.g.*, 4:18-23, 5:10-14, 7:3-9; Sechen ¶ 69.) Fig. 4 shows a physical memory device module including two banks each including 8+ **MLC flash memory modules** and 2+ **SLC NAND flash memory modules**). A controller “coupled” to the MLC and SLC modules performs L2P/FTL functions essential for NAND flash operation and also performs common wear leveling. (3:3-35 [BACKGROUND FTL/wear leveling]; *compare* Sechen ¶¶ 34-36.)

Only two features are proposed in the DETAILED DESCRIPTION, for “increasing the reliability and lifetime of a NAND flash storage system” (5:7-7:35).

The first, “data integrity test” feature is shown as the NAND flash method steps of Figs. 3A and 3B, explained in the text (6:15-52). Dr. Sechen identifies (§ 71) substantial ambiguities and inconsistencies even as to the disclosed comparison of “**stored data**” and “**retained data.**” The specification text is unclear as to whether addresses are compared or data written to those addresses (Sechen note 39) and what “**device controller memory**” is referenced at different steps (Sechen note 38). The only RAM mentioned is “**DRAM**” where data to be written to flash is held (6:18-20); “DRAM 20” of generic Fig. 1 is explained as “controlled” by the controller 14 among other possible memories such as rotating disk or the distinct MLC and SLC **modules** (5:34-52). But “**volatile memory**” is admitted in the ‘300 BACKGROUND for “**buffering, caching**” (3:63-64).

The second feature is functionally explained in two sentences, the first describing what appears to be wear leveling by “**allocat[ing]** ‘hot’ blocks i.e., those blocks that receive frequent writes, into the **SLC NAND flash memory module 28**, while allocating ‘cold’ blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26.” (6:53-65 [emphasis added].) The second sentence suggests implementation of the first by “**maintain[ing]** a count of those blocks that are accessed (written to) most frequently” and “**transfer[ring]** the

contents of those blocks into the SLC NAND flash memory module 28” – “on a periodic basis” such as “every 10,000 writes.” (6:59-63 [emphasis added].) Dr. Sechen identifies (§ 73) multiple fundamental ambiguities, including (1) whether the described functions refer to **logical or physical blocks**, (2) whether they are performed on a **dynamic** (writing as directed by the host) or **static** (background) basis, and (3) what is the “transfer” condition of “**periodic basis**” in view of the exemplary **threshold** (10K being the full expected MLC “life”).

B. The First Three Lifetime Patents on Operation of a Known Hybrid MLC-SLC NAND Flash Memory System.

Each of the first three Lifetime Patents claimed around the known, physical hybrid flash system of (1) “at least one **MLC** non-volatile memory **module** comprising a plurality of individually erasable blocks” (‘298 [Ex. 1005] 7:31-32, ‘385 [Ex. 1007] 7:14-15, ‘240 [Ex. 1009] 7:31-32 [claim 1] and 8:21-22 [claim 6] [emphasis added]), (2) “at least one **SLC** non-volatile memory **module** comprising a plurality of individually erasable blocks” (‘298 7:33-34, ‘385 7:16-17, ‘240 7:33-34 [claim 1] and 8:23-24 [claim 6] [emphasis added]), and (3) a **controller/FTL** “coupled” to the **modules** performing *ordinary* **L2P address mapping** functions (‘298 7:13-25, ‘385 7:19-28, ‘240 7:35-46 [claim 1] and 8:25-36 [claim 6]) and the *operational features* of **data integrity test** (‘298 7:26-32, ‘385 7:29-36, ‘240 7:47-54 [claim 1] and 8:42-49 [claim 6] and “**wear leveling**” (‘298 8:1-9, ‘385 7:41-8:4, ‘240 7:55-87 [claim 1] and 8:37-41 and 8:50-59 [claim 6])). As reviewed at

paragraphs 75-78 of the Sechen Declaration, the “point of invention” for each of these inventions over the multi-modal NAND flash system of U.S. Patent Appl. Pub. No. 2010/0172179 by Gorobets et al. (“Gorobets ‘179,” Ex. 1044) was found in the “**transfer**” action of the particular “wear leveling” recited (Sept. 2, 2014, [‘298] Notice of Allowability at 2 [Ex. 1006 at 80]; June 17, 2014, [‘298] Office Action at 7-8 [Ex. 1006 at 45-46]; Apr. 16, 2018, [‘240] Notice of Allowability at 2-3 [Ex. 1010 at 110-11] [“after reaching the **predetermined** count value of {accesses/**writes**} {emphasis added}”]).

C. 2018 ‘300 Patent Abstraction of the Disclosed Hybrid MLC-SLC Flash System.

On June 12, 2018 – six years after the April 25, 2012, filing of the specification common to all the Lifetime Patents – the application resulting in the ‘300 patent was filed with its original independent claim rewriting the base hybrid MLC-SLC NAND flash memory system into an unsupported and vague mix of “memory spaces” and “memory elements,” including “at least one random access volatile memory element” (June 12, 2018, [‘300] Application at 14 [Ex. 1012 at 14]), although the only RAVM mentioned in the common specification relating to any suggested invention was the “DRAM” where host data is received for the disclosed data integrity test (6:18-20) and “volatile memory” in the BACKGROUND art for “caching, buffering” (3:63-64). As explained at paragraphs 80 and 81 of the Sechen declaration, the new terms and recitations had no basis in the specification and made

no contribution to structural clarity (notice), but to the contrary, appeared intentionally vague to cover “lifetime” enhancing technology for other than the known and relied-upon (for operational structure) system of MLC and SLC NAND flash modules. As explained at paragraphs 82 and 83 of the Sechen declaration, confronted with continuing rejection over the Gorobets ‘179 (Ex. 1044) multi-modal NAND flash system, amendments were made that altered connections between the claim elements, introducing language in places that made claim elements nonsensical (*e.g.*, Sechen note 50 [“transfer of . . . stored data from . . . physical addresses . . . determined to have failed the data integrity test”). In partial resolution of the vagueness of “memory space,” the claims were amended so that the MLC and SLC “memory elements” were “mapped” to their respective “memory spaces,” that, with the recited controller mapping, made clear that those “memory spaces” were logical addresses or “logical address space,” although the RAVM became no longer an “element” mapped to its “volatile memory space” (Sechen note 51, discussing Oct. 8, 2020, [‘300] Amendment at 2-5 [Ex. 1012 at 71-74]). Ultimately, the ‘300 claims were allowed after an argument that the asserted art did not disclose enough “conventional cache” to perform the comparison of the recited data integrity test. (Sechen ¶ 83, quoting the argument at Oct. 8, 2020, [‘300] Amendment at 9 [Ex. 1012 at 78] and reciting the Examiner’s reliance at Jan. 27, 2021, [‘300] Notice of Allowability at 2 [Ex. 1012 at 86].)

VI. The Challenged Claims of the ‘300 Patent (37 C.F.R. § 42.104(b)(1):

Independent **claims 1 and 12** of the ‘300 patent rewrite the common specification description of “data integrity test” and “wear leveling” operations of a known hybrid system of MLC and SLC memory modules and controller (with well-understood L2P mapping functionality and needs) into abstract “memory space” with patched-on mapping of MLC and SLC “memory elements” and a vague RAVM (not “element”), with mapping to “maximize lifetime” and a data integrity test, failure of which results in remapping to a different physical address (not necessarily SLC) and a nonsensical transfer. The dependent claims limit claim 1. **Claim 2** qualifies the FTL recited in claim 1 as a software or firmware module. **Claim 3** requires the RAVM, MLC or SLC to be “embedded” in the controller. **Claims 4, 8, 9 and 11** require the MLC and SLC memory elements to be “flash” and MLC to store multiple bits per cell and SLC to be of higher endurance than MLC. **Claims 5 and 6** require the RAVM to be, respectively, DRAM and SRAM. **Claim 7** qualifies the data integrity test failure remapping to the SLC element. **Claim 10** requires periodic movement of “contents” of “frequently accessed” portions of the memory space to “SLC space.”

In view of the claims and disclosure of the ‘300 patent, the accompanying prior art references and supporting declaration of Dr. Sechen (Ex. 1002), Petitioner

respectfully requests cancellation of the Challenged Claims as summarized (pursuant to 37 C.F.R. § 42.104(b)(1), (2), -(4) and (5) below.

Grounds	Exhibits
<p>Ground 1: Claims 1-12 are unpatentable under U.S.C. § 103 as obvious over Gavens and incorporated disclosures in view of a POSITA’s knowledge of NAND flash technology.</p>	<p>1001, 1002, 1003, 1025, 1039, 1040, 1041, 1042, 1043, 1045, 1049, 1050, 1051, 1058</p>

VII. Person of Ordinary Skill in the Art

A person of ordinary skill in the art at the time of the claimed invention would have a bachelor’s degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least two years of experience in the design, development, implementation, or management of memory devices and systems. A person with an advanced degree in a relevant field would require less experience than noted above. As is common, one could obtain equivalent knowledge and perspective from other life experiences as well. (Sechen ¶¶ 60-61.)

VIII. 37 C.F.R. § 42.104(b)(3): CLAIM CONSTRUCTION

Under 37 C.F.R. § 42.100(b), claims in an *inter partes* review proceeding are construed using the same standard as that in a civil action. This includes “construing

the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent,” *id.* The standard for claim construction is set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

The following terms have distinct, established, customary meanings for a POSITA (Section IV *supra* and Sechen Section V) as proposed by Phison in the court litigation:

- “**MLC non-volatile memory**” means “**non-volatile memory cells arranged with circuitry capable of storing multiple logical pages in a single physical page of cells**” and
- “**SLC non-volatile memory**” means “**non-volatile memory cells arranged with circuitry incapable of storing multiple logical pages in a single physical page of cells**”

In the context of the ‘300 claims, the terms modify “**elements**,” which, for the claim amendment reasons set forth in Section V(C) *supra* (Sechen note 51), mean the **physical locations mapped** to their respective “**memory spaces**” as “**logical address spaces**.” The POSITA, backed by specification explanation of enhancing NAND flash system lifetime by wear leveling at a physical block level (e.g., 3:13-35, 6:53-65), would understand that the ‘300 patent “memory element” is a **physical flash memory block**. Thus, in this proceeding, “MLC memory element” and “SLC memory element” should be construed as NAND-mappable/addressable physical

blocks that are those distinct memory types and not just one-bit (1 programming level, 2 threshold voltage levels) versus n -bit (n programming level, 2^n threshold voltage levels) storage cells that are not themselves memories and addressable; and “memory space” should be construed as logical address space, subdivided by mapping to physical MLC and SLC memory (*also* Sechen ¶ 86).

Controller/FTL: Phison maintains the position in the court litigation the terms “controller” and “FTL” are indefinite for failure of the patent specification to disclose structure in the way of specific algorithms for its recited functions. As the Board cannot make that finding in this proceeding, Phison requests that the terms be construed as customary for the POSITA (*e.g.*, Sechen ¶¶ 31-38).

Phison maintains the position in the court litigation that the terms “**mapping** . . . to maximize **lifetime**” and “**remapping** . . . and **transfer** . . . to achieve enhanced **endurance**,” across claims of the Lifetime Patents, are indefinite. Phison requests that the terms be construed in accordance with the POSITA understanding that “maximizing **lifetime**” and “enhancing **endurance**” means acting to avoid premature failure of a NAND flash component (Sechen ¶¶ 39, 58-61, 81, and 87 and note 26). Phison also maintains the position in the court litigation that “data integrity test” means “a test that compares stored data to retained data.” Although that is not in dispute for the Challenged Claims, there are issues regarding both the location of the recited RAVM memory for “retained data” (Sechen note 38) and the

results of failure, where what is “transferred” is nonsensically recited (Sechen note 50) for which Phison will assert the PHOSITA’s understanding.

* * * * *

Grounds for Review Under 37 C.F.R. § 42.104(b)(4) -(5):

IX. Ground 1: The Challenged Claims Are Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA

Independent claims 1 and 12 of the ‘300 patent each claim a memory system that describes known hybrid MLC-SLC flash memory systems with known, necessary L2P mapping operations, including wear leveling to avoid premature unreliability of NAND flash systems, as admitted in the ‘300 BACKGROUND (Sechen ¶¶ 66, 67), detailed in multiple prior art textbooks, articles and patents (Sechen Section V(C), and in Gorobets ‘179 and Oribe relied upon by the ‘300 Examiner (Sechen ¶ 83). As a publication of such a system which includes error management disclosing the ‘300 patent data integrity feature, Gavens (Ex. 1045) and its incorporated references disclose or render obvious each of the Challenged Claims in view of the knowledge of the POSITA.

A. Claim 1 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

Gavens (Ex. 1045), among the SanDisk portfolio and incorporating by reference others of that portfolio,¹⁴ is a published reference that discloses a complete multi-modal NAND flash system with the ordinary L2P/FTL function of its controller, a variety of post-write read error detection and management schemes, and

¹⁴ See, e.g., U.S. Patent No. 6,456,528 to Chen (“Chen ‘528”), Ex. 1040, incorporated by reference at Gavens 16:29-40 (binary mode operation); U.S. Patent Appl. Pub. No. 2011/0153912 (“Gorobets ‘912”), Ex. 1049, incorporated by reference at Gavens 20:53-59 (post-write-read error management with binary mode portion); U.S. Patent No. 5,930,167 to Lee et al. (“Lee ‘167”), Ex. 1050, incorporated by reference at Gavens 17:57-67 (MLC with binary mode cache); U.S. Patent Appl. Pub. No. 2010/0172180, to Paley et al. (“Paley ‘180”), Ex. 1051, incorporated by reference at Gavens 8:41-42 (block management system). Also, U.S. Patent No. 5,936,971 to Harari et al. (“Harari”), Ex. 1057, was incorporated by reference by Paley ‘180 at ¶ [0027] (using RAM in write cache for flash). Hereinafter, it should be understood that reference to a specific portion of any of the above references is understood to be disclosed by Gavens due to incorporation by reference, as if the incorporated document was explicitly contained in Gavens.

the capability of and compatibility for employing other known tools used to avoid premature NAND system failure. (Sechen ¶¶ 58-61, 91.)

Although the Gavens system is not a “pure” SLC-MLC hybrid system, since the 2001 (*e.g.*, Cho, Ex. 1039) emergence of the terms “multi-level program cell” (MLC) memory and (thereby distinguished) “single level program cell” (SLC) memory, there have been implementations of hybrid MLC memory modules and SLC memory modules availing of the endurance advantages of SLC. (Sechen ¶ 92, *e.g.*, Lee ’794 [Ex. 1041], Sutardja [Ex. 1042], and Moshayedi [Ex. 1043].) Many NVM implementations disclosed in the SanDisk patent portfolio, such as Gavens, involve the partitioning and configuration of some MLC (or TLC) blocks for one-level (two states) or pseudo-SLC (pSLC) operation. (Sechen ¶ 92.) The pSLC mode of operation enjoys superior endurance compared to MLC in multi-level mode – though not as superior or as fast as “real” (native”) SLC memory which uses different circuitry. (Sechen ¶¶ 49, 92; *also* Gavens 12:6-10.) It would be obvious to a POSITA to use an MLC module operating entirely in pSLC mode (and thus be considered a pSLC memory module, which, as mentioned in [Sechen ¶ 49], are marketed as such), still with endurance superior to MLC in multi-level mode, or use a “real” or “native” SLC module, both with assured success. (Sechen ¶ 92.) Gavens clearly is a system for storing data as recited in the claim 1 preamble. (Sechen ¶ 95, Gavens Fig. 1 (90), 8:13-17.) It discloses or makes obvious, with its incorporated

references, each of the limitations of the following elements of claim 1 in view of the knowledge of the POSITA:

1. **[1a][1a1] memory space containing volatile memory space and nonvolatile memory space, [1a2] wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;**

The ‘300 patent claims construct of “memory spaces” and “memory elements” has no basis in the ‘300 patent specification and are ambiguous. (Sechen ¶¶ 80, 96.) To the extent that they refer to the aggregate of actual memory components in the claimed system, Gavens satisfies claim element [1a] by reciting memory components that satisfy the memory component limitations of claim elements [1c], [1d] and [1e], as explained in Sections [IX(A)(3)-(5) *infra*]. (Sechen ¶ 96.) As explained at [Sechen ¶¶ 80 and 86 and note 51], however, the amendment to claim elements [1c] and [1d] that MLC and SLC “memory elements” be “mapped” to “memory space” (7:45-48), where mapping had been recited as between “logical and physical addresses” (7:66-67), established that the “memory space” is the logical address space mapped to the corresponding MLC and SLC physical components at any particular point in time. (Sechen ¶¶ 80, 86 and 96 and notes 51 & 55.) This aligns with the “logical address space” seen by a host mapped to MLC and SLC memory in ordinary NAND flash operation, as admitted at the ‘300 BACKGROUND (2:30-3:13). (Sechen ¶¶ 32-34, 66 and 96; *see* Section [IX(A)(2)] *infra*). In this view, the

recited “memory space” and subdivisions are defined by mapping of the memory components as addressed by the controller, where the recited-for-the-first-time random access volatile memory (“RAVM,” “element” before amendment [Sechen ¶ 83]) is also addressed by the controller for “controlling access” to it (element [1g], 7:54-56); thus, the existence of the physical memories in the NAND flash system which are disclosed or obvious over Gavens (Sections [IX(A)(3)-(5) *infra*], elements [1c]-[1e]) establish the existence of the corresponding logical “memory spaces” recited in element [1a]. (Sechen ¶ 96.)

[1a1] The recited “memory space” is disclosed by the existence or definition of the memory components shown in Sections [IX(A)(3)-(5) *infra*], where “volatile memory space” is satisfied or defined by the RAVM of Section [IX(A)(5) *infra*] and the “nonvolatile memory space” is satisfied or defined by the MLC and SLC memories of Sections [IX(A)(3)-(4) *infra*]. (Sechen ¶ 97.)

[1a2] The recited “multilevel cell (MLC) memory space” is disclosed by the existence of or definition by the “MLC nonvolatile memory element” of Section [IX(A)(3) *infra*], and the recited “single level cell (SLC) memory space” is disclosed by the existence of or definition by the “SLC nonvolatile memory element” of Section [IX(A)(4) *infra*]. (Sechen ¶ 98.)

Thus, Gavens and its incorporated references, in view of the admitted art and the knowledge of the POSITA, disclose or make obvious element **[1a]**.

2. [1b] at least one controller to operate memory elements and associated memory space;

(Sechen ¶ 100):Gavens Fig. 1 shows controller 102. The controller 102 manages one or more memory chips 100 in the memory device 90. (8:17-18, 32-35.) Taking the “memory space” as logical addresses, in Gavens, “[a] memory block management system implemented in the controller stages the [logical] sectors and maps and stores them to the physical structure of the memory array” (8:36-39.)

Thus, Gavens discloses claim element [1b].

3. [1c] at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;

(Sechen ¶ 102): Gavens’s memory chip 100 “includes a memory array 200 of memory cells with each cell capable of being configured as a multi-level cell (“MLC”) (8:19-21). The memory array may be organized in erasable blocks erased together in a “flash” operation (Fig. 6, 11:4-20). The base memory chip of Gavens meets the characteristics of the POSITA-understood MLC flash memory module of cells, circuitry and programming explained in [Sechen ¶¶ 26-30, 42 and 43]. It meets Phison’s multiple level page programming construction (distinguished from single-level only SLC), as programming of those levels of logical pages is disclosed in Fig. 23 (25:18-26:30). As noted in [Sechen ¶ 100 and Section IX(A)(3) *supra*], the Gavens controller maps logical “memory spaces” to the physical memory (Gavens 8:36-39).

Thus, Gavens discloses claim element [1c].

4. [1d] at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;

(Sechen ¶104): Gavens does not disclose the use of a “native” SLC flash memory module or chip as described at [Sechen ¶¶ 26-30] because the Gavens memory module or chip 100 is capable, with its circuitry, of programming more than one logical page into a physical page, as explained in [Sechen ¶ 86]. However, Gavens discloses partitioning, configuration and use of portions of its memory array 200 in 1-bit mode, the “pseudo-SLC” mode explained at [Sechen ¶ 49]. Specifically, Gavens discloses, as a base system for multiple operational embodiments, “[a] first portion has each memory cell storing one bit of data and [a] second portion has each memory cell storing more than one bit of data” (4:32-34, 12:6-8 [calling memory operating in 1-bit mode “binary” or “SLC” memory]). Regarding one aspect of the difference, it is explained that the first portion, being “configured as lower density storage[,] . . . operates with a wider margin of error than that of the second portion” (18:16-20, also 12:6-10, 21:6-9). As explained in [Sechen ¶ 91], it would be obvious to a POSITA to substitute a “native” SLC flash memory module for the Gavens first portion, with a similar, if not wider margin of error than binary mode operation of MLC (*see* [Sechen ¶ 49]) and achieve similar, if not better results with the same NAND flash controller Fig. 1(102) with assurance of success. Again, the Gavens controller maps logical “memory spaces” to the physical memory (8:36-39) and

would be capable of writing to different NAND flash modules, as would be presumed in its memory array. As it is the memory module that performs the physical reading and writing based on controller commands and addresses, the NAND flash controller would be capable of writing to both MLC and “native” SLC (e.g., Moshayedi [Ex. 1043] Figs. 1, 2, ¶¶ [0036]-[0038] [controller 102 controlling virtual-to-physical mapping with RAM 214 for four channels of commercial SLC chips 112 and MLC chips 114]).

Thus, Gavens, in view of the POSITA’s knowledge of NAND flash, renders obvious claim element **[1d]**.

5. [1e] at least one random access volatile memory;

(Sechen ¶ 106): It is well-known to use RAVM (also known as “RAM”) in a NAND flash controller as a staging or cache location for data to be written to the flash memory. (E.g., Rao ‘916 [Ex. 1004] Fig. 3 [“Data Reg.”][, also ‘300 3:63-64 {“buffering, caching”}].) Gavens incorporated by reference Gorobets ‘912 (Ex. 1049) and Paley ‘180 (Ex. 1051), the latter expressly for block management ([note 14 *supra*]). Both share Fig. 1 showing a controller 100 with RAM 130, shown in Gorobets ‘912 Fig. 11 and Paley ‘180 Fig. 15 as “Cache (RAM) 102” within the controller. Gorobets ‘912 explains the controller cache 102 as one of a series of “high speed storage for temporarily storing data being passed between a higher speed component of the system” (¶ [0109]) and as a “volatile buffer memory . . . which is

typically part of the controller” for host-originated “logically consecutive data” before staging in the binary portion of MLC that it shares with the Gavens embodiment. Paley ‘180 similarly explains that “[t]ypically high-speed volatile RAM are employed . . . in a controller cache 102 of the memory controller.” (§ [0197].) Both Gorobets ‘912 and Paley ‘180 incorporated by reference ([note 14 *supra*]) (1) Harari (Ex. 1057), which shows as part of its Fig. 8 “cache buffer 705” as part of a cache system 701 “as part of the controller,” explained at 12:20-35, 13:24-42 and 12:58-14:11, and (2) Gorobets PCT (Ex. 1058), which explained:

The SRAM block 30 stores all temporary information [thus volatile memory] within the controller 16, this storing function includes [1] the buffering of [logical] sector data and [2] storage of control data structures and variables, as well as firmware code.

. . . .

During the operation of the controller all [logical] sector data being transferred between the logical interface 14 to host system 12, and the physical interface 18 to Flash memory 20 is buffered in the SRAM 30. Sufficient capacity in the SRAM 30 is allocated for buffering of two sectors

(11:10-12:3 [emphasis added].) A POSITA would also understand that there would be random access volatile memory for controller functions, including mapping (*e.g.*, Rao ‘916 [Ex. 1004] Fig. 3 [“InstReg.” and “Add- Map”]; Moshayedi [Ex. 1043] Fig. 2 [RAM 214]) as disclosed in Gavens, at least in incorporated references

Gorobets PCT 11:12-13 (quoted above, [2]), Gorobets ‘912 ¶ [0018] and Harari Fig. 8 (memory 709).

Thus, Gavens and its incorporated references disclose claim element [1e].

6. [1f] an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;

(Sechen ¶108): An FTL would be understood by the POSITA as the software layer supporting the L2P functions of a NAND controller (¶¶ 31-38 above, Micheloni [Ex. 1025] at 40, 492-98, and 516-17 [Fig. 18.3]), and thus is included within a NAND controller performing such functions as disclosed in Gavens. Gavens discloses the ordinary NAND controller function: “A memory block management system implemented in the controller stages the sectors and maps and stores them to the physical structure of the memory array” (8:36-39.) Gavens discloses updating of “a directory in a block management system embedded in the firmware of the controller (see Fig. 1)” to direct accesses to one or the other portions of the memory (17:17-19, 18:47-49, 18:64-66). Gavens, for further explanation of block management, incorporated by reference Paley ‘180 ([note 14 *supra*]):

(Sechen ¶ 109): Incorporated reference Paley ‘180 (Ex. 1051) provides further detail:

A memory-side memory manager 300 is implemented in the controller 100 of the memory system 90 to manage the storage and

retrieval of the data of host logical sectors among metablocks of the flash memory 200. The memory manager comprises a front-end system 310 and a back-end system 320. The front-end system 310 includes a host interface 312. The back-end system 320 includes a number of software modules for managing erase, read and write operations of the metablocks. The memory manager also maintains system control data and directory data associated with its operations among the flash memory 200 and the controller RAM 130.

(¶ [0155] [emphasis added]; *also* Gorobets ‘912 ¶ [0095].) Paley explains the use of “the currently prevalent LBA interface” (¶ [0020]). “The memory manager 300 is preferably implemented in the controller 100. It translates logical addresses received from the host into physical addresses within the memory array, where the data are actually stored, and then keeps track of these address translations.” (¶ [0150].) Referring to Fig. 9, “the media management layer 330” (¶ [0157]) and “dataflow and sequencing layer 340” (¶ [0158]) combine to perform the role of FTL. Specifically, the media management layer handles “updates, tables and lists used for logical-to-physical address translation and free block management, and wear leveling based on hot counts” (¶ [0201] [emphasis added]). As further explained in the incorporated Gorobets PCT (Ex. 1058), the media management layer is implemented in firmware “control[ling] the transfer of data sectors between the logical interface 14 to host 12 and the physical interface 18 to Flash memory 20” (Gorobets PCT 13:5-8 [emphasis added]) with the following algorithms:

The data structures required to support the Cyclic Storage [7:20-24: “method of ensuring uniformity of distribution of use”¹⁵] media management algorithms [18:1-10: (1) Data Write location to write host data, (2) Block Erase controlling erasure of obsolete data, (3) Block Sequencing of flash blocks used for storing data, and (4) Address Translation controlling “mapping of host logical addresses to physical memory addresses”] are stored principally in flash memory 10 together with the host data sectors, with only a very limited amount of control data being held temporarily in the control processor’s volatile RAM 30. Information held in the volatile memory 30 is non-critical, and can be reconstructed from flash memory if the power supply is interrupted.

(27:22-28:5 [emphasis added].) As explained at [Sechen ¶ 34], it was well-known, as corroborated by Goodson (submitted with the 2012 ‘298 application¹⁶), that the

¹⁵ An objective is “to obtain even use of blocks in the non-volatile memory for storage of data over a long period of operation, and to avoid ‘hot-spots’ in non-volatile memory usage, thereby increasing the reliability of the memory system.” (Gorobets PCT 2:4-8 [emphasis added].)

¹⁶ As explained at [Sechen ¶¶ 82 and 83], the Examiner maintained through several amendments that the independent claims of the ‘300 patent were obvious over Gorobets ‘179 (Ex. 1044) in view of Goodson, until allowance when the data integrity test was amended to recite what was to be compared.

address tables were loaded in controller RAVM and backed up in the flash memory. The NAND flash memory system disclosed in Gavens as further detailed in its incorporated references ([note 14 *supra*]), explained:

The top level of hierarchy of the mapping structure [Fig. 5 schematic of the “address translation process”] is the sector address table 52, which is a master table containing a physical address for every logical sector stored in the system 10 and which is stored in Flash memory 20. . . .

The sector address record 56 is a list stored in the controller’s memory volatile memory SRAM 30 It may also be reconstructed during device initiation from the sequence of recently written sectors which may be traced in the Flash memory 20. The intermediate temporary sector address table 54 is contained in flash memory 20 and is updated with the contents of the sector address record 56

This hierarchy of mapping structures . . . efficiently supports logical to physical address translation . . . even if electrical power is unpredictably removed from the system 10.

(Gorobets PCT [Ex. 1058] 26:11-27:21 [emphasis added].) Gavens thus discloses an FTL that maintains address tables in both the RAVM and the flash memory.

Thus, Gavens discloses claim element **[1f]**.

7. **[1g] [1g1] the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, [1g2] the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;**

(Sechen ¶ 111): Incorporated here the opinions and explanations in Sections [IX(A)(2)-(6) *supra*] regarding the L2P and block management operations of the Gavens controller, which are common to the NAND flash background art (‘300 2:21-3:12 [writing host data to NAND flash nonvolatile memory]; [Sechen ¶¶ 30-38]).

(Sechen ¶ 112): **[1g1]** It was shown in Sections [IX(A)(2)-(4) and (6) *supra*] that Gavens discloses a controller which “cooperates with the [NAND flash] memory chip [MLC partially operated in 2-state, pSLC mode, obviously substitutable with ‘real’ SLC] and controls and manages high level operations,” for example, a host write translated in logical sectors to the memory array (8:32-36); the operation obviously involves control of the RAM data cache or buffer disclosed by Gavens (Section [IX(A)(5) *supra*], e.g., incorporated Paley ‘180 ¶ [0197]).

(Sechen 113): **[1g2]** With the POSITA understanding that “such stored data” written to (and “to be stored” in) the NVM (flash), the recited “Write access” operation is satisfied by Gavens by “storing” data in the NVM that was and is cached

(temporarily stored or “retained”) in the disclosed RAVM, as further explained for the data integrity test element [1h].

Thus, Gavens and its incorporated references disclose or make obvious in view of the knowledge of the POSITA the ordinary NAND flash L2P mapping and writing operation of claim element [1g].

8. [1h] the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory;

(Sechen ¶ 115): As reviewed at [Sechen ¶¶ 53-55], Gavens discloses multiple techniques for error management, efficiently deployed near the end-of-life of a memory system. One discloses the ‘300 patent data integrity test as recited in element [1h].

(Sechen ¶ 116): In one variant of the Gavens post-write-read error management embodiment of Figs. 14 and 15 (explaining text at 16:13-17:42), user data is written to the higher density (*e.g.*, MLC) portion as a “first copy.” (Gavens 16:41-45.) Then, in a “post write read,” there may be a check for errors “by comparison with the original copy which may be cached” (16:46-49 [emphasis added]). If the number of error bits is less than a predetermined amount, the first copy is deemed valid and subsequent reads of the data page will be from that copy with any errors corrected by ECC. (16:50-56.) If the number is greater, then a copy is written to the lower

density, lower error rate (more robust, *e.g.*, pSLC) portion; this is performed in one embodiment by copying from a cached copy “of the original data.” (17:9-11.) As explained in Section [IX(A)(5) *supra*], in the Gavens NAND flash technology corpus, “[u]sing RAM in a write cache operating with flash memory has been disclosed” (*e.g.*, Gorobets ‘180 [Ex. 1049] ¶ [0024], Paley ‘180 [Ex. 1051] ¶ [0027]); thus, the “original data” temporarily stored (“cached” in RAM, understood to be RAVM) is compared to the stored (in flash) data, and if the stored data fails to match, the “original data” (temporarily stored or “retained”) is sent to the more robust pSLC. Thus, this error management variant discloses a data integrity test on written (stored) data that compares it against retained (cached) “original data” in RAM cache.

(Sechen ¶ 117): It is understood that these write and compare actions are directed by the controller. The use of “real” SLC memory instead of a binary-mode portion of the MLC memory does not affect element [1h] and does not increase overall latency, since “copying” of the “stored data” is from the MLC, involving relatively slow decoding (reading), and reading of the “retained data” is from relatively fast RAM; any subsequent “transfer” (write) for element [1j] would be faster for “real” SLC than pSLC (*see* [Sechen notes 11 & 45]).

Thus, Gavens and its incorporated references disclose claim element **[1h]**.

- 9. [1i] wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and**

(Sechen ¶ 119): Incorporated is the explanation in Section [IX(A)(6) *supra*] regarding Gavens’s use of address tables to map logical and physical addresses that may be blocks or pages in ordinary NAND flash operation. To the extent that the “maximize lifetime” limitation can be understood (*see* [Sechen ¶ 81]), Gavens’s (1) flash system media management wear leveling ([Sechen ¶ 108] and note [15 *supra*]) and (2) error management embodiment which satisfies (Section [IX(A)(10) *infra*]) claim element [1j] remapping and transfer for data integrity failure (to the extent **it** can be understood) each satisfy this limitation by enhancing lifetime.

Thus, Gavens and its incorporated references disclose claim element **[1i]**.

- 10.[1j] wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.**

(Sechen ¶ 121): As explained at [Sechen ¶ 81 and note 50] and as apparent from the text itself, the results of failure of the data integrity test of element [1h] are stated ambiguously with regard to placement of internal limitations and nonsensically for what is “transferred” (data “from those [physical addresses]

determined to have failed”). Construing claim element [1j] as requiring both remapping and transferring of the retained “original” data that was written to an originally mapped physical location from which a copy failed a data integrity test comparison, as explained in Section [IX(A)(8) *supra*], Gavens, in at least one disclosed error management technique, disclosed claim element [1j].

(Sechen ¶ 122): As explained in Section [IX(A)(8) *supra*], in the Gavens embodiment, after the data stored in the less robust (MLC) portion fails a data integrity test by exceeding a predetermined number of bit errors, the “original data” is rewritten to the more robust (pSLC) portion (Gavens 17:9-12). For that to occur, the original data must be remapped, and any “transfer” in this context is the writing of that original data to the remapped – different – location (physical address), thereby satisfying the remapping and transfer limitation of claim element [1j]. Whether the language “to achieve enhanced endurance” limits the transfer or the data integrity test is [ambiguous from the language of the claim], and the only clue provided in the specification was the apparent assumption that preferential mapping to superior endurance SLC helped [lifetime]. On that clue, the Gavens disclosed result of rewriting to the more robust (pSLC) memory satisfies the endurance enhancement limitation; and rewriting to an even more robust “real” SLC more so.

Thus, Gavens discloses or makes obvious, in view of the knowledge of the POSITA, claim element [1j].

* * * * *

In summary, Gavens and its incorporated references make obvious, in view of knowledge of the POSITA, each limitation of ‘300 claim 1.

B. Claim 2 to a Software FTL Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 125 and 126): Claim 2, the system of claim 1 “*wherein the FTL flash translation layer is a software module, or a firmware module containing software updates,*” is obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]): As explained in Section [IX(A)(6) *supra*], Gavens disclosed through its reference for block management (8:40-43), namely, Paley ‘180 (Ex. 1051) (¶¶ [0155]-[0159], [0201]), which further incorporated Gorobets PCT (Ex. 1058) [note 14 *supra*], disclosed the use of a media management layer and a dataflow and sequencing layer that perform: a) the L2P mapping/translation, and b) the wear leveling and block management functions of known FTL (*compare* ‘300 3:3-35, [Sechen ¶¶ 34-38]). The next sentence in Gavens (8:44-45) refers to firmware 60 to implement the functions of the controller, and Gorobets PCT disclosed its sector sequencer, media management layer and flash controller layer, “control[ling] the transfer of data sectors between the logical interface 14 to host 12 and the physical interface 10 to Flash memory 20,” specifically as firmware (12:22-13:8), clearly updatable as located in SRAM (11:10-13).

Gavens and its incorporated references disclose **claim 2**.

C. Claim 3, Limited to RAVM, MLC or SLC in the Controller, Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 128 and 129): Claim 3, the system of claim 1 “*wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller,*” is obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]): As explained in Section [IX(A)(5) *supra*], Gavens discloses, through incorporated references, the embedding of RAVM in the controller both as a data cache and as a temporary location for data for other controller functions (*e.g.*, respectively, Gorobets ‘912 [Ex. 1049] ¶ [0197], [0018] ; *also*, Gorobets PCT [Ex. 1058] 11:10-13 [both]). Although there was an argument made during prosecution of the ‘300 patent application that two “blocks” of “nonvolatile [sic, probably ‘volatile’] memory” were required for the data integrity test and that a “conventional cache” was not that large (¶ 83 above), there is no support in the specification for any hardware departure from the known hybrid MLC-SLC memory system and no claim is made to such a new hardware combination. Indeed, incorporated Gorobets PCT (Ex. 1058) explained that “[s]ufficient capacity in the SRAM 30 is allocated for buffering of two sectors” (11:24-12:2).

Thus, Gavens and its incorporated references disclose **claim 3**.

D. Claims 4, 7-9 and 11, Limited to the Nature of MLC and SLC Memory and Remapping to the Latter, Are Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 131-133, 141-142, 144-145, 147-148 and 158-159): Claims 4, 7-9 and 11, the system of claim 1 wherein [4] “*the MLC and SLC nonvolatile memory elements comprise flash memory,*” [7] “*the controller, upon detection of a failure of the data integrity test, remaps the data to the SLC nonvolatile memory element,*” [8] “[with the limitation of claim 7] “*the SLC memory element has a higher endurance than the MLC memory element,*” [9] “*the MLC is a multilevel cell, wherein the multilevel cell stores at least 2 bits per cell*” and [11] “*the MLC allows a single cell to store multiple bits,* are obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]): These limitations are inherent in the understood meanings of “MLC” and “SLC” and the superior endurance of SLC over MLC.

(Sechen ¶¶ 132 and 133 [**claim 4** “flash”]): Gavens, which would be understood by a POSITA to describe a NAND flash system with multiple MLC NAND flash modules, expressly describes its MLC non-volatile memory modules as including MLC NAND flash memory elements, which by definition are flash memory. (Fig. 4, 9:49-50 [page of memory cells in the memory array 200 is organized in the NAND configuration], 1:18-19, 4:14-18 [flash memory having a first portion and a second portion storing higher density compared to the first

portion], 2:65-66, 8:65-67 [flash memory devices with NAND string structures; Fig. 1 (90) [flash memory device].) As explained at [Sechen ¶¶ 92 and 104], a POSITA would readily and successfully substitute for Gavens’s partitions of MLC memory elements configured for 2-state pseudo-SLC operation an SLC non-volatile memory module which is understood to include SLC NAND flash memory elements. As to Gavens’s MLC NAND flash memory operated in pseudo-SLC mode, they are also described as flash memory. (Fig. 4, 9:49-50 [a page of memory cells in the memory array 200 is organized in the NAND configuration], 1:18-19, 4:14-18 [flash memory having a first portion and a second portion storing higher density compared to the first portion], 2:65-66, 8:65-67 [flash memory devices with NAND string structures], Fig. 1 [flash memory device 90].)

(Sechen ¶ 141 [**claim 7** remap to SLC]): As explained in Section [IX(A)(8) *supra*], in that Gavens error management embodiment, after the data stored in the less robust (MLC) portion fails a data integrity test by exceeding a predetermined number of bit errors, the “original data” is rewritten to the more robust (pSLC) portion (Gavens 17:9-12). (Sechen ¶ 145 [**claim 8** SLC endurance]): It is admitted art that SLC memory has higher endurance than MLC memory (‘300 3:44-50 [50-100K writes v. 3-10K writes]). The Gavens embodiment making obvious the system of claim 1 (Section X(A)) includes a portion of the memory having cells “configured as lower density storage . . . operating in two states [pSLC mode for] faster

programming and a longer operational life” (Gavens 16:19-35). (Sechen ¶¶ 141 and 145 [both claims]): As explained in [Sechen ¶¶ 92 and 104], it would be obvious to substitute “real” SLC memory for the pSLC portion in Gavens; it would be a faster process ([Sechen ¶ 117]) and arguably more endurance-enhancing ([Sechen ¶ 122]).

(Sechen ¶¶ 148 and 159 [**claims 9 and 11** MLC capacity]): It is admitted art that “MLC allows a single cell to store multiple bits, and accordingly to assume more than two values” (‘300 3:38-39). The Gavens embodiment making obvious the system of claim 1 (Section [IX(A) *supra*]) includes a portion of the memory having cells “configured as high density storage with each cell storing multiple bits of data” (Gavens 16:17-19).

Thus, Gavens and incorporated references, in view of the knowledge of the POSITA, disclose or render obvious **claims 4, 7-9 and 11**.

E. Claims 5 and 6, Limited to the Type of the RAVM, Are Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 135-136 and 138-139): Claims 5 and 6, the system of claim 1 “*wherein the random access volatile memory is*” [5] “*dynamic random access memory*” and [6] “*static random access memory,*” are obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]), in view of a POSITA’s understanding that dynamic random access memory (DRAM) and static random access memory (SRAM) are common types of random access volatile

memory (RAVM) that may be used for purposes of temporarily holding data to be compared as is the recited role of RAVM in claim 1, either would be an obvious choice for Gavens's cache of "original data" for comparison (16:47-49).

(Sechen ¶ 136 [**claim 5** DRAM]): The background art supports such use of DRAM for cache and other NAND flash functions. (*E.g.*, Moshayedi [Ex. 1043] Fig. 1 (106), ¶ [0028] [Dynamic Random Access Memory 106 shown external to but "can be present in controller 102" and "may be used to buffer data to be written into the flash array 108"], *also* ¶ [0004] [DRAM used in management of read and write operations of flash, contain addressing table correlating logical and physical addresses], ¶ [0053] [DRAM for linked lists, saved on SLC], ¶ [0054] [DRAM for tables and 4K logical blocks of data cache], ¶ [0067][suitable amounts of DRAM for different SLC-MLC combinations]; Duann (Ex. 1034), p. 6 [utilize DRAM as cache].)

(Sechen ¶ 139 [claim 6 SRAM]): Gavens discloses the use of SRAM through incorporation of Gorobets PCT (Ex. 1058) (11:10-12:3 [buffering of logical data and storage of control data and tables], *quoted* at ¶ 109 above; *also* Paley '180 Fig. 17, ¶¶ [0423]-[0425], [0502], [0503], [0506] [SRAM for storing "group address tables"])). Duann (Ex. 1034), p. 6, suggested "[b]igger internal SRAM as cache" for a hybrid SLC and MLC system.

Thus, Gavens, in view of the knowledge of the POSITA, makes obvious **claims 5 and 6.**

F. Claim 10, Limited To Include Wear Leveling, Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 150-156): Claim 10, the system of claim 1 “*wherein the contents of frequently accessed portions of the memory space are periodically moved from the MLC space to the SLC space,*” is obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]): It is admitted prior art that NAND flash memory systems use various wear leveling techniques “to attempt to ensure that ‘hot’ blocks, i.e., blocks that are frequently written, are not rendered unusable much faster than other blocks” (‘300 3:13-55). The Gavens NAND flash memory system that is the basis for the obviousness of claim 1 would be expected by the POSITA to employ one or more wear leveling techniques which can be applied compatibly with its error management system; in fact, for block management, Gavens incorporated by reference ([note 14 *supra*]) Paley ‘180 (Ex. 1051) which explained that the system’s media management layer handles, among other things, “wear leveling based on hot counts” (¶ [0201]), which incorporated Gorobets PCT (Ex. 1058). As reviewed at [Sechen ¶ 109 and note 15 *supra*], the disclosed media management firmware ensured uniform use of blocks of NVM, avoiding “hot-spots” and “thereby increasing the reliability of the memory system”

(Gorobets PCT 2:4-8). Dr. Sechen reviewed some of the known wear leveling art (Sechen ¶¶ 34-39, 46-48, and 58-61) as well as the ‘300 patent DETAILED DESCRIPTION of an apparent wear leveling embodiment (6:53-65).

(Sechen ¶ 152): As explained at [Sechen ¶ 73 and note 44], the two-sentence description left ambiguities as to whether logical or physical blocks were referenced and what “periodic basis” means when the only examples provided were threshold write counts, among others. As described at [Sechen ¶¶ 80 and 87], the introduction of the term “memory space” – which appeared in the specification only as a quantity of memory – as a claim term created a fundamental ambiguity. However, as explained at [Sechen ¶¶ 86 and 96 and note 51], an amendment during the ‘300 patent prosecution established that “memory space” is the logical address space that is mapped to physical MLC or SLC memory at a particular time. A reasonable construction of claim 10 is that it calls for remapping on a “periodic,” *i.e.*, “threshold count” basis, to SLC memory of a logical address range that has been “accessed” more than that threshold count. That construction reads on several prior art wear leveling procedures for mixed-level NAND flash reviewed at [Sechen ¶¶ 46-48 and 48-61]:

(Sechen ¶ 153): Lee ‘794 (Ex. 1041), explained and illustrated at [Sechen ¶ 46], discloses an embodiment by which “hot data,” determined by logical counts where the user file has been accessed more than a predefined number of times or the

access counter of a user file shows a high number of accesses, is sent to SLC memory (6:58-66).

(Sechen ¶ 154): Sutardja (Ex. 1042), explained at [Sechen ¶ 47], discloses a primary algorithm similar to Lee ‘794, mapping logical addresses with high write frequency (reported by the host) to the higher endurance (SLC) memory. (Fig. 7A (506) & (508). Branches from the main algorithm, where “time,” including counts of access to the physical memory in variations of wear leveling and “swapping” of data currently stored in physical locations [e.g., ¶ [0167], likely would meet other constructions of claim 10.

(Sechen ¶ 155): Moshayedi (Ex. 1043), explained at [Sechen ¶ 48], also discloses a similar process, where the drive

keeps track of the number of times that data for each logical block address (LBA) has been written to the flash memory, and determines whether to store newly received data associated with a particular LBA in SLC flash or in MLC flash, depending on the number of writes that have occurred for that particular LBA.

(¶ [0024]). As in Sutardja, there are optional processes that are based on actual wear counts on physical memory and “swapping” of data currently stored in physical locations (e.g., ¶¶ [0030], [0032]).

(Sechen ¶ 156): With the base Gavens disclosure of the claim 1 recited memory system with a data integrity test, a POSITA could select one or more of these or other wear leveling techniques to meet the limitation recited by claim 10.

Thus, Gavens and incorporated references, in view of the knowledge of the POSITA, make obvious **claim 10**.

G. Claim 12 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

Claim 12 differs from claim 1 in wholly inconsequential broadening of language from (1) subdivisions of “nonvolatile memory space” from claim element [1a] “[MLC/SLC] memory space” (7:39-42) to claim element [12a] “[MLC/SLC] space” (8:41-43 [claim 12]) and (2) mapping of MLC and SLC memory elements into claim element [1c] “MLC memory space” and [1d] “SLC memory space” to their mapping into claim elements [12c] and [12d] “nonvolatile memory space.” In addition, claim element [1f] recites an FTL, which, in some combination with the controller, “maintain[s] an address table in one or more of the memory elements and random access volatile memory” (7:50-53) while claim element [12b] requires that the controller “maintain an address table in one or more of the memory elements” (8:44-46). As shown in Section IX(A) *supra* for claim 1, claim 12 added no structure or process to the known, admitted hybrid MLC-SLC NAND flash system by recitation of abstract “memory spaces,” ambiguous RAVM, and location of ordinary L2P address maps. Published Gavens and its incorporated references disclose each

limitation of claim 12, in view of the knowledge of the POSITA as to reading of ambiguous or nonsensical terms or modifiers and the obvious substitution of “real” SLC for Gavens’s 1-bit mode use of multi-bit MLC.

1. [12a][12a1] memory space containing volatile memory space and nonvolatile memory space, [12a2] wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

Gavens and its incorporated references disclose an ordinary NAND flash memory system with MLC memory elements (blocks and pages), which may be operated in 1-bit, “pseudo-SLC” mode, and RAVM. These are either themselves “nonvolatile memory space [divided into “MLC” and “SLC”] and “volatile memory space” and with FTL mapping them to the logical address “memory space,” or, as compelled by the “mapping” requirements of claim elements [12c] and [12d], “mapped” to logical address “memory space” (Sechen ¶¶ 80, 86 and 96 and note 51). Further, it would be obvious, in view of the knowledge of the POSITA, to substitute “real” SLC memory for MLC memory blocks operating in 1-bit mode (Sechen ¶¶ 92 and 104). Thus, Gavens and its incorporated references, in view of the knowledge of the POSITA, disclose or make obvious element [12a]. See Section IX(A)(1) *supra* for corresponding element [1a] (Sechen ¶ 163 [difference inconsequential between [1a] “MLC/SLC memory space” and [12a] “MLC/SLC space”]).

2. [12b] at least one controller to operate memory elements and associated memory space, and to maintain an address table in one or more of the memory elements;

Gavens and its incorporated references disclose an ordinary NAND flash memory controller that operates MLC memory elements (blocks and pages) with FTL mapping them to the logical address “memory space,” including an address table in controller RAVM and MLC backup, thereby satisfying element [12b]. *See* Sections IX(A)(2) and –(6) *supra* for corresponding elements [1b] (controller operating MLC) and [1f] (address maps in RAVM and flash). (Sechen ¶ 164.)

3. [12c] at least one MLC nonvolatile memory element that can be mapped into the nonvolatile memory space;

Gavens discloses MLC nonvolatile memory (blocks and pages) mapped to logical address space associated with nonvolatile memory, satisfying element [12c]. *See* Section IX(A)(3) *supra* for corresponding element [1c] (Sechen ¶ 165 [no material difference for element [1c] mapping to “MLC memory space”]).

4. [12d] at least one SLC nonvolatile memory element that can be mapped into the nonvolatile memory space;

Gavens, in view of the knowledge of the POSITA, discloses SLC nonvolatile memory (blocks and pages) mapped to logical address space associated with nonvolatile memory, satisfying element [12d]. *See* Section IX(A)(4) *supra* for corresponding element [1d] (Sechen ¶ 166 [no material difference for element [1d] mapping to “SLC memory space”]).

5. [12e] at least one random access volatile memory;

Gavens and its incorporated references disclose this RAVM element [12e].

See Section IX(A)(5) *supra* for corresponding element [1e] (Sechen ¶ 167).

6. [12f] [12f1] the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, [12f2] the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

Gavens and its incorporated references, in view of the knowledge of the POSITA, disclose this data integrity test comparison with data retained in RAVM element [12f]. *See* Section IX(A)(7) *supra* for corresponding element [1g] (Sechen ¶ 168).

7. [12g] the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory;

Gavens and its incorporated references disclose this data integrity test comparison with data retained in RAVM element [12g]. *See* Section IX(A)(8) *supra* for corresponding element [1h] (Sechen ¶ 169).

8. [12h] wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

Gavens discloses this address table mapping to maximize lifetime element

[12h]. See Section IX(A)(9) *supra* for corresponding element [1i] (Sechen ¶ 170).

9. [12i] wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

Gavens discloses this data integrity test failure-and-remap/transfer element

[12i]. See Section IX(A)(10) *supra* for corresponding element [1j] (Sechen ¶ 171).

* * * * *

Thus, Gavens and its incorporated references, in view of the knowledge of the POSITA, make obvious claim 12. (Sections IX(G)(1)-(9) *supra*; Sechen ¶¶ 161-172.)

* * * * *

In sum, Gavens (Ex. 1045) and its incorporated references, in view of the knowledge of the POSITA, make obvious each of the Challenged Claims of the ‘300 patent. (Sections IX(A)-(G) *supra*; Sechen ¶¶ 90-173.)

* * * * *

X. THE PENDING LITIGATIONS IN THE WESTERN DISTRICT OF TEXAS DO NOT WARRANT DENYING INSTITUTION.

With eight current patents asserted by Vervain against Phison based on varying word claims to the same two “data integrity test” and “wear leveling” functions described in the same specification for a known hybrid SLC-MLC NAND flash memory, review by this Board is more appropriate than by the District Court where those word variations can escape scrutiny. Construction of the multiple terms of the eight patents are restricted in number (12) in the District Court (per “side” in related cases as present here), even counting contentions of indefiniteness. As demonstrated in the above-stated grounds (Section IX *supra*), the case against this patent is compelling. Balancing of the six factors set forth by the Board in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential) does not warrant denying institution here. Rather, institution would best serve the interest in “system efficiency, fairness, and patent quality” (*id.* at 5), allowing due resolution of the substantial patentability questions (*id.* at 15).

As to *Fintiv* Factor 5, the petitioner and defendant in the parallel proceeding are the same party. Phison filed this petition expeditiously, where it received first notice of Vervain’s assertion in the Complaint filed March 8, 2024, and the Amended Complaint filed May 13, 2024 (Ex. 1082). No substantive opinions have issued regarding the scope or validity of the Challenged Claims. The parallel proceeding is in an early stage: the Court recently granted-in-part Phison’s motion

to dismiss (*see* Docket List [Ex. 1080] entries 12, 24, 26 and 38), Phison has not otherwise answered, fact discovery has not yet proceeded beyond automatic disclosure and Phison's invalidity and subject-matter eligibility contentions were filed on August 16, 2024, and claim construction materials exchanged in accordance with the Scheduling Order (Ex. 1083). A *Markman* hearing, initially scheduled for December 5, 2024, is postponed until January 9, 2025. ([Ex. 1080] entry 39) Thus, as to Factor 3, there has not been overriding investment in the parallel proceeding; to the contrary, the requirements of the parallel proceeding limited Markman construction to twelve terms between the parties for eight patents of verbal variations of the same specification. Thus, as to Factor 4, there is overlap, in the greater inclusiveness of the requested review as the District Court will not consider all the issues properly raised in this Petition, pending PGR2024-00047, PGR2024-00048, IPR2025-00212, IPR2025-00213 and IPR2025-00214, and others that Petitioner may petition.

Factors 1 and 2 do not significantly weigh for or against instituting the requested IGR. Petitioner does not know if the District Court will stay the case if trial by this Board is instituted and the Court has *tentatively* set jury selection for December 15, 2025 (Scheduling Order [Ex. 1083] at 4).

Regarding the sixth factor, the merits strongly weigh in favor of instituting trial as shown through the strength of the grounds in this Petition. "Other

circumstances” favor institution. As described at note 4 *supra*, there are separate suits by Patent Owner Vervain (following the same template) against Phison and a customer (Kingston Docket List [Ex. 1081]). This presents the complexity of eight patents with method and apparatus claims that Vervain asserts against multiple, sometimes competing products (that thus must be held confidential between the defendants) that implicate third-party actors who may be implicated in divided or indirect infringement as users who select the configuration or performance of the claimed system. Moreover, unlike Phison, its customer defendant in the other case moved to dismiss for improper venue and to transfer (Kingston Docket List [Ex. 1081] entries 13 and 20) with attendant discovery and confidentiality proceedings (*id.* entries 15 and 16).

The interest of the public in cleaning away such verbal variants of questionable innovation in the eight Vervain patents are best served by the requested review. The Board may take notice that such litigation, if it reaches trial, will have been drastically reduced in claims and theories asserted – beginning with the limitation of terms for construction for eight patents. An IPR trial, in contrast, may resolve all Challenged Claims of a patent, substantially simplifying district court trial without the extensive district court discovery for which the America Invents Act offered this alternative before the Board. And, of course, Petitioner has shown its case to be compelling.

XI. CONCLUSION

Petitioner submits that for the reasons set forth above, it has been shown that more likely than not, the Challenged Claims are invalid under all of 35 U.S.C. § 103 and should reviewed by the Board and canceled.

Date: December 17, 2024

Respectfully submitted,
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CERTIFICATION OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above-captioned Petition for *Inter Partes* Review of U.S. Patent No. 10,950,300 (and accompanying exhibits), was served in its entirety on December 17, 2024, upon Patent Owner's correspondent of record via USPS Express Priority Mail:

*Patent owner's correspondent
address of record for U.S. Patent No. 10,950,300*

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CERTIFICATION OF WORD COUNT (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the attached Petition, including footnotes, but not the cover page, exhibit list, table of contents, mandatory notices, and certifications, contains 13,448 words, as measured by the Word Count function of Microsoft Word. This is less than the limit of 14,000 words as specified by 37 C.F.R. § 42.24(a)(i).

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