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Paper 9
Date: March 17, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,
Petitioner,

v.

VERVAIN, LLC,
Patent Owner.

PGR2024-00047
Patent 11,830,546 B2

Before STACEY G. WHITE, JON M. JURGOVAN, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

AMUNDSON, *Administrative Patent Judge*.

DECISION
Denying Institution of Post-Grant Review
35 U.S.C. § 324

I. INTRODUCTION

Phison Electronics Corporation ("Petitioner") filed a Petition requesting a post-grant review of claims 1–7 in U.S. Patent No. 11,830,546 B2 ("the '546 patent") (Exhibit 1001) under 35 U.S.C. §§ 321–329. Paper 2 ("Pet."). Vervain, LLC filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute a post-grant review. We may not institute a post-grant review unless we determine that "the information presented in the petition filed under section 321, if such information is not rebutted, would demonstrate that it is more likely than not that at least 1 of the claims challenged in the petition is unpatentable." 35 U.S.C. § 324(a) (2024).

After considering the Petition, the Preliminary Response, and the evidence of record, and for the reasons explained below, we determine that Petitioner has failed to demonstrate that it is "more likely than not" that at least one of the claims challenged in the Petition is unpatentable. Hence, we deny the Petition and do not institute a post-grant review.

II. BACKGROUND

A. Real Parties in Interest

Petitioner identifies itself as the sole real party in interest. Pet. 4. Patent Owner identifies itself as the sole real party in interest. Paper 4, 1. The parties do not raise any issue about real parties in interest.

B. Related Matters

Petitioner and Patent Owner identify the following civil actions as related matters involving the '546 patent:

- *Vervain, LLC v. Kingston Technology Co., Inc. et al.*, No. 1:24-cv-254 (W.D. Tex. filed March 7, 2024); and
- *Vervain, LLC v. Phison Electronics Corporation*, No. 1:24-cv-259 (W.D. Tex. filed March 8, 2024) (the "Texas case").

Pet. 2 n.4, 5; Paper 4, 1.

C. The '546 Patent (Exhibit 1001)

The '546 patent, titled "Lifetime Mixed Level Non-Volatile Memory System," issued on November 28, 2023, from U.S. Patent Application No. 17/203,385 filed on March 16, 2021. Ex. 1001, codes (21), (22), (45), (54). The '546 patent is a continuation of U.S. Patent No. 10,950,300 B2 ("the '300 patent") (Exhibit 1011). *Id.* at code (60). The applications that issued as the '546 patent and the '300 patent are part of a series of continuation applications with the earliest nonprovisional ancestor application filed on April 25, 2012. *Id.* at 1:7–22, code (60); Ex. 1011, 1:7–23, code (60).

The '546 patent incorporates by reference (1) U.S. Patent Application No. 12/256,362, filed on October 22, 2008, and issued as U.S. Patent No. 7,855,916 B2 ("the '916 patent") and (2) U.S. Patent Application No. 12/915,177, filed on October 29, 2010, and issued as U.S. Patent No. 8,194,452 B2 ("the '452 patent") (Exhibit 1004).[1] Ex. 1001, 1:23–31. The '452 patent is a continuation of the '916 patent. Ex. 1004, 1:8–10, code (63).

The '546 patent states that the disclosure relates to:

> a system and method for providing reliable storage through the use of non-volatile memories and, more particularly, to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use

[1] Patent Owner filed a copy of the '452 patent as Exhibit 2012.

> of a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage without substantially raising the cost of the NAND flash storage system.

Ex. 1001, 1:35–42, 7:7–11.

The ’546 patent explains that generally “MLC NAND flash enjoys greater density than SLC NAND flash, at the cost of a decrease in access speed and lifetime (endurance).” Ex. 1001, 3:32–35. For example, MLC NAND flash may withstand “between 3,000 and 10,000 writes,” while SLC NAND flash may withstand “between 50,000 and 100,000 writes.” *Id.* at 3:35–41. But “even SLC NAND flash has a considerably lower lifetime (endurance) than rotating magnetic media,” such as a hard disk drive (HDD). *Id.* at 3:35–37. The patent purports to address deficiencies in conventional storage systems by describing “various embodiments of a NAND flash storage system that provides long lifetime (endurance) storage at low cost.” *Id.* at 3:58–60.

To account for the differences in MLC NAND flash and SLC NAND flash and provide “reliable storage of data in non-volatile memory,” the ’546 patent discloses a storage system with a controller that maintains “two separate banks of NAND flash.” Ex. 1001, 4:64–5:2. A first bank “contains economical MLC NAND flash.” *Id.* at 5:2–3. A second bank “contains high endurance SLC NAND flash.” *Id.* at 5:3–4.

The controller may conduct “a data integrity test after every write” or alternatively only “as time permits.” Ex. 1001, 5:4–5, 5:51–54. “If a particular address range fails a data integrity test, the address range is remapped from MLC NAND flash to SLC NAND flash.” *Id.* at 5:5–7; *see id.* at 5:54–57. Because “the SLC NAND flash is used to boost the lifetime (endurance) of the storage system, it can be considerably lesser in amount

than the MLC NAND flash." *Id.* at 5:7–10. For instance, "a system may set SLC NAND flash equal to 12.5% or 25% of MLC NAND flash (total non-volatile memory storage space=MLC+SLC)." *Id.* at 5:10–12.

The '546 patent's Figure 1 (reproduced below) depicts a computer system with a NAND flash storage system:

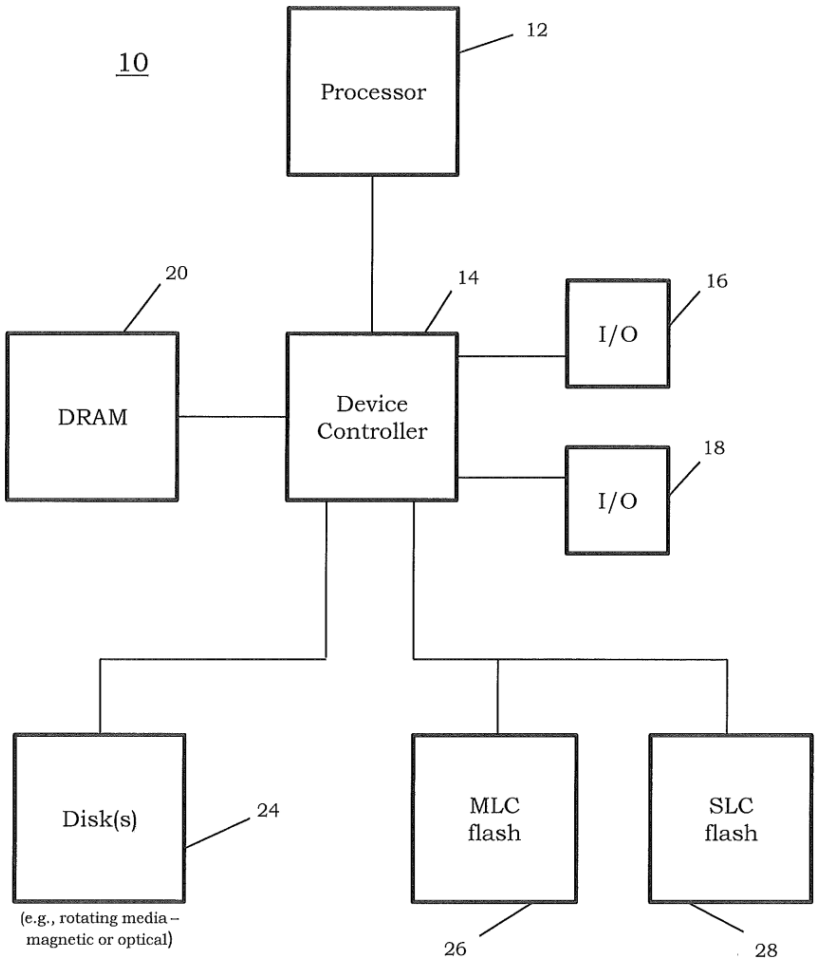


FIG. 1

Figure 1 illustrates computer system 10 including the following components:

- processor 12;
- device controller 14 coupled to processor 12;
- "a number of input/output ports 16 and 18" for device controller 14;

- dynamic random-access memory (DRAM) 20 coupled to device controller 14;
- "one or more disks 24, such as, for example, a rotating magnetic disk, or an optical disk," coupled to device controller 14;
- "MLC NAND flash memory module 26" coupled to device controller 14; and
- "SLC NAND flash memory module 28" coupled to device controller 14.

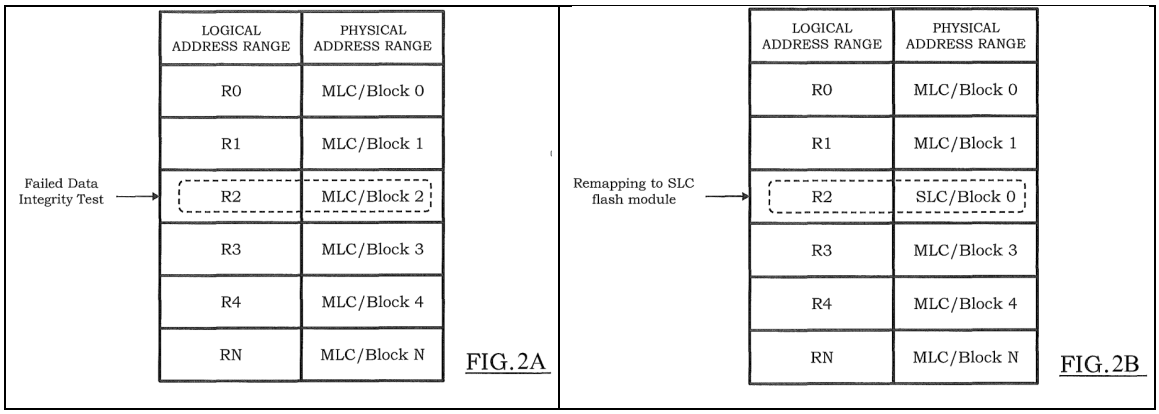
Ex. 1001, 4:50–51, 5:13–32, Fig. 1.

Device controller 14 maintains a translation table/address map that "maps logical computer system addresses to physical addresses in each one of the MLC- and SLC-NAND flash memory modules 26 and 28, respectively." Ex. 1001, 5:37–41. Because "MLC flash memory is less expensive than SLC flash memory, on a cost per bit basis, the translation table will initially map all logical NAND flash addresses to the MLC NAND flash memory module 26." *Id.* at 5:41–44. "The address ranges within the translation table will assume some minimum quantum, such as, for example, one block, although a smaller size, such as one page could be used, if the NAND flash has the capability of erasing the smaller size quantum." *Id.* at 5:44–48.

Computer system 10 uses a "read-modify-write" scheme "to write data to the NAND flash." Ex. 1001, 5:49–50. Specifically, data maintained in DRAM 20 is written "to an address within a particular address range" in MLC NAND flash memory module 26. *Id.* at 5:50–52. Then, device controller 14 reads the data in that address range "to ensure the integrity of the written data." *Id.* at 5:52–54. "If a data integrity test fails, the address range is remapped from the MLC NAND flash memory module 26 to the

next available address range in the SLC NAND flash memory module 28." *Id.* at 5:54–57.

The '546 patent's Figures 2A and 2B (reproduced below) depict an illustrative translation table/address map:



Above on the left, Figure 2A illustrates "a list of logical address ranges (R0–RN)" translated to physical address ranges in various blocks in MLC NAND flash memory module 26. Ex. 1001, 5:59–63, Fig. 2A. Figure 2A also illustrates an example failed data integrity test for the logical address range R2 corresponding to a "failed quanta of data" stored in block 2 in MLC NAND flash memory module 26. *Id.* at 5:63–67, Fig. 2A. Above on the right, Figure 2B illustrates the "failed quanta of data" from Figure 2A "remapped to the next available range of physical addresses" in SLC NAND flash memory module 28, i.e., SLC/block 0 in this example. *Id.* at 5:67–6:4, Fig. 2B.

The '546 patent discloses an embodiment where device controller 14 allocates "hot" blocks (those blocks that receive frequent writes) to SLC NAND flash memory module 28 and allocates "cold" blocks (those blocks that only receive infrequent writes) to MLC NAND flash memory module 26. Ex. 1001, 6:44–50. To do so, device controller 14 may "simply maintain a count of those blocks that are accessed (written to) most

frequently, and, on a periodic basis, such as, for example, every 1000 writes, or every 10,000 writes, transfer the contents of those blocks into the SLC NAND flash memory module 28." *Id.* at 6:50–56. By implementing a wear-leveling algorithm, device controller 14 attempts to ensure that "hot" blocks are "not rendered unusable much faster than other blocks." *Id.* at 3:4–10.

The '546 patent's Figure 4 (reproduced below) depicts a NAND flash module:

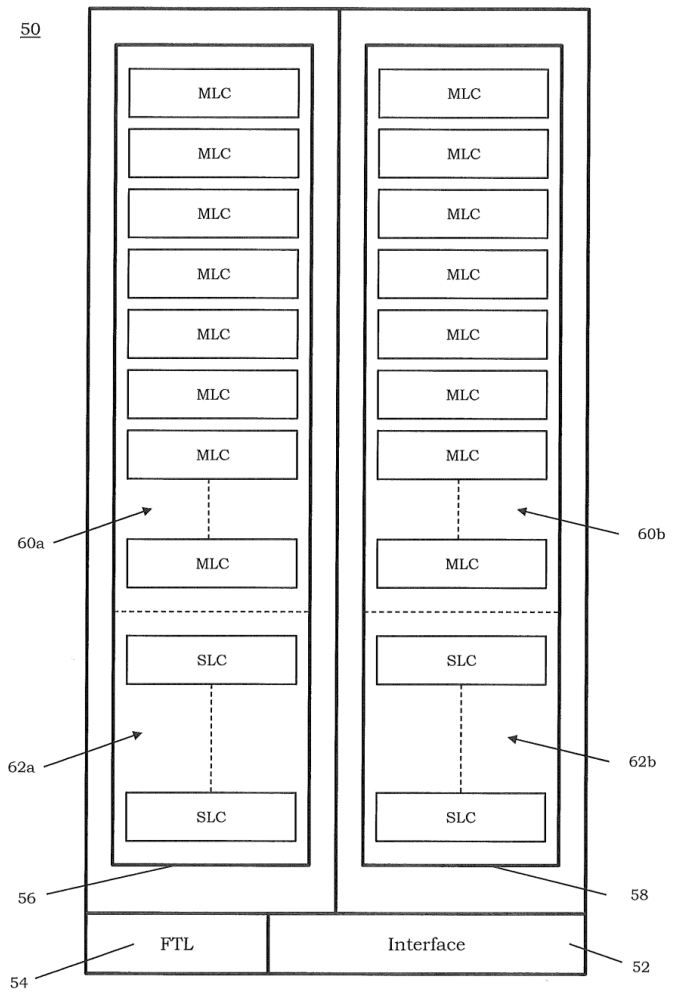


FIG. 4

Figure 4 illustrates NAND flash module 50 including the following components:

- NAND flash memory bank 56 comprising "a plurality of MLC NAND flash memory modules 60a and a plurality of SLC NAND flash memory modules 62a";
- NAND flash memory bank 58 comprising "a plurality of MLC NAND flash memory modules 60b and a plurality of SLC NAND flash memory modules 62b";
- "standard NAND flash interface 52"; and
- flash translation layer (FTL) logic 54 for managing interface 52 as well as NAND flash memory bank 56 and NAND flash memory bank 58.

Ex. 1001, 6:57–67, Fig. 4. In NAND flash module 50, FTL logic 54 may maintain a translation table/address map and perform other control functions instead of device controller 14. *Id.* at 7:1–6, Fig. 4.

D. The Challenged Claims

The '546 patent includes seven claims. Ex. 1001, 7:28–8:50. Independent claim 1 recites a "system for storing data." *Id.* at 7:28–8:34. Claims 2–7 depend directly from claim 1. *Id.* at 8:35–50. Petitioner challenges all seven claims. Pet. 1, 21–22, 28–76.

Claim 1 exemplifies the challenged claims and reads as follows (with formatting added for clarity and with bracketed numbers and letters added for reference purposes):[2]

1. [1pre] A system for storing data comprising:

   [1a] memory space containing

   [1a1] volatile memory space and

   [1a2] nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space;

[2] We use the same reference numbers and letters that Petitioner uses to identify the claim language. *See* Pet. 46–69.

[1b] at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements;

[1c] a bank of nonvolatile memory, including:

[1c1] a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and

[1c2] at least one SLC memory module including at least one SLC nonvolatile memory element;

[1d] at least one random access volatile memory element;

[1e] a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements;

[1f] the controller having associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data;

[1g] the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

> [1h] wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and
>
> [1i] wherein a failure of the data integrity test performed on the stored data by the controller results in
>
> > [1i1] a remapping of address space to a different physical range of addresses and
> >
> > [1i2] transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

Ex. 1001, 7:28–8:34.

E. The Asserted References

For its challenges, Petitioner relies on the following references:

Name	Reference	Exhibit
Gavens	US 8,634,240 B2, issued January 21, 2014 (based on an application filed September 1, 2010)	1045
Chen[3]	US 6,456,528 B1, issued September 24, 2002 (based on an application filed September 17, 2001)	1040
Gorobets[4]	US 2011/0153912 A1, published June 23, 2011 (based on an application filed December 18, 2009)	1049
Lee[5]	US 5,930,167, issued July 27, 1999 (based on an application filed July 30, 1997)	1050

[3] Gavens states that it incorporates by reference Chen's entire disclosure. Ex. 1045, 16:38–40.
[4] Gavens states that it incorporates by reference Gorobets's entire disclosure. Ex. 1045, 20:53–59.
[5] Gavens states that it incorporates by reference Lee's entire disclosure. Ex. 1045, 17:65–67.

Name	Reference	Exhibit
Paley[6]	US 2010/0172180 A1, published July 8, 2010 (based on an application filed January 5, 2009)	1051

Pet. 45–76.

At this stage of the proceeding, Patent Owner does not dispute that each reference identified above qualifies as prior art. *See, e.g.*, Prelim. Resp. 2, 49–86.

F. The Asserted Challenges to Patentability

Petitioner asserts the following challenges to patentability:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–7	101	Eligibility
1–7	112	Written Description
1–7	112	Enablement
1–7	112	Indefiniteness
1–7	103	Gavens[7]

Pet. 21–76.

G. Testimonial Evidence

To support its challenges, Petitioner relies on the declaration of Carl Sechen, Ph.D. (Exhibit 1002). Dr. Sechen states, "I have been asked to provide my expert opinions on a petition for post-grant review" of the '546 patent. Ex. 1002 ¶ 2. Dr. Sechen explains that he earned (1) a "B.E.E.

[6] Gavens states that it incorporates by reference Paley's entire disclosure. Ex. 1045, 8:40–43.
[7] When arguing unpatentability based on § 103, Petitioner relies on Gavens as well as several patent applications and patents that Gavens purports to incorporate by reference, e.g., Chen, Gorobets, Lee, and Paley. *See* Pet. 45–76.

in Electrical Engineering from the University of Minnesota in 1975," (2) an "M.S. in Electrical Engineering from the Massachusetts Institute of Technology in 1977," and (3) a "Ph.D. in Electrical Engineering from the University of California, Berkeley in 1986." *Id.* ¶ 8.

To support its positions, Patent Owner relies on the declaration of Sunil P. Khatri, Ph.D. (Exhibit 2001). Dr. Khatri states, "I have been retained on behalf of [Patent Owner], and its counsel, McKool Smith, P.C., as an expert in this proceeding." Ex. 2001 ¶ 1. Dr. Khatri explains that he earned (1) a "Bachelor of Science in Electrical Engineering in 1987 from the Indian Institute of Technology," (2) an "M.S. degree in 1989 from the University of Texas," and (3) a "Doctor of Philosophy degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley," in 1999. *Id.* ¶¶ 5, 7.

III. PATENTABILITY ANALYSIS

A. Eligibility for Post-Grant Review

The post-grant review provisions in § 6(d) of the Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011), apply only to patents subject to the AIA's first-inventor-to-file provisions. *See* AIA § 6(f)(2)(A) (explaining that the amendments made in § 6(d) "shall apply only to patents described in" § 3(n)(1)). Patents subject to the AIA's first-inventor-to-file provisions are those that issue from applications "that contain[] or contained at any time . . . a claim to a claimed invention that has an effective filing date . . . on or after" March 16, 2013. AIA § 3(n)(1). Additionally, a "petition for a post-grant review may only be filed not later than the date that is 9 months after the date of the grant of the patent or of the issuance of a reissue patent (as the case may be)." 35 U.S.C. § 321(c).

The ’546 patent issued on November 28, 2023. Ex. 1001, code (45). Petitioner filed the Petition on August 27, 2024, i.e., less than nine months after the date of the grant of the ’546 patent. Pet. 80. Patent Owner does not dispute that the ’546 patent is eligible for post-grant review. *See, e.g.*, Prelim. Resp. 15–86.

Because Petitioner has failed to show it is more likely than not that any of the challenged claims are unpatentable based on the merits of its challenges, we need not decide whether the ’546 patent is eligible for post-grant review. *See infra* §§ III.D.4, III.E.4, III.F.4, III.G.4, III.H.3–III.H.4. For purposes of analysis, we assume without deciding that the ’546 patent is eligible for post-grant review.

B. Level of Ordinary Skill in the Art

Factors pertinent to determining the level of ordinary skill in the art include (1) the educational level of the inventor; (2) the type of problems encountered in the art; (3) prior-art solutions to those problems; (4) the rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the educational level of workers active in the field. *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–97 (Fed. Cir. 1983). Not all factors may exist in every case, and one or more of these or other factors may predominate in a particular case. *Id.* These factors are not exhaustive, but merely a guide to determining the level of ordinary skill in the art. *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007). Moreover, the prior art itself may reflect an appropriate skill level. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Petitioner asserts that a person of ordinary skill in the art at the time of the alleged invention would have had “a bachelor’s degree in computer

engineering, electrical engineering, computer science, or a closely related field, along with at least two years of experience in the design, development, implementation, or management of memory devices and systems." Pet. 22–23. Petitioner also asserts that a "person with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the development and use of memory devices and systems." *Id.* at 23. Dr. Sechen's testimony supports Petitioner's assertions. *See* Ex. 1002 ¶ 58.

Patent Owner's declarant, Dr. Khatri, proposes a definition of the person of ordinary skill in the art. Ex. 2001 ¶ 24. Dr. Khatri, however, notes that his opinions would be the same under either his proposal or Petitioner's proposal. *Id.* ¶¶ 25–26. For purposes of the Preliminary Response, Patent Owner "adopts Petitioner's definition of a person of ordinary skill in the art." Prelim. Resp. 14 (citing Ex. 2001 ¶¶ 22–26).

Based on the current record and for purposes of this decision, we accept Petitioner's definition of a person of ordinary skill in the art because it comports with the technology and claims of the '546 patent as well as the asserted references. *See* Ex. 1002 ¶ 58; Ex. 2001 ¶¶ 24–26.

C. Claim Construction

1. Background

We construe claim terms "using the same claim construction standard" that district courts use to construe claim terms in civil actions for patent infringement. *See* 37 C.F.R. § 42.200(b). Under that standard, claim terms "are given their ordinary and customary meaning, which is the meaning the term would have to a person of ordinary skill in the art at the time of the invention." *Power Integrations, Inc. v. Fairchild Semiconductor*

Int'l, Inc., 904 F.3d 965, 971 (Fed. Cir. 2018) (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc)). The meaning of claim terms may be determined by "look[ing] principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

The "person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Phillips*, 415 F.3d at 1313. "Properly viewed, the 'ordinary meaning' of a claim term is its meaning to the ordinary artisan after reading the entire patent." *Id.* at 1321.

2. PETITIONER'S POSITION

Petitioner proposes explicit constructions for the following terms: (1) "module"; (2) "MLC memory modules"; (3) "SLC memory modules"; and (4) "comparing." *See* Pet. 23–27. Additionally, Petitioner identifies allegedly indefinite claim language. *Id.* at 27–28.

In particular, Petitioner proposes the following explicit constructions:

(1) "module" means "interchangeable unit" in the hardware context, such as a "chip" that "provides 'a complete function' such as the NAND flash chips that organize the NAND memory arrays operated in flash block erase and page writes";

(2) "MLC memory modules" means "[p]hysical modules each comprising an array of NAND cells as well as circuitry for writing two logical pages in two passes into a single row (physical page) of cells, for reading either

page in that single row of cells, and for erasing a block of cells at one time";

(3) "SLC memory modules" means "[p]hysical modules each comprising an array of NAND cells as well as circuitry for writing one logical page in one pass into a single row (physical page) of cells, for reading that page in that single row of cells, and for erasing a block of cells at one time"; and

(4) "comparing" means "direct bit-by-bit match."

Pet. 23–24, 27.

3. PATENT OWNER'S POSITION

Patent Owner disagrees with Petitioner's proposed constructions for "MLC memory modules," "SLC memory modules," and "comparing." *See* Prelim. Resp. 14–15. Patent Owner contends, however, that an explicit construction of those terms is "not necessary to resolve the parties' dispute regarding whether institution should be granted." *Id.* at 14.

Patent Owner notes that Petitioner's proposed constructions for "MLC memory modules" and "SLC memory modules" in this proceeding differ from Petitioner's proposed constructions for those terms in the Texas case. Prelim. Resp. 14–15 (citing Pet. 24; Ex. 2004, 2–3).

4. DISCUSSION

"[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy." *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *see Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Based on the current record, we determine that no claim term requires an explicit construction to decide whether Petitioner satisfies the "more likely than not" standard for instituting a post-grant review.

D. Alleged Failure to Claim Patent-Eligible Subject Matter Under § 101: Claims 1–7

1. LEGAL PRINCIPLES

The Patent Act defines patent-eligible subject matter broadly: "Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title." 35 U.S.C. § 101. In *Mayo* and *Alice*, the Supreme Court explained that § 101 "contains an important implicit exception" for laws of nature, natural phenomena, and abstract ideas. *Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 566 U.S. 66, 70 (2012); *Alice Corp. v. CLS Bank Int'l*, 573 U.S. 208, 216 (2014); *see also Diamond v. Diehr*, 450 U.S. 175, 185 (1981). In *Mayo* and *Alice*, the Court set forth a two-step analytical framework for evaluating patent eligibility. *Mayo*, 566 U.S. at 77–80; *Alice*, 573 U.S. at 217–18.

Under *Mayo*/*Alice* step one, we "determine whether the claims at issue are directed to" a judicial exception, i.e., an abstract idea, a law of nature, or a natural phenomenon. *Alice*, 573 U.S. at 217. Step one involves looking at the "focus" of the claims at issue and their "character as a whole." *Simio, LLC v. FlexSim Software Prods., Inc.*, 983 F.3d 1353, 1359 (Fed. Cir. 2020); *SAP Am., Inc. v. InvestPic, LLC*, 898 F.3d 1161, 1167 (Fed. Cir. 2018). Under *Mayo*/*Alice* step one, we "consider the patent's written description, as it informs our understanding of the claims." *CardioNet, LLC v. InfoBionic, Inc.*, 955 F.3d 1358, 1368 (Fed. Cir. 2020).

In January 2019, the Office issued revised guidance for determining whether claims are directed to a judicial exception. *See* 2019 Revised Patent

Subject Matter Eligibility Guidance, 84 Fed. Reg. 50 (Jan. 7, 2019) ("2019 Guidance").[8,9] The 2019 Guidance applies to the Board. *Id.* at 50–51, 57 n.42; *see* 35 U.S.C. § 3(a)(2)(A) (investing the Director with responsibility "for providing policy direction" for the Office).

The 2019 Guidance specifies two prongs for the analysis under *Mayo*/*Alice* step one (PTO step 2A). 84 Fed. Reg. at 54–55. Prong one requires evaluating "whether the claim recites a judicial exception, *i.e.*, an abstract idea, a law of nature, or a natural phenomenon." *Id.* at 54. "If the claim does not recite a judicial exception, it is not directed to a judicial exception," and it satisfies § 101. *Id.* "If the claim does recite a judicial exception, then it requires further analysis" under prong two. *Id.* Prong two requires evaluating "whether the claim as a whole integrates the recited judicial exception into a practical application of the exception." *Id.* "When the exception is so integrated, then the claim is not directed to a judicial exception," and it satisfies § 101. *Id.* "If the additional elements do not integrate the exception into a practical application, then the claim is directed to the judicial exception," and it "requires further analysis" under *Mayo*/*Alice* step two (PTO step 2B). *Id.*

Under *Mayo*/*Alice* step two, we "consider the elements of each claim both individually and 'as an ordered combination' to determine whether the

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[8] In response to received public comments, the Office issued further guidance in October 2019 with further explanations about various aspects of the 2019 Guidance. October 2019 Update: Subject Matter Eligibility (Oct. 17, 2019) (available at https://www.uspto.gov/sites/default/files/documents/peg_oct_2019_update.pdf).

[9] The Manual of Patent Examining Procedure (MPEP) now incorporates the 2019 Guidance and the October 2019 Update. *See* MPEP §§ 2103–21.06.07(c).

additional elements" add enough to transform the "nature of the claim" into "significantly more" than the judicial exception. *Alice*, 573 U.S. at 217–18, 221–22 (quoting *Mayo*, 566 U.S. at 78–79). Step two involves the search for an "inventive concept." *Alice*, 573 U.S. at 217–18, 221; *Univ. of Fla. Research Found., Inc. v. Gen. Elec. Co.*, 916 F.3d 1363, 1366 (Fed. Cir. 2019). "[A]n inventive concept must be evident in the claims." *RecogniCorp, LLC v. Nintendo Co.*, 855 F.3d 1322, 1327 (Fed. Cir. 2017).

2. PETITIONER'S CONTENTIONS

Petitioner challenges the '546 patent's claims as encompassing a patent-ineligible abstract idea. *See* Pet. 21, 28–30. In particular, Petitioner contends that:

(1) the '300 patent's claims substituted the term "memory space" for "the well-known SLC and MLC NAND flash modules" claimed in earlier ancestors of the '546 patent;

(2) the '546 patent is a continuation of the '300 patent;

(3) the '546 patent's claims recite "memory space";

(4) "memory space" corresponds to a "storage capacity property of a memory";

(5) the "unqualified claiming of a property is an abstract idea or 'disembodied concept' at the heart of" the Supreme Court's jurisprudence regarding patent eligibility; and

(6) the '546 patent's claims (a) "fail to integrate the claimed 'memory space' into a practical application" and (b) "do not provide an inventive concept to counterweigh (provide 'significantly more than') the unqualified claiming of the property of 'memory space.'"

Id. at 29–30 (emphases omitted) (citing Ex. 1001, 2:40, 5:10–12; Ex. 1002 ¶¶ 71, 73).

Petitioner also contends that the "unqualified nature" of claiming "memory space" extends to "subject matter well established to be outside of the scope of the patent statute." Pet. 30. According to Petitioner, the '546 patent's claims do not "require that the 'memory space' property be other than some transitory 'signal' (information)." *Id.* (citing *In re Nuijten*, 500 F.3d 1346 (Fed. Cir. 2007)).

3. PATENT OWNER'S CONTENTIONS

Patent Owner contends that Petitioner mischaracterizes the '546 patent's claims and improperly "untethers the single element of a 'memory space' from all the remaining claim language" to assert that the claims are "directed exclusively to this single element." Prelim. Resp. 23–24. Patent Owner contends that the claims are not directed to the abstract idea of a "memory space" but instead directed to a "system for storing data" that includes "device elements that are both physical and highly unconventional." *Id.* at 24 (quoting Ex. 1001, 7:28 (claim 1's preamble)) (citing Ex. 2001 ¶¶ 46–58). According to Patent Owner, the claimed "system for storing data" transfers "retained data to a different physical address based on a data integrity test where there is 'no apparent exception [i.e. abstract idea] recited in the claims,' thereby ensuring they are patent eligible." *Id.* at 25 (alteration by Patent Owner) (emphasis omitted) (quoting Ex. 2008 (PTO Subject Matter Eligibility Examples), 22).

Patent Owner also contends that "additional limitations" other than "memory space" make clear that "the claims cannot be directed to a transitory signal, as no transitory signal could read on, among other limitations, 'at least one controller to operate memory elements.'" Prelim. Resp. 24 (quoting Ex. 1001, 7:33 (limitation 1b)).

Patent Owner asserts that the claimed "system for storing data" improves computer functionality by "allowing for selective mapping between a higher capacity, but lower endurance MLC module, and a higher endurance, but lower capacity SLC module, based in part on a 'data integrity test' on data in an MLC module." Prelim. Resp. 26 (citing Ex. 1001, 5:2–10; Ex. 2001 ¶¶ 52–58). Patent Owner explains that this "selective mapping between different memory modules helps to optimize memory storage to improve system capacity, endurance, and access speed." *Id.* (citing Ex. 1001, 4:20–31; Ex. 2001 ¶¶ 54–58).

Patent Owner asserts that the claimed "system for storing data" addresses "a meaningful technical problem arising from the need to balance the various parameters of capacity, endurance, and accessibility in memory systems." Prelim. Resp. 26–27 (citing Ex. 2001 ¶¶ 51–58). Patent Owner asserts that the claimed "system for storing data" provides "a meaningful technical solution to this problem by, among other things, remapping logical memory to different physical addresses if data stored in an MLC nonvolatile memory element fails a data integrity test." *Id.* at 27. Patent Owner explains that the claimed remapping improves "the performance of the memory system by, for example, ensuring that data is reliably stored in locations of memory where integrity is not in doubt." *Id.*

4. ANALYSIS

Based on the current record, Petitioner does not establish sufficiently for purposes of institution that the '546 patent's claims are ineligible for patenting under § 101. *See* Pet. 28–30; Ex. 1002 ¶¶ 71–73, 76–77. After analyzing the '546 patent's claims as a whole in light of the patent's written description, we determine that the claims do not recite an abstract idea and

are not directed to an abstract idea under *Mayo*/*Alice* step one. *See* Ex. 1001, 7:28–8:50; Ex. 2001 ¶¶ 46–58.

For instance, claim 1 recites a "system for storing data" and requires "memory space" encompassing "at least one random access volatile memory element," "a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element," and "at least one SLC memory module including at least one SLC nonvolatile memory element." Ex. 1001, 7:28–32, 7:37–42; *see* Ex. 2001 ¶¶ 46–47. According to Petitioner, a hardware "chip" exemplifies a "module." Pet. 24; *see* Ex. 1002 ¶ 62. Additionally, "SLC and MLC do not denote an abstract concept, but rather are ways to implement a physical memory system." Ex. 2001 ¶ 47. Hence, we understand "memory space" as referencing physical memory rather than an abstract property.

Also, claim 1 requires "circuitry to read and write data from/to the memory cells." Ex. 2001 ¶¶ 48, 50; *see* Ex. 1001, 7:28–8:34. In particular, claim 1 recites (1) "at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements" and (2) "a flash translation layer (FTL)." Ex. 1001, 7:33–36, 7:43. Further, claim 1 specifies that the "at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements," and that the "controller perform[] a data integrity test on stored data." *Id.* at 7:43–46, 8:10–11.

Because claim 1 requires "memory modules," e.g., hardware "chips," and "circuitry to read and write data from/to the memory cells," claim 1 does not encompass a "transitory 'signal' (information)," contrary to Petitioner's

contention. *See* Ex. 1001, 7:28–8:34; Ex. 2001 ¶¶ 46–48, 50; Pet. 30. Although Petitioner cites the *Nuijten* decision as support for its argument that the challenged claims are "directed to an abstract idea," that decision addressed whether claims reciting a transitory "signal" were "directed to statutory subject matter," i.e., "process, machine, manufacture, or composition of matter." *See Nuijten*, 500 F.3d at 1353–54; Pet. 28–30.

As for Petitioner's argument that the challenged claims are "directed to an abstract idea," we disagree based on the current record. *See* Pet. 28–30. Instead, we agree with Patent Owner that the claimed "system for storing data" improves computer functionality by "allowing for selective mapping between a higher capacity, but lower endurance MLC module, and a higher endurance, but lower capacity SLC module, based in part on a 'data integrity test' on data in an MLC module." *See* Ex. 1001, 4:64–5:12, 7:28–8:50; Ex. 2001 ¶¶ 49, 51–58; Prelim. Resp. 26. Specifically, to account for the differences in MLC NAND flash and SLC NAND flash and provide "reliable storage of data in non-volatile memory," the '546 patent discloses and claims a storage system with a controller that maintains separate types of NAND flash, i.e., "economical MLC NAND flash" and "high endurance SLC NAND flash." Ex. 1001, 4:64–5:4, 7:28–8:34; *see* Ex. 2001 ¶¶ 53–55.

The controller may conduct "a data integrity test after every write" or alternatively only "as time permits." Ex. 1001, 5:4–5, 5:51–54; *see* Ex. 2001 ¶¶ 56–57. "If a particular address range fails a data integrity test, the address range is remapped from MLC NAND flash to SLC NAND flash." Ex. 1001, 5:5–7; *see id.* at 5:54–57; Ex. 2001 ¶ 57. Because "the SLC NAND flash is used to boost the lifetime (endurance) of the storage system, it can be

considerably lesser in amount than the MLC NAND flash." Ex. 1001, 5:7–10. For instance, "a system may set SLC NAND flash equal to 12.5% or 25% of MLC NAND flash (total non-volatile memory storage space=MLC+SLC)." *Id.* at 5:10–12.

Because the claimed "system for storing data" improves computer functionality, the claims are directed to a technological improvement rather than an abstract idea. *See* Ex. 1001, 4:64–5:12, 7:28–8:50; Ex. 2001 ¶¶ 49, 51–58; *Visual Memory LLC v. NVIDIA Corp.*, 867 F.3d 1253, 1259 (Fed. Cir. 2017) (deciding that the claims satisfied § 101 under *Mayo*/*Alice* step one because the claims were directed to "a technological improvement," i.e., "an improved computer memory system").

For the reasons discussed above, the '546 patent's claims do not recite an abstract idea and are not directed to an abstract idea under *Mayo*/*Alice* step one. Hence, Petitioner does not establish sufficiently for purposes of institution that the '546 patent's claims are ineligible for patenting under § 101. *See* Pet. 28–30; Ex. 1002 ¶¶ 71–73, 76–77; 84 Fed. Reg. at 54.

E. Alleged Failure to Satisfy § 112's Written-Description Requirement: Claims 1–7

1. Legal Principles

A patent's specification must "contain a written description of the invention." 35 U.S.C. § 112(a). The written-description requirement serves to "clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc) (alteration by the court) (quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563 (Fed. Cir. 1991));

see Blue Calypso, LLC v. Groupon, Inc., 815 F.3d 1331, 1344 (Fed. Cir. 2016).

The "test for sufficiency is whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Ariad*, 598 F.3d at 1351; *Mentor Graphics Corp. v. EVE-USA, Inc.*, 851 F.3d 1275, 1296 (Fed. Cir. 2017). The "test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art." *Ariad*, 598 F.3d at 1351.

While the written-description requirement "does not demand any particular form of disclosure" or "that the specification recite the claimed invention *in haec verba*, a description that merely renders the invention obvious does not satisfy the requirement." *Ariad*, 598 F.3d at 1352. The analysis for disclosure sufficiency may consider "such descriptive means as words, structures, figures, diagrams, formulas, etc." *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997).

2. PETITIONER'S CONTENTIONS

Petitioner challenges the '546 patent's claims as failing to satisfy § 112's written-description requirement. *See* Pet. 21, 30–37. In particular, Petitioner contends that the '546 patent lacks support for the following claim terms and limitations:

(a) "memory space";

(b) "memory element";

(c) "wherein the mapping is performed as necessitated by the system to maximize lifetime";

(d) "transfer of data corresponding to the retained data to those remapped physical addresses from those physical

addresses determined to have failed the data integrity test"; and

(e) "at least one . . . memory element," i.e., "at least one MLC nonvolatile memory element" and "at least one SLC nonvolatile memory element" in "a bank of nonvolatile memory."

See id. at 31–37.

More specifically, Petitioner asserts that the term "memory space" is "unsupported for other than NAND flash operation." Pet. 31–32 (citing Ex. 1002 ¶¶ 71, 73, 80). Petitioner asserts that the term "memory element" is "not even mentioned in the specification." *Id.* at 32. Further, Petitioner asserts that the specification contains no "mention of 'maximiz[ing] lifetime' of anything." *Id.* at 33 (alteration by Petitioner).

3. PATENT OWNER'S CONTENTIONS

As explained below, Patent Owner disputes that the '546 patent's claims fail to satisfy § 112's written-description requirement. *See* Prelim. Resp. 2, 27–35.

(a) "Memory Space"

Regarding the term "memory space," Patent Owner contends that Petitioner "does not clearly identify or explain the basis for its challenge" because its "argument spans only four sentences, beginning as an apparent written description challenge but later ambiguously referencing enablement." Prelim. Resp. 28 (citing Pet. 30–31). Patent Owner contends that "neither [Patent Owner] nor the Board should be forced to guess what Petitioner is arguing." *Id.*

Additionally, Patent Owner contends that the term "memory space" describes where data is stored. Prelim. Resp. 29; *see id.* at 36–37. Then,

Patent Owner quotes the ’546 patent’s disclosure that the “total non-volatile memory storage space=MLC+SLC.” *Id.* at 29 (quoting Ex. 1001, 5:12). Patent Owner explains that this disclosure “indicates that there are two spaces—MLC and SLC—where data is stored, and the total space is the combination of the two.” *Id.* (citing Ex. 2001 ¶ 64). Further, Patent Owner cites the ’546 patent’s Figures 1, 2A–2B, and 4 as showing “examples of MLC and SLC memory space.” *Id.* at 29–30.

(b) <u>“Memory Element”</u>

Patent Owner contends that the term “memory element” describes an element of memory. Prelim. Resp. 31 (citing Ex. 2001 ¶ 65); *see id.* at 37 (citing Ex. 2001 ¶¶ 76–81). Patent Owner contends that the “specification shows in great detail, albeit with different words, how MLC and SLC memory elements are used to store data,” e.g., an SLC flash memory cell storing a single bit of data and an MLC flash memory cell storing multiple bits of data. *Id.* at 31 (citing Ex. 1001, 2:5–11, 5:33–6:67, Figs. 1, 4). Further, Patent Owner asserts that the Federal Circuit has held that (1) “the specification does not need to use the exact language of the claims” and (2) “it is unnecessary to ‘recite the claimed invention *in haec verba*.’” *Id.* (quoting *Ariad*, 598 F.3d at 1352).

Additionally, Patent Owner notes that the ’546 patent incorporates by reference the ’452 patent. Prelim. Resp. 37 (citing Ex. 1001, 1:24–31). Then, Patent Owner quotes the ’452 patent’s disclosure that “an exemplary NAND memory integrated circuit [is] one element of the . . . nonvolatile memory system.” *Id.* (second alteration by Patent Owner) (quoting Ex. 1004, 2:52–54).

(c) "Wherein the Mapping Is Performed . . . to Maximize Lifetime"

Regarding the limitation "wherein the mapping is performed as necessitated by the system to maximize lifetime" in claim 1, Patent Owner contends that Petitioner's argument "is again disjointed, beginning as a written description challenge but including references to enablement, and fails to articulate a clear argument." Prelim. Resp. 31 (citing Pet. 33–35).

Additionally, Patent Owner contends that the '546 patent explains that "mapping is performed to increase the 'reliability and lifetime' of the memory." Prelim. Resp. 31–32 (citing Ex. 1001, 1:35–42). As support, Patent Owner cites the '546 patent's Figures 2A–2B and 3A–3B as showing how "data is remapped to boost or prolong the lifetime of the system." *Id.* at 32.

As further support, Patent Owner identifies the '546 patent's disclosures that:

(1) if "there is failure of a data integrity test, the data is transferred to a block with higher endurance"; and

(2) if "a block is heavily used, the data is mapped to a block that is less-used, or a higher-performance block."

Prelim. Resp. 32 (citing Ex. 1001, 3:19–26, 5:54–57, 6:50–56). Patent Owner contends that "[i]n each case, the lifetime of the memory is maximized." *Id.*

(d) "Transfer of Data . . ."

Regarding the limitation "transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test" in claim 1, Patent Owner cites the '546 patent's Figures 2A–2B and 3A–3B as support. Prelim. Resp. 32. Patent Owner contends that Figures 2A–2B and the

related disclosures "describe remapping a 'physical address range' after a 'failed data integrity test.'" *Id.* Patent Owner contends that Figures 3A–3B and the related disclosures "describe transferring data to the remapped address." *Id.* (citing Ex. 1001, 6:5–43 (describing Figs. 3A–3B)).

(e) "At Least One . . . Memory Element"

Regarding the phrase "at least one . . . memory element," Patent Owner asserts that the '546 patent's specification "clearly conveys possession." Prelim. Resp. 33. As support, Patent Owner cites the '546 patent's Figures 2A–2B and 4 as showing "MLC and SLC memory elements," i.e., MLC and SLC blocks in Figures 2A–2B and MLC and SLC flash memory modules in Figure 4. *Id.* at 34.

4. ANALYSIS

Based on the current record and for the reasons explained below, Petitioner does not establish sufficiently for purposes of institution that the '546 patent's claims fail to satisfy § 112's written-description requirement. *See* Pet. 30–37; Ex. 1002 ¶¶ 64–73.

(a) "Memory Space"

As support for the term "memory space," the '546 patent explains that because "the SLC NAND flash is used to boost the lifetime (endurance) of the storage system, it can be considerably lesser in amount than the MLC NAND flash." Ex. 1001, 5:7–10; *see* Ex. 2001 ¶ 85. Then, the patent provides a specific example where "a system may set SLC NAND flash equal to 12.5% or 25% of MLC NAND flash (total non-volatile memory storage space=MLC+SLC)." Ex. 1001, 5:10–12; *see* Ex. 2001 ¶¶ 64, 74. An ordinarily skilled artisan would understand this as disclosing that "there

are two spaces—MLC and SLC—where data is stored, and the total memory space is the combination of the two." Ex. 2001 ¶ 64.

Further, the '546 patent's Figure 1 depicts "memory space," e.g., dynamic random-access memory (DRAM) 20, one or more disks 24, MLC NAND flash memory module 26, and SLC NAND flash memory module 28. Ex. 1001, 5:24–32, Fig. 1; *see* Ex. 2001 ¶ 64. The '546 patent's Figure 4 also depicts "memory space," e.g., NAND flash memory bank 56 comprising "a plurality of MLC NAND flash memory modules 60a and a plurality of SLC NAND flash memory modules 62a" and NAND flash memory bank 58 comprising "a plurality of MLC NAND flash memory modules 60b and a plurality of SLC NAND flash memory modules 62b." Ex. 1001, 6:61–67, Fig. 4; *see* Ex. 2001 ¶ 64.

For these reasons, the '546 patent's disclosure "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *See Ariad*, 598 F.3d at 1351.

(b) <u>"Memory Element" and "At Least One . . . Memory Element"</u>

As support for the term "memory element" and the phrase "at least one . . . memory element," the '546 patent's Figures 2A–2B depict "memory elements," e.g., MLC and SLC blocks. Ex. 1001, 5:58–6:4, Figs. 2A–2B; *see* Ex. 2001 ¶ 69. The '546 patent's Figure 4 also depicts "memory elements," e.g., "a plurality of MLC NAND flash memory modules 60a," "a plurality of MLC NAND flash memory modules 60b," "a plurality of SLC NAND flash memory modules 62a," and "a plurality of SLC NAND flash memory modules 62b." Ex. 1001, 6:61–67, Fig. 4; *see* Ex. 2001 ¶ 69.

Further, the '546 patent incorporates by reference the '452 patent. Ex. 1001, 1:23–31. The '452 patent describes an "exemplary NAND

memory integrated circuit" as an "element" of a "nonvolatile memory system." Ex. 1004, 2:52–54, Fig. 2; *see* Ex. 2001 ¶ 78. Petitioner admits that the '452 patent's "exemplary NAND memory integrated circuit" corresponds to a "NAND flash memory module." Pet. 32 n.6.

For these reasons, the '546 patent's disclosure "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *See Ariad*, 598 F.3d at 1351.

(c) "Wherein the Mapping Is Performed . . . to Maximize Lifetime"

As support for the limitation "wherein the mapping is performed as necessitated by the system to maximize lifetime" in claim 1, the '546 patent explains that "mapping is performed to increase the 'reliability and lifetime' of the memory." Ex. 1001, 1:35–42; *see* Ex. 2001 ¶¶ 66, 84. Synonyms and near synonyms for "maximize" include the words "increase," "boost," and "prolong." Ex. 2017, 1; *see* Ex. 2001 ¶ 85. The '546 patent's specification uses the words "increase," "boost," and "prolong" or variations of them, e.g., "prolonging," when discussing system lifetime. *See, e.g.*, Ex. 1001, 1:35–42, 3:14–19, 5:7–10, 7:7–11; Ex. 2001 ¶ 85.

Also, as Patent Owner asserts, the '546 patent's Figures 2A–2B and 3A–3B show how "data is remapped to boost or prolong the lifetime of the system." Ex. 2001 ¶¶ 66, 85; *see* Prelim. Resp. 32. For instance, Figures 2A–2B and the related descriptions in the specification disclose remapping data for an MLC/block to an SLC/block after a failed data integrity test. Ex. 1001, 5:58–6:4, Figs. 2A–2B; *see* Ex. 2001 ¶¶ 66, 85.

Further, the '546 patent discloses various wear-leveling techniques for transferring data to less-used blocks or higher-performance blocks including (1) "select[ing] an available target block with the lowest overall erase count"

and (2) remapping from MLC NAND flash memory to SLC NAND flash memory. Ex. 1001, 3:19–26, 5:5–7, 5:54–57, 5:63–6:4, 6:44–56, code (57); *see* Ex. 2001 ¶¶ 66, 86. According to the patent, remapping from MLC NAND flash memory to SLC NAND flash may include allocating "hot" blocks (those blocks that receive frequent writes) to SLC NAND flash memory and allocating "cold" blocks (those blocks that only receive infrequent writes) to MLC NAND flash memory. Ex. 1001, 6:44–56.

The wear-leveling techniques disclosed in the '546 patent boost or prolong lifetime such that "the lifetime of the memory is maximized," e.g., by repeatedly performing one or more of them. *See* Ex. 2001 ¶¶ 66, 86; Ex. 1001, 3:19–26, 5:5–7, 5:54–57, 5:63–6:4, 6:44–56, code (57). Moreover, an ordinarily skilled artisan would understand that "the lifetime of the system is maximized by transferring data to blocks with higher endurance, whether it is a block that is less-used, or a higher-performance block," as the patent discloses. Ex. 2001 ¶ 86.

For these reasons, the '546 patent's disclosure "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *See Ariad*, 598 F.3d at 1351.

(d) <u>"Transfer of Data . . ."</u>

As support for the limitation "transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test" in claim 1, the '546 patent's Figures 3A–3B and the related descriptions in the specification disclose the claimed subject matter. Ex. 1001, 6:5–43, Figs. 3A–3B; *see* Ex. 2001 ¶ 68. More specifically, Figures 3A–3B illustrate "a method for utilizing a NAND flash memory system" that includes:

(1) writing data from DRAM to a device controller's memory (step 102);

(2) writing data from the device controller's memory to NAND flash memory (step 110);

(3) performing a data integrity test on the data newly written to NAND flash memory by (a) reading the data newly written to NAND flash memory (step 112) and (b) comparing the data just read from NAND flash memory to the data retained in the device controller's memory (step 114); and

(4) if the comparison indicates that the data sets do not match, remapping the data retained in the device controller's memory to SLC NAND flash memory (steps 116, 120, 122, and 126).

Ex. 1001, 6:5–43, Figs. 3A–3B; *see* Ex. 2001 ¶ 68.

For these reasons, the '546 patent's disclosure "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *See Ariad*, 598 F.3d at 1351.

(e) Summary

Based on the current record and for the reasons discussed above, Petitioner does not establish sufficiently for purposes of institution that the '546 patent's claims fail to satisfy § 112's written-description requirement. *See* Pet. 30–37; Ex. 1002 ¶¶ 64–73; *Ariad*, 598 F.3d at 1351; *supra* §§ III.E.4(a)–(d).

F. Alleged Failure to Satisfy § 112's Enablement Requirement: Claims 1–7

1. LEGAL PRINCIPLES

A patent's specification "must enable the full scope of the invention as defined by its claims." *Amgen Inc. v. Sanofi*, 143 S. Ct. 1243, 1254 (2023); *see* 35 U.S.C. § 112(a). "The more one claims, the more one must

enable." *Amgen*, 143 S. Ct. at 1254. The enablement requirement "enforces the essential '*quid pro quo* of the patent bargain' by requiring a patentee to teach the public how 'to practice the full scope of the claimed invention.'" *McRO, Inc. v. Bandai Namco Games Am. Inc.*, 959 F.3d 1091, 1099–100 (Fed. Cir. 2020) (quoting *AK Steel Corp. v. Sollac*, 344 F.3d 1234, 1244 (Fed. Cir. 2003)).

"To be enabling, the specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention without 'undue experimentation.'" *Genentech, Inc. v. Novo Nordisk, A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997) (quoting *In re Wright*, 999 F.2d 1557, 1561 (Fed. Cir. 1993)). Determining the need for "undue experimentation" is not "a single, simple factual determination, but rather is a conclusion reached by weighing many" factors. *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988). Those factors (the *Wands* factors) include:

> (1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims.

Id. (citing *In re Forman*, 230 USPQ 546, 547 (BPAI 1986)).

The Federal Circuit did not "interpret *Amgen* to have disturbed [its] prior enablement case law, including *Wands* and its factors." *Baxalta Inc. v. Genentech, Inc.*, 81 F.4th 1362, 1367 (Fed. Cir. 2023). The Office "continue[s] to use the *Wands* factors to ascertain whether the experimentation required to enable the full scope of the claimed invention is reasonable" because "Federal Circuit precedent applying the *Wands* factors

prior to *Amgen* is still informative." 89 Fed. Reg. 1,563, 1,565–66 (Jan. 10, 2024).

2. PETITIONER'S CONTENTIONS

Petitioner challenges the '546 patent's claims as failing to satisfy § 112's enablement requirement. *See* Pet. 21, 30–37. As explained below, Petitioner alleges deficiencies for several claim terms and limitations. *See infra* §§ III.F.2(a)–(d).

(a) "Memory Space"

Regarding the term "memory space," Petitioner contends that unless the term is limited to a "measure of memory capacity," use of the term "in the claims is unsupported in the specification, which thus fails to enable" an ordinarily skilled artisan "to practice the claimed invention." Pet. 31; *see id.* at 38.

(b) "Wherein the Mapping Is Performed . . . to Maximize Lifetime"

Regarding the limitation "wherein the mapping is performed as necessitated by the system to maximize lifetime" in claim 1, Petitioner contends that the '546 patent's specification does not explain "mapping . . . necessitated by the system to maximize lifetime" for even "the disclosed SLC-MLC NAND flash memory system, much less of memory systems of other than SLC-MLC NAND flash." Pet. 34. According to Petitioner, the "specification thus does not enable" an ordinarily skilled artisan "to practice the claimed invention limited by the 'maximize lifetime' clause." *Id.* at 34–35.

(c) "Transfer of Data . . ."

Regarding the limitation "transfer of data corresponding to the retained data to those remapped physical addresses from those physical

addresses determined to have failed the data integrity test" in claim 1, Petitioner contends that the '546 patent's specification "fails to enable" an ordinarily skilled artisan "to practice the claimed invention." Pet. 35. Further, Petitioner asserts that "the recited transfer would be pointless as propagating failed data." *Id.*

(d) "A Bank of Nonvolatile Memory"

Regarding the limitation "a bank of nonvolatile memory" with "at least one MLC nonvolatile memory element" and "at least one SLC nonvolatile memory element" in claim 1, Petitioner contends that "modules having only 'at least one . . . memory element' (and without understood NAND flash circuitry for erasing/writing blocks) would not be understood by" an ordinarily skilled artisan "as enabled by the specification." Pet. 35–36 (citing Ex. 1002 ¶ 82). Further, Petitioner asserts that a system with just a "single block" of MLC memory and a "single block" of SLC memory would be "inoperative" and not "useful." *Id.* at 36, 38–39. Petitioner also asserts that "there is nothing in the specification describing the sufficient number of blocks or 'memory elements' needed for the claimed inventions to enhance or maximize lifetime, or any way to determine a sufficient number." *Id.* at 37.

3. PATENT OWNER'S CONTENTIONS

As explained below, Patent Owner disputes that the '546 patent's claims fail to satisfy § 112's enablement requirement. *See* Prelim. Resp. 2, 27–35.

(a) "Memory Space"

Regarding the term "memory space," Patent Owner contends that Petitioner "does not clearly identify or explain the basis for its challenge"

because its "argument spans only four sentences, beginning as an apparent written description challenge but later ambiguously referencing enablement." Prelim. Resp. 28 (citing Pet. 30–31). Patent Owner contends that "neither [Patent Owner] nor the Board should be forced to guess what Petitioner is arguing." *Id.*

(b) "Wherein the Mapping Is Performed . . . to Maximize Lifetime"

Regarding the limitation "wherein the mapping is performed as necessitated by the system to maximize lifetime" in claim 1, Patent Owner contends that Petitioner's argument "is again disjointed, beginning as a written description challenge but including references to enablement, and fails to articulate a clear argument." Prelim. Resp. 31 (citing Pet. 33–35).

(c) "Transfer of Data . . ."

Regarding the limitation "transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test" in claim 1, Patent Owner contends that the '546 patent's specification "fully enables" this limitation. Prelim. Resp. 32 (citing Ex. 2001 ¶¶ 67–68). Patent Owner characterizes Petitioner's assertion about "propagating failed data" as "plainly incorrect." *Id.* at 32–33 (citing Pet. 35). Patent Owner contends that "the claimed 'transfer' does not propagate 'failed data.'" *Id.* at 33. As support, Patent Owner cites the '546 patent's disclosures that:

(1) "when data is remapped after a failed data integrity test, 'the write is repeated' from 'memory within the device controller'"; and

(2) the "memory within the device controller would not contain the failed data written to" the nonvolatile memory.

Prelim. Resp. 33 (citing Ex. 1001, 6:5–43 (describing Figs. 3A–3B); Ex. 2001 ¶ 68).

(d) "A Bank of Nonvolatile Memory"

Regarding the limitation "a bank of nonvolatile memory" with "at least one MLC nonvolatile memory element" and "at least one SLC nonvolatile memory element" in claim 1, Patent Owner contends that the '546 patent's specification enables the full scope of "at least one . . . memory element." Prelim. Resp. 33 (citing Ex. 2001 ¶¶ 69–70). As support, Patent Owner cites the '546 patent's Figures 2A–2B and 4 as showing "MLC and SLC memory elements," i.e., MLC and SLC blocks in Figures 2A–2B and MLC and SLC flash memory modules in Figure 4. *Id.* at 34. Based on those disclosures, Patent Owner asserts that an ordinarily skilled artisan "would have understood how to make and use the full scope of the claimed invention without undue experimentation." *Id.* (citing Ex. 2001 ¶ 69).

4. ANALYSIS

Based on the current record and for the reasons explained below, Petitioner does not establish sufficiently for purposes of institution that the '546 patent's claims fail to satisfy § 112's enablement requirement. *See* Pet. 30–37; Ex. 1002 ¶¶ 64, 66–68, 71, 73.

(a) Petitioner's Failure to Properly Analyze Enablement/Nonenablement

As an initial matter, we agree with Patent Owner that Petitioner "does not clearly identify or explain the basis for" its nonenablement arguments. *See* Pet. 21, 30–37; Prelim. Resp. 28, 31.

As an example, the Petition's table summarizing the unpatentability grounds includes the following text: "Ground 2: Claims 1–7 are invalid under 35 U.S.C. § 112(a) because '546 patent specification fails to provide

written description enabling, much less demonstrate the possession of any invention claimed." Pet. 21 (emphasis omitted). As another example, the Petition's section containing nonenablement and lack-of-support arguments includes the following heading: "Ground 2: The Challenged Claims Lack a Written Description Describing the Claimed Subject Matter in Accordance with 35 U.S.C. § 112(a)." *Id.* at 30.

Further, Petitioner fails to address—or even acknowledge—the *Wands* factors. *See* Pet. 30–37; Ex. 1002 ¶¶ 64, 66–68, 71, 73. Petitioner does not analyze the nature or amount of experimentation needed to make and use the full scope of the claimed invention. *See* Pet. 30–37; Ex. 1002 ¶¶ 64, 66–68, 71, 73. Hence, Petitioner does not demonstrate a need for "undue experimentation" to make and use the full scope of the claimed invention. *See* Pet. 30–37; Ex. 1002 ¶¶ 64, 66–68, 71, 73. For this reason alone, Petitioner does not establish sufficiently for purposes of institution that the '546 patent's claims fail to satisfy § 112's enablement requirement.

(b) <u>"Transfer of Data . . ."</u>

Regarding the limitation "transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test" in claim 1, Petitioner erroneously asserts that "the recited transfer would be pointless as propagating failed data." *See* Pet. 35; Prelim. Resp. 32–33; Ex. 2001 ¶ 68.

The '546 patent's Figures 3A–3B illustrate "a method for utilizing a NAND flash memory system" that transfers valid data to SLC NAND flash memory after a failed data integrity test by:

(1) writing data from DRAM to a device controller's memory (step 102);

(2) writing data from the device controller's memory to NAND flash memory (step 110);

(3) performing a data integrity test on the data newly written to NAND flash memory by (a) reading the data newly written to NAND flash memory (step 112) and (b) comparing the data just read from NAND flash memory to the data retained in the device controller's memory (step 114); and

(4) if the comparison indicates that the data sets do not match, remapping the data retained in the device controller's memory to SLC NAND flash memory (steps 116, 120, 122, and 126).

Ex. 1001, 6:5–43, Figs. 3A–3B; *see* Ex. 2001 ¶ 68. Claim 1 encompasses the method illustrated in Figures 3A–3B. *See* Ex. 1001, 6:5–43, 7:47–8:34, Figs. 3A–3B. Petitioner admits that "the 'data integrity test' elements of claim 1 . . . roughly follow the NAND flash method steps in Figs. 3A and 3B." Pet. 40 (citing Ex. 1001, 6:5–44, 8:1–21, 8:28–34).

(c) <u>"A Bank of Nonvolatile Memory"</u>

Regarding the limitation "a bank of nonvolatile memory" with "at least one MLC nonvolatile memory element" and "at least one SLC nonvolatile memory element" in claim 1, an ordinarily skilled artisan would understand that "flash memory systems are large, typically containing megabytes, gigabytes, or even terabytes of storage, and comprising thousands of blocks." Ex. 2001 ¶ 70. As for the extreme lower end of the range, i.e., a system with just a "single block" of MLC memory and a "single block" of SLC memory as Petitioner proposes, a patent's claims need not "specifically exclude" possibly inoperative embodiments. *See Atlas Powder Co. v. E.I. du Pont De Nemours & Co.*, 750 F.2d 1569, 1576 (Fed. Cir. 1984); Pet. 36. "Even if some of the claimed combinations were

inoperative, the claims are not necessarily invalid." *Atlas Powder*, 750 F.2d at 1576.

Additionally, claim 1 does not encompass a system with just a "single block" of MLC memory and a "single block" of SLC memory as Petitioner proposes. *See* Ex. 1001, 7:28–8:34; Pet. 36. Instead, claim 1 requires "a bank of nonvolatile memory, including: a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and at least one SLC memory module including at least one SLC nonvolatile memory element." Ex. 1001, 7:37–41. The claimed "plurality of MLC memory modules" includes a plurality of MLC nonvolatile memory elements, e.g., a plurality of blocks. *Id.*

(d) Summary

Based on the current record and for the reasons discussed above, Petitioner does not establish sufficiently for purposes of institution that the '546 patent's claims fail to satisfy § 112's enablement requirement. *See* Pet. 30–37; Ex. 1002 ¶¶ 64, 66–68, 71, 73; *Genentech*, 108 F.3d at 1365; *Atlas Powder*, 750 F.2d at 1576; *supra* §§ III.F.4(a)–(c).

G. Alleged Failure to Satisfy § 112's Definiteness Requirement: Claims 1–7

1. LEGAL PRINCIPLES

(a) § 112's Definiteness Requirement

A patent's specification must "conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention." 35 U.S.C. § 112(b). In particular, "a patent's claims, viewed in light of the specification and prosecution history, [must] inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instr., Inc.*,

572 U.S. 898, 910 (2014). The definiteness requirement "strikes a 'delicate balance' between 'the inherent limitations of language' and providing 'clear notice of what is claimed.'" *Sonix Tech. Co. v. Publ'ns Int'l, Ltd.*, 844 F.3d 1370, 1377 (Fed. Cir. 2017) (quoting *Nautilus*, 572 U.S. at 909).

(b) Means-Plus-Function Claiming

The patent statute provides that "[a]n element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." 35 U.S.C. § 112 ¶ 6. The absence of the word "means" in a claim limitation creates a rebuttable presumption that § 112's means-plus-function provision does not apply. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015) (en banc in relevant part).

When a claim limitation lacks the word "means," a party may rebut the presumption that § 112's means-plus-function provision does not apply by demonstrating that "the claim term fails to 'recite[] sufficiently definite structure' or else recites 'function without reciting sufficient structure for performing that function.'" *Williamson*, 792 F.3d at 1348 (alteration by the court) (quoting *Watts v. XL Sys., Inc.*, 232 F.3d 877, 880 (Fed. Cir. 2000)). But § 112's means-plus-function provision does not apply if a claim limitation contains a term or phrase "used in common parlance or by persons of skill in the pertinent art to designate structure." *Lighting World, Inc. v. Birchwood Lighting, Inc.*, 382 F.3d 1354, 1359 (Fed. Cir. 2004). For instance, "many devices take their names from the functions they perform,"

such as "'filter,' 'brake,' 'clamp,' 'screwdriver,' or 'lock.'" *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1583 (Fed. Cir. 1996).

When a limitation recites two or more functions, the specification "must disclose adequate corresponding structure to perform *all* of the claimed functions." *Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1374 (Fed. Cir. 2015) (emphasis by the court); *see Noah Sys., Inc. v. Intuit Inc.*, 675 F.3d 1302, 1318–19 (Fed. Cir. 2012) (considering means-plus-function limitation specifying two functions).

For a computer-implemented function, the "corresponding structure" for a means-plus-function limitation "may differ from more traditional, mechanical structure." *Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1298 (Fed. Cir. 2014), overruled on other grounds by *Williamson*, 792 F.3d at 1349. In particular, "there must be some explanation of how the computer performs the claimed function." *Blackboard, Inc. v. Desire2Learn, Inc.*, 574 F.3d 1371, 1384 (Fed. Cir. 2009). Hence, a patent's specification must disclose more than a general-purpose computer or microprocessor because those devices "can be programmed to perform very different tasks in very different ways," and merely disclosing one of those devices as structure for performing a claimed function does not limit claim scope. *Aristocrat Techs. Austl. Pty Ltd. v. Int'l Game Tech.*, 521 F.3d 1328, 1333 (Fed. Cir. 2008).

For a computer-implemented function, an algorithm "for performing the claimed function" supplies the necessary disclosure. *Williamson*, 792 F.3d at 1352. "Requiring disclosure of an algorithm properly defines the scope of the claim and prevents pure functional claiming." *Ergo Licensing, LLC v. CareFusion 303, Inc.*, 673 F.3d 1361, 1364 (Fed. Cir. 2012). A patent's specification may disclose an algorithm "for

performing the claimed function" as "a mathematical formula, in prose, as a flow chart, or in any other manner that provides sufficient structure." *Williamson*, 792 F.3d at 1352; *see Function Media, L.L.C. v. Google, Inc.*, 708 F.3d 1310, 1318 (Fed. Cir. 2013).

(c) Failure to Adequately Disclose Corresponding Structure

When a patent's specification lacks an adequate disclosure of structure corresponding to the function or functions recited in a means-plus-function limitation, there is a failure "to particularly point out and distinctly claim the invention" as required by the patent statute. *In re Donaldson Co.*, 16 F.3d 1189, 1195 (Fed. Cir. 1994) (en banc). Without an adequate disclosure of corresponding structure for a means-plus-function limitation, for instance, those skilled in the art could not ascertain the limitation's "equivalents" according to the patent statute. *See* 35 U.S.C. § 112 ¶ 6. Hence, a failure to adequately disclose corresponding structure equates to a failure to satisfy the definiteness requirement and renders a claim unpatentable. *See, e.g.*, *Aristocrat Techs.*, 521 F.3d at 1337–38.

2. PETITIONER'S CONTENTIONS

Petitioner challenges the '546 patent's claims as failing to satisfy § 112's definiteness requirement. *See* Pet. 22, 37–45. As explained below, Petitioner alleges indefiniteness for several claim terms and limitations. *See infra* §§ III.G.2(a)–(f).

(a) "Memory Space"

Petitioner contends that the term "memory space" is "indefinite as to whether it refers to 'logical' memory locations in a NAND flash [logical-to-physical] table or to something physical, such as the physical capacity

available for NAND flash reading, writing and erasing for those logical memory locations." Pet. 38.

(b) "Memory Element"

Petitioner contends that the term "memory element" is "so open-ended that it could be any of claim 1's mapping is [sic] of 'blocks, pages, or bytes of data', or even a cell." Pet. 38 (citation omitted) (quoting Ex. 1001, 8:26). According to Petitioner, there is also uncertainty whether a "memory element" is either:

(1) an "SLC NAND module" as shown in Figure 2 of the incorporated '452 patent and similarly an "SLC memory module" as recited in claim 1; or

(2) "something more inclusive," such as the "NAND flash memory module 50" shown in the '546 patent's Figure 4.

Id. at 39 (citing Ex. 1001, 6:57–59, 7:40; Ex. 1004, 2:52–53).

Further, Petitioner asserts that if "the system is not limited to an SLC-MLC NAND flash system" with "structure including NAND [logical-to-physical] mapping, block erase, multiple level page write-pulsing, the uncertainty is increased." Pet. 39.

(c) "Wherein the Mapping Is Performed . . . to Maximize Lifetime"

Regarding the limitation "wherein the mapping is performed as necessitated by the system to maximize lifetime" in claim 1, Petitioner asserts that "there are multiple axes of uncertainty" because:

(1) "every mapping" in "the life of a NAND flash system, if followed ordinarily by writing, decreases expected useful lifetime";

(2) claim 1 "fails to specify any user-elected strategy/ configuration of NAND flash mapping to distribute wear (stress)";

(3) the ’546 patent contains no claim covering the “hot” blocks versus “cold” blocks wear-leveling technique; and

(4) “the elements confuse what is transferred after remapping” and “themselves are indefinite as when the test and remapping are performed.”

Pet. 39–40.

(d) “Controller”

Petitioner contends that § 112’s means-plus-function provision applies to the term “controller” because that term is a nonce word. Pet. 41. Petitioner also contends that the ’546 patent’s specification “does not adequately disclose structure” corresponding to the “controller” functions recited in claim 1. *Id.* According to Petitioner, the following “controller” functions recited in claim 1 lack adequate structural support in the specification:

(1) “operate memory elements and associated memory space”;

(2) “control[] access” of memory elements “for storage of the received data therein”;

(3) “operable” to store data in (i) the MLC nonvolatile memory element and (ii) the random access volatile memory element;

(4) “maintain an address table” that “maps logical and physical addresses adaptable to the system”; and

(5) “mapping is performed as necessitated by the system to maximize lifetime.”

Id. at 41–43 (alteration by Petitioner) (citing Ex. 1001, 7:33–34, 7:44–46, 7:48–51, 8:5–8, 8:21–25).

Further, Petitioner asserts that "the identity and location of 'the controller' memory are themselves indefinite." Pet. 42 (citing Ex. 1002 ¶ 86).

(e) Alleged Method Steps Within System Claims

Petitioner contends that the '546 patent's claims cover "a method of operation of a system" and are unpatentable "for impermissibly mixing product and process claims across different § 101 classifications." Pet. 43 (citing *IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005); Manual of Patent Examining Procedure (MPEP) § 2173.05(p)(II)). Petitioner identifies claim 1's language "the controller performing a data integrity test" as "a method step within the system claim" that renders "the claims invalid under *IPXL* and MPEP § 2173.05(p)(II)." *Id.* at 44 (emphasis omitted). According to Petitioner, there are "multiple options" for performing a data integrity test, and "it may be the user's choice if and when some of the recited controller functions are performed." *Id.*

(f) Alleged Uncertainty About when to Perform a Data Integrity Test

Petitioner contends that the '546 patent's claims are indefinite because the limitation "the controller performing a data integrity test . . . after the at least a Write access operation" in claim 1 "does not specify when the test is performed other than after some 'Write access' – and not necessarily after every 'Write access.'" Pet. 44–45 (emphasis omitted). Petitioner notes that the patent's specification states that the "controller conducts a data integrity test after every write" but also indicates that the test occurs "if time permits." *Id.* at 45 (emphasis omitted) (quoting Ex. 1001, 5:4–5, 5:52–53 (but misquoting 5:52–53)). According to Petitioner, "claim 1 is silent on the issue" and indefinite due to this uncertainty. *Id.*

3. PATENT OWNER'S CONTENTIONS

As explained below, Patent Owner disputes that the '546 patent's claims fail to satisfy § 112's definiteness requirement. *See* Prelim. Resp. 2, 35–49.

(a) "Memory Space"

Patent Owner asserts that an ordinarily skilled artisan would understand the term "memory space" as describing where data is stored. Prelim. Resp. 36–37 (citing Ex. 2001 ¶ 72); *see id.* at 29. Patent Owner asserts that claim 1's language "requires that memory space be 'associated' with physical memory elements and that non-volatile memory space 'includes both multi-level cell (MLC) space and single level cell (SLC) space.'" *Id.* at 35–36 (citing Ex. 1001, 7:29–32). Patent Owner also asserts that "the surrounding claim language specifies that data may be stored in memory elements, and these memory elements may be mapped into the memory space." *Id.* at 36 (citing Ex. 1001, 7:33–36).

Additionally, Patent Owner quotes the '546 patent's disclosure that the "total non-volatile memory storage space=MLC+SLC." Prelim. Resp. 36 (quoting Ex. 1001, 5:12). Patent Owner asserts that an ordinarily skilled artisan would understand that disclosure to mean that "the 'memory space' refers to where data is stored, and 'memory storage space' refers to the sum of the memories that make up a given memory." *Id.* (citing Ex. 2001 ¶ 74).

Further, Patent Owner asserts that "memory space" is "commonly used" to refer to where data is stored. Prelim. Resp. 37. As support, Patent Owner cites a patent application published in 2007 and assigned to Petitioner that uses "memory space" to refer to "the 'addressable locations' where data

is stored." *Id.* (citing Ex. 2007 ¶ 7). As additional support, Patent Owner cites a 2010 textbook titled "Inside NAND Flash Memories" and the Declaration of Dr. David Liu from IPR2021-01550 challenging claims in the '300 patent, i.e., the '546 patent's parent. *Id.* (citing Ex. 2003, 485, 493;[10] Ex. 2011 (Ex. 1009 in IPR2021-01550) ¶ 63). For instance, Patent Owner quotes Dr. Liu's testimony that "a set of addresses is known as an 'address space' or 'memory space.'" *Id.* (quoting Ex. 2011 ¶ 63).

(b) "Memory Element"

Patent Owner asserts that an ordinarily skilled artisan would understand the term "memory element" as describing an element of memory. Prelim. Resp. 37 (citing Ex. 2001 ¶¶ 76–81); *see id.* at 31 (citing Ex. 2001 ¶ 65). Patent Owner also asserts that "memory element" is "a well understood term in the art." *Id.* at 37.

As support, Patent Owner notes that the '546 patent incorporates by reference the '452 patent. Prelim. Resp. 37 (citing Ex. 1001, 1:24–31). Then, Patent Owner quotes the '452 patent's disclosure that "an exemplary NAND memory integrated circuit [is] one element of the . . . nonvolatile memory system." *Id.* (second alteration by Patent Owner) (quoting Ex. 1004, 2:52–54).

As further support, Patent Owner quotes (1) Dr. Liu's testimony that "'flash memory elements' were 'well known to any [person of ordinary skill]' by 2010" and (2) the Oxford Dictionary of Computing definition of

[10] For Exhibit 2003 (textbook titled "Inside NAND Flash Memories"), we cite to the page numbers that appear in the publication instead of the page numbers that Patent Owner applied to the exhibit.

"memory element" as a "device that stores one item of information." Prelim. Resp. 37–38 (quoting Ex. 2011 ¶ 59; Ex. 2013, 312).[11]

Additionally, Patent Owner contends that one of Petitioner's customers has a patent that "similarly uses 'memory element' to broadly refer to an element where data is stored." Prelim. Resp. 38 (citing Ex. 2014 ¶¶ 9, 17–20).

Patent Owner asserts that the evidence discussed above confirms that the term "memory element" has a "broad but understood" meaning to an ordinarily skilled artisan. Prelim. Resp. 38.

(c) "Wherein the Mapping Is Performed . . . to Maximize Lifetime"

Regarding the limitation "wherein the mapping is performed as necessitated by the system to maximize lifetime" in claim 1, Patent Owner explains that the "point of the ['546 patent] is to increase the 'reliability and lifetime' of the memory, and the specification is replete with examples of how to do this." Prelim. Resp. 39 (citing Ex. 1001, 1:35–42). Patent Owner asserts that an ordinarily skilled artisan "reading the specification would understand that [the disputed limitation] refers to transferring data from MLC to SLC, or from heavily used MLC to less used MLC, in order to prolong or otherwise boost the lifetime of the memory." *Id.* (citing Ex. 2001 ¶ 84). As support, Patent Owner cites the '546 patent's Figures 2A–2B and 3A–3B as showing how "data is remapped to boost or prolong the lifetime of the system." *Id.* at 39.

[11] For Exhibit 2013 (Oxford Dictionary of Computing), we cite to the page numbers that appear in the publication instead of the page numbers that Patent Owner applied to the exhibit.

As further support, Patent Owner identifies the '546 patent's disclosures that:

(1) if "there is failure of a data integrity test, the data is transferred to a block with higher endurance"; and

(2) if "a block is heavily used, the data is mapped to a block that is less-used, or a higher-performance block."

Prelim. Resp. 39–40 (citing Ex. 1001, 3:19–26, 5:54–57, 6:50–56). Patent Owner contends that "[i]n each case, the lifetime of the memory is maximized." *Id.* at 40.

Patent Owner also contends that when Dr. Liu considered the disputed limitation as it also appears in the '300 patent's claim 1, Dr. Liu "had no problem determining its claim scope and opined that it relates to rewriting data to more robust SLC cells to boost lifetime." Prelim. Resp. 40 (citing Ex. 2011 ¶¶ 85, 183–186).

Further, responding to Petitioner's assertion that claim 1 "fails to specify any user-elected strategy/configuration of NAND flash mapping to distribute wear (stress)," Patent Owner contends that "Petitioner mistakes breadth for indefiniteness." Prelim. Resp. 40–41. According to Patent Owner, claim 1 "does not need to be limited to a specific type of mapping to be patentable." *Id.* at 41.

(d) <u>"Controller"</u>

Patent Owner contends that claim 1 does not contain the word "means" and that Petitioner fails to rebut the resulting presumption that § 112's means-plus-function provision does not apply to the term "controller." Prelim. Resp. 41 (citing Ex. 2001 ¶¶ 88–98). Further, Patent Owner asserts that the "Federal Circuit and numerous other courts have consistently held that 'controller' is not a nonce term, and it has a

sufficiently definite structure." *Id.* at 41–42. Patent Owner asserts that Petitioner "provides no support for its argument that 'controller' is a nonce term." *Id.* at 44.

Patent Owner asserts that an "overwhelming wealth of technical dictionaries and well-known textbooks" establish that the term "controller" refers to a known class of structures. Prelim. Resp. 43–44. As an example, Patent Owner quotes the Microsoft Computer Dictionary definition of "controller" as "a device that other devices rely on for access to a computer subsystem." *Id.* at 43 (quoting Ex. 2015, 128).[12]

Patent Owner asserts that the '546 patent's specification "confirms that the claimed 'controller' is an electronic device with a known structure." Prelim. Resp. 42. As support, Patent Owner quotes the following statements in the specification's "Background" section:

(1) "[s]ometimes, a plurality of files has to be combined and/or modified, which poses an enormous challenge for the memory controller device of a non-volatile memory system";

(2) "the vast majority of NAND flash in enterprise servers utilizes a SLC architecture, which further comprises a NAND flash controller and a flash translation layer (FTL)";

(3) "wear leveling algorithms are used with the flash devices (as firmware commonly known as FTL or managed by a controller)";

(4) "the controller maintains a lookup table";

[12] For Exhibit 2015 (Microsoft Computer Dictionary), we cite to the page numbers that appear in the publication instead of the page numbers that Patent Owner applied to the exhibit.

(5) "the controller's wear-leveling algorithm determines which physical block to use each time data is programmed"; and

(6) "[d]epending on the wear-leveling method used, the controller typically either writes to . . . ."

Id. at 42–43 (emphases omitted) (quoting Ex. 1001, 2:36–43, 3:5–7, 3:11–12, 3:14–15, 3:19–20).

Additionally, Patent Owner contends that an ordinarily skilled artisan would understand the claimed "controller" to be "a component that uses firmware to 'control' or 'manage' the data flow to and from the memory." Prelim. Resp. 43 (citing Ex. 2001 ¶ 93; Ex. 2003, 39–43). Patent Owner also contends that an ordinarily skilled artisan would know that "firmware implemented by the controller may manage tasks such as wear leveling, garbage collection, and bad block management." *Id.* (citing Ex. 1001, 3:6–7; Ex. 2003, 40).

Further, Patent Owner asserts that even if § 112's means-plus-function provision applied to the term "controller," the '546 patent's specification adequately discloses structure corresponding to the "controller" functions recited in claim 1. Prelim. Resp. 44. Patent Owner identifies Figures 2A–2B and 3A–3B and the related descriptions in the specification as disclosing "algorithms for the claimed functionality." *Id.* at 45 (citing Ex. 2001 ¶¶ 97–98). According to Patent Owner, Figures 2A–2B "describe the data integrity test, including mapping and remapping addresses," and Figures 3A–3B "provide a 'flow chart illustrating' the invention." *Id.* (quoting Ex. 1001, 4:55, 6:5).

(e) Alleged Method Steps Within System Claims

Patent Owner contends that the ’546 patent’s claims “do not improperly mix apparatus elements and method steps, contrary to Petitioner’s contention.” Prelim. Resp. 45 (citing Pet. 43–44). Patent Owner contends that “the functional language in the claims describes how the controller is configured to operate.” *Id.* at 46 (emphasis omitted).

Patent Owner distinguishes the ’546 patent’s claims from the claim in *IPXL* that failed to satisfy § 112’s definiteness requirement by explaining that the ’546 patent’s claims do not require any user action and “never refer to ‘the user.’” Prelim. Resp. 46–47 (citing *IPXL*, 430 F.3d at 1384; Ex. 2001 ¶ 100).

Regarding claim 1’s language “the controller performing a data integrity test” and Petitioner’s argument about “user choice” determining actual test performance, Patent Owner contends that claim 1 does not require any user action. Prelim. Resp. 47. Patent Owner explains that claim 1 recites “the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation,” and thus specifies that “the controller is ‘capable’ of responding to a Write access operation.” *Id.* According to Patent Owner, it is permissible to “claim the system’s capability,” e.g., the system’s capability “to receive and respond to user selection.” *Id.* (quoting *MasterMine Software, Inc. v. Microsoft Corp.*, 874 F.3d 1307, 1316 (Fed. Cir. 2017)).

(f) Alleged Uncertainty About when to Perform a Data Integrity Test

Patent Owner contends that there is “nothing ambiguous” about the limitation “the controller performing a data integrity test . . . after the at least

a Write access operation" in claim 1. Prelim. Resp. 47. Patent Owner notes that the '546 patent's specification explains that a data integrity test may be performed "after every write" or alternatively only "as time permits." *Id.* at 48 (citing Ex. 1001, 4:20–22, 5:4–5, 5:51–54). Therefore, according to Patent Owner, an ordinarily skilled artisan would understand that claim 1 encompasses "data integrity tests performed after every Write access operation" or only "after some Write access operations." *Id.* (citing Ex. 2001 ¶ 102).

Patent Owner contends that Petitioner's arguments concerning uncertainty confuse "breadth with indefiniteness." Prelim. Resp. 48.

4. ANALYSIS

Based on the current record and for the reasons explained below, Petitioner does not establish sufficiently for purposes of institution that the '546 patent's claims fail to satisfy § 112's definiteness requirement. *See* Pet. 37–45; Ex. 1002 ¶¶ 76–91.

(a) "Memory Space"

Based on the current record, including the intrinsic evidence and the extrinsic evidence, we agree with Patent Owner that an ordinarily skilled artisan would understand "memory space" as describing where data is stored. *See* Prelim. Resp. 29, 36–37; Ex. 2001 ¶¶ 72–75. Dr. Khatri testifies that data may be "stored in a volatile memory space." Ex. 2001 ¶ 72. Consistent with that testimony, claim 1 recites "volatile memory space." Ex. 1001, 7:29; *see* Ex. 2001 ¶ 73. Dr. Khatri also testifies that data may be "stored in a non-volatile memory space." Ex. 2001 ¶ 72. Consistent with that testimony, claim 1 recites "nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and

single level cell (SLC) space." Ex. 1001, 7:30–32; *see* Ex. 2001 ¶ 73. Further, as Patent Owner asserts, "the surrounding claim language specifies that data may be stored in memory elements, and these memory elements may be mapped into the memory space." *See* Ex. 1001, 7:33–36; Prelim. Resp. 36.

Additionally, the '546 patent discloses that the "total non-volatile memory storage space=MLC+SLC." Ex. 1001, 5:12. An ordinarily skilled artisan would understand that disclosure to mean that "the 'memory storage space' refers to the total amount of space where data can be stored in a given memory, and the 'memory space' refers to where data is stored." Ex. 2001 ¶ 74.

Also, as Patent Owner points out, a patent application published in 2007 and assigned to Petitioner uses "memory space" to refer to "the 'addressable locations' where data is stored." Ex. 2007 ¶ 7; *see* Prelim. Resp. 37. As Patent Owner also points out, a 2010 textbook titled "Inside NAND Flash Memories" and the Declaration of Dr. David Liu from IPR2021-01550 indicate that "memory space" refers to where data is stored. Ex. 2003, 485, 493; Ex. 2011 ¶ 63; *see* Prelim. Resp. 37.

As for Petitioner's contention concerning ambiguity because "memory space" may refer to something "logical" or something "physical," even if the challenged claims encompassed "logical" memory as well as "physical" memory, claim "breadth is not indefiniteness." *See BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1367 (Fed. Cir. 2017); Pet. 38.

(b) <u>"Memory Element"</u>

Based on the current record and for the reasons stated by Patent Owner and supported by both the intrinsic evidence and the extrinsic

evidence, including Dr. Khatri's testimony, we agree with Patent Owner that the term "memory element" has a "broad but understood" meaning to an ordinarily skilled artisan. *See* Ex. 1004, 2:52–54; Ex. 2001 ¶¶ 76–81; Ex. 2011 ¶ 59; Ex. 2013, 312; Ex. 2014 ¶¶ 9, 17–20; Prelim. Resp. 37–38.

As for Petitioner's contention concerning ambiguity because "memory element" may refer to bytes, pages, blocks, modules, or "something more inclusive," claim "breadth is not indefiniteness." *See BASF*, 875 F.3d at 1367; Pet. 39.

(c) "Wherein the Mapping Is Performed . . . to Maximize Lifetime"

Based on the current record, the limitation "wherein the mapping is performed as necessitated by the system to maximize lifetime" in claim 1, viewed in light of the specification, informs those skilled in the art about the scope of the invention with reasonable certainty. *See* Ex. 1001, 1:35–42, 3:19–26, 5:54–6:56, 7:28–8:34, Figs. 2A–2B, 3A–3B; Ex. 2001 ¶¶ 82–87; Ex. 2011 ¶¶ 85, 183–186. As Patent Owner asserts, the '546 patent's Figures 2A–2B and 3A–3B show how "data is remapped to boost or prolong the lifetime of the system." Ex. 2001 ¶¶ 66, 85; *see* Prelim. Resp. 39.

For instance, Figures 2A–2B and the related descriptions in the specification disclose remapping data for an MLC/block to an SLC/block after a failed data integrity test. Ex. 1001, 5:58–6:4, Figs. 2A–2B; *see* Ex. 2001 ¶¶ 66, 85. Moreover, Figures 3A–3B illustrate "a method for utilizing a NAND flash memory system" that transfers valid data to SLC NAND flash memory after a failed data integrity test. Ex. 1001, 6:5–43, Figs. 3A–3B; *see* Ex. 2001 ¶ 68.

Further, the '546 patent discloses various wear-leveling techniques for transferring data to less-used blocks or higher-performance blocks including

(1) "select[ing] an available target block with the lowest overall erase count" and (2) remapping from MLC NAND flash memory to SLC NAND flash memory. Ex. 1001, 3:19–26, 5:5–7, 5:54–57, 5:63–6:4, 6:44–56, code (57); *see* Ex. 2001 ¶¶ 66, 86. According to the patent, remapping from MLC NAND flash memory to SLC NAND flash may include allocating "hot" blocks (those blocks that receive frequent writes) to SLC NAND flash memory and allocating "cold" blocks (those blocks that only receive infrequent writes) to MLC NAND flash memory. Ex. 1001, 6:44–56.

The wear-leveling techniques disclosed in the '546 patent boost or prolong lifetime such that "the lifetime of the memory is maximized," e.g., by repeatedly performing one or more of them. *See* Ex. 2001 ¶¶ 66, 86; Ex. 1001, 3:19–26, 5:5–7, 5:54–57, 5:63–6:4, 6:44–56, code (57). Moreover, an ordinarily skilled artisan would understand that "the lifetime of the system is maximized by transferring data to blocks with higher endurance, whether it is a block that is less-used, or a higher-performance block," as the patent discloses. Ex. 2001 ¶ 86.

(d) <u>"Controller"</u>

Based on the current record and for the reasons stated by Patent Owner and supported by both the intrinsic evidence and the extrinsic evidence, including Dr. Khatri's testimony, we agree with Patent Owner that the term "controller" in the '546 patent refers to a known class of structures. *See* Ex. 1001, 2:36–43, 3:4–26; Ex. 1004, 2:55–56, Fig. 3; Ex. 1045, 2:56–58; Ex. 2001 ¶¶ 88–96; Ex. 2003, 39–43; Ex. 2015, 128; Prelim. Resp. 41–44.

For example, the ’546 patent incorporates by reference the ’452 patent, and the ’452 patent depicts an illustrative controller in Figure 3 as reproduced below:

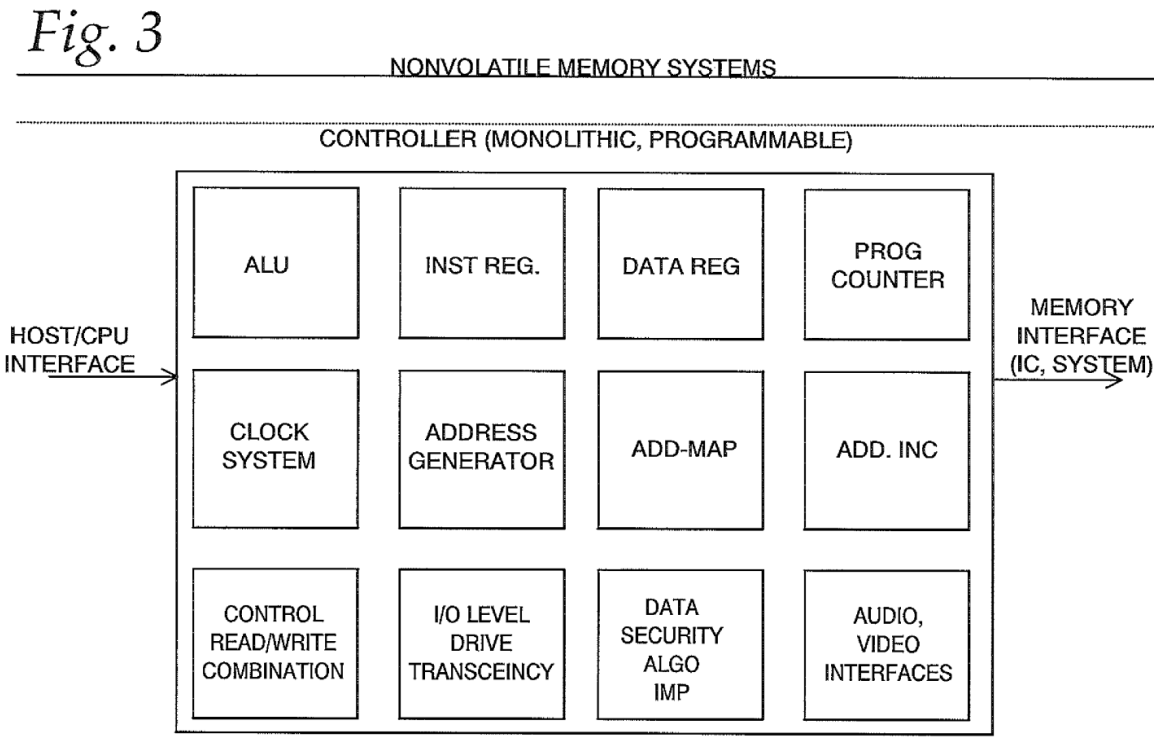

Figure 3 “shows various components of a controller for [a] nonvolatile memory system (NVMS),” including, among other things, an arithmetic logic unit (ALU), a clock system, and an address generator. Ex. 1004, 2:55–56, Fig. 3.

As another example, Gavens explains that “more sophisticated memory devices also come with a controller that performs intelligent and higher level memory operations and interfacing.” Ex. 1045, 2:56–58.

Because the term “controller” in the ’546 patent refers to a known class of structures, (1) Petitioner fails to rebut the presumption that § 112’s means-plus-function provision does not apply to that term and (2) Petitioner’s indefiniteness arguments based on § 112’s means-plus-function provision lack merit. *See* Pet. 40–43.

As for Petitioner's assertion that "the identity and location of 'the controller' memory are themselves indefinite," the absence of those recitations in claim 1 does not result in indefiniteness, e.g., because claim "breadth is not indefiniteness." *See BASF*, 875 F.3d at 1367; Pet. 42. Also, Figure 1 illustrates computer system 10 including device controller 14 coupled to processor 12 and also coupled to dynamic random-access memory (DRAM) 20, one or more disks 24, MLC NAND flash memory module 26, and SLC NAND flash memory module 28. Ex. 1001, 5:13–32, Fig. 1. Additionally, in contrast to claim 1, dependent claim 3 specifies that "at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller." *Id.* at 8:37–40.

(e) Alleged Method Steps Within System Claims

Based on the current record, we agree with Patent Owner that the '546 patent's claims "do not improperly mix apparatus elements and method steps." *See* Ex. 2001 ¶¶ 99–101; Prelim. Resp. 45–47. Rather, the claims recite system capabilities, e.g., the controller's capability to perform a data integrity test, and "do not claim activities performed by the user." *See* Ex. 1001, 7:28–8:50; *MasterMine Software, Inc. v. Microsoft Corp.*, 874 F.3d 1307, 1316 (Fed. Cir. 2017).

The Federal Circuit's decision in *IPXL* does not undermine this determination because the '546 patent's claims differ materially from the claim in *IPXL* that failed to satisfy § 112's definiteness requirement. *See IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377, 1379, 1383–84 (Fed. Cir. 2005). In *IPXL*, claim 2 recited an "electronic financial transaction system" including "an input means." *Id.* at 1379, 1384.

Claim 25 depended from claim 2 and recited that "the user uses the input means" to either change the predicted transaction information or accept the displayed transaction. *Id.* at 1384. The Federal Circuit decided that claim 25 failed to satisfy § 112's definiteness requirement because it was unclear (1) "whether infringement of claim 25 occurs when one creates a system that allows the user to change the predicted transaction information or accept the displayed transaction" or (2) "whether infringement occurs when the user actually uses the input means to change transaction information or uses the input means to accept a displayed transaction." *Id.*

In contrast to claim 25 in *IPXL*, the '546 patent's claims do not require any user action. *See* Ex. 1001, 7:28–8:50.

(f) Alleged Uncertainty About when to Perform a Data Integrity Test

Based on the current record and for the reasons stated by Patent Owner and supported by both the intrinsic evidence and the extrinsic evidence, including Dr. Khatri's testimony, we agree with Patent Owner that an ordinarily skilled artisan would understand that claim 1 encompasses "data integrity tests performed after every Write access operation" or only "after some Write access operations." *See* Ex. 1001, 4:20–22, 5:4–5, 5:51–54, 7:28–8:34; Ex. 2001 ¶ 102; Prelim. Resp. 47–48. As Patent Owner contends, Petitioner's arguments concerning uncertainty confuse "breadth with indefiniteness." *See* Pet. 44–45; Prelim. Resp. 48; *BASF*, 875 F.3d at 1367.

(g) Summary

Based on the current record and for the reasons discussed above, Petitioner does not establish sufficiently for purposes of institution that the

'546 patent's claims fail to satisfy § 112's definiteness requirement. *See* Pet. 37–45; Ex. 1002 ¶¶ 76–91; *BASF*, 875 F.3d at 1367; *supra* §§ III.G.4(a)–(f).

H. Alleged Obviousness over Gavens: Claims 1–7

Petitioner contends that claims 1–7 are unpatentable under § 103 because the claims would have been obvious over Gavens in view of an ordinarily skilled artisan's knowledge.[13] *See* Pet. 22, 45–76. Patent Owner disputes Petitioner's contentions. *See* Prelim. Resp. 2, 49–86.

Below, we provide an overview of Gavens. Then, we consider the obviousness issues. For the reasons explained below, Petitioner does not establish sufficiently for purposes of institution that claims 1–7 are unpatentable under § 103 because the claims would have been obvious over Gavens in view of an ordinarily skilled artisan's knowledge.

1. LEGAL PRINCIPLES

A patent may not be obtained "if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains." 35 U.S.C. § 103. An obviousness analysis involves underlying factual inquiries including (1) the scope and content of the prior art; (2) differences between the claimed invention and the prior art; (3) the level of ordinary skill in the art; and (4) where in evidence, objective indicia of nonobviousness, such as commercial success, long-felt but unsolved

[13] Gavens states that it incorporates by reference the entire disclosure in each of Chen, Gorobets, Lee, and Paley. Ex. 1045, 8:40–43, 16:38–40, 17:65–67, 20:53–59.

needs, and failure of others.[14] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18, 35–36 (1966); *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1047–48 (Fed. Cir. 2016) (en banc).

When evaluating a proposed combination, an obviousness analysis should address "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Whether a proposed combination rests on "combining disclosures from multiple references, combining multiple embodiments from a single reference, or selecting from large lists of elements in a single reference, there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful." *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017).

We analyze the obviousness issues according to these principles.

2. OVERVIEW OF GAVENS (EXHIBIT 1045)

Gavens is a U.S. patent titled "Non-Volatile Memory and Method with Accelerated Post-Write Read to Manage Errors," filed on September 1, 2010, and issued on January 21, 2014. Ex. 1045, codes (12), (22), (45), (54). Gavens states that it incorporates by reference numerous patent applications and patents, including Chen, Gorobets, Lee, and Paley. *See, e.g.*, *id.* at 8:40–43, 14:37–40, 16:38–40, 17:4–6, 17:65–67, 20:53–59.

Gavens states that the disclosure "relates to the operation of re-programmable non-volatile memory systems such as semiconductor flash memory, and, more specifically, to handling and efficient managing of errors in memory operations." Ex. 1045, 1:16–20. Gavens explains that "the

[14] The parties do not provide evidence or argument regarding objective indicia of nonobviousness. *See, e.g.*, Pet. 45–76; Prelim. Resp. 49–86.

integrity of the data being stored is maintained by use of an error correction technique." *Id.* at 3:28–30. "Most commonly, an error correction code (ECC) is calculated for each sector or other unit of data that is being stored at one time, and that ECC is stored along with the data." *Id.* at 3:30–33. Typically, an ECC relates to "a unit group of user data," such as "a sector or a multi-sector page." *Id.* at 3:33–36. "When this data is read from the memory, the ECC is used to determine the integrity of the user data being read." *Id.* at 3:36–38.

Gavens also explains that as "the flash memory ages, its error rate increases rapidly" near the memory's end of life. Ex. 1045, 3:56–57. Using an "ECC to correct a worst-case number of error bits" near the memory's end of life "consume[s] a great amount processing time," and the memory's performance will degrade. *Id.* at 3:60–63.

Gavens identifies "a need to provide a nonvolatile memory of high storage capacity without the need for a resource-intensive ECC over designed for the worse-case." Ex. 1045, 4:3–5. To address that need, Gavens discloses adaptively rewriting data from a higher-density memory portion to a lower-error-rate memory portion to control error rate. *See, e.g.*, *id.* at 4:9–5:30, 16:14–19:24, code (57), Figs. 14A–14B, 15, 16A–16C, 17.

For example, "a flash memory having an array of memory cells is configured with a first portion and a second portion." Ex. 1045, 4:14–16, code (57). The "first portion operat[es] with less error but of lower density storage." *Id.* at code (57). The "second portion operat[es] with a higher density but less robust storage." *Id.* Initially, the data "is written to the second portion for efficient storage." *Id.* at 4:18–19. Then, the data "is read back in a post-write read operation to check for excessive error bits." *Id.*

at 4:19–21. "If the error bits exceeded a predetermined amount, the data is rewritten or kept at the less error-prone first portion." *Id.* at 4:21–22. This arrangement "allows a smaller and more efficient error correction code ('ECC') to be designed for correcting a smaller number of errors bits, thereby improving the performance and reducing the cost of the memory." *Id.* at 4:28–31.

In a preferred embodiment, the "first portion has each memory cell storing one bit of data," and the "second portion has each memory cell storing more than one bit of data." Ex. 1045, 4:32–34. For instance, the "less error-prone [first] portion has each memory cell storing 1 bit of data," and the "high density storage [second] portion of the memory has each memory cell storing 3 bits of data." *Id.* at 5:15–17; *see id.* at 16:22–24.

Gavens's Figure 14B (reproduced below) depicts an array of memory cells configured with a first portion and a second portion:

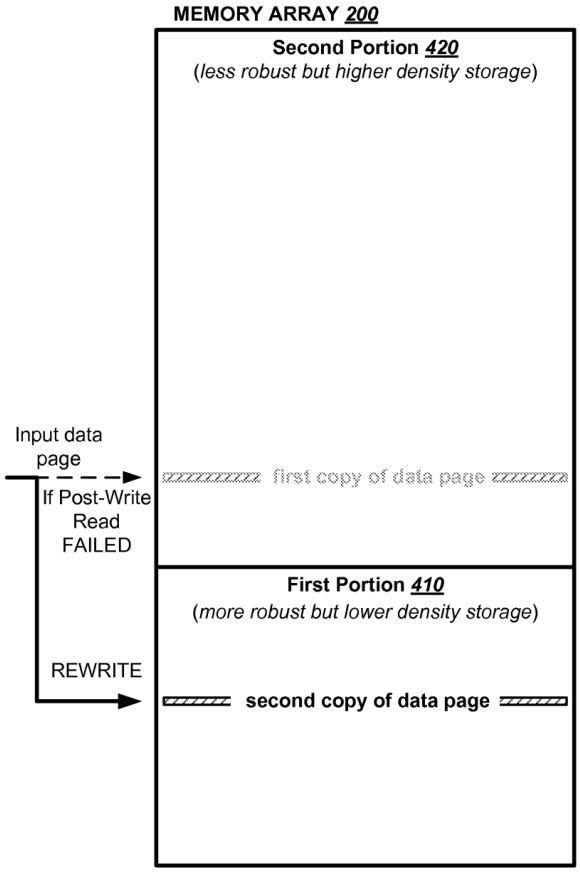

FIG. 14B

Figure 14B illustrates memory array 200 "partitioned into a first portion 410 and a second portion 420." Ex. 1045, 16:14–17, 17:7–8, Fig. 14B. "The first portion 410 has the memory cells configured as lower density storage with each cell storing less number of bits than that of the second portion." *Id.* at 16:19–22. "The second portion 420 has the memory cells configured as high density storage with each cell storing multiple bits of data." *Id.* at 16:17–19. Memory array 200 is a flash memory, i.e., a non-volatile memory. *Id.* at 1:18–19, 1:27–28, 4:13–16, 9:36–40, 11:14–18, 17:24–29, 17:41–42.

Preferably, a page of incoming data "to be written to the memory array 200" is "stored in the high density second portion for the sake of efficiency and high capacity." Ex. 1045, 16:41–43. Thus, "a first copy of the data page is written to the second portion." *Id.* at 16:44–45. Then, "the first copy of the data page is read back" in a post-write read operation "to determine if there are any errors." *Id.* at 16:46–47.

If "the number of error bits does not exceed the predetermined amount, the first copy is regarded stored in the second portion [and] is deemed valid." Ex. 1045, 16:51–54. But if the post-write read operation detects that "the number of error bits in the data page has exceeded the predetermined amount, a second copy of the data page is rewritten to the first portion." *Id.* at 17:9–11. Figure 14B shows "a rewrite of a second copy of the data page into the first portion of the memory array." *Id.* at 17:7–8, Fig. 14B.

After "the second copy has been written to the first portion, it will replace the first copy in the second portion as the valid copy." Ex. 1045, 17:15–17. Then, the "first copy will become obsolete," and "a directory in a block management system" will be "updated to direct subsequent access to the second copy." *Id.* at 17:17–20.

Gavens's Figure 16A (reproduced below) depicts another array of memory cells configured with a first portion and a second portion:

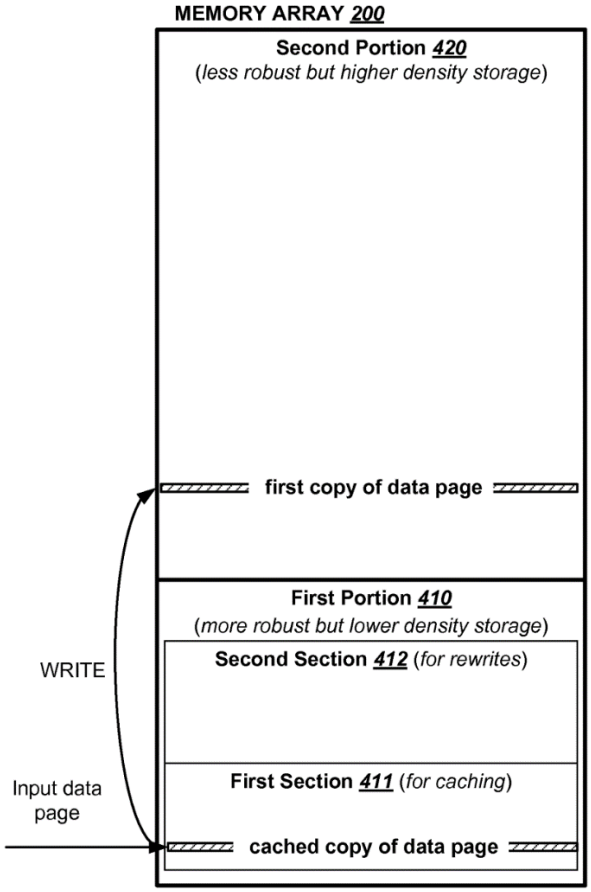

FIG. 16A

Figure 16A illustrates memory array 200 "partitioned into a first portion 410 and a second portion 420." Ex. 1045, 18:12–14, Fig. 16A. "The first portion 410 has the memory cells configured as lower density storage with each cell storing less number of bits than that of the second portion." *Id.* at 18:16–18. "The first portion 410 is further provided with a first section 411 for caching incoming data and a second section 412 for storing rewrites from the second portion." *Id.* at 18:21–23. "The second portion 420 has the memory cells configured as high density storage with each cell storing multiple bits of data." *Id.* at 18:14–16. Memory array 200

is a flash memory, i.e., a non-volatile memory. *Id.* at 1:18–19, 1:27–28, 4:13–16, 9:36–40, 11:14–18, 19:1–6, 19:23–24.

A page of incoming data "to be written to the memory array 200" is "cached in the first section 411 of the first portion 410." Ex. 1045, 18:24–26. Next, a first copy is "stored in the high density second portion for the sake of efficiency and high capacity." *Id.* at 18:26–28. Thus, "a first copy of the data page is written to the second portion." *Id.* at 18:28–29. Then, the "first copy of the data page in the second portion is read back" in a post-write read operation "to determine if there are any errors." *Id.* at 18:41–43. "This is accomplished by comparison with the cached copy." *Id.* at 18:43–44.

If "the number of error bits does not exceed the predetermined amount, the first copy stored in the second portion is deemed to be valid." Ex. 1045, 18:45–47. If so, the "cached copy will become obsolete," and "a directory in a block management system" will be "updated to direct subsequent access to the first copy." *Id.* at 18:47–50. But if the post-write read operation detects that "the number of error bits in the data page of the first copy has exceeded the predetermined amount, a second copy of the data page is rewritten to the second section 412 of the first portion 410." *Id.* at 18:55–59. "The second copy is taken from the cached copy." *Id.* at 18:59–60.

After "the second copy has been written to the second section 412 of the first portion, it will replace the first copy in the second portion" as the valid copy. Ex. 1045, 18:61–63. Then, the "first copy and the cached copy will become obsolete," and "a directory in a block management system" will

be "updated to direct subsequent access to the second copy." *Id.* at 18:63–67.

3. Independent Claim 1

(a) Limitation 1g

Claim 1 recites as follows:

> the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation.

Ex. 1001, 8:10–21 (limitation 1g). Thus, limitation 1g requires that when the "controller" performs a data integrity test, the "controller" reads the data that was written to the MLC nonvolatile memory element and then compares the data that was just read from the MLC nonvolatile memory element to the "retained data" in the "random access volatile memory." *Id.*

(b) Petitioner's Contentions

Petitioner contends that Gavens discloses "random access volatile memory" according to claim 1, e.g., as required by limitation 1g, in the following locations:

(1) the "Background of the Invention" section as "RAM"; and

(2) Figure 16A as first section 411 in first portion 410, with first section 411 used for caching such that "a cache copy of the input data is programmed into the cache."

Pet. 53 (citing Ex. 1045, 1:26, 4:35–37, Fig. 16A).

Petitioner contends that Gorobets discloses "random access volatile memory" according to claim 1, e.g., as required by limitation 1g, in the following locations:

(1) the "Background" section in paragraph 18 as "controller RAM";

(2) Figure 1 as RAM 130 "in the controller 100";

(3) Figure 11 as cache RAM 102 "in the controller"; and

(4) Figure 20 as RAM 511 "in the controller and in the memory 503."

Pet. 53–54 (citing Ex. 1049 ¶¶ 18, 56, 109, 130, Figs. 1, 11, 20).

For example, Gorobets's Figure 11 (reproduced below) depicts a host operating with a flash memory device through a series of caches at different levels of the system:

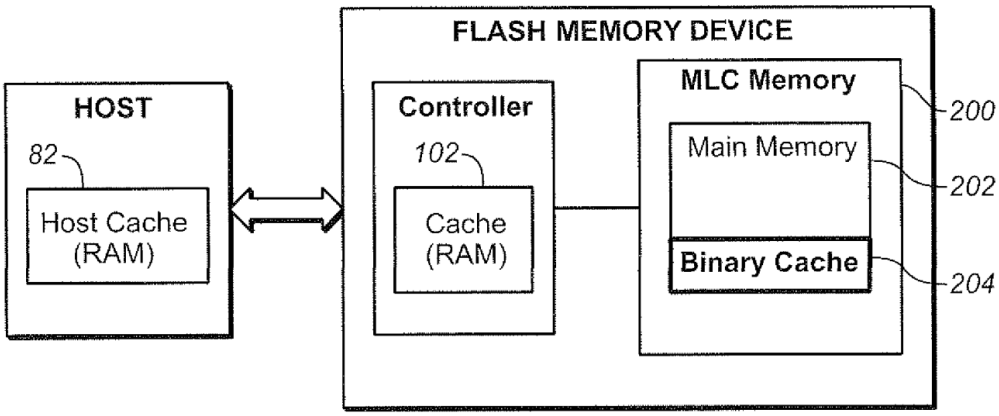

FIG. 11

Figure 11 illustrates a host including host cache (RAM) 82 operating with a flash memory device having (1) a controller including controller cache (RAM) 102 and (2) MLC non-volatile memory 200 partitioned into (i) "first portion 202 [that] has the memory cells operating as a main memory for user data in either MLC or binary mode" and (ii) "second portion 204 [that] has

the memory cells operating as a cache in a binary mode." Ex. 1049 ¶ 109, Fig. 11.

Regarding limitation 1g's requirement that when the "controller" performs a data integrity test, the "controller" reads the data that was written to the MLC nonvolatile memory element and then compares the data that was just read from the MLC nonvolatile memory element to the "retained data" in the "random access volatile memory," Petitioner asserts that "[i]t would have been obvious to compare the data read from the second portion of MLC memory to a cached copy of the data retained in the RAM." Pet. 63. As support, Petitioner cites Gorobets's disclosures about (1) RAM used "as a controller cache of the memory controller" and (2) transferring data initially from a host to RAM and subsequently from RAM to non-volatile memory. *Id.* (citing Ex. 1002 ¶ 125; Ex. 1049 ¶¶ 24, 104, 109, 130, 136, 143–144).

For example, Gorobets's Figure 20 (reproduced below) depicts a data transfer flow initially from a host to RAM and subsequently from RAM to non-volatile memory:

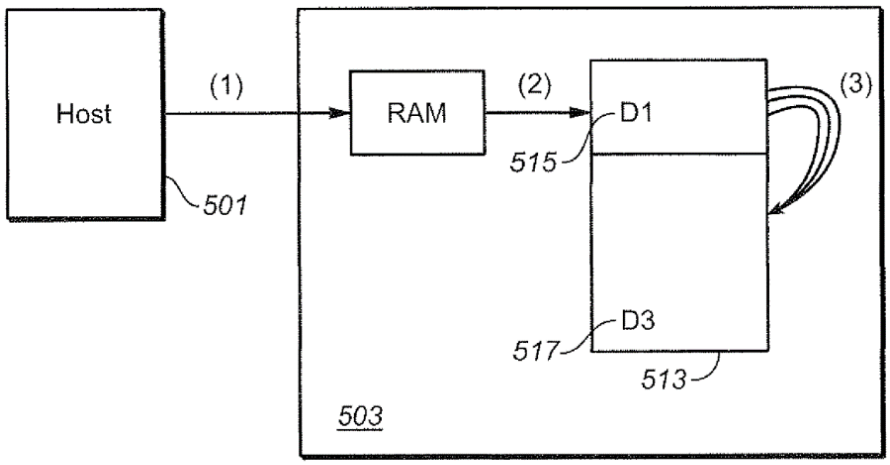

FIG. 20

Figure 20 illustrates host 501 and memory 503 including RAM 511 and non-volatile memory 513 partitioned into binary section D1 515 and MLC section D3 517. Ex. 1049 ¶ 130, Fig. 20. As indicated by step (1) in Figure 20, data is transferred from host 501 to memory 503 and "initially stored on the volatile buffer memory RAM 511, which is typically part of the controller." *Id.* ¶¶ 130, 136, Fig. 20; *see id.* ¶ 142. As indicated by steps (2) and (3) in Figure 20, from "RAM 511 the data is then written into the non-volatile memory 513, first into the binary section D1 515 and then on into the MLC section D3 517." *Id.* ¶¶ 130, 136, Fig. 20; *see id.* ¶¶ 143–144.

For limitation 1g, Petitioner also cites Paley's disclosure that a memory manager in a controller "maintains system control data and directory data associated with its operations among the flash memory 200 and the controller RAM 130." Pet. 63 (quoting Ex. 1051 ¶ 155).

(c) Patent Owner's Contentions

Patent Owner disputes that Gavens discloses "random access volatile memory" according to claim 1, e.g., as required by limitation 1g. *See* Prelim. Resp. 68–73. Regarding the "RAM" discussed in Gavens's "Background of the Invention" section, Patent Owner contends that Gavens distinguishes RAM and non-volatile memory by stating as follows: "Unlike RAM (random access memory) that is also solid-state memory, flash memory is non-volatile, and retaining its stored data even after power is turned off." *Id.* at 68 (quoting Ex. 1045, 1:26–29); *see id.* at 72. Regarding Gavens's disclosure that "a cache copy of the input data is programmed into the cache," Patent Owner contends that the cache is non-volatile memory

rather than "random access volatile memory" as required by limitation 1g. *Id.* at 73 (citing Ex. 1045, 4:14–15, 4:35–37).

Patent Owner contends that Gavens's Figure 16A does not depict "random access volatile memory" as required by limitation 1g. *See* Prelim. Resp. 72. Patent Owner explains that Gavens describes "storing data in 'a first section of the first portion' and 'a second section of the first portion' 'in the nonvolatile memory.'" *Id.* (citing Ex. 1045, 4:13–16, 19:1–24).

As for Gorobets, Patent Owner asserts that Petitioner "cites caches from Gavens and Gorobets that are entirely unrelated." Prelim. Resp. 74. According to Patent Owner, Gavens's Figure 16A concerns "caching data in non-volatile memory where it is retained for use in error detection" because "this reduces reliance on the controller," whereas Gorobets's disclosure of RAM concerns "a volatile RAM-based cache for temporarily storing data before it is passed to non-volatile memory." *Id.* at 74, 78–79 (emphases omitted) (citing Ex. 1045, 18:21–67; Ex. 1049 ¶¶ 109, 144).

Patent Owner contends that Petitioner "does not explain how the disparate teachings" of the documents that Gavens incorporates by reference, including Gorobets and Paley, "combine with the cited teachings of Gavens" to yield the claimed invention. *See* Prelim. Resp. 78–85. Patent Owner contends that Petitioner "does not explain what teachings from Gorobets and/or Paley are being used to modify Gavens's system" or why an ordinarily skilled artisan "would have made any modification" to Gavens's system. *Id.* at 82–83. According to Patent Owner, Petitioner alleges that "it would have been obvious to compare data read from MLC with data retained in random access volatile memory" as required by limitation 1g, and then

Petitioner "provides a disjointed list of citations from Gorobets and Paley." *Id.* at 83 (citing Pet. 63).

Further, Patent Owner argues that "even when parsed individually, Petitioner's citations fail to show that Gavens in view of Gorobets and/or Paley discloses or suggests" limitation 1g. Prelim. Resp. 83 (citing Pet. 63). Patent Owner asserts that the cited portions of Gorobets (1) relate to using RAM to temporarily store data before transferring the data to non-volatile memory and (2) say "nothing about retaining data" in RAM "for later use in a data integrity test performed by the controller" as required by limitation 1g. *Id.* at 83–84 (citing Ex. 1049 ¶¶ 109, 130, 144; Ex. 2001 ¶ 169). Patent Owner also asserts that Paley's disclosure that a memory manager in a controller "maintains system control data and directory data associated with its operations among the flash memory 200 and the controller RAM 130" has "no relation" to limitation 1g. *Id.* at 84 (quoting Ex. 1051 ¶ 155) (citing Pet. 63; Ex. 2001 ¶ 171).

(d) <u>Analysis</u>

Based on the current record, we agree with Patent Owner that Petitioner does not explain how the teachings of Gorobets and Paley "combine with the cited teachings of Gavens" to yield limitation 1g. *See* Pet. 57–63; Prelim. Resp. 78–85.

Initially, contrary to Petitioner's contention, Gavens does not disclose "random access volatile memory" according to claim 1, e.g., in a "system" with, among other things, a "controller" and a "bank of nonvolatile memory." *See* Ex. 1001, 7:28–8:34; Ex. 1045, 1:26–29, 4:35–37, 16:14–19:24, code (57), Figs. 14A–14B, 15, 16A–16C, 17; Ex. 2001 ¶¶ 135–139, 155, 161; Pet. 53. Regarding the "RAM" discussed in Gavens's

"Background of the Invention" section, Gavens states as follows: "Unlike RAM (random access memory) that is also solid-state memory, flash memory is non-volatile, and retaining its stored data even after power is turned off." Ex. 1045, 1:26–29; *see* Ex. 2001 ¶¶ 106, 136. Hence, Gavens distinguishes "its purported invention from RAM." Ex. 2001 ¶ 106.

Regarding Gavens's disclosure that "a cache copy of the input data is programmed into the cache," Gavens explains that "the first portion" of a flash memory "serves as a cache for incoming data, so a cache copy of the input data is programmed into the cache." Ex. 1045, 4:13–16, 4:35–37, 17:43–45. Gavens also explains that a "flash memory is non-volatile." *Id.* at 1:27–28; *see* Ex. 2001 ¶¶ 106, 136, 138. Thus, "the first portion" that "serves as a cache for incoming data" is non-volatile memory and does not correspond to the claimed "random access volatile memory." Ex. 2001 ¶ 148; *see* Ex. 1045, 4:13–16, 4:35–37.

Further, Gavens's Figure 16A illustrates memory array 200 "partitioned into a first portion 410 and a second portion 420" where the first portion includes "a first section 411 for caching incoming data and a second section 412 for storing rewrites from the second portion." Ex. 1045, 18:12–14, 18:21–23, Fig. 16A. According to Gavens, memory array 200 is a flash memory, i.e., a non-volatile memory. Ex. 1045, 1:18–19, 1:27–28, 4:13–16, 9:36–40, 11:14–18, 17:24–29, 17:41–42, 19:1–6, 19:23–24; *see* Ex. 2001 ¶¶ 106, 136, 138. Hence, contrary to Petitioner's contention, first section 411 is non-volatile memory and does not correspond to the claimed "random access volatile memory." *See* Ex. 2001 ¶¶ 145, 150–151; Pet. 53.

Regarding limitation 1g's requirement that when the "controller" performs a data integrity test, the "controller" reads the data that was written

to the MLC nonvolatile memory element and then compares the data that was just read from the MLC nonvolatile memory element to the "retained data" in the "random access volatile memory," Petitioner makes the conclusory assertion that "[i]t would have been obvious to compare the data read from the second portion of MLC memory to a cached copy of the data retained in the RAM." *See* Pet. 63; Ex. 1002 ¶ 125. Although Petitioner relies on the combined disclosures in Gavens and Gorobets or Paley (or both) for teaching that requirement, Petitioner does not explain how or why an ordinarily skilled artisan would have combined those disclosures to yield limitation 1g. *See* Pet. 63; Ex. 1002 ¶¶ 125–126; Ex. 2001 ¶¶ 157, 166–169, 171.

Whether a proposed combination rests on "combining disclosures from multiple references, combining multiple embodiments from a single reference, or selecting from large lists of elements in a single reference, there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful." *Stepan*, 868 F.3d at 1346 n.1. Petitioner fails to identify a motivation to combine multiple embodiments from Gavens and Gorobets or Paley (or both) to yield limitation 1g. *See* Pet. 63; Ex. 1002 ¶¶ 125–126; Ex. 2001 ¶¶ 166–169, 171.

Further, as Patent Owner asserts, the cited portions of Gorobets (1) relate to using RAM to temporarily store data before transferring the data to non-volatile memory and (2) say "nothing about retaining data" in RAM "for later use in a data integrity test performed by the controller" as required by limitation 1g. *See* Pet. 63; Prelim. Resp. 83–84; Ex. 1002 ¶ 125; Ex. 1049 ¶¶ 24, 104, 109, 130, 136, 143–144, Figs. 1, 11, 20–21; Ex. 2001 ¶ 169. Additionally, Paley's disclosure that a memory manager in a

controller "maintains system control data and directory data associated with its operations among the flash memory 200 and the controller RAM 130" does not cure the deficiencies in Gavens and Gorobets with respect to limitation 1g. *See* Ex. 1051 ¶ 155; Ex. 2001 ¶ 171.

Based on the current record and for the reasons discussed above, Petitioner does not show sufficiently for purposes of institution that the cited prior art teaches limitation 1g. Hence, Petitioner does not establish sufficiently for purposes of institution that claim 1 is unpatentable under § 103 because the claim would have been obvious over Gavens in view of an ordinarily skilled artisan's knowledge.

4. DEPENDENT CLAIMS 2–7

Claims 2–7 depend directly from claim 1. Ex. 1001, 8:35–50. Hence, claims 2–7 incorporate all the limitations of claim 1. 35 U.S.C. § 112 ¶ 4.

Based on the current record and for the reasons discussed for claim 1, Petitioner does not establish sufficiently for purposes of institution that claims 2–7 are unpatentable under § 103 because the claims would have been obvious over Gavens in view of an ordinarily skilled artisan's knowledge. *See supra* § III.H.3(d).

IV. DISCRETIONARY DENIAL UNDER 35 U.S.C. § 324(a) IN VIEW OF PARALLEL LITIGATION

Under § 324(a), the Director possesses "broad discretion" in deciding whether to institute a post-grant review. *See* 35 U.S.C. § 324(a); *Saint Regis Mohawk Tribe v. Mylan Pharms. Inc.*, 896 F.3d 1322, 1327 (Fed. Cir. 2018). The Board decides whether to institute a post-grant review on the Director's behalf. 37 C.F.R. § 42.4(a).

Based on *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential), Patent Owner argues that we should exercise our discretion under § 324(a) to deny institution in view of the Texas case. *See* Prelim. Resp. 1–2, 15–23; *supra* Section II.B. Petitioner argues that we should decline to exercise our discretion under § 324(a) to deny institution. *See* Pet. 76–79.

Based on the current record and for the reasons discussed above, we determine that Petitioner has failed to demonstrate that it is "more likely than not" that at least one of the claims challenged in the Petition is unpatentable. *See supra* §§ III.D.4, III.E.4, III.F.4, III.G.4, III.H.3–III.H.4. Hence, we do not consider discretionary denial under § 324(a).

V. DISCRETIONARY DENIAL UNDER 35 U.S.C. § 325(d)

Section 325(d) provides that "[i]n determining whether to institute" a post-grant review, "the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." 35 U.S.C. § 325(d).

When deciding whether to exercise our discretion under § 325(d), we follow the two-part framework set forth in *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential). Specifically, we must first determine "whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office." *Id.* at 8. That determination involves "two separate issues":

(1) "whether the petition presents to the Office the same or substantially the same art previously presented to the Office"; and

(2) "whether the petition presents to the Office the same or substantially the same arguments previously presented to the Office."

Id. at 7.

If "either condition of first part of the framework is satisfied," we must then determine "whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims." *Advanced Bionics*, IPR2019-01469, Paper 6 at 8. "An example of a material error may include misapprehending or overlooking specific teachings of the relevant prior art where those teachings impact patentability of the challenged claims." *Id.* at 8 n.9.

Patent Owner argues that we should exercise our discretion under § 325(d) to deny institution because "both parts of the *Advanced Bionics* framework are met." Prelim. Resp. 64, 68. Specifically, Patent Owner asserts that the Examiner reviewed the published patent application (U.S. Patent Application Publication No. 2011/0096601) that issued as Gavens. *Id.* at 64. Patent Owner also asserts that Petitioner ignores "clear issues" under § 325(d) and fails to demonstrate material error by the Office. *Id.* at 66–67.

Petitioner does not address issues under § 325(d). *See, e.g.*, Pet. 28–79.

Based on the current record and for the reasons discussed above, we determine that Petitioner has failed to demonstrate that it is "more likely than not" that at least one of the claims challenged in the Petition is unpatentable. *See supra* §§ III.D.4, III.E.4, III.F.4, III.G.4, III.H.3–III.H.4. Hence, we do not consider discretionary denial under § 325(d).

VI. CONCLUSION

After considering the Petition, the Preliminary Response, and the evidence of record, and for the reasons discussed above, we determine that Petitioner has failed to demonstrate that it is "more likely than not" that at least one of the claims challenged in the Petition is unpatentable. Hence, we deny the Petition and do not institute a post-grant review.

VII. ORDER

Accordingly, it is

ORDERED that the Petition is denied and no trial is instituted.

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