

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,
Petitioner,

v.

VERVAIN, LLC,
Patent Owner.

IPR2025-00215
U.S. Patent No. 10,950,300

**PATENT OWNER'S REQUEST FOR DISCRETIONARY DENIAL OF
INSTITUTION**

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EXHIBIT LIST

Exhibit No.	Description
2001	Declaration of Dr. Sunil Khatri
2002	[RESERVED]
2003	[RESERVED]
2004	[RESERVED]
2005	[RESERVED]
2006	<i>Vervain v. Western Digital Corp. et al.</i> , No. 6:21-cv-488-ADA, Dkt. 41 (W.D. Tex. Jan. 24, 2022) (Claim Construction Order)
2007	[RESERVED]
2008	[RESERVED]
2009	[RESERVED]
2010	[RESERVED]
2011	[RESERVED]
2012	[RESERVED]
2013	[RESERVED]
2014	[RESERVED]
2015	[RESERVED]
2016	[RESERVED]
2017	[RESERVED]
2018	<i>Vervain, LLC v. Phison Electronics Corporation</i> , No. 1:24-cv-259-ADA, Dkt. 16 (W.D. Tex. Jul. 15, 2024) (agreed scheduling order)
2019	[RESERVED]

Exhibit No.	Description
2020	[RESERVED]
2021	“Judge Albright Patent FAQ,” https://www.txwd.uscourts.gov/for-attorneys/judge-albright-courtroom-faq/ . Accessed December 18, 2024)
2022	[RESERVED]
2023	Judge Albright’s Standing Order Governing Proceedings (OGP) 4.4—Patent Cases, Filed January 23, 2024.
2024	Excerpts from the Prosecution History of U.S. Patent No. 11,830,546
2025	U.S. Patent App. Pub. No. 2011/0096601 to Gavens et al. (“Gavens-601”)
2026	[RESERVED]
2027	[RESERVED]
2028	[RESERVED]
2029	[RESERVED]
2030	[RESERVED]
2031	Preliminary Claim Constructions for <i>Vervain, LLC v. Phison Electronics Corporation</i> , No.1:24-cv-259-ADA and <i>Vervain, LLC v. Kingston Technology Company., et al.</i> , No. 1:24-cv-254-ADA – email from Mr. Brown received on February 5, 2025.
2032	Markman Hearing Transcript dated February 6, 2025, for <i>Vervain, LLC v. Phison Electronics Corporation</i> , No. 1:24-cv-259-ADA and <i>Vervain, LLC v. Kingston Technology Company., et al.</i> No. 1:24-cv-254-ADA.
2033	<i>Vervain v. Western Digital Corp. et al.</i> , No. 6:21-cv-00488-ADA, Dkt. 180 (W.D. Tex. Jul. 26, 2023) (Redacted Copy of Order on the Pending Motions and Motions <i>In Limine</i>).

Exhibit No.	Description
2034	[RESERVED]
2035	[RESERVED]
2036	[RESERVED]
2037	<i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259, Dkt. 53 (W.D. Tex. Jan. 29, 2025) (Joint Notice Extending Deadlines)
2038	[RESERVED]
2039	<i>Phison Electronics Corp. v. Vervain, LLC</i> , PGR2024-00047, Paper 9 (P.T.A.B. Mar. 17, 2024) (Decision Denying Institution of Post-Grant Review of U.S. Patent No. 11,830,546)
2040	[RESERVED]
2041	<i>Phison Electronics Corp. v. Vervain, LLC</i> , PGR2024-00048, Paper 9 (P.T.A.B. April 28, 2025) (Decision Denying Institution of Post-Grant Review of U.S. Patent No. 11,854,612)
2042	Docket Sheet for <i>Vervain, LLC v. Phison Electronics Corporation</i> , No. 1:24-cv-259-ADA (W.D. Tex.) (accessed May 12, 2025)
2043	Phison’s Final Invalidity Contentions served on February 28, 2025 in <i>Vervain, LLC v. Phison Electronics Corporation</i> , No. 1:24-cv-259-ADA (W.D. Tex.)
2044	“Interim Processes for PTAB Workload Management Memorandum,” issued March 26, 2025, https://www.uspto.gov/sites/default/files/documents/InterimProcesses-PTABWorkloadMgmt-20250326.pdf . Accessed May 13, 2025.

I. INTRODUCTION

Pursuant to the “Interim Processes for PTAB Workload Management Memorandum” issued March 26, 2025 (“the *PTAB Memorandum*”) and the Board’s Notice Extending the Deadline for Discretionary Briefing dated April 14, 2025 (Paper 8), Patent Owner Vervain, LLC (“PO” or “Vervain”) respectfully submits this brief requesting that the Director exercise her discretion to deny institution of the Petition for *Inter Partes* Review (IPR) (Paper 2) of U.S. Patent No. 10,950,300 (“300 Patent” or “the Challenged Patent”) filed by Phison Electronics Corporation (“Phison” or “Petitioner”).

The Director should exercise her discretion and deny institution under 35 U.S.C. § 314(a)—instituting this Petition would require a considerable and inefficient use of the Board’s resources. The parties are already litigating a parallel case in district court, which involves the Challenged Patent and seven others. The parallel case is well past its infancy. Before the institution decision is due in this IPR proceeding, the district court will have already held the *Markman* hearing, and the parties will have completed fact discovery and submitted expert reports. And trial in the district court case is scheduled for *eight months before* the final written decision deadline here. Furthermore, Petitioner advances overlapping invalidity grounds in district court but *has not stipulated to any estoppel* in the event this

Petition is instituted. The advanced parallel proceeding should proceed, and this Petition should be denied.

Further, the Petition is weak on the merits. The Petition includes one ground challenging claims 1-12 (“Challenged Claims”). This ground relies on a single-reference obviousness theory based on U.S. Patent No. 8,634,240 (“Gavens”) (Ex. 1045). However, the argument underlying Petitioner’s Gavens ground was already rejected by the Board in its decisions denying institution of the related PGRs. *See* Exs. 2039 (denying institution of PGR2024-00047), 2041 (denying institution of PGR2024-00048). Specifically, the obviousness ground fails to reconcile key differences between the Challenged Claims and Gavens. The Challenged Claims require a controller that performs a data integrity test based upon data *retained in random access volatile memory* (RAM), a feature that Gavens neither discloses nor suggests.

Accordingly, PO respectfully requests that the Director exercise her discretion to deny institution of the Petition.

II. BACKGROUND

A. The 300 Patent And The Vervain Patent Family

U.S. Patent No. 10,950,300 (the “Challenged Patent”) belongs to a family of patents including U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; 10,950,300; 11,830,546; 11,854,612; 11,967,369; and 11,967,370 (the “Vervain Patents”).

These patents share the same specification and are continuations stemming from U.S. Patent No. 8,891,298.

The Vervain Patents, each entitled “Lifetime Mixed Level Non-Volatile Memory System,” have effective filing dates of July 19, 2011. Ex. 1001, Cover. Dr. G. R. Mohan Rao is the sole named inventor of the Vervain Patents.

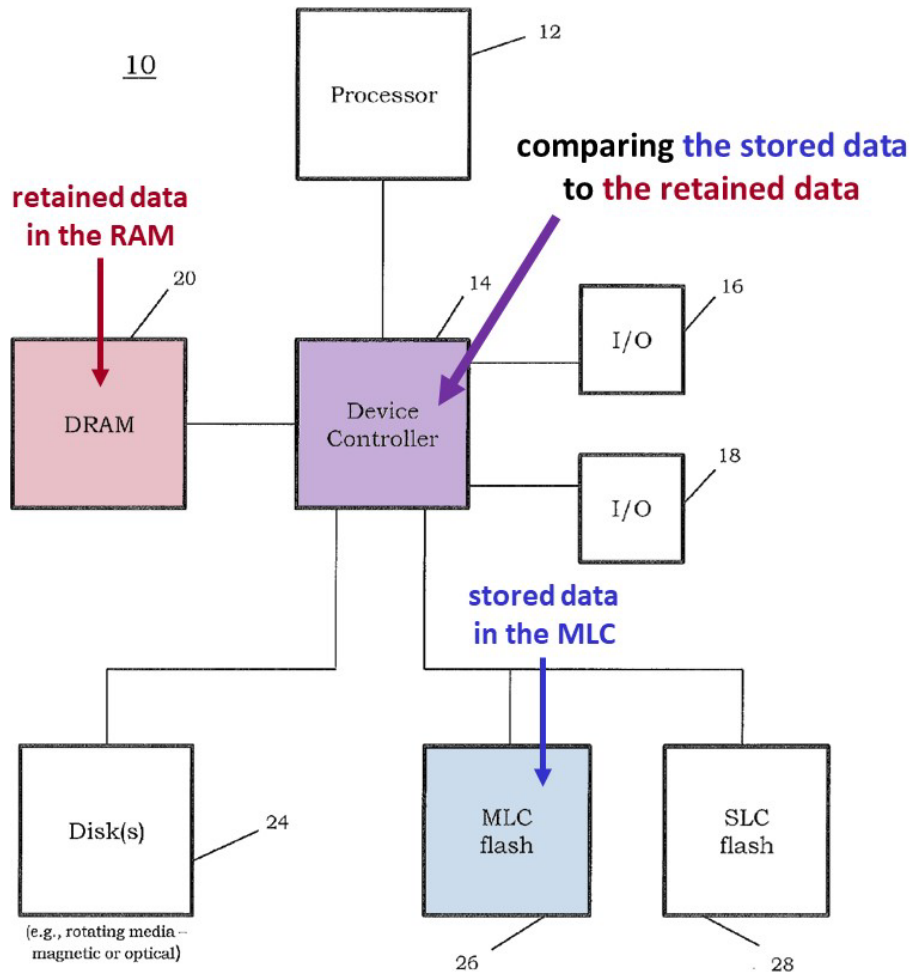
At a high level, the Vervain Patents describe a reliable flash memory storage system combining both single-level cell (SLC) and multi-level cell (MLC) non-volatile memories.¹ Ex. 1001, Abstract; Ex. 2001, ¶37. SLC memory stores 1 bit per cell, and MLC memory stores more than 1 bit per cell. Ex. 1001, 2:17-20; Ex. 2001, ¶¶32-34. In general, SLC is faster and less prone to errors, but requires more space and power to store a given amount of data. Ex. 1001, 1:58-62.

The Vervain Patents describe a particular way of writing data to MLC and performing a data integrity test. The data integrity test checks the integrity of the data (*i.e.*, whether errors have occurred). The Vervain Patents explain that, if the data integrity test reveals a problem such as corrupt data, the data can be remapped

¹ Non-volatile memories can store information even after the system is powered off. Flash memory is a specific type of non-volatile memory, where data is stored in “blocks” of “pages.” Ex. 1001, 2:52-3:2; Ex. 2001, ¶27.

to SLC (which is less error-prone) or other MLC blocks. Ex. 1001, 3:13-3:35, 4:30-36.

As seen in Figure 1 below, the Vervain Patents describe a controller (purple) that controls a dynamic random access memory (DRAM) (red).

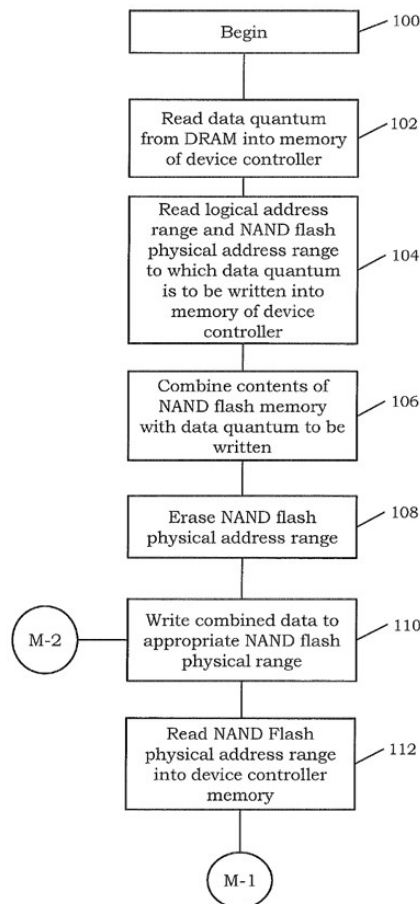


Ex. 1001, Fig. 1 (annotations added), 5:37-38.

The DRAM is used during a write access operation to the MLC flash (highlighted blue). The data to be written to the MLC flash is maintained (or retained) in the DRAM. Ex. 1001, 5:59-61. If time permits, the controller performs

a data integrity test on the data that was stored in the MLC. *Id.*, 5:61-64. If the stored data fails the data integrity test, the address range for the stored data is remapped to a new location (*e.g.*, the SLC flash). *Id.*, 5:64-67.

Figures 3A and 3B show in more detail how the DRAM and controller are used during the write access operation and data integrity test.



Id., Fig. 3A.

The write access operation begins at step 100. *Id.*, 6:17-22. In step 102, the data to be written to the MLC is read from the DRAM into a controller memory. *Id.* In step 104, the controller obtains the logical and physical address ranges for the data

to be written to the MLC. *Id.*, 6:22-25. In step 106, the controller combines the data from the DRAM with data from the MLC. *Id.*, 6:25-27. In step 108, the controller erases the physical address range where the data is being written. *Id.*, 6:27-28. Finally, in step 110, the combined data is written to the MLC flash. *Id.*, Fig. 3A (step 110), 6:28-30.

The data integrity test begins at the bottom of Figure 3A and continues to Figure 3B (below). In step 112, the data that was stored in the MLC (“the stored data”) is read into the controller memory. *Id.*, 6:30-32. In step 114, the stored data is compared to the data that was retained in the DRAM (“the retained data”). *Id.*, 6:33-38.

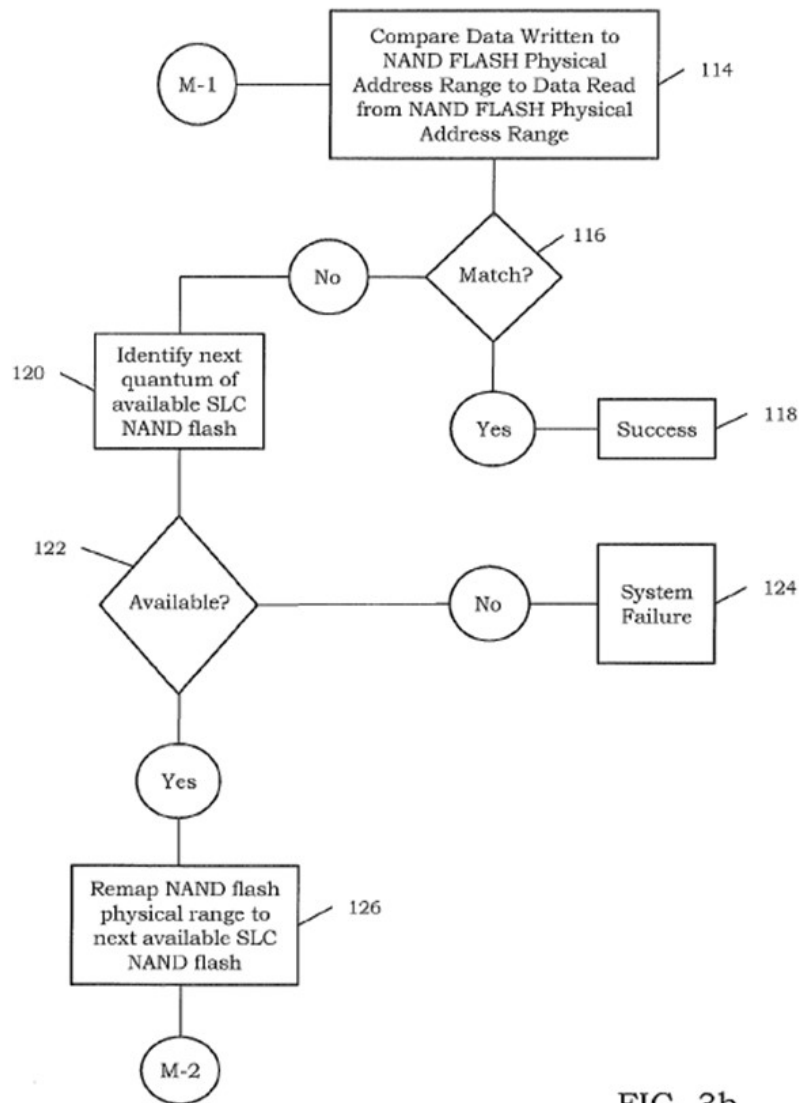


FIG. 3b

Id., Fig. 3B.

If there is a match, the data was successfully stored in the MLC. *Id.*, 6:38-40.

If not, the retained data is written to another location (*e.g.*, SLC). *Id.*, 6:40-44.

1. The Challenged Claims

Dr. Rao recognized that there were advantages in retaining data at the random access volatile memory (RAM) to assist with the data integrity test. Accordingly,

data retained in RAM is a key feature of the invention claimed in the Challenged Patent.

The Challenged Patent includes two independent claims: Claims 1 and 12. Claim 1 is representative for purposes of this brief and requires a system for storing data comprising: (1) MLC non-volatile memory; (2) SLC non-volatile memory; and (3) a controller that performs a data integrity test based upon data retained in random access volatile memory (shown in red font below). The data retained in RAM is particularly important to the “data integrity test” in [1h].

Claim 1	
[1Pre]	A system for storing data comprising:
[1a]	memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;
[1b]	at least one controller to operate memory elements and associated memory space;
[1c]	at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;
[1d]	at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;
[1e]	at least one random access volatile memory ;

[1f]	an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory ;
[1g]	the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and <u>retain such stored data in the random access volatile memory</u> ;
[1h]	the controller performing a <u>data integrity test</u> on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the <u>retained data in the random access volatile memory</u> ;
[1i]	wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and
[1j]	wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

B. Petitioner’s IPR And PGR Filings

Petitioner filed requests for *inter partes* review and post grant review challenging each of the Vervain Patents—U.S. Patent Nos. 8,891,298 (IPR2025-00212); 9,196,385 (IPR2025-00213); 9,997,240 (IPR2025-00214); 10,950,300 (IPR2025-00215); 11,830,546 (PGR2024-00047); 11,854,612 (PGR2024-00048); 11,967,369 (PGR2025-00010); and 11,967,370 (PGR2025-00011).

The Board has already denied institution of two petitions on the merits—PGR2024-00047 and PGR2024-00048 (“the Denied PGRs”). *See* Exs. 2039, 2041. The Board issued detailed decisions denying institution, substantively rejecting each of Petitioner’s grounds. *See generally id.*

The Board is expected to issue a decision on whether to institute IPR2025-00212 by June 26, 2025.

The Director is expected to decide by July 14, 2025, whether to exercise her discretion to deny institution of the five remaining petitions, including the present Petition. If the Director does not exercise her discretion, the Board is expected to decide whether to deny institution on the merits by August 14, 2025.

C. The Parallel District Court Litigation

On March 8, 2024, Patent Owner (“PO”) filed a complaint against Phison asserting infringement of the Challenged Patent, along with five additional Vervain Patents, in *Vervain, LLC v. Phison Electronics Corporations*, No. 1:24-cv-259-ADA

(W.D. Tex.) (“the Parallel Litigation”). *See* Ex. 2042 (docket sheet showing the original Complaint, filed March 8, 2024, which asserted infringement of the first six Vervain Patents); *see also* Ex. 1082 (First Amended Complaint, filed May 13, 2024, which added infringement assertions for two more Vervain Patents—U.S. Patent Nos. 11,967,369 and 11,967,370).

The Parallel Litigation is well underway. The parties completed claim construction briefing, and the Court (with Judge Albright presiding) provided constructions for the disputed terms—all in PO’s favor—at a *Markman* hearing on February 6, 2025. *See* Exs. 2031-2032. Fact discovery opened on December 9, 2024, and the parties exchanged final invalidity and infringement contentions on February 28, 2025. *See* Exs. 2018, 2037. The Petitioner then moved for leave to file amended final invalidity contentions on March 27, 2025, and PO moved for leave to file amended final infringement contentions on May 2, 2025. *See* Ex. 2042.

Further, the Parallel Litigation is rapidly approaching trial. Fact discovery closes on July 7, 2025, necessitating that the parties begin depositions in June. *See* Ex. 2018. Opening expert reports are due July 11, 2025, followed by summary judgment and *Daubert* motions on September 12. *See* Ex. 2018. ***Trial is scheduled to begin on December 15, 2025.*** *See id.*

D. Prior Litigation Involving The Vervain Patents

Vervain previously asserted four of the Vervain Patents—U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; and 10,950,300—against Western Digital and Micron in *Vervain, LLC v. Micron Technology, Inc. et al.*, No. 6:21-cv-487-ADA (W.D. Tex) and *Vervain, LLC v. Western Digital Corp et al.*, No. 6:21-cv-488-ADA (W.D. Tex.) (“the Prior Litigation”). In these cases, the Court held a *Markman* hearing and ruled on summary judgment motions, maintaining the validity of the Vervain Patents. *See, e.g.*, Exs. 2006 (Claim Construction Order, issued January 24, 202), 2033 (Summary Judgment Order).

Further, in these cases, Micron filed IPRs against U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; and 10,950,300 (*see* IPR2021-01547, -01548, -01549, and -01550). These IPRs were terminated prior to Final Written Decisions, following the parties’ joint motions to terminate after reaching a settlement.

III. THE DIRECTOR SHOULD EXERCISE HER DISCRETION AND DENY INSTITUTION UNDER 35 U.S.C. § 314(a)

The Director should exercise her discretion and deny institution on all grounds because of the significant overlap with the Parallel Litigation, which is scheduled for trial well before a Final Written Decision would be expected here.

As shown below, the *Fintiv* factors all weigh in favor of denying institution under 35 U.S.C. § 314(a). *See NXP USA, Inc. v. Impinj, Inc.*, PGR2022-00005, Paper 18 at 7 (P.T.A.B. May 2, 2022) (weighing *Fintiv* factors and denying

institution); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (“*Fintiv*”).

A. Factor 1: The Parallel Litigation Has Not Been Stayed And Is Unlikely To Be Stayed Even If This Petition Is Instituted

This factor weighs against institution because a stay of the Parallel Litigation is highly unlikely. Petitioner has not sought a stay, and the Board’s institution decision is expected by August 14, 2025. Given the timing and complexity of the Parallel Litigation, it is improbable that Judge Albright would grant a stay even if the Petition is instituted.

Particularly, August 14, 2025, is after the *close* of fact discovery (July 7, 2025), and after the parties serve opening (July 11, 2025) and rebuttal (August 8, 2025) expert reports. *See* Ex. 2018. Accordingly, the Court will have “expended significant resources,” and would be unlikely to grant a stay. *See, e.g., Sonrai Memory Ltd. v. LG Elecs. Inc.*, No. 6:21-cv-00168-ADA, 2022 WL 2307475, at *3 (W.D. Tex. June 27, 2022) (denying stay when fact discovery opened two weeks before the institution decision).

Further, in the Parallel Litigation, PO asserted *eight patents* against Petitioner Phison. *See* Ex. 1082, ¶2. Phison filed IPR or PGR petitions against each of these patents. But the Board has already denied institution on two of those petitions—PGR2024-00047 and PGR2024-00048. *See* Exs. 2039, 2041. In circumstances such as these, it is even more unlikely that the Court would grant a stay. *See Smart Mobile*

Techs. LLC v. Apple Inc., No. 6:21-cv-00603-ADA, 2023 WL 5051374, at *6 (W.D. Tex. Aug. 8, 2023) (denying stay based on instituted IPRs when institution was not granted on all asserted patents).

Thus, Factor 1 weighs against institution.

B. Factor 2: The Board Would Likely Issue A Final Written Decision Eight Months After Trial

This factor weighs against institution because trial is scheduled to begin eight months before the projected final written decision. Should the Director not exercise her discretion to deny institution, the Board is expected to decide whether to institute by August 14, 2025. Accordingly, the projected statutory deadline for a final written decision would be August 14, 2026—*eight months after the December 15, 2025, trial date*. See Ex. 2018. Judge Albright is highly unlikely to move this trial date, as he has a practice of “not mov[ing] the trial date except in extreme situations.” Ex. 2021; see also *NXP USA*, PGR2022-00005, Paper 18 at 9 (weighing factor 2 in favor of discretionary denial when “the currently scheduled trial in the parallel proceeding is scheduled to begin over two months before our deadline to reach a final decision”); *Google LLC v. Cerence Operating Co.*, IPR2024-01465, 2025 WL 1182608, at *4 (P.T.A.B. Apr. 23, 2025) (weighing factor 2 in favor of discretionary denial when “the district court has set a trial date of October 6, 2025, which is almost seven months before the final written decision in this proceeding would be due in late April

2026” and “nothing in the...record indicates a trial in the District Court Litigation would not take place months before our deadline to reach a final decision”).

C. Factor 3: The Court And Parties Have Invested Heavily In The Parallel Litigation

This factor weighs against institution because the parties and the Court have invested and will continue to invest significant resources in the Parallel Litigation. The Board weighs “the amount and type of work already completed in the parallel litigation by the court and the parties at the time of the institution decision.” *Fintiv*, IPR2020-00019, Paper 11 at 9.

By the time the Board decides whether to institute this IPR in August 2025, the parties will have completed *Markman* briefing (Nov. 22, 2024); briefed a motion to dismiss (which the Court resolved on Dec. 2, 2024); exchanged final infringement and invalidity contentions (Feb. 28, 2025); moved to amend those contentions (Mar. 27, 2025 and May 2, 2025); completed fact discovery (closes July 7, 2025); exchanged opening expert reports (July 11, 2025); and exchanged rebuttal expert reports (Aug. 8, 2025). *See* Exs. 2018, 2037, 2042. In addition, the parties will have completed extensive document production and numerous fact and expert witness depositions.

Furthermore, the Court will have held the *Markman* hearing and issued its constructions (Feb. 6, 2025) and ruled on numerous discovery disputes. *See* Exs. 2031 (Court’s preliminary claim constructions), 2032 (transcript for the February 6

Markman hearing, during which the Court adopted its preliminary constructions); *see also Fintiv*, Paper 11 at 10 (“[D]istrict court claim construction orders may indicate that the court and parties have invested sufficient time in the parallel proceeding to favor denial.”).

Thus, the Court and the parties have invested and will continue to invest significant resources in the Parallel Litigation and, accordingly, this factor weighs against institution. *See NXP USA*, PGR2022-00005, Paper 18 at 9-10 (weighing factor 3 in favor of discretionary denial where the *Markman* hearing and the service of final infringement and invalidity contentions occurred before the Board’s institution decision deadline); *Motorola Sols., Inc. v. Stellar, LLC*, IPR2024-01205, 2025 WL 947070, at *1 (P.T.A.B. Mar. 28, 2025) (Order Granting Director Review, Vacating the Decision Granting Institution, and Denying Institution of *Inter Partes* Review) (finding “factor 3 strongly favors discretionary denial” when “the parties had served extensive infringement and invalidity contentions, served opening and rebuttal expert reports, filed claim construction briefs, and conducted several depositions” and “[t]he court also had held a claim construction hearing and construed the disputed claim terms”).

D. Factor 4: There Is Significant Overlap Between Issues Raised In This Petition And In The Parallel Litigation

This factor weighs against institution given the significant overlap between the Petition and the Parallel Litigation. The Parallel Litigation involves the same

300 Patent as this proceeding, along with seven additional patents. *See* Ex. 1082, ¶2.

Further, the Parallel Litigation already involves the only ground raised in the Petition. Specifically, the Parallel Litigation involves the same Gavens reference (U.S. Patent No. 8,634,240, Ex. 1045) that Petitioner relies on in its single-reference obviousness ground. *See generally* Petition, 6-7. Gavens is the ***only primary reference*** identified for the 300 Patent in Phison’s Invalidity Contentions. *See* Ex. 2043, 6-7. And Phison charted Gavens to the claims. *See id.* (referencing charts included in “Exhibit D”).

Despite this significant overlap, ***Petitioner has not filed a Sotera stipulation or any other stipulation*** to mitigate concerns of duplicative efforts between the District Court and the Board, as well as any concerns regarding potentially conflicting decisions. *See Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 19 (P.T.A.B. Dec. 1, 2020). If this Petition is instituted, Petitioner would necessarily rely on its Gavens ground both before the Board and in the Parallel Litigation, including in its expert report and at trial.

Thus, this factor weighs heavily against institution. *See NXP USA*, PGR2022-00005, Paper 18 at 11-12 (weighing factor 4 in favor of discretionary denial when the petitioner “d[id] not offer a stipulation” and “assert[ed] the same prior art in both proceedings”).

E. Factor 5: The Parties Are The Same In Both Proceedings

The Petitioner and the defendant in the Parallel Litigation “are the same party,” so “this factor weighs in favor of discretionary denial.” *NXP USA*, PGR2022-00005, Paper 18 at 12.

F. Factor 6: Other Circumstances Weigh Against Institution

1. The Merits Of The Petition Are Weak²

The Petition’s single-reference obviousness ground is weak on the merits. Most tellingly, and as explained below, the arguments underlying this ground have already been considered—and rejected—by the Board. *See* Exs. 2039, 2041.

Petitioner presents a single-reference obviousness ground based on Gavens, U.S. Patent No. 8,634,240 (Ex. 1045). As preliminary matter, this ground is weak on the merits because it fails to provide a clear mapping to the prior art and omits even a basic obviousness analysis to support its conclusory assertions about what a person of ordinary skill (“POSA”) would have “understood.” Notwithstanding, Petitioner’s ground—to the extent it can be understood—relies on modifications to Gavens that a POSA would have never made and that cannot be supported. Indeed,

² Patent Owner also filed a “Preliminary Response On The Merits And Other Non-Discretionary Considerations” on May 14, 2025, which provides a more detailed explanation of the Petition’s numerous substantive weaknesses.

the Board already considered a similar argument, which it rejected in denying institution of PGR2024-00047 and PGR2024-00048. *See* Exs. 2039, 2041.

First, Gavens fails to provide a clear mapping to the prior art to identify what it contends reads on the claimed “random access volatile memory.” For example, for limitation [1e], Petitioner ambiguously cites the distinct disclosure from *five different references*. Petition, 32-34. Petitioner cites Gavens itself, along with four references that Gavens purportedly incorporated by reference: Gorobets 912 (Ex. 1049), Paley 180 (Ex. 1051), Harari (Ex. 1057), and Gorobets PCT (Ex. 1058). *See id.* But Petitioner does not make clear what from these distinct disclosures it is mapping to the claimed RAM. Instead, Petitioner vaguely cites distinct disclosure related to RAM from each of the references. *See* Petition, 32 (“Gorobets ‘912 explains the controller [RAM] cache 102...”), 33 (“Paley ‘180 similarly explains that...RAM are employed...”), 33 (“Harari...shows as part of its Fig. 8 ‘cache buffer 705’...”), 33 (“Gorobets PCT...which explained: ‘The SRAM block...’”).

Thus, Petitioner fails to clearly map the distinct teachings of these references to what is claimed, for example to identify what it contends maps to the “random access volatile memory” of limitation [1e]. *See id.* In effect, Petitioner’s ground asks the Board to pick and choose between distinct elements from different disclosures; thus, Petitioner has not demonstrated with particularity how limitation [1e] maps to the prior art, as required by 35 U.S.C. § 312(a)(3). *See also Captioncall*,

LLC v. Ultratec, Inc., IPR2020-01215, 2021 WL 278381, at *7 (P.T.A.B. Jan. 27, 2021) (denying institution when petitioner relied on “distinct” embodiments from a reference and another reference that was incorporated by reference, explaining that “[a]nticipation requires all elements arranged as in the claim without the need to pick and choose elements from different disclosures”); *Masimo Corp. v. Apple Inc.*, IPR2023-00745, Paper 44 (final written decision), 36 (P.T.A.B. Oct. 15, 2024) (determining that the challenged claim is not unpatentable, explaining: “In essence, Petitioner invites the Board to piece together a single theory that meets all claim elements from these disparate theories that each require distinct structures....”) (citing *Amazon.com, Inc., et al. v. Avago Technologies General IP (Singapore) PTE. LTD.*, IPR2017-01112, Paper 11, at 13 (P.T.A.B. Aug. 23, 2017) (“Petitioner is inviting us to assume the role of archeologist of the record, which invitation we decline.”)); *Nearmap US, Inc. v. Eagle View Technologies, Inc.*, IPR2024-00716, Paper 9, 18 (P.T.A.B. Oct. 9, 2024) (denying institution of *inter partes* review, explaining that “[t]he question before us is not whether we could come up with a way to understand how the asserted prior art could render the challenge claims unpatentable, but rather did Petitioner provide the arguments and evidence to show that the challenged claims are unpatentable.”); *Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1379 (Fed. Cir. 2023) (“While the Board should review a petition holistically, it is not obligated to cobble together assertions from different sections of a petition

or citations of various exhibits in order to infer every possible permutation of a petitioner’s argument.” (cleaned up)).

Furthermore, for limitation [1e], Petitioner fails to provide *any* obviousness analysis to combine the distinct disclosures of these references. *See* Petition 32-34, 34 (concluding, “Gavens and its incorporated references *disclose...*”).

Petitioner made the same error in its reliance on Gavens in PGR2024-00047 and PGR2024-00048, which the Board noted in denying institution of those petitions on the merits. The Board agreed with PO’s arguments and determined that Gavens does not disclose a system that relies on any RAM, contrary to Petitioner’s contentions here. *See* Ex. 2041, 42 (decision denying institution of PGR2024-00048, finding: “Gavens’s invention is directed specifically to non-volatile memory” and “a [POSA] would [not] have found Gavens to teach or suggest [a memory system] that includes RAM.”); Ex. 2039, 76 (decision denying institution of PGR2024-00047, where the Board determined that “Gavens does not disclose ‘random access volatile memory’ according to claim 1, e.g. in a ‘system’ with, among other things, a ‘controller’ and a ‘bank of nonvolatile memory’”). The Board explained: “*Incorporation by reference does not relieve Petitioner of its burden to explain how these teachings* [from Gorobets 912] *are to be applied* and why one of ordinary skill in the art would have learned of the recited limitation from the cited material. Petitioner and its declarant do not provide an explanation as to how one of

ordinary skill in the art would have viewed these teachings and why that would have taught or suggested the disputed limitation.” Ex. 2041, 44-45 (emphasis added).

The Board also already determined that Petitioner’s failure to provide the requisite obviousness analysis—for example, to explain how and why a POSA would have misinterpreted Gavens to disclose a system including RAM—is fatal to its ground. *See, e.g.,* Ex. 2041, 43 (“As Patent owner correctly notes, ‘Petitioner...does not state whether Gorobets’s ‘RAM’ is being used to modify Gavens’s system, and why a POSA would have made any modification.’”).

Second, the deficiencies in Petitioner’s ground compound further into its conclusory treatment of limitation [1h], which requires a data integrity test in which a comparison is performed with “*retained data in the random access volatile memory*.” *See* Petition, 39-40; *see also* Petition, 38-39 (including Petitioner’s cursory and conclusory analysis for limitation [1g]; limitation [1g], which provides the foundation for limitation [1h], requires: “*retain* such stored data in the random access volatile memory”).

In its argument for limitation [1h], Petitioner relies on what it contends would have been “understood” when interpreting Gavens, but Petitioner again fails to provide the requisite obviousness analysis for misinterpreting (or altering) Gavens as Petitioner proposes. *See* Petition, 39-40, 40 (relying only on what “Gavens and its incorporated references *disclose*...”).

Specifically, for limitation [1h], Petitioner appears to rely on a “cache” taught by Gavens and conclusory asserts that this “cache” would be “understood to be RAVM [(RAM)].” Petition, 40 (citing Ex. 1045 (Gavens), 16:46-49). But Petitioner again merely cites teachings from Gorobets 912 and Paley 180 and fails to explain how those references would have led a POSA to misinterpret Gavens’s teachings of a ***non-volatile*** (i.e., non-RAM) “cache.” *See id.*; Ex. 2039, 77 (considering teachings of Gavens, and determining: “Thus, ‘the first portion’ [of Gavens] that ‘serves as a cache for incoming data’ ***is non-volatile memory*** and does not correspond to the claimed ‘random access volatile memory.’” (emphasis added)); *see also* Ex. 2001, ¶¶44-114 (providing, along with PO’s Preliminary Response On The Merits filed concurrently with this brief, a detailed description of the technical weaknesses in Petitioner’s argument, including how Gavens *teaches away* from a RAM-based cache).

For example, Petitioner does not explain what aspect of the claim limitation is missing in Gavens and, correspondingly, does not explain what from Gavens must be modified to arrive at the claim language. And Petitioner also does not explain whether any of the allegedly incorporated references’ RAM is being used to modify Gavens’s system, and why or how a POSA would have been motivated to make any modification. Petitioner fails to perform ***any*** obviousness analysis, which requires, among other things, ascertaining the “differences between the prior art and the

claims at issue.” *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966); *see also In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (“Whether a rejection is based on combining disclosures from multiple references, combining multiple embodiments from a single reference, or selecting from large lists of elements in a single reference, there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination.”).

In denying institution of PGR2024-00047, the Board likewise determined that Petitioner’s failure to justify its ground warranted denial of institution on the merits; the Board explained, “Petitioner does not explain how the teachings of Gorobets [912] and Paley [180] ‘combine with the cited teachings of Gavens’ to yield” what was claimed. Ex. 2039, 71, 76 (considering a claim limitation requiring: “comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the *retained data that was associated with the stored data in the random access volatile memory*” (emphasis added)).

Accordingly, the Petition’s weak merits—which have already been rejected by the Board—weigh heavily against institution. *See also* Ex. 2044, 2 (stating that “The strength of the unpatentability challenge” should be considered in determining whether to discretionarily deny a petition). The arguments underlying Petitioner’s

challenge “ha[ve] already been adjudicated” and the Board should not expend its resources to revisit these arguments here. Ex. 2044, 2 (noting that, in evaluating whether to exercise discretion to deny institution, the Director should consider “[w]hether the PTAB or another forum has already adjudicated the validity or patentability of the challenged patent claims”).

2. The Petition Relies Heavily On Expert Testimony

“The extent of the petition’s reliance on expert testimony” should also be considered in assessing whether to exercise discretion to deny institution. Ex. 2044, 2. This Petition is heavily reliant on expert testimony. Petitioner’s obviousness ground—based on “Gavens *in view of POSITA Knowledge*”—relies on expert testimony to establish what they contend would have been the relevant knowledge of a POSA, including and how a POSA would have artificially reconstructed Gavens to fit the language of the Challenged Claims. *See generally* Petition, 25-42. For example, in its ground for limitation [1e] (including the scattershot citations to the allegedly incorporated references), Petitioner relies on what its expert contends “[a] POSITA would also understand....” Petition, 33; *see also* Petition, 40 (for limitation [1h], relying on expert testimony to argue what would have been “understood” from Gavens). Petitioner’s substantial reliance on expert testimony underscores that these arguments are more appropriately resolved in the Parallel Litigation—further supporting discretionary denial.

3. The Challenged Patent Belongs To A Family Of Patents With Settled Expectations

The “[s]ettled expectations of the parties, such as the length of time the claims have been in force” should also be considered in assessing whether to exercise discretion to deny institution. Ex. 2044, 2. Here, the first four Vervain Patents—including the 300 Patent challenged here—were successfully litigated in the Prior Litigation. *See supra* Sections II.A and II.D. This family of patents, which claims priority to 2011, embodies the inventions of a single inventor, Dr. G. R. Mohan Rao. The longstanding nature of these patents and the settled expectations surrounding Dr. Rao’s inventions further support discretionary denial.

4. Instituting This Petition Would Unnecessarily Burden The Board’s Resources

Finally, Petitioner filed eight separate petitions challenging the eight patents asserted in the Parallel Litigation. The Board has already denied institution of two of those petitions. *See* Exs. 2039, 2041. As a result, only six petitions remain pending. The purpose of discretionary denial is to “allay[] concerns about inefficiency and duplication of efforts.” *Fintiv*, Paper 11 at 6. Instituting six separate PGRs/IPRs to address only some of the issues currently being addressed in the single, mature district court case would be inefficient and an unnecessary expenditure of the Board’s resources.

Thus, all *Fintiv* factors—including multiple additional circumstances—weigh against institution, and the Director should exercise her discretion to deny institution under 35 U.S.C. § 314(a).

IV. CONCLUSION

For the foregoing reasons, the Director should exercise her discretion to deny institution.

Date: May 14, 2025

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies that the word count for the foregoing **PATENT OWNER'S REQUEST FOR DISCRETIONARY DENIAL OF INSTITUTION** is 5,295 words, which is within the limit set in 37 C.F.R. §42.24(b)(1). This word count does not include the table of contents, table of authorities, exhibit list, certificate of word count, and certificate of service. This word count was prepared using Microsoft Word.

Date: May 14, 2025

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CERTIFICATE OF SERVICE

I hereby certify, in accordance with 37 C.F.R. § 42.205, that the foregoing
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